Chapter 1

Introduction

1.1 Background

SiGe heterojuction bipolar transistors (HBTs) were become popular in wireless communication applications in the form of wireless transceiver circuit [1] [2], due to it is provided with the advantage of high cut-off frequency, high breakdown voltage, and low operation voltage. Wireless local area network (WLAN) chipset at 2.4GHz have been announced where the use of SiGe reduced the IC chip count and power consumption by 50%. The SiGe HBT marketplace covers a wide range of product requirements, and is now appearing in virtually all analog and high-frequency market segments. Fig.1-1 is a flow chart of device/circuit/system design, and device model is between the device design and circuit or system. Hence, the quality of device model will directly influence the performance of circuit or system. Besides, it is important to provide an accurate device model to circuit designer. A circuit designer can base on the precise model to optimize the circuit characteristic.

In order to design high-performance HBT circuits and maximize the device performance, more accurate device modeling, especially in the RF range, is indispensable. Most small-signal model parameter extraction methods are based on numerical optimization which fits the parameters to the measured S-parameters. Although this is useful for circuit design, it is difficult to apply this for device parameter analysis, since numerical optimization might result in non-uniqueness and uncertainly of the extracted parameters. Several authors have proposed parameter extraction method which determined most of parameters directly so as to avoid the optimization process [3]-[6]. Schaper et al. [3] reported unique determination process with loop algorithms, which assume the resistance parameters (emitter resistance and

collector resistance) are constant. Besides, Costa et al. [4] proposed a direct parameter extraction method using some test structures to extract parasitic elements so as to obtain the intrinsic device parameters. However, this method needs several test structures to extract parasitic parameters. Pehlke and Pavlidis [5] proposed another direct determination technique of HBT small-signal model parameters from measured S-parameters. This method used numerical optimization for determining the last four parameters which are input conductance, storage capacitance, emitter resistance and emitter inductance.

Recently, several papers have reported small-signal equivalent-circuit parameter-extraction methods for SiGe HBTs [7]-[10] in which the substrate effects have been taken into account. Johansen et al. describe in [7] a direct substrate network parameter extraction technique where feedback signal through the internal circuit elements was neglected. The S-parameters measured with only collector port connected was used in [8], allowing a direct parameter extraction of a three-element substrate network. An alternative parameter extraction approach for substrate network of SiGe HBTs was also proposed in [9], in which the collector-substrate depletion capacitance was directly extracted from measured $\mathrm{Im}(Y_{22}+Y_{21})/\omega$ at low frequency and the substrate resistance and substrate capacitance were extracted from two analytical equations under certain assumption. Finally, Lee et al. proposed a parameter extraction approach [10], in which a new collector-substrate parasitic capacitance was used accounting for the parasitic capacitance arising from the open-short de-embedding procedure. Most of these extraction techniques for the substrate network were based on the use of frequency behavior of $(Y_{22}+Y_{21})$. However, we found that the feedback signal through the internal circuit elements makes $(Y_{22}+Y_{21})$ deviate from the admittance of substrate network and the modeling results may have no physical meaning if the parameters extraction of substrate network is directly performed on the measured $(Y_{22}+Y_{21})$. Therefore, extracting the substrate network parameters, the intrinsic circuit elements of SiGe HBTs should be determined first.

In this thesis, all the circuit elements are extracted directly from the measured S-parameters without any pre-knowledge or numerical optimization. In the extraction of substrate network parameters, we extract the intrinsic circuit parameters first to erase the influence of feedback signal through the internal circuit elements. The proposed extraction procedure was experimentally verified on a SiGe HBT in the frequency range 1-18 GHz [11].

1.2 Organization

There are five chapters in this thesis. In Chapter 2, a new parameter extraction technique for hybrid-π topology HBT small-signal modeling is described. The proposed method is taken the intrinsic circuit elements into consideration in substrate network extraction. In Chapter 3, we extract the small-signal model parameters of a SiGe HBT with different bias conditions. The physical mechanisms, which influence the bias dependence of model parameters, are discussed. In Chapter 4, the model parameters of devices with different geometrical sizes are extracted. A scaling rule for extracted parameters is illustrated. Finally, some conclusions are given in Chapter 5.

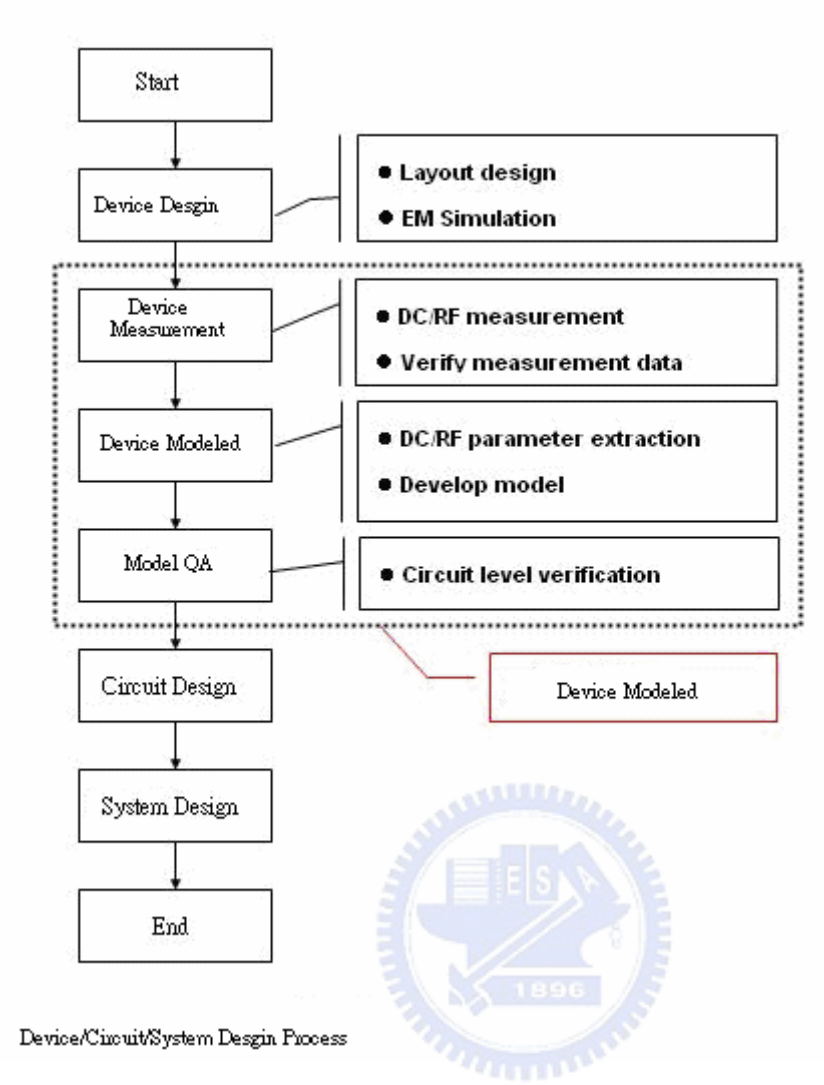

Fig.1-1 Device/Circuit/System design process.