國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

沉積後電漿處理對二氧化鉿金氧半導體結構電特性之影響

The Effect of Post-Deposition Plasma Treatment on The Electrical Characteristics of HfO_2 MOS Structure

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摘 要

當場效電晶體的閘極介電層厚度微縮至1.5 奈米厚時，將產生一些諸如電子穿遂效應等嚴重的問題。因此極需以高介電係數材料取代二氧化矽作為閘極絕緣層，其中二氧化鉿就是目前被認為最有可能取代二氧化矽的材料。本實驗以鋁-二氧化鉿-矽之MIS 電容結構為分析元件。首先利用直流濺鍍法沉積鉿金屬，接著以低溫通氧氣的爐管氧化金屬鉿，而得到氧化鉿薄膜。接下來，試片在氧化後立刻去做各種不同時間的電漿處理，其氣體來源分別是氮氣，一氧化二氮，氧氣。在不同電漿處理條件下的薄膜電性，經由C-V 和I-V 量測得知，並討論二次離子質譜儀的特性圖。另外也藉由磁滯效應、SILC特性、定電壓加壓測試和崩潰電荷分佈量測來討論各種電漿處理條件下元件的可靠度。在這些條件之中，其中以通一分鐘氮氣電漿的樣品的呈現出最大的電容質(增加了50%)，最小的漏電流(兩個數量級的下降)，以及優異的可靠度。這是因為氮氣電漿處理會抑制介面氧化層的成長，所以其電容

值在被電漿傷害破壞前，會因修補介面的效應而持續的增加。另一方面，雖然一氧化二氮和氧氣電漿處理在較短的製程時間內依然是可行的改良電性的方法，但由於其容易促生額外氧化層的特性，使得其電容值還是比氮氣電漿處來得小。

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ABSTRACT

When the MOSFET gate insulator is scaled below 1.5 nm, some serious problems such as direct electric tunneling will occur. Therefore, high dielectric constant material is very desirable to replace SiO_2. Hafnium oxide is a most promising material for future MOSFET gate oxide applications. In this study, we used Al-HfO_2-Si MIS capacitor as our analysis device. First, we used DC sputter system to deposit hafnium metal and then proceeded with furnace under oxidation at low temperature to prepare HfO_2 thin film. After oxidation process, we had an additional plasma treatment with N_2, N_2O, or O_2 plasma for different process durations. The electrical characteristics of the film under different oxidation conditions were discussed by C-V and I-V curves. Moreover, the SIMS (Secondary Ion Mass Spectrometer) profile was also analyzed. The reliability of the film under different plasma treatment conditions were discussed by hysteresis effect, SILC (Stress Induced Leakage Current) profile, CVS (Constant Voltage Stress) test, and Q_{BD} (charge-to-breakdown) distribution. Among these conditions, the sample treated by N_2 plasma for 1 minute represents the largest capacitance (50% increasement), lowest leakage current (2 order reduction), and excellent reliability. Since the N_2 plasma

treatment can suppress the the formation of interfacial oxide between the high-k/Si interface, the capacitance of the high-k dielectric can take advantage from the N_2 plasma treatment before the plasma damage occur. On the contrary, the N_2O and O_2 plasma can improve the interface characteristics in short period, the property that they are easy to form an additional oxide layer in the high-k/Si interface will degrade the dielectric's capacitance when compared with N_2 plasma treatment

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Chapter 1

Introruction

1.1 Background

According to the famous ”Moore’s Law”, proposed by Gordon Moore in 1965, which states that the number of transistors on integrated circuits doubles every 18 months, pursuing better performance with lower cost is needed. For decades, the progress in the IC industry more or less follows this law. On the other word, ”Moore’s Law” is the basis for the overwhelmingly rapid growth of the computing power. In order to achieve the goal, the scaling down of the device dimension is an inevitable tendency.

In terms of the first order current-voltage relation, the driving current of a MOSFET can be given as

$$I_{dsat} = \frac{1}{2} C_g \mu_n \frac{W}{L_{eff}} \left(V_{GS} - V_t\right)^2 \quad \textbf{(1.1)}$$

$$C_g = \kappa \varepsilon_0 \frac{A}{t_{inv}} \quad \textbf{(1.2)}$$

Where V_{GS} is the applied gate to source, L_{eff} is the effective channel length, W is the channel width, V_t is the threshold voltage, μ_n is the mobility for electrons, C_g is

the gate capacitance, κ is the dielectric constant, ε_0 is the permittivity of free space and t_{inv} is the electrical film thickness. From the formula, we know that with reduced threshold voltage, smaller effective channel length, and increased gate capacitance as well as gate-to-source voltage, the device can achieve better current driving ability. Of course, it can also have higher device density, which means a better performance and much more transistors on the chip. However, a large V_{GS} will degrade the reliability while too small V_t will result in statistical fluctuation in thermal energy at a typical operation circumstance of up to 100℃. So a bigger C_g and shorter L_{eff} will be needed to maintain device performance.

1.2 The Need to Use High-k Dielectric

Over the past 30 years, SiO_2 has served its role as a perfect gate dielectric, and has been scaled down from a thickness of 100nm to 1.2nm at 90nm process technology node today, in order to gain a large C_g and a higher density. In 1999, Schulz in Nature predicted that, in order to keep up with the roadmap goal, in 2012 the thickness of gate oxide is slated to scale down to 1nm, which represents only five silicon atoms thick (see Fig 1-1) [1]. Thus the direct tunneling current which depends strongly on film physical thickness will increase to an unacceptable range, resulting in a high power dissipation and heat .we can see the machine from(1.3).

$$I_{DT} \propto \exp - \left(\sqrt{\frac{2mq\phi}{\left(h/2\pi \right)^2}} T_{phys} \right) \qquad \textbf{(1.3)}$$

We can see from Fig. 1-2, Lo et al. find that the gate oxide can be scaled down to

2nm before exceeding the limit of 1A/cm^2 from the viewpoint of allowable stand-by power dissipation. Below 2nm, however, the oxide tunneling current will quickly becomes problematic. For easily sensing the seriousness of leakage problem: as SiO_2 thickness is reduced, leakage current increases exponentially (~10×/2Å)[2]

On the other hand, we can take the view of Roadmap of gate dielectric. Fig. 1-3 shows the high-performance logic scaling-up of gate leakage current density limit and of simulated gate leakage due to direct tunneling. In 2006, the EOT (Effective Oxide Thickness) is about 1.1 nm and the leakage current density of the oxynitride is below the leakage limit line. However, after 2008, the EOT is below 1.0 nm and the oxynitride is incapable of meeting the limit on the gate leakage current density. Fig. 1-4 shows the low operating power (LOP) scaling-up of gate leakage current density limit and simulated gate leakage due to direct tunneling. In 2006, the EOT is only 1.3 nm but the leakage current density of the oxynitride is still below the limit line because the application of high-performance logic could endure larger gate leakage current. However, after 2010, the oxynitride couldn't be used for high-performance logic anymore. Fig. 1-5 shows the Low Standby Power scaling-up of gate leakage current density limit and simulated gate leakage due to direct tunneling. About this case we can notice that the oxynitride couldn't be used for Low Standby Power device anymore after 2007. Table 1-1 is the roadmap of 2004 ITRS (International Technology Roadmap for Semiconductor) for the high-performance logic technology. After 2008, the requirement of EOT even reduces to less than 1 nm. It would be a big challenge because the leakage current is too large to be acceptable for SiO_2 under such a thin thickness

Because the leakage current is related to the physical thickness of the gate oxide from (1.3), we can notice that if we make the gate dielectric thicker and still maintain

the same Cg value, the leakage current problem would be solved. This is mean that there will be a new material to replace traditional SiO_2gate dielectric. In order to maintain the same C_g value, (1.2) can be rewritten as follows:

$$t_{high-k} = \frac{k_{high-k}}{k_{ox}} t_{eq} = \frac{k_{high-k}}{3.9} t_{eq} \quad \textbf{(1.4)}$$

where the $\mathbf{t_{eq}}$ term represents the theoretical thickness of SiO_2. So by increasing the gate dielectric constant, the same equivalent oxide thickness can be obtained with a thicker physical thickness, which can reduce the gate leakage current (i.e., direct tunneling), without sacrificing the performance. Consequently, SiO_2gate dielectric needs to be replaced by the material with high dielectric constant.

1.3 The Choice of High-k Materials

High-k gate materials can maintain the same EOT with thicker physical thickness, and is therefore expected drastically reduced direct-tunneling current. From Fig1-6, the increased physical thickness significant reduces the probability of tunneling across the insulator, and hence, reduces the amount of off-state leakage current density. [3]

The relationship between dielectrics constant and thickness is followed:

$$EOT = \frac{k_{ox} \times t_{high-k}}{k_{high-k}} \quad \textbf{(1.5)}$$

There are many potential candidates for replacing SiO_2, such as HfO_2, ZrO_2,

Al_2O_3, Ta_2O_5 and so on. Which one will emerge as the winner for replacing the silicon dioxide? Since over the past three decades, SiO_2 has served as an ideal gate dielectric, its several advantages, such as being amorphous phase through the whole integration processing, high quality interface, and good thermal stability, can indeed serve as a good guide of choosing high-k material. So, an ideal gate dielectric should meet the following requirements below:

1.3.1 Physical Properties

(a) Thermodynamic stability in direct contact with silicon,

Preserve capacitance of gate stack after processing.

(b) Film morphology (amorphous) and stable process compatibility,

In the VLSI process, the thermal budget is an important concern since high temperature changes dielectric phase. Once the gate dielectric material has transformed to polycrystalline from amorphous phase, the large grain boundaries would serve as leakage path, and induce large leakage current.

(c) Suitable high k value (12~60),

A suitable k value is indispensable. Those with not enough high k value could not satisfy (1.3) to lower the leakage by increasing physical thickness. While those with too high a k value, in general, would suffer from thermal stability issues and larger fringing field.

(d) Wide bandgap with conduction band offset > 1eV,

It is found that most of the high-k materials do not have wide enough bandgap. In contact with silicon and gate electrode, the bandgap is closely related to the barrier height for carrier transport. Too low a bandgap will lead to intolerably high gate leakage (leakage current ~exp(-$\triangle E_c$)) [4].

(e) Gate material compatibility

Materials such as metal gate, and metals have been considered for better controllability and better performance.

1.3.2 Electrical Properties

(a)Low interface state density (D_{it}< $5x10^{10}$ /cm^2-eV^{-1}), and SiO_2-like mobility,

The interface would affect the carrier mobility in the channel, and from (1.2), mobility degradation is related to poor current drivability. In high-k, there are so many sources that would reduce mobility, such as fixed charge, remote phonon, interfacial dipoles, remote surface roughness, surface roughness and phase separation crystallization. And most of them can be avoided by improving process technology.

(b) T_{inv}<1nm,

(c) J<10^{-3} A/cm^2 @ V_{DD},

(d) V_{FB} and hysteresis < 20mV,

(e) No C-V dispersion,

(f) Reliability issue.

To serve as a new gate dielectric, we must also take into consideration electrical reliabilities, such as stress-induced leakage current (SILC), time dependent dielectric breakdown (TDDB), hot carrier aging, bias temperature instability and charge trapping issues [5].

1.3.3 The Reason Why We Choice HfO_2

There are many kinds of high-k materials, including Al_2O_3, Y_2O_3, Ta_3O_5, TiO_2, ZrO_2 and HfO_2 etc. Table 1-2 lists basic characteristics of several high-k dielectrics. Unfortunately, many high-k materials such as Ta_20_5, TiO_2, $SrTiO_3$, and $BaSrTi0_3$ are thermally unstable when directly contacted with silicon [6] and need an additional barrier layer which may add process complexity and impose thickness scaling limit. Also, materials with too low or too high dielectric constant may not be adequate choice for alternative gate dielectric application. Ultra high-k materials such as STO or BST may cause fringing field induced barrier lowering effect. [7] Materials with relatively low dielectric constant such as $A1_2O_3$ and Y_2O_3 do not provide sufficient advantages over SiO_2 or Si_3N_4 [8].

Among the medium-k materials compatible with silicon, oxides of Zr and Hf are attracting much attention recently. Especially, Hf forms the most stable oxide with the highest heat of formation (ΔHf = 27l Kcal/mol) among the elements in IVA group of the periodic table (i.e. Ti, Zr, Hf). Unlike other silicides, the silicide of Hf can be easily oxidized [9]. HfO_2 possesses a dielectric constant of up to 25 [10], a large bandgap of 5.7 eV with sufficient band offset of larger than 1.5 eV [11], and well thermal stability in contact with silicon [12]. Fig 1.7 shows HfO_2 is the most suitable material about the struggle between dielectric constant and bandgap. HfO_2 is very resistive to impurity diffusion and intermixing at the interface because of it's high density (9.68 g/cm3) [13]. In addition, HfO_2 is the first high-k material showing compatibility with polysilicon gate process [14]. These properties make HfO_2 one of the most promising candidates for alternative gate dielectric application. [15]

1.4 The Challenges of High-k dielectrics

Recently, HfO_2-based insulator become promising candidates for the

generation of sub-1.5-nm gate dielectrics. Although several groups have demonstrated in recent years the excellent electrical properties of MOS capacitors featuring HfO_2-based gate dielectrics, [16~18] there still remain many challenging issues, such as the exists of the interfacial layer which causes the C value lower and degrades the mobility [18] in MOSFET devices. Besides these, traps in high-k gate dielectrics have been demonstrated as another issue of concern because their presence can cause threshold voltage instability [20 common 21] and a degradation in their reliability [22], such as hysteresis caused by charge-trapping [23]. It is investigated that the reasons of threshold voltage instability likely be Fermi-level pinning [24].The results indicate that pinning occurs due to the interracial Si-Hf bonds for HfO_2. Finally, the high temperature of activation process introduce to thermal stability problem. For example, crystallization may let leakage current issue become worse because of providing leakage path. In brief, we summarize the challenge if High-k dielectrics as below:

(a) extra interfacial layer growing lower the C value

(b) the degradation of mobility

(c) threshold voltage instability and hysteresis issue

(d) charge-trapping issue

(e) thermal stability problem

In a word, High-k dielectrics although provide a low leakage current and satisfied C value, but the reliability issues can not be ignorable. So, it needs some

treatments to overcome these problems.

1.5 Plasma Nitridation

According to traditional view of improving SiO_2 device performance, we can find that nitridation is a common method to improve the interface. [25] Property with the result that there is often N_{it} or D_{it} in the interface, imperfect bonding of interface often makes the characteristic of the device deteriorate. Such as charge will be trapped by the defects of the interface, it produce flat band voltage shift and also reduce mobility. Another shortcoming is that these dangling bonds will easily bond with oxygen atom in the following high temperature environment. The extra chemical reaction will let the interfacial oxide growth, and it will reduce the C value because of the lower dielectric constant. Moreover, the quality of interfacial layer formed by oxidation is worse, and there still will be the more problems of charge trapping.

In order to solve these problems, nitridation treatment can let the atom of nitrogen bond with these dangling bonds and fix it while entering the interface layer, and then improve the stability and reliability of interface. Consequently, nitridation treatment is a workable solution to improve interface quality

As we note before, the question about using high-k materials to replace SiO_2 is that there are too many defects in the interface to cause reliability degradation. Therefore, when we use high-k materials, it is consider that nitridation treatment is a more suitable way to improve reliability and thermal stability of device. These kind of treatment have already used in some relevant references. [26] [27] Among them, someone take nitridation treatment at high temperature, others take so-called plasma

nitridation . According to [28], we can understand that the effect of plasma nitridation is better than thermal nitridation. The reason is that high-k materials are afraid of high temperature. As long as the temperature reaches certain degree, we can see phenomenon of crystallization. The crystallization of dielectric will raise leakage current substantially, because it offers the path of leahage. On the other hand, the meaning of plasma nitridation is to activate the source gas first. The high activation energy of radical will provide better mend which is better than nitridation at high temperature. For all these reasons, we adopt plasma nitridation in present experience.

1.6 Thesis Organization

Following chapters in the thesis are primarily organized as follow：

In chapter 2, we make a description of experimental details. DC magnetron sputtering system is used to deposit hafnium on silicon surface.

In chapter 3, we discuss the characteristics of ultra-thin HfO_2 insulator by Metal-Insulator-Semiconductor (MIS) capacitors.

In chapter 4, we discuss the reliability of ultra-thin HfO_2 insulator by Metal-Insulator-Semiconductor (MIS) capacitors.

In chapter 5, we make the conclusions for this thesis and provide some suggestions for future work.

Chapter 2

Experiments of Al/HfO_2/Si MIS Capacitor

2.1 MIS Capacitors Fabrication Process

In this thesis, Al/HfO_2/Si MIS capacitor were fabricated to study ultra thin HfO_2 gate dielectrics. Figure 2-1 shows the fabrication flow of this experiment. The starting wafer was four inch (100) orientated p-type wafer with boron doped . It was one side polished and its resistivity was 5~10 ohm-cm.

After standard initial RCA cleaning, wafers were put into chamber and grew a hafnium layer with DC magnetron sputtering system. The thickness of as-deposit hafnium thin films was 20 Å which was read by the sensor inside the sputtering system. During sputtering, chamber pressure was maintained around 7.6×10^{-3} torr and the flow rate of Ar was 24 standard cubic centimeters per minute (sccm). Subsequently, samples were oxidized in furnace system at 400 ℃ for 15 minutes with oxygen flow rate 5000 sccm. The reasons why we adopt this two-step method to prepare HfO_2 films will be shown at the next section 2.2.

After the HfO_2 films were prepared, some samples were subjected to an additional plasma treatment at the substrate temperature of 300 ℃ while the pressure was 100 mTorr and the plasma power was 1 W/cm^2.The plasma treatment conditions were in pure N_2, N_2O, or O_2 plasma for 10 second, 30 second, 1 minute, 3 minute, or

5 minute respectively and the flow rate were 100 sccm. After that, pure aluminum films were thermally evaporated on the top side of wafers.

Mask defined the top electrode. Then, we used wet etching to etch undefined Al and HfO_2 films. After patterning, backside native oxide was stripped with diluted HF solution, and Al was deposited as bottom electrode. The detailed fabrication process flow was listed as follows.

1. Initial RCA cleaning.

2. DC magnetron sputtering hafnium 20 Å.

3. Thermal oxidize hafnium in furnace in an O_2 ambient at 400 ℃ for 15 minutes.

4. Plasma treatment with N_2, N_2O, or O_2 plasma for 10 second, 30 second, 1 minute, 3 minute, or 5 minute respectively

5. Thermally evaporate 5000 Å aluminum as top electrode.

6. Mask：define top electrode and then wet etch undefined Al and HfO_2 films.

7. Strip backside native oxide and coat 5000 Å aluminum as bottom electrode.

After the Al/HfO_2 /Si MIS capacitors were prepared, we used semiconductor

parameter analyzer (HP4156A) and C-V meas urement (HP4284) to analysis electric characteristics (i.e. I-V, C-V, EOT, leakage current density etc.). Then we tested their reliability, including stress induced leakage current (SILC), constant current stress(CCS), constant voltage stress (CVS), Hysteresis effect.

2.2 Sputtering System

There are various methods to prepare high-k thin films, such as chemical vapor deposition (i.e. ALCVD, MOCVD, PECVD etc.) [29] [30] [31] and physical vapor deposition (i.e. Sputtering, PLD etc.) [32]. About HfO_2 films, the usual methods are ALCVD, MOCVD and Sputtering. Comparing with these methods, we choice sputtering system to despite HfO_2 films because the advantages of the DC magnetron sputtering are simple and cheap. In addition, the HfO_2 film prepared by CVD system easily contains organic impurities and oxygen vacancies inside. This will cause leakage current through Frenkel-Pool effect or trap assisted tunneling [33]. Less contaminants are produced by the process of the sputtering because there are no other unnecessary chemicals. However, the uniformity of the DC sputtering is worse than that of the ALCVD and the MOCVD in 12 inch diameter Si wafer. Further, sputtering in an O_2 ambient easily produces SiO2 interfacial layer. Therefore, we decide to sputter Hf in an Ar ambient only. After pure hafnium has been deposited on Si substrate, we put the wafer into furnace system with O_2 ambient at low temperature for oxidation. At some low temperature (400℃), Si will not react with O_2 to form the SiO_2. Then, the HfO_2 film is prepared without SiO_2 interfacial layer.

Four inch high purity hafnium target was used to deposit thin film by DC magnetron sputtering system. The sputtering conditions were as follows. In the DC sputtering process chamber, the wafers were mounted on a face-down holder which

can rotate during deposition to increase film uniformity. The system was pumped down to 2×10^{-6} torr first. This process made the chamber clean enough and thus decreased the impurity of the deposited hafnium film. Then the deposition pressure was controlled at 7.6×10^{-3} torr. Before started to deposit hafnium, the surface of the hafnium target was treated by low power pre-sputtering cleaning for ten minutes. The inert gas source was argon (Ar) and its flow rate was 24 sccm. It has heavy atomic weight and could be served as a heavy iron to knock down the hafnium atoms on the target surface. Therefore, the hafnium atoms could be sputtered onto the wafers. The thickness of the deposited hafnium was read by the sensor inside the sputtering system. Then, the oxidation process of hafnium was performed by furnace system. The DC magnetron sputtering power was set at 100 W and the corresponding deposition rate was 0.2 Å/s. The thickness of hafnium films was 20 Å.

2.3 Furnace System

After hafnium had been deposited on silicon, we need an oxidation process to make it become hafnium dioxide. These Si wafers deposited with hafnium films were immediately loaded into furnace tube just as the sputtering process was finished. To start with, the tube temperature was set at 400 ℃ and sufficient N_2 gas was purging continuously. After the tube temperature was stable in five minutes letter, N_2 gas was closed and O_2 gas was introduced. The oxygen gas flow rate was set at 5000 (sccm). We provided sufficient oxygen gas and proper time to oxidize these films.

2.3 Plasma treatment system

When the oxidation process of hafnium performed by furnace system was

finished, some samples were subjected to an additional plasma treatment in order to improve the electrical properties of gate dielectric. There were various source gas and process time which were N_2, N_2O, or O_2 plasma for 10 second, 30 second, 1 minute, 3 minute, or 5 minute as the experiment conditions. Parallel plate high-density plasma reactor employing an ICP source was a single-wafer treated and computer-controlled system.

Fig. 2.2 illustrates ICP system that was used in this experiment. 13.56 MHz RF power was coupled to the top electrode through a matching network. After the sample load to reactor, the system was pumped down to keep the chamber clean enough. Subsequently, the source gas was become radical by the plasma system, as the chamber pressure was 100 mTorr and the substrate temperature was 300℃ so that to achieve the goal of low temperature process. The power of working plasma was kept constant at 1W/cm^2 and the flow rate of source gas was 100 sccm. While the process of plasma treatment was finished, these samples were brought to deposit Al for metal gate immediately because the effect of plasma treatment would be decrease probably.

Chapter 3

Electrical Characteristics of Al/HfO2/Si MIS Capacitors

3.1 Capacitance-Voltage Characteristics

In order to measure the C-V characteristics of our MIS capacitors we used HP2484A LCR meter in our experiments. We swept the gate bias from inversion region to accumulation region to obtain the curve at the frequency of 10 kHz. There are three kinds of plasma treatment with different source gas (i.e. N_2, N_2O, and O_2) and they were treated for different process time (i.e. 10 sec, 30sec, 1min, 3min, and 5 min). Firstly, the relationship of difference process time in one kinds of plasma treatment will be discussed. Then compare with the effect of different source gas.

Fig. 3-1 reveals the capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time. The capacitor treated for 1 minute shows the maximum capacitance among these conditions of process time. In addition, the capacitor treated for 10 second and 30 second both show the good C values which are larger then the capacitor with the condition of no treatment. This phenomenon indicates that the N_2 plasma treatment was workable to improve the capacitance. Maybe it is caused of the intensifying of the interface structure or high-k bulk itself. The growing of interfacial oxide has also been restrained. On the other hand, the capacitance treated for 5 minute is very low and it is

even lower than the no-treated sample. It is seems that the plasma damage occur and then destroy the structure of high-k capacitance when the duration of plasma treatment is too long. The degradation of capacitance also can be found at the case of 3 min-treatment time, although the C value is still larger then the case without plasma treatment.

Fig. 3-2 shows the capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time. Just like the group of N_2 plasma treatment. The improvement of capacitance and the damage cause by excessive plasma treatment both can be seen. At this condition, the capacitance treated with N2O plasma treatment for 10 second shows the largest value. Then, the capacitance becomes worse and worse with the increase of the treatment time. By the way, the samples besides 3 min and 5 min all perform well about larger capacitance then the sample without treatment. It is indicated that N_2O plasma treatment is also a practicable method to improve the capacitance-voltage characteristics of HfO_2 gate dielectrics.

Fig. 3-3 shows the capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with O_2 plasma treatment for different process time. The experiment of plasma treatment only with oxygen radical is wanted to see if it is still existed the improvement of capacitance, even if without nitridation. Consequently, it is shown that the capacitors treated for 10 sec and 30 ses have larger capacitances than the no-treated sample, especially for 30ses provided the maximum capacitance. Take the view of 1min condition, its capacitance has begun lower than the sample which is no treated. As the same time of 1min conditions, the other kinds of treatments still remain good capacitances then no-treated sample. So it can be know

that there are some reasons besides plasma damage occurred at the condition of 1min treatment. It is suggested that plasma treatment with oxygen radical may cause additional oxidation followed by repairing of the interface structure. Because the interfacial oxide provides lower k value, the total capacitance was be effected and become lower.

Fig. 3-4 shows the capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for 1 min, N_2O plasma treatment for 10 sec, and O_2 plasma treatment for 30 sec. It is indicated that the capacitance treated with N_2 plasma treatment for 1 min shows the most excellent value (i.e. 50% increasing about capacitance). Among these samples, the capacitance treated with O_2 plasma treatment is the worst because the growing of interfacial oxide is unavoidable while the oxygen atoms become radical and enter the interface. Besides this, the reason why the sample treated with N_2O plasma has lower capacitance then N_2 plasma treatment is complex.

It is may be the growing of interfacial oxide made the capacitance degradation. Thus, the capacitance improvement by interface repair was easily eliminated by the interfacial oxide which has lower k value. So, the capacitance becomes degradation when the process time only exceeds 10 second.

3.2 Current-Voltage Characteristic

Fig. 3-5 shows the J-V characteristics of p-type HfO_2 capacitors treated by N_2 plasma with different process time from 0 V to -1 V. We observed that the gate leakage current density is suppressed while treatment conditions are 10sec, 30sec,

1min, and 3 min. It is indicated that N_2 plasma treatment supply an effective barrier against the leakage current. The lower leakage shows that the weak structure of interface must be fixed by the plasma nitridation, especially for 1 min capacitor which both has the lowest leakage and largest capacitance value from Fig. 3.1. Gate leakage current density of no treatment insulator at VG = 1 V is about 3.25×10^{-6} A/cm^2. From fig.3-5, however, gate leakage current density of the capacitor treated for 1 min N2 plasma at VG = -1 V is only about 1.35×10^{-8} A/cm^2. It has less gate leakage than no treatment insulator about 2 orders. Furthermore, we notices that the 3 min capacitor although has little leakage, its capacitance has become degradation. This is an interesting phenomenon. Even though the plasma damage has begun to reduce C value, the amount of leakage current is still kept very well. It means that the capacitance value is more easily affected by plasma damage than leakage current.

Fig. 3-6 shows the J-V characteristics of p-type HfO2 capacitors treated by N_2O plasma with different process time from 0 V to -1 V. After N2O plasma treatment, we can see the reduction of leakage current in contrast of no treatment samples. It is worthy to be noticed that the capacitors treated by 10 sec N2O plasma which has the best C value also performs a low leakage current about 5.97×10^{-8} A/cm^2. In addition, we find that the leakage currents of 3 min and 5 min treatment are larger then 1min. But for counterpart, they are not larger then no treatment sample. Relative to the case of N_2 plasma, we can see that the level of leakage current increasing obviously mitigate. It is possibly due to the additional oxidation layer formed by oxygen radical. The interfacial oxidation layer will let the dielectric thicker to prevent from gate leakage.

Fig. 3-7 shows the J-V characteristics of p-type HfO_2 capacitors treated by O_2

plasma with different process time from 0 V to -1 V. All of the samples depict the presence of the reduction in leakage current. It is indicated that there are not only the effect of improving interface quality but also another effect to suppress the leakage current in the case. According to the discussion about Fig. 3-3, we know that the growth of interfacial oxide layer will decrease the C value. Now the interfacial layer introduces a hard barrier to suppress leakage current. Consequently, the leakage current all displays a lower value including the capacitor treated by O_2 plasma for 5 min even if it is must be damaged by plasma.

Fig. 3-8 shows the J-V characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for 1 min, N_2O plasma treatment for 10 sec, and O_2 plasma treatment for 30 sec. By the compare of the samples which has the best capacitance in their own gas, we can realize the most suitable treatment condition which both has the best capacitance and lowest leakage current. It is showed that the N_2 plasma treatment for 1 min is the best one. It is proved that without thick oxidation layer, it can also reach the smallest leakage current when there is enough long-time treatment.

3.3 Summary and SIMS profile

In order to deeply realize the effect of the plasma treatment, we take SIMS (Secondary Ion Mass Spectrometer) analysis to verify the phenomenon observed from CV and JV curve. Fig. 3-9 and Fig. 3-10 show the SIMS profiles of different plasma treatment conditions. Fig. 3-9 shows the counts of Hf-N bonds with different conditions which are N_2 for 1 min, N_2O for 10 sec, and O_2 for 30 sec. And Fig. 3-10 shows the counts of oxygen secondary ion. These three samples which show good electrical characteristic are the best process time in their own gas conditions

respectively. So we take these three samples to do SIMS analysis. First, from the Fig. 3-9 and Fig. 3-10 the sample of N_2 for 1 min shows the most Hf-N bonds and the less oxygen concentration. This explains why the sample of N_2 for 1 min has the best C value. Moreover, it is the evidence of the oxidation suppression by N_2 plasma treatment compared with no treatment sample. With the proof we can understand why the sample of N_2 for 1 min has the best C value and less leakage: the suppression of oxidation and the Hf-N bonds which appear at the interface fix the interface structure and strengthen it.

On the other hand, although the sample of N_2O for 10 sec shows a mount of Hf-N bonds at interface, there is still oxidation at interface so that the sample shows the less C value compared with N_2 plasma treatment. However, if we take a look at the sample of O_2 for 30 sec, we can find that the oxidation phenomenon is more serious so that its C value is the less.

As a consequence, the N_2 , N_2O, and O_2 plasma treatment all shows better electrical properties than no treatment sample. Furthermore, the N element and O element all can fix the interface and promote the electrical properties include of CV curve and JV curve. But for the reason of oxidation caused by oxygen radical, the N_2O and O_2 plasma treatment samples shows the lower C value. Just because the oxidation phenomenon, the films will become thicker so that the plasma damage will not easily effect the leakage current profile.

Chapter 4

Reliability of Al/HfO2/Si MIS Capacitors

4.1 Hysteresis

The name of Hysteresis was borrowed from electromagnetics. It is means that when a ferromagnetic material is magnetized in one direction, it will not relax back to zero magnetization when the applied magnetizing field is removed. It must be driven back to zero by the additional opposite direction magnetic field. If an alternating magnetic field is applied to the material, its magnetization will trace out a loop called a hysteresis loop. [34].

The hysteresis phenomenon is similar in the C-V curve of the MIS capacitor device. When we apply a voltage in opposite direction, it will not fit the original C-V curve measured previously. It is due to the traps of interface which can trap charges to influence the flat band voltage and C-V curve. [23] Fig. 4-1 shows the hysteresis of p-type HfO_2 gate dielectrics treated without plasma treatment. Fig. 4-2 shows the hysteresis of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time. Hysteresis of p-type HfO_2 capacitors are changed with the increase of plasma treatment time. First, about the case of 10 sec and 30 sec we can see the hysteresis happened. When the treatment time has achieved 1min, the hysteresis is suppressed by means of the fixing ability at the interface. Until the time continues for 3 min the hysteresis becomes worse again and it attributes to plasma damage.

Fig. 4-3 shows the hysteresis of p-type HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time. The tendency of hysteresis is similar with the case of N_2 plasma treatment. Fig. 4-4 shows the hysteresis of p-type HfO_2 gate dielectrics treated with O_2 plasma treatment for different process time. It also shows a likely tendency. As a consequence, the plasma treatment can improve the reliability of hysteresis for the shorter process time for fear of the plasma damage brought by long process duration. Among these samples, we can find that the hysteresis of N_2 plasma treatment for 1 min is the smallest. Therefore, we can speculate that the quality of interfacial oxide is not very well so that the charge was be trapped at the interface and introduce hysteresis.

4.2 Stress Induced Leakage Current (SILC)

In order to investigate the reliability of MIS capacitor device, the stress induced leakage current is a common experiment. The machine about SILC is the stress induced trap density in the bulk in thin film. The trap density introduce new leakage path. Fig. 4-5 shows the SILC curve of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time. After the stress of constant voltage (1V) for 30 second, the gate leakage current become larger then before. The degree of leakage current degradation can be judged for the reliability of MIS capacitor. From Fig. 4-5, it displays the improvement of SILC compared with no-treated capacitor. Second, it is considered that the SILC of 1 min-treated sample which has the largest C value and the lowest leakage shows a very small degradation. On the other hand, it is also can be noticed that the SILC of 3 min-treated sample become worse due to the plasma damage.

Fig. 4-6 and Fig. 4-7 display the SILC curve of p-type HfO_2 gate dielectrics treated with N_2O plasma treatment and O_2 plasma treatment respectively. They all show the distinct improvement as long as they are treated with plasma treatment. So the plasma treatment including of N_2, N_2O, and O_2 as source gas can intensify the reliability of devices to suppress SLIC. Fig. 4-8 shows the SILC compare of HfO_2 gate dielectrics treated with N_2 plasma treatment for 1 min, N_2O plasma treatment for 10 sec, and O_2 plasma treatment for 30 sec. The sample treated by N_2 plasma treatment for 1 min shows the smallest SILC degradation because of it's best improvement of interface quality.

4.3 Constant Voltage Stress (CVS)

To study the reliability of HfO_2 film, stressing the film with a constant voltage or a constant current are two common methods. The machine about CVS is the charge trapping by the interfacial trap density which is caused by stress for long time. Furthermore, the mount of charges cause more interface trap density and from new leakage path to add leakage. In our experiments, we use constant voltage stress (CVS) to test the reliability of HfO_2 film. Fig. 4-9 shows gate current shift of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time as a function of stress time during Vg = 1 V CVS stress. From the condition of 10 sec to 1min, the current shift is smaller and smaller. Then the current shift begins to become great by the damage of plasma at the process time of 3 min. Fig. 4-10 shows gate current shift of p-type HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time as a function of stress time during Vg = 1 V CVS stress. It has similar behavior about the trend. Fig. 4-11 shows gate current shift of p-type HfO_2 gate dielectrics treated with O_2 plasma treatment for different process time as a

function of stress time during Vg = 1 V CVS stress. While the 30-sec treated sample presents the lowest current shift, the 1-min treated sample become to be destroyed by the plasma damage. Fig. 4-12 shows the CVS compare of HfO_2 gate dielectrics treated with N_2 plasma treatment for 1 min, N_2O plasma treatment for 10 sec, and O_2 plasma treatment for 30 sec. It is verified that the sample using by N_2 plasma treatment for 1 min has the best quality of thin film.

4.4 Charge to Breakdown (Q_{BD})

Another important issue of reliability is to investigate the breakdown behavior of the gate dielectrics. As long as we inject large number of charge by the stress at constant voltage or constant current for a long period, we can find the breakdown profile and calculate the count of Q_{BD}.

Fig. 4-13 shows the charge-to-breakdown characteristics (Q_{BD}) of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time. The charge to breakdown characteristics was measured at a constant current of -1 A/cm^2. As we respect, the capacitor treated for 1 min shows the larger Q_{BD} and it means that the capacitor more hardly begins to breakdown. Fig. 4-14 shows the charge-to breakdown-characteristics (Q_{BD}) of p-type HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time. Although the capacitor treated for 10 second shows the largest Q_{BD}, the capacitor treated for 1 min has become degradation. Fig. 4-15 shows the charge-to-breakdown characteristics (Q_{BD}) of p-type HfO_2 gate dielectrics treated with O_2 plasma treatment for different process time. Like CVS curve, the capacitor treated for 30 sec shows the best characteristics compared to other process time. And then, we try to compare the three plasma treatment process of

different source gas. Fig. 4-16 shows the charge to breakdown characteristics (Q_{BD}) of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for 1min, N_2O for 30 sec, and O_2 for 30 sec. It is indicated that the sample of N_2 plasma has larger Q_{BD} then that of other plasma treatment. We thought that it is because of well structure of interface fixed by N_2 plasma for a long time.

Chapter 5

Conclusions and future work

5.1 Conclusions

In this thesis, we performed the post-deposition plasma treatment to enrich the HfO_2 film quality. The plasma treatment conditions are N_2, N_2O, and O_2 plasma for 10 sec, 30 sec, 1 min, 3 min, 5 min individually. Several important phenomena were observed and summarized as follows.

First of all, improvement in the electrical characteristics of Al/HfO_2/Si MIS capacitors using plasma treatment has been demonstrated in this work. ALL of the plasma treatment can promote the electrical characteristics and reliability until the plasma damage happened. Among these treatments, the sample using N_2 plasma for 1 min represents a fairly great improvement, such as good capacitance (50% increasing), reduced leakage current (2 order reduction). It is showed that the

formation of interfacial layer has been suppressed and the weak structure of interface has been repaired by N_2 plasma respectively. With the analysis of SIMS profile, it can be demonstrated. Besides, the sample treated by N_2 plasma for 1 min also shows an excellence promotion about reliability issue, such as smaller hysteresis (< 1 mV), less SILC, better CVS curve, and larger Q_{BD}. These advancements were ascribed to the good interface quality.

On the other hand, the N_2O and O_2 plasma treatment also provide a good effect on electrical characteristics although most samples are still worse than that of N_2 plasma treatment. The reason is that the samples using N_2O and O_2 plasma treatment will introduce oxygen bonding to from additional interfacial layer so that the capacitance will be decreased. But for another hand, the thicker oxidation layer becomes a good resistance against leakage current even if the plasma damage has begun to occur. Therefore, we can find that these samples show lower leakage current at the process conditions of 3 min and 5 min even if their capacitance has been seriously degraded by plasma damage.

Finally, in this thesis, the point we focus on is the improvement of capacitance. The treatment of N_2 plasma for 1 min is the best condition because the capacitance has 50% increasing. Simultaneously, its reliability also represents a excellent progress. The most suitable way for post -deposition treatment by plasma to improve electrical characteristics on MIS structure is observed

5.2 Future work

In this experiment, the HfO_2 film was deposited by sputter and furnace system. In

the future, the ALCVD (Atomic Layer CVD) system will become another important deposition technology. Further experiment and analysis are required to clarify if the treatment condition is also suitable for ALCVD film. On the other hand, the MOSFET will be fabricated by the same treatment condition to verify the effect on device characteristics, such as mobility, subthreshold swing, and transonductance.

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Table

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
L_g: *Physical* L_{gate} *for High Performance logic (nm) [1]*	32	28	25	22	20	18	16	14	13
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	12	11	11	9	7.5	6.5	5	5	
UTB FD (Å)				9	8	7	6	5	5
DG (Å)							8	7	6
Gate Poly Depletion and Inversion-Layer Thickness [3]									
Extended Planar Bulk (Å)	7.3	7.4	7.4	2.9	2.8	2.7	2.5	2.5	
UTB FD (Å)				4	4	4	4	4	4
DG (Å)							4	4	4
EOT_{elec}: *Electrical Equivalent Oxide Thickness in inversion [4]*									
Extended Planar Bulk (Å)	19.3	18.4	18.4	11.9	10.3	9.2	7.5	7.5	
UTB FD (Å)				13	12	11	10	9	9
DG (Å)							12	11	10
$J_{g,limit}$: *Maximum gate leakage current density [5]*									
Extended Planar Bulk (A/cm^2)	1.88E+02	5.36E+02	8.00E+02	9.09E+02	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
FDSOI (A/cm^2)				7.73E+02	9.50E+02	1.22E+03	1.38E+03	2.07E+03	2.23E+03
DG (A/cm^2)							6.25E+02	7.86E+02	8.46E+02
V_{dd}: *Power Supply Voltage (V) [6]*	1.1	1.1	1.1	1	1	1	1	0.9	0.9
$V_{t,sat}$: *Saturation Threshold Voltage [7]*									
Extended Planar Bulk (mV)	195	168	165	160	159	151	146	148	
UTB FD (mV)				169	168	167	170	166	167
DG (mV)							181	184	185
$I_{sd,leak}$: *Source/Drain Subthreshold Off-State Leakage Current [8]*									
Extended Planar Bulk (µA/µm)	0.06	0.15	0.2	0.2	0.22	0.28	0.32	0.34	
UTB FD (µA/µm)				0.17	0.19	0.22	0.22	0.29	0.29
DG (µA/µm)							0.1	0.11	0.11
$I_{d,sat}$: *effective NMOS Drive Current [9]*									
Extended Planar Bulk (µA/µm)	1020	1130	1200	1570	1810	2050	2490	2300	
UTB FD (µA/µm)				1486	1625	1815	2015	2037	2198
DG (µA/µm)							1899	1932	2220
Mobility Enhancement Factor for $I_{d,sat}$ *[10]*									
Extended Planar Bulk	1.09	1.09	1.08	1.09	1.10	1.10	1.12	1.11	
UTB FD				1.06	1.06	1.06	1.06	1.05	1.05
DG							1.05	1.04	1.05
Effective Ballistic Enhancement Factor [11]									
Extended Planar Bulk	1	1	1	1	1	1	1	1	
UTB FD				1	1	1	1	1	1.1
DG							1.17	1.25	1.31

Table 1-1 High-performance Logic Technology Requirements Roadmap.

(ITRS：2005 updae)

Material	SiO_2	Si_3N_4	Al_2O_3	HfO_2	ZrO_2	La_2O_3	Ta_2O_5	TiO_2	Pr_2O_3	$SrTiO_3$
K value	3.9	7.1	9	25	29	30	26	95	31	200
Bandgap (eV)	9	5.3	8.8	6	5.8	6	4.4	3.1	4.2	3.3
E_{bd} (MV/cm)	10	15	13.8	6.7	5.7	5.6	3.7	2.5	3.4	2.2

Table 1-2 Characteristics of various high-k materials.

Figure-chapter 1

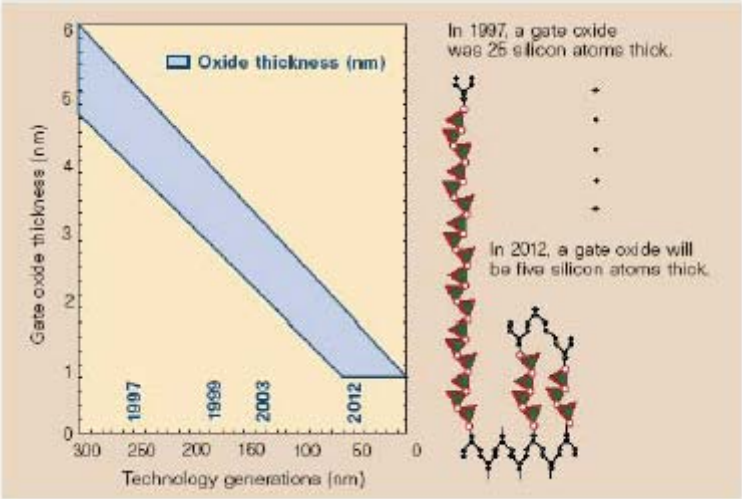


Fig. 1-1 With the marching of technology nodes, gate dielectric has to be shrunk and five silicon atoms thick of gate dielectric is predicted for 2012.[1]

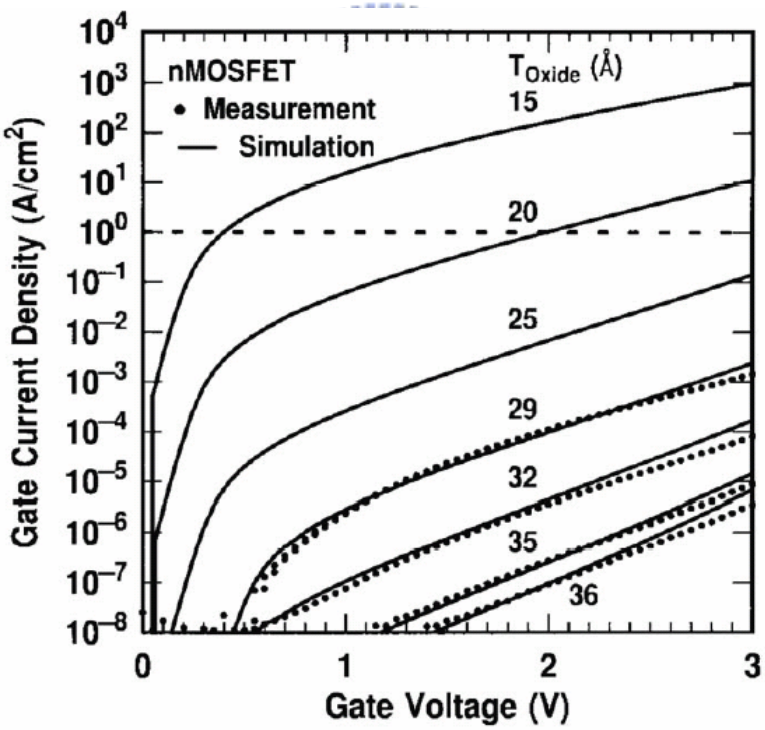


Fig. 1-2 Measured and simulated I_g-V_g characteristics under inversion condition for nMOSFETs. The dotted line indicates the 1A/cm^2 limit for the leakage current. [2]

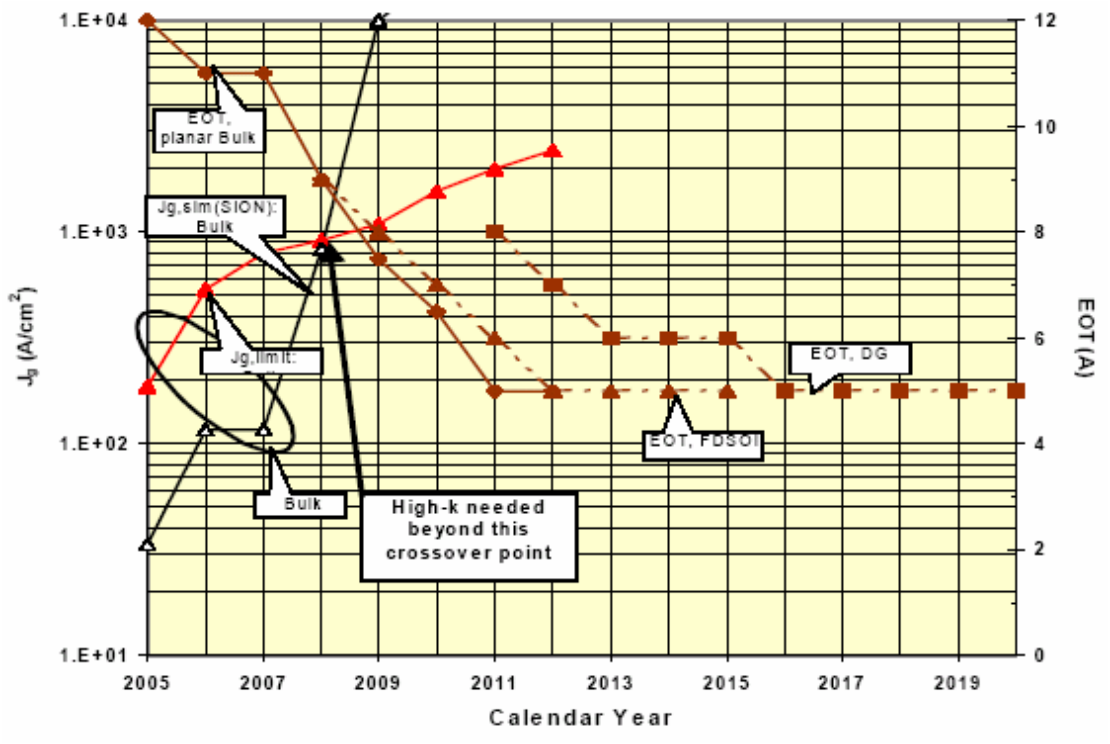


Fig. 1-3 Jg,limit versus Jg,simulated for High-Performance Logic(ITRS: 2005 update)

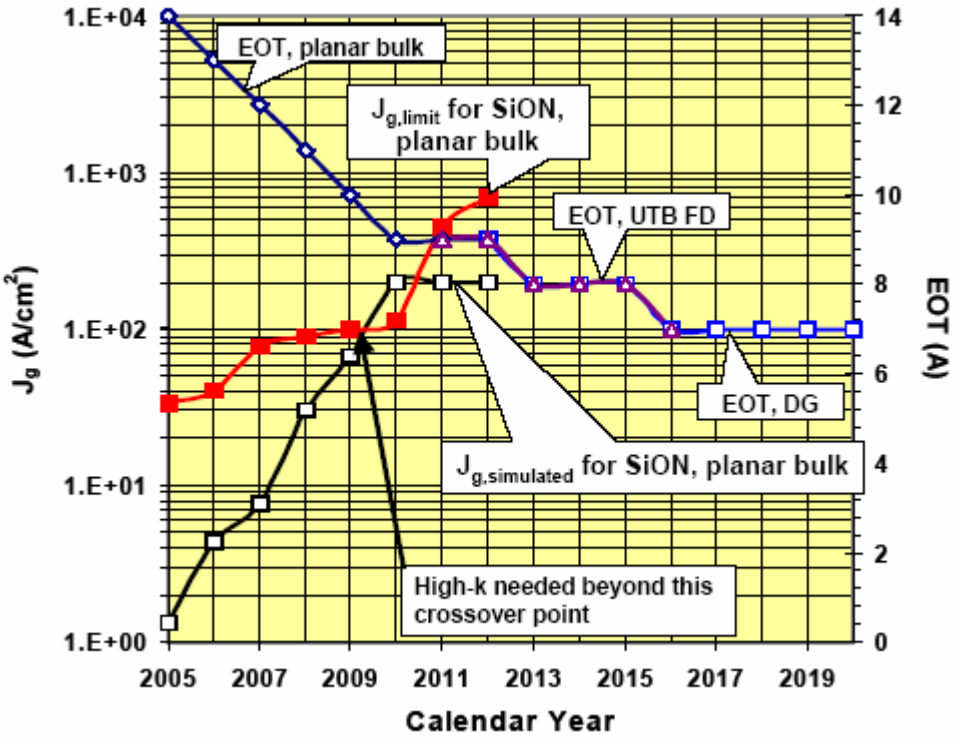


Fig. 1-4 Jg,limit versus Jg,simulated for Low Operating Power (ITRS: 2005 update)

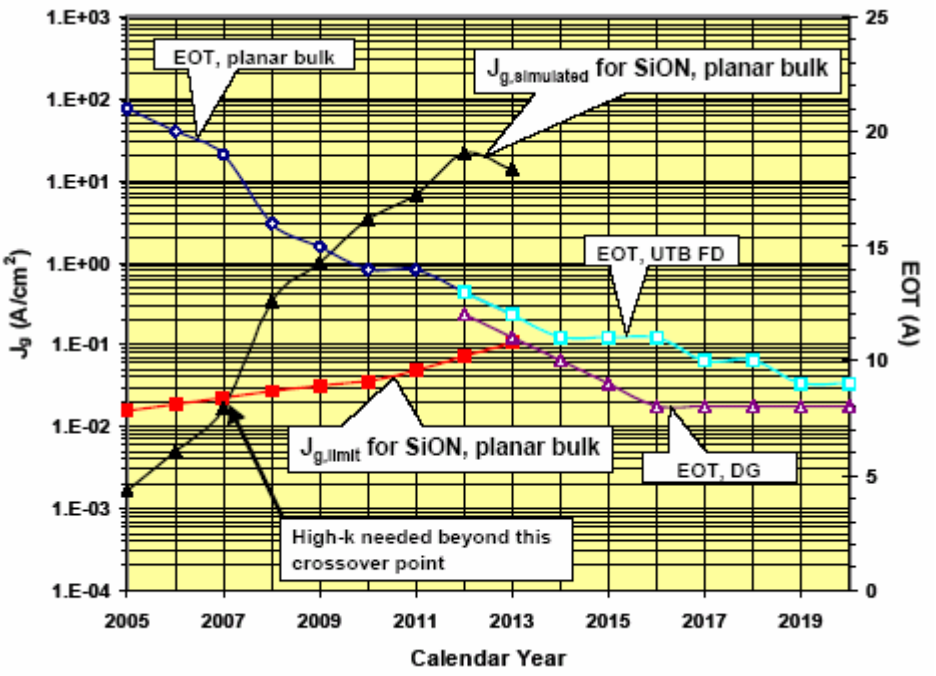


Fig. 1-5 Jg,limit versus Jg,simulated for Low Standby Power (ITRS: 2005 update)

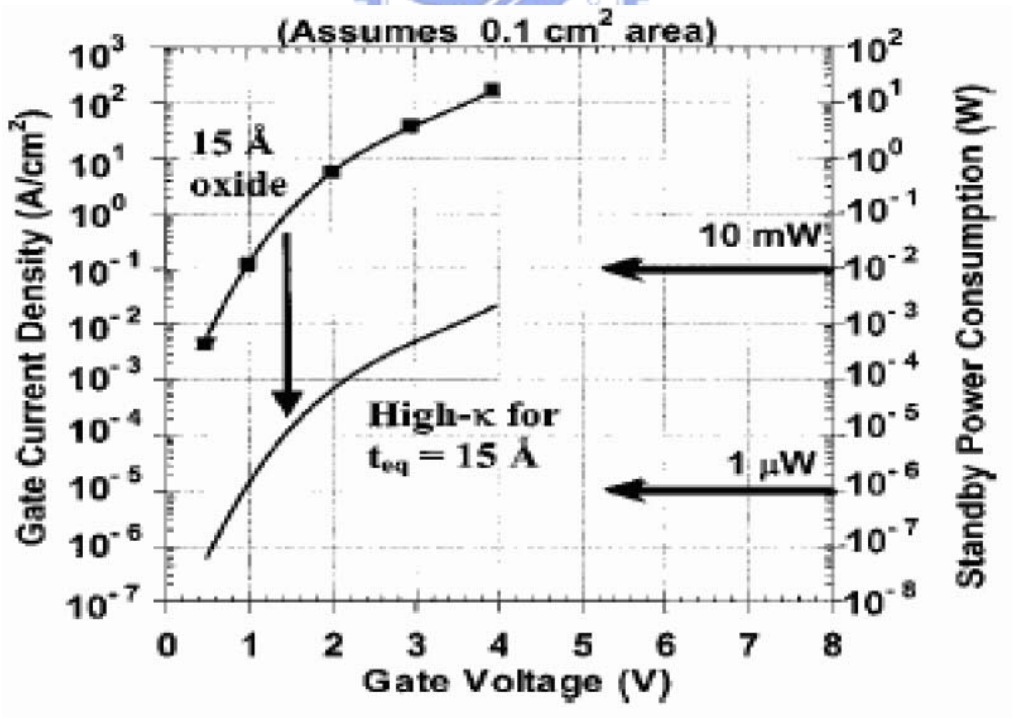


Fig. 1-6 Power consumption and gate leakage current density comparing to the potential reduction in leakage current by an alternative dielectric exhibiting the same equivalent oxide thickness [3].

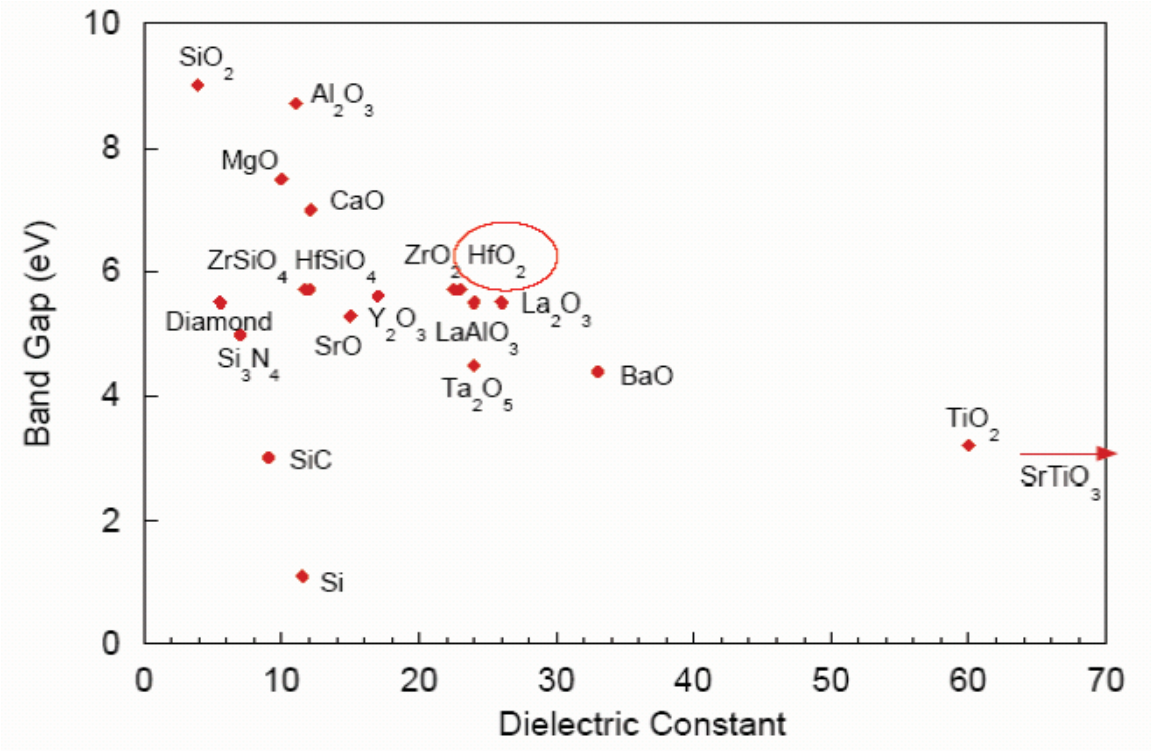
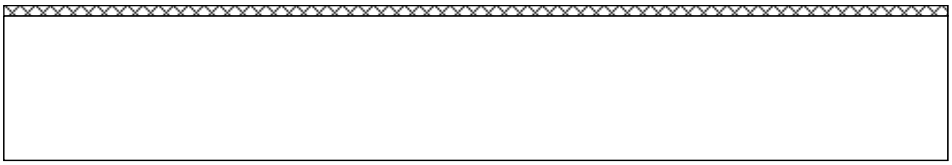


Fig. 1-7 Several high-k gate dielectric materials with their bandgaps and dielectric constants.[15]

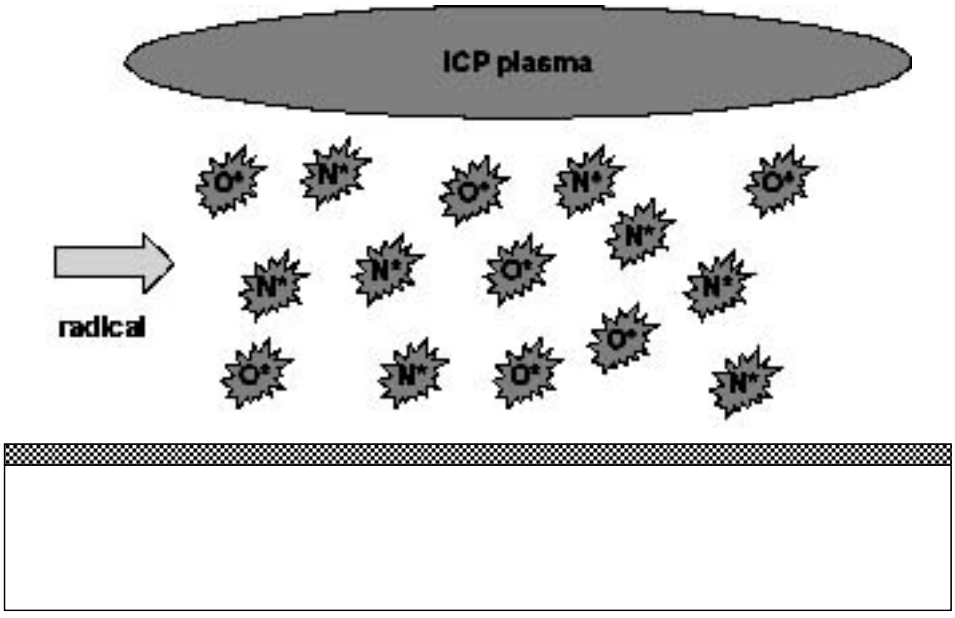
Figure-chapter 2

1. Initial RCA cleaning.

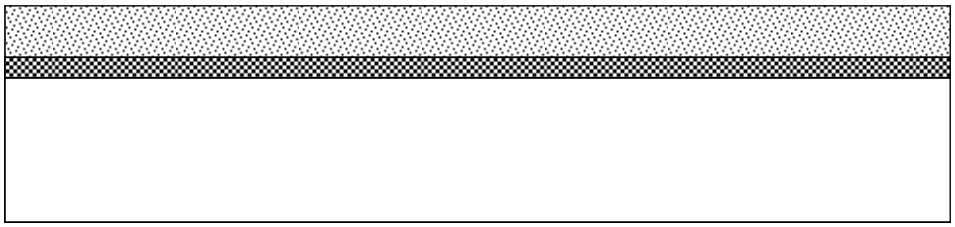


2. DC magnetron sputtering hafnium 20 Å.

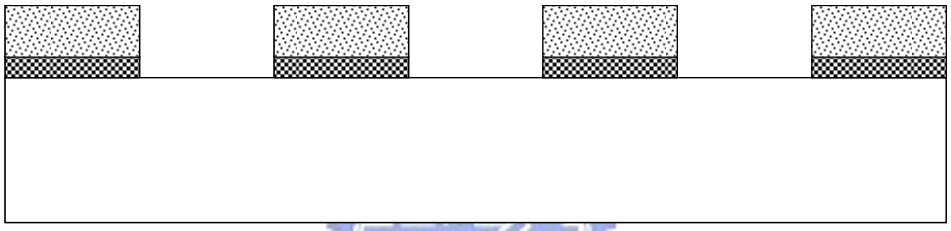
3. Thermal oxidize hafnium in furnace in an O2 ambient at 400 ℃ for 15 minutes to from HfO_2 film.



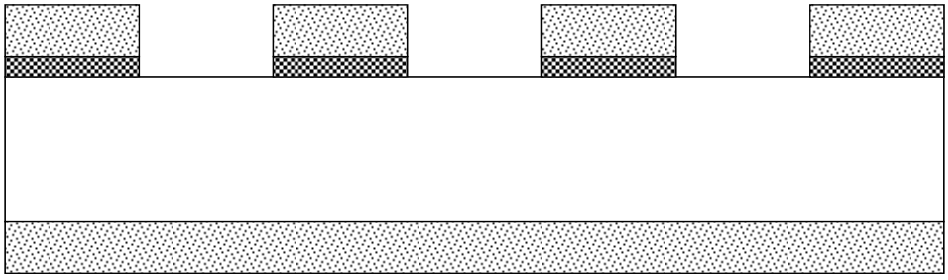
4. Plasma treatment with N_2, N_2O, or O_2 plasma for 10 second, 30 second, 1 minute, 3 minute, or 5 minute respectively



5. Thermally evaporate 5000 Å aluminum as top electrode.



6. Mask：define top electrode and then wet etch undefined Al and HfO_2 films.



7. Strip backside native oxide and coat 5000 Å aluminum as bottom electrode.

Fig. 2-1 The fabrication flow of this experiment

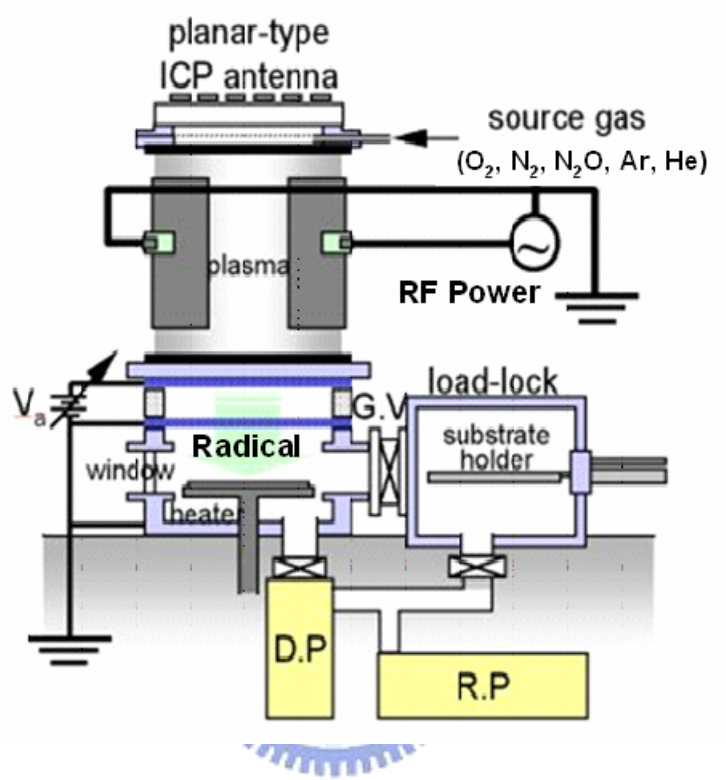


Fig. 2-2 The ICP plasma system that was used in this experiment.

Figure-chapter 3

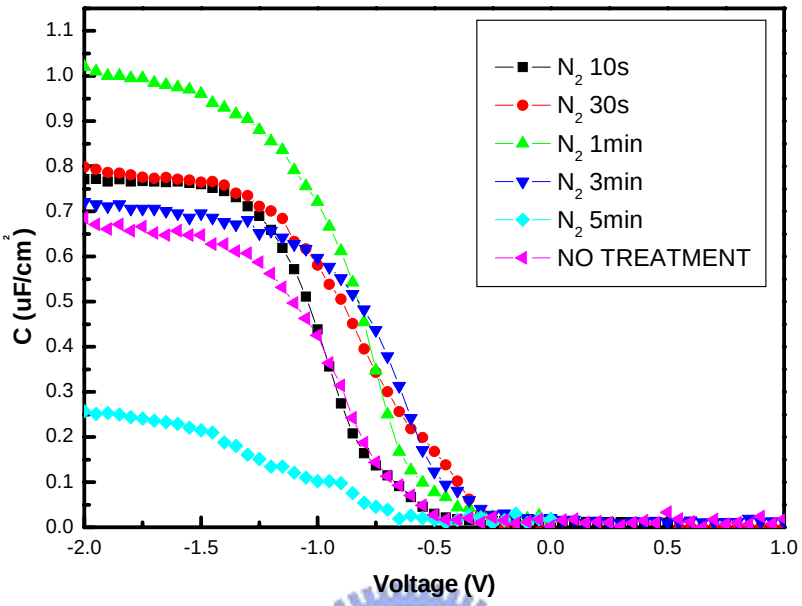


Fig.3-1 The capacitance-voltage (C-V) characteristics of HfO2 gate dielectrics treated with N_2 plasma treatment for different process time.

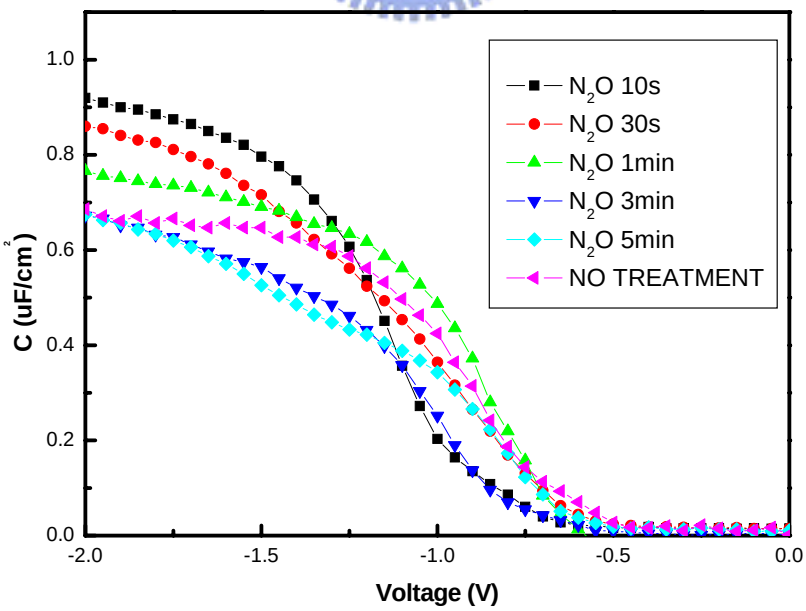


Fig.3-2 The capacitance-voltage (C-V) characteristics of HfO2 gate dielectrics treated with N_2O plasma treatment for different process time.

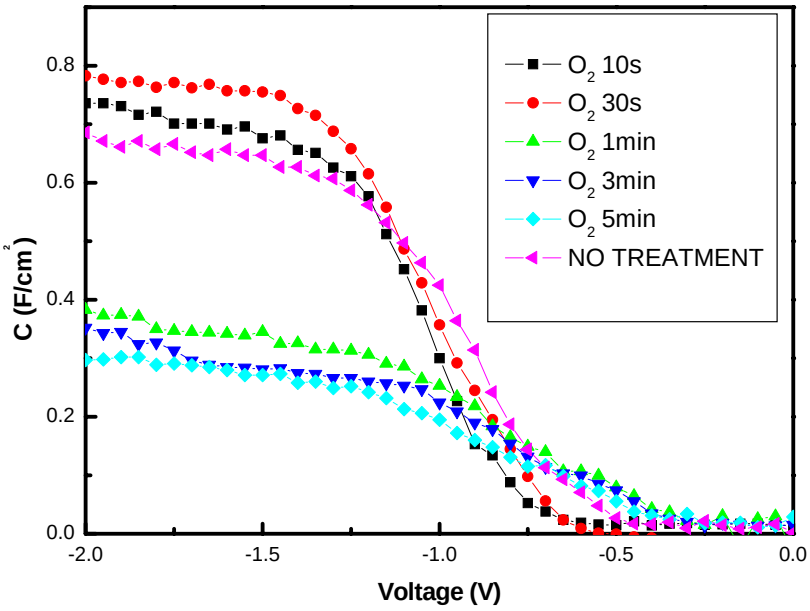


Fig.3-2 The capacitance-voltage (C-V) characteristics of HfO2 gate dielectrics treated with O_2 plasma treatment for different process time.

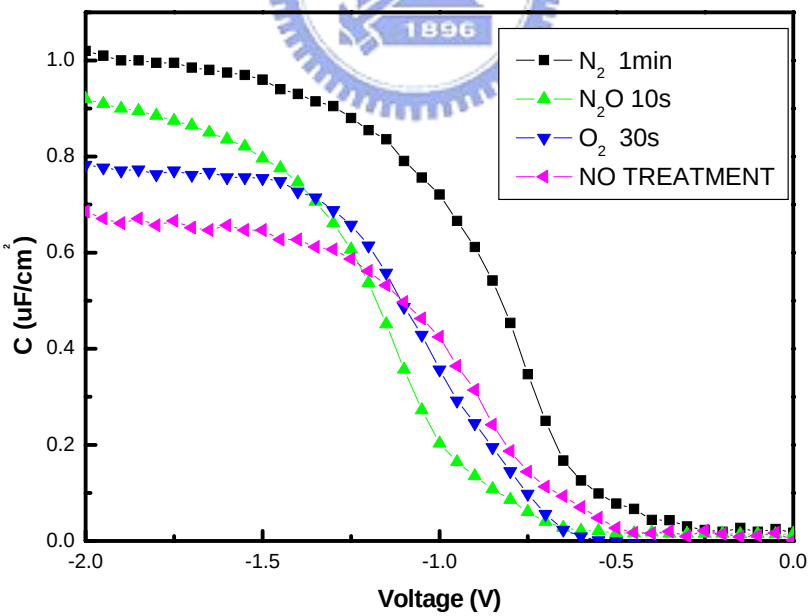


Fig.3-4 The capacitance-voltage (C-V) characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for 1 min, N_2O plasma treatment for 10 sec, and O_2 plasma treatment for 30 sec.

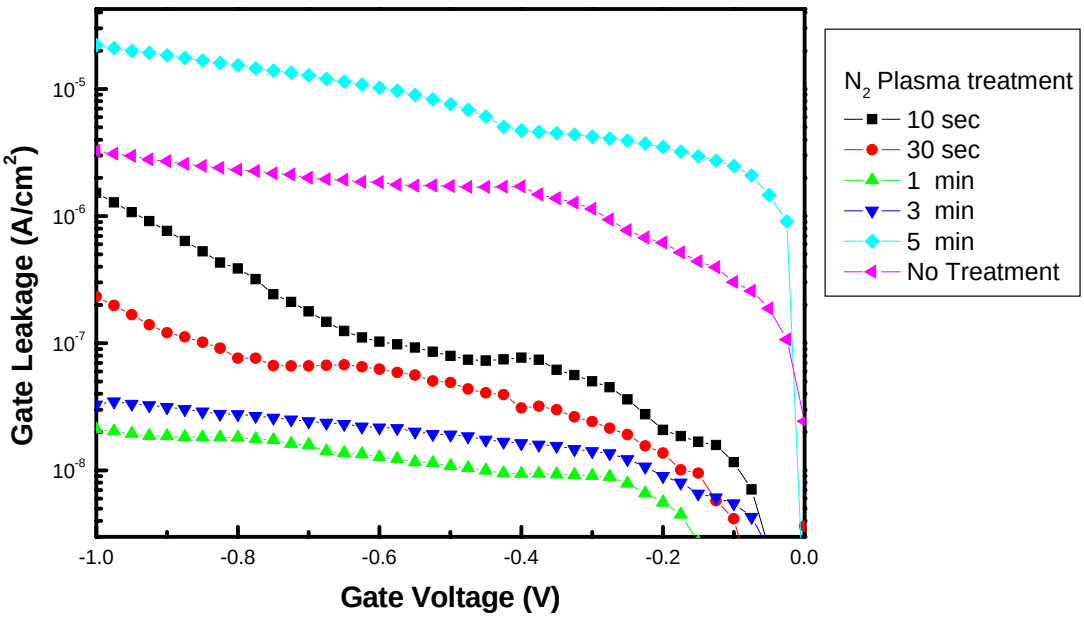


Fig. 3-5 The J-V characteristics of p-type HfO_2 capacitors treated by N_2 plasma with different process time from 0 V to -1 V.

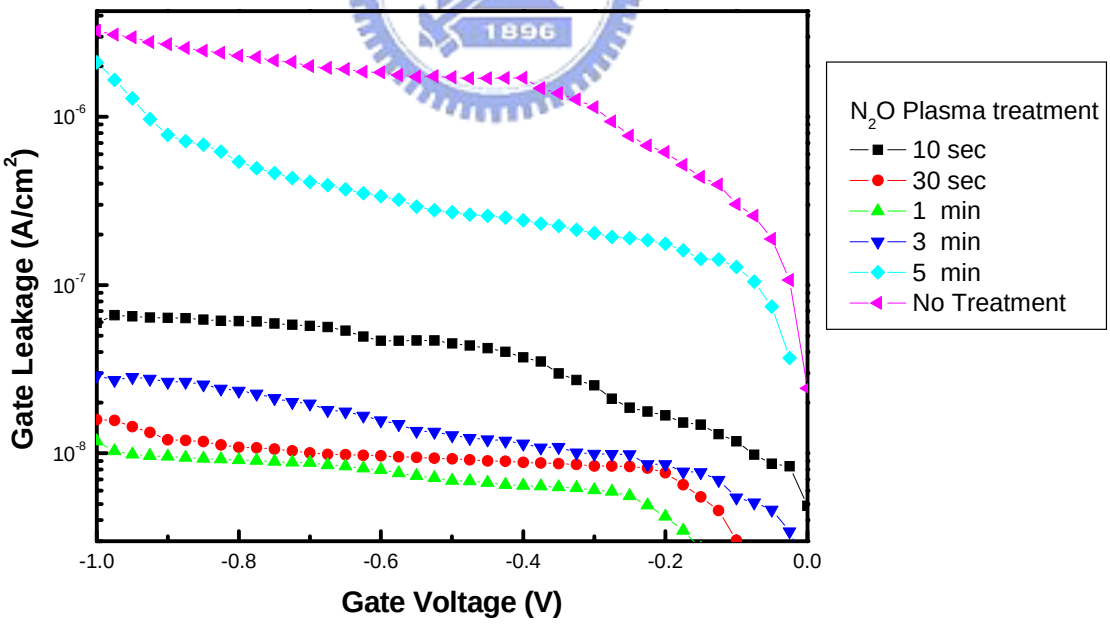


Fig. 3-6 The J-V characteristics of p-type HfO_2 capacitors treated by N_2O plasma with different process time from 0 V to -1 V.

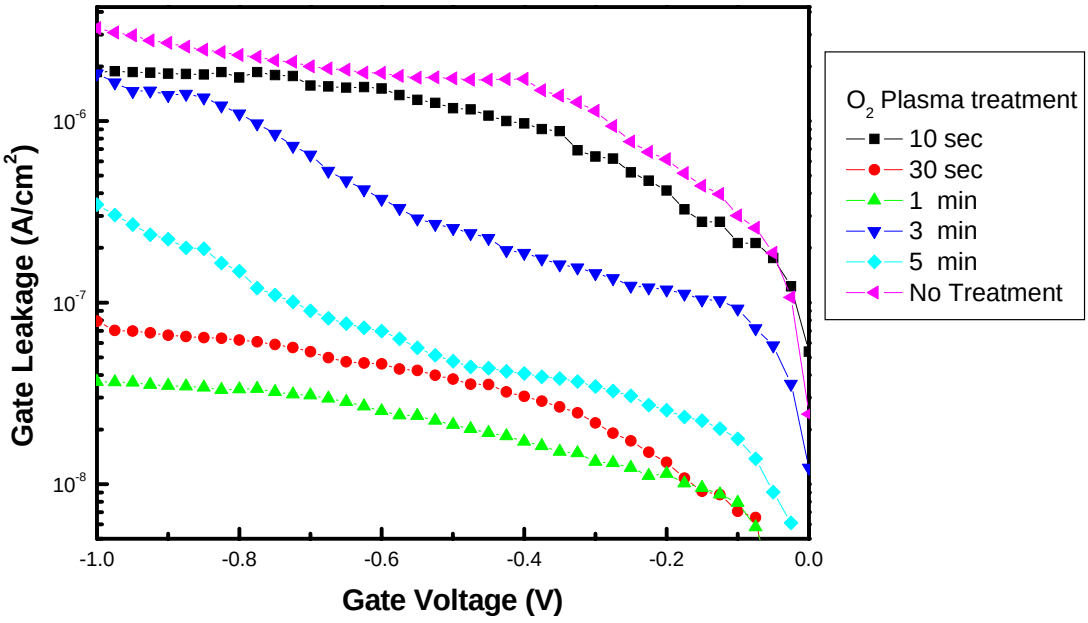


Fig. 3-7 The J-V characteristics of p-type HfO_2 capacitors treated by O_2 plasma with different process time from 0 V to -1 V.

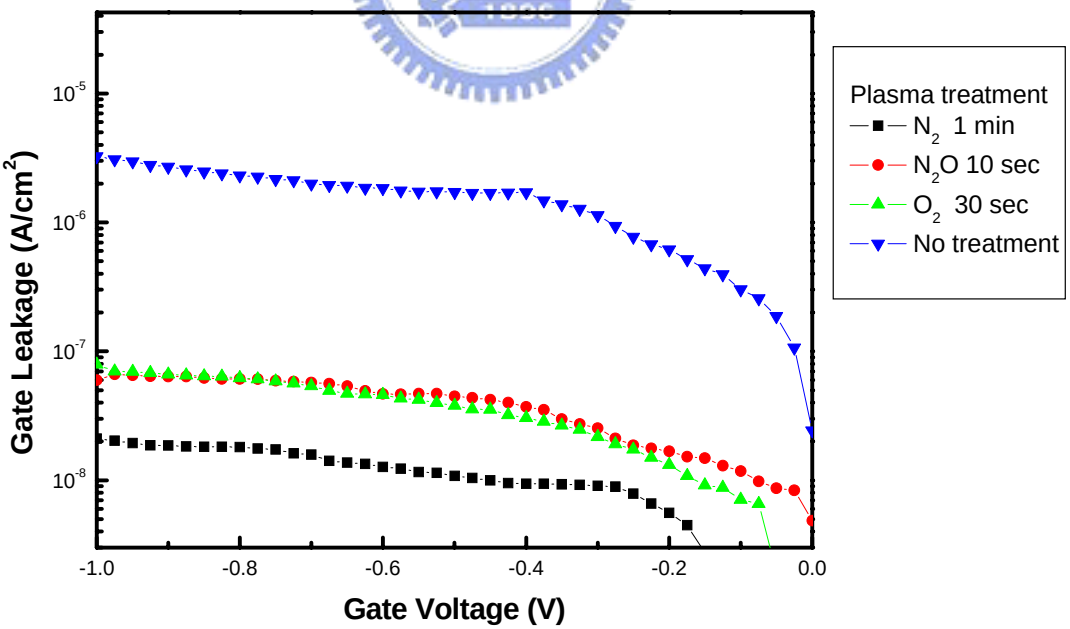


Fig. 3-8 The J-V characteristics of HfO_2 gate dielectrics treated with N_2 plasma treatment for 1 min, N_2O plasma treatment for 10 sec, and O_2 plasma treatment for 30 sec.

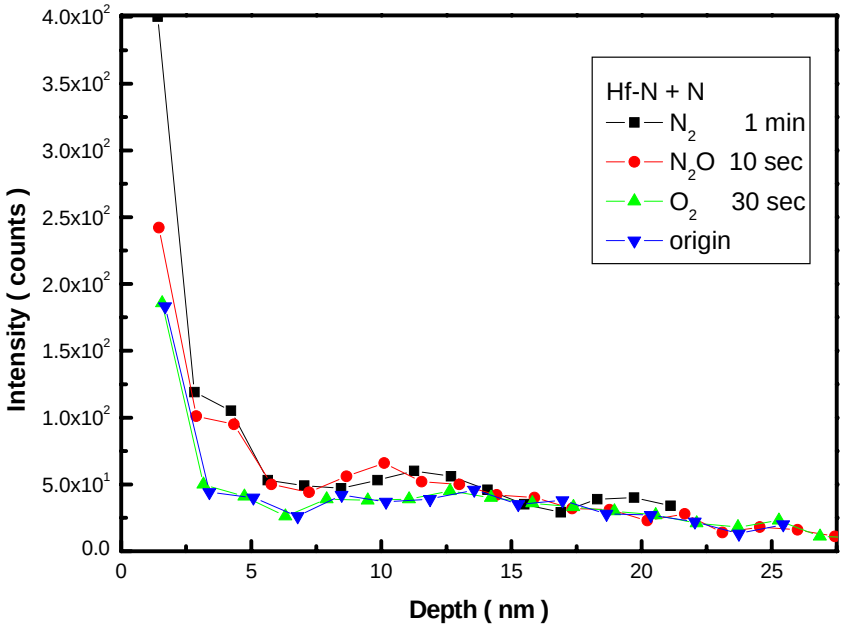


Fig. 3-9 The counts of Hf-N bonds with different conditions which are N_2 for 1 min, N_2O for 10 sec, and O_2 for 30 sec.

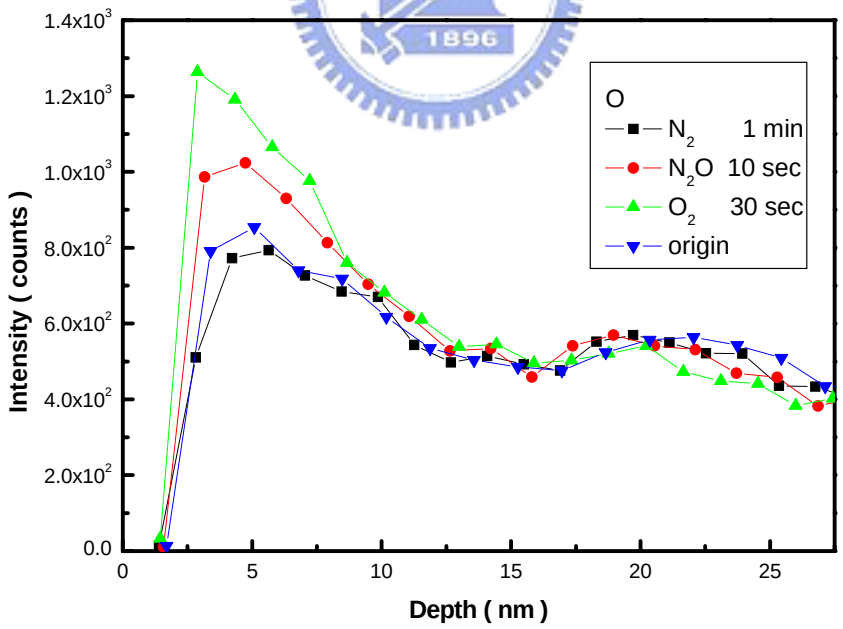


Fig. 3-9 The counts of oxygen with different conditions which are N_2 for 1 min, N_2O for 10 sec, and O_2 for 30 sec.

Figure-chapter 4

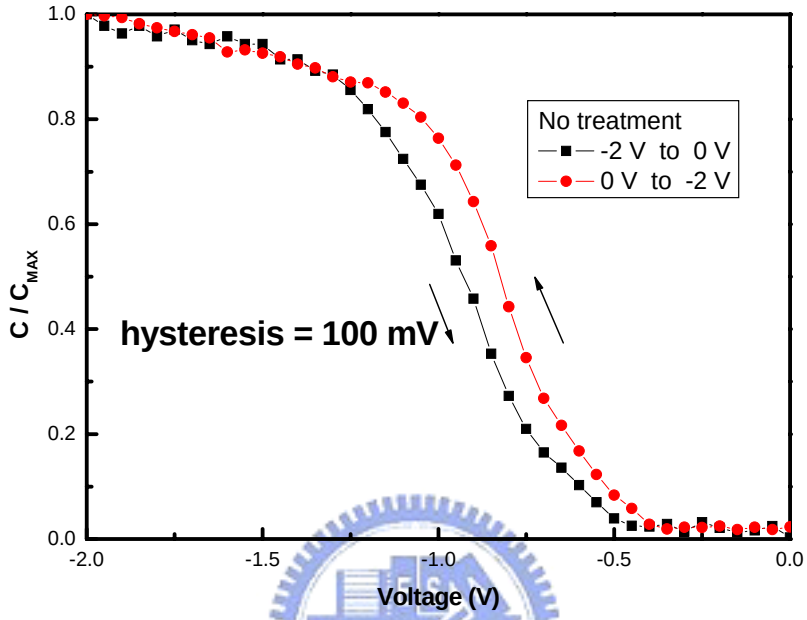


Fig. 4-1 The hysteresis of p-type HfO_2 gate dielectrics treated without treatment

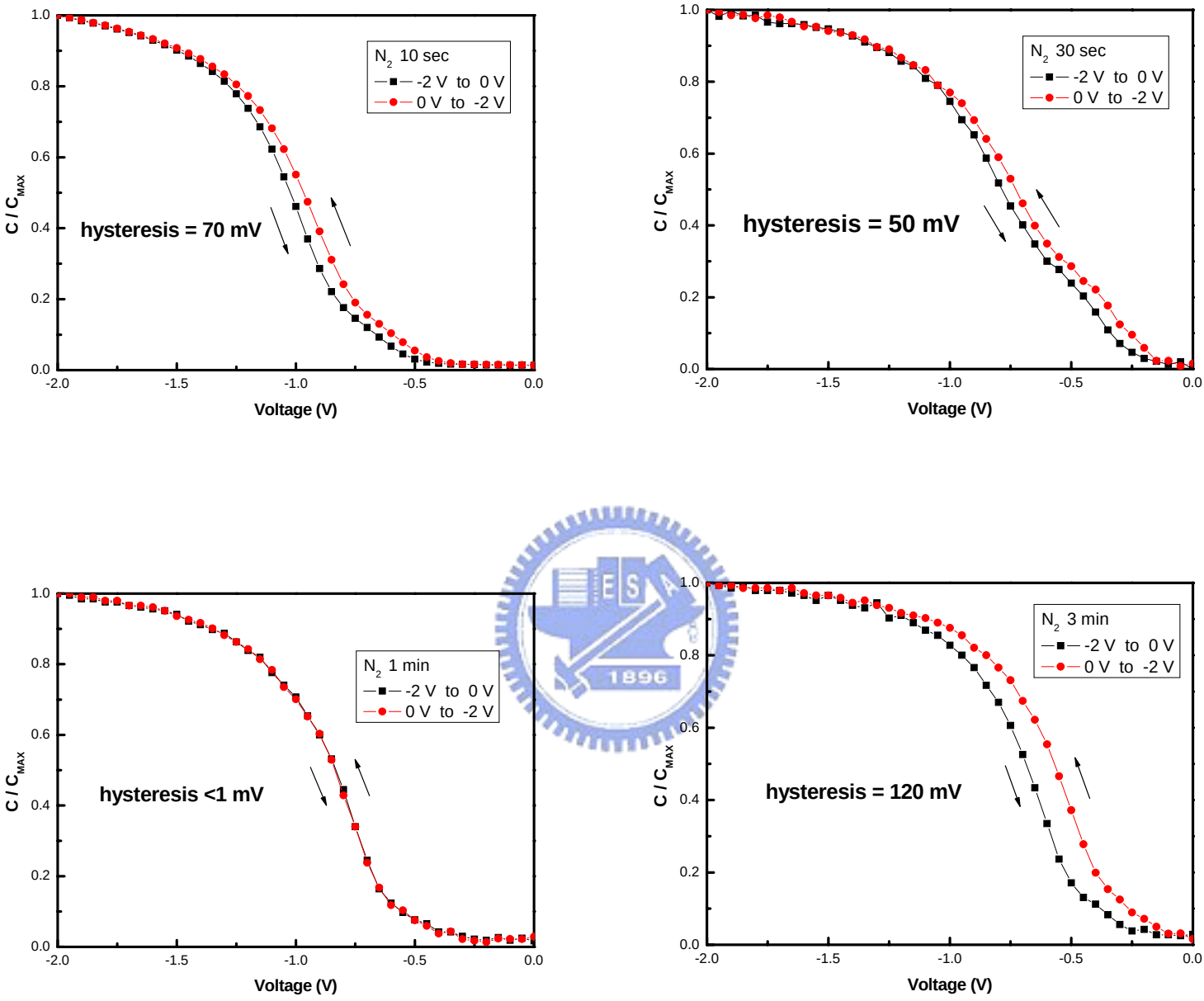


Fig. 4-2 The hysteresis of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time.

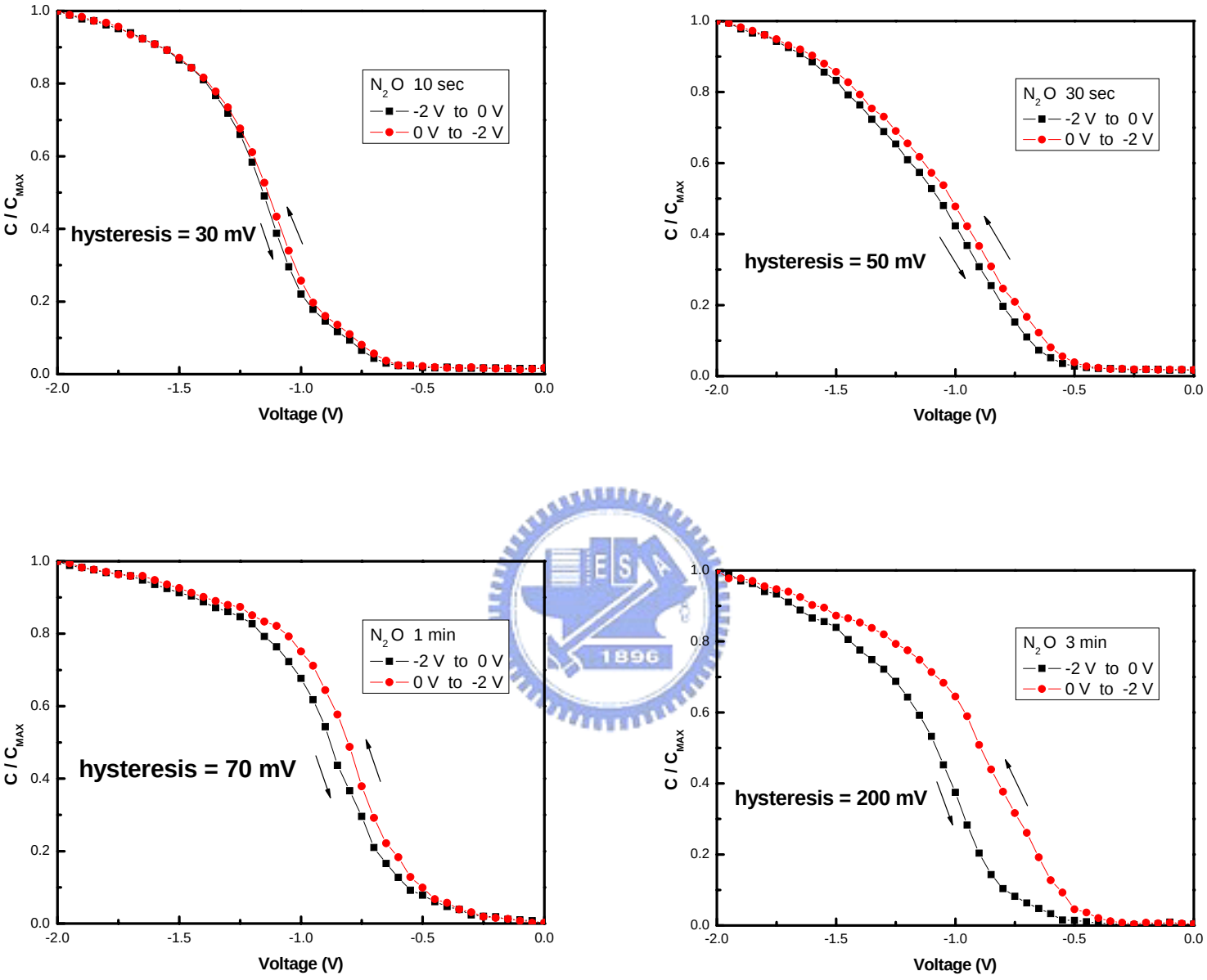


Fig. 4-3 The hysteresis of p-type HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time

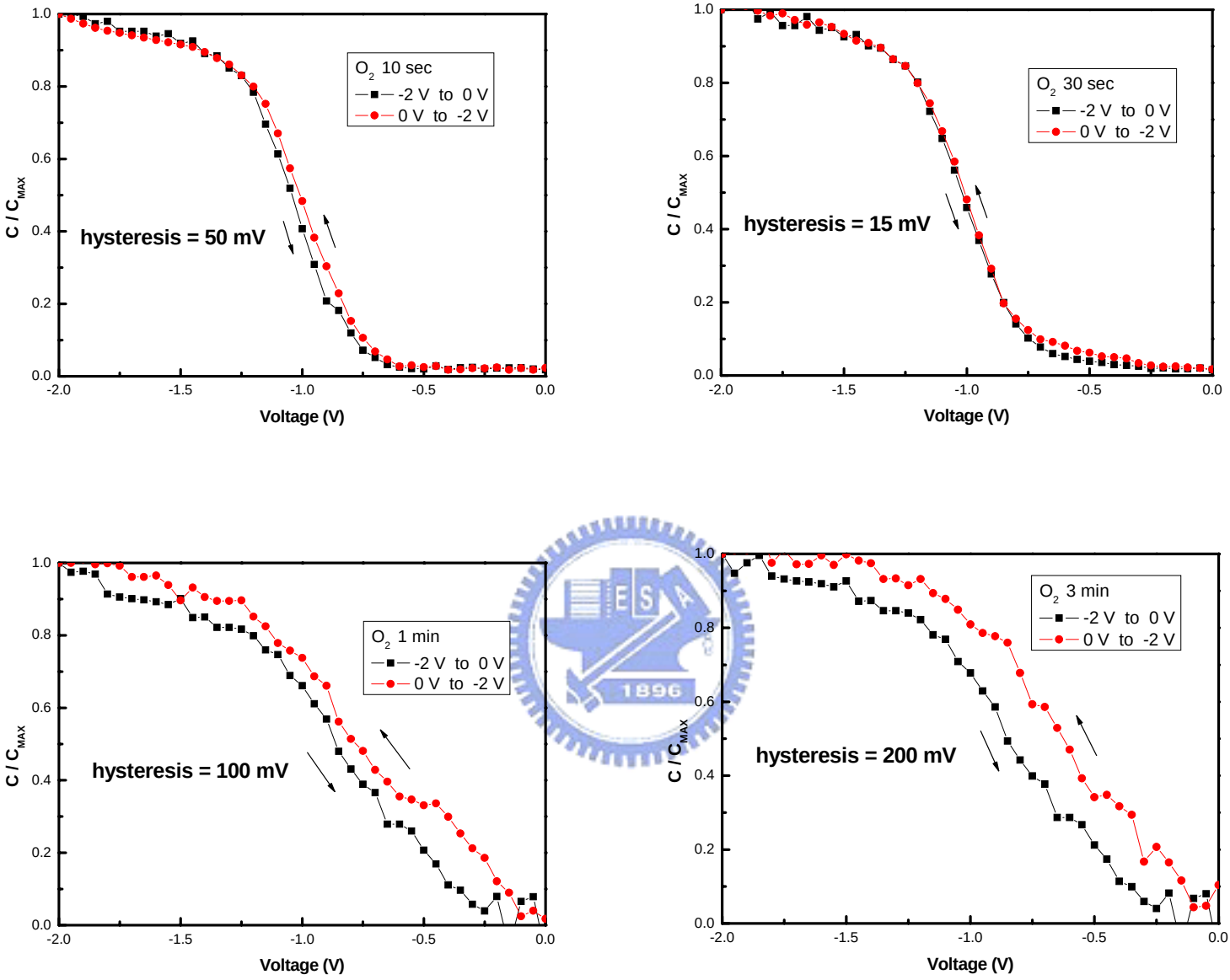


Fig. 4-4 The hysteresis of p-type HfO_2 gate dielectrics treated with O_2 plasma treatment for different process time.

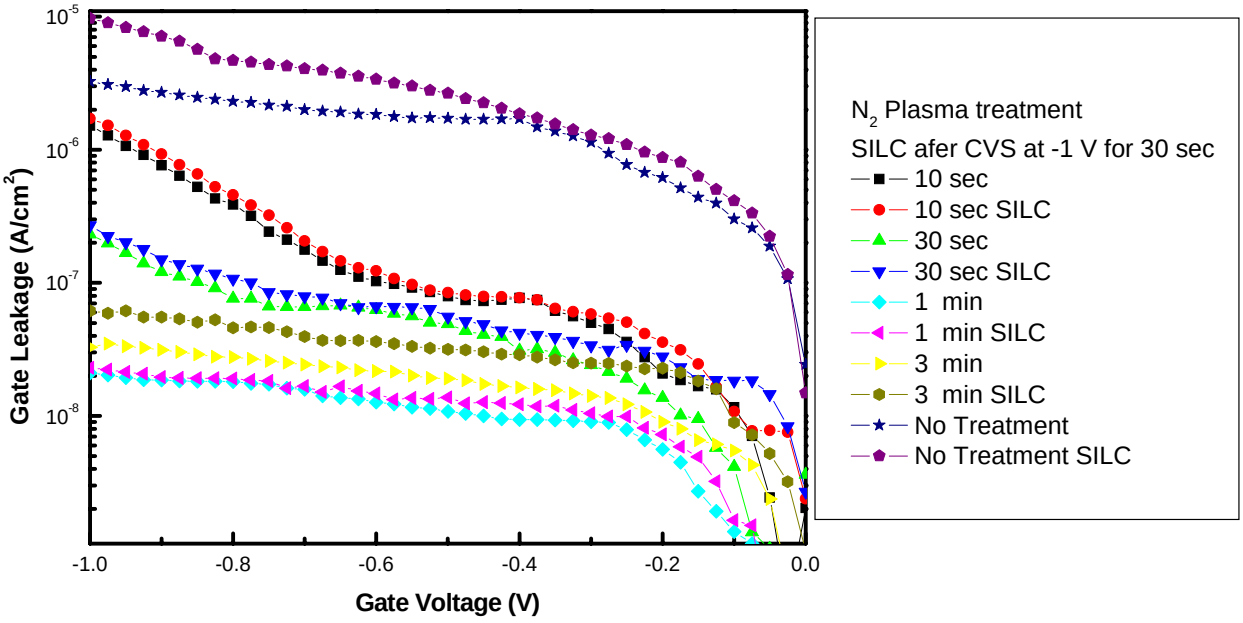


Fig. 4-5 The SILC curve of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time.

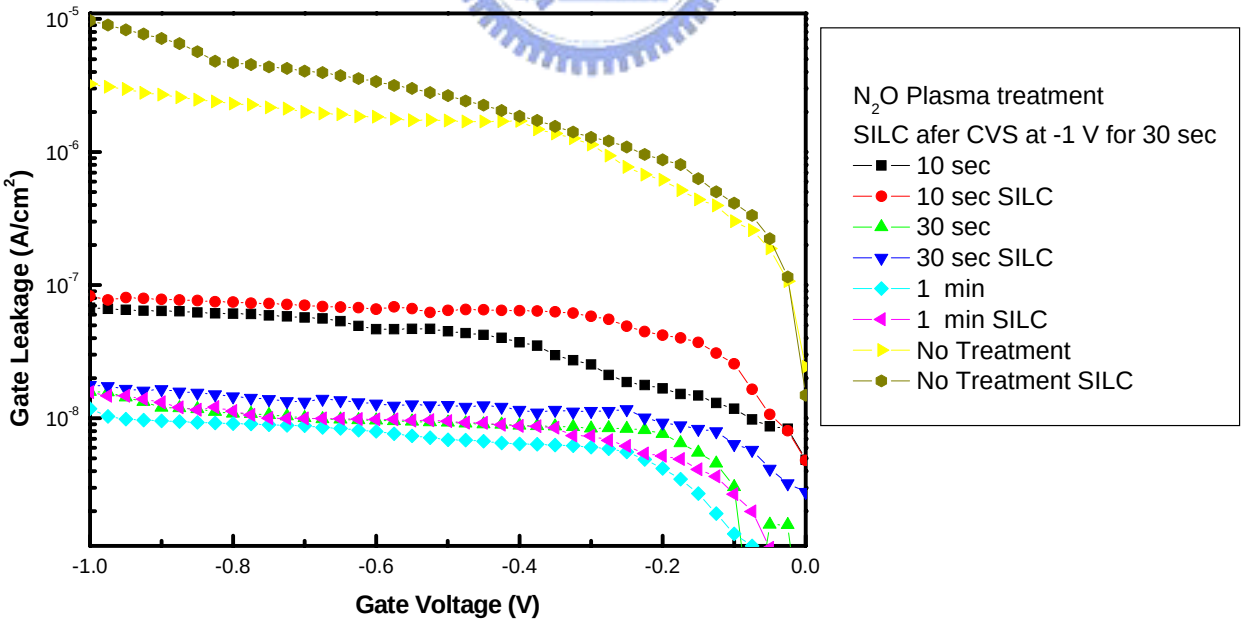


Fig. 4-6 The SILC curve of p-type HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time.

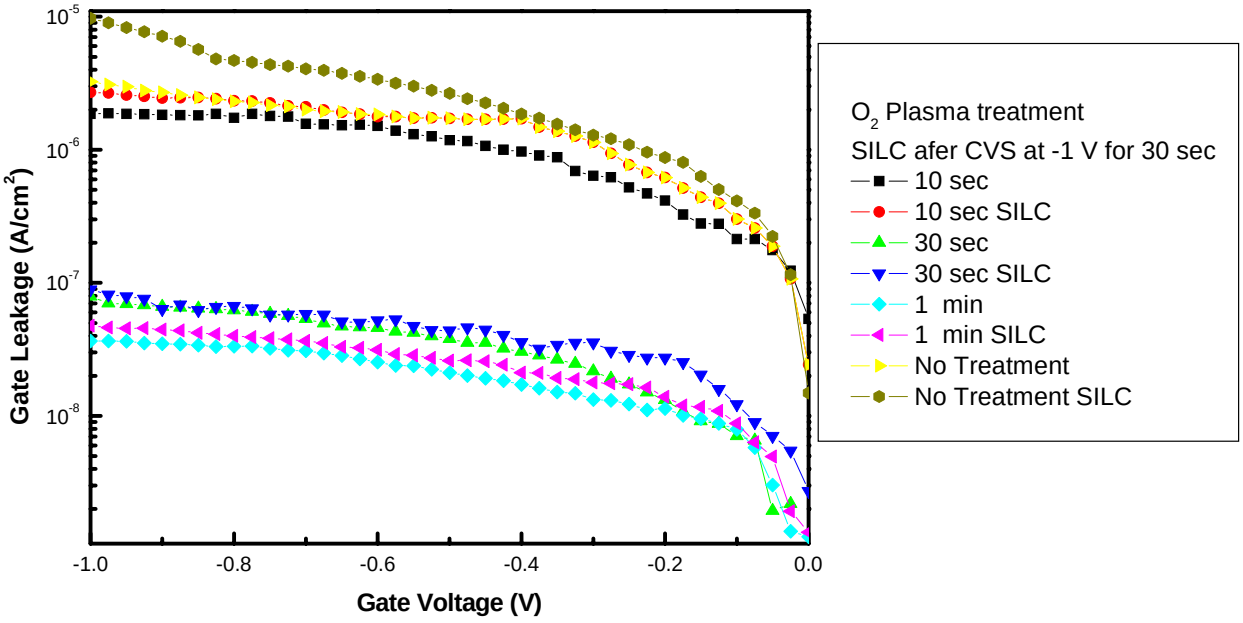


Fig. 4-7 The SILC curve of p-type HfO_2 gate dielectrics treated with O_2 plasma treatment for different process time.

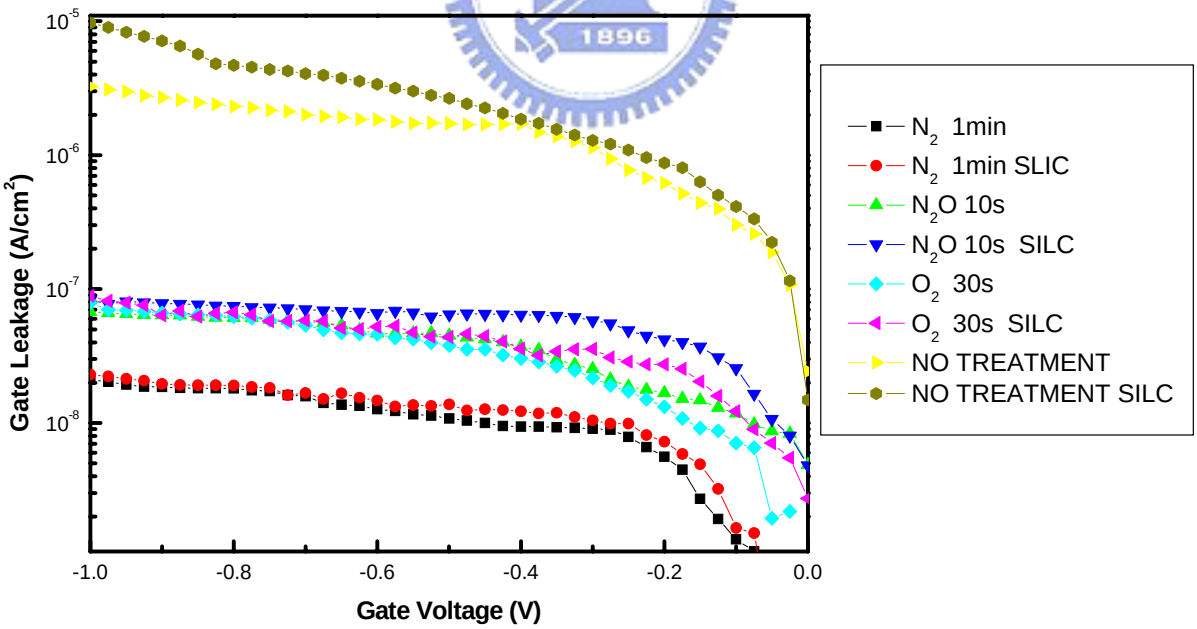


Fig. 4-8 The SILC compare of HfO_2 gate dielectrics treated with N_2 plasma treatment for 1 min, N_2O plasma treatment for 10 sec, and O_2 plasma treatment for 30 sec.

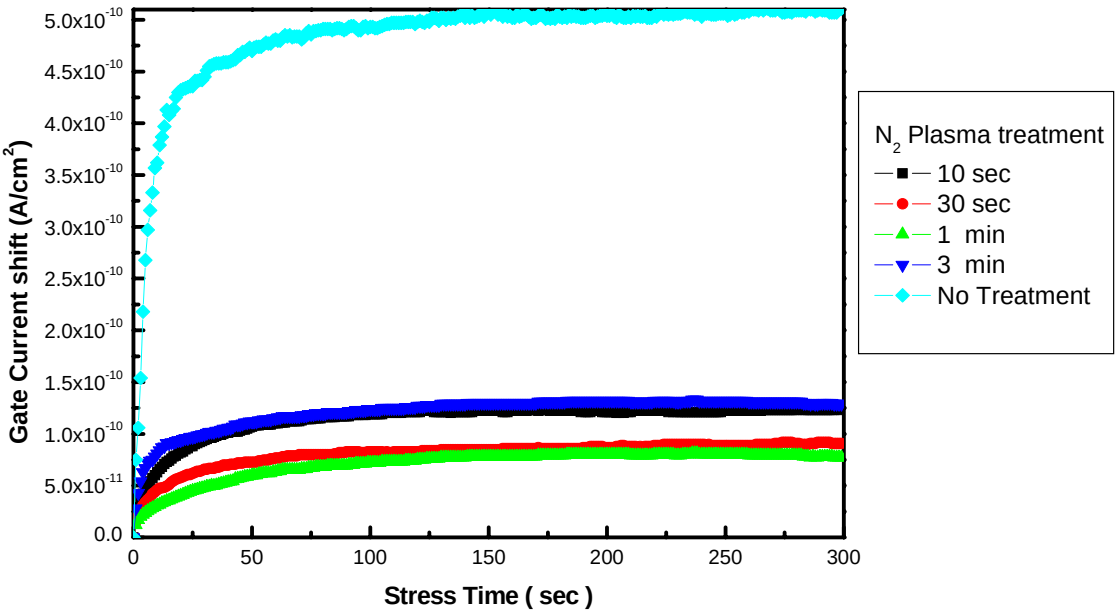


Fig. 4-9 The gate current shift of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time as a function of stress time during Vg = 1 V CVS stress.

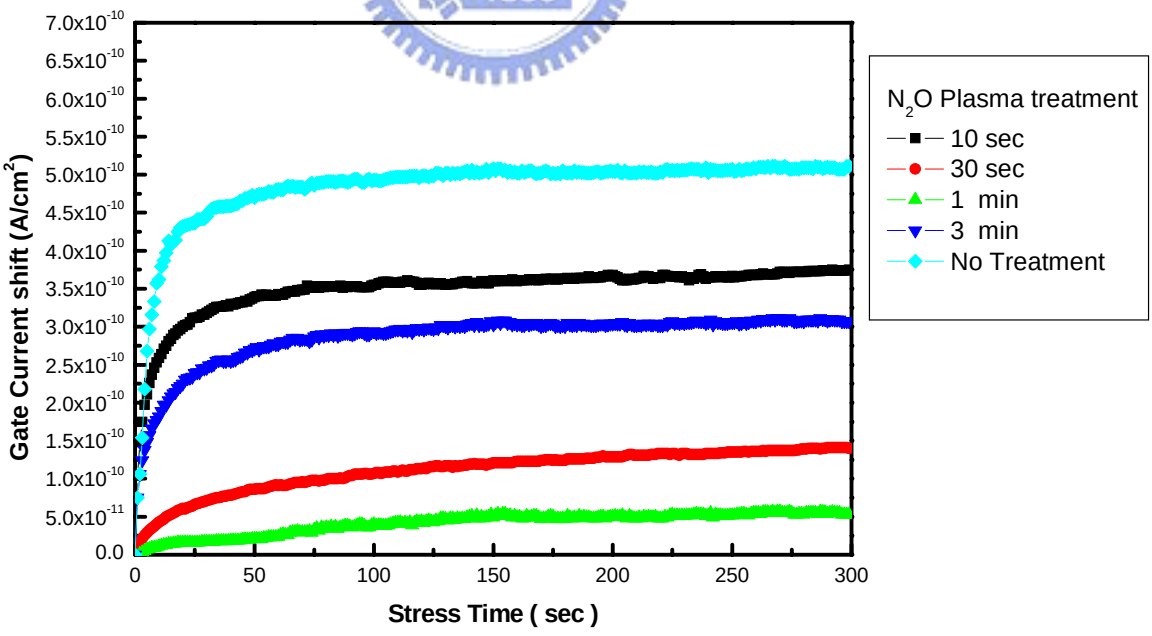


Fig. 4-10 The gate current shift of p-type HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time as a function of stress time during Vg = 1 V CVS stress.

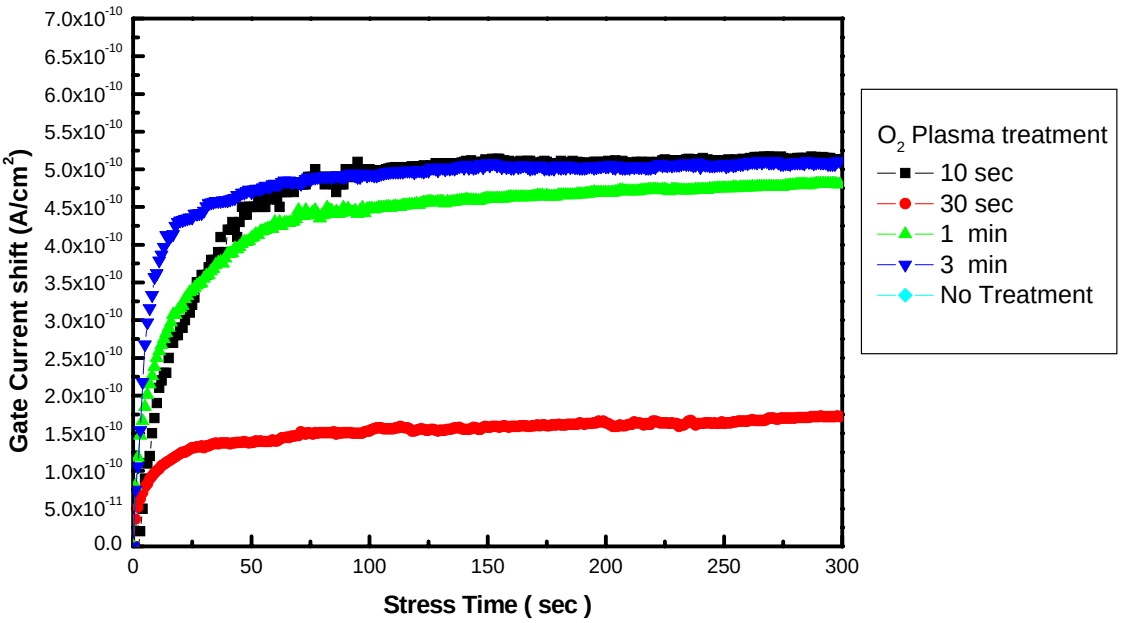


Fig. 4-11 The gate current shift of p-type HfO_2 gate dielectrics treated with O_2 plasma treatment for different process time as a function of stress time during Vg = 1 V CVS stress.

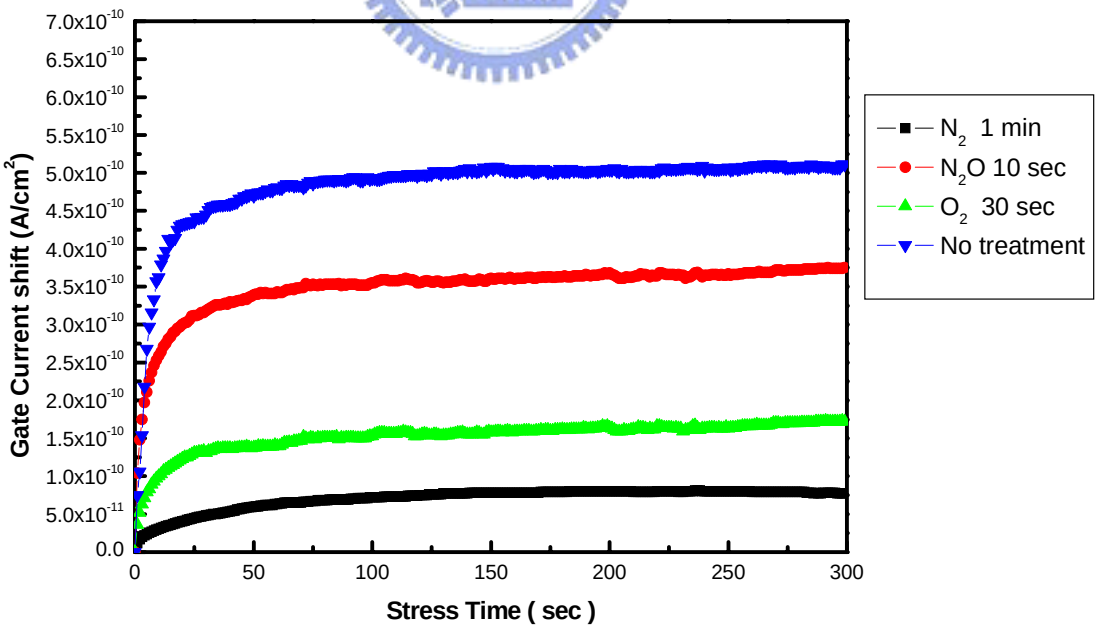


Fig. 4-12 The CVS compare of HfO_2 gate dielectrics treated with N_2 plasma treatment for 1 min, N_2O plasma treatment for 10 sec, and O_2 plasma treatment for 30 sec.

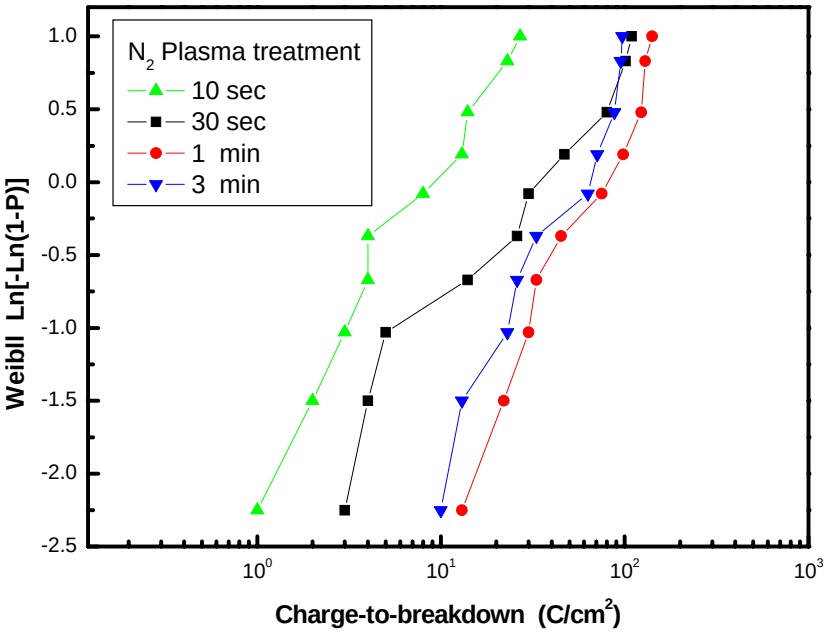


Fig. 4-13 The charge-to-breakdown characteristics (Q_{BD}) of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for different process time.

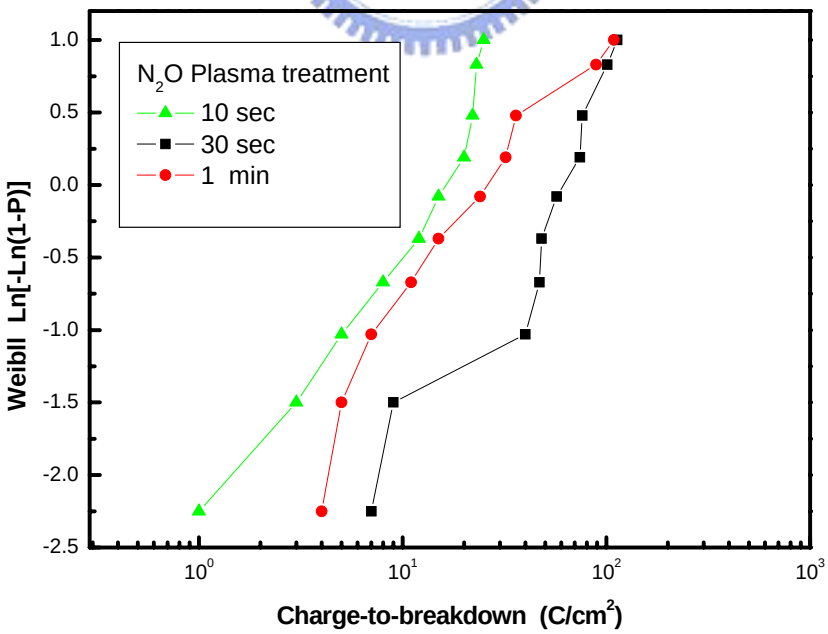


Fig. 4-14 The charge-to-breakdown characteristics (Q_{BD}) of p-type HfO_2 gate dielectrics treated with N_2O plasma treatment for different process time.

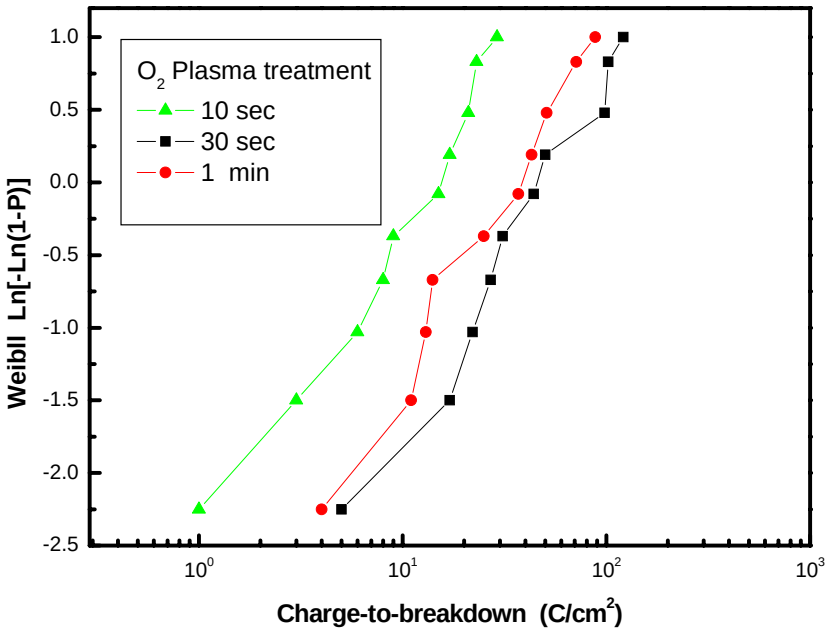


Fig. 4-15 The charge-to-breakdown characteristics (Q_{BD}) of p-type HfO_2 gate dielectrics treated with O_2 plasma treatment for different process time.

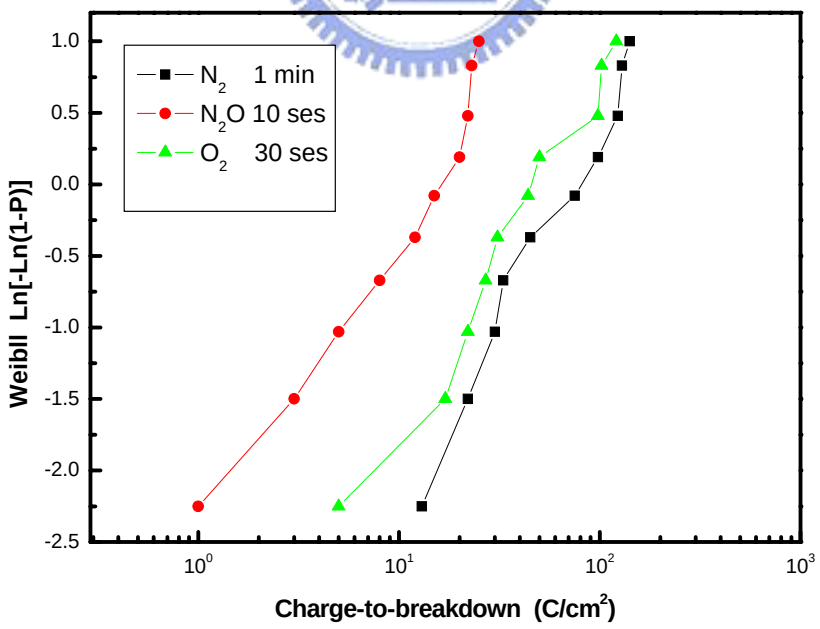


Fig. 4-16 The charge to breakdown characteristics (Q_{BD}) of p-type HfO_2 gate dielectrics treated with N_2 plasma treatment for 1min, N_2O for 30 sec, and O_2 for 30 sec.

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碩士論文：沉積後電漿處理對二氧化鉿金氧半導體結構電特性之影響

The Effect of Post-Deposition Plasma Treatment on The Electrical Characteristics of HfO_2 MOS Structure