國 立 交 通 大 學

電子工程學系　電子研究所

碩 士 論 文

於3.1-10.6GHz無線應用的超寬頻金氧半功率放大器

An Ultra-Wideband CMOS Power Amplifier for 3.1 to 10.6 GHz Wireless Applications

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摘要

本論文以 TSMC 0.18um 的 CMOS 製程環境下，首先設計了一個兩級在 3.1 到 10.6GHz 的超寬頻功率放大器。第一級在共源、共閘的串疊結構之中，加入了電阻的迴授結構。這樣帶來了高的功率增益以及寬頻的輸入組抗匹配；而第二級利用了共源加上電阻電感迴授的結構，來達到寬頻組抗匹配以及平坦的功率增益。

接下來針對上述的功率放大器研究後，我們改進了設計的細節，進一步設計了一個 3 到 8GHz 的兩級超寬頻功率放大器。藉由將電容加入上述的迴授結構，我們減少了在迴授路徑上面的直流功率消耗。再加上對負載線設計的加強，我們在線性度以及功率轉換效益上有很大的突破。

An Ultra-Wideband CMOS Power Amplifier for 3.1 to 10.6 GHz Wireless Applications

Student: Ke-Min Chen **Advisor: Dr. Albert Chin**

Department of Electronics Engineering & Institute of Electronics

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Abstract

This thesis is based on TSMC 0.18um CMOS process. A two-stage ultra-wideband CMOS power amplifier is applied for 3.1 to 10.6GHz. The 1st stage introduces the common-source and common-gate topology called "cascade" with the resistor feedback configuration. It brings higher power gain and wideband input impedance match. And the 2nd stage utilizes the common-source with resistor and inductor in order to wideband matching and power gain flatness.

After further studying for the above-mentioned power amplifier, we improve the detail and design a two-stage power amplifier for 3 to 8GHz. By adding a capacitor to the feedback path, both feedback configurations at the 1st and 2nd stages decreases the DC power loss. And we obtain more suitable DC bias condition by focusing on the load-line design; it does work very much to our efficiency and linearity.

Acknowledgement

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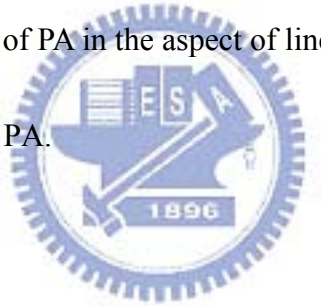


Chapter 5 Summary

Chapter 1

Introduction

1.1 Motivation

For portable wireless communication devices has given great push to the development of a next generation of low power radio frequency integrated circuits (RFIC) product. Such as wireless phones, cordless and cellular, global positioning satellite (GPS), pagers, wireless modems, wireless local area network (LAN), and RF ID tags, etc., require more low cost; low noise and high power efficiency solutions to supply the demand for low-price product [1].

In UWB systems, the power level from the UWB transmitter should be low enough not to interfere with the already existing communication systems, for example 802.11a. The low output levels that specified by the Federal Communications Commission (FCC) is less than -41.3 dBm/MHz. Therefore, for a 7 GHz bandwidth, the peak output power is approximately-3 dBm or 500 μW. UWB systems need not require large transistors, and greatly lighten the difficult of CMOS technology. The main challenging task becomes to achieve a high gain and good impedance match over the entire frequency band.

The RF integrated circuit used for UWB devices are encounter with various possibilities: CMOS, Bi CMOS, and GaAs MESFET, bipolar (BJT), hetero-junction

bipolar transistor (HBT), and PHEMT, etc,. We just study and discuss on the CMOS technology.

Chapter 2 discusses the basic concepts of power amplifier. Chapter 3 presents the basic power amplifiers design for UWB. Chapter 4 deals with wideband matching network, gain flatness and load-line analysis by using inductor-resistor feedback, presents the UWB proposals, design, implementation of our power amplifiers. Chapter 5 concludes this research effort with some future directions.

Chapter2

Basic concepts of Power Amplifier

2.0 Introduction

A reasonable start of power amplifier, which is abbreviated as PA, would be to recall some classical results of linear RF amplifier theory because many PA designs are simple extensions or modifications of linear design. We can read the detail results of RF linear amplifier in many books, so we skip those and assume some concepts of RF linear amplifier is well known.

As we discuss about power amplifier, some basic concepts should be motioned. First, the PA operates at a high out power state; for example, CMOS devices could be saturated, and therefore nonlinear effect become significant. If the output power is 1Watt, and how much power the PA should be dissipated? Ideally, we want all the DC supply power be converted to signal power, but it is impossible in practice. Therefore the efficiency is the important performance of PA. And some issues about optimum output power should be studied including load line match and load-pull technology. So, this chapter presents the main concepts and challenges of RF power amplifiers.

2.1 Amplifier Parameter Definitions

2.1.1 Weakly Nonlinear Effects: Power Series Analysis

Power series is a generalized formula expressing nonlinear behaviors in many

aspects, but it has some limitations: there is no phase component in the linear output term, letting alone the nonlinear terms. A much stronger formula of the power series, called the Volterra series, would be used including phase effects. Weak nonlinearities may be, for instance, inter-modulation distortion at levels lower than, say, -30dBc. Unfortunately, the PA operating at or beyond the compression point requires different treatment because the nonlinearities become “strong” and arise through the cutoff and clipping behavior of the transistor; besides, the Power and Volterra series is not sufficiently accurate. The fifth and seventh order terms of Power series usually become significant as the 1dB compression point is approached and can dominate at still higher drive levels.

While plenty of RF amplifiers can be described as a linear model to obtain their response of small signals, nonlinearities often lead to interesting and important phenomena. Generally, the “Power Series” is applied to further analysis. For simplicity, we ignore the higher order terms of the series and assume that

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.1}$$

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer powers of the input frequency.

If $x(t) = A\cos\omega t$, then

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t + \alpha_3 A^3\cos^3\omega t \tag{2.2}$$

$$= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right) \cos \omega t + \frac{\alpha_2 A^2}{2} \cos 2\omega t + \frac{\alpha_3 A^3}{4} \cos 3\omega t \quad (2.3)$$

In Eq. (2.3), the term $\cos \omega t$ is called the "fundamental" and the higher-order terms the "harmonics." The amplitude of the n_{th} harmonic, $\cos n\omega t$, consists of a term proportional to A^n.

In (2.3), the gain written as $\alpha_1 + \frac{3\alpha_3 A^2}{4}$ is therefore a decreasing function of A if $\alpha_3 < 0$. In most circuits, the output is a "compressive" or "saturating" function of the input; that is, the gain approached zero for sufficiently high input levels. This effect is quantified by the "1-dB compression point," defined as the input signal level that causes the small-signal gain to drop by 1 dB. If it's plotted on a log-log scale as a function of the input level, the output level falls below its ideal value by 1 dB at the 1-dB compression point.

When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are not harmonics of the input frequencies. Called inter-modulation (IM), this phenomenon arises from multiplication of the two signals when their sum is raised to a power greater than unity. We assume that

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \quad (2.4)$$

Thus, $y(t) = \alpha_1 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + \alpha_2 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2$

$$+ \alpha 3 (A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \quad (2.5)$$

Expanding the left side and discarding DC terms and harmonics, we obtain the inter-modulation products:

$$\omega \to 2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^{\,2} A_2}{4}\cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 A_1^{\,2} A_2}{4}\cos(2\omega_1 - \omega_2)t \quad (2.6)$$

$$\omega \to 2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2^{\,2} A_1}{4}\cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 A_2^{\,2} A_1}{4}\cos(2\omega_2 - \omega_1)t \quad (2.7)$$

Because the difference between ω_1 and ω_2 is small, the components at $2\omega_1$-ω_2 and $2\omega_2$-ω_1 appear in the vicinity of ω_1 and ω_2. In a typical two-tone test, A_1=A_2=A, and the ratio of the amplitude of the output third-order products to α_1A defines the IM distortion. If a weak signal accompanied by two strong interferers experiences third-order nonlinearity, then one of the IM products falls in the band of interest, corrupting the desired component.

Use IP_3 to characterize this behavior. Called the "third intercept point" (IP_3), this parameter is measured by a two-tone test in which A is chosen to be sufficiently small so that higher-order nonlinear terms are negligible and the gain is relatively constant and equal toα_1. The third-order intercept point is defined to be at the intersection of the two lines [2].

2.1.2 Strongly Nonlinear Effects

Strongly nonlinear effects refer to the distortion of the signal waveform that is caused by the limiting behavior of the transistor. The drain current exhibits cutoff, or

pinch-off, when the channel is completely closed by the gate-source voltage and reaches a maximum, or open-channel condition, in which further increase of gate-source voltage results in little or no further increase in drain current.

2.1.3 Nonlinear Device Models for CAD

To devise a comprehensive model for a device, it is necessary to characterize both the weak and the strong nonlinear behavior. Unfortunately, each of the nonlinearity traits in a particular device arises from quite different aspects of the device physics. The PA designer is much more sensitive to some of the shortcomings of widely used computer-aided design (CAD) models than designers of many other kinds of RF devices. The central issue in modeling RF power transistors is scaling. The detailed modeling and curve fitting are done on a small periphery sample device and may be quite accurate. The PA designer has to take that small cell and scale up it, even hundreds, to “build” a power transistor. Unfortunately, such scaling is not a simple set of electrical nodal connections, and can not be handled easily enough on a modern circuit simulator. The large periphery device will display a range of secondary phenomena that may have been quite negligible in the small periphery device model cell. The low impedance by multiple parallel connections evokes other-effects to come, that would be neglected in normally, including current spreading at bond-wire contacts, electro-acoustic coupling in the semiconductor crystal, and mutual coupling

between bond-wire.

Even a basic I-V measurement can pose serious difficulties for an RF power transistor. Mary I-V curve tracers work at speeds several slower than the RF signal for which the model is require and can be slow enough that transient junction heating effects, which will not occur to any significant extent during an RF cycle, intrude into the measurement. Accurate I-V curve are difficult to obtain for RF power transistors; that has led many to develop custom-built teat rigs, usually incorporating a pulsed measurement scheme [10]. An alternative approach is to build a curve tracer that sweeps through the I-V characteristics at rates in RF range [9].

Reference [11], [12], [15-17] provides starter bibliography, but the research continues.

2.1.4 Gain Match and Power Match

We can get the maximum gain when input and output of circuits was conjugate match. It is well known by circuit theorem that we can deliver maximum power into load component when load impedance is equal to real part of the generator impedance, and the reactive part should be resonated out. This is the concept of conjugate match or gain match. However, the practical devices have physical limited such as V_{max} and I_{max}, the maximum supply voltage and the maximum generated current. V_{max} could be maximum DC supply voltage or breakdown voltage of devices; and I_{max} could be

saturation current of devices. By referring Figure 2-1, this seen the gain match cannot used the full capacity of transistor. If we want to utilize the maximum current and voltage swing of the transistor, a lower value of load resistance would need to be selected; the value is commonly referred to as the load-line match, Ropt, and in its simplest form simply would be the ratio:

$$R_{opt} = V_{\max} / I_{\max} \tag{2.8}$$

Where we assume the generator's resistance is high and is not taken into account. This R_{opt} is so called the load-line match or power match. The power match represents a real compromise that is necessary to extract the maximum power from RF transistors and at the same time keep the RF voltage swing within specified limits and the available dc supply.

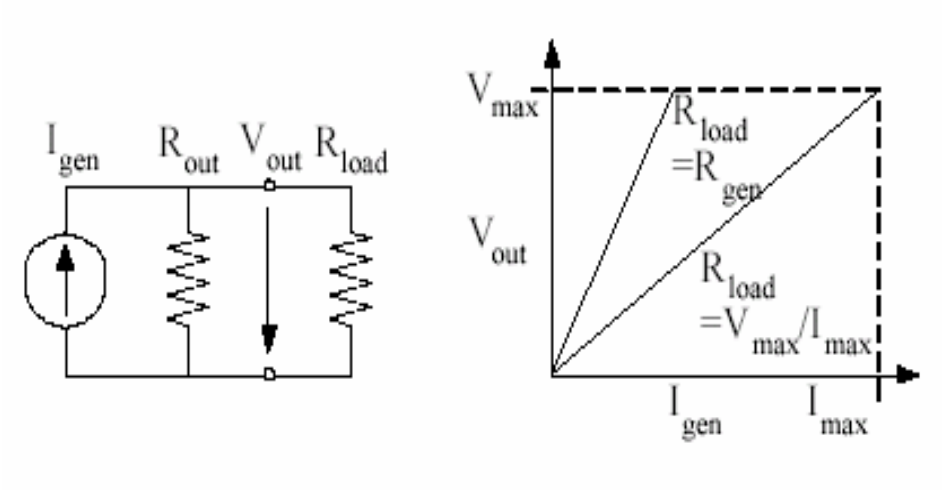


Figure2-1: Conjugate match and load-line match.

2.1.5 Knee voltage effect

The knee voltage (pinch-off voltage) divides the saturation and the linear region of the transistor and can be defined as, for example, V_{ds} at the 95% of I_{max} point. As shown in Figure 2-2[18]. And the optimum load resistance become

$$R_{opt} = (V_{\max} - V_{knee}) / I_{\max} \tag{2.9}$$

For sub-micron CMOS transistors, V_{knee} is only about 10% to 15% of the supply voltage for typical power transistors, while it can be as high as 50% of the supply for deep sub-micron technologies as shown in Figure 2-2. A large portion of the RF cycle could be in linear region. Accordingly, both saturation and linear region must be considered when determining the optimum of operation [18] or relying on balance simulations of circuits.

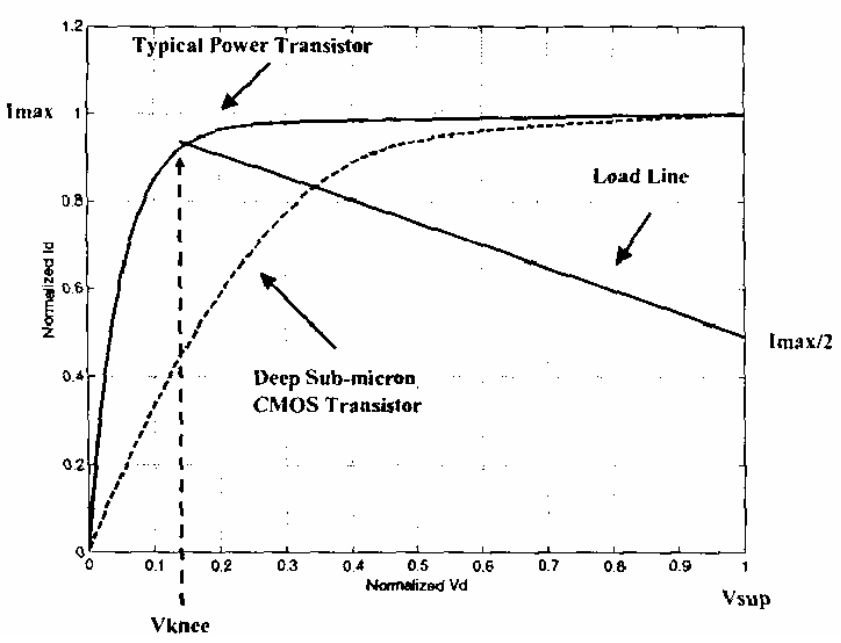


Figure2-2: The knee voltage of deep sub-micron CMOS transistor.

2.1.6 Load-Pull Measurement

A load-pull test setup consists of the device under test with some form of calibrated tuning device on its output. A typical block diagram is shown in Figure 2-3.

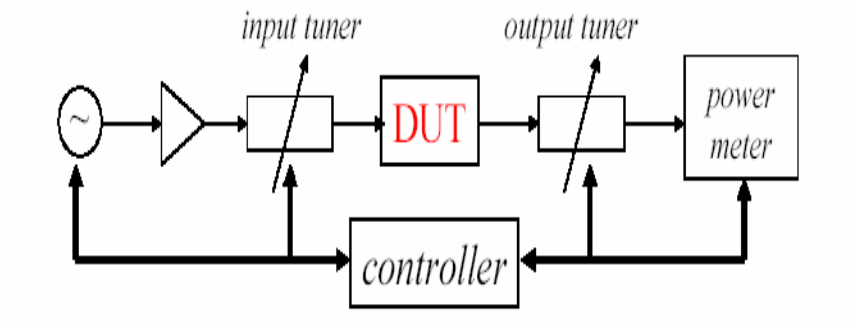


Figure 2-3: Typical configuration of load-pull.

The input probably also will be tunable, but this is mainly to boots the power gain of the device, and the input match typically be fixed close to a good match at each frequency.

Load-pull measurement can find the practical R_{opt} of PA, and also the maximum output power.

2.1.7 Input and Output VSWR

VSWR are measured at small-signal conditions as well as at large-signal conditions. There come some problems with power match, It will cause reflections and VSWR at output, the reflected power is entirely a function of the degree of match between the antenna and the 50-Ohm system. The PA does not present a mismatched reverse termination, which could be a problem in some situation. A questionable concept of

large signal impedance, once a device starts to operate in a significantly nonlinear fashion, the apparent value of the impedance will change, but the whole concept of impedance starts to break down as well, because the waveforms no longer are sinusoidal.

2.1.8 Power gain

The power amplifiers are characterized by transducer power gain defined as the ratio of the power delivered to the load (P_o) to the power available from the source (P_{in}) to the amplifier, i.e.,

$$G = P_o / P_{in} \tag{2.10}$$

2.1.9 Output Power and P_{1dB}

Power delivered to the load (P_o) is known as the output power, which is a strong function of the input power. The output power when the gain is compressed by 1 dB is defined as P_{1dB}, which is normally used as a figure of merit to characterize nonlinearity in amplifiers.

2.1.10 Power Added Efficiency (PAE), Drain Efficiency (ηd),and Power Utilization Factor

The PAE is defined as

$$PAE = \frac{output\_signal\_power - input\_signal\_power}{dc\_power} = \frac{Po - Pin}{Pdc}$$

$$PAE = \frac{Po}{Pdc}(1 - \frac{1}{G}) = \eta d(1 - \frac{1}{G}). \quad , \tag{2.11}$$

where ηd is known as the drain efficiency. For high-efficiency amplifiers, single-stage gain is required to be on the order of 10 dB or higher. If the RF power gain is less than 10 dB, the drive power requirement will start to take a serious bite out of output efficiency of a PA stage, and the higher the efficiency, the more serious the effect. Sometimes, it is just as well to keep gain and output efficiency as separate stage, it is noted that at system level or even multistage PA level they will behave interactively on the overall efficiency.

One of the most importance concepts in comparing different PA configurations is the power utilization factor (PUF). PUF is the ratio of the power it would deliver as a simple class A amplifier.

$$PUF = \frac{P\_rf}{Plin}, \tag{2.12}$$

$$Plin = \frac{Vdc * Ipk}{4}, \tag{2.13}$$

where P*lin* is known as the output power of class A having the same dc supply voltage and peak RF current.

2.1.11 Spectral Regrowth

In a digitally modulated waveform, for example, QPSK, need a low-pass filter precede the modulator to limit the bandwidth of the signal, there by suppressing spectral leakage into adjacency channels. We expect limiting the bandwidth tends to smooth out the abrupt transitions in the time domain. And after filtering, exhibiting

variation in its envelope as the filter bandwidth decreases. If the power amplifier is to maintain the spectrum to the limited bandwidth, then it must also amplify the envelope variations linearly. However, if the PA exhibits significant nonlinearity, then shape signals, it is not preserved and the spectrum is not limited to the desired bandwidth. This effect is called “spectral regrowth” [19], [20] and can be quantified by the relative adjacent channel power [20]. Generally, nonlinear PA has better efficiency than linear PA. Therefore, digital modulation schemes exhibit a trade-off between spectral efficiency and power efficiency.

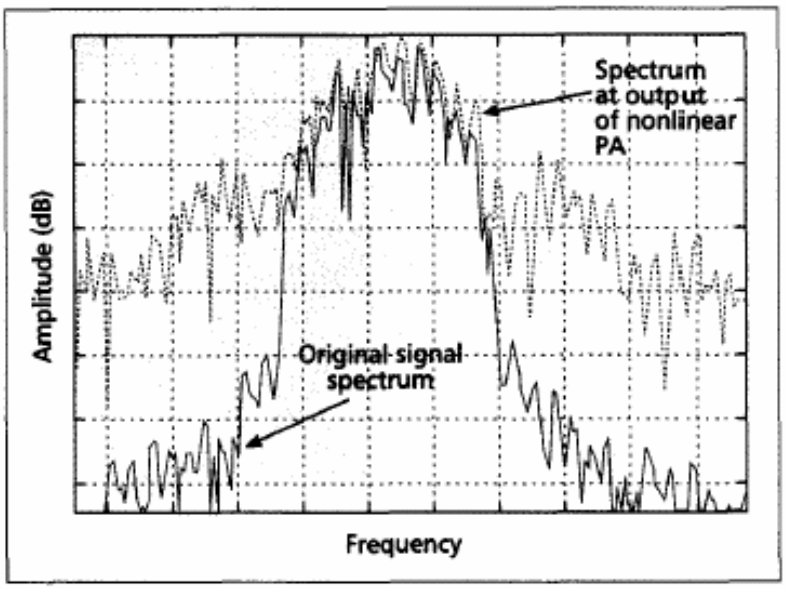


Figure2-4: The spectral regrowth due to amplifier nonlinearity.

2.1.12 Adjacent Channel Power Ratio (ACPR) [21]

ACPR is a commonly used figure of merit to evaluate the inter-modulation performance of RF power amplifiers designed for CDMA wireless communication systems, ACPR is a measure of spectral regrowth, appears in the signal sidebands, and

is analogous to IM3/IM5 for an analog RF amplifier.

$$ACPR = \frac{power\_spectral\_density\_in\_the\_main\_channel\_1}{power\_spectral\_density\_in\_the\_offset\_channel\_2or3}, \quad (2.14)$$

There offset frequencies and measurement bandwidths vary with system application.

2.1.13 Peak-to-Average Ratio (PAR) [22]

All single or multi-carrier (modulated or un-modulated) have a peak-to-average ratio. The ratio between the peak power (P_p) and the average power (P_a) of a signal is called the peak-to-average ratio, i.e.,

$$\chi = \frac{Pp}{Pa}, 10\log\frac{Pp}{Pa}(dB). \quad (2.15)$$

The peak-to-average ratio ΔP_s of an input signal consisting of N carriers, each having a average power P_i is defined as

$$\Delta Ps = \frac{(\sum_{i=1}^{n}\sqrt{P_i\chi_i})^2}{\sum_{i=1}^{n}P_i}. \quad (2.16)$$

Here χ_i is the peak-to-average ratio of the i_{th} carrier. If there are n carriers in a given operating bandwidth, it is easy to see that the theoretical maximum peak-to-average power ratio will be $\sqrt{n}$. Gaussian noise has a peak-to-power ratio of about 9 dB, so very dense multi-carrier systems might require about 6 dB more power back-off to achieve a similar level of IM distortion compared to a two-carrier signal having the same power.

2.1.14 Nonlinearity Effect in Power Amplifier Use Two-tone Analysis

There many different ways to measure the nonlinearity behavior of an amplifier. The simplest method is the measurement of the 1dB compression power level P1dB. Another method that uses two closely spaced frequencies:

$$Vi(t) = v\cos(\omega_1 t) + v\cos(\omega_2 t) \tag{2.17}$$

V_i input to amplifier and measure the output frequencies component, this is so-call the inter-modulation (IM) products. The third-order products are at frequencies 2ω2-ω1 and 2ω1-ω2, and the fifth-order IM products are at frequencies 3ω2-2ω1 and 3ω1-2ω2. The third-order Intercept point (IP3) is a concept that represents the intersection between the extrapolated 1:1 slope of fundamental gain, and the 3:1 slope of the third-order IM (IM3) products. IM3 is given by [23]:

$$IM3(dBc) = \frac{P_{2\omega_1-\omega_2}}{P_{\omega_1}} = \frac{P_{2\omega_2-\omega_1}}{P_{\omega_2}} = 2(IP3 - P_f) \tag{2.18}$$

,

where P_f (dBm) is the average value of $P_{\omega 1}$ and $P_{\omega 2}$.

Another “softness” of the compression characteristic can be varied by choosing two tangible parameters, P_{COMP} and P_{SAT}. P_{COMP} represent, in decibels, the different between the P_{1dB} compression point and the maximum linear power point; P_{SAT} represent, in decibels, the different between the saturated power point and the maximum linear power point, about this value, the characteristic is defined to be ideally flat, or saturated. The detail discuss of nonlinear effect can be studied at [24].

2.1.15 AM-to-PM Effect

Any amplifier, when driven into a strongly nonlinear condition, will exhibit phase as well as amplitude distortion.

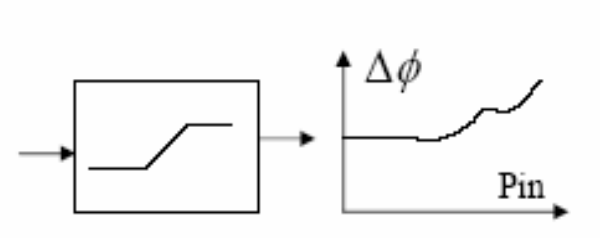


Figure 2-5: The phase-shift distortion with input power increases.

This usually is characterize in terms of AM-to-PM conversion and represents a change in the phase of the transfer characteristic as the drive level is increased toward and beyond the compression. The most common manifestation of AM-to-PM effects is an irritating asymmetrical slewing of the inter-modulation (IM) or spectral regrowth display. The detail discuss of AM-to-PM effect can be studied at [24].

2.2 Class of Power Amplifiers

What determine the class of operation of power amplifier is conduction angle of amplifier, input signal overdrive, and the output load network. Figure 2-6 shows how the PA relates to conduction angle and the input signal over-drive. For a small RF input signal V_{in}, the amplifier can operate in class A, AB, B, or C depending on the conduction angle (bias voltage relative to the transistor's threshold voltage).

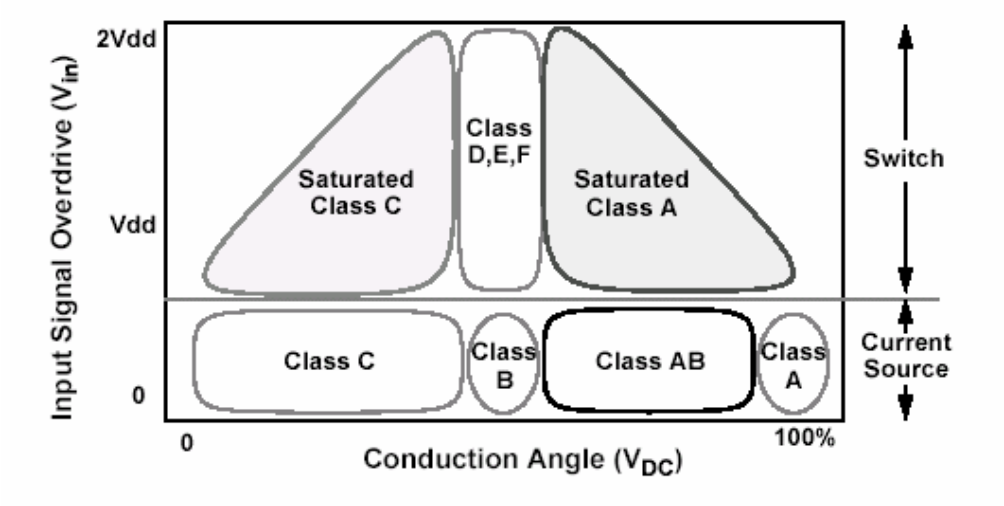


Figure 2-6: The classification of Power amplifier.

The PA efficiency can be improved by reducing its conduction angle by moving the design into class C operation, but at the expense of lower output power. An alternative approach to increasing efficiency without sacrificing output power is to increase the input over-drive such that the transistor acts as a switch.

2.2.1 Class A, AB, B, and C Power Amplifiers

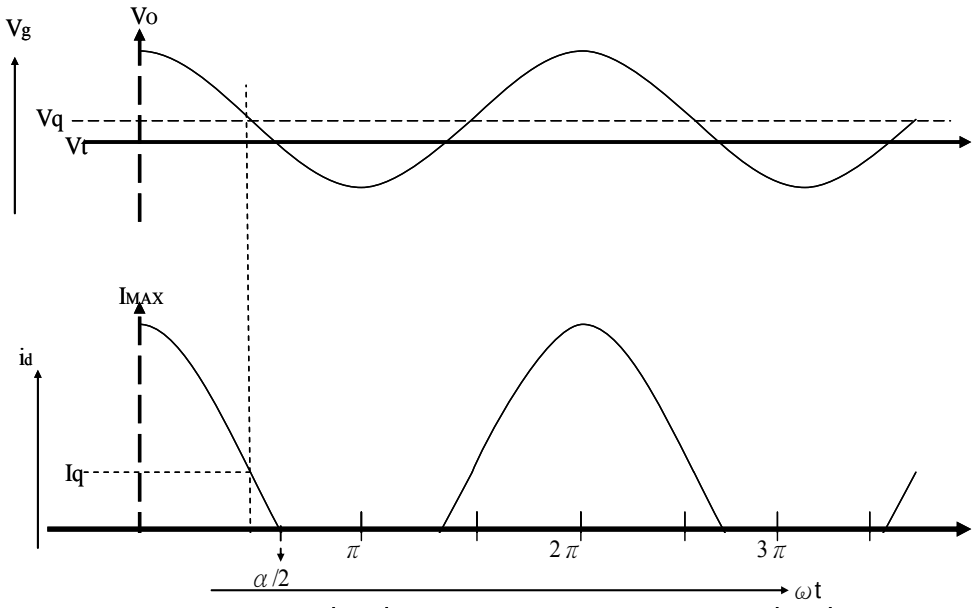


Figure 2-7: Reduced conduction angle current waveform.

The simple process of reducing the conduction angle is illustrated in Figure 2-7, where V_t is the threshold voltage of V_{gs} for transistors. The required signal voltage amplitude will be

$$V_s = 1 - V_q \tag{2.19}$$

Where Vq is the normalized quiescent bias point, defined according to Vt=0, Vo=1. The current in the device has the familiar looking, truncated sine-wave appearance. The conduction angle, α, indicates the proportion of the RF cycle for which conduction occurs, the current cutoff points point are at ±α/2. So the drain current waveform can be written as

$$\begin{aligned} i_d &= I_q + I_{pk}\cos\theta \quad -\alpha/2 < \theta < \alpha/2 \\ i_d &= 0 \quad -\pi < \theta < -\alpha/2; -\alpha/2 < \theta < \pi \end{aligned} \tag{2.20}$$

By Fourier analysis of the waveforms, the results can be written:

$$In = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{\max}}{1-\cos(\alpha/2)}[\cos\theta - \cos(\alpha/2)]\cos n\theta d\theta \tag{2.21}$$

then it is clear that

$$Idc = \frac{I_{\max}}{2\pi}\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}$$

$$I_{fundamental} = \frac{I_{\max}}{2\pi}\frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \tag{2.22), (2.23}$$

We use the conduction angle to define the class of power amplifier, for class A condition, α=0; for class B condition, α=π; for class AB condition, 0<α<π; and for the condition of class C, α>π. The harmonics amplitude is plotted in Figure 2-8.

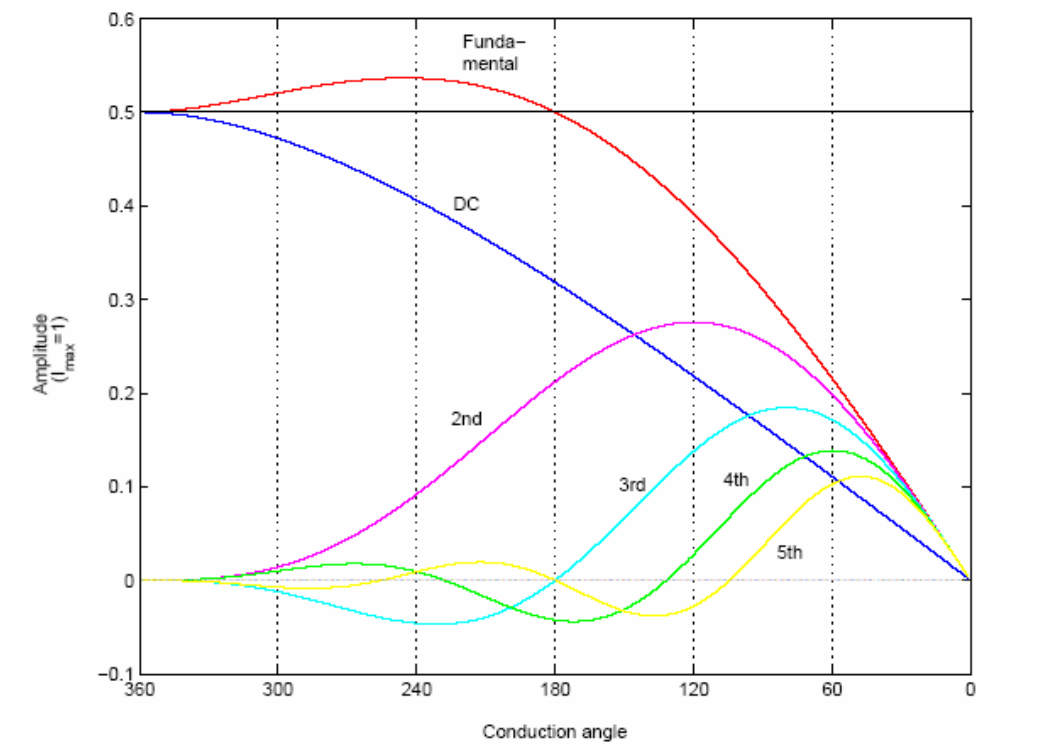


Figure 2-8: Fourier component of power amplifier relate to conduction angle.

We can see the odd harmonics be seen to pass through zero at the class B point, but in AB mode, the third harmonic is not negligible.

Then, the RF fundamental output power is given by

$$P1 = \frac{Vdc}{\sqrt{2}}\frac{I1}{\sqrt{2}}$$

$$Pdc = VdcIdc \quad , \qquad (2.24),\ (2.25)$$

the output efficiency is defined by:

$$\eta = \frac{P1}{Pdc} \quad , \qquad (2.26)$$

then we can plot the result on Figure 2-9. From this Figure the main features of class A, AB, B and C can be determined.

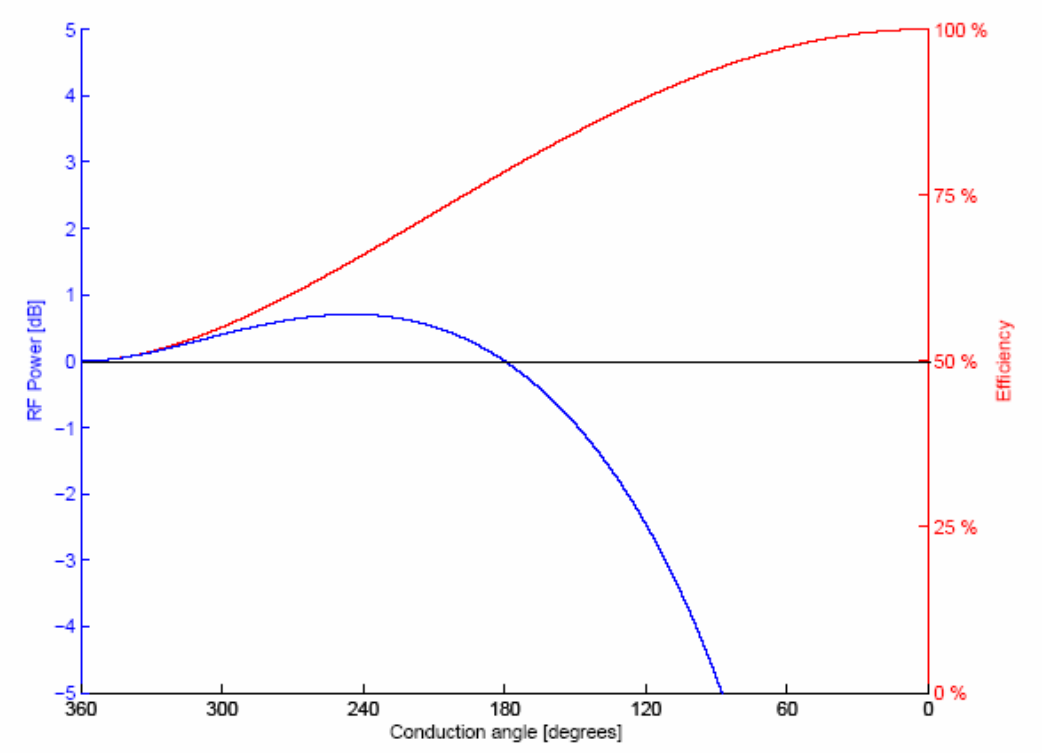


Figure 2-9: RF power and efficiency with conduction angle sweep; assume optimum load and harmonic short.

2.2.2 Class D, E and F Power Amplifier

In this class the active device works as a switch; with very low resistance in the "ON" state and very high impedance in the "OFF" state, and respect to the load impedance. If the "ON" resistance is negligible, no power dissipation in the device and if the "OFF" impedance is very large, no current flows through the device. Therefore, in an ideal switching amplifier one can achieve 100% drain efficiency. The different between a class D and a class E is that a class E amplifier has a high Q-tuned circuit at the output of the device provide desired reactive load at the fundamental frequency and open to other higher harmonics.

A class F amplifier is designed in the same manner as a class AB/B amplifier, except that the output circuit is designed to present a short circuit to the second harmonic and an open circuit to the third harmonic. The output waveform could become a square, such as a switch, and the theoretical efficiency approaches 100%.

Switch mode power amplifier in practice, efficiency could be degraded because the finite ON resistance and also there is significant transition time from the ON state to the OFF state and vice versa.

2.2.3 Power Amplifier Stability Issues

General speaking, k-factor analysis is useful to a linear two-port devices, it is usually a satisfactory assumption to assume that RF oscillations in power amplifiers will more likely occur when the amplifiers is backed off into its linear region, where the k-factor analysis is valid. At the condition of class AB or B operation, it is necessary to increase the quiescent current to perform the stability analysis with a represent amount of gain.

Stability of multi-stage amplifier is usually used k-factor analysis of individual stages. Any single stage must be designed with k-factor greater than unity from the low-frequency bias circuit range all the way up to the frequency at the gain rolls off to lower than unity. The use of resistive element will affect the efficiency of the PA, and is an effective way to obtain good stability performance.

$$k = \frac{1 - |S11|^2 - |S22|^2 + D^2}{2|S11||S12|}, D = S11 * S22 - S12 * S21 \quad ,. \qquad (2.27)$$

2.3 Challenges of RF Power Amplifiers in CMOS Technology

CMOS technology is not friendly towards design of power amplifiers. We simple list some issues that affected the PA performance.

2.3.1 Low Breakdown Voltage of Deep Sub-micron Technologies.

This limits the maximum gate-drain voltage and delivering lower power. Unfortunately, COMS technology has lower current drive, the single stage gain is very low, and multiple stages would be used but affect the linearity and efficiency of amplifiers.

2.3.2 Substrates Coupling Effects

In contrast to semi-insulating substrates, a highly doped substrate is common in CMOS technology. This results in substrate interaction in a highly integrated CMOS IC. The leakage from an integrated power amplifier might affect the stability of other circuits, for example the VCO or LNA.

2.3.3 Large Signal CMOS RF Models

Conventional transistor models for CMOS devices have been found to be moderately accurate for RFIC. And need to be improved for analog operation at radio frequencies. Large signal CMOS RF models and substrate modeling are critical to the successful design and operation of integrated CMOS radio frequency power

amplifiers, owing to the large currents and voltage changes that the output transistors experience [16]. So that, traditional PA design relies heavily on data measured from single transistors, such as load-pull measurement. It is noted that the RF model of TSMC 0.18μm is not sufficient accurate to support the large signal, because the RF devices only have one width with 5μm*(number of finger), and the source wire line would not sufficient width to supply the large current of large transistor. As the result, some un-expectably effect might cause the RF model un-accurate.

2.3.4 Low-Q Passive Element at the Output Matching Network

Since the inherent output device impedance in the power amplifier case is very low, impedance matching require higher impedance transformation ratios, it becomes very difficult. The output matching elements require lower loss, and good thermal properties since there are usually significant RF currents flowing in these elements. However, in CMOS technology, the losses in the substrate will decrease the quality factor (Q) of the passive element in the matching network, this great reduce the efficiency of circuits.

2.3.5 Electro-migration and Reliability of CMOS Devices

The power amplifier operation at a high output power state, large current and high voltage swing, this can be cause electro-migration and parasitic effect in the circuit may cause performance degradation [16] and reliability problems. After a long time,

the output power of PA should be degrade [25].

How long a CMOS PA can work? The recommended voltage to avoid hot carrier degradation is usually based on DC/transient reliability tests, and designer bias at the level below the result of tests [25].

Chapter 3

Basic Power Amplifiers Design

3.1 General consideration in RF Amplifiers

3.1.1 Stability

The stability of an amplifier is a very important consideration in a design and can be determined from the S parameters, the matching networks, and the terminations. The two-port network is shown in Figure 3-1.

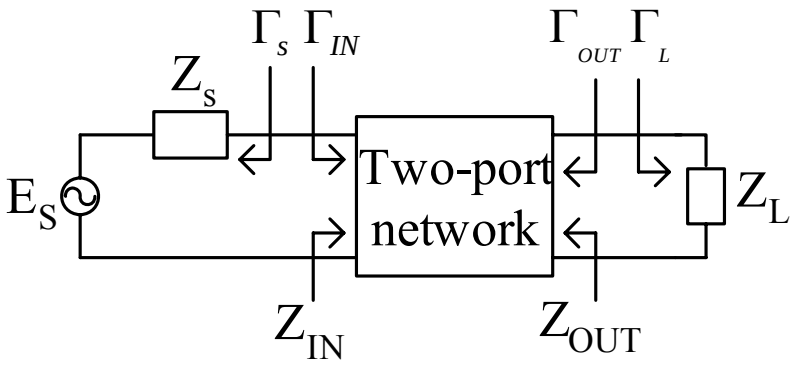


Figure 3-1: Stability of two-port networks.

A two-port network to be unconditionally stable can be derived from (3.1) to (3.4).

$$|\Gamma_s| < 1 \tag{3.1}$$

$$|\Gamma_L| < 1 \tag{3.2}$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{3.3}$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_S} \right| < 1 \tag{3.4}$$

For unconditional stability any passive load or source in the network must produce a

stable condition. The solution of (3.1) to (3.4) gives the required conditions for the two-port network to be unconditionally stable [5].

A convenient way of expressing the necessary and sufficient conditions for unconditional stability is

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}, \quad k > 1 \tag{3.5}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \qquad , |\Delta| < 1. \tag{3.6}$$

3.1.2 Impedance matching

Consider the RF system shown in Figure 3-2. Here the source and load are 50Ω (a very popular impedance), as are the transmission lines leading up to the IC. For optimum power transfer, prevention of ringing and radiation, and good noise behavior, for example, we needs the circuit input and output impedances matched to the system. In general, some matching circuit must almost always be added to the circuit.

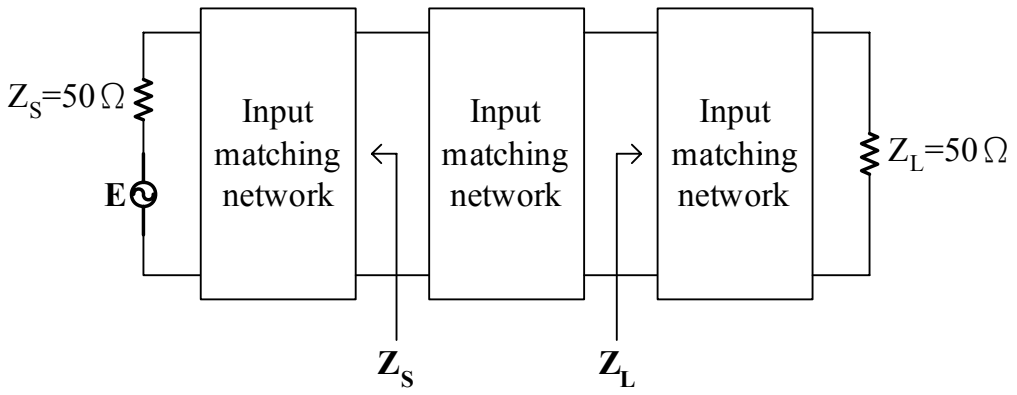


Figure 3-2: Circuit embedded in a 50-Ω system.

Typically, reactive matching circuits are used because they are lossless and because they do not add noise to the circuit which will only be matched at a range of frequency. If a broadband matching is required, then other techniques may need to be used. Note that, in general, the impedance of a circuit is complex $(R + jX)$.Then, to match it, the matching must be driven for its complex conjugate $(R - jX)$.

A more general matching is required if the real part is not 50Ω. For example, if the real part of Z_{in} is less than 50Ω, then the circuit can be matching using the circuit in Figure 3-3.

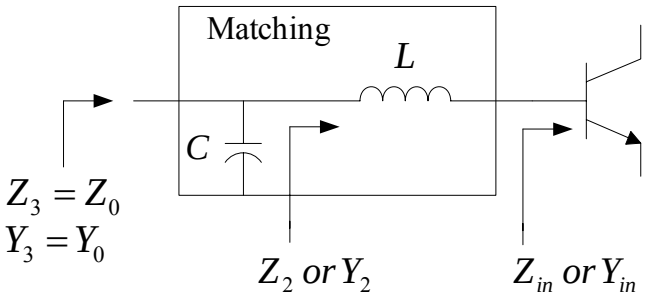


Figure 3-3: A possible impedance-matching network.

In order to the best power transfer into the circuit, it is necessary to match its input impedance to the source and the output impedance to the load. It's very common to use reactive components to achieve this matching because they do not absorb any power or add noise. Thus, series or parallel components can be added to the circuit to provide an impedance transformation. Series components will move the impedance along a constant resistance circle on the Smith Chart: series inductor for clockwise moving and series capacitor for counterclockwise. Parallel components will move the

admittance along a constant conductance circle: parallel capacitor for clockwise moving and parallel inductor for counterclockwise moving.

With the proper choice of two reactive components, any impedance can be moved to a desired point on the Smith Chart. There are eight possible two-components matching networks, also known as *ell* networks, as shown in Figure 3-4. Each will have a region in which a match is possible and a region in which a match is not possible.

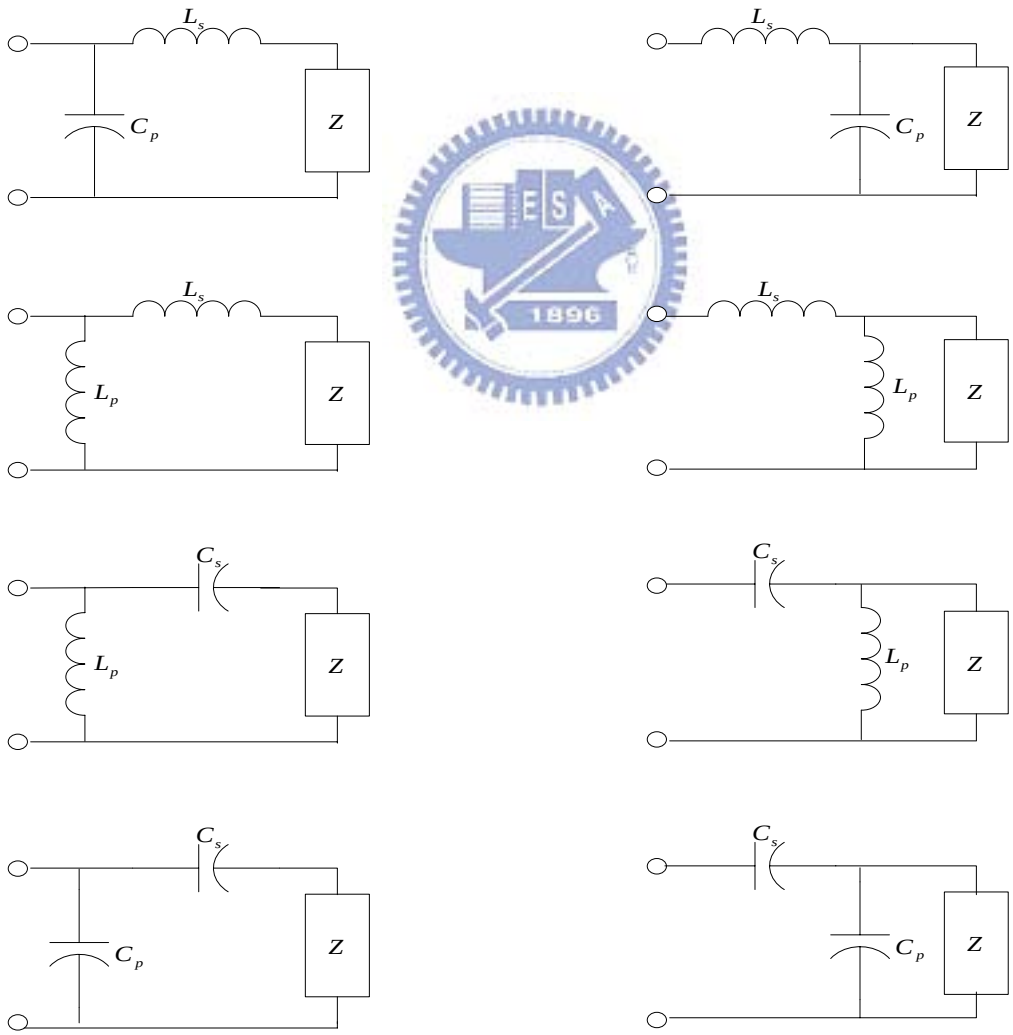


Figure 3-4: The eight possible impedance-matching networks with two components.

In any particular region on the Smith Chart, several matching circuits will work and others will not. This is illustrated in Figure 3-5, which shows what matching networks will work in which regions. Since more than one matching network will work in any region, how does one choose? There are popular reasons for choosing one over another:

1. Sometimes matching component can be used as dc blocks (capacitors) or to provide bias currents (inductors).
2. Some circuits may result in more reasonable component values.
3. Personal preference. Not to be underestimated, sometimes when all paths look equal, you just have to shoot from the hip and pick one.
4. Stability. Since transistor gain is higher at lower frequencies, there may be a low-frequency stability problem. In such a case, sometimes a high-pass network (series capacitor, parallel inductor) at the input may be more stable.
5. Harmonic filtering can be done with a low-pass matching network (series *L*, parallel *C*). This may be important, for example, for power amplifiers. [10]

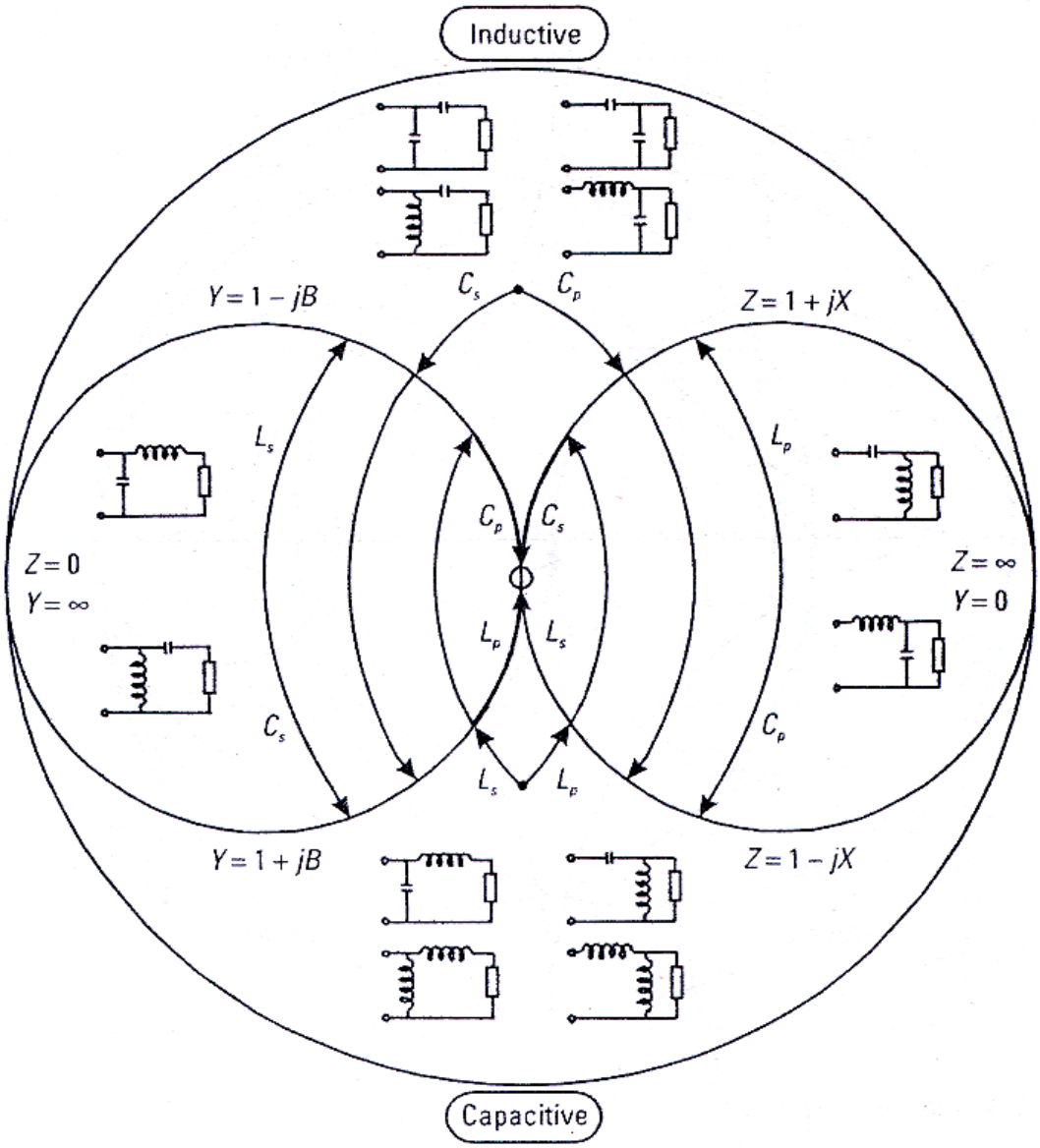
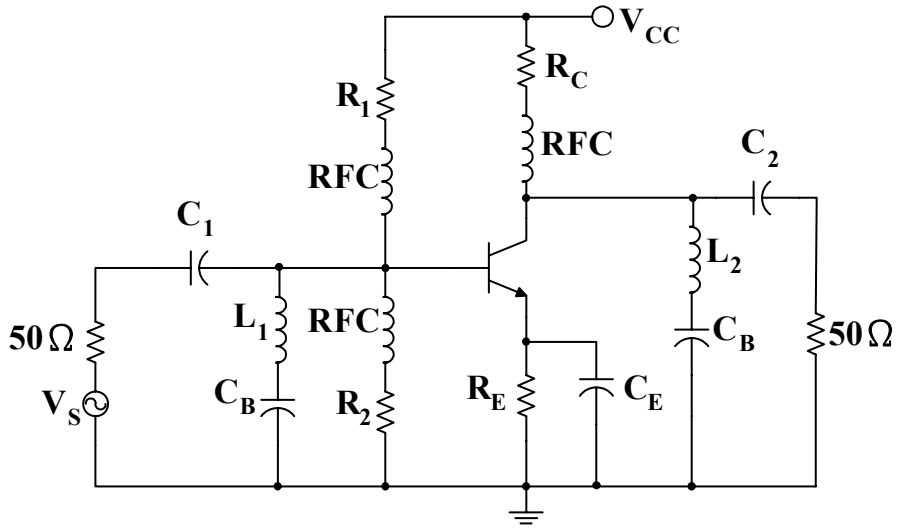
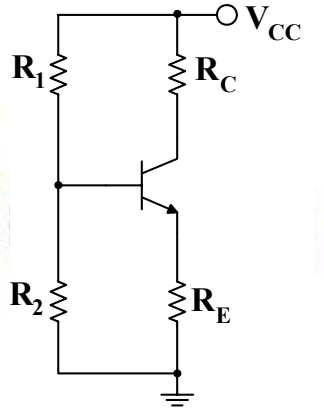


Figure 3-5: Which ell matching networks will work in which regions.

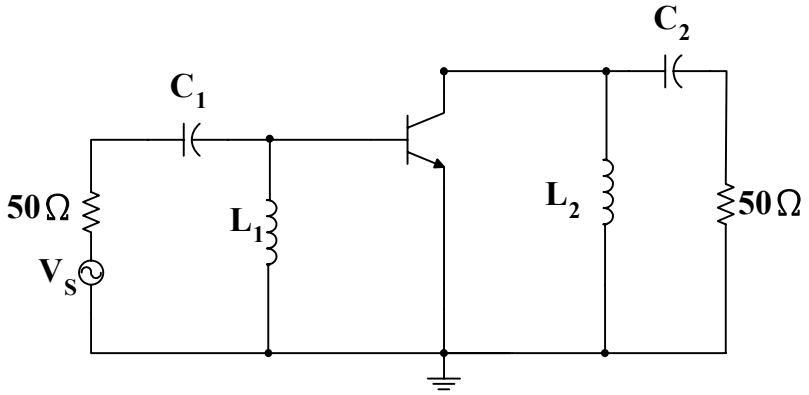
In a RF amplifier, the input and output matching networks provide the appropriate ac impedances to the transistor. The transistor must also be biased at an appropriate quiescent point. A complete RF amplifier contains both dc bias components and the ac matching network. RFC_S, bypass capacitors, and coupling capacitors need to be introduced so the dc bias components do not affect the ac performance of the amplifier. Illustrate conceptually in Fig. 3-6. [5]



(a)



(b)



(c)

Figure 3-6: (a) A discrete RF amplifier; (b) the dc model; (c) the ac model.

3.1.3 Special Topic for Output: Load-line Match

Continuing with this topic from Chapter 2, we again emphasize the load-line method because of its importance to the amplifier, especially to the PA. The method is to design the load of the power-oriented amplifiers and makes them to fit the I-V characteristic of the transistors which are the core of the amplifiers. If we operate the amplifier in the linear characteristic region of the device like the saturation region of the MOSFET, the output signal swings between V_{max} and V_{knee}; that is, the current varies from zero to I_{max}. In the V-I plot of the device, the slope of the "load line," from (V_{max} , 0) to (V_{knee} , I_{max}), is so called R_{opt}. Thus, when the amplifier has its output load which equals to R_{opt}, it will operate at the maximal DC variance range to deliver the RF power.

In general, the output load of out design goal seldom equals to the R_{opt} of the amplifier; hence, to design PAs, we usually adopt the matching network including the reactive device to transform R_{load} for R_{opt}, as shown in Figure 3-7.

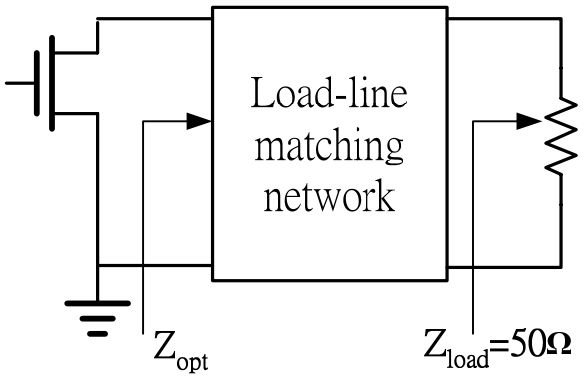


Figure 3-7: The load with the load-line matching network.

3.2 Conventional RF power amplifier design

3.2.1 Starting at LNA

It is well-known that the LNA is the pioneer of the PA because of the ease to extend concepts parameters of LNA to PA. So studying the design of the PA, we usually pick up those of the LNA. In the design of low noise amplifier, there are many key points. These include noise figure minimization, providing sufficient gain with good linearity, reasonable power consumption, and acceptable impedance matching. It is worthy of surveying that we just need to ensure the noise level low enough, not guarantee for minimum, because the input signal level of PA is higher than that of LNA. Fig 3-8 illustrates the input stage of the low noise amplifier with source degeneration. A simple calculation is

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs2}} + \left(\frac{g_{m2}}{C_{gs_2}}\right)L_s . \tag{3.7}$$

Choosing appropriate value of inductance and capacitance, then L_g+L_s and C_{gs} will resonate at certain frequency. By choosing L_s appropriately, the real term can be made equal to 50Ω. The gate inductance L_g is used to set the resonance frequency once Ls is chosen to satisfy the criterion of a 50Ω input impedance. The matching method in noise performance is better than using resistance termination of the input end.

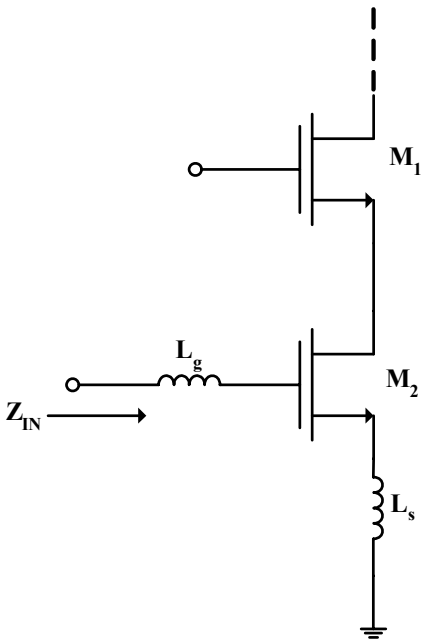


Fig. 3-8: Common source stage use inductance degeneration.

3.2.2 Wide-band amplifier design

For wide-band amplifier design, it's difficult to achieve the impedance matching in wide frequency range and gain flatness in it. Again, we start this topic at the wide-band LNA topology. Figure 3-9 is the LNA circuit schematic. We discuss this circuit step by step from the first stage. First, to make $1/g_m = 50\Omega$, the g_m value of common gate amplifier is going to be fixed at certain trans-conductance. An additional stage is required to provide sufficient gain over the desired band. A shunt feedback common source amplifier is used in the second stage for this purpose. The first step is the selection of transistor size and bias condition of the M1 to yield $\mathrm{Re}|Z_{11}| = 1/g_m = 50\Omega$. This ensures input matching condition for wide-band of frequency. But this condition is violated with optimum noise condition. There is a

trade-off between noise and impedance matching in the LNA circuit. One of the major problems in the wide bandwidth amplifier design is the limitation imposed by the gain-bandwidth product of the active device. We know that any active device has a gain roll off at high frequency because of the gate-drain and gate-source capacitance in the transistor. This effect degrades the forward gain as the frequency increases and eventually the transistor stops functioning as an amplifier at the high frequency. Therefore the second design step is the selection of optimal bias point of second stage of LNA so that it operates at its maximum f_T. In addition to this $|S_{21}|$ degradation with frequency other complications that arises in wide-bandwidth amplifier design includes, increase in reverse gain $|S_{12}|$ and noise figure at high frequency. Negative feedback configuration is used to reduce these effects and increase the bandwidth. An inductor L is connected in series with R_f such that after certain frequency the negative feedback decreases in proportion to the S_{21} roll-off. This technique improves gain flatness at high frequency. The load inductance of L_1 and L_2 replace the resistor load which is used conventionally. The magnitude of the inductor's impedance increases as frequency increases. This increase inductor impedance compensates the active device gain degradation that occurs at high frequency [13].

Another wide-band LNA design schematic is shown in Figure 3-10. In Figure 3-10, the R_f is added as a shunt feedback element to the conventional cascade narrow

band LNA and L_{load} is used as shunt peaking inductor at the output. The capacitor C_f is used for the ac coupling purpose. The source follower, composed of M_3 and M_4, is added for measurement proposes only, and provides wideband output matching. C_1 and C_2 are ac coupling capacitor. The small-signal equivalent circuit at he input of the LNA is shown in Figure 3-11. The resistor $R_{fM} = R_f /(1 - A_v)$ represents the Miller equivalent input resistance of R_f, where A_v is the open-loop voltage gain of the LNA. From equivalent circuit, the value of R_f can be much larger than that of the conventional resistance shunt-feedback. In the conventional resistance shunt-feedback, the size of R_f is limited as R_{fM} determines the input impedance. One of the key roles of the feedback resistor R_f is to reduce the Q-factor of the resonating narrowband LNA input circuit. The Q-factor of the circuit shown in Figure 3-11 can be approximately given by

$$Q_{WB} \approx \frac{1}{\left[R_S + \omega_T L_S + \frac{(\omega_0 L_g)^2}{R_{fM}} \right] \cdot \omega_0 \cdot C_{gs}} \tag{3.8}$$

From (3.8), and considering the inversely linear relation between the -3dB bandwidth and the Q-factor, the narrowband LNA in Figure 3-9 can be converted into a wideband amplifier by the proper selection of R_f. To design a wideband amplifier that covers a certain frequency band, the narrowband amplifier will be optimized at the center frequency. The feedback resistor R_f also provides its conventional roles of

flattening the gain over a wider bandwidth of frequency with much smaller noise figure degradation [14].

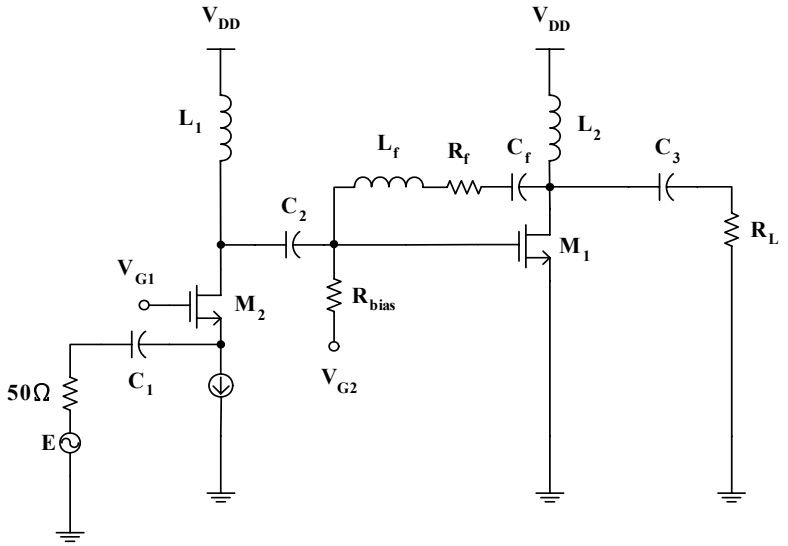


Figure 3-9: A wide-band LNA circuit schematic.

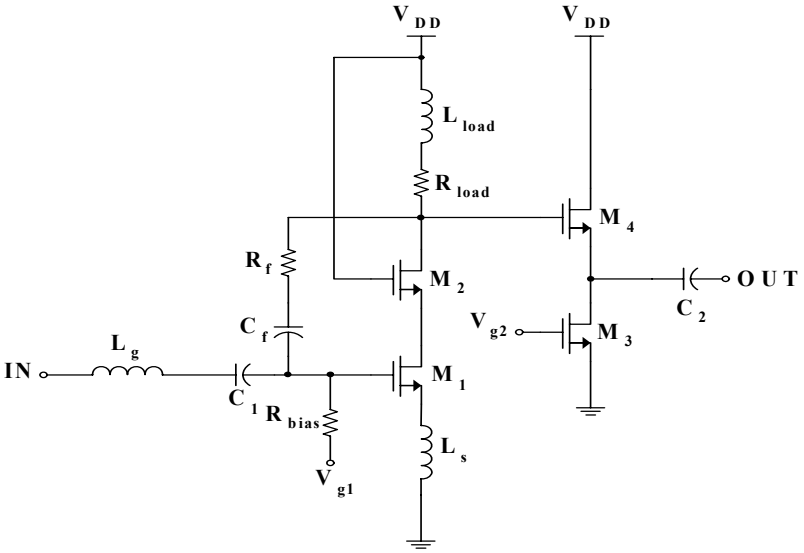


Figure 3-10: Another wide-band LNA schematic.

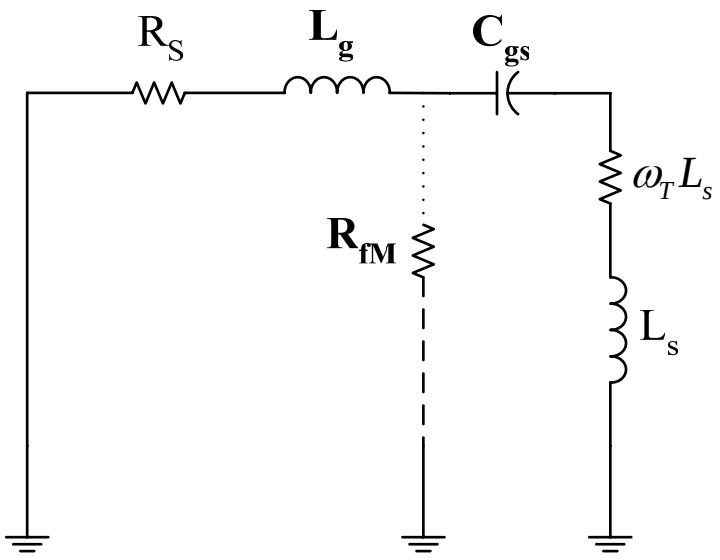


Figure 3-11: Small-signal equivalent circuit at the input.

Chapter4

UWB CMOS Power Amplifier design

4.1 The PA Issues of UWB Transmitter

In UWB systems, the power level from the UWB transmitter should be low enough not to interfere with the already existing communication systems, for example 802.11a. As shown in Figure 4.1[33], the low output levels that specified by the Federal Communications Commission (FCC) is less than -41.3 dBm/MHz. Therefore, for a 7 GHz bandwidth, the peak output power is approximately-3 dBm or 500 μW. UWB systems need not require large transistors, and greatly lighten the difficult of CMOS technology. The main challenging task becomes to achieve a high gain and good impedance match over the entire frequency band.

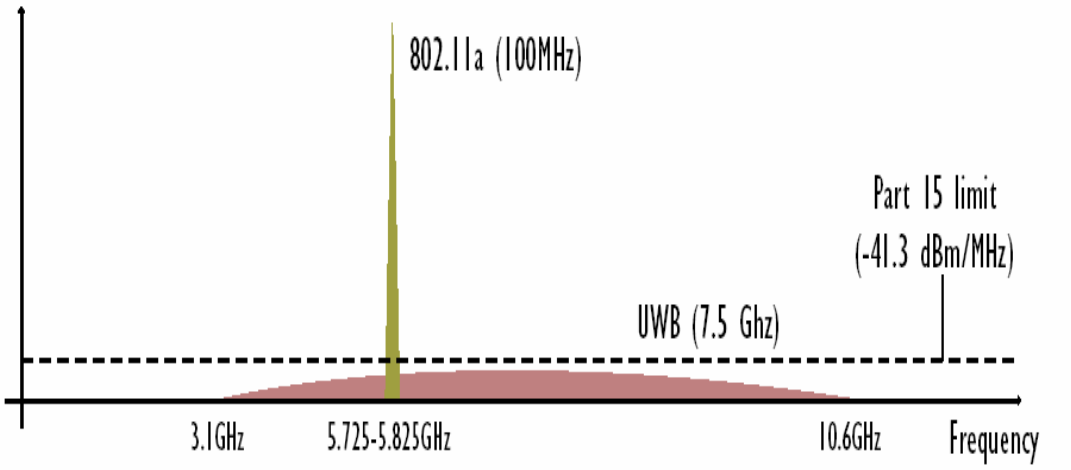


Figure 4-1: The power level of UWB.

Linearity is another issue in UWB systems. For constant envelope modulation schemes like GMSK, FSK, the amplitude remains constant and non-linear high

efficiency power amplifier is used. However, non-constant envelope modulation schemes like CDMA, the amplitude of the signal also carries some data information and hence it is important to maintain the exact shape of the signal without introducing any distortion through the power amplifier. It is noted that because the bandwidth of MB-OFDM is less than DS-CDMA, the linearity requirements is more relaxed.

4.2 UWB Design for CMOS Power Amplifier

In this chapter, we introduce a two stage power amplifier for UWB application. To design a UWB PA, the first consideration is to achieve wide bandwidth matching network. At the same time, gain flatness is another important goal of the wide-band amplifier design. There are many methods for wide bandwidth matching network, such as distributed amplifier (DA) and balance amplifier etc., but we'll provide our solution using CMOS PA design for these key points.

4.2.1 Input Matching: Cascode with Resistor Feedback

As we mentioned in Chapter 3.2, the cascade topology of resistor feedback is considered to starting my design at wide-band matching. Figure 4-2 shows the first stage of our design. The R_f is added as a shunt feedback element to the conventional cascade narrow band amplifier and L_{load} is used as shunt peaking inductor at the output. Figure 4-3 shows the small-signal equivalent circuit, in which the R_S means

the impedance of the signal source. The resistor $R_{fM} = R_f /(1 - A_v)$ represents the Miller equivalent input resistance of R_f, where A_v is the open-loop voltage gain of the cascode amplifier. From its equivalent circuit, the value of R_f can be much larger than that of the conventional resistance shunt-feedback. In the conventional resistance shunt-feedback, the size of R_f is limited as R_{fM} determines the input impedance. One of the key roles of the feedback resistor R_f is to reduce the Q-factor of the resonating narrow-band amplifier input circuit. Recalling (3.7), the impedance of the amplifier with source degeneration can be derived as

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \left(\frac{g_m}{C_{gs}}\right)L_s \approx \frac{1}{sC_{gs}} + \omega_T L_s \tag{4.1}$$

The Q-factor of the circuit shown in Figure 4-3 can be approximately given by

$$Q_{WB} \approx \frac{1}{\left[R_S + \omega_T L_S + \frac{(\omega_0 L_g)^2}{R_{fM}}\right] \cdot \omega_0 \cdot C_{gs}} \tag{4.2}$$

From (4.2), and considering the inversely linear relation between the -3dB bandwidth and the Q-factor, the amplifier can be converted into a wideband amplifier by the proper selection of R_f. To design a wideband amplifier that covers a certain frequency band, the amplifier will be optimized at the center frequency. The feedback resistor R_f also provides its conventional roles of flattening the gain over a wider bandwidth of frequency with much smaller noise figure degradation [14].

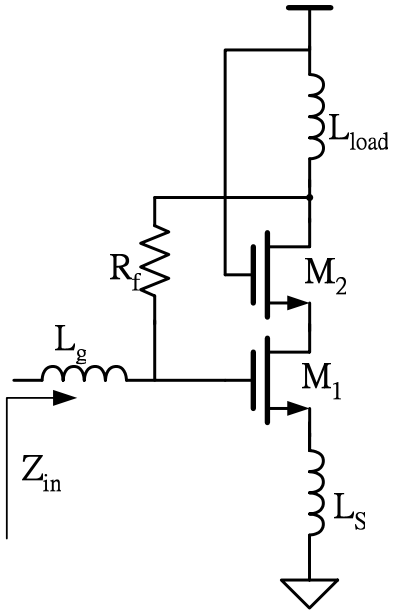


Figure 4-2: The input stage of our PA.

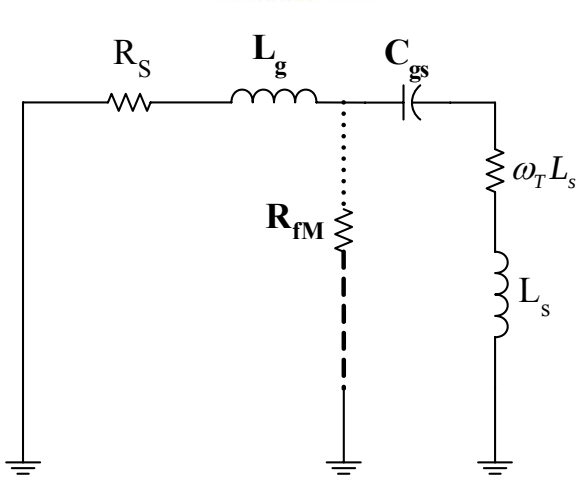


Figure 4-3: The small-signal equivalent circuit at the input.

4.2.2 Output Matching with Inductor-resistor Feedback

Output matching networks are also a problem to UWB PA. Since, antenna connect to the output of PA, the matching networks of PA must transfer to 50Ω for wideband application. As the components of matching network are increasing, the parasitic effects are also increasing. There come some bothering interferences such as power

loss, efficiency increase, and output noise increase.

In this work, we simplify output matching network by load-line theorem. The basic concept is selecting an optimum device it has optimum output load at 50Ω. By simulation of I-V curve, the inductor-resistor feedback topology not only benefits the goal of gain flatness but also has good performance for wideband design, as shown in Figure 4-4.

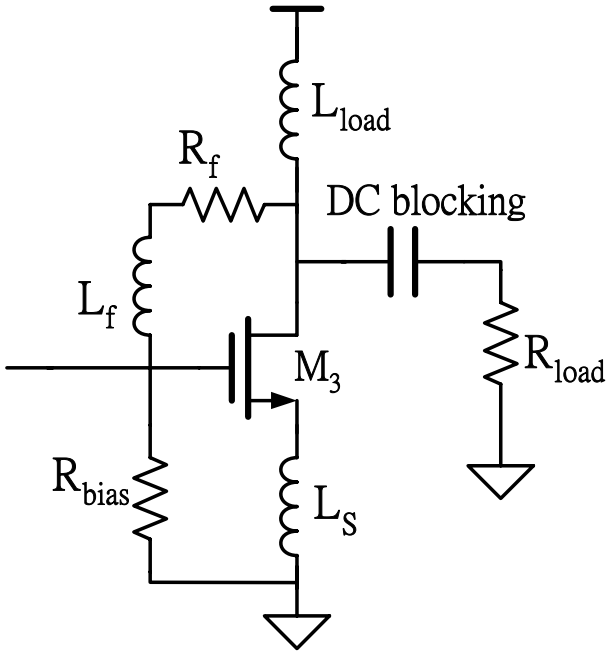


Figure 4-4: The output stage of our design.

Now we discuss the load-line result about this PA, as shown in Figure 4-5. In this case, the NMOS transistor of TSMC 0.18um process, has the width of160-um and the length of 0.18-um length. L_f is 2.25nH, R_{bias} is 350Ω, R_f is 150Ω, and L_{load} is 3.47nH. When R_{load} is 50Ω, we set the operation point of the bias to be 1.2V of V_{DS} and 0.8V of V_{GS}.

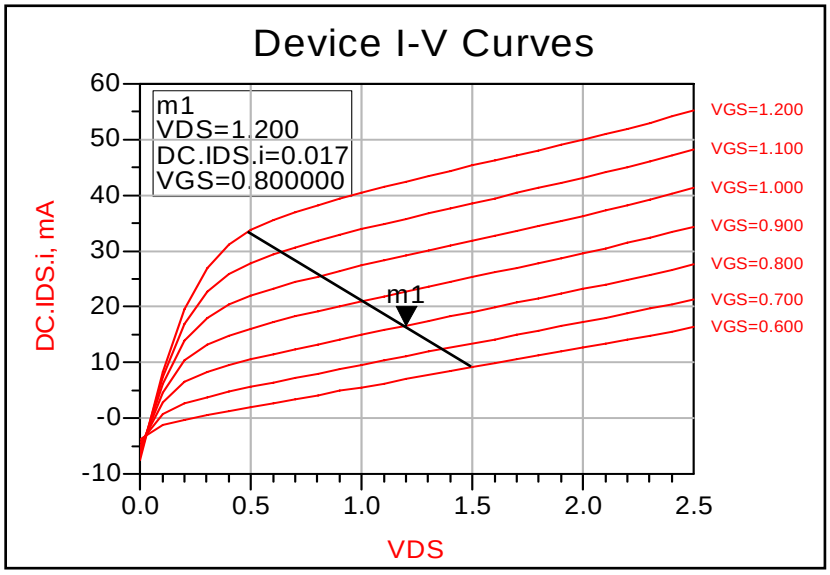


Figure 4-5: The I-V curve of the load-line study of the PA.

4.2.3 Gain flatness of amplifier with inductor-resistor feedback

This is the measurement of uniformity of the gain across the wide frequency range of interest. This parameter commonly used for wideband systems can impact pulse distortion in impulse-based UWB. It is desired that the gain be flat over the frequency band, typically a tolerance of ±0.5 dB.

It's worth discussing further for the feedback of our input stage. The feedback resistor, $R_{f1,}$ plays a key role for the gain as known in circuit theorems, and so do the L_{f2} and R_{f2} in the output stage. The resistor feedback can be design in such a way that it can provide the require match at both the input and output ends. Figure 4-4 show the characteristic of resistor feedback. Clearly, the low frequency gain drops due to small feedback resistor, and large feedback resistor provide good gain but have large gain variation, as shown in Figure 4-6. Since input impedance is usually on 50Ω,

small resistor can get better matching. Therefore, we might trade off between better matching and larger low frequency gain.

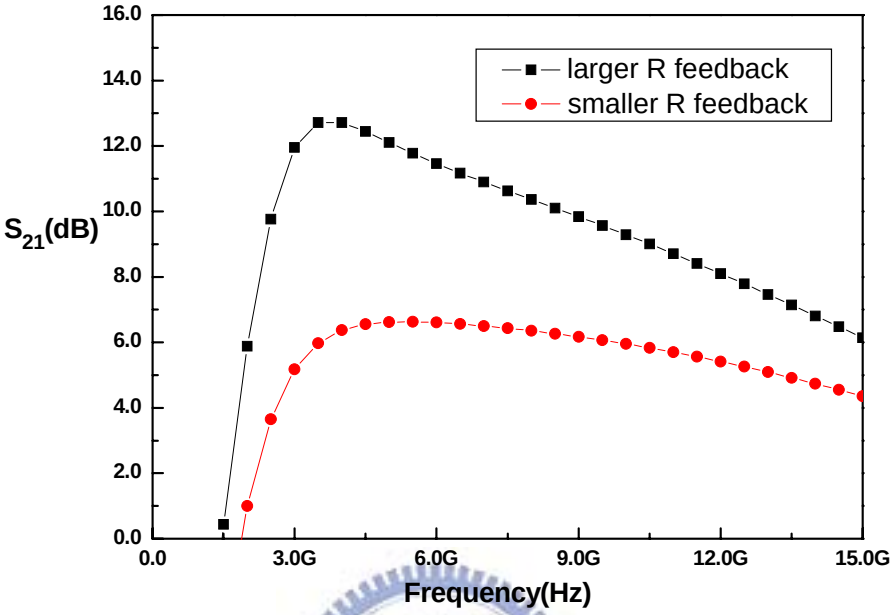


Figure 4-6: The comparison with the value of the feedback resistor.

We use inductor-resistor feedback to improve the gain at matching consideration. Inductor-resistor feedback impedance can be written as:

$$Z_f = R_f + X_f = R_f + j\omega L_f , \tag{4.3}$$

Analyzing with circuit theorem, the gain of the shunt-shunt feedback

$$A_f = \frac{A(j\omega)}{1 + A(j\omega)\beta(j\omega)}, \beta(j\omega) = -\frac{1}{Z_f}, A(j\omega) = \left.\frac{V_o}{I_i}\right|_{R_L=0} \tag{4.4}$$

In (4.4), $A(j\omega)$ means the open-loop trans-resistance gain. According to (4.3) and (4.4), it is clear that Z_f is small at low frequency and increase with the frequency raise. Therefore, the high frequency gain can slight increase. By cascading two stages, it should get flatness over the wide bandwidth. The concept is shown at Figure 4-7.

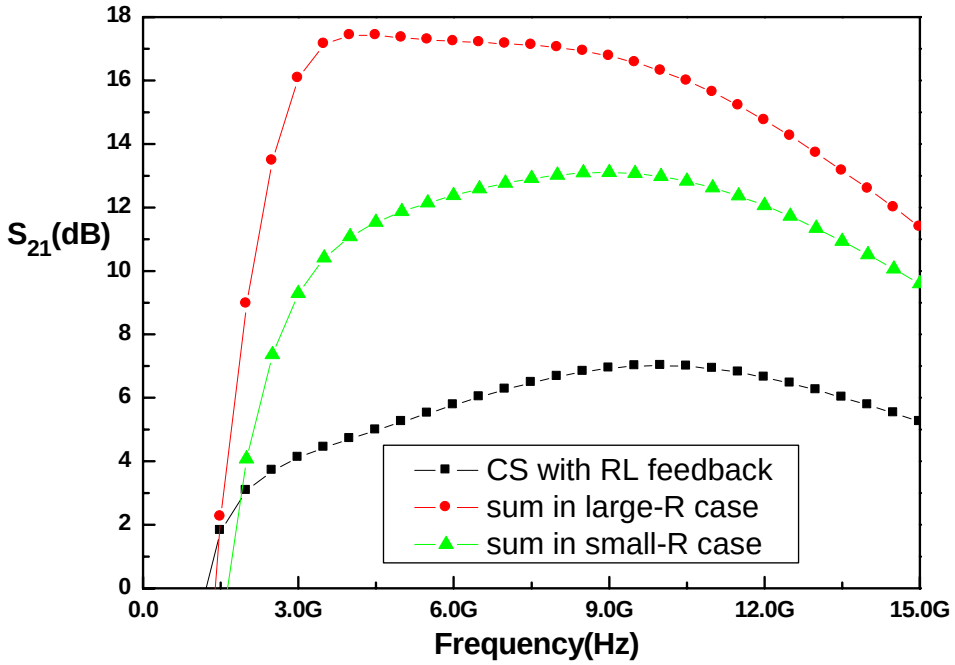


Figure 4-7: The $|S_{21}|$ of "common-source with RL feedback" and "two stages overall".

4.2.4 Detail of the Power Amplifier for UWB application

We start to design a two stage power amplifier and apply Advance Design System (ADS) for simulation tools, which can supports load-pull and large signal simulation. TSMC 0.18μm process is used in this work, and small signal model and large signal model are supported by TSMC. At first, we decide the transistor parameters. We choose the width per finger is 2.5um and the finger number of each NMOS is 64; so the width of each NMOS is 160um. Besides, we add two capacitors C_1 and C_2 in order to connect with the two stages: not only for inter-stage matching but also for the DC blocking purpose. After simulating, the total topology is decided as Figure 4-8 and the detail of the passive devices is listed on Table 4-1.

Device	Value	Device	Value
R_{f1}	400Ω	L_{f2}	2.25nH
L_{g1}	0.908nH	R_{f2}	150Ω
L_{load1}	2.45nH	L_{load2}	3.47nH
L_{S1}	0.1nH	C_2	2.85pF
C_1	0.951pF	L_{S2}	0.15nH
R_{bias}	350Ω		

Table 4-1: Passive devices of the PA.

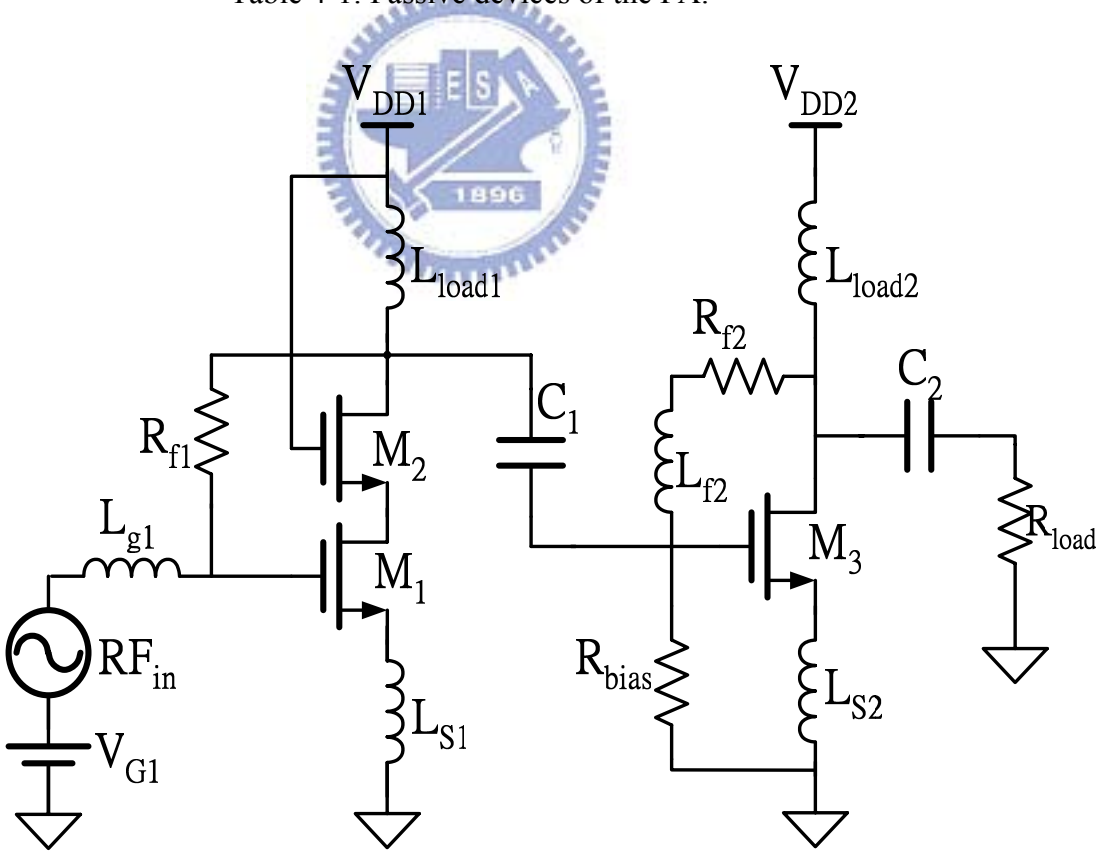


Figure 4-8: The overall schema of our UWB PA.

4.2.5 Simulation Results

To simulate the result, we apply 0.7V to V_{G1}, 1.8V to V_{DD1}, and 1.2V to V_{DD2} respectively. Figure 4-9 shows the simulated S-parameter. $|S_{11}|$ and $|S_{22}|$ are lower than -10dB between 3.1 and 10.6GHz. And $|S_{21}|$ is higher than 13.5dB at the same range in our simulation results. The -3dB bandwidth is 2.5~11.7GHz for the simulation. The noise figure (NF) of this UWB LNA is shown in Figure 4-10. The noise figure varies between 3.8 to 4.1 at 3.1~10.6GHz. Figure 4-11 shows one of the index representing the stability. This amplifier is unconditionally stable at any frequency. The two-tone test results for third-order inter-modulation distortion are shown in Figure 4-12. The test is performed at 8GHz. IIP3 is to 16.7dBm, and the input referred 1-dB compression point (ICP) is 3.98dBm. The proposed UWB PA dissipate 38.9mW with two power supplies; one is 1.8V, and the other is 1.2V. Table 4-2 represents the performance between 3.1G to 10.6GHz.

B.W. (GHz)	Power Gain(dB)	P-1db (dBm)	OIP3 (dBm)	PAEmax (%)	Power consumption (mW)
3.1~10.6	14.21~13.54 (15.18)	3.28~4.10 (3.99)	15.06~16.16 (16.691)	7.27~10.51 (10.79)	38.9

Table 4-2: The specification of the PA. In the brackets are the indexes at 8GHz.

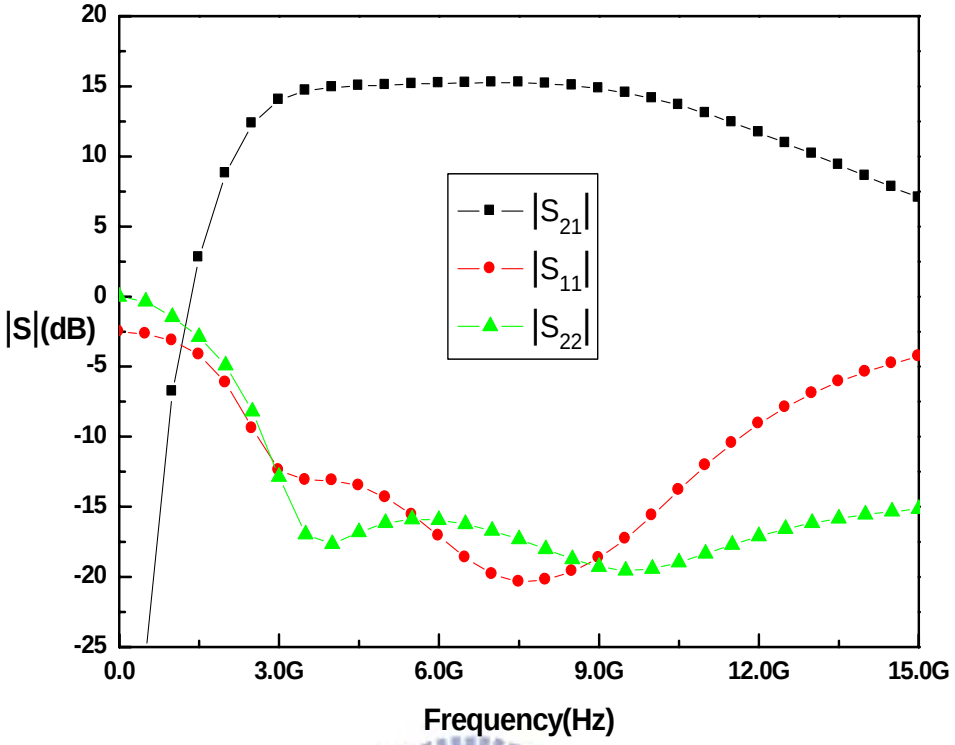


Figure 4-9: The S-parameter of the PA.

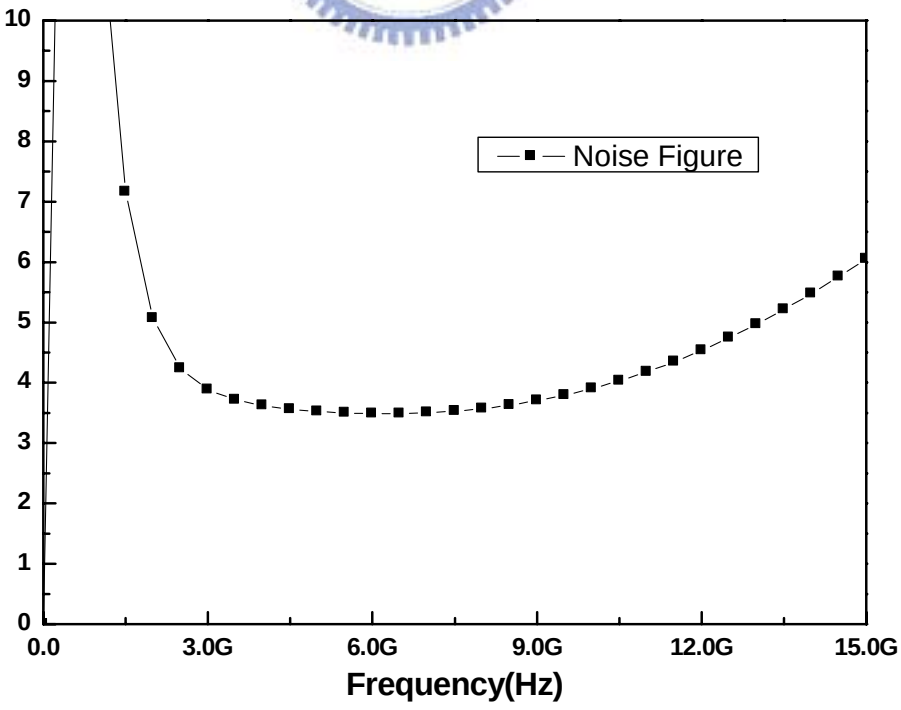


Figure 4-10: The Noise Figure.

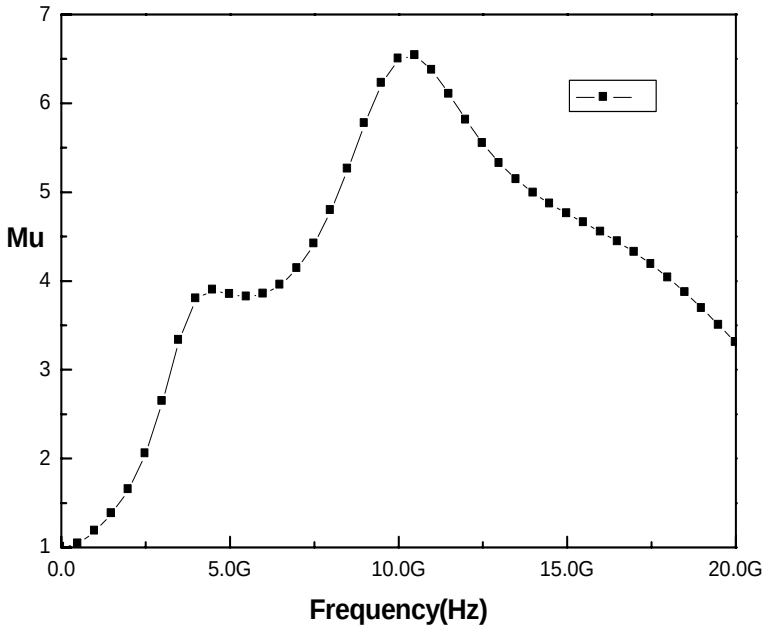
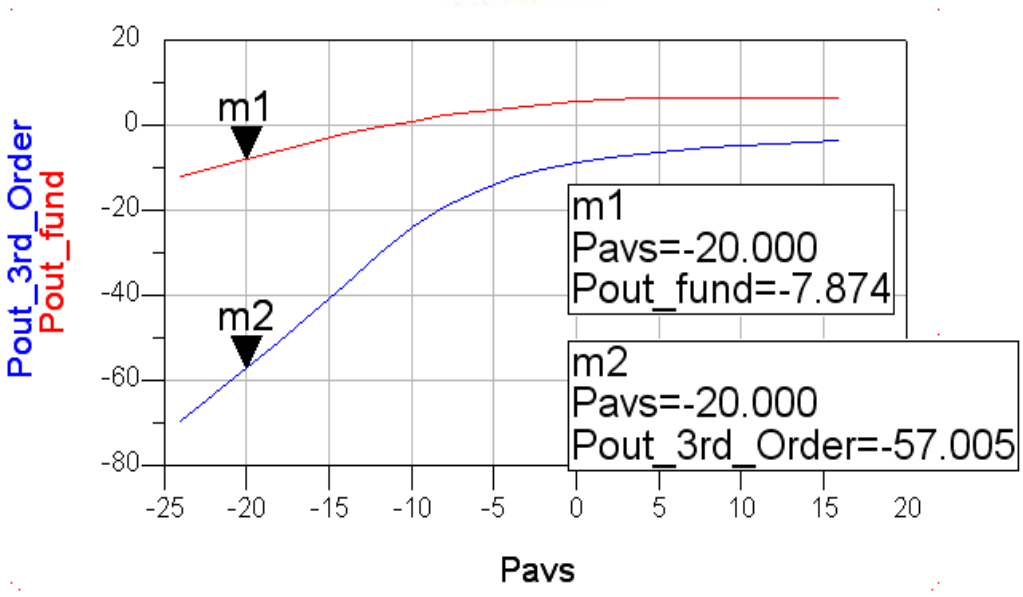


Figure 4-11: The stability index: Mu.



Pavs	TOI_output
-20.000	16.691

GainCompression	Pout_at_GainCompression
-1.002	3.984

Figure 4-12: The performance of PA in the aspect of linearity.

4.2.6 Layout

The layout is shown in Figure 4.13, the total size occupied by the PA is 0.98x0.83 mm^2, The capacitor is used metal-insulator-metal (MIM) capacitance supported by TSMC, the models of the resistor and inductor are supplied by TSMC. The metal width is decided according to the capacity of current flow and AC signal power. Input and output pads use GSG with 50Ω, and bias-tee is used for the input end.

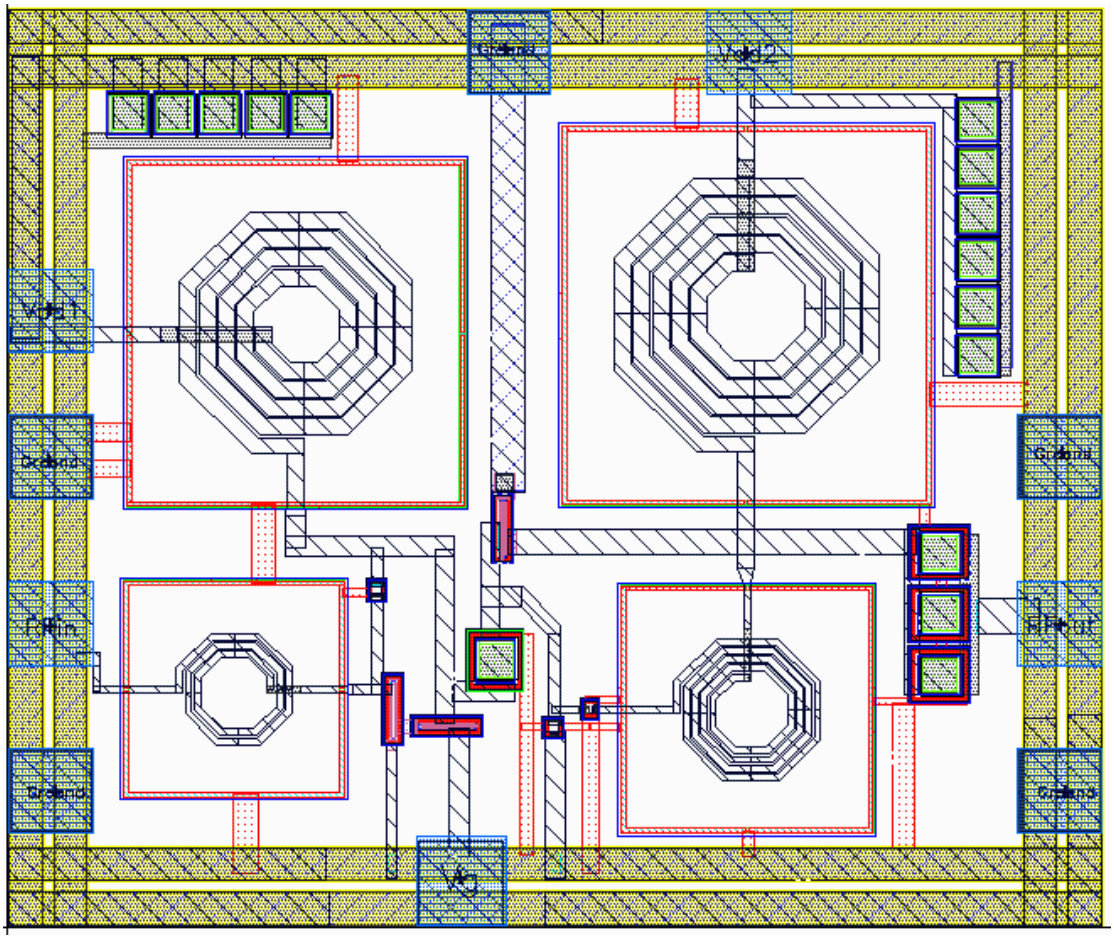


Figure 4-13: The layout of the PA.

4.3 Further Design for Better Efficiency and Linearity

Review Figure 4-5 again, and we will find the I-V curve inclined. Because it is asymmetric to the operation point, the output signal swings in a smaller range. Besides, the large signal linearity is limited. To improve these characteristics, we make a further design, as shown in Figure 4-14.

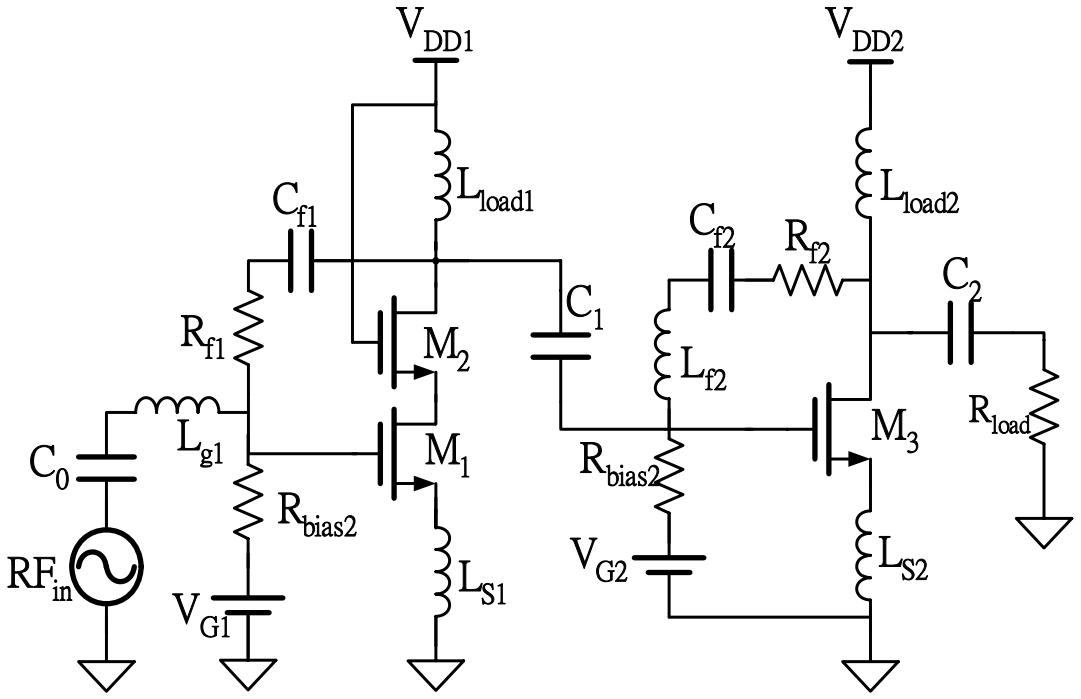


Figure 4-14: The further design of PA.

To take the advantages of previous PA, we choose the similar topology except for the DC-block capacitors on the feedback path. One capacitor is added on the input stage and the other is added for output stage. These capacitors play an important role to avoid the current leakage through the feedback path. In this work, the amplifier efficiency increases because of the better use for the DC power allocation.

4.3.1 Further Design by Load-line Curve

Beginning the topic to design a class A power amplifier, we need to take a look at Figure 4-15 and Figure 4-16. The size of the transistor and the DC bias condition must be synthesized. When we simulate the I-V curve for load-line decision, by the DC-block capacitor C_{f2} the impedance of Z_f is neglect and we obtain the vertical plot. Thus, we can decide the transistor size and locate the load-line easier. In Figure 4-16, the point m1 means the operation point (V_{DS}=1.8V ,and V_{GS}=1.1V) and m2 is represented as knee point as (V_{GS}=1.8V, I_{max}). The line connected with m1 and m2 is surely the desired load-line instead of the other line, called the optimum line, which passes to the punch-off region. Choosing the width as 100um, the R_{opt} is almost well-designed to 50Ω.

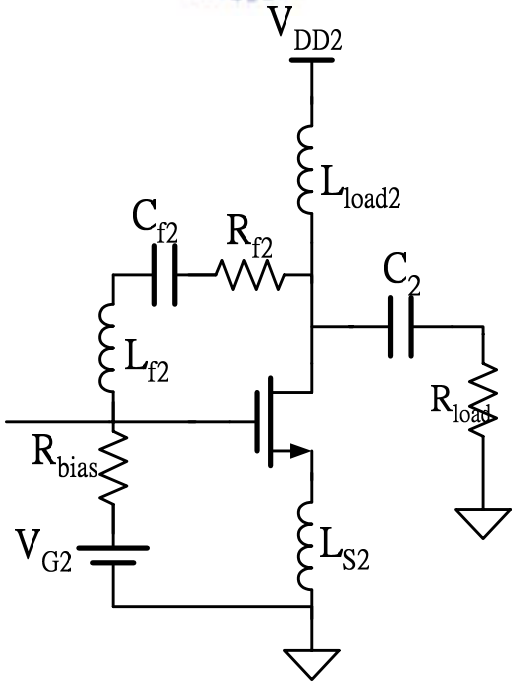
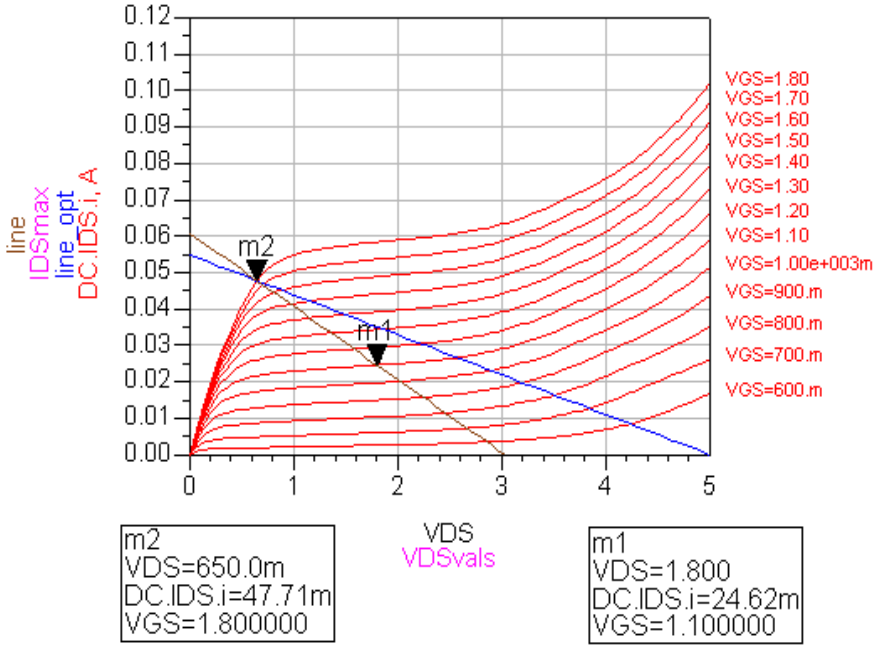
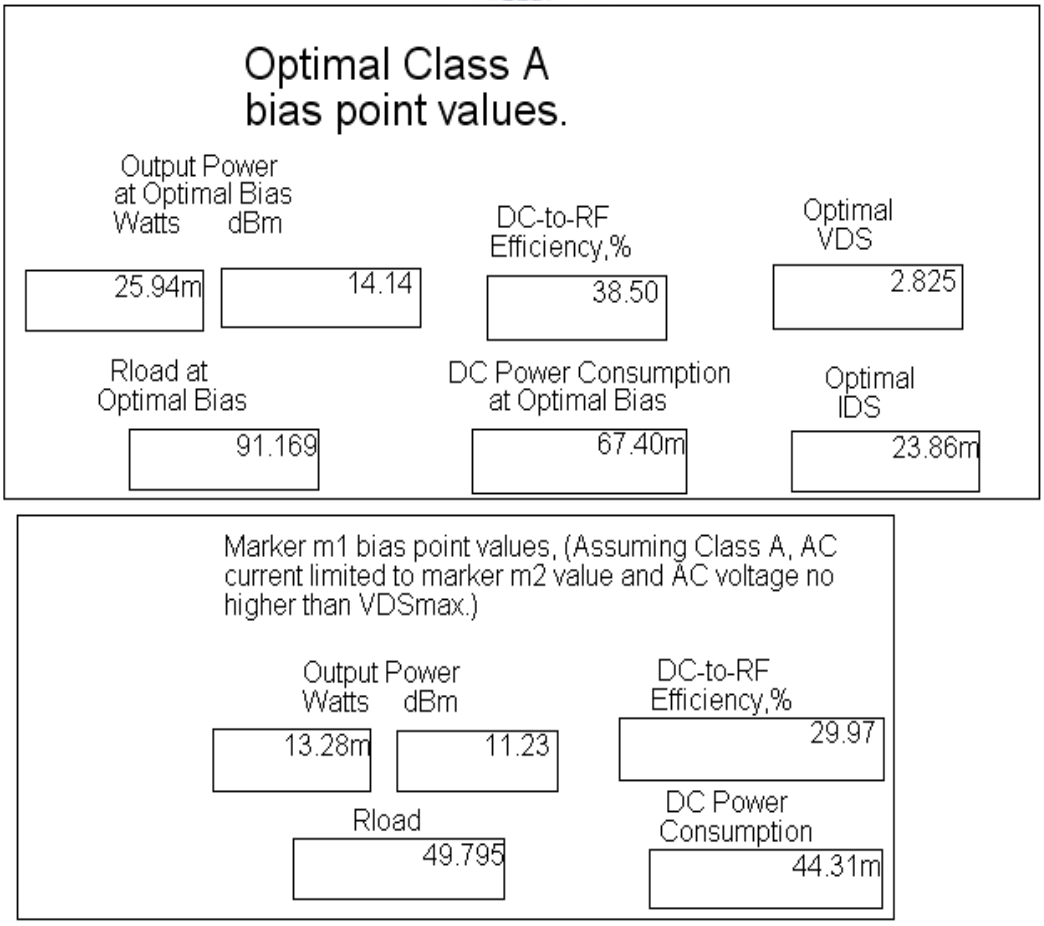


Figure 4-15: The output stage of the PA.



(a)



(b)

Figure 4-16: (a) The 50Ω-line and opt-line. (b) The load-line analysis by ADS tools.

4.3.2 Simulation for Further Design

The circuit has shown in Figure 4-14. By changing the transistor size and the circuit topology, we obtain a UWB PA for 3-8GHz applications. It is decided that the width of the transistor M_3 is 100um (2um per finger and 50 fingers.) To transfer signal from M_1 and M_2 to M_3, M_1 and M_2 must not be wider than M_3. Thus we design them as the same width. Table 4-3 figures out the value of each passive device. From Figure 4-17 to Figure 4-20 there are simulation results, and Table 4-2 represents the performance between 3GHz to 8GHz.

Device	Value	Device	Value
R_{f1}	850Ω	L_{f2}	3.27nH
L_{g1}	1.2nH	R_{f2}	250Ω
R_{bias1}	450Ω	R_{bias2}	1000Ω
L_{load1}	3.47nH	L_{load2}	3.47nH
L_{S1}	0.1nH	C_2	2.85pF
C_1	0.951pF	L_{S2}	0.1nH
C_{f1}	0.951pF	C_{f2}	0.951pF
C_0	DC block		

Table 4-3: The passive devices of the PA.

B.W.(GHz)	Power Gain(dB)	P_{-1db}(dBm)	OIP3(dBm)	PAEmax(%)	Power consumption (mW)
3~8Ghz	>16.67	8.532	23.110	15.914	70 @max PAE

Table 4-4: The specification of the PA.

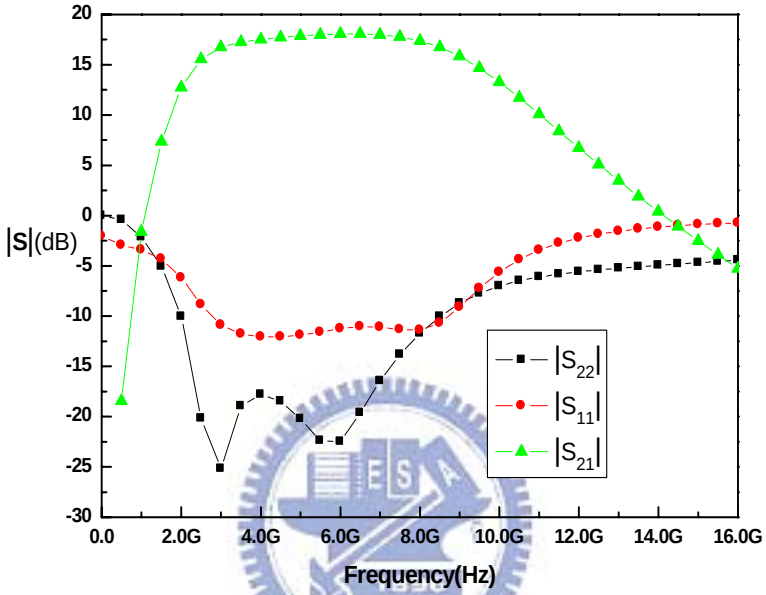


Figure 4-17: The S-parameter of the PA.

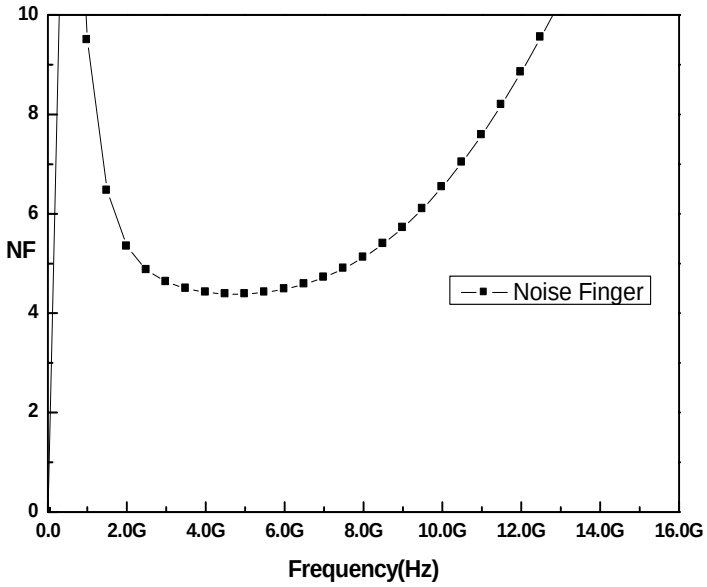


Figure 4-18: The Noise Figure.

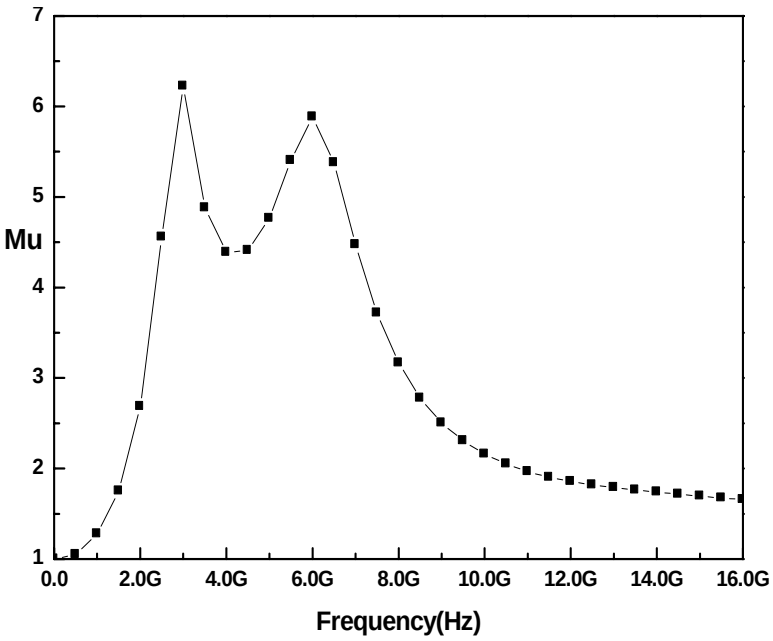
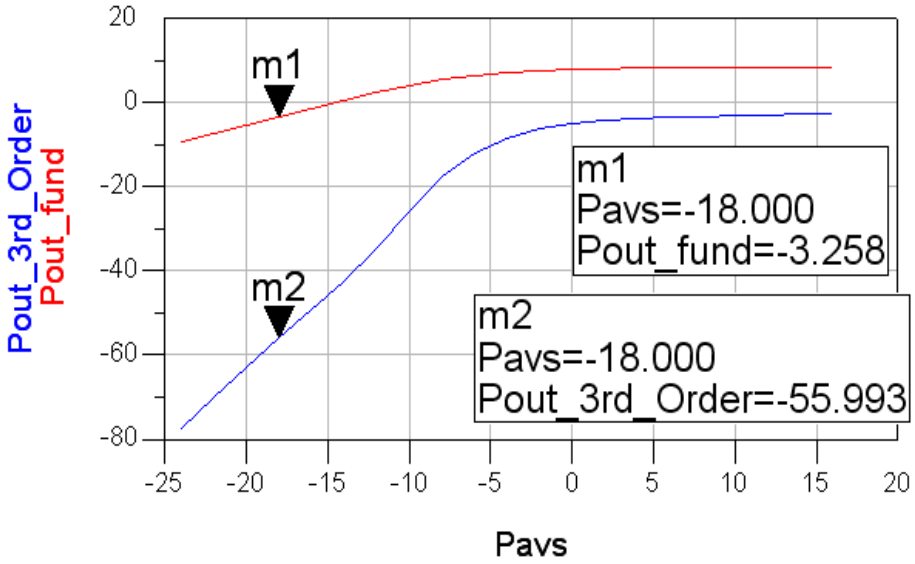


Figure 4-19: The stability index: Mu.



Pavs	TOI_output
-18.000	23.110

GainCompression	Pout_at_GainCompression
-1.117	8.532

Figure 4-20: The performance of PA in the aspect of linearity.

4.3.3 Layout of the Further Design

The layout is shown in Figure 4.21, the total size occupied by the PA is 1.073x0.927mm^2, The capacitor is used metal-insulator-metal (MIM) capacitance supported by TSMC, the models of the resistor and inductor are supplied by TSMC. The metal width is decided according to the capacity of current flow and AC signal power. Input and output pads use GSG with 50Ω.

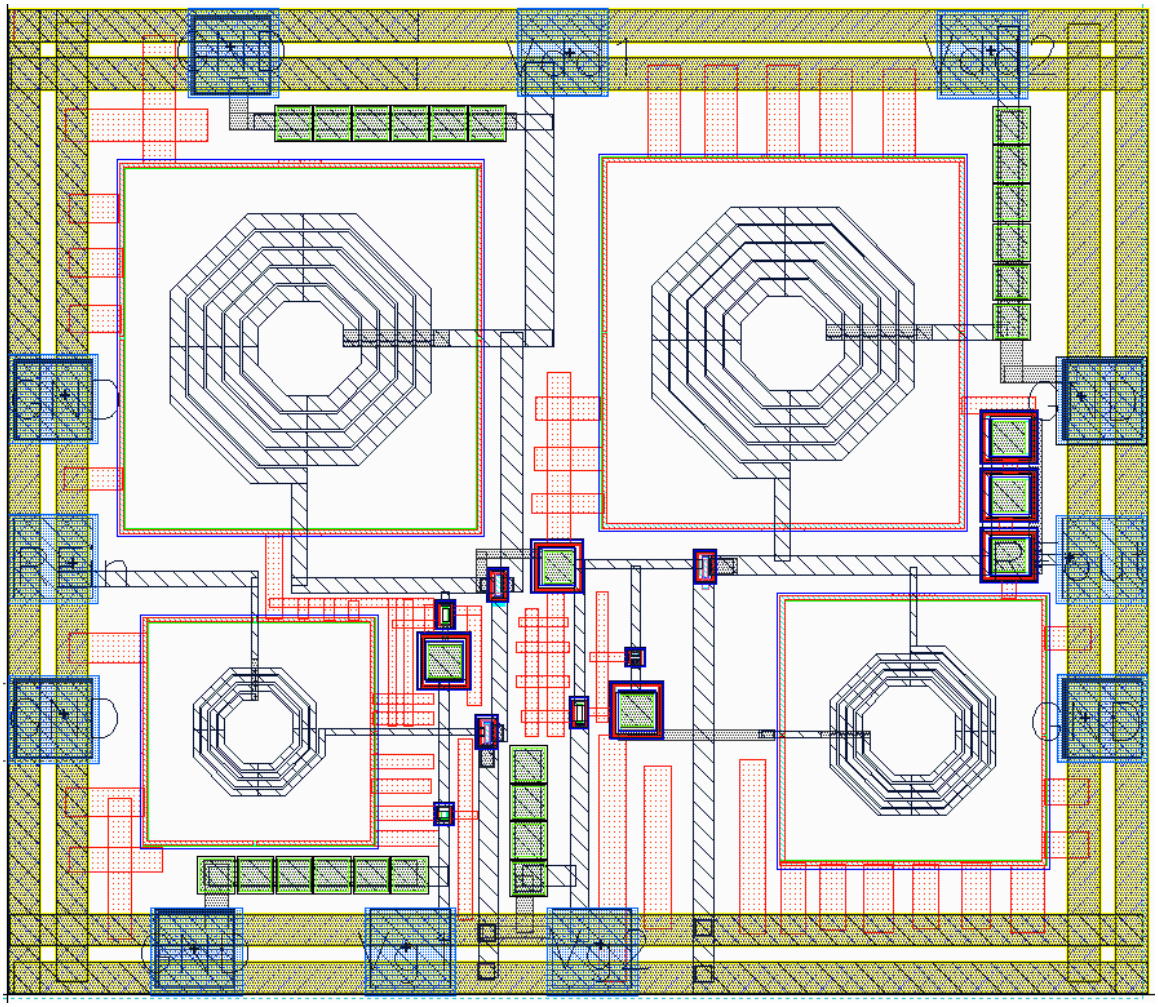


Figure 4-21: The layout of the PA.

Chapter5 Summary

Modern wireless standards need good power efficiency or wideband for applications. However, as CMOS technology is getting scaling down, breakdown voltage is also getting lower. This trend takes challenges to the CMOS power amplifier design. In this thesis, we have presented the two designs of RF CMOS power amplifier.

One is 3.1~10.6GHz two stages power amplifier for ultra wide-band applications, by using cascode configuration with feedback and the common source with feedback. According to the simulation result, the PA allows the maximum output power 16.7dBm, power gain 15.18dB, P_{1dB} as 4dBm, and total current consumption 38.9mA at DC supply 1.2V and 1.8V. Since cascode configuration with feedback can increase the power gain, provide the stable wideband matching, and flatten the power gain with the 2^{nd} stage. But the resistor-inductor feedback path does take some DC power loss; the limited and asymmetric output signal range does not succeed in suitable PAE.

Based on the previous design, we follow up studying to design a 3~8GHz power amplifier suitable for group A, group B, and group C of MB-OFDM. By using feedback configuration including inductor, resistor, and capacitor, we obtain better performance at efficiency and linearity: PAE_{max} is about 15.9%, P_{1dB} is 8.5dBm, and

OIP3 is 23.11dBm. Total power consumption is 70mW with the power supply 1.8V condition. The UWB power amplifier can be used for MB-OFDM. As the 130nm and 90nm CMOS technologies using in recent days, the gain will increase and should be able to cover the entire spectrum from 3.1 GHz to 10.6 GHz. The inductor-resistor feedback configuration provides a process to design a wideband matching network, with good performance of noise and gain flatness.

Reference

[01] P. Miliozzi, K. Kundert , K. Lampaert , P. Good, and M. chian, “A design system for RFIC: Challenges and solutions.” Proceedings of the IEEE, Oct.2000.

[02] B. Razavi, *RF Microelectronics*, 1st ed. NJ, USA: Prentice-Hall PTR, 1998.

[03] H. S. Momose, F. morifuji, T. Yoshittomi, T Ohguro, M. Saito, T. Morimoto, Y. Katsuma, H. Iwai, “High frequency AC characteristics of 1.5nm gate oxide MOSFET ” IEEE international Electron Device Meeting, December 1996.

[04] S. P. Voinigescu, S. W. Tarasewicz, T. MacElwee, and J. Ilowski, ”An assessment of the state-of-the-art 0.5um bulk CMOS technology for RF applications” proc. IEEE internationall Electron Devices Meeting, 1995.

[05] G. Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*, 2nd ed. NJ: Prentice-Hall, Inc. 1997.

[06] A. Rofougaran, G. Chang, J. Rael, et al. “A single –chip 900MHz spread spectrum wireless transceiver in 1mm CMOS-part I: architecture and transmitter design.” IEEE J. Solid State Circuits, vol. 33, pp.513-534, April 1998.

[07] J. Rudell, et al.,“A 1.9GHz wide band IF double conversion CMOS receiver for cordless telephone applications” IEEE J. Solid-state Circuits, vol.32, pp.2071-2088, Dec.1997.

[08] P. Orsatti, F. Piazza, Q. Huang, and T. Mosrimoto, “A 20 mA receive 55 mA

transmit GSM transceiver in 0.25-mm CMOS," in In Int. Solid-State Circuits Conf. Dig. Tech. Papers.(San Francisco), pp. 232-233,Feb. 1999.

[09] F. O. Eynde, J Schmit, V. Charher, et al. "A fully integrated single chip SOC for Buletooth," in In Int. Solid-State Circuits Conf. Dig. Tech. Papers, (San Francisco), pp. 196-197. Feb. 2001.

[10] C.Yoo and Q.Huang, "A common-gate switched 0.9W class E power with 41% PAE in 0.2μm CMOS" In 2000 Symposium on VLSI circuits, (Honolulu, HI), pp.56-57, June 2000.

[11] Chaudhury, P.; Mohr, W.; Onoe, S., "The 3GPP proposal for IMT-2000"; Communications Magazine, IEEE Volume 37, Issue 12, Dec. 1999

[12] Ryynanen, J.; Kivekas, K.; Jussila, J.; Parssinen, A.; Halonen, K.A.I.; "A dual-band RF front-end for WCDMA and GSM applications" Solid-State Circuits, IEEE Journal of Volume 36, Issue 8, Aug. 2001 Page(s):1198 – 1204

[13] A. Bevilacqua, and A. M. Niknejad, "An Ultrawideband CMOS Low-Noise Amplifier for 3.1-10.6-GH_Z Wireless Receivers," *IEEE J. Solid-State Circuits*, vol.39, no. 12. December 2004.

[14] C-W. Kim, M-S. Kang, P. T. Anh, H-T. Kim and S-G. Lee, "An Ultra-Wideband CMOS Low Noise Amplifier for 3-5-GH_Z UWB System," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, February, 2005.

[15] King-Chun Tsai; Gray, P.R.; “A 1.9-GHz, 1-W CMOS class-E power amplifier for wireless communications” Solid-State Circuits, IEEE Journal of Volume 34, Issue 7, July 1999 Page(s):962 - 970

[16] P. Asbeck and C. Fallesen, “A power amplifier for wireless applications in a digital CMOS process” in Proc. Of the 18th norchip Conference, pp.28-33, Nov.2000.

[17] Melly, T.; Porret, A.-S.; Enz, C.C.; Vittoz, E.; “A 1.2 V, 433 MHz, 10 dBm, 38% global efficiency FSK transmitter integrated in a standard digital CMOS process” Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000 21-24 May 2000 Page(s):179 - 182

[18] Kuo, T.C.; Lusignan, B.; “A 1.5 W class-F RF power amplifier in 0.2 μm CMOS technology” Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC.2001 IEEE International 5-7 Feb. 2001 Page(s):154 - 155, 442

[19] D. H. Morais and K. Feher, “The Effect of Filtering and Limiting on the Performance of QPSK, Offset QPSK, and MSK Signals” IEEE Trans. Communications, Vol.28, pp. 1999-2009, December 1980.

[20] J. F. Sevic and J. Staudinger, “Simulation of Adjacent Channel Power for Digital Wireless Communication Systems” microwave J., pp. 66-80, October 1996.

[21] M. Slovick. “Measuring ACPR in CDMA amplifiers” Microwave Journal. 1998;

pp: 74-80.

[22] N. Pothecary. “Feedforward linear power amplifiers” Artech House, Norwood, MA, 1999.

[23] K. Chang, Inder Bahl, and Vijay Nair; “RF and Microwave Circuit and Component Design for Wireless Systems” 2002.

[24] S.C. Cripps; “RF Power Amplifiers for Wireless Communications” Artech House, Norwood, MA, 1999.

[25] Sowlati, T.; Leenaerts, D.;”A 2.4GHz 0.18/spl mu/m CMOS self-biased cascode power amplifier with 23dBm output power” Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International

[26] Su, D.; Zargari, M.; Yue, P.; Rabii, S.; Weber, D.; Kaczynski, B.; Mebta, S.; Singh, K.; Mendis, S.; Wooley, B.; “A 5GHz CMOS transceiver for IEEE 802.11a wireless LAN” Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International

[27] B. McFarland, et al., “A 2.4 & 5 GHz dual band 802.11 WLAN supporting data rates to 108 Mb/s” in *IEEE Gallium Arsenide Integrated Circuit Symp. Dig.*, Oct. 2002, pp. 11-14

[28] Behzad, A.; Lin, L.; Shi, Z.M.; Anand, S.; Carter, K.; Kappes, M.; Lin, E.; Nguyen, T.; Yuan, D.; Wu, S.; Wong, Y.C.; Fong, V.; Rofougaran, A.;

“Direct-conversion CMOS transceiver with automatic frequency control for 802.11a wireless LANs” Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International

[29] Yun Seong Eo, KwangDu Lee.; “A fully integrated 24-dBm CMOS power amplifier for 802.11a WLAN applications” Microwave and Wireless Components Letters, IEEE.

[30] Aiello, G.R. “Challenges for ultra-wideband (UWB) CMOS integration” Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE

[31] www.ieee802.org/15/pub/TG3a.html

[32] Matt Wellborn. “Xtreme Spectrum CFP Presentation” May, 2003. http://grouper.ieee.org/groups/802/15/pub/2003/May03/03153r4P802-15_TG3a-XtremeSpectrum-CFP-Presentation.pdf.

[33] Ketan Mandke, Haewoon Nam,Lasya Yerramneni, and Christian Zuniga,” The Evolution of UWB and IEEE 802.15.3a forVery High Data Rate WPAN” EE 381K-11 Wireless CommunicationsUWB Group, The University of Texas at AustinPrepared for Dr. T. S. Rappaport May 6, 2003.