國 立 交 通 大 學

電子工程學系　電子研究所

碩 士 論 文

應用於超寬頻3.1-10.6 GHz低雜訊放大器之設計

Design of an UWB CMOS LNA for 3.1 to 10.6 GHz with RL-feedback

研究生: 王鴻瑋

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摘要

本論文研製一個應用於超寬頻 3.1-10.6 GHz 的低雜訊放大器是採用電阻-電感回授做輸入匹配，而在輸出端是用 current buffer做匹配。本研究是以 0.18 微米互補式金氧半製程實現。此低雜訊放大器是以三級放大為主架構，第一級為 RL-feedback 結構，是為了增加頻寬，第二級為傳統的 CS 結構，可以增加平均順向增益(S_{21})，第三級則是 current buffer，主要是在輸出端做匹配。為了能在所應用的頻段內達到相對的平坦增益，在前兩級中利用 shunt peaking 的方法去實現。供應電壓 V_{DD} 為 1.8 伏特時，整個電路功率消耗約為 23.04mW，及包含 pad 的情況下整個電路大小約為 0.776 mm^2。本研究的低雜訊放大器所量測的規格，平均順向增益(S_{21})在 3.1-10.6GHz 時為 6.9dB-4.5dB，逆向隔離(S_{12})為 -33dB 以下，S11 為-10dB 以下，S22 約為-16dB 以下，而平均雜訊指數約為 6dB。

Design of an UWB CMOS LNA for 3.1 to 10.6 GHz with RL-feedback

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Abstract

A 3.1-10.6 GH_Z low noise amplifier is applied for ultra-wideband, it introduces RL feedback for input matching. And current buffer is used for output matching. This research is fabricated in 0.18-μm CMOS process. Three amplified stages are formed for main topology in low noise amplifier. The first stage introduces RL-feedback configuration, it can improve the bandwidth. The second stage introduces traditional CS configuration, it can improve the average forward S_{21}. The third stage introduces current buffer configuration, it is used for output matching. Relatively flat gain is essential over the entire desired band. The low noise amplifier introduces the shunt peaking to achieve the above purpose. The total power dissipation of the chip is about 29 mW at power supply 1.8 volt. The chip size included pad is 0.776 mm^2. The measurement result of this study expect that the average forward S_{21} is 6.9dB at 3.1-10.6GHz, the reverse isolation S_{12} is under -33dB, the magnitude of S_{11} is under -10 dB, the magnitude of S_{22} is under -16dB, and the noise figure is 6dB.

誌謝

本論文得以完成，首先要感謝我的指導老師　荊鳳德 教授，在兩年的碩士研究生涯裡，給予我豐富的指導與照顧，不論是研究上與生活裡都讓我在這兩年裡獲得許多的收穫。

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Chapter 1

Introduction

1.1 UWB CMOS Receivers

UWB (Ultra Wideband) is a ring in the wireless communication field. Main application 10 about short distance high-speed communication, and more than 100 metres, even 1 kilometer one communicate at a low speed remotely. If compare UWB and 802.11a, pure according to view on technology, the high transfer rate of UWB and power of low consumption are superior to 802.11a . UWB can allow to convey the materials of 500 Mega Bits per second in (about five metres) range of 15 feet , in other words, UWB is the specification of conveying a large number of materials in the short distance, another advantage of UWB is that the power consumption is very low. The FCC has allocated 7.5 GH_Z of spectrum for unlicensed use of UWB devices in the 3.1 to 10.6 GH_Z frequency band. The low noise amplifier needs to amplify the received UWB signal with sufficient gain and as little as possible.

The majority implementation of the RF integrated circuit used for wireless devices are encounter with various possibilities: CMOS, Bi CMOS, and GaAs MESFET, bipolar (BJT), hetero-junction bipolar transistor (HBT), and PHEMT, etc,. We just focus on the CMOS technology, CMOS process reduce the minimum channel length from the present years, so the unity gain cut off frequency (f_t) is increasing.

For example, a deep sub-micron prototype CMOS technology has realized devices with f_t exceeding 100 GHz [1] and minimum noise figures less than 0.5-dB at 2 GHz. The more commercially available sub-micron CMOS technologies have display f_t's of 20GHz and minimum noise figures of 1.6-dB at 2Ghz [2]. The VLSI capabilities of CMOS make it proper to very high levels of mixed signal radio integration while increasing the functionality of a single chip radio to cover multiple RF standards [3]. Due to the advancement of circuit design technology, circuit size is small and cost down consideration. With the work at [4] [5] [6], low cost and low power devices of RF front-end system implemented by CMOS technology, the prospect of a single chip CMOS system has received considerable interest. Even the SOC is difficult and hard to implement at this time, but a set of separate chips in the same CMOS technology may bring significant economic benefits [7].

1.2 motivation

For portable wireless communication devices has given great push to the development of a next generation of low power radio frequency integrated circuits (RFIC) product. Such as wireless phones, cordless and cellular, global positioning satellite (GPS), pagers, wireless modems, wireless local area network (LAN), and RF ID tags, etc., require more low cost; low noise and high power efficiency solutions to supply the demand for low-price product [8].

Chapter 2 discusses the basic concepts in RF design. Chapter 3 presents the basic low-noise amplifiers design for UWB. Chapter 4 deals with wideband matching network by using inductor-resistor feedback, presents the UWB proposals, design, implementation of a low-noise amplifier. Chapter 5 concludes this research effort with some future directions.

Chapter 2

Issues in RFIC Design

2.1 Noise Analysis

2.1.1 The Concept of Noise Figure

Noise is usually generated by the random motions of charges or charge carriers in devices and materials. Because the noise process is random, one cannot identify a specific value of voltage at a particular time, and the only recourse is to characterize the noise with statistical measures, such as the mean-square or root-mean-square values. Because of having various noise sources in the circuit, we need to simplify calculation of the total noise at the output [9]. Obviously, the output-referred noise does not allow a fair comparison of the performance of different circuits because it depends on the gain. According the circuit theory, we can use the input-referred noise of circuits to represent the noise of behavior in the circuits.

The signal-to-noise ratio (SNR), defined as the ratio of the signal power to the total noise power, is an important parameter. In RF circuit, most of the front-end receiver blocks are characterized in terms of their "noise figure" rather than the input-referred noise. Noise figure has many different definitions. The most commonly accepted definition is

$$\text{noise figure} = \frac{SNR_{in}}{SNR_{out}}, \tag{2.1}$$

Noise figure is a measure of how much the SNR degrades as the signal passes through a circuit. If a circuit has no noise source, the SNR_{out}=SNR_{in}, regardless of the gain.

Noise added by electronics will be directly added to the noise from the input. Thus, for reliable detection, the previously calculated minimum detectable signal level must be modified to include the noise from the active circuitry. Noise from the electronics is described by noise factor F, which is a measure of how much the signal-to-noise ratio is degraded through the system. We note that

$$S_o = G \cdot S_i \tag{2.2}$$

where S_i is the input signal power, S_o is the output signal power, and G is the power gain S_o/S_i. We derive the following equation for the noise factor:

$$F = \frac{SNR_i}{SNR_o} = \frac{S_i/N_{i(source)}}{S_o/N_{o(total)}} = \frac{S_i/N_{i(source)}}{(S_i \cdot G)/N_{o(total)}} = \frac{N_{0(total)}}{G \cdot N_{i(source)}} \tag{2.3}$$

where $N_{o(total)}$ is the total noise at the output. If $N_{o(source)}$ is the noise at the output originating at the source, and $N_{o(added)}$ is the noise at the output added by electronic circuitry, then we can write:

$$N_{o(total)} = N_{o(source)} + N_{o(added)} \tag{2.4}$$

Noise factor can be written in several useful alternative forms:

$$F = \frac{N_{o(total)}}{G \cdot N_{i(source)}} = \frac{N_{o(total)}}{N_{o(source)}} = \frac{N_{o(source)} + N_{o(added)}}{N_{o(source)}} = 1 + \frac{N_{o(added)}}{N_{o(source)}} \tag{2.5}$$

This shows that the minimum possible noise factor, which occurs if the electronics add no noise, is equal to 1. Noise figure NF is related to noise factor *F* by

$$NF = 10 \log_{10} F \tag{2.6}$$

Thus, while noise factor is at least 1, noise figure is at least 0 dB. In other words, an electronic system that adds no noise has a noise figure of 0 dB.

In the receiver chain, for components with loss (such as switches and filters), the noise figure is equal to attenuation of the signal. For example, a filter with 3 dB of loss has a noise figure of 3 dB. This is explained by noting that output noise is approximately equal to input noise, but signal is attenuated by 3 dB. Thus, there has degradation of SNR by 3 dB. [10]

2.1.2 The Noise Figure of an Amplifier Circuit

Now, we can make use of the definition of noise figure just developed and apply it to an amplifier circuit. For the purposes of developing (2.5) into a more useful form, it is assumed that all practical amplifiers can be characterized by an input-referred noise model, such as shown in Figure 2-1, where the amplifier is characterized with current gain A_i. In this model, all noise sources in the circuit are lumped into series noise voltage source v_n and a parallel current noise source i_n placed in front of a noiseless transfer function.

If the amplifier has finite input impedance, then the input current will be split by

some ratio α between the amplifier and the source admittance Y_s:

$$SNR_{in} = \frac{\alpha^2 i_{in}^2}{\alpha^2 i_{ns}^2} \tag{2.7}$$

Assuming that the input-referred noise sources are correlated, the output signal-to-ratio is

$$SNR_{out} = \frac{\alpha^2 A_i^2 i_{in}^2}{\alpha^2 A_i^2 (i_{ns}^2 + |i_n + v_n Y_s|^2)} \tag{2.8}$$

Thus, the noise factor can now be written in terms of the preceding two equations:

$$F = \frac{i_{ns}^2 + |i_n + v_n Y_s|^2}{i_{ns}^2} = \frac{N_{o(total)}}{N_{o(source)}} \tag{2.9}$$

This can also be interpreted as the ratio of the total output noise to the total output noise due to the source admittance.

In (2.8), it was assumed that the two input noise source were correlated with each other. In general, they will not be correlated with each other, but rather the current i_n will be partially correlated with v_n and partially uncorrelated. We can expand both current and voltage into these two explicit parts:

$$i_n = i_c + i_u \tag{2.10}$$

$$v_n = v_c + v_u \tag{2.11}$$

In addition, the correlated components will be related by the ratio

$$i_c = Y_c v_c \tag{2.12}$$

where Y_c is the correlation admittance.

The noise figure can now be written as

$$NF = 1 + \frac{i_u^2 + \left|Y_c + Y_s\right|^2 v_c^2 + v_u^2 \left|Y_s\right|^2}{i_{ns}^2} \tag{2.13}$$

The noise current and voltages can also be written in terms of equivalent resistance and admittance:

$$R_c = \frac{v_c^2}{4kT\Delta f} \tag{2.14}$$

$$R_u = \frac{v_u^2}{4kT\Delta f} \tag{2.15}$$

$$G_u = \frac{i_u^2}{4kT\Delta f} \tag{2.16}$$

$$G_s = \frac{i_{ns}^2}{4kT\Delta f} \tag{2.17}$$

Thus, the noise figure is now written in terms of these parameters:

$$NF = 1 + \frac{G_u + \left|Y_c + Y_s\right|^2 R_c + \left|Y_s\right|^2 R_u}{G_s} \tag{2.18}$$

$$NF = 1 + \frac{G_u + \left[(G_c + G_s)^2 + (B_c + B_s)^2\right] R_c + \left(G_s^2 + B_s^2\right) R_u}{G_s} \tag{2.19}$$

It can be seen from this equation that NF is dependent on the equivalent source impedance. [10]

For a cascade of stages, the overall noise figure can be obtained in terms of the NF and gain of each stage. For m-stages, the NF_{tot} is equal to

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \cdots A_{p(m-1)}} \tag{2.20}$$

where A_{pm} is the available power gain of the m-th stage. This is called the Friis equation. The Friis equation indicates that the noise contributed by each stage decreases as the gain preceding the stage increases, implying that the first few stages in a cascade are the most critical [11].

2.2 Linearity in RF Circuits

Mathematically, any nonlinear transfer function can be written as series expansion of power terms unless the system contains memory. While many RF circuits can be approximated with a linear model to obtain their response to small signals, nonlinearities often lead to interesting and important phenomena. For

simplicity, we assume that:

$$v_{out} = k_0 + k_1 v_{in} + k_2 v_{in}^2 + k_3 v_{in}^3 + \ldots \tag{2.21}$$

One common way of characterizing the linearity of a circuits is called the two-tone test. In this test, an input consisting of two sine waves is applied to the circuit.

$$v_{in} = v_1 \cos \omega_1 t + v_2 \cos \omega_2 t = X_1 + X_2 \tag{2.22}$$

When this tone is applied to the transfer function given in (2.21), the result is a number of terms:

$$v_0 = k_0 + \underbrace{k_1 (X_1 + X_2)}_{desired} + \underbrace{k_2 (X_1 + X_2)^2}_{\text{sec } ond \ \ order} + \underbrace{k_3 (X_1 + X_3)^3}_{third \ \ order} \tag{2.23}$$

$$\begin{aligned} v_0 = & k_0 + k_1 (X_1 + X_2) + k_2 (X_1^2 + 2X_1 X_2 + X_2^2) \\ & + k_3 (X_1^3 + 3X_1^2 X_2 + 3X_1 X_2^2 + X_1^2) \end{aligned} \tag{2.24}$$

These terms can be further broken down into various frequency components. For instance, the X_1^2 term has a zero frequency (dc) component and another at the second harmonic of the input:

$$X_1^2 = (v_1 \cos \omega_1 t)^2 = \frac{v_1^2}{2}(1 + \cos 2\omega_1 t) \tag{2.25}$$

The second-order terms can be expands as follows:

$$(X_1 + X_2)^2 = \underbrace{X_1^2}_{dc+HD2} + \underbrace{2X_1 X_2}_{IM2} + \underbrace{X_2^2}_{dc+HD2} \tag{2.26}$$

where second-order terms are composed of second harmonics HD2, and mixing

components, here labeled IM2 for second-order intermodulation. The mixing components will appear at the sum and difference frequencies of the two input signals. Note also that second-order terms cause an additional dc term to appear.

The third-order terms can be expanded as follows:

$$(X_1 + X_2)^3 = \underbrace{X_1^3}_{FUND\ +HD\ 3} + \underbrace{3X_1^2X_2}_{IM\ 3+FUND} + \underbrace{3X_1X_2^2}_{IM\ 3+FUND} + \underbrace{X_2^3}_{FUND\ +HD\ 3} \tag{2.27}$$

Third-order nonlinearity results in third harmonics HD3 and third-order intermodulation IM3. Expansion of both the HD3 and IM3 terms shows output signals appearing at the input frequencies. The effect is that third-order nonlinearity can change the gain, which is seen as gain compression. This is summarized in Table 2.1.

Note that in the case of an amplifier, only the terms at the input frequency are desired. Of all the unwanted terms, the last two at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are the most troublesome, since they can fall in the band of desired output if ω_1 is close in frequency to ω_2 and therefore cannot be easily filtered out. These two tone are usually referred to as third-order intermodulation terms (IM3 products)

2.2.1 Third-Order Intercept point and The 1-dB Compression Point

One of the most common ways to test the linearity of a circuit is to apply two signals at the input, having equal amplitude and offset by some frequency, and plot fundamental output and intermodulation output power as function of input power as

show in Figure 2-2. From the plot, the *third-order intercept point* (IP3) is determined. The third-order intercept point is a theoretical point where the amplitudes of the fundamental tones at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are equal to the amplitudes of the fundamental tones at ω_1 and ω_2.

From Table 2.1, if $v_1 = v_2 = v_i$, then the fundamental is given by

$$\text{fund} = k_1 v_i + \frac{9}{4} k_3 v_i^3 \tag{2.28}$$

The linear component of (2.28) given by

$$\text{fund} = k_1 v_i \tag{2.29}$$

can be compared to the third-order intermodulation term given by

$$\text{IM3} = \frac{3}{4} k_3 v_i^3 \tag{2.30}$$

The small v_i, the fundamental rise linearity (20dB/decade) and that the IM3 terms rise as the cube of the input (60dB/decade). A theoretical voltage at which these two tones will be equal can be defined:

$$\frac{\frac{3}{4} k_3 v_{IP3}^3}{k_1 v_{IP3}} = 1 \tag{2.31}$$

This can be solved for v_{IP3} :

$$v_{IP3} = 2\sqrt{\frac{k_1}{3k_3}} \tag{2.32}$$

That (2.32) gives the input voltage at the third-order intercept point. The input power at this point is called the *input third-order intercept point* (IIP3). If IP3 is specified at the output, it is called the *output third-order intercept point* (OIP3).

The third-order intercept point cannot actually be measured directly, since by the time the amplifier reached this point, it would be heavily overloaded. Therefore, it is useful to describe a quick way to extrapolate it at a given power level. Assume that a device with power gain *G* has been measured to have an output power of P_1 at the fundamental frequency and a power of P_3 at the IM3 frequency for a given input power of P_i, as illustrated in Figure 2-2. On a log plot of P_3 and P_1 versus P_i, the IM3 terms have a slope of 3 and the fundamental terms have a slope of 1. Therefore,

$$\frac{OIP\,3 - P_1}{IIP\,3 - P_i} = 1 \tag{2.33}$$

$$\frac{OIP\,3 - P_3}{IIP\,3 - P_i} = 3 \tag{2.34}$$

since subtracation on a log scale amounts to division of power.

Also note that

$$G = OIP3 - IIp3 = P_1 - P_i \tag{2.35}$$

These equations can be solved to given

$$IIP3 = P_1 + \frac{1}{2}[P_1 - P_3] - G = P_i + \frac{1}{2}[P_1 - P_3] \tag{2.36}$$

In addition to measuring the IP3 of a circuit, the 1-dB compression point is another common way to measure linearity. This point is more directly measurable than IP3 and requires only one tone rather than two. The 1-dB compression point is simply the power level, specified at either the input or the output, where the output power is 1dB less than it would have been in an ideally linear device. It is also marked in Figure 2-2. [10]

2.2.2 Cascaded Nonlinear Stages

Since in RF systems, signals are processed by cascaded stages, it is important to know how the nonlinearity of each stage is referred to the input of the cascade. Consider two nonlinear stages in cascade. As shown in Figure2-3. Assuming that the input-output relationship is

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.37}$$

$$y_2(t) = \beta_1 y_1(t) + \beta_2 y_1^{\,2}(t) + \beta_3 y_1^{\,3}(t) \tag{2.38}$$

Substitute (2.37) into (2.38) results in the relation

$$y_2(t) = \alpha_1\beta_1 x(t) + (\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3)x^3(t) \tag{2.39}$$

If we consider only the first- and third-order terms, then

$$A_{IP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1\beta_1}{\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + \alpha_1^3\beta_3}\right|}. \tag{2.40}$$

From equation (2.40) can be simplified if the two sides are inverted and squared:

$$\frac{1}{A^2_{IP3}} = \frac{1}{A^2_{IP3,1}} + \frac{3\alpha_2\beta_2}{2\beta_1} + \frac{\alpha_1^2}{A^2_{IP3,2}}, \tag{2.41}$$

where $A_{IP3,1}$ and $A_{IP3,2}$ represent the input IP_3 points of the first and second stages, respectively. From the above result, we note that as α_1 increases, the overall IP_3 decreases. This is because with higher gain in the first stage, the second stage senses larger input levels, thereby producing much greater IM_3 products [11].

Table 2.1

Frequency	Component Amplitude
dc	$k_0 + \frac{k_2}{2}\left(v_1^2 + v_2^2\right)$
ω_1	$k_1 v_1 + k_3 v_1\left(\frac{3}{4}v_1^2 + \frac{3}{2}v_2^2\right)$
ω_2	$k_1 v_2 + k_3 v_2\left(\frac{3}{4}v_2^2 + \frac{3}{2}v_1^2\right)$
$2\omega_1$	$\frac{k_2 v_1^2}{2}$
$2\omega_2$	$\frac{k_2 v_2^2}{2}$
$\omega_1 \pm \omega_2$	$k_2 v_1 v_2$
$\omega_2 \pm \omega_1$	$k_2 v_1 v_2$
$3\omega_1$	$\frac{k_3 v_1^3}{4}$
$3\omega_2$	$\frac{k_3 v_2^3}{4}$
$2\omega_1 \pm \omega_2$	$\frac{3}{4}k_3 v_1^2 v_2$
$2\omega_2 \pm \omega_1$	$\frac{3}{4}k_3 v_1 v_2^2$

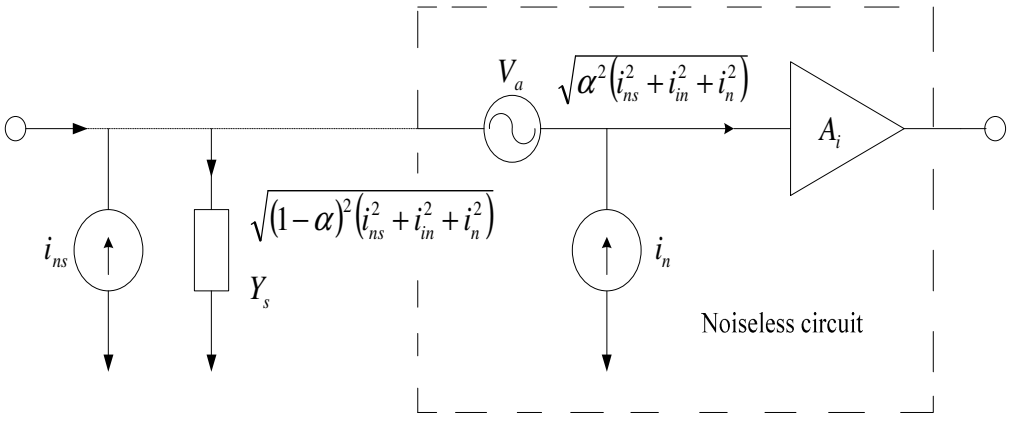

Figure 2-1 Input-referred noise model for device.

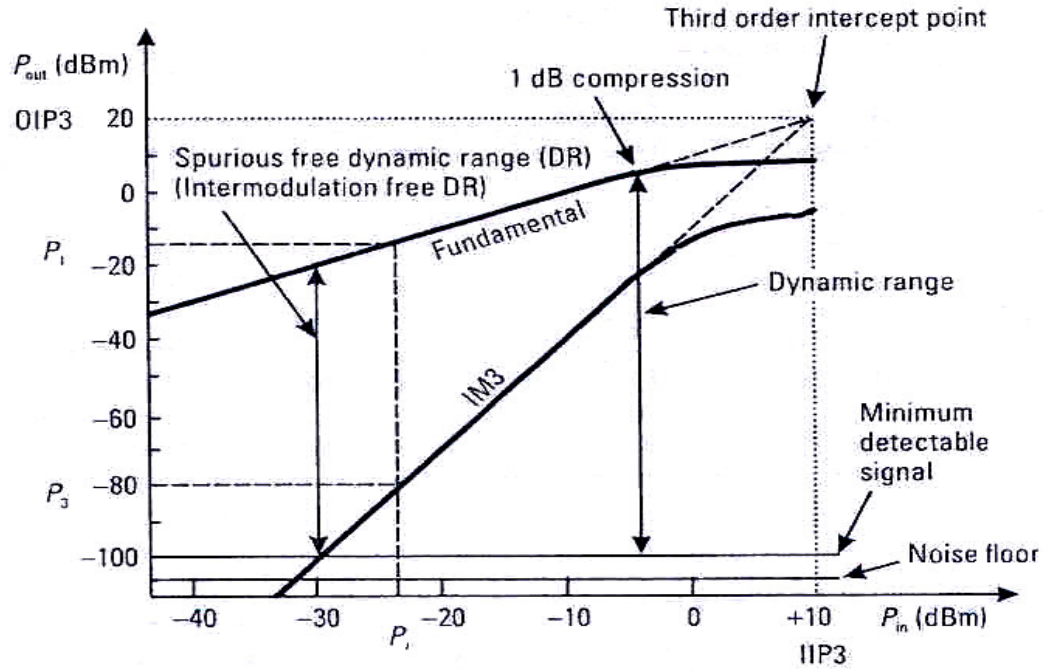

Figure 2-2 Plot of input output power of fundamental and IM3 versus input power.

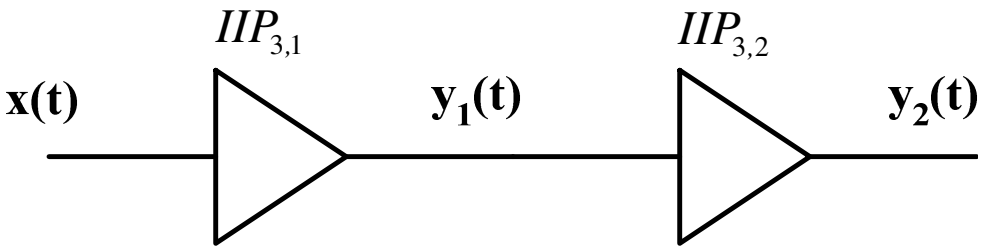

Figure 2-3 Cascaded nonlinear stages.

Chapter 3

Basic LNA Design

3.1 Consideration in Low-Noise Amplifiers

3.1.1 Impedance Matching

Consider the RF system shown in Figure 3-1. Here the source and load are 50Ω (a very popular impedance), as are the transmission lines leading up to the IC. For optimum power transfer, prevention of ringing and radiation, and good noise behavior, for example, we needs the circuit input and output impedances matched to the system. In general, some matching circuit must almost always be added to the circuit, as shown in Figure 3-2.

Typically, reactive matching circuits are used because they are lossless and because they do not add noise to the circuit will only be matched over a range of frequencies and not at others. If a broadband matching is required, then other techniques may need to be used. An example of matching a transistor amplifier with a capacitive input is shown in Figure 3-3. The series inductance adds an impedance of $j\omega L$ to cancel the input capacitive impedance. Note that, in general, when an impedance is complex $(R + jX)$. Then to match it, the impedance must be driven from its complex conjugate $(R - jX)$.

A more general matching is required if the real part is not 50Ω. For example, if

the real part of Z_{in} is less than 50Ω, then the circuit can be matching using the circuit in Figure 3-4.

The input impedance of a circuit can be any values. In order to have the best power transfer into the circuit, it is necessary to match this impedance to the impedance of the source driving the circuit. The output impedance must be similarly matched. It is very common to use reactive components to achieve this impedance transformation, because they do not absorb any power or add noise. Thus, series or parallel inductance or capacitance can be added to the circuit to provide an impedance transformation. Series components will move the impedance along a constant resistance circle on the Smith Chart. Parallel components will move the admittance along a constant conductance circle. Table 3.1 summarizes the effect of each component.

With the proper choice of two reactive components, any impedance can be moved to a desired point on the Smith Chart. There are eight possible two-components matching networks, also known as *ell* networks, as shown in Figure 3-5. Each will have a region in which a match is possible and a region in which a match is not possible.

In any particular region on the Smith Chart, several matching circuits will work and others will not. This is illustrated in Figure 3-6, which shows what matching

networks will work in which regions. Since more than one matching network will work in any region, how does one choose? There are a number of popular reasons for choosing one over another.

1. Sometimes matching component can be used as dc blocks (capacitors) or to provide bias currents (inductors).
2. Some circuits may result in more reasonable component values.
3. Personal preference. Not to be underestimated, sometimes when all paths look equal, you just have to shoot from the hip and pick one.
4. Stability. Since transistor gain is higher at lower frequencies, there may be a low-frequency stability problem. In such a case, sometimes a high-pass network (series capacitor, parallel inductor) at the input may be more stable.
5. Harmonic filtering can be done with a lowpass matching network (series *L*, parallel *C*). This may be important, for example, for power amplifiers. [10]

Table 3.1

Component Added	Effect	Description of Effect
Series inductor	$z \rightarrow z + j\omega L$	Move clockwise along a resistance circle
Series capacitor	$z \rightarrow z - j/\omega C$	Smaller capacitance increases impedance $(-j/\omega C)$ to move counterclockwise along a conductance circle
Parallel inductor	$y \rightarrow y - j/\omega L$	Smaller inductance increases admittance $(-j/\omega L)$ to move counterclockwise along a conductance circle
Parallel capacitor	$y \rightarrow y + j\omega C$	Move clockwise along a conductance circle

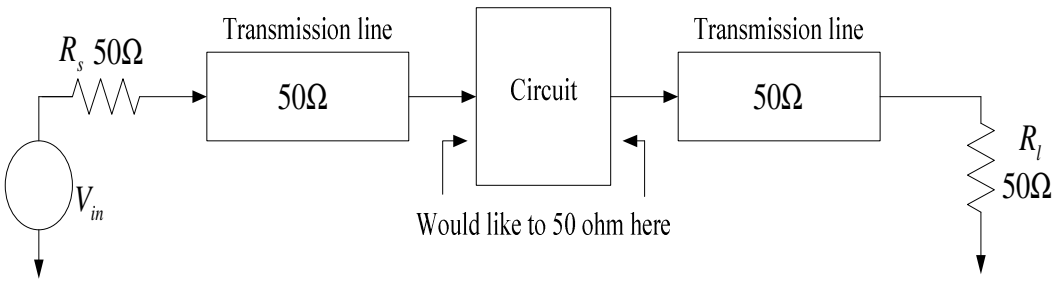

Figure 3-1 Circuit embedded in a 50-Ω system .

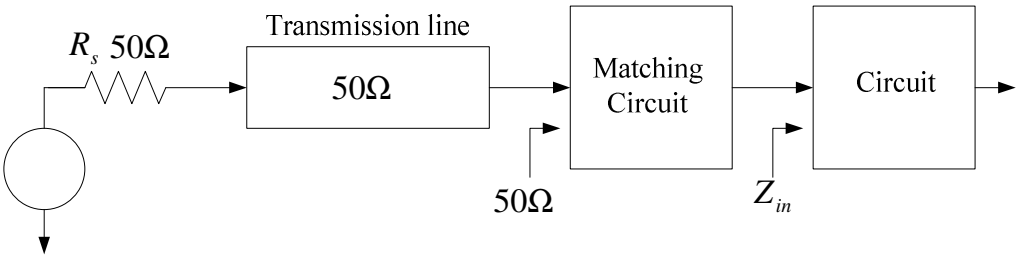

Figure 3-2 Circuit embedded in a 50-Ω system with matching circuit .

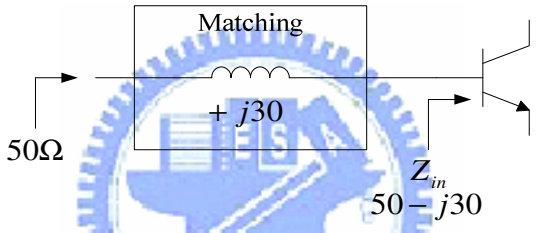

Figure 3-3 Example of a very sample matching network.

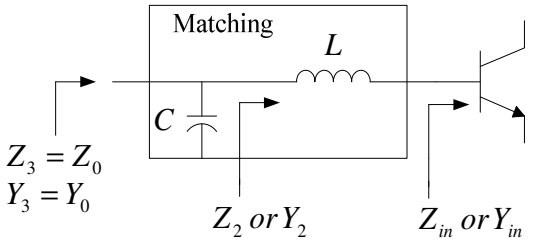

Figure 3-4 A possible impedance-matching network.

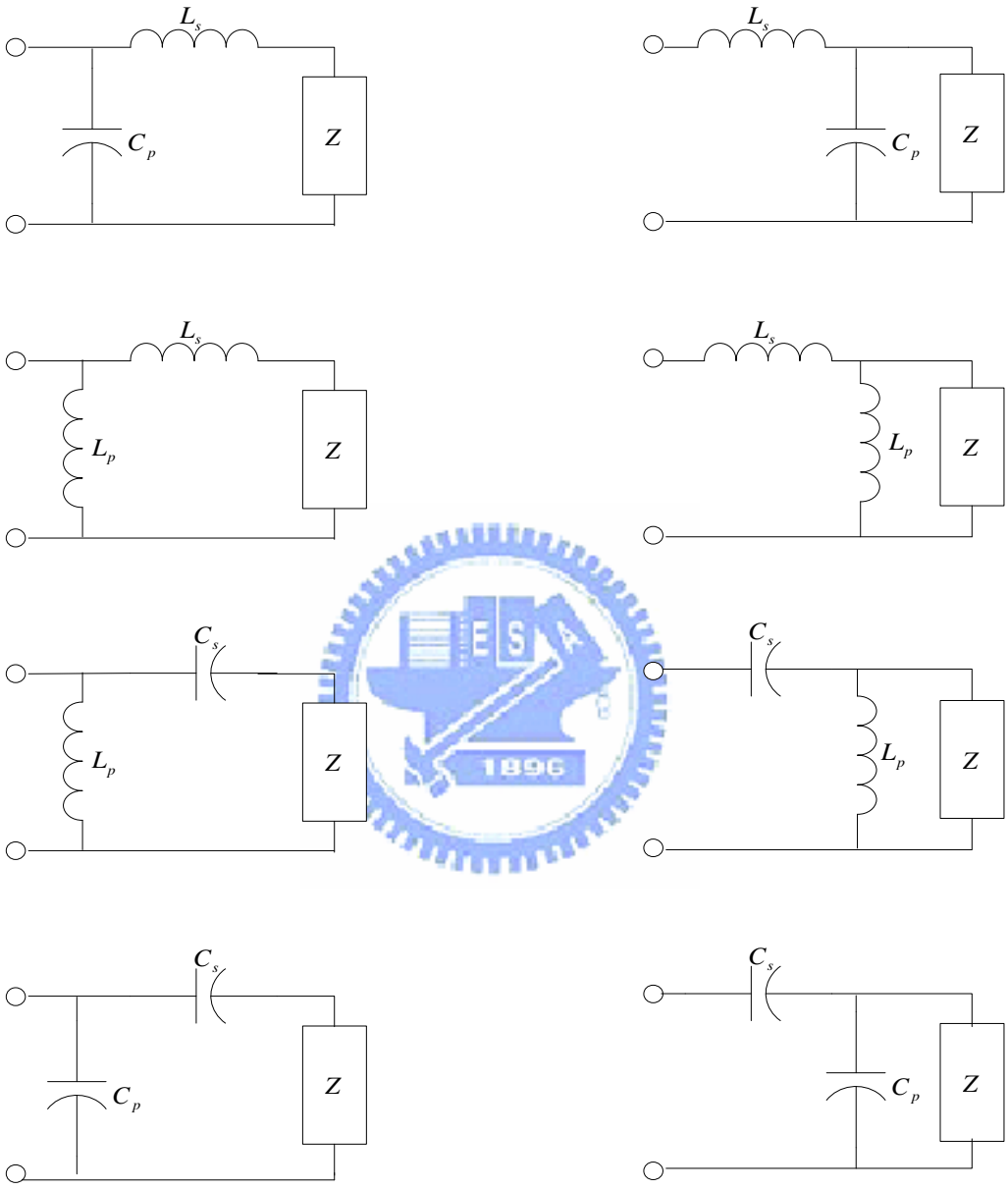

Figure 3-5 The eight possible impedance-matching networks with two reactive components.

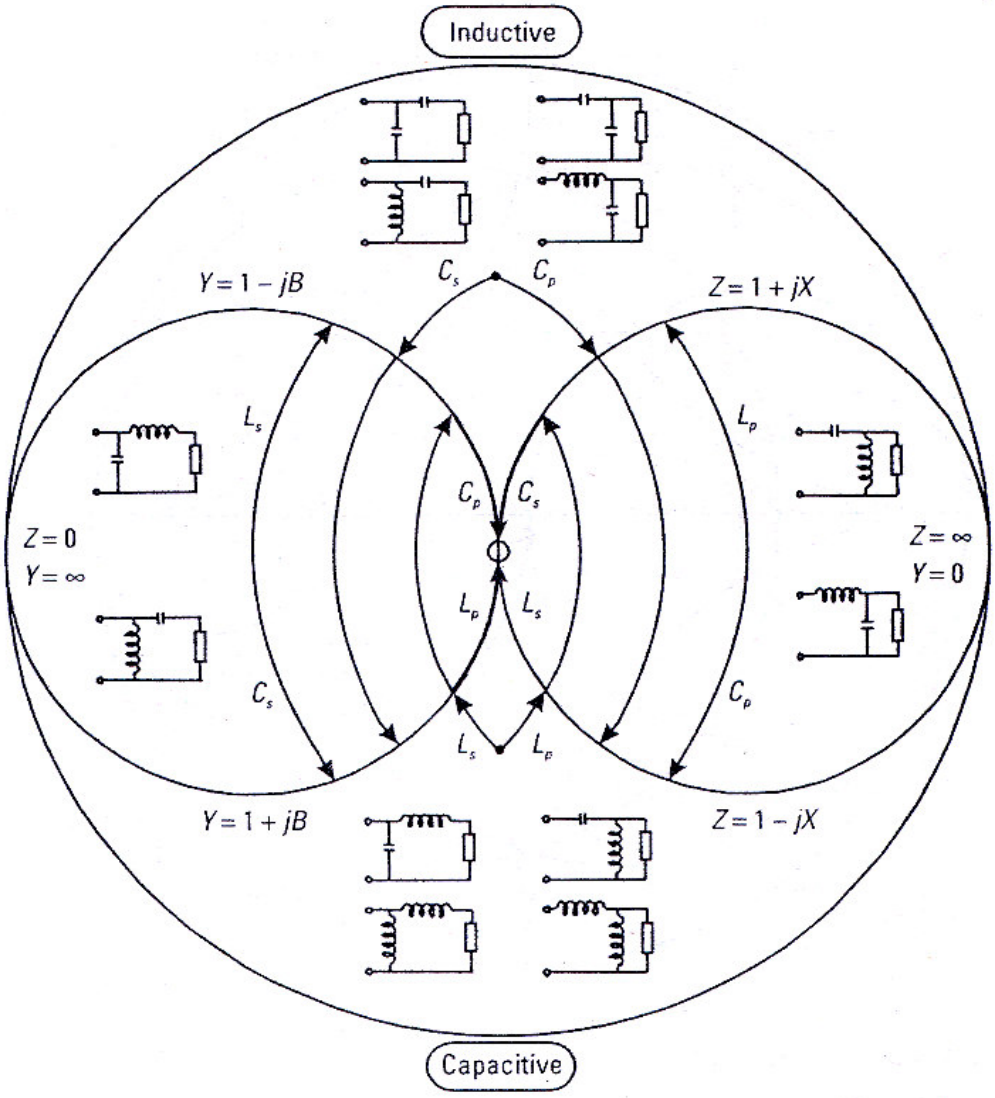

Figure 3-6 Which ell matching networks will work in which regions.

3.1.2 Stability

The stability of an amplifier is a very important consideration in a design and can be determined from the S parameters, the matching networks, and the terminations. A two-port network to be unconditionally stable can be derived from (3.1) to (3.4).

$$\left|\Gamma_s\right| < 1 \tag{3.1}$$

$$\left|\Gamma_L\right| < 1 \tag{3.2}$$

$$\left|\Gamma_{IN}\right| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| < 1 \tag{3.3}$$

$$\left|\Gamma_{OUT}\right| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_S}\right| < 1 \tag{3.4}$$

The two-port network is shown in Figure 3-7. For unconditional stability any passive load or source in the network must produce a stable condition. The solution of (3.1) to (3.4) gives the required conditions for the two-port network to be unconditionally stable. [12]

$$k = \frac{1 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2 + \left|\Delta\right|^2}{2\left|S_{12}S_{21}\right|} \tag{3.5}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.6}$$

A convenient way of expressing the necessary and sufficient conditions for unconditional stability is

$$k > 1 \tag{3.7}$$

$$|\Delta| < 1 \tag{3.8}$$

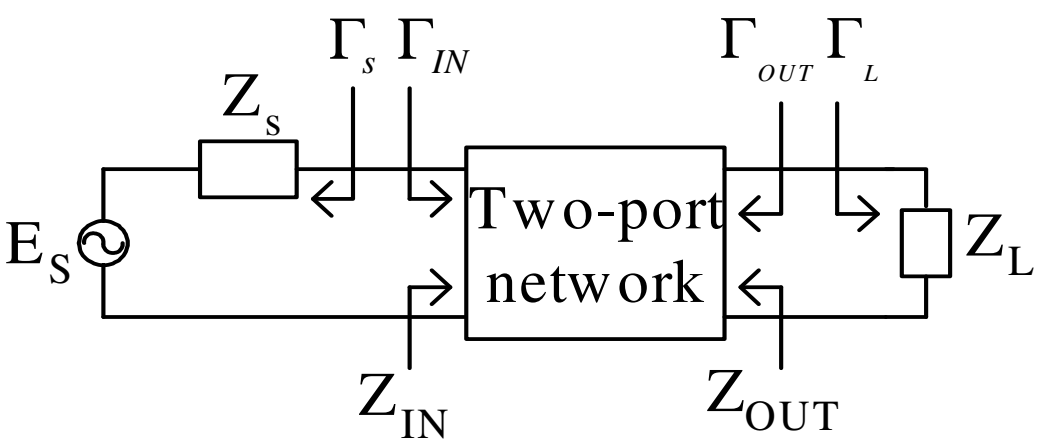

Figure 3-7 Stability of two-port networks.

3.2 Wide-band LNA design

Figure 3-8 is the LNA circuit schematic. We discuss this circuit step by step from the first stage. First, to make $1/g_m = 50\Omega$, the g_m value of common gate amplifier is going to be fixed at certain trans-conductance. An additional stage is required to provide sufficient gain over the desired band. A shunt feedback common source amplifier is used in the second stage for this purpose. The first step is the selection of transistor size and bias condition of the M1 to yield $\mathrm{Re}|Z_{11}| = 1/g_m = 50\Omega$. This ensures input matching condition for wide-band of frequency. But this condition is violated with optimum noise condition. There is a trade-off between noise and impedance matching in the LNA circuit. One of the major problems in the wide bandwidth amplifier design is the limitation imposed by the gain-bandwidth product of the active device. We know that any active device has a gain roll off at high frequency because of the gate-drain and gate-source capacitance in the transistor. This effect degrades the forward gain as the frequency increases and eventually the transistor stops functioning as an amplifier at the high frequency. Therefore the second design step is the selection of optimal bias point of second stage of LNA so that it operates at its maximum f_T. In addition to this $|S_{21}|$ degradation with frequency other complications that arises in wide-bandwidth amplifier design includes, increase in reverse gain $|S_{12}|$ and noise figure at high frequency. Negative

feedback configuration is used to reduce these effects and increase the bandwidth. An inductor L is connected in series with R_f such that after certain frequency the negative feedback decreases in proportion to the S_{21} roll-off. This technique improves gain flatness at high frequency. The load inductance of L_1 and L_2 replace the resistor load which is used conventionally. The magnitude of the inductor's impedance increases as frequency increases. This increase inductor impedance compensates the active device gain degradation that occurs at high frequency [13].

Another wide-band LNA design schematic is shown in Figure 3-9. In Figure 3-9, the R_f is added as a shunt feedback element to the conventional cascade narrow band LNA and L_{load} is used as shunt peaking inductor at the output. The capacitor C_f is used for the ac coupling purpose. The source follower, composed of M_3 and M_4, is added for measurement proposes only, and provides wideband output matching. C_1 and C_2 are ac coupling capacitor. The small-signal equivalent circuit at he input of the LNA is shown in Figure 3-10. The resistor $R_{fM} = R_f /(1 - A_v)$ represents the Miller equivalent input resistance of R_f, where A_v is the open-loop voltage gain of the LNA. From equivalent circuit, the value of R_f can be much larger than that of the conventional resistance shunt-feedback. In the conventional resistance shunt-feedback, the size of R_f is limited as R_{fM} determines the input impedance. One of the key roles of the feedback resistor R_f is to reduce the Q-factor of the resonating narrowband LNA

input circuit. The Q-factor of the circuit shown in Figure 3-10 can be approximately given by

$$Q_{WB} \approx \frac{1}{\left[R_S + \omega_T L_S + \frac{(\omega_0 L_g)^2}{R_{fM}} \right] \cdot \omega_0 \cdot C_{gs}} \tag{3.9}$$

From (3.9), and considering the inversely linear relation between the -3dB bandwidth and the Q-factor, the narrowband LNA in Figure 3-9 can be converted into a wideband amplifier by the proper selection of R_f. To design a wideband amplifier that covers a certain frequency band, the narrowband amplifier will be optimized at the center frequency. The feedback resistor R_f also provides its conventional roles of flattening the gain over a wider bandwidth of frequency with much smaller noise figure degradation [14].

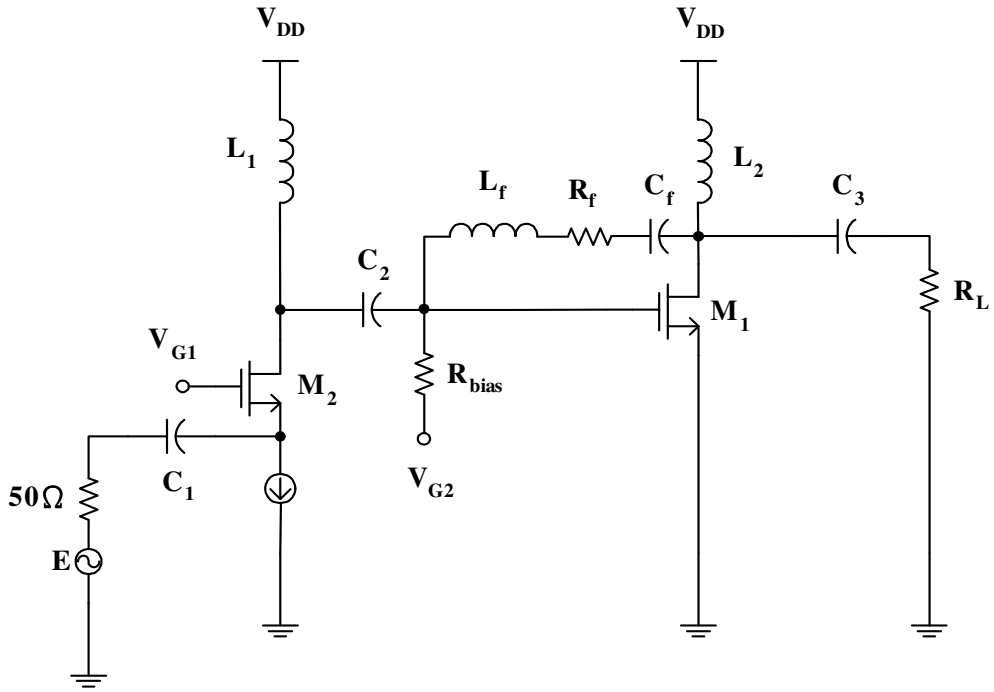

Figure 3-8 Wide-band LNA circuit schematic.

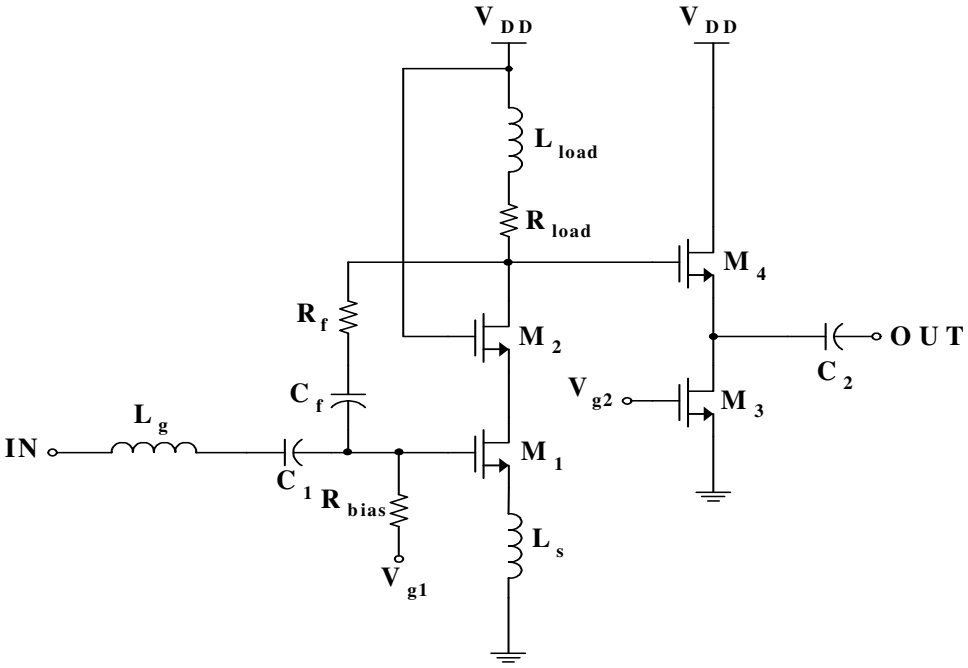

Figure 3-9 Another wide-band LNA schematic.

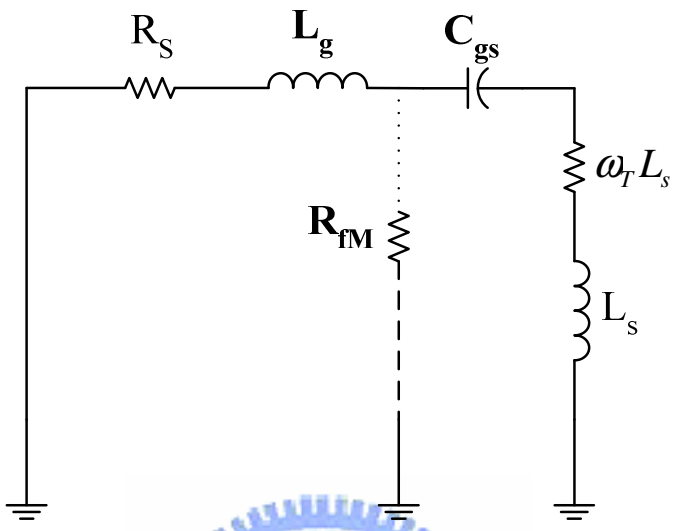

Figure 3-10 Small-signal equivalent circuit at the input.

Chapter 4

UWB CMOS LNA Design

4.1 Design Procedures

This circuit is three-stage LNA, Figure 4-1 shows the proposed ultra-wideband CMOS LNA topology, Figure 4-2 shows the chip layouts. We first use inductor-resistance feedback to pull the gain at low frequency. So we can reach flat gain in 3.1 to 10.6 GHz. As the circuit is operated when relatively low frequency, the impedance of the inductance is low, the amount of inductance-resistance feedback is strengthened, make gain drop and make circuit relatively stable, and when the circuit is operated in relatively high frequency, the impedance of the inductance is high, the amount of inductance-resistance feedback is diminished, gain drops slightly, and when the inductance in inter-stage heals high frequency, impedance heavy, make $Av1 = Gm1 \cdot Rout$ becomes great, so after the proper selecting value, will enable reaching flat-gain in operating the frequency band.

Use inductance and inductor-resistance feedback to reach input matching. At output we use current-buffer to reach matching. Inductive degeneration can be used and gone to reach simultaneous matching in narrow-band amplifier. The same, can also be used in Broadband amplifier to reach matching.

The ultra-wideband is for 3.1 to 10.6 GH_Z application. The flat forward gain

over the whole bandwidth is essential. A technique that satisfied this requirement of large bandwidth at low cost is known as shunt peaking. The resistance R_d improves the gain at lower frequency. At high frequency, the L_d can improve the gain.

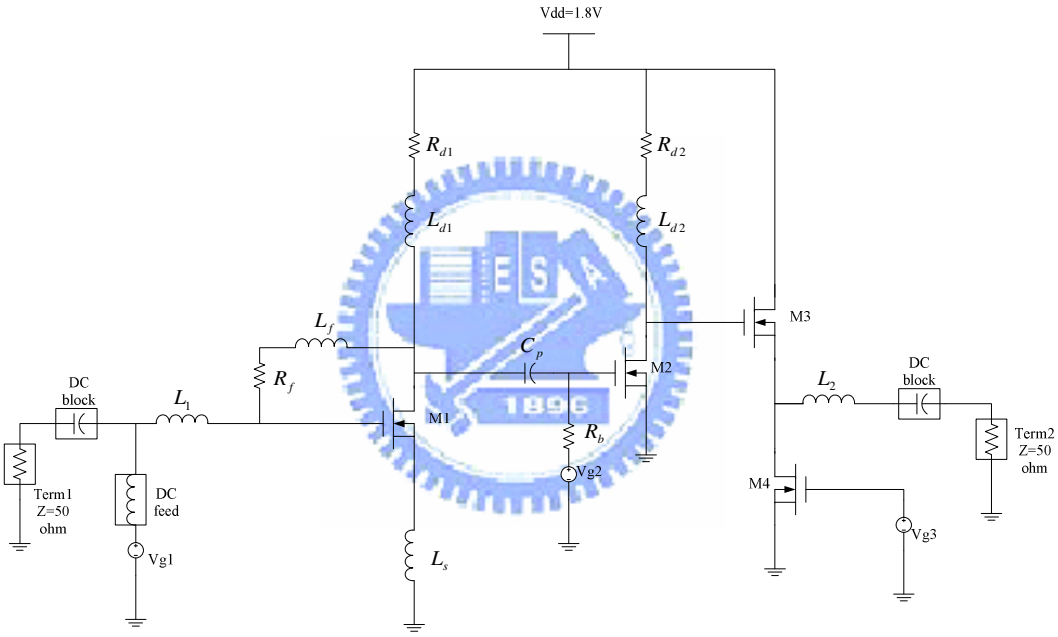

Figure 4-1 Circuits diagram.

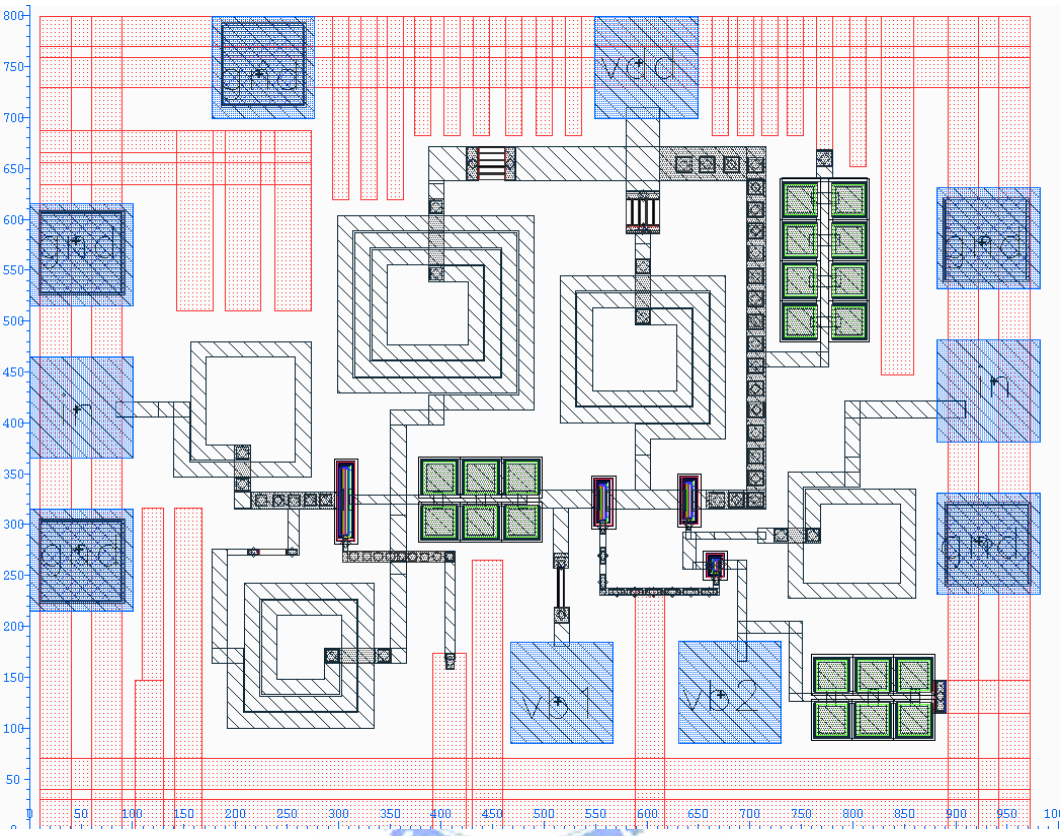

Figure 4-2 Chip layout.

4.1.1 Inductor-Resistance Feedback

We consider with a parallel low Q LC circuit, as shown in Figure 4-3, and can write a admittances formula:

$$Y_{ab} = \frac{1}{r_{LP} + jX_{LP}} + \frac{1}{r_{LP} - jX_{cp}} = \frac{r_{LP}}{r_{LP}^2 + X_{LP}^2} + \frac{r_{CP}}{R_{CP}^2 + X_{CP}^2} + j\left(\frac{X_{CP}}{r_{CP}^2 + X_{CP}^2} - \frac{X_{LP}}{r_{LP}^2 + X_{LP}^2}\right) \tag{4.1}$$

When the imaginary part is zero, it indicates that the parallel circuit is at resonance, and we get

$$\frac{X_{CP}}{r_{CP}^2 + X_{CP}^2} = \frac{X_{LP}}{r_{LP}^2 + X_{LP}^2} \tag{4.2}$$

There we use $X_{cp} = \frac{1}{\omega C_P}$ and $\omega L_P = X_{LP}$, then (4.2) become

$$\omega^2 = \frac{L_P - C_P r_{LP}^2}{L_P C_P (L_P - C_P r_{CP}^2)} \tag{4.3}$$

From (4.3), if we choose

$$r_{LP} = r_{CP} = \sqrt{\frac{L_P}{C_P}} \tag{4.4}$$

then the tank circuit should be pure resistance at any frequency.

The Figure 4-4 shows a general common-source amplifier with inductor degeneration, that input impedance has the following form:

$$Z_{in} = \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_S \approx \frac{1}{sC_{gs}} + \omega_T L_S \tag{4.5}$$

And we consider an inductor-resistor feedback amplifier which is shown at Figure 4-5, the feedback circuit can be analysis by Miller approximation. It is result that an equivalent circuit is shown at Figure 4-6, where $Lf = (L2/Av)$ and $Rf = (R2/Av)$, Av is noted as voltage gain. Figure4-6 is similar to Figure 4-3, if we set $Cgs = C_P, Lf = L_P$ and $r_{CP} = \omega_T L_S$. And from (4.4) we can get the formula:

$$Lf = (\frac{g_m}{C_{gs}} L_S)^2 \times C_{gs} = (g_m L_S)^2 / C_{gs} \tag{4.6}$$

and

$$L2 = Av \cdot Lf \tag{4.7}$$

So, from (4-6) and (4-7), feedback inductor can be decided.[15]

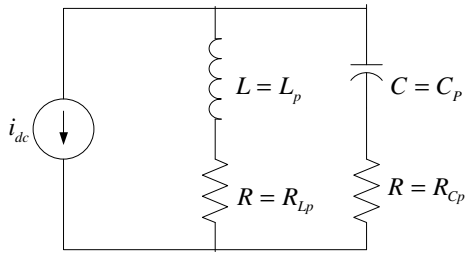

Figure 4-3 Parallel resonance circuits.

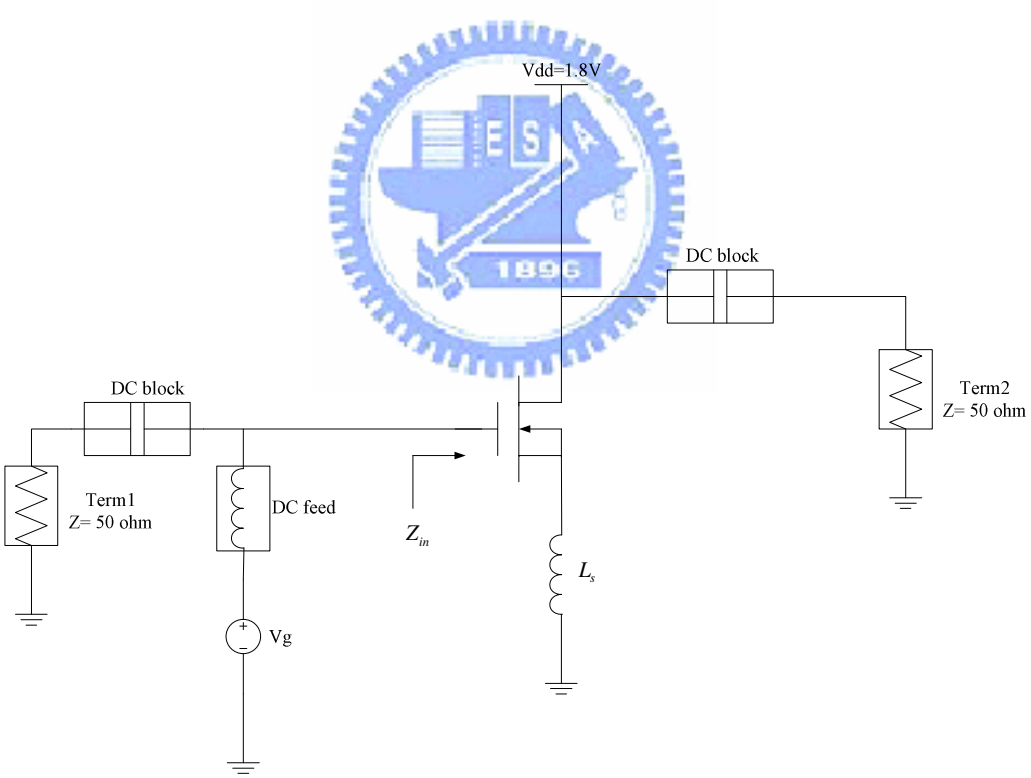

Figure 4-4 C-S amplifier with source degeneration.

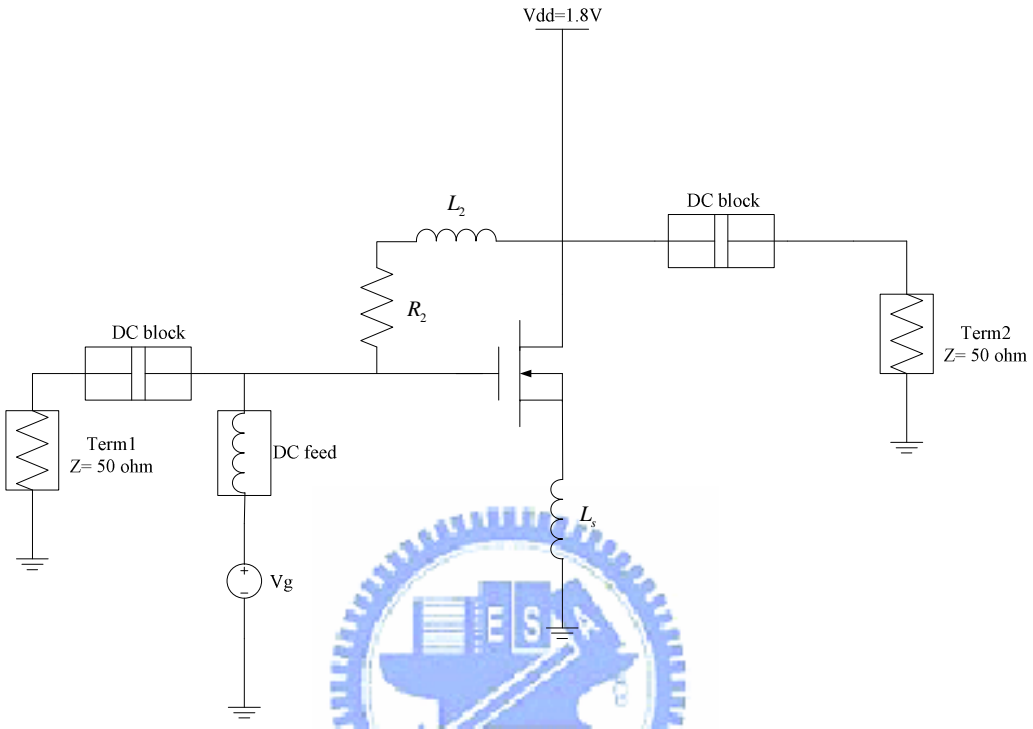

Figure 4-5 A source degeneration amplifier with inductor-resistor feedback.

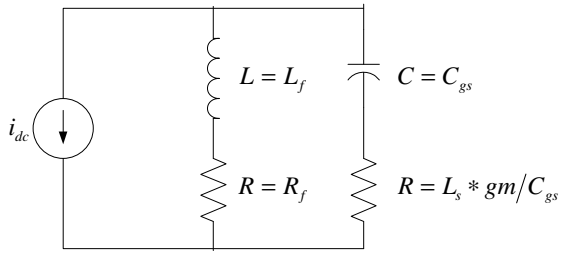

Figure 4-6 The equivalent circuit of source degeneration amplifier with inductor-resistor feedback.

4.1.2 Shunt Peaking

A model of shunt peaking amplifier is shown in Figure 4-7. The capacitance *C* may be taken to represent all the loading on the output node, including that of a subsequent stage. The resistance *R* is the effective load resistance at that node and the inductor provides the bandwidth enhancement. It's clear from the model that the transfer function v_{out}/i_{in} is just the impedance of the *RLC* network, so it should be straightforward to analyze. The addition of an inductance in series with the load resistor provides an impedance component that increases with frequency, which helps offset the decreasing impedance of the capacitance, leaving net impedance that remains roughly constant over a broader frequency range than that of the original *RC* network. The impedance of the *RLC* network may be written as

$$Z(s) = (sL + R) // \frac{1}{sC} \tag{4.8}$$

We introduce a factor *m*, defined as the ratio of the *RC* and *L/R* time constant:

$$m = \frac{RC}{L/R} \tag{4.9}$$

Then, the transfer function becomes

$$Z(s) = \frac{R[s(L/R)]+1}{s^2LC+sRC+1} = \frac{R(\tau s+1)}{s^2\tau^2 m+s\tau m+1} \tag{4.10}$$

where $\tau = L/R$.

The magnitude of the impedance, normalized to the DC value as a function of frequency, is then

$$\frac{|Z(j\omega)|}{R} = \sqrt{\frac{(\omega\tau)^2 + 1}{(1-\omega^2\tau^2 m)^2 + (\omega\tau m)^2}} \tag{4.11}$$

so that

$$\frac{\omega}{\omega_1} = \sqrt{\sqrt{\left(-\frac{m^2}{2}+m+1\right)^2 + m^2} + \left(-\frac{m^2}{2}+m+1\right)} \tag{4.12}$$

where ω_1 is the uncompensated -3dB frequency. Chose $m = 1+\sqrt{2} \approx 2.414$, then can lead to a bandwidth that is about 1.72 times as large as the un-peaked case. Hence, at least for the shunt-peaked amplifier, both a maximally flat response and a substantial bandwidth extension can be obtained simultaneously.[9]

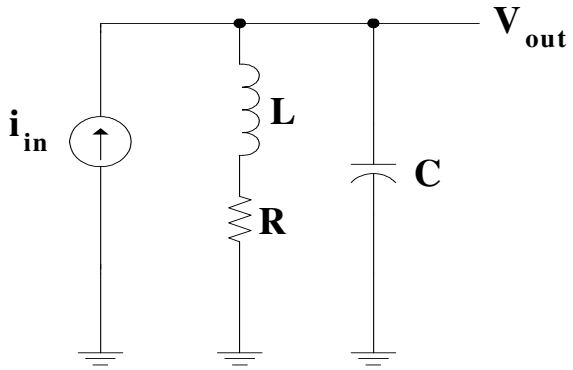

Figure 4-7 The model of shunt peaking amplifier.

4.2 Simulation Results

Figure 4-8 shows the simulated input and output reflection coefficients. S11 is lower than -10dB between 3.1 and 12GHz. The output buffer achieves excellent matching such that S22 is lower than -16dB from 3.1GHz to 10.6 GHz. Figure 4-9 is the power gain versus frequency, and the maximum power gain is 9.27dB in our simulation results. Since the output source follower drives a matched load, the voltage gain of the core amplifier is exactly 6dB higher than S21. The -3dB bandwidth is 0.4~9.9GHz for the simulation. The noise figure (NF) of this UWB LNA is shown in Figure 4-10. The noise figure is as low as 4.12dB at 10.6GHz, while the average noise figure in-band is about 4.7dB. Figure 4-11 and 4-12 show the simulated reverse isolation S12 and stability factor respectively. The two-tone test results for third-order intermodulation distortion are shown in Figure 4-13. The test is performed at 5.5GHz. IIP3 is to 5.19dBm, and the input referred 1-dB compression point (ICP) is -2dBm. These results imply excellent linearity of our LNA. The proposed UWB LNA dissipate 23.04mW with a power supply of 1.8V.

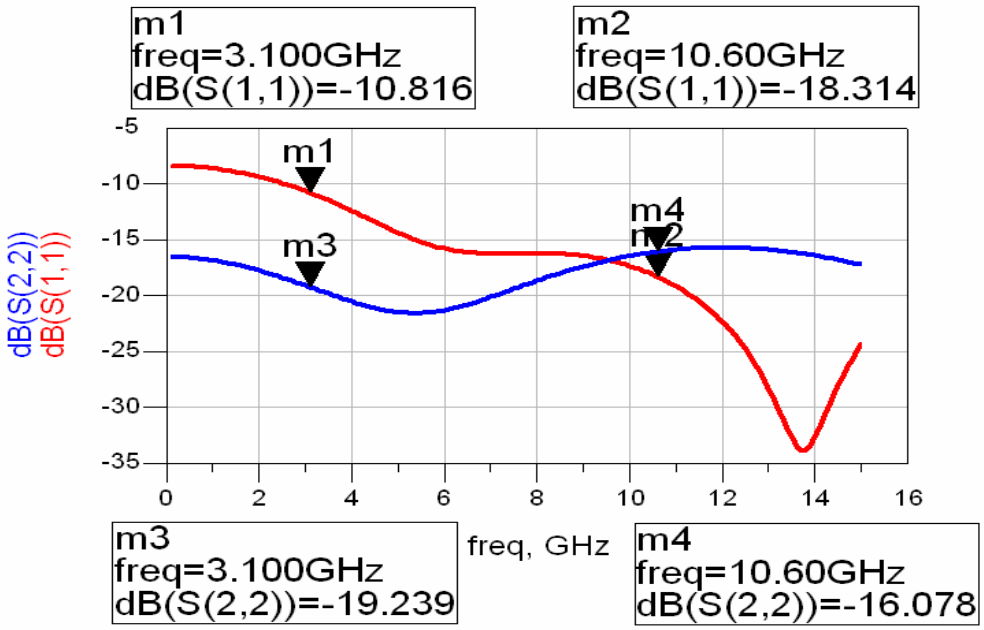

Figure 4-8 Simulated S11&S22.

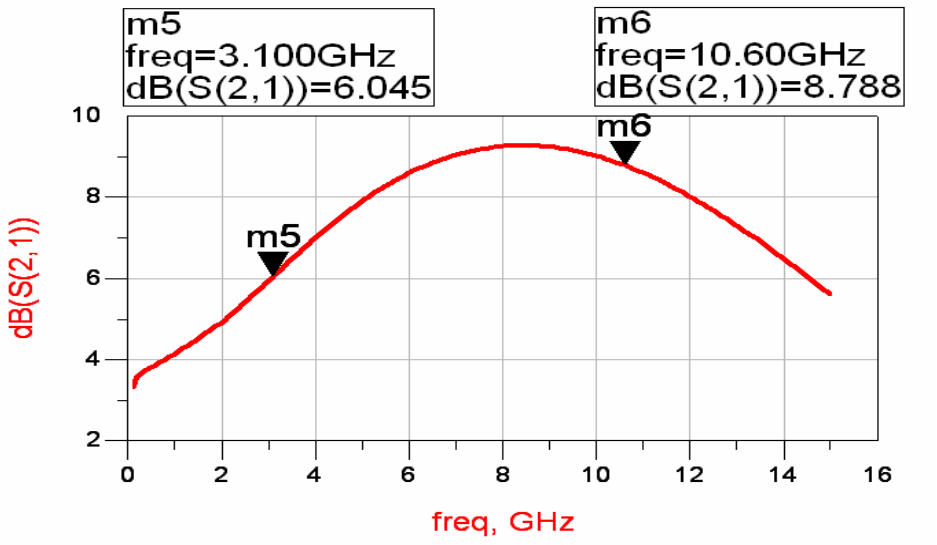

Figure 4-9 Simulated S21.

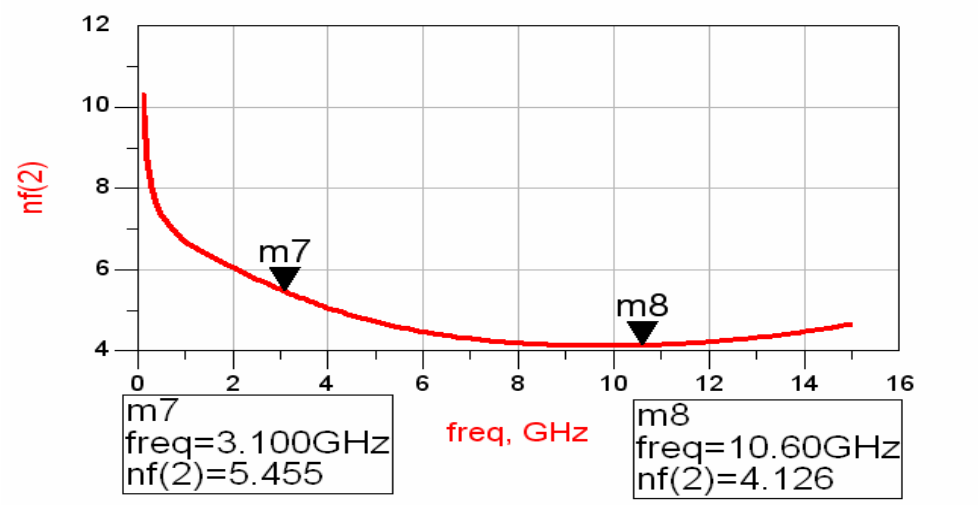

Figure 4-10 Simulated NF.

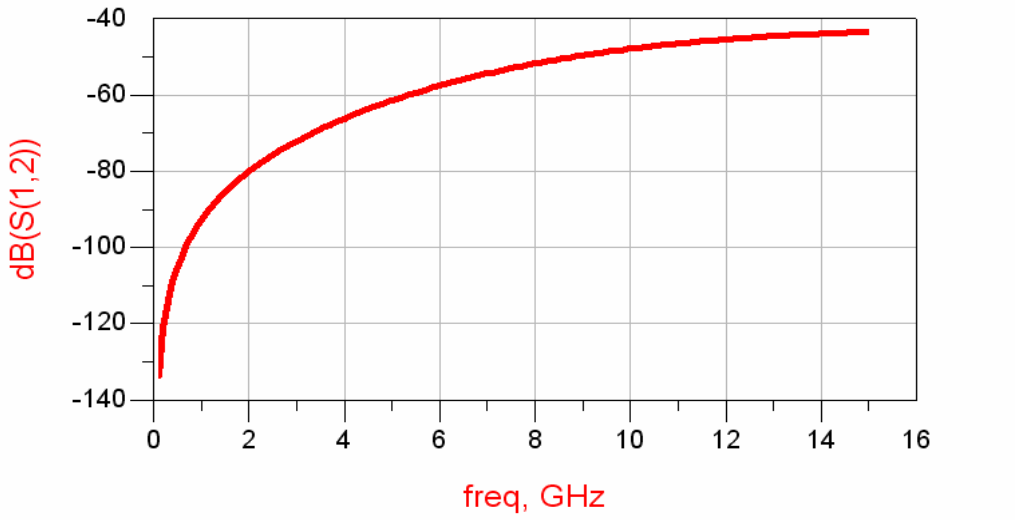

Figure 4-11 Simulated S12.

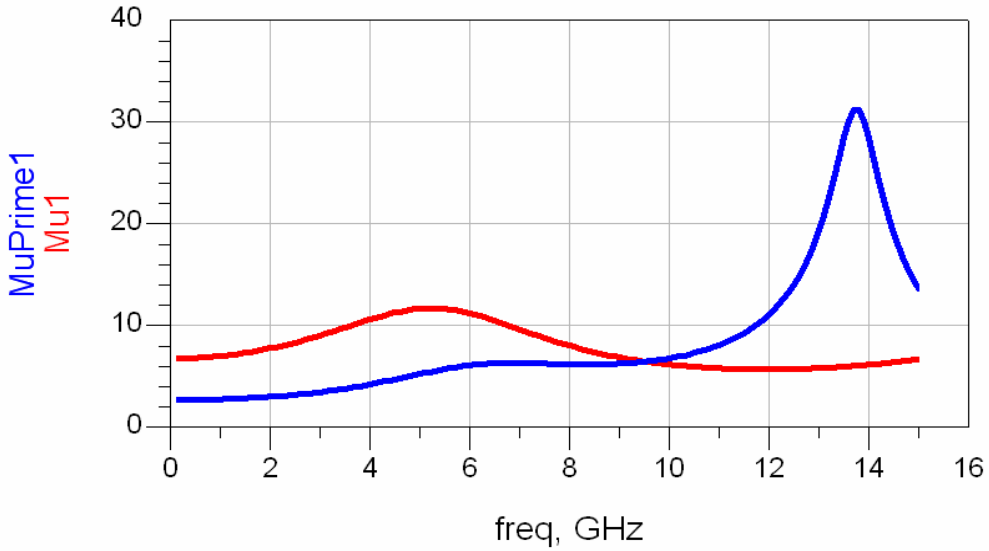

Figure 4-12 Simulated stability.

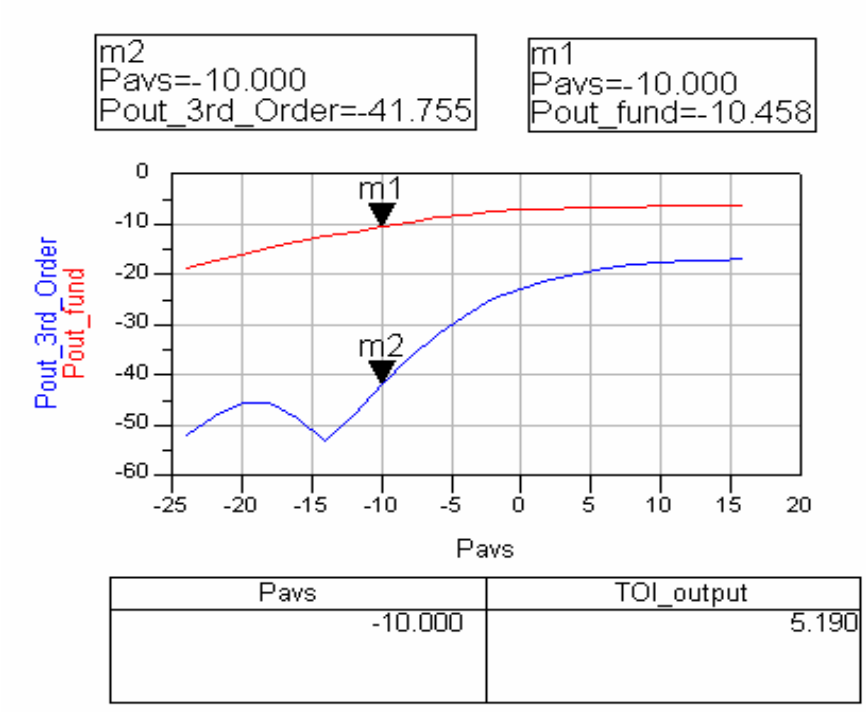

Figure 4-13 Two tones test.

4.3 Measurements and Conclusions

The following Figure4-14 ~ Figure4-19 are the measurement result which are slightly different from simulation. Which imply good accuracy of simulation and good circuit design. The some of the gain compression at high frequency showing in Figure 4-14 maybe due to the underestimate of the load resistor parasitic.

The bandwidth of this work with considering matching and gain is from 2 to 10 GHz, while the average gain is about 7dB. Figure 4-16 shows the measurement result of S11 and the Figure 4-17 shows the measurement result of S22. Input and output matching are achieved very well from 2 to 10 GHz. The S11 can bellow -9dB and the S22 can bellow -16dB. Figure 4-18 shows the measured noise figure. The noise performance is very flat and the minimum noise figure is 5.97dB at 4GHz. The noise figure can be better if we solve the resistor parasitic. Figure 4-20 shows the die photo of this circuit. Total power consumption is 32.7mw which the vdd is 1.8V and vg1 is 0.75v and vg2 is 0.7v. Table 4.1 is the measurement result summary. By the inductor-resistance feedback we proposed, a good input and output matching, broadband, a low power consumption amplifier is developed for UWB system applications.

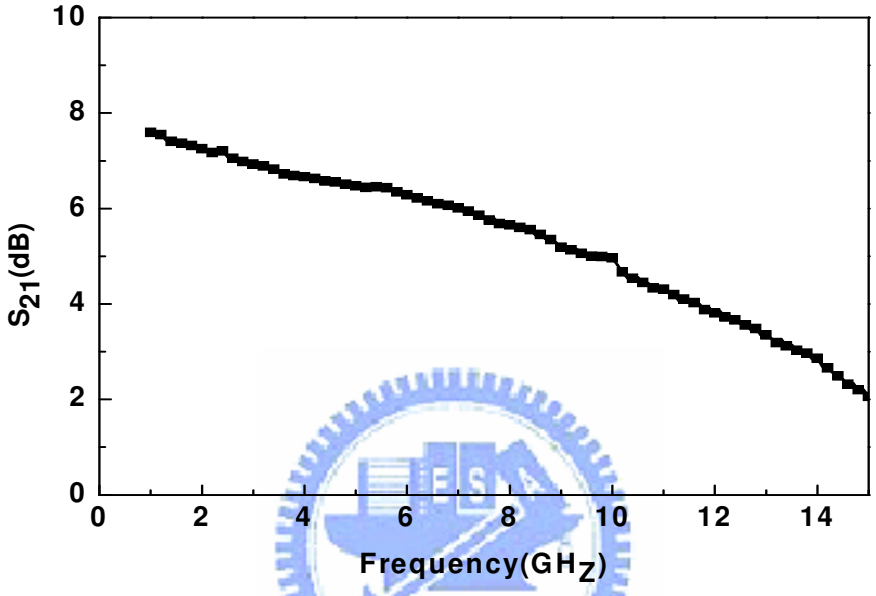

Figure 4-14 Measured S21.

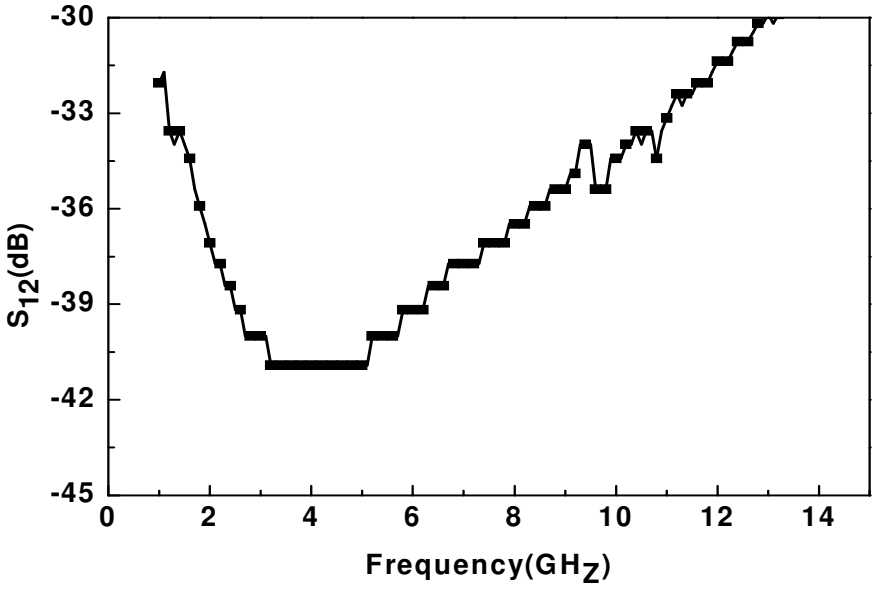

Figure 4-15 Measured S12.

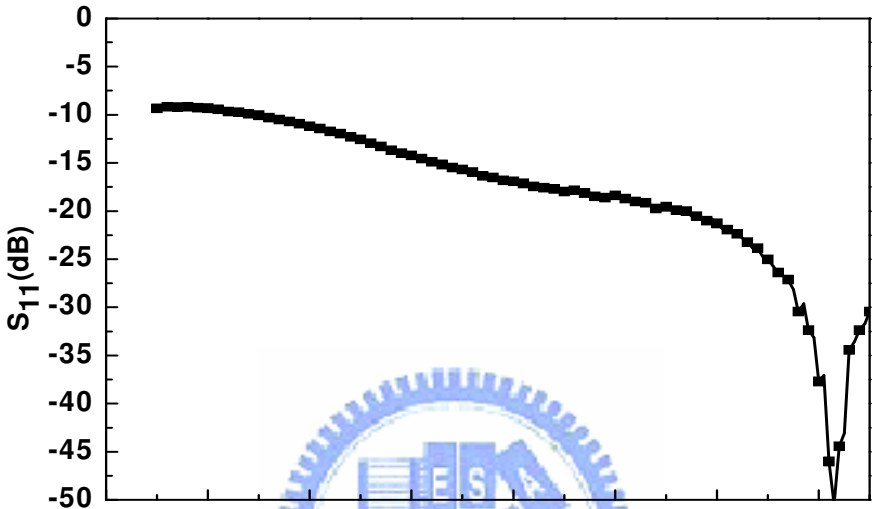

Figure 4-16 Measured S11.

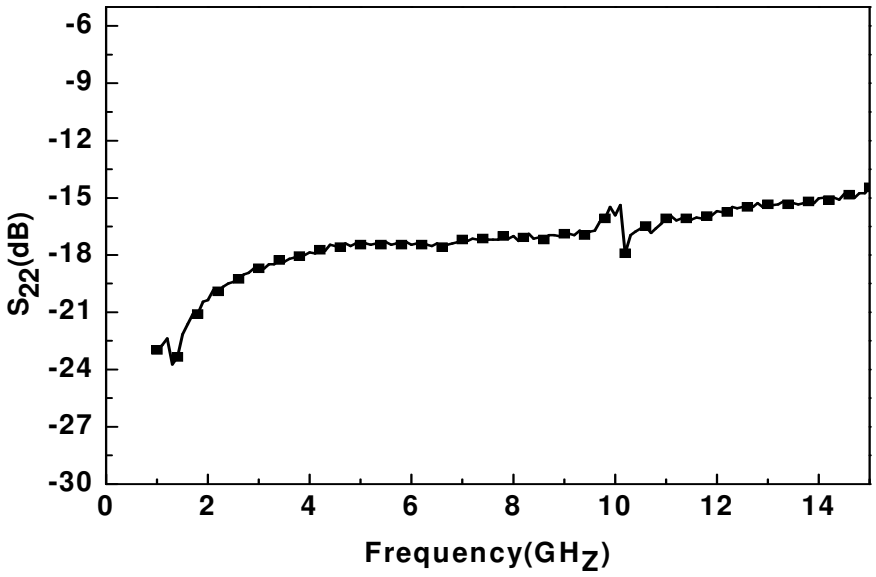

Figure 4-17 Measured S22.

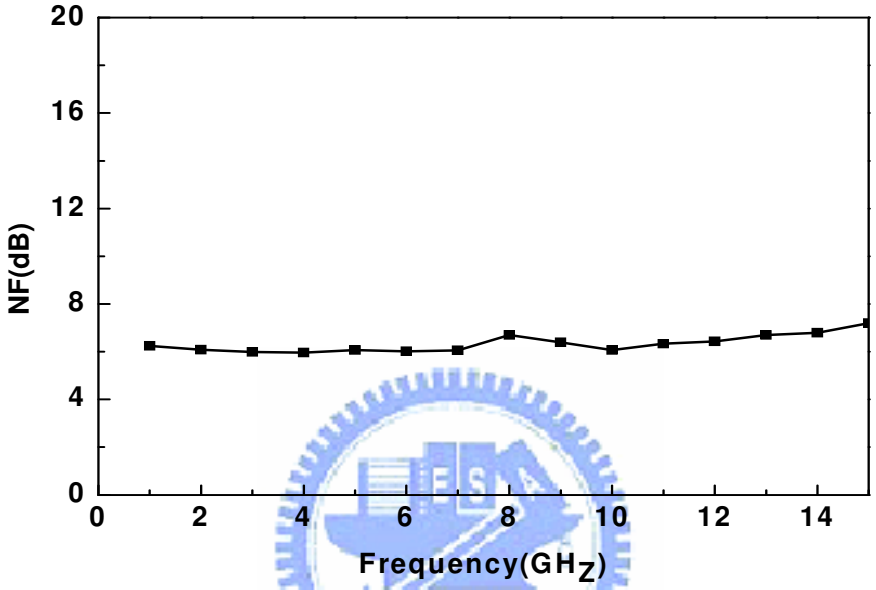

Figure 4-18 Measured noise figure.

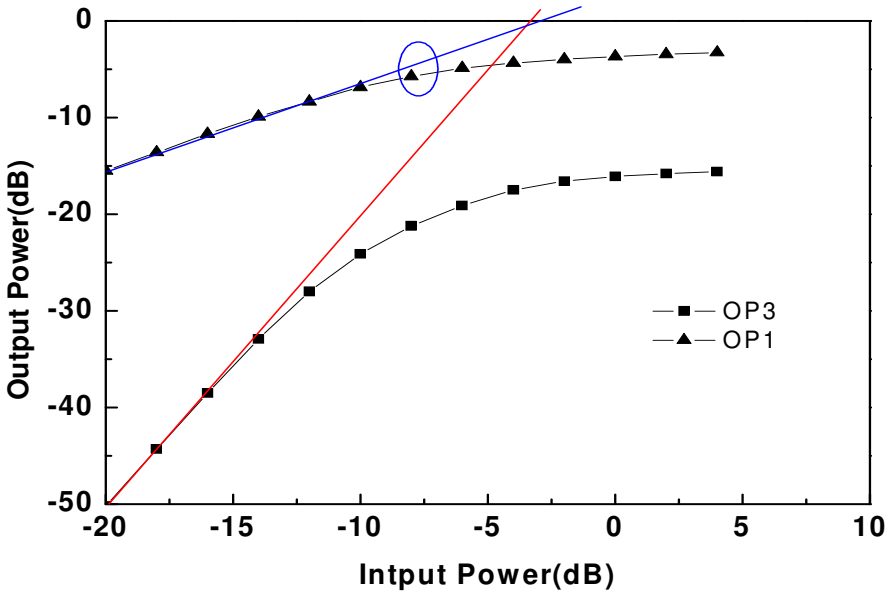

Figure 4-19 Measured linearity.

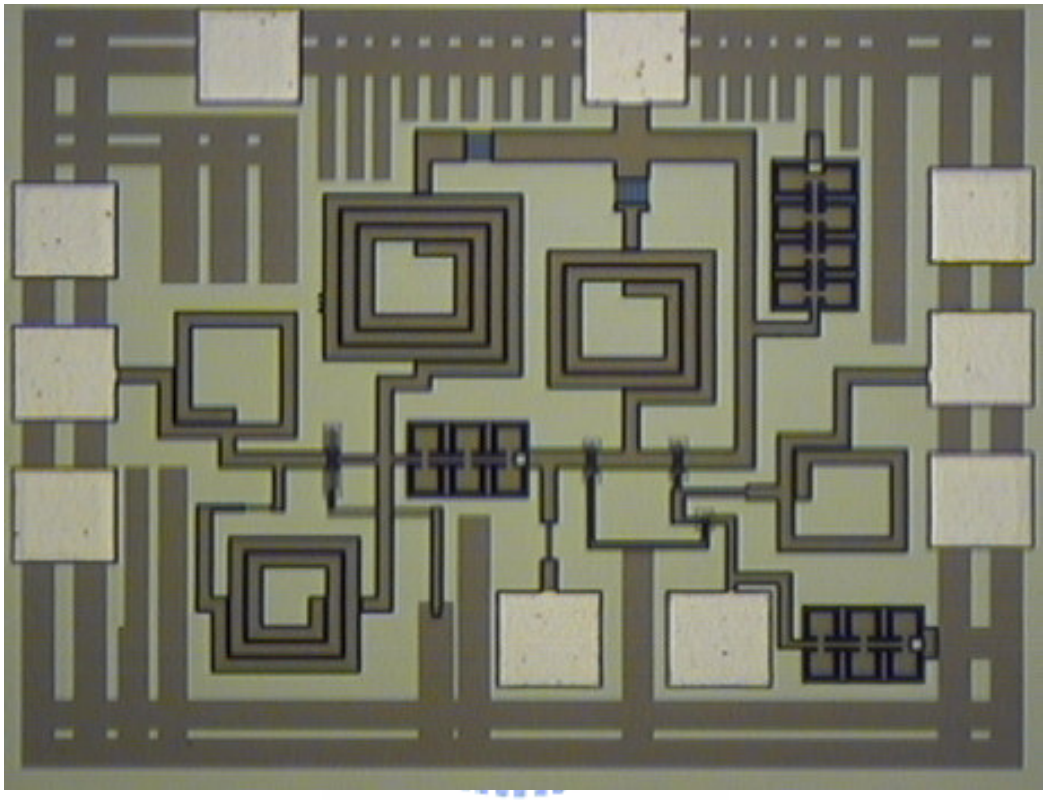

Figure 4-20 Die photo.

B.W. **(GHz)**	**Gain** **(dB)**	**NF** **(dB)**	**S11** **(dB)**	**S22** **(dB)**	**IIP3** **(dBm)**	**Pdc** **(mW)**
2~11	7	6.2	< -9	< -16	-3	32.7

Table 4.1 Measured results summary.

Chapter 5

Summary

By the inductor-resistance feedback we proposed, a good input and output matching, broadband, a low power consumption amplifier is developed for UWB system applications.

Table 5.1 is the comparison of broadband LNA performance. We can find out by this table , by using R -L feedback technolog y, can pull to bei ng wide very big arrival 2-11GHz frequently. All the advantages are important for UWB system considerations.

Ref.	**B.W. (GHz)**	**Gain (dB)**	**NF (dB)**	**S11 (dB)**	**S22 (dB)**	**IIP3 (dBm)**	**Pdc (mW)**	**Tech.**	**year**
[16]	2.4~9.5	9.3	4~9	< -9	< -20	-6.7	9*	.18 CMOS	2004
[17]	0.6~22	8.1	4.3~6	< -8	< -9	NA	52	.18 CMOS	2003
This work	2~11	7	6.~6.3	< -9	< -16	-3	32	.18 CMOS	2006

Table 5.1 Comparison of broadband LNA performance　　* LNA core only

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論文題目：

應用於超寬頻3.1-10.6 GHz低雜訊放大器之設計

Design of an UWB CMOS LNA for 3.1 to 10.6 GHz with RL-feedback