CHAPTER 2

THE CHARACTERISTICS OF NANODEVICE AND CMOS SENSING CHIP

2.1 THE OPTICAL AND ELECTRICAL PROPERTIES OF Au and CdSe NANOPARTICLES

Recently, many several of nanostructure or nanoparticles (NPs) has been proposed and improved significantly. They have their unique electrical and optical properties, herein, in order to achieve a nanodevice that have good performance, we must to know their electrical and optical properties as well as the size and the synthesis procedure of the NPs. In nanometer-sized metal particles (e.g., gold and silver) are certain to be important fundamental building blocks of future nanoscale electronic and optical devices. However, there are numerous challenges and questions that must be addressed before NPs technologies can be implemented successfully. Metal particles comprise a fundamentally interesting class of matter in part because of an apparent dichotomy that exists between their sizes and many of their physical and chemical properties. For example, Au particles may be synthesized in diameters that span from the macroscopic down to the molecular scale (0.8 μm). Across almost this entire size regime, however, their electrical and optical behaviors are described with relatively simple classical equations, rather than the quantum mechanical concepts required understanding molecular entities. The classical free electron theory combined with optical constants for bulk gold is employed to successfully model the intense visible extinction of Au NPs. Moreover, the electrical and optical properties of metal particles can be tuned considerably simply by adjusting the size, shape, or extent of aggregation of the particles. For example, a typical solution of 13 nm diameter Au NPs is red in color and exhibits a surface plasmon band centered at

518-520 nm. After aggregation, the extended polymeric Au NPs/polynucleotide aggregate shows a red to purplish blue color change in solution, due to a red shift in surface plasmon resonance of Au NPs [4]. The optical property of Au NPs is dominated by collective oscillation of conduction electrons resulting from the interaction with electromagnetic radiation. The electric field of incoming radiation induces the formation of a dipole in the NP. A restoring force in the NP tries to compensate for this, resulting in a unique resonance wavelength. The oscillation wavelength depends on particle size, particle shape and surrounding medium. [27]

In semiconductor nanocrystals, however, exhibit a wide range of size-dependent properties when the size regime is below 10 nm [9] [11]. Variations in fundamental characteristics ranging from phase transitions to electrical conductivity can be induce by controlling the size of the crystals [11]. There are two major effects to explain these size variation properties in nanocrystals. First, the number of surface atoms is a large fraction of the total atoms of a single nanocrystal. The high surface-to-volume ration will make a contribution to variations in thermodynamic properties of nanocrystals, such as melting point, and solid-solid phase transition. Second, nanocrystals with the same interior bonding geometry as the corresponding bulk material but with only a few hundred to thousand atoms exhibit dramatic size-dependent optical and electrical properties. These variations are because the density of states of electronic energy levels transforms as a function of the size of interior nanocrystal, known as **quantization effects** [11]. Nanocrystals lie in between the atomic and molecular limit of discrete density of electronic states and the extended crystalline limit of continuous bands.

The diagrams of density of states in metal and semiconductor nanocrystals are shown in Fig. 2.1. Now in any material, there will be a size below which there is substantial variation of fundamental electrical and optical properties with size, which will be seen when the energy level spacing exceeds the temperature. For a given temperature, this occurs at a very large size in semiconductors, as compared to metal, insulators, and Van der Waals or molecular crystals. This can be understood by considering that the bands of a solid are centered about atomic levels, with the

width of the band related to the strength of nearest-neighbor interactions. As the size of solid increases, the center of a band develops first and the edges develop last. Thus, in metal, the Fermi level lies in the center of a band, so that the relevant energy level spacing is still very small, and at temperature above a few Kelvin, the electrical and optical properties of a metal solid react more closely like those of no energy level spacing, even as small as tens or hundreds of atoms. In semiconductor, however, the Fermi level lies between two bands, so that the edges of bands dominate the low-energy optical and electrical behavior. Optical excitations across the gap depend strongly on the size, even for crystallites as large as 10,000 atoms. Besides, the HOMO-LUMO gap increases as the semiconductor nanocrystals become smaller (bellow 10 nm) [11].

In this work, we used water-soluble negative-charged D, L-mercaptosuccinic acid (MSA)-capped and positive-charged 2-aminoethane thiol (AET)-capped CdSe/ZnS (core/shell) NPs of approximately 5 nm in diameter as photoreceptors to detect lamination with above band gap photoexcitation [11]. We proposed two nanodevices composed of semiconductor NPs and/or metal NPs for self-assembly: (1) Au / AET-CdSe/ZnS. (2) MSA-CdSe/ZnS / AET-CdSe/ZnS. However, some properties about CdSe NPs we must to know that the **exciton Bohr radius** r_b is the spatial extent of the electron hole pair in material and is defined as $r_b = 4\pi\hbar^2\varepsilon / (m * e^2)$, where $\hbar$ is the Plank's constant, ε is the permittivity in bulk material, and m* is the effective mass. For CdSe semiconductor, the electron's effective mass is 0.13 m_e and hole effective mass is 0.45 m_e. So the exciton Bohr radius of CdSe is calculated to be 4.9 nm [8] [9]. If the dimension of CdSe NPs is smaller than 4.9 nm, the **quantum confinement** of electron hole pairs effects significantly. As size is reduced, the electronic excitation shift higher energy, and there is concentration of oscillator strength into a few transitions [9]. The dynamics of the charge carriers in CdSe NPs have been studied in several reports. These studies revealed that photoexcitation leads to a bleach of the lowest exciton transition within the first few hundred femtoseconds [20]. The bleach recovery has a lifetime between several picoseconds to microseconds, which is similar to the lifetime of the photoluminescence. In literature, it is well known that electron acceptors adsorbed on the surface of

CdSe NPs quench the exciton emission by fast electron transition [20]. Monitored the electrons shuttling across the interface of CdSe NPs by femtosecond laser spectroscopy and showed that in CdSe NPs with no electron acceptors adsorbed on the particle surface, the excited electrons get trapped at the surface within 30 ps. Subsequently, electron-hole recombination takes place on a much longer time period of > 10^{-7} s [20]. This is quite a useful knowledge for understanding the dynamics of electrons in CdSe NPs.

The electrical transport properties of nanocrystals also depend strongly on size. On extended crystal, the energy required to add successive charges does not vary. In a nanocrystal, the presence of one charge prevents the addition of another charge. Thus, in metal or semiconductor, the current-voltage curves of individual nanocrystal resemble a staircase, known as **Coulomb blockade effect** [11]. Steps in the staircase are spaced proportional to 1/radious of nanocrystal. A typical Coulomb blockade staircase is shown in Fig. 2.2.

2.2 REVIEW ON Tyramine-CdSe / Au NANODEVICE

The nanodevice composed of Citrate-capped Au NPs and Tyramine-capped CdSe NPs has been designed and fabricated on silicon chip previously [14]. The silicon chip was fabricated in 0.35μm 2P4M CMOS technology. The electrodes structure was formed by opening a passivation window (86 μm^2) over a pair of closely separated (5-15 μm) Al metal lines. The two metal lines were connected to two pads on the chip respectively; on the other hand, serve as two electrodes that make close attachment to the nanodevice. First, the chip was modified by 10% TMSPED/methanol to make the silicon oxide substrate provide amino groups ($-NH3^+$). Subsequently, Au NPs (~15 nm) and CdSe NPs (~5 nm) will be self-assembly layer-by-layer, between the electrodes. The overall fabrication process of the Au/CdSe nanostructure was observed and evaluated by SEM images at each stage of the procedure, are shown in Fig. 2.3, and the close photographs of SiO_2/Si wafer fragments before and after repeated assembly process are shown in Fig. 2.4.

The optical microscope image of the silicon chip before the fabrication of the nanodevice is shown in Fig. 2.5(a), where electrodes of various shapes and sizes were fabricated at the central part. The SEM images of the two sets of electrodes, 30 μm / 15 μm and 30 μm / 5 μm (width / length) are shown in Figs. 2.5(b) and 2.5(c). The images recorded by the edge of the electrodes after the fabrication of the single-layered structure of (Au NPs / SiO_2) and the four-layered structure (CdSe NPs / Au NPs / CdSe NPs / Au NPs / SiO_2) are shown in Figs. 2.5(d) and 2.5(e). Therefore, a 2.5mW/cm^2, 375 nm laser source was employed for the photo-activation.

For the structure with only a layer of Au NPs on the silicon oxide surface (Au NPs / SiO_2), the I-V characteristics were virtually identical to those of the open electrodes. A current of less than 10 fA was observed throughout the applied voltages with or without illumination. The relatively large distance [5-20 nm, Fig. 2.3(f)] between the Au NPs prohibited the electrodes from tunneling between the NPs and electrodes. However, for the four-layered structure (CdSe NPs / Au NPs / CdSe NPs / Au NPs / SiO_2), the nanodevice was resistive in the dark and produced a constant increment of photocurrent after illumination. The measurement results of the four-layered nanodevice are shown in Fig. 2.6. There are several notable characteristics of the results and a new model is developed to explain the measured characteristics. Firstly, the increment of photocurrent throughout the applied voltage biases after illumination was found to be constant and specific to the electrodes type, 2 nA (30 μm / 15 μm) and 1.2 nA (30 μm / 5 μm). In the proposed nanodevice structure, there are many semiconductor-metal junctions formed at the interfaces between CdSe and Au NPs. They are called the 'nano-Schottky-diodes' because of the nano-scale and the semiconductor-metal contact. The small size and high surface-to-volume ratio of NPs causes a massive number of nano-Schottky-diodes structure to be formed in a very small volume. Since the Au NPs have low conductivity due to their small size, they can be treated as resistors. Thus the proposed Au/CdSe nanodevice structure forms a there-dimensional array of nano-Schottky-diodes and resistors as shown in Fig. 2.7(a). For simplicity of discussion, only one-dimensional array is considered here. When applying a voltage bias between the two electrodes, the two nano-Schottky-diodes associated

with a CdSe NP become forward-biased and reserve-biased alternately along one direction [21]. Since the CdSe NPs have a diameter of ~5 nm, the reverse-biased nano-Schottky-diode causes its CdSe NP to be fully depleted even under zero bias. With uniform photoexcitation ($h\upsilon > E_g$), electron-hole-pairs generated within the CdSe depletion region of reverse-biased Schottky junctions are separated by the electric field with electrons swept to the Au NP of the forward-biased Schottky diode and holes swept to the Au NP of the reverse-biased Schottky diode, producing the photocurrent. Since the CdSe NP is fully depletion even at zero bias, the generated photocurrent is constant for different bias voltages and hence the conductivity does not increase under light illumination as shown in Fig. 2.6. This characteristic is different from that of bulk CdSe where the conductivity increases after illumination. By illuminating the CdSe NPs with light source of wavelength for above bandgap excitation ($h\upsilon > E_g$), the electrons in the nanocrystal will be excited to the particles surface, and be trapped on the surface for 30 ps. If the electric field between electrodes is large enough to take these electrons into current flow, the increased conductivity of nanodevice will be observed. However, if the electric field is not large enough or the nanostructure of CdSe NPs is partially damaged by photooxidation, the phenomenon of increased conductivity after illumination will not be observed. For Au NPs, they have no response to illumination, even with quantum size. As we described above, across all size regime, the Au NPs are always behave like pure metal.

From the conduction mechanism of the array of nano-Schottky-diode and resistors described above, a new model was proposed. In the dark condition, a large resistor R2 = 5MΩ is connected in parallel with the reverse-biased Schottky diode D2, representing the small reverse-biased diode conductance as shown in Fig. 2.7(b), where the resistance of Au NPs is R1 = 1MΩ. Under steady illumination, the large resistor R2 is replaced by a very small current source I = 5pA, as shown in Fig. 2.7(c), representing the photocurrent generated by the reverse-biased Schottky diode. As shown in the measurement result, the conductivity of the proposed nanodevice structure varies with length when width was kept constant. There was less conductivity with the increased length but a larger generated photocurrent under illumination was obtained. For electrodes of length 15 μm, the average

resistance R was 33.1 KΩ and average photocurrent $I_{illumination}$-I_{dark} = 2 nA. For electrodes of length 5 μm, the average resistance R was 24.1 KΩ and average photocurrent $I_{illumination}$-I_{dark} = 1.2 nA. To explain this I-V behavior, the circuits in Figs. 2.7(b) and 2.7(c) were simulated by HSPICE with a voltage bias (0.4V). To simulate the nanodevice structure with long (short) length, 45 (15) subcircuits were connected in series. From the simulation results, a photocurrent of 3.3 pA for the longer chain (45 subcircuits) and 1.4 pA for the shorter chain (15 subcircuits) were obtained. Physically, the larger photocurrent in the longer nanodevice structure was caused by the larger number of reverse-biased Schottky diodes, which had forward photovoltaic voltages to effectively increase the bias voltage of the array and thus the photocurrent.

When compared to the conventional CdSe thin film [22], the four-layered photo-sensing nanodevice has a much higher photocurrent volume density (PVD). In [22], the CdSe thin film of 200 nm thick was deposited on a glass substrate by thermal evaporation technique. The electrodes with a 3-mm space were made to measure the photoresponse. The results show that a generated photocurrent of 1.25 nA was observed under a 10 V voltage bias and a 7600 lux white light illumination. PVD is defined as the amount of generated photocurrent per unit volume under illumination. Using this definition, it was found that the PVD of the proposed nanodevice was measured to be at least 38 times greater than that of the CdSe thin film. This high PVD is caused by the fully depleted CdSe NPs and the extremely high-density nano-Schottky-diodes. This confirms the superiority of the fabricated photo-sensing nanodevice with CdSe and Au NPs on its silicon chip. In addition to the photoconductivity property of CdSe NPs, the junctions between CdSe and Au NPs are also very important in photo-sensing behavior. Any interface between CdSe and Au NPs will result in a “nano Schottky diode” structure. For a nano diode structure, it is reasonable to detect photo illumination, like the photodiode structure based on p-n junction.

Anyway, the electrical and optical properties of Au and CdSe NPs described above provide a potential application as photo-sensor. Although the high PVD can be obtained which compared with that of the CdSe thin film. In fact, the photocurrent is too small to unfold its potential, because the

absorbance of the Tyramine-capped CdSe NPs is not obviously. In this thesis, we use water-soluble AET-capped CdSe/ZnS NPs instead of Tyramine-capped CdSe NPs and then constructed the multi-layers nanodevice composed of Au NPs and AET-CdSe/ZnS NPs. However, we also construct another nanodevice that composed of MSA-CdSe/ZnS NPs and AET-CdSe/ZnS NPs. The cross sectional figures of new photo-sensing nanodevices on silicon chip are shown in Fig. 2.8.

2.3 THE OPERATIONAL PRINCIPLES OF CMOS SENSING CHIP

Theoretically, the CdSe NPs have well-known size-dependent photoconductivity property, which means that the conductivity of CdSe NPs will increase when illuminated with light source of proper wavelength. When the size of particles becomes smaller, the energy bandgap will become larger, resulting in blue shift of absorbance spectrum. In contrast, the Au NPs have no photoconductivity behavior like metal material regardless of the size variation. However, when the two NPs are assembled together to form nanodevice on silicon oxide substrate, the overall conductivity of the nanodevice is expected to have photo-sensing property. Moreover, the mechanism and measurement of this photo-sensing property was proposed in section 2.2, and we obtained the conductivity of the nanodevice, which composed of Au and CdSe NPs does not increase after light illumination. Therefore, in this work, CMOS sensing circuit is designed to detect the transient dc photocurrent of photo-sensing nanodevice when illuminated with light of different wavelength. There is one commonly used method---to apply a voltage across the nanodevice that have a constant resistance and measure the resulting current (designed to be 50 nA) flowing through device, continuously, increase the voltage across the nanodevice to simulate the photo-sensing properties when illuminated with light of different wavelength. In order to linearly amplify the small dc current, the most convenient method is to integrate the current with time by charging a capacitance. The schematic of CMOS sensing circuit is shown Fig. 2.9. The characteristics of this circuit are: First, low current (50 nA) flowing through the photo-sensing nanodevice, preventing

from unanticipated oxidation or other forms of damage of the device. Second, high linearity and sensitivity are necessary.

The $\mathbf{M_{1\sim5}}$ and $\mathbf{M_f}$ form an operation amplifier with negative feedback loop to stabilize and lock the voltage at $\mathbf{V_{ip}}$ with $\mathbf{V_{in}}$. $\mathbf{R}_d$ is representative of the photo-sensing nanodevice and the voltage difference between $\mathbf{V_{bias}}$ and $\mathbf{V_{ip}}$ is the voltage bias across the nanodevice (V_{cross}). The current flowing through nanodevice (I_d) is linearly amplified by current mirror $\mathbf{M_6}$-$\mathbf{M_7}$ and $\mathbf{M_8}$-$\mathbf{M_9}$, each current mirror providing dc current gain 20 and 6 respectively. The current signal generated by nanodevice has two parts, the background current when dark (designed to be 50 nA) and the added light current due to illumination. Only the light current is the signal we desire. As a result, the constant background current is subtracted by $\mathbf{I_{offset}}$ to make only the added light current able to charge capacitance $\mathbf{C_a}$ and make integration with time. In this circuit, $\mathbf{M_{10}}$, $\mathbf{M_{11}}$, are used to form cascode structure to make current mirrors have larger output resistance. However, $\mathbf{M_A}$, $\mathbf{M_B}$, $\mathbf{M_C}$, is used to form active cascode structure to make current mirrors pair $\mathbf{M_{12}}$-$\mathbf{M_{13}}$ have larger output resistance. **Reset**, $\mathbf{M_{14}}$ and $\mathbf{M_{15}}$ are used to control the length of charging and discharging time period. Finally, $\mathbf{M_{16}}$ and $\mathbf{M_{17}}$ form the output stage. The DC analysis of CMOS sensing circuit is shown below:

Output (dark) = $[(V_{cross1} / R_d) * A_i - I_{offset}] * T_{charge} * (1 / C_a) + |Vgs_{17}|$

Output (illumination) = $[V_{cross2} / (R_d) * A_i - I_{offset}] * T_{charge} * (1 / C_a) + |Vgs_{17}|$

Output (illumination) – Output (dark) = $(V_{cross1} - V_{cross2}) * A_i / R_d * T_{charge} / C_a$

A_i = *DC current gain = 20 * 6 = 120*

V_{cross1} = *voltage bias across the device under dark situation*

V_{cross2} = *voltage bias across the device under illumination situation*

R_d = *the resistance of nano-photo-sensing device = 7.5 k*Ω

C_a = *the charging capacitance = 3 pF*

In the HSPICE simulation, the R_d is fixed to 7.5 kΩ to match the measurement result of 4-layered Au / AET-CdSe/ZnS nanodevice (30μm * 5μm) in section 4.6. The simulation results (TT) of CMOS sensing circuit are shown in Fig. 2.10. The voltage bias of the simulation is shown in Table 2.1. The simulation result of output versus the I_d of photo-sensing nanodevice is also shown in Fig. 2.11. The linearity is 99.85% when the I_d ranging from 50 nA to 100 nA. In addition to the output waveforms, it is also very important to make sure the voltage value of V_{ip} is locked to that of V_{in} due to the existence of operational amplifier and negative feedback loop. A part of list file of the simulation result is shown below. As we can see, the vds of M_5 + the vgs of M_f = 0.5911579 + 1.1096 = 1.700758 ~ V_{in}. Besides, the current flowing through R_d is very close to 50 nA, the value we desire. Finally, the simulation results of the other four corners (SS, SF, FS, FF) are also accomplished and checked for all MOSFETs in saturation region and the whole circuit in normal function.

subckt element	0:m1	0:m2	0:m3	0:m4	0:m5	0:mf
model	0:pch.2	0:pch.1	0:pch.1	0:nch.1	0:nch.1	0:pch.4
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-80.7277u	-40.4356u	-40.2921u	40.4356u	40.2921u	-50.1549n
ibs	15.8696a	8.2555f	8.2555f	-59.5171a	-59.3060a	115.9100a
ibd	925.9101a	14.8895p	27.4756p	-38.2199f	-38.2199f	118.1706a
vgs	-1.3000	-1.0021	-1.0013	699.0049m	699.0049m	-1.1096
vds	-597.9239m	-2.0031	-2.1109	699.0049m	591.1579m	-1.1507
vbs	0.	597.9239m	597.9239m	0.	0.	1.5992
vth	-755.4656m	-859.8218m	-859.4459m	551.9205m	552.0712m	-1.0491
vdsat	-548.7497m	-190.3974m	-190.0297m	164.8354m	164.7228m	-119.1986m
beta	539.2814u	2.7461m	2.7466m	3.2250m	3.2249m	10.3606u
gam eff	395.2365m	412.0864m	412.0864m	468.6969m	468.6969m	341.0727m
gm	253.2586u	423.5236u	422.7551u	426.3541u	425.2525u	727.4781n
gds	18.2671u	1.8353u	1.8106u	1.2891u	1.3850u	2.6920n
gmb	56.1266u	73.2146u	73.0920u	126.1849u	125.8553u	99.8688n
cdtot	13.8287f	85.4673f	84.3912f	36.6088f	37.2032f	1.3600f
cgtot	33.6159f	555.6944f	555.2094f	199.7660f	199.7660f	15.6280f
cstot	51.0927f	690.4170f	689.7340f	260.1315f	260.1316f	15.0249f
cbtot	36.1217f	307.5245f	306.4360f	137.9662f	138.5606f	7.4572f
cgs	28.9552f	489.4254f	488.8531f	169.2020f	169.2020f	11.9995f
cgd	1.8391f	16.5249f	16.5249f	6.2179f	6.2179f	192.1500a

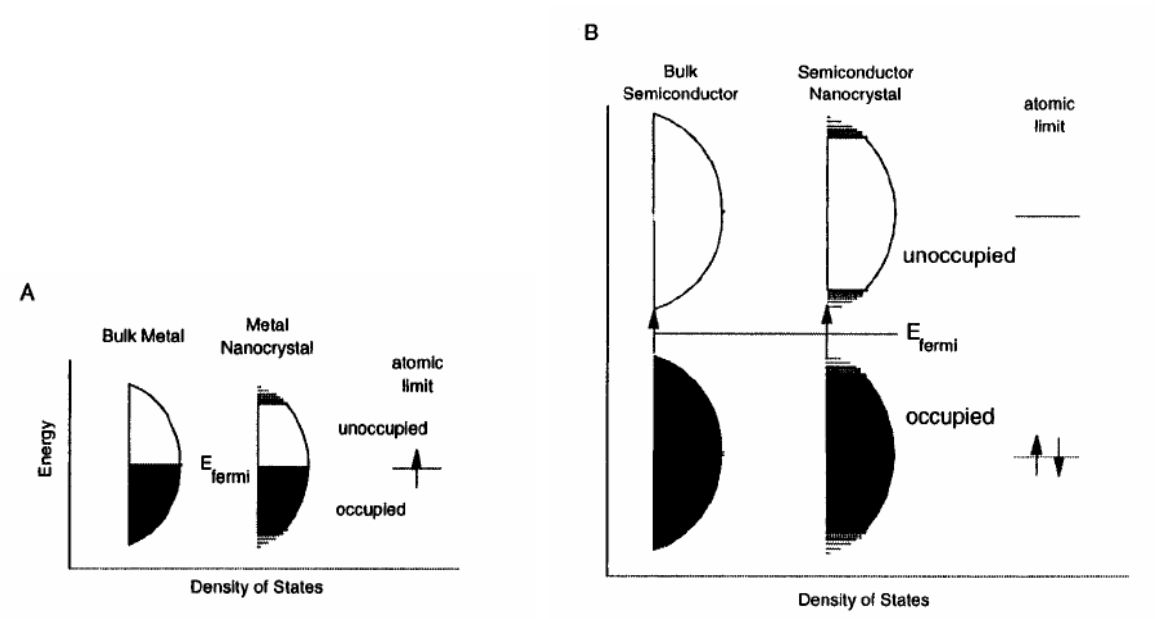
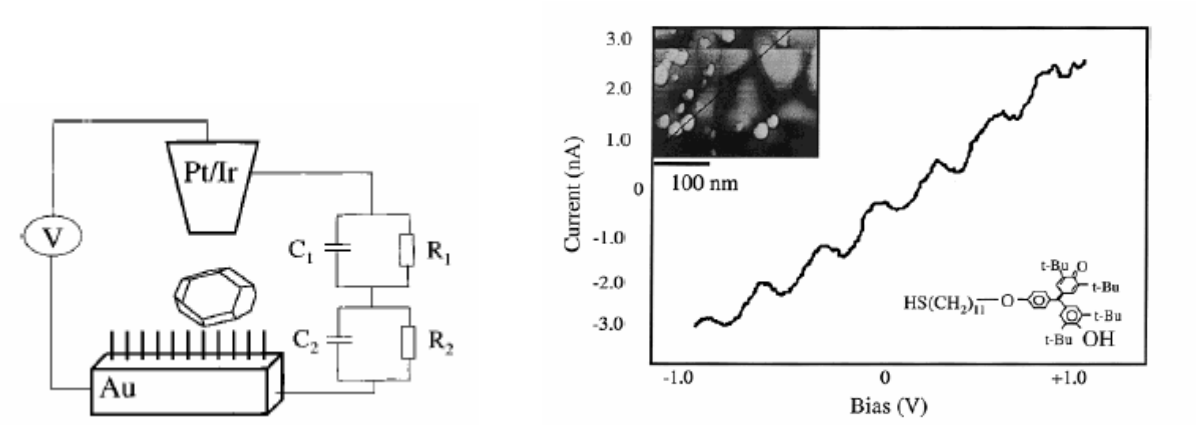


Fig. 2.1 Density of states in metal (A) and semiconductor (B) nanocrystals. In each case, the density of states is discrete at the band edges. The Fermi level is in the center of a band in a metal, and so *kT* will exceed the level spacing even at low temperature and small size. In semiconductor, the Fermi level lies between two bands, so that there is large level spacing even at large size. The HOMO-LUMO gap increases as the semiconductor nanocrystals of smaller size (bellow 10 nm) [11].



(a) (b)

Fig. 2.2 (a) Illustration of a STM tip-single metal NP-insulator coated gold substrate double tunnel junction and corresponding equivalent circuit. (b) Current versus voltage for a single galvinol-coated Au NP acquired in aqueous solution at pH 5. Insect shows an STM image of the sample. Tip was coated with Apiezon wax and gold substrate was coated with hexanethiol [8].

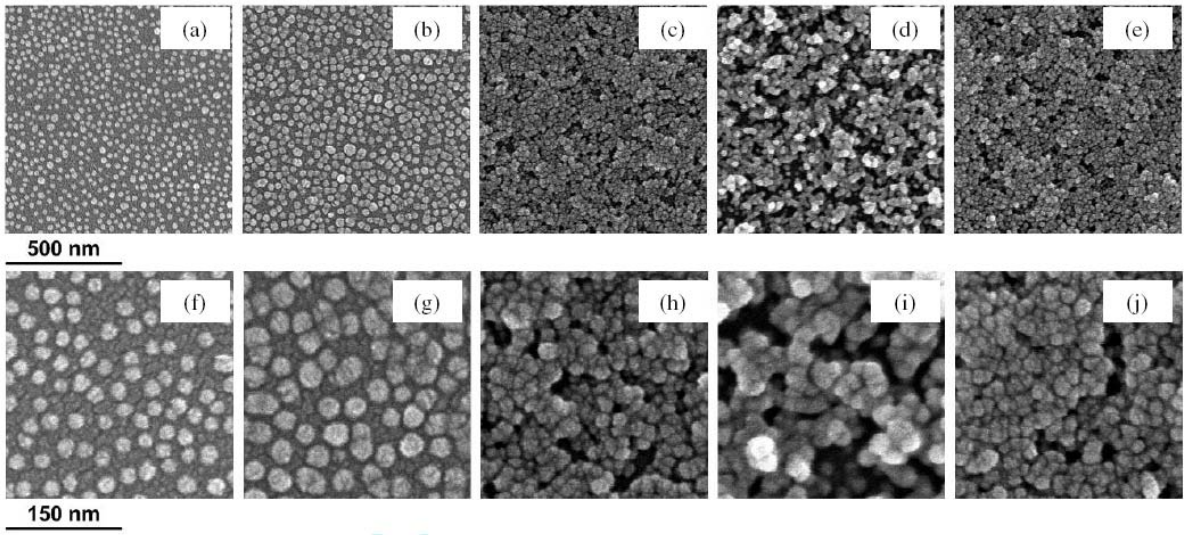


Fig. 2.3 SEM images of (a)-(e) 50k magnification and (f)-(j) 150k magnifications. (a) (f) Au NPs / SiO_2 (Au NPs assembled on SiO_2 substrate), (b) (g) CdSe NPs / Au NPs / SiO_2, (c) (h) Au NPs CdSe NPs / Au NPs / SiO_2, (d) (i) CdSe NPs / Au NPs / CdSe NPs / Au NPs / SiO_2, and (e) (j) Au NPs / CdSe NPs / Au NPs / CdSe NPs / Au NPs / SiO_2. Note that for better resolution, 3 nm thickness of Pt was plated on each sample prior to SEM performing [14].

Fig. 2.4 The close photographs of SiO_2/Si wafer fragments of different level assembly process. (right 1) blank SiO_2/Si wafer fragment. (right 2) Au NPs on SiO_2/Si wafer fragment. (right 3) CdSe NPs + Au NPs on SiO_2/Si wafer fragment. (right 4) Au NPs + CdSe NPs + Au NPs on SiO_2/Si wafer fragment. (right 5) CdSe NPs + Au NPs + CdSe NPs + Au NPs on SiO_2/Si wafer fragment. (right 6) Au NPs + CdSe NPs + Au NPs + CdSe NPs + Au NPs on SiO_2/Si wafer fragment [14].

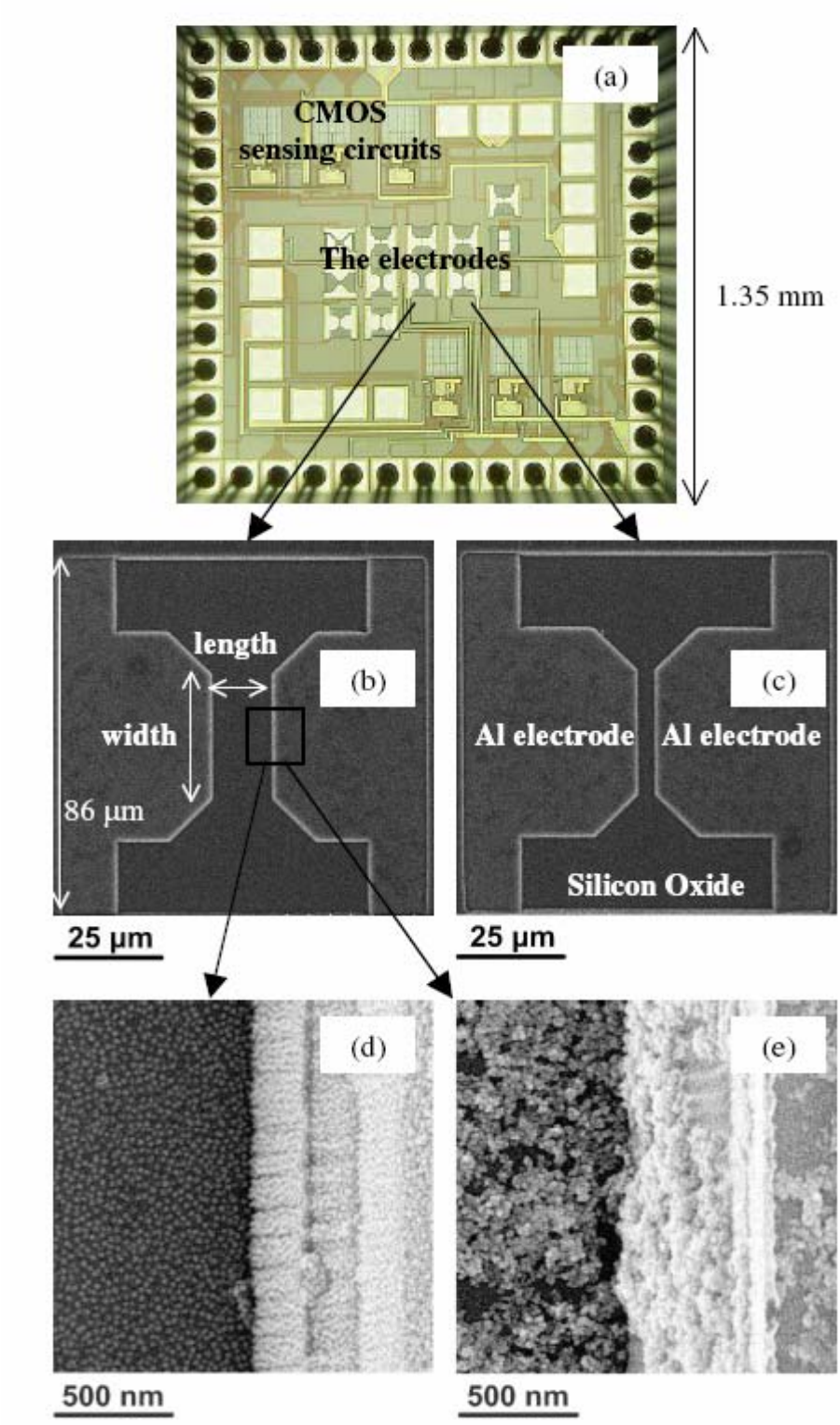


Fig. 2.5 The images of the electrodes at different stages. (a) Optical microscope image of the silicon chip. (b) (c) SEM images of the two types of electrodes of size 30 μm / 15 μm and 30 μm / 5 μm (width / length). (d) (e) The larger magnification of the edge part of the electrodes after fabrication of a layer of Au NPs (Au NPs / SiO_2) and the 4-layered structure (CdSe NPs / Au NPs / CdSe NPs / Au NPs / SiO_2) [14].

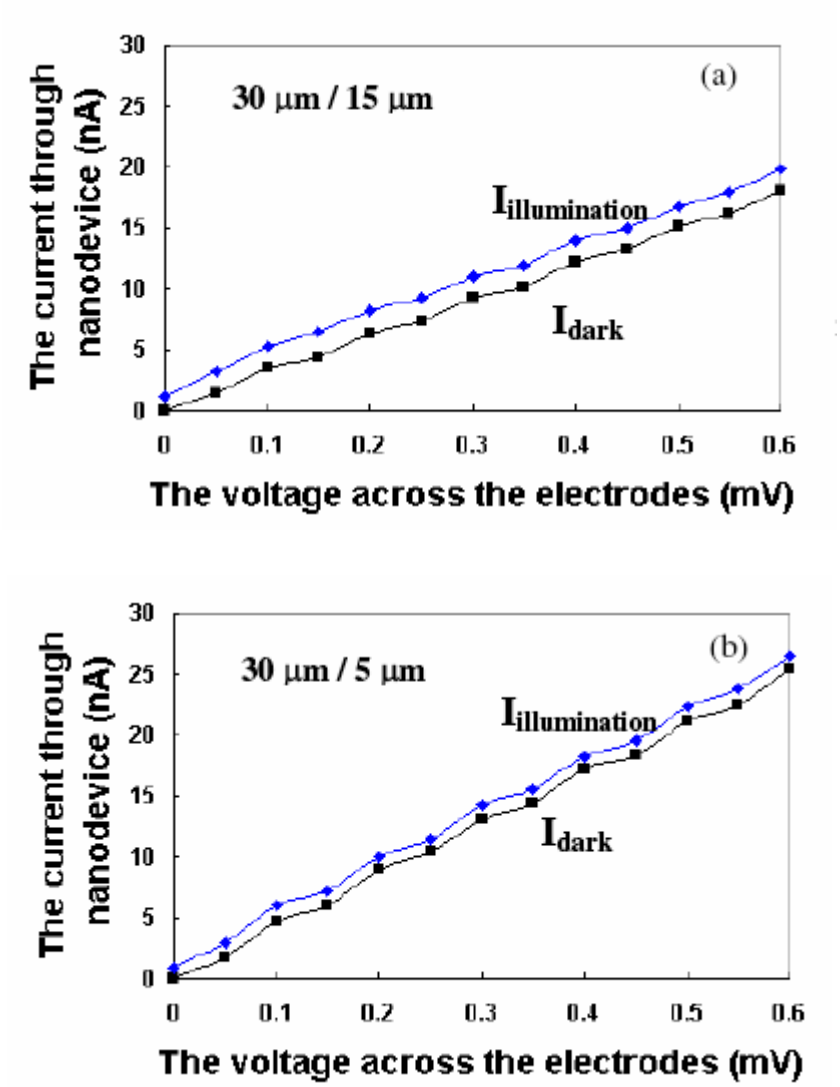


Fig. 2.6 The measurement results of the nanodevice with and without illumination. Two sets of electrodes (a) 30 μm / 15 μm and (b) 30 μm / 5 μm were investigated. I_{dark} means the current measured in the dark while $I_{illumination}$ represents the current measured under the illumination of 375 nm laser. (Average R = 1 / the slope of I-V curves) [14].

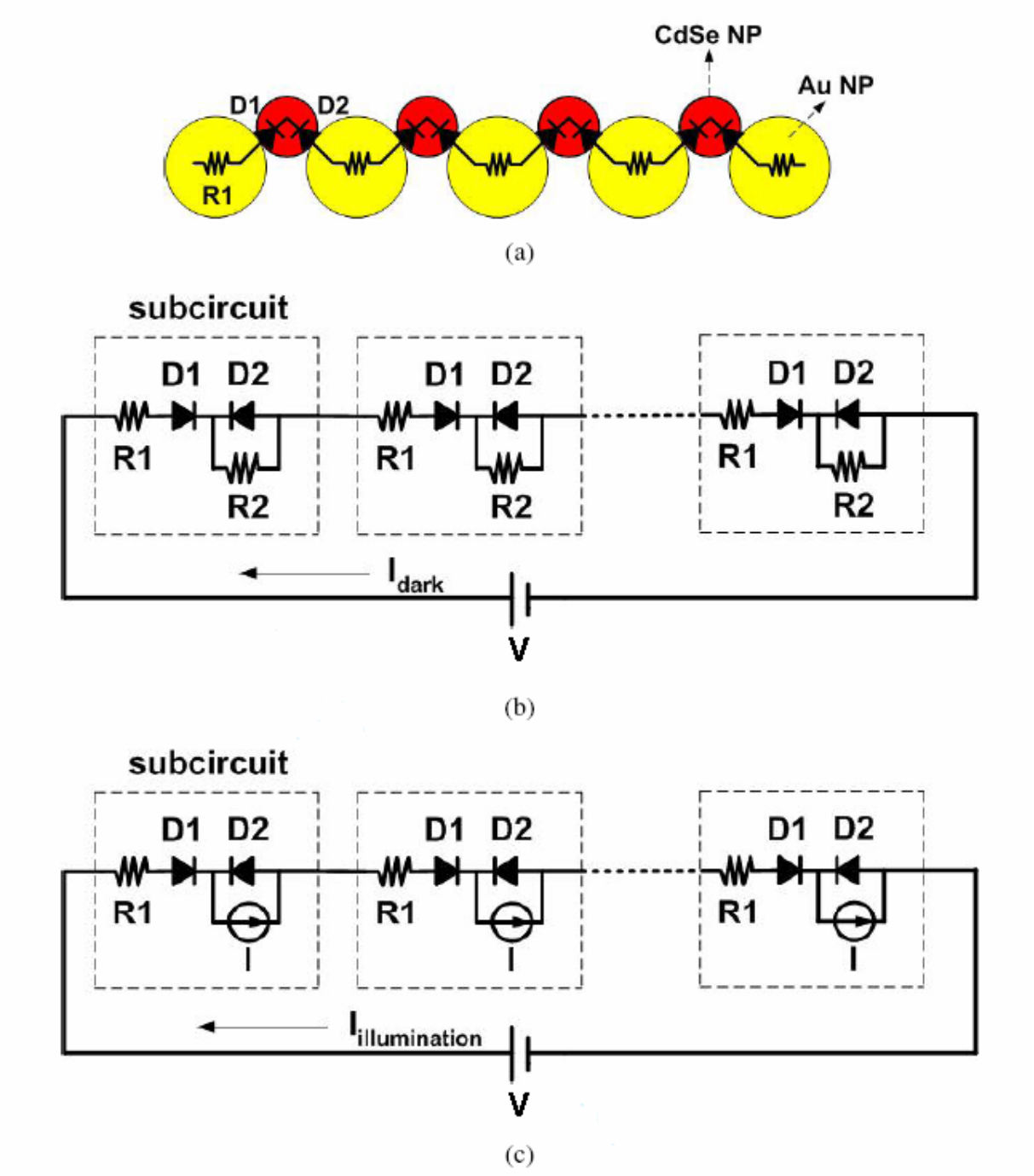


Fig. 2.7 (a) One-dimensional array of resistors and nano-Schottky-diodes, where D1 represents the forward-biased Schottky diode, D2 the reverse-biased Schottky diode and R1 the resistance of Au NP. (b) (c) The models for nanodevice in dark and under illumination. For HSPICE simulation, Fowler-Nordheim diode model was employed, V = 0.4 V, R1 = 1 MΩ, R2 = 5 MΩ and I = 5 pA [14].

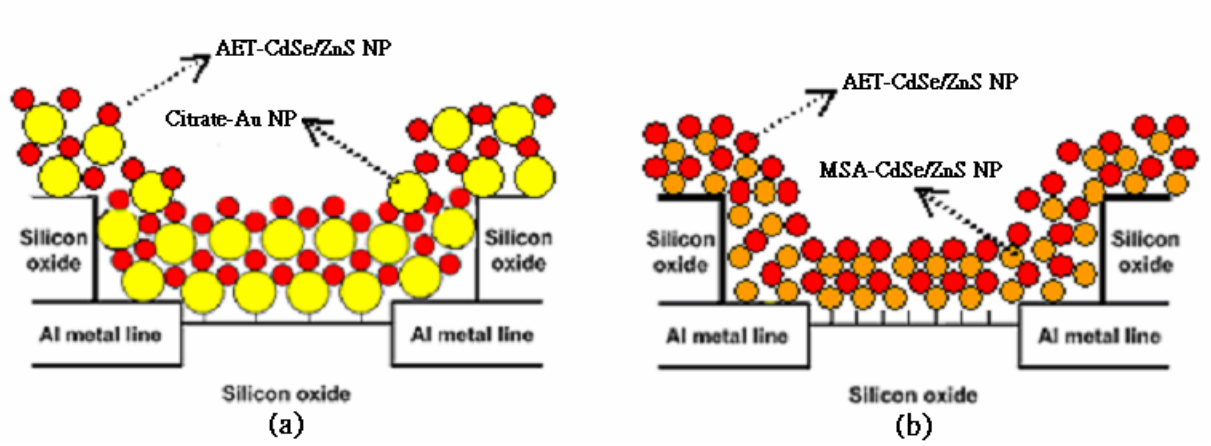


Fig. 2.8 The cross sectional figure of two kinds of photo-sensing nanodevices on CMOS sensing chip. (a) Au / AET-CdSe/ZnS nanodevice. (b) MSA-CdSe/ZnS / AET-CdSe/ZnS nanodevice.

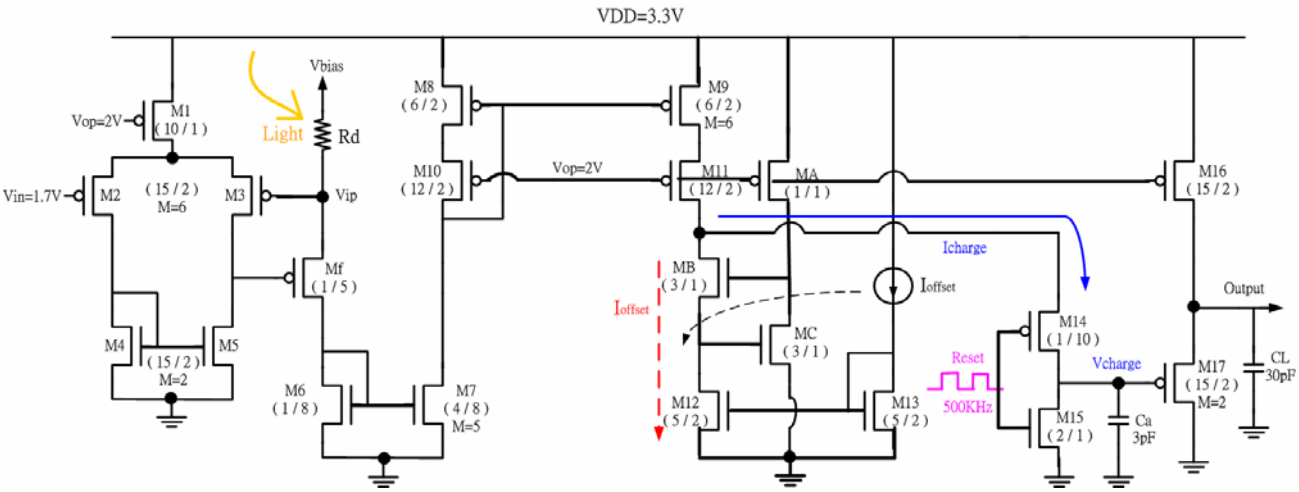
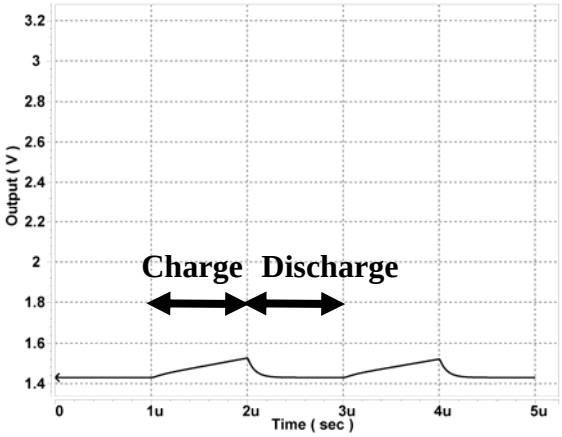


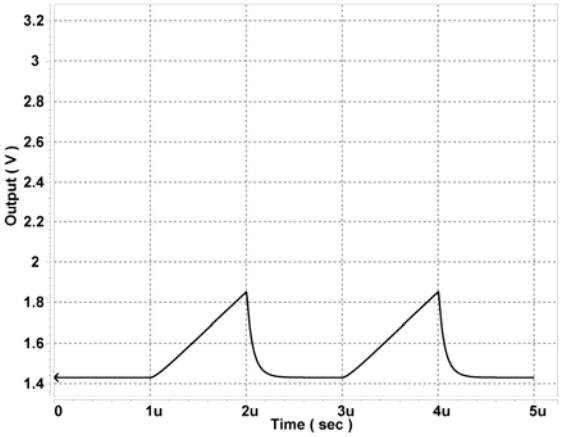
Fig. 2.9 The schematic of CMOS sensing circuit.

V_{dd}	3.3 V
V_{op}	2 V
V_{in}	1.7 V
V_{bias}	1.70118 V ~ 1.70196 V
I_{offset}	6 μA
Reset	Square wave, 3~0 V, 500 kHz
R_d	7.5 kΩ

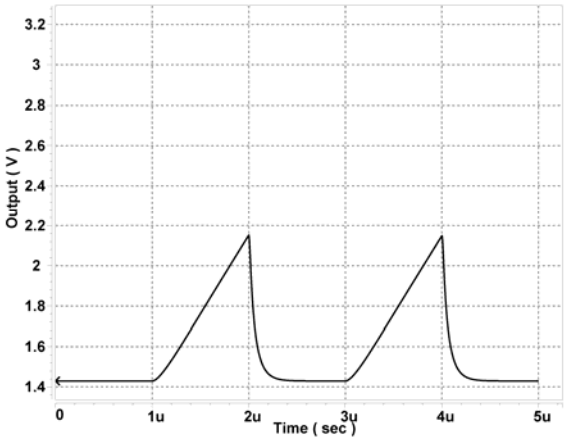
Table. 2.1 The voltage biases of CMOS sensing circuit for simulation results shown below.



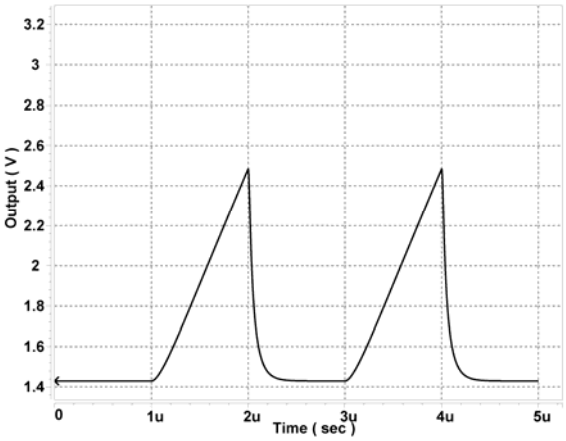
(a) V_{bias} = 1.70118 V, Id ~ 50 nA
Output = 1.526 V



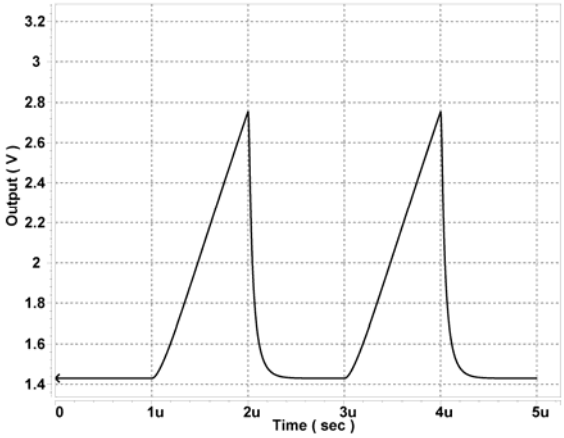
(b) V_{bias} = 1.70135 V, Id ~ 60 nA
Output = 1.851 V



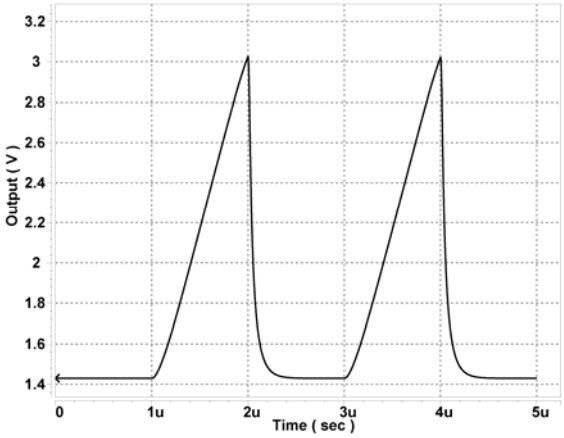
(c) V_{bias} = 1.70151 V, Id ~ 70 nA
Output = 2.152 V



(d) V_{bias} = 1.70167 V, Id ~ 80 nA
Output = 2.484 V



(e) V_{bias} = 1.70181 V, Id ~ 90 nA
Output = 2.753 V



(f) V_{bias} = 1.70196 V, Id ~ 100 nA
Output = 3.025 V

Fig. 2.10 The HSPICE simulation results of CMOS sensing circuit (a)~(f).

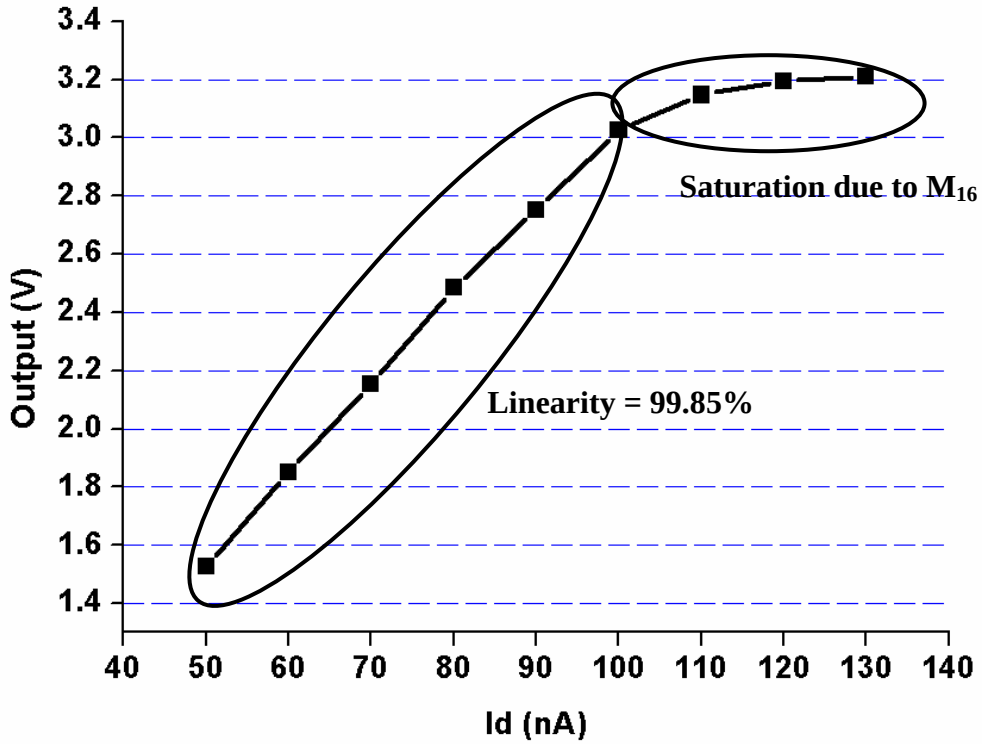


Fig. 2.11 The simulation result of Output versus I_d, the resistance value of photo-sensing nanodevice is fixed to 7.5 kΩ. The linearity is 99.85% when the I_d ranging from 50 nA to 100 nA. When the I_d is upon 100 nA, the output will gradually saturate because M_{16} will leave the saturation region, entering triode region.