CHAPTER 4

THE EXPERIMENTAL RESULTS AND DISCUSSIONS

4.1 THE ENVIRONMENT SETUP FOR MEASUREMENT

After fabrication, the silicon oxide substrate was observed and evaluated by using scanning electron microscopy (SEM) images at each stage of the procedure. The SEM was performed with JSM-6500F high-resolution scanning microscope. In addition to surface structure observation, the photo-sensing properties of the nanodevice were also verified by using laser diode as illumination light source. The environment setup for I-V characteristics measurement was shown in Fig. 4.1. The laser diode, laser diodes driver, optical measurement table and the clean room are all in ***Professor Eric Diau's Femtochemistry Laboratory***. The laser diode driver is PicoQuant POL 800D and the 375 nm, 400 nm, 435 nm laser diodes are PicoQuant LDH-P-C375, 400, 435. The current meter is Keithley 2410 1100V SourceMeter. The PCB on which the nanodevice-modified silicon chip was located was put in the vacuum chamber or normal room condition when measuring the I-V characteristics. During the measurement, the environment was kept in dark except the laser diode.

We also measured the UV-visible and Photoluminescence (PL) spectra to confirm the specific optical characteristics of the nanostructure. The measurement instruments are all in ***Professor Teng-Ming Chen's Phosphors Research Laboratory***. The UV-visible absorbance spectrum analysis was performed with Hitachi-U-3010 Spectrophotometer. The detecting wavelength was in the range of 190 nm to 1000 nm, and according the transmitted of sample, it's absorption spectra is monitored by Beer's Law. The typical experimental setup is shown in Fig. 4.2. A beam of light from a visible and/or UV light source (red colored) is separated into its component wavelengths by a prism or diffraction grating. Each monochromatic (single wavelength) beam in turn is split into two equal intensity beams by a half-mirrored device. One beam, the sample beam (colored magenta), passes

through a small transparent container (cuvette) containing a solution of the compound being studied in a transparent solvent. The other beam, the reference (colored blue), passes through an identical cuvette containing only the solvent. The intensities of these light beams are then measured by electronic detectors and compared. The intensity of the reference beam, which should have suffered little or no light absorption, is defined as $\mathbf{I_0}$. The intensity of the sample beam is defined as **I**. Over a short period of time, the spectrometer automatically scans all the component wavelengths in the manner described. The ultraviolet (UV) region scanned is normally from 200 to 400 nm, and the visible portion is from 400 to 800 nm. If the sample compound does not absorb light of a given wavelength, $\mathbf{I} = \mathbf{I_0}$. However, if the sample compound absorbs light then **I** is less than $\mathbf{I_0}$, and this difference may be plotted on a graph versus wavelength. Absorption may be presented as **transmittance** ($\mathbf{T} = \mathbf{I/I_0}$) or **absorbance** ($\mathbf{A} = \mathbf{log\ I_0/I}$). If no absorption has occurred, T = 1.0 and A = 0. Most spectrometers display absorbance on the vertical axis, and the commonly observed range is from 0 (100% transmittance) to 2 (1% transmittance).

The PL spectrometer analysis is performed with Jobin Yvon Instrument S. A. Inc. Spectrometer. The scanning range is from 200 nm to 1000 nm. The typical experimental setup for PL intensity spectrum measurement is shown in Fig. 4.3. When light of sufficient energy is incident on a material, photons are absorbed and excite the electrons from ground state. If radiative relaxation occurs, the emitted light is called photoluminescence (PL). This light can be collected and analyzed to yield a wealth of information about the photo-excitation nanostructure. In this experiment, we used laser source with different wavelengths to photo-activate the nanostructures. Subsequently, the emitted light was passing through a filter lens that can filter out the wavelengths < 500 nm, then analyzed by spectrometer and got into a photo-detector. Eventually, the PL signal data are recorded into computer.

4.2 SEM AND OPTICAL ABSORPTION / EMISSION SPECTRA

The overall layout figure of CMOS sensing chip is shown in Fig. 4.4. The most significant characteristic of the layout design is the electrodes structure combined with CMOS sensing circuits on the same silicon substrate. The electrodes structures are fabricated by opening a passivation window (86 μm * 86 μm) over two closely separated metal lines, as shown in Fig. 4.5. The electrodes are placed at the center part of the silicon chip for convenient nanodevice construction. The SEM image of the 13 electrodes and their sizes (width * length of oxide region between electrodes) are shown in Fig. 4.6. The electrodes, (1)-(8) are connected to the eight identical CMOS sensing circuits. The rest five electrodes, E1~E5 are connected directly to pads for direct measurement.

The SEM images of the surface of SiO_2/Si wafer fragments after repeated assembly process are shown in Fig. 4.7 (Au / AET-CdSe/ZnS nanostructure) and Fig. 4.8 (MSA-CdSe/ZnS / AET-CdSe/ZnS nanostructure). As we can see in the images, the structure become more and more compact when increases the number of layers step by step. Besides, for Au / AET-CdSe/ZnS nanostructure, after the multi-layered structure was formed, typically more than 3 layers, the gold color shining can be easily observed by naked eye. The fabrication process of the photo-sensing nanodevice on CMOS sensing chip is similar to that on SiO_2/Si wafer fragments, as described in section 3.3. First, the silicon chip is modified by N-[3-(trimethoxysilyl)propyl]-ethylene diamine (TMSPED), which provides positive-charged amino ($-NH_3^+$) groups to attract negative ($-COO^-$) charged Au or MSA-CdSe/ZnS NPs. Second, the AET-modified CdSe/ZnS NPs that have positive-charged amino groups on the particle surface are assembled on Au or MSA-CdSe/ZnS NPs. Theoretically, the assembly process can be repeated for several times to form multi-layered nanostructure of CdSe/ZnS and/or Au NPs. Third, fixing the nanodevice-modified silicon chip on PCB by using aqueous insulation gel. In this step, the quick-drying gel with organic solvent is not suitable. Fourth, bonding wire from silicon chip to PCB, and 125℃ heating process is extremely

harmful to nanodevice during bonding. Fifth, measurement of nanodevice which fixing on PCB and then illumination the silicon chip by 2.5mW / cm^2 laser diodes (375 nm, 400 nm, 435 nm) under vacuum or normal room condition. Finally, remove the silicon chip from PCB and then SEM observation of nanodevice structure. The overall experimental procedure of fabrication and measurement of the photo-sensing nanodevices on TSMC 0.35 μm silicon chip is shown in Fig 4.9. The fabrication process of the photo-sensing nanodevices on silicon oxide substrate of TSMC 0.35 μm silicon chip was also observed by SEM, as shown in Fig. 4.10 (blank electrodes), Fig 4.11 (Au / AET-CdSe/ZnS nanostructure) and Fig 4.12 (MSA-CdSe/ZnS / AET-CdSe/ZnS nanostructure). From the SEM images, Fig. 4.11 and Fig. 4.12, it is interesting to note that, in additional to the silicon oxide surface, the surface of Al electrodes was also labeled with NPs. This phenomenon may be caused by the presence of the –OH groups on the surface of the electrodes, which can be modified by TMSPED molecules, making them suitable sites for NP assembly. The presence of NPs on the Al electrodes enhances continuity at the interface between the NP's packed silicon oxide surface and the Al electrodes. Identically, it also enhances continuity at the interface between the NP's packed field oxide surface and the Al electrodes. Fig. 4.13(a) shows the cross section figure of the electrodes structure correspond to SEM image of the nanodevice-modified silicon chip. In theoretically, the NPs will be self-assembly covering the silicon chip. Although we cannot sure the edge between the Al electrodes and silicon oxide will be continuing self-assembly labeled with NPs firmly. In the worse case, we must consider the whole chip area (1460 μm * 1460 μm) for calculation, not the area of the electrodes. Fig. 4.13(b) shows the current flow trend of the nanodevice structure. Although it is very complicated for calculation, but we can sure that the electrodes dominated the source of the generated current.

Furthermore, in order to prove that the closely packed nanostructure has superior optical properties, we used quartz glass to simulate the silicon oxide substrate and observed the variation of UV-visible and Photoluminescence (PL) intensity spectra at different layer nanostructure. From the absorption spectrum, we can see the peak of absorbance rises when the number of layers increases,

as shown in Fig. 4.14. Besides, the nanostructure retains the optical characteristics of CdSe/ZnS NPs when they are bound to each other, which can be verified by identifying the characteristic absorbance peaks of Au NPs (~520 nm) and CdSe/ZnS NPs (~580 nm) in the spectrum. However, in some cases, we observed the peaks of Au NPs (~520 nm) and CdSe/ZnS NPs (~580 nm) are so close that they merge to form a board band in the spectrum for Au / AET-CdSe/ZnS nanostructure as shown in Fig. 4.14(a). Specifically, both the absorption onset and the band edge peak of the CdSe/ZnS NPs are unaffected as a result of their binding to the Au NPs. By comparing the UV-visible spectrum to the sizing curve reported by Peng and co-workers [26], we obtained that the diameter of CdSe/ZnS NPs is about 4 nm ~ 5 nm, which can also be proved by TEM images.

The PL intensity spectrum of multi-layered nanostructure on quartz glass was shown in Fig. 4.15. There are some important characteristics: First, the band edge peak of the PL intensity will increase in magnitude when the wavelength of incident light decreases (435 nm, 400 nm, 375 nm, 365 nm) [Fig. 4.15(a) and 4.15(c)]. It shows that more electron-hole-pairs are generated and return to the ground state under illumination with smaller excitation wavelength. Second, for both Au / AET-CdSe/ZnS and MSA-CdSe/ZnS / AET-CdSe/ZnS multi-layered structures, the PL intensity will also increase when the number of layers increases when we used 375 nm wavelength for optical excitation, as shown in Fig. 4.15 (b) and (d). It means that the nanostructure becomes more compact and has fewer defects on the particle surface. During the dip-and-wash procedure, the instable bond between the NPs will cause the existence of defect. So the probability of defect will be reduced when the number of layers increases. Third, as shown in Fig. 4.15(b), there is no absorption for Au NPs under optical excitation; therefore, there is no PL intensity with only a layer of Au NPs on quartz glass (Black Line). The PL intensity in 3-layered (5-layered) nanostructure is smaller than 2-layered (4-layered) nanostructure can also be proved. The Au NPs, which have no absorbance, block the incident light for CdSe/ZnS NPs to be photo-activated in the 3-layered (5-layered) structure. Fourth, we observed the PL intensity in 4-layered nanostructure become larger than 2-layered nanostructure. Specifically, they have the same structure that the CdSe/ZnS NPs was on

the top-layer. This result means that multi-layers constitute a more compact and fewer defects structure. The same, the 8-layered and 12-layered nanostructures show higher PL intensity than the 4-layered nanostructure. Nevertheless, although the ionic assembly using this dip-and-wash process can repeat as many times as we design to, the PL intensity increment will eventually be saturated.

4.3 Au / AET-CdSe/ZnS NANODEVICE

In this section, we measured the I-V characteristics of multi-layered Au / AET-CdSe/ZnS nanodevice structure. The two electrodes sets we used, 30 μm / 15 μm and 30 μm / 5 μm (width / length) were directly connected to the bonding pads around the chip. After the fabrication process described in Section 3.3, the I-V measurement was performed by applying voltage biases to the electrodes and measuring the current flowing through the nanodevice while in dark or under illumination of 375 nm, 400 nm, 435 nm laser diode. The SEM pictures of the electrodes are in Fig. 4.16. Electrodes 1 and 2 have silicon oxide region of 30 μm * 15 μm and 30 μm * 5 μm (width * length) respectively. The measurement results of the nanodevice with the two sets of electrodes are shown in Fig. 4.17. If there is only one layer of Au NPs labeling between electrodes, as shown in Fig. 4.11(a), the I-V characteristics were virtually identical to those of blank electrodes. The current less than 10 fA was observed throughout the applied voltages (-1mV ~ 1mV) with or without illumination. The relatively large spacing between the Au NPs prohibited the electrons from tunneling. However, for multi-layered Au / AET-CdSe/ZnS nanodevice, we found that the nanodevice was resistive in dark and produced an obvious constant increment of photocurrent under illumination. Simultaneously, it was seen that the I-V curve passes through the second quadrant and hence the nanodevice can deliver power.

In the previous work as described in section 2.2, for the 4-layered nanodevice composed of Citrate-capped Au NPs and Tyramine-capped CdSe NPs, there was constantly 1.2 nA (30 μm / 5 μm) and 2 nA (30 μm / 15 μm) increment of photocurrent throughout the applied voltage biases after 375

nm laser source illumination. In this present work, instead of using Tyramine-capped CdSe NP, we used AET-capped CdSe/ZnS NPs to construct the nanodevice. Basically the ZnS layer served as a passivation layer, which can make the particle structure stable. Besides the large band gap of ZnS contributed to higher quantum yield as we proposed in section 3.2. The measurement results of 4-layered nanodevice composed of Citrate-capped Au NPs and AET-capped CdSe/ZnS NPs show that there were constantly 28 nA (30 μm / 5 μm) and 70 nA (30 μm / 15 μm) increment of photocurrent throughout the applied voltage biases after 375 nm laser illumination. Even at zero bias point, this constant increment remained. So this confirms the higher performance by using AET-capped CdSe/ZnS NPs than Tyramine-capped CdSe NPs. Furthermore, for the measurement result of 12-layered nanodevice, there was constantly 56 nA (30 μm / 5 μm) and 121 nA (30 μm / 15 μm) increment of photocurrent throughout the applied voltage biases after illumination with 375 nm laser, and it had average R = 1.44 kΩ, V_{oc} = -0.099mV (30 μm / 5 μm) and average R = 2.23 kΩ, V_{oc} = -0.285mV (30 μm / 15 μm). There was more photocurrent generated as we used the electrodes of larger length, because there were more nano-Schottky-diodes formed in the multi-layered structure between the electrodes. As we know that in previous work, the photocurrent volume density (PVD) (A/nm^3) of the nanodevice composed of Citrated-capped Au NPs and Tyramine-capped CdSe NPs, 4-layered nanodevice, is at least 38 times better than that of CdSe thin film [22]. In this work, we also compared the PVD of the Au / AET-CdSe/ZnS nanodevice with that of the CdSe thin film once more. We found that the PVD of the 4-layered nanodevice and 12-layered nanodevice composed of Au and AET-CdSe/ZnS NPs is at least 1183 and 682 times better than that of CdSe thin film, respectively. In sum, short-circuit current (I_{sc}), open-circuit voltage (V_{oc}), and PVD ratio of the 4, 8, 12-layered nanodevice structures under 375, 400, 435 nm wavelength illumination were shown in Table 4.1.

In conclusion, there are several notable characteristics of the results in Fig. 4.17 and Table 4.1. First, the longer length of the electrodes leads to the larger photocurrent and larger V_{oc} after illumination, because there was more nano-Schottky-diodes formed in the structure and the length of

the electrodes depends on the equivalent resistance, therefore dominating the $V_{oc.}$ We obtained the same phenomenon as we used HSPICE to simulate two-dimension "nano-schottky-diode" arrays model. The simulation condition is similar to the one-dimension diode-resistor arrays model described in section 2.2, except the resistance R1 changed to 0.25MΩ and one-dimensional diode-resistor array changed to two-dimensional one, as shown in Fig. 4.18. To simulate the nanodevice structure with long (short) length, 45 (15) stages were connected in series. The simulation results are shown in Table. 4.2, and we can observe the data just match the measurement results that the larger length of the electrodes (45 stages) leads to the larger photocurrent. Second, more photocurrent generated in shorter wavelength illumination because more electron-hole-pairs generated within the depletion region with uniform photoexcitation ($hv > E_g$). This result just matches the UV-visible and PL intensity spectra as shown in Fig. 4.14 and Fig. 4.15, respectively. Third, more photocurrent was generated in the nanostructure which has a larger number of layers. Fourth, from the Table 4.1, we found that the PVD ratio will gradually decrease when the number of layers increases. The PVD ratio means the PVD of the nanodevice compared with the CdSe thin film [22]. Theoretically, the photocurrent is proportioned to the PL intensity of the nanostructure; therefore, the photocurrent per unit volume (PVD) is proportional to the PL intensity per unit volume. From the PL intensity spectrum in the multi-layered Au / AET-CdSe/ZnS nanostructure, we found that the PL intensity did not increase as fast as the volume did; therefore we can confirm that the PVD ratio will decrease when the number of layers, that is the volume, increases. This phenomenon can also be observed from the HSPICE simulation results. Physically, when the number of layers increased, more nano-Schottky-diodes were formed and therefore more photocurrent was generated. However, the increase of photocurrent does not mean that the "efficiency" will also increase proportionally, because the more layers the nanostructure has, the more nano-Shottky-diodes are blocked from photo-excitation by the Au NPs in the upper layers.

4.4 MSA-CdSe/ZnS / AET-CdSe/ZnS NANODEVICE

For the MSA-CdSe/ZnS / AET-CdSe/ZnS nanodevice with only a layer of MSA-CdSe/ZnS NPs on the silicon oxide substrate [Fig. 4.12(a)], the I-V characteristics was large resistive about 20GΩ (30 μm / 5 μm) and 60GΩ (30 μm / 15 μm) in dark and the photocurrent was less than 20 pA with 375 nm illumination. The measurement results of multi-layered nanodevice composed of MSA-CdSe/ZnS and AET-CdSe/ZnS NPs are shown in Fig. 4.19. For 12-layered nanodevice, there were 2.2 nA (30 μm / 5 μm) and 3.1 nA (30 μm / 15 μm) increment of photocurrent at zero bias (short-circuit current I_{sc}) after 375 nm illumination. In dark condition, the I-V characteristics was resistive about 0.88 GΩ (30 μm / 5 μm) and 0.99GΩ (30 μm / 15 μm). Although the electric resistance is not linearly proportional to the length of the electrodes (maybe due to the defects between CdSe/ZnS NPs), but we can make sure that the larger length of electrodes leads to the larger electric resistance in dark condition. Based on the results presented in Fig. 4.19, we can concluded that the nanodevice composed of only CdSe/ZnS NPs acts like a photoresistor whose resistance decreases with increasing incident light intensity. As described in literature, a photoresistor is made of a high-resistance semiconductor. If light illuminated on the device is of high enough frequency, photons absorbed by the semiconductor give bound electrons enough energy to jump into the conduction band. The resulting free electron (and its hole partner) conduct electricity, thereby lowering resistance. The only difference between the CdSe/ZnS nanodevice and conventional photoresistor is that the resistance decreased with decreasing incident light wavelength. In other words, shorter incident light wavelength caused more PL intensity as shown in Fig. 4.15(c). We also measured the different layered MSA-CdSe/ZnS / AET-CdSe/ZnS nanodevices with or without illumination, and the measurement results are shown in Table 4.3. At last, we found that the PVD of the 12-layered MSA-CdSe/ZnS / AET-CdSe/ZnS nanodevice is at least 34 times better than that of CdSe thin film [22].

In conclusion, there are several notable characteristics of the results in Fig. 4.19, and Table 4.3.

First, unlike the I-V measurement results of the nanodevice composed of Au / AET-CdSe/ZnS NPs in which the conductivity remained constant with or without illumination, the conductivity of the nanodevice composed of MSA-CdSe/ZnS / AET-CdSe/ZnS NPs increased under illumination. In the Au / AET-CdSe/ZnS nanodevice, there are enormous number of nano-Schottky-diodes in the structure which can absorb the illuminated light, generate electron-hole pairs in the depletion region and thus produce the photocurrent without changing the conductivity. In contrast, in MSA-CdSe/ZnS / AET-CdSe/ZnS nanodevice, there is no diode structure, only the same semiconductor material, CdSe/ZnS. When illuminated with light, the nanodevice can generate electron-hole-pairs, which in turn increase the conductivity. However, without the depletion region, the nanodevice can hardly produce photocurrent at zero bias. Therefore, we can conclude that ***the Au / AET-CdSe/ZnS nanodevice acts like a photodiode while the MSA-CdSe/ZnS / AET-CdSe/ZnS nanodevice acts like a photoresistor.*** Second, the longer length of electrodes leads to smaller electric resistance after illumination, which can be easily understood that the longer length the electrodes has, the more electron-hole-pairs generated after illumination. Third, from the Table 4.3, we found that the PVD ratio will increase when the number of layers increases. From the PL intensity spectra in the multi-layered MSA-CdSe/ZnS / AET-CdSe/ZnS nanostructure, we found that the growth rate of the PL intensity was larger than the growth rate of the volume; therefore we can confirm that the PVD ratio will increase when the number of layers increases.

4.5 Au / AET-CdSe/ZnS SOLOR CELL EFFICIENCY

Solar cell is a critical technology for overcoming global environmental and energy problems. The invention of p-n junction in 1949 formed the basis of the discovery of the crystalline Si solar cell by Pearson in 1954. Since then, solar cells have been developed and produced with polysilicon, CdTe, and GaAs. Applications of solar cells are now an important and integral part of our daily lives, ranging from calculators to solar powered irrigation systems. Over 95% of solar cells in production

are silicon based. In our works, the nanodevice composed of Au and AET-CdSe/ZnS NPs has ultra-high performance of photo-sensing ability, as described in section 4.3. In order to show that the proposed nanodevice structure composed of NPs has a similar or even better photo-sensing ability than conventional solar cells, we calculate the power conversion efficiency and compare it with other solar cell structures. In the measurement results, we obtained the highest output power occurred in 8-layered nanodevice. The I-V characteristics of a solar cell were shown in Fig. 4.20. V_{oc} is the maximum voltage obtainable at the load under open-circuit condition of the nanodevice, and I_{sc} is the maximum current through the load under short-circuit condition. The power delivered by the nanodevice can be maximized by maximizing the area under the curve in Fig. 4.20, that is, maximizing the product (I_{sc} * V_{oc}). By properly choosing the load resistor, the output power can be as high as (I_m * V_m) = 0.8 * (I_{sc} * V_{oc}) in typical p-n junction solar cell. In our system, the output power can be as high as (I_m * V_m) = 0.5 * (I_{sc} * V_{oc}). If we focus on 8-layered nanodevice which under 375 nm illumination, and then obtained the V_{oc} ≈ -0.2mV (30 μm / 5 μm) and V_{oc} ≈ -0.6mV (30 μm / 15 μm). From the result we can know that the V_{oc} depended on the length of the electrodes and approximated to direct proportion to the length of the electrodes. As we know that the power efficiency is defined as J_{sc}(mA / cm^2) * V_{oc} / P_{in}(mW / cm^2), so we must correct V_{oc} when the electrodes area become more larger by extend the length of the electrodes. First, we set the length of the electrodes as an variable X, so the cell area was [2000 + 80X] μm^2, and the image of the electrodes of size 30 μm / X μm (width / length) is shown in Fig. 4.21. The cell area was 2400 μm^2 (length X = 5 μm), and the short-circuit current I_{sc} = 40 nA as we measured. When the cell area is similar to 1cm^2, the length of the electrodes X = 1250,000 μm, and the J_{sc} = 40 nA / (1460 μm * 1460 μm) = 1.877*10^{-3} (mA / cm^2). However, the V_{oc} (X = 1250,000 μm) = -0.2mV (X = 5 μm) • 1250,000 / 5 = -50V. So the power efficiency = 0.5 • 1.877*10^{-3}mA • 50V / 2.5mW = 1.89%. We also obtained the power efficiency can achieve 40% (X = 26625,000 μm) which larger than other solar cell structures before a 2005 technology overview [18]. Although such estimate method is not very accurate, because we can not make sure that such photocurrent can be generated when the

length of the electrodes become more large. In our future works, the nanodevice with large area electrodes will be designed and fabricated to verify our ideal inference.

4.6 THE PHOTO-SENSING CIRCUIT

The measurement results of 4-layered, 30 μm * 5 μm electrodes, Au / AET-CdSe/ZnS nanodevice combined with CMOS sensing circuit was shown in Fig. 4.22. The measurement condition for measuring was shown in Table 4.4. The equivalent resistance of the nanodevice R_d is about 7.5 kΩ. We fixed the V_{bias} ~ 1.70118 V to make the dark current was first set closely to 50 nA in both HSPICE simulation and this measurement, consequently, illuminated with different wavelengths (375, 400, 435 nm) of a 2.5mW / cm^2 laser source. The result of output versus I_d in both HSPICE simulation and this measurement is also shown in Fig. 4.23. There are some notable characteristics of the result. First, the value of V_{ip} is very close to V_{in} = 1.7 V, which means the gain of negative feedback loop is large enough to lock V_{ip} with V_{in}. Second, the conductivity of the nanodevice is not increasing after light illumination, but the current flowing the nanodevice, $I_{d,}$ is increasing after light illumination. This phenomenon means the large number of reverse-biased Schottky diodes that had forward photovoltaic voltages to effectively increase the bias voltage across the nanodevice after light illumination and thus increase the current flowing the nanodevice.

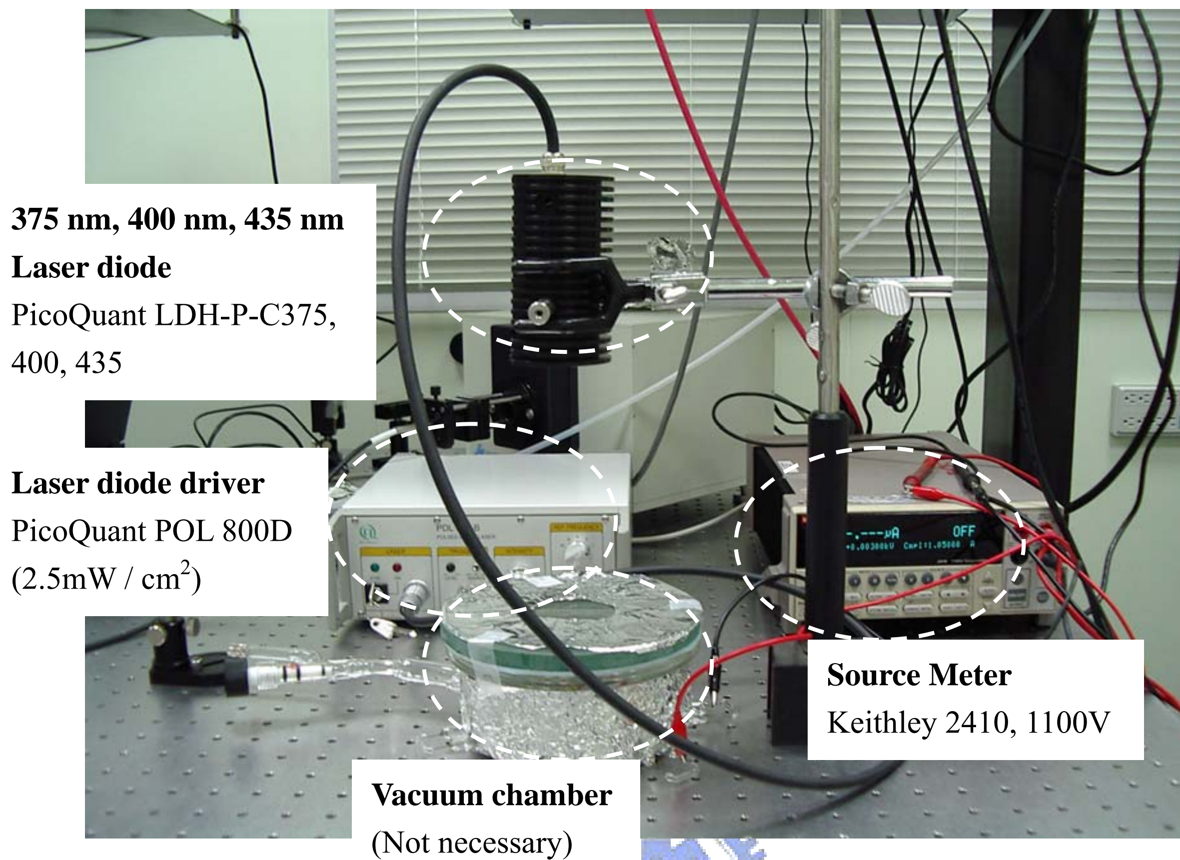


Fig. 4.1 The environment setup for I-V characteristics measurement.

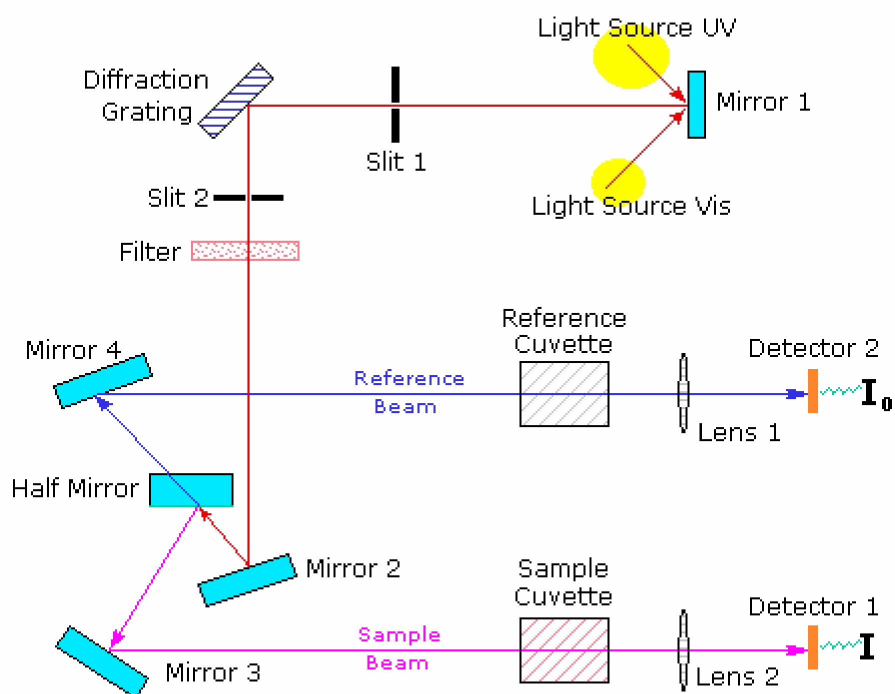


Fig. 4.2 The environment setup for UV-visible absorbance spectrum measurement.

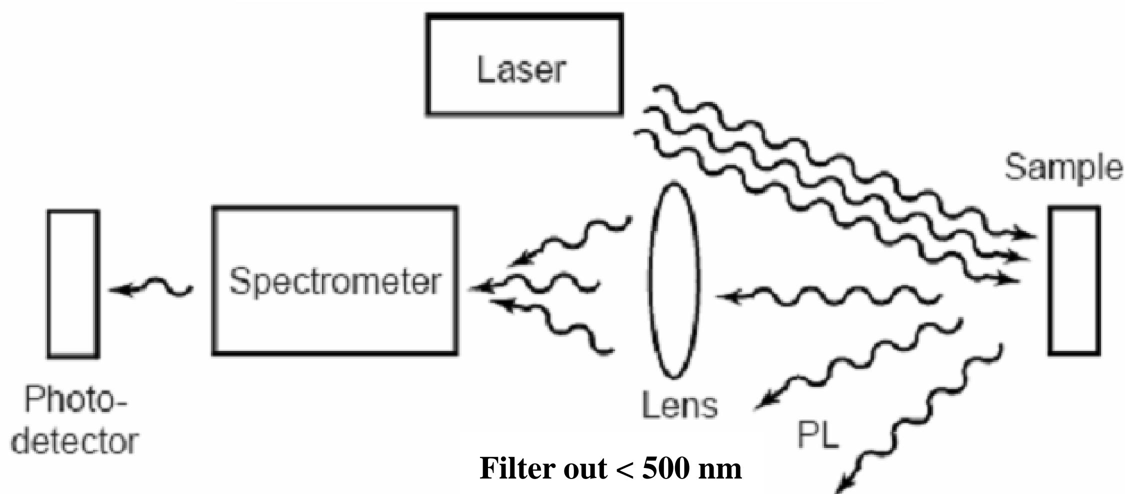


Fig. 4.3 The environment setup for PL intensity spectrum measurement.

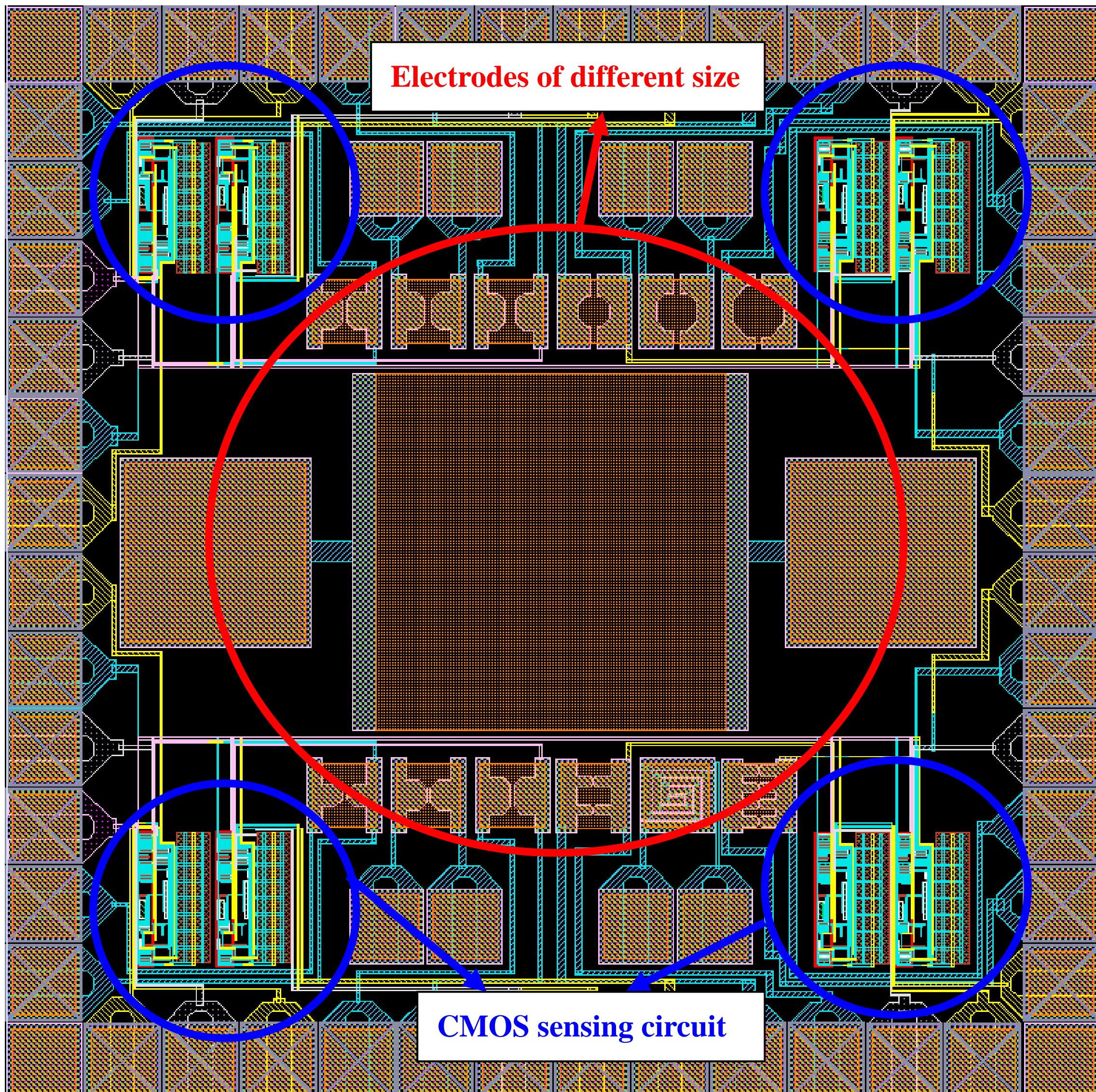


Fig. 4.4 The layout of the CMOS sensing chip. The chip is 1460 μm * 1460 μm and has 48 pins. There are eight identical CMOS sensing circuits at the corner part of the chip, and thirteen different size/shape electrodes at the center part of the chip.

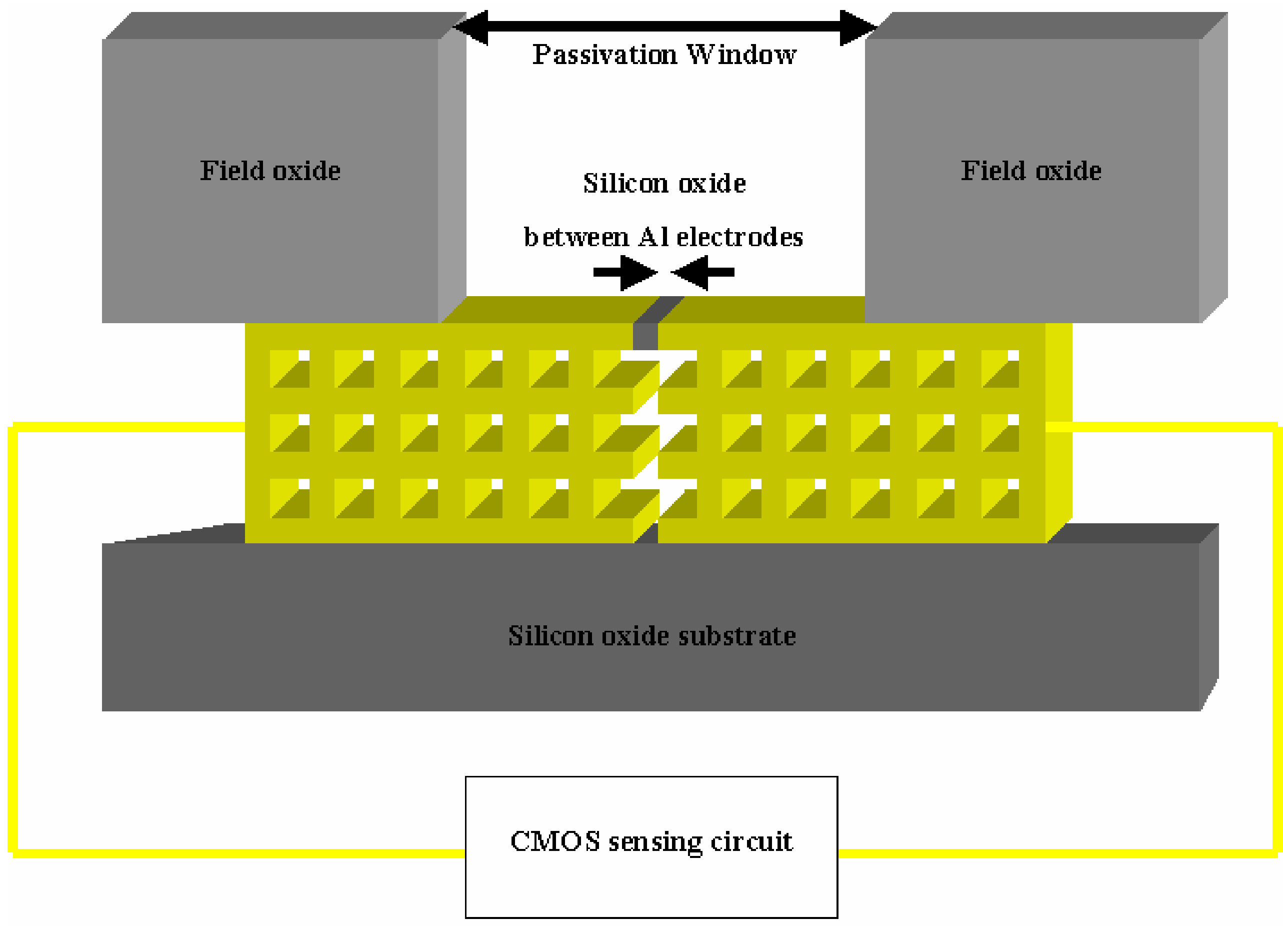
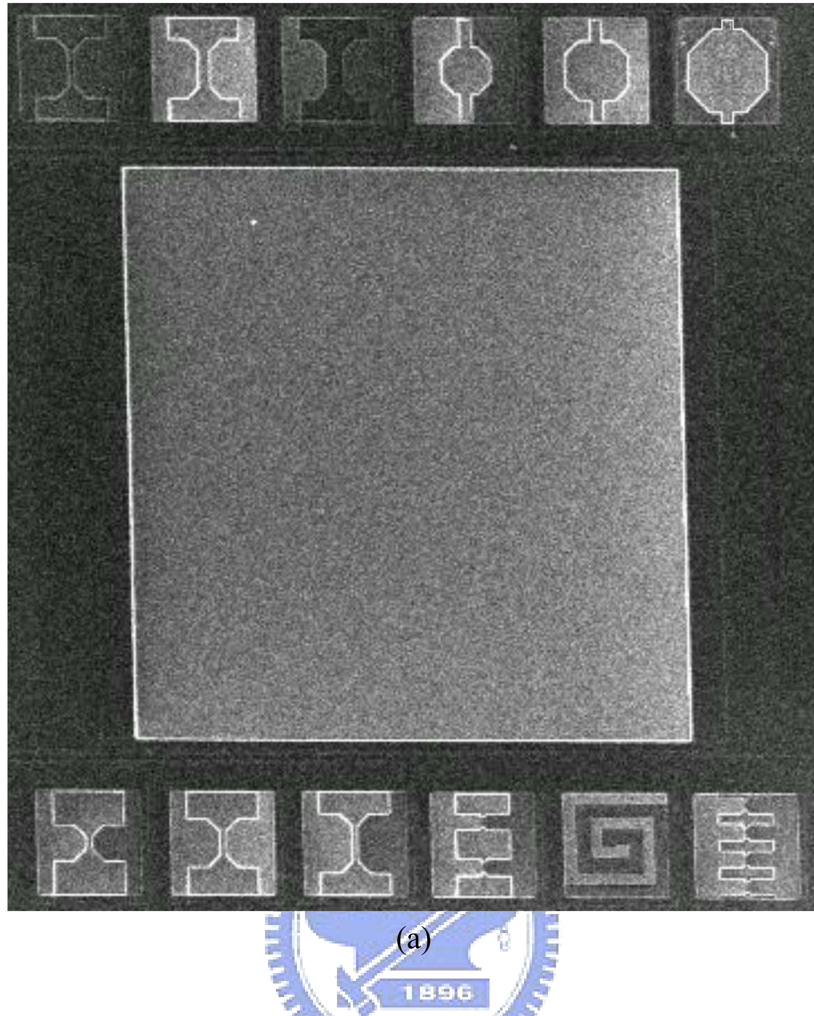


Fig. 4.5 The cross section figure of electrodes structure, where the four layers of metal lines (~ 6 μm thickness) are connected by vias. The passivation window in this work is 86 μm * 86 μm. The silicon oxide region between Al electrodes has different shapes.

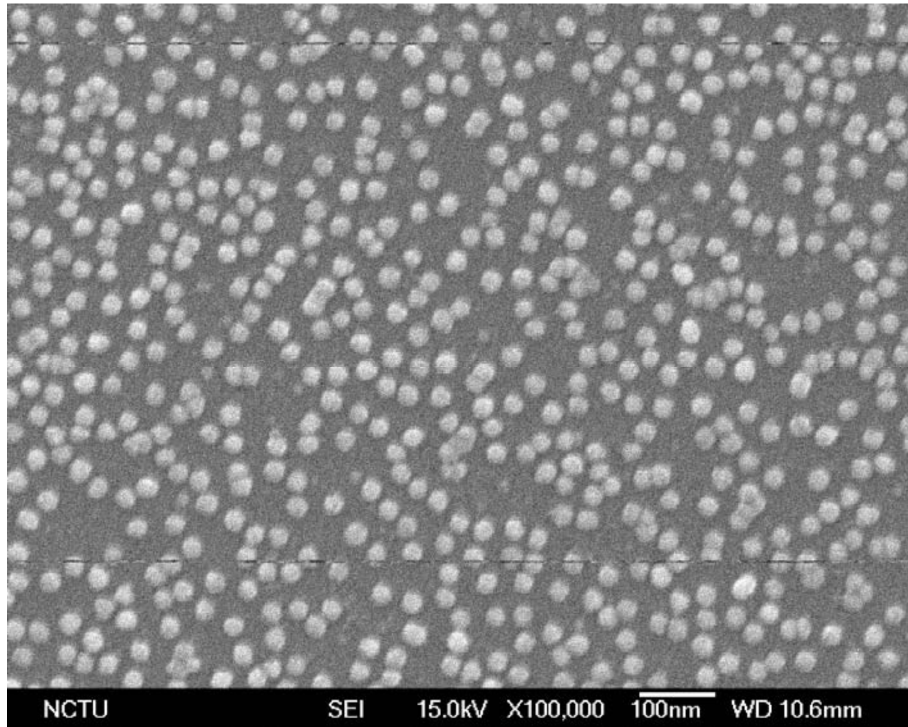


(a)

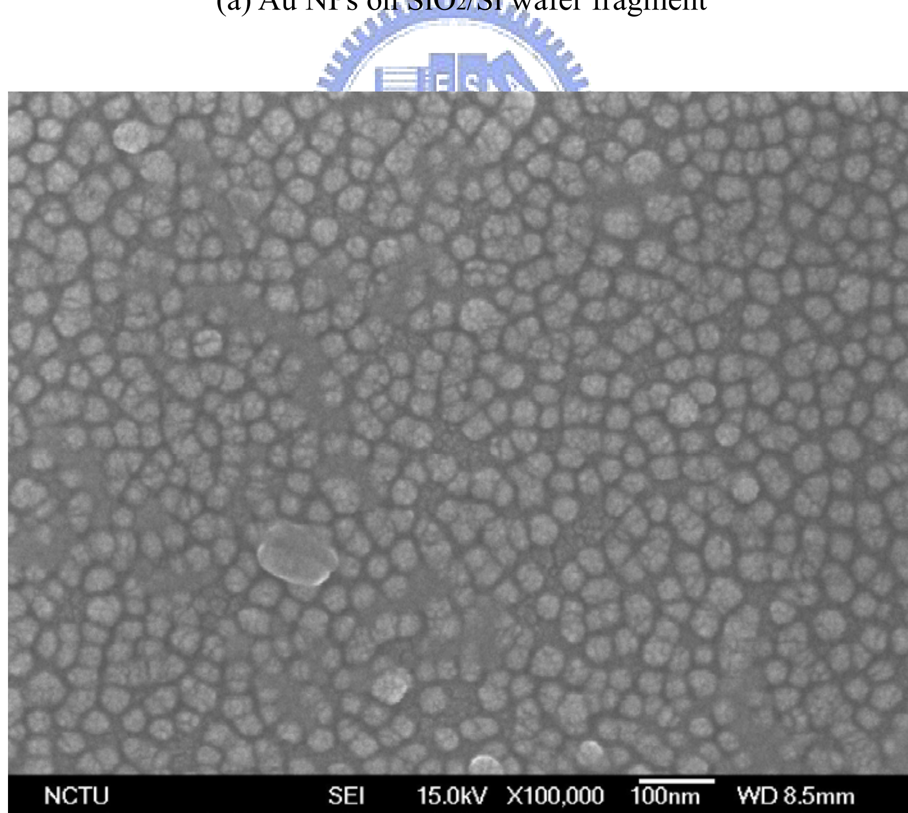
(1)=30um*5um	E1=30um*10um	(2)=30um*15um	(3)=21um diameter	E2=27um diameter	(4)=35um diameter
			E5=500um*500um		
(5)=10um*5um	E3=20um*5um	(6)=30um*5um	(7)=8um*1um, M=2	E4=285um*1um	(8)=8um*1um, M=4

(b)

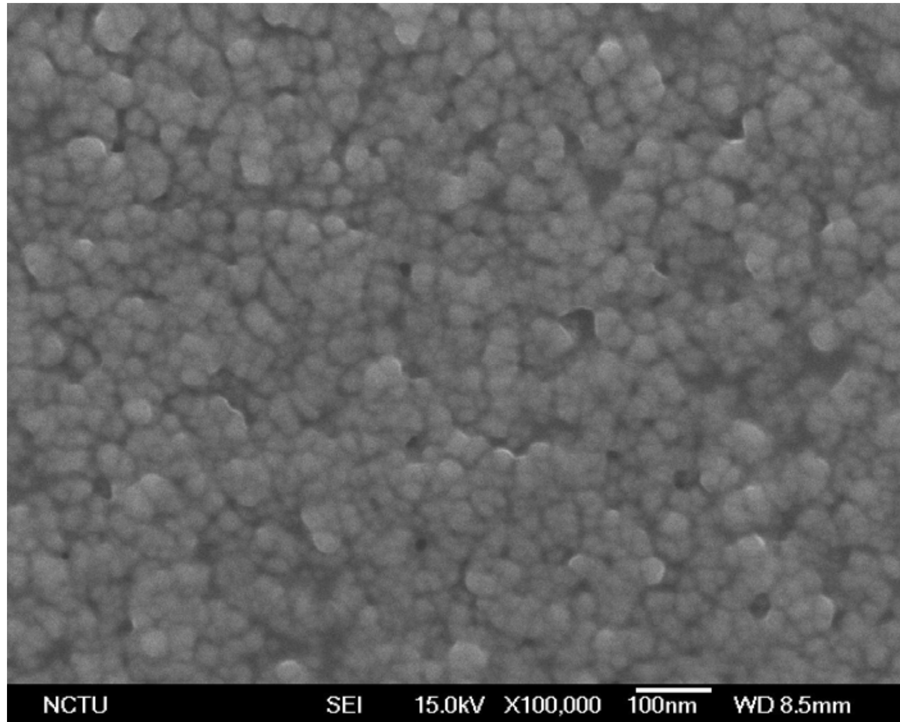
Fig. 4.6 (a) The SEM image of the 13 electrodes. (b) The size (width * length between electrodes) figure of the corresponding 13 electrodes. The electrodes, (1)~(8), are connected to the eight identical CMOS sensing circuits. The rest five electrodes, E1~E5 are connected directly to pads for direct measurement.



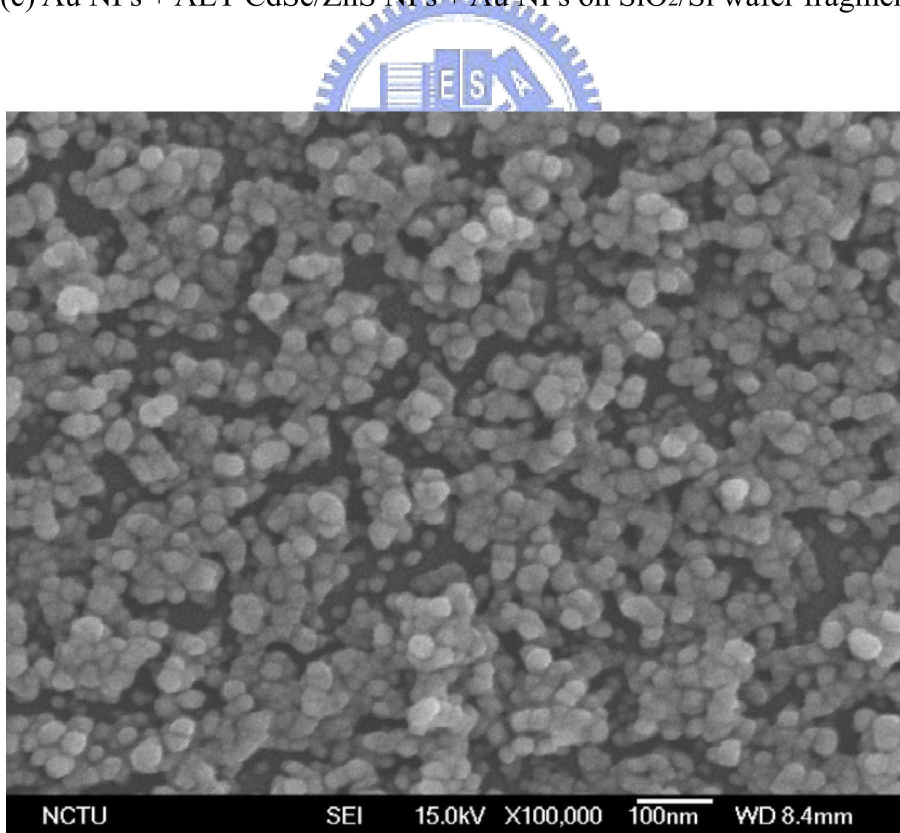
(a) Au NPs on SiO_2/Si wafer fragment



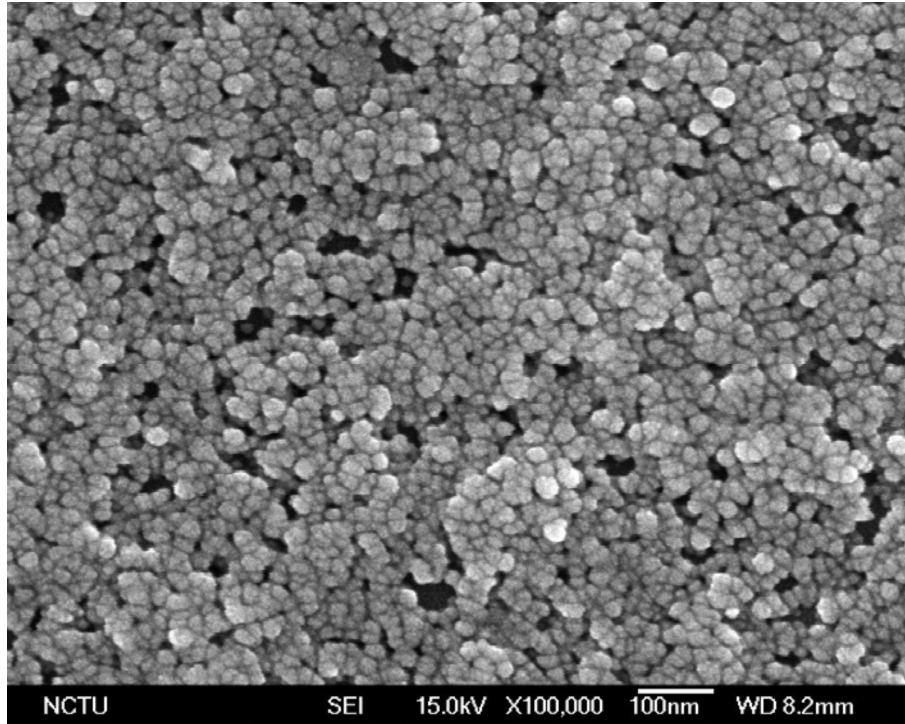
(b) AET-CdSe/ZnS NPs + Au NPs on SiO_2/Si wafer fragment



(c) Au NPs + AET-CdSe/ZnS NPs + Au NPs on SiO_2/Si wafer fragment

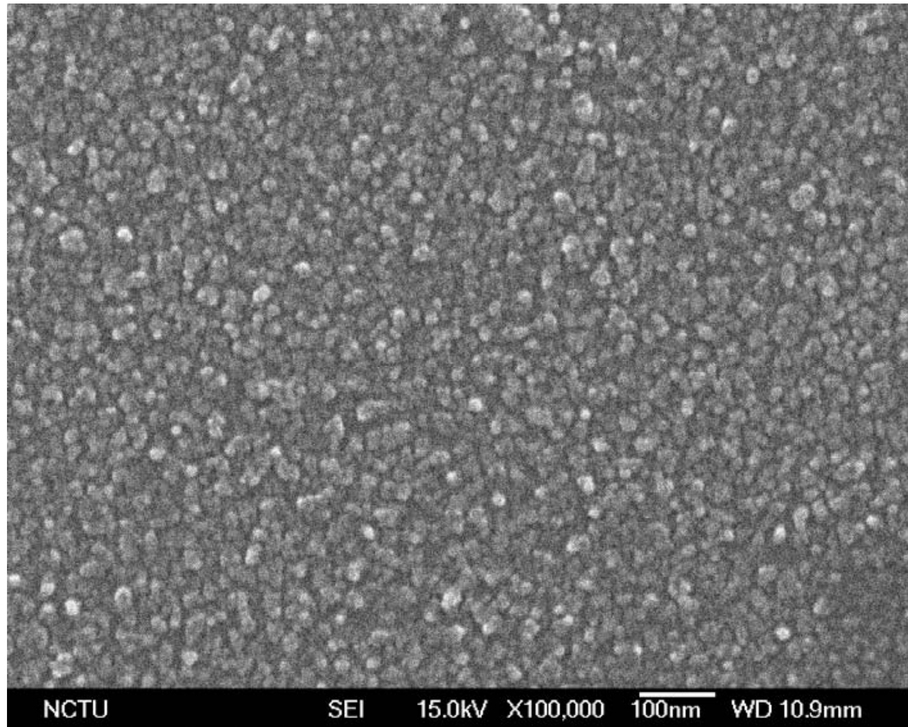


(d) AET-CdSe/ZnS NPs + Au NPs + AET-CdSe/ZnS NPs + Au NPs on SiO_2/Si wafer fragment

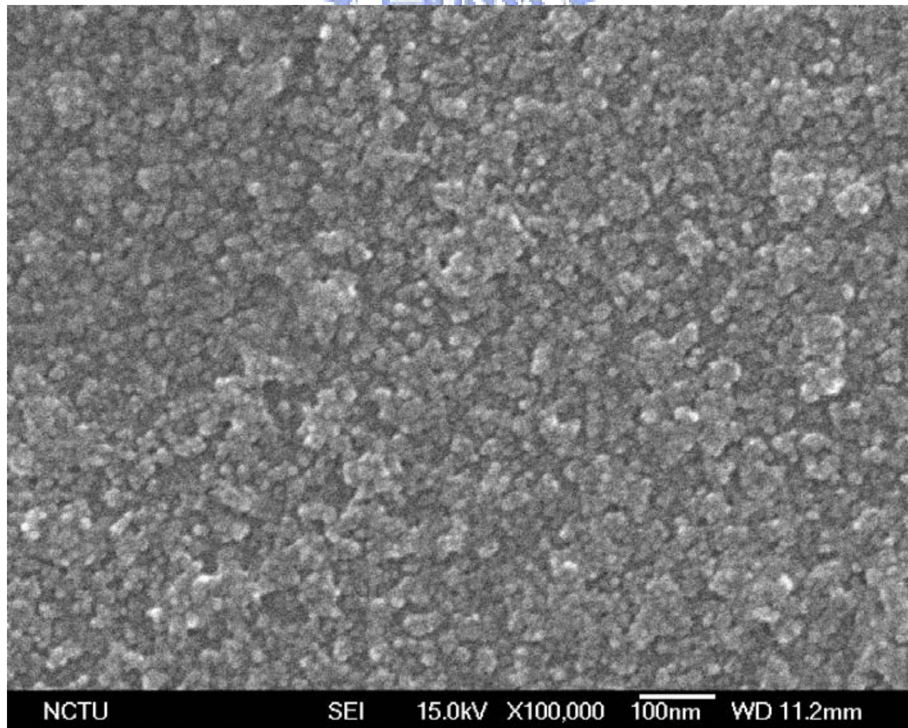


(e) Au NPs + AET-CdSe/ZnS NPs + Au NPs + AET-CdSe/ZnS NPs + Au NPs on SiO_2/Si wafer fragment

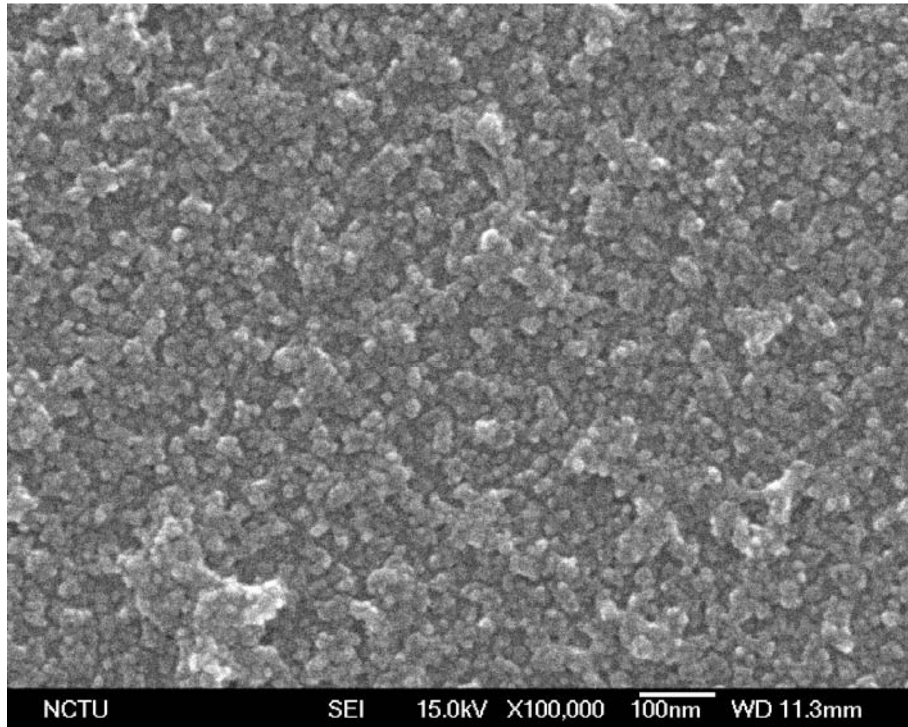
Fig. 4.7 The SEM images (100k magnification) of Au / AET-CdSe/ZnS nanostructure of different level construction are shown above (a)~(e).



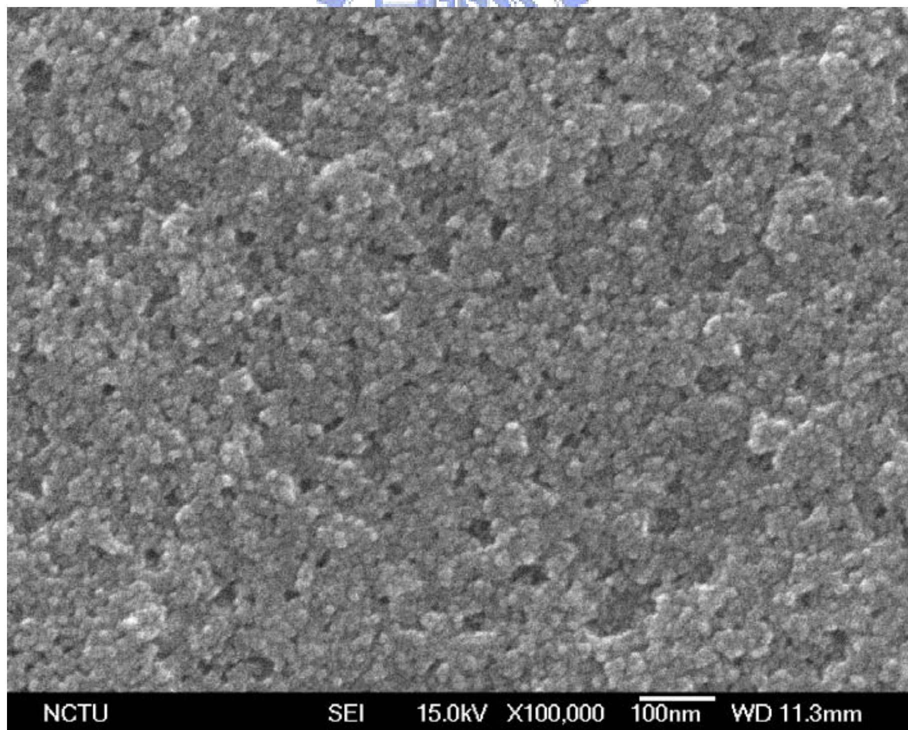
(a) MSA-CdSe/ZnS NPs on SiO_2/Si wafer fragment



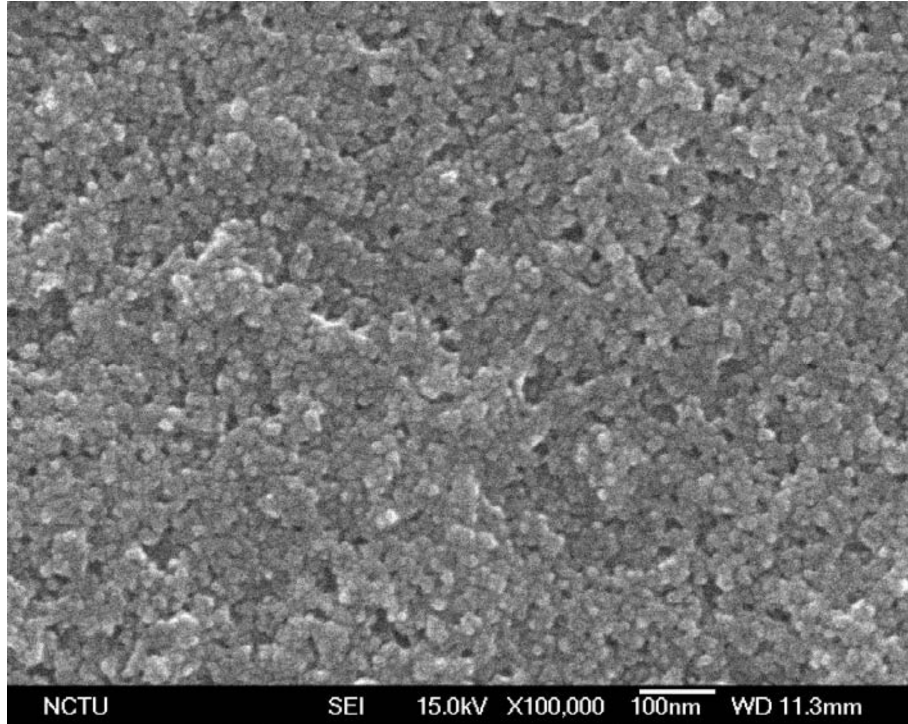
(b) AET-CdSe/ZnS NPs + MSA-CdSe/ZnS NPs on SiO_2/Si wafer fragment



(c) MSA-CdSe/ZnS + AET-CdSe/ZnS NPs + MSA-CdSe/ZnS NPs on SiO_2/Si wafer fragment



(d) AET-CdSe/ZnS NPs + MSA-CdSe/ZnS + AET-CdSe/ZnS NPs + MSA-CdSe/ZnS NPs on SiO_2/Si wafer fragment



(e) MSA-CdSe/ZnS + AET-CdSe/ZnS NPs + MSA-CdSe/ZnS + AET-CdSe/ZnS NPs + MSA-CdSe/ZnS NPs on SiO_2/Si wafer fragment

Fig. 4.8 The SEM images (100k magnification) of MSA-CdSe/ZnS / AET-CdSe/ZnS nanostructure of different level construction are shown above (a)~(e).

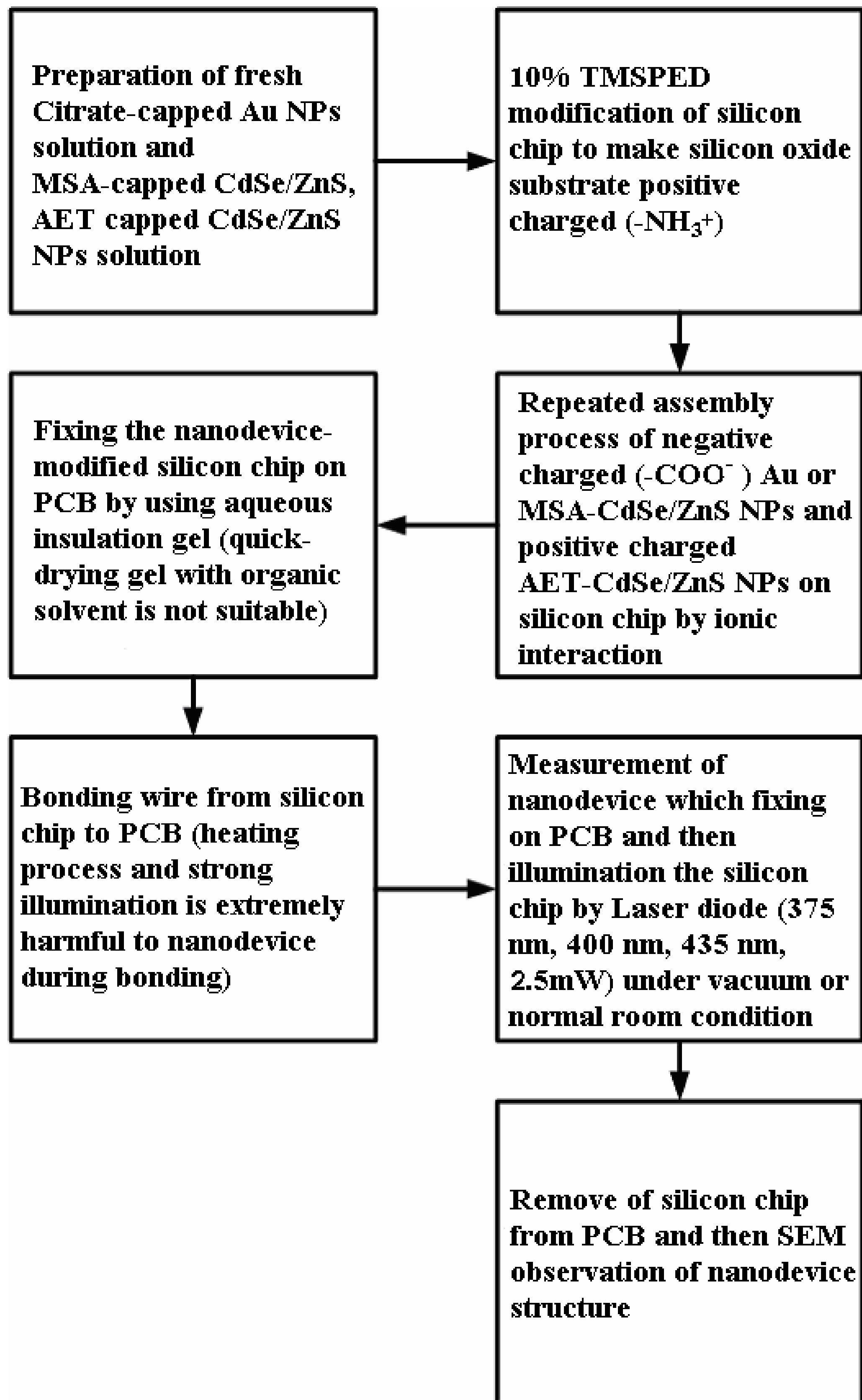
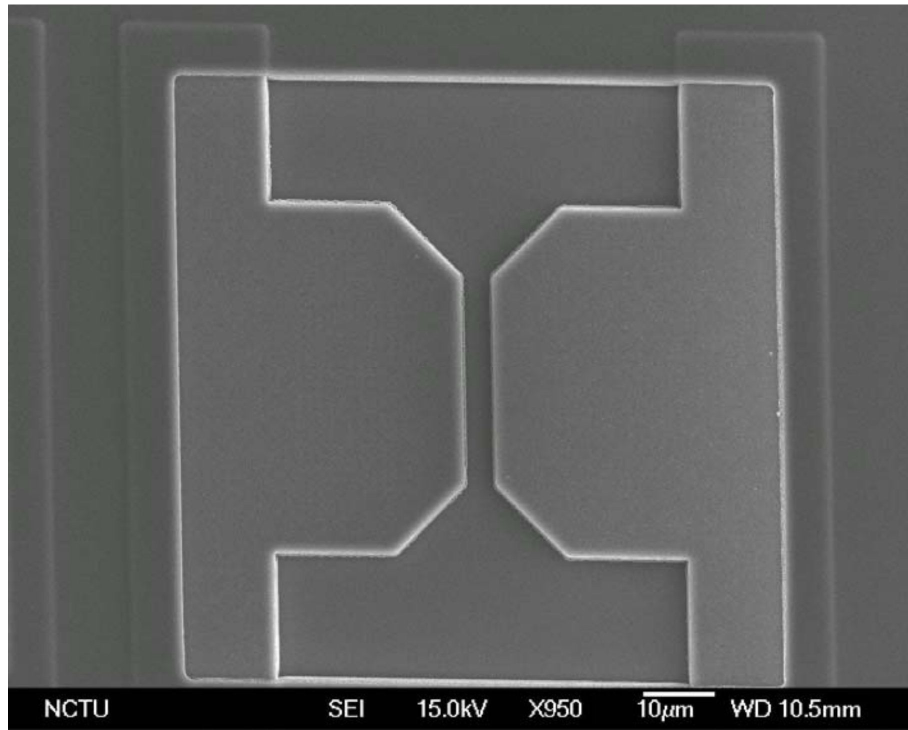
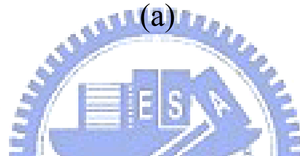
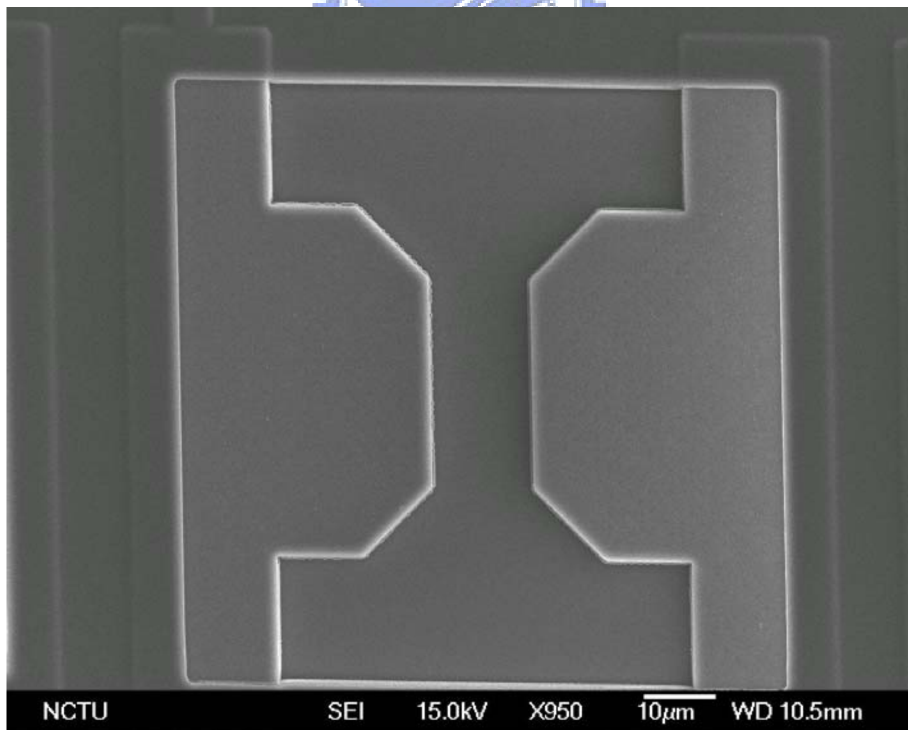


Fig. 4.9 The overall experimental procedure of fabrication and measurement of photo-sensing nanodevice on TSMC 0.35 μm silicon chip.

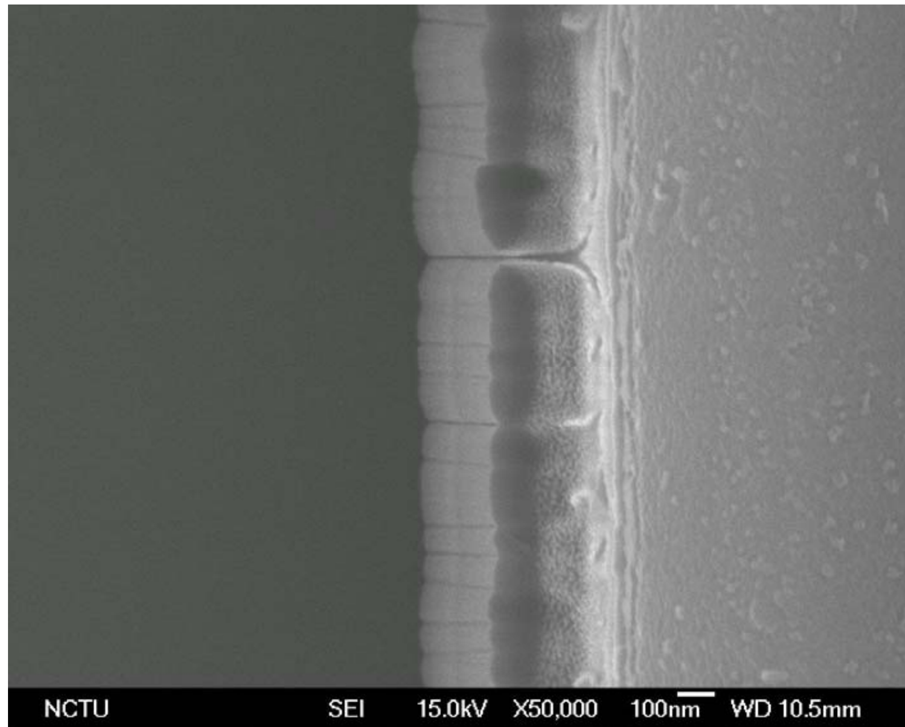


(a)





(b)



(c)

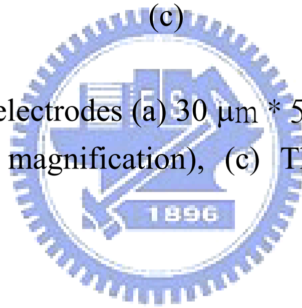
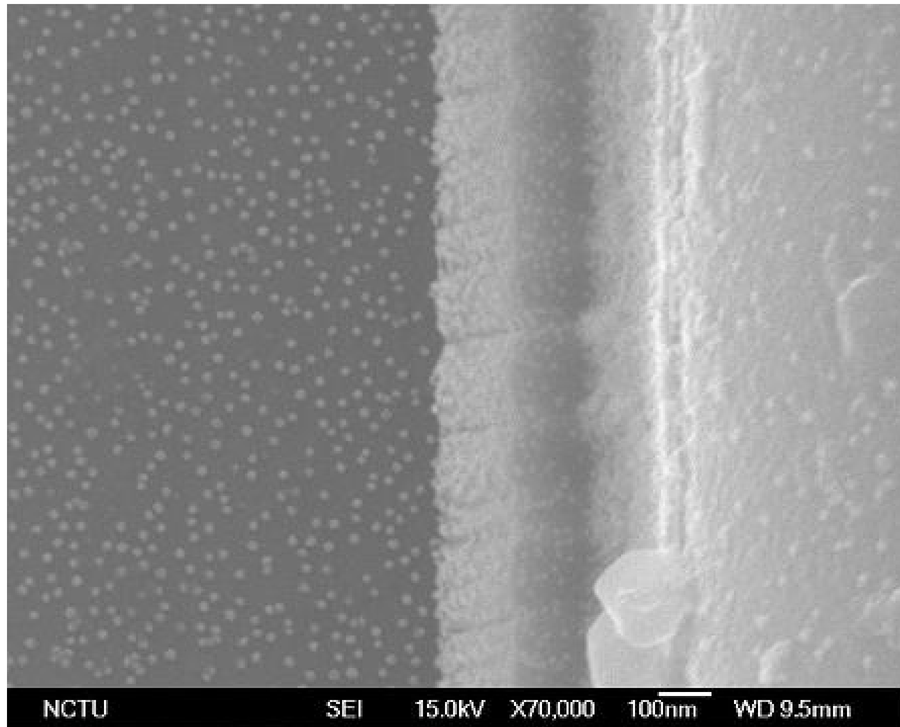
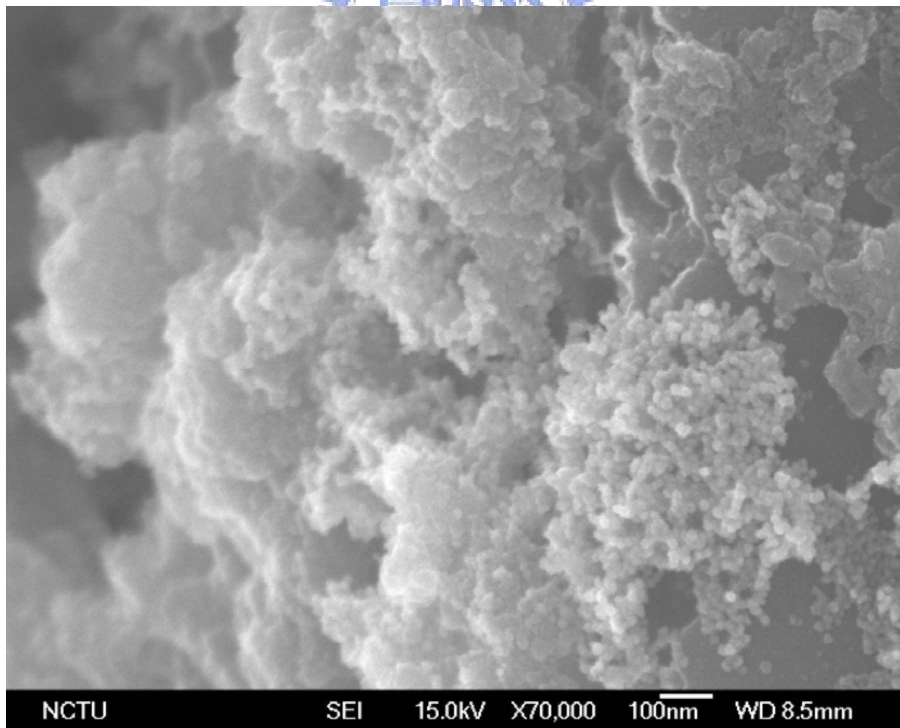


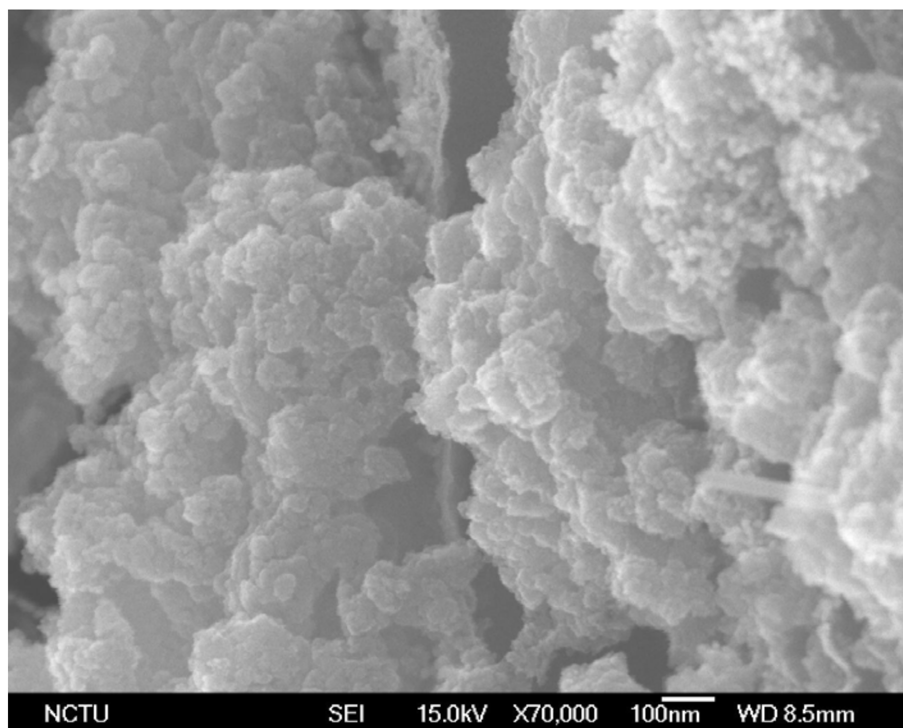
Fig. 4.10 The SEM images of blank electrodes (a) 30 μm * 5 μm electrodes (950 magnification), (b) 30 μm * 15 μm electrodes (950 magnification), (c) The edge part of the electrodes (50k magnification).



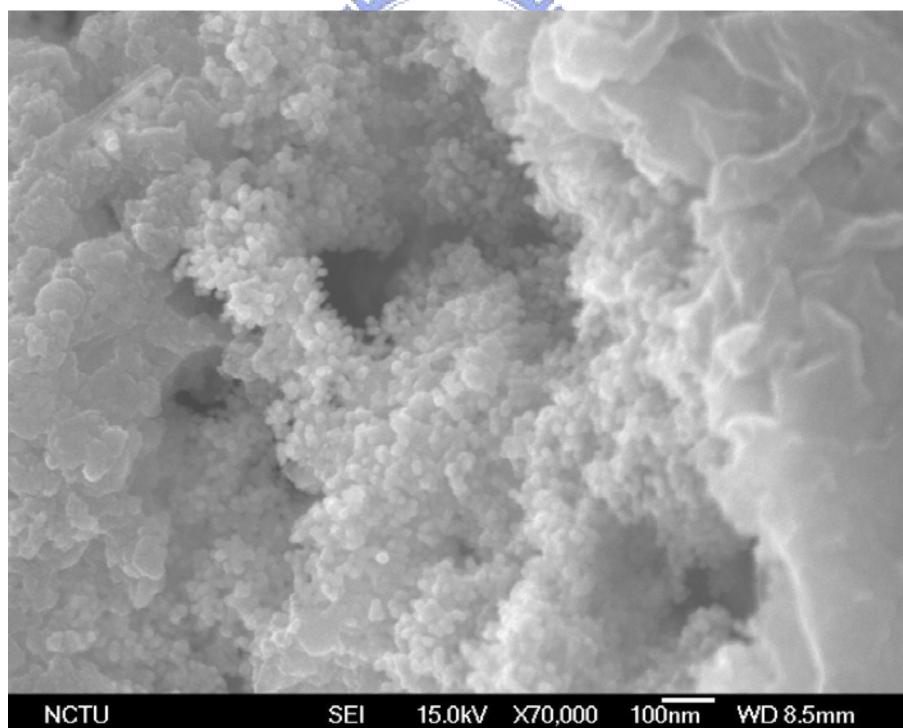
(a)



(b)

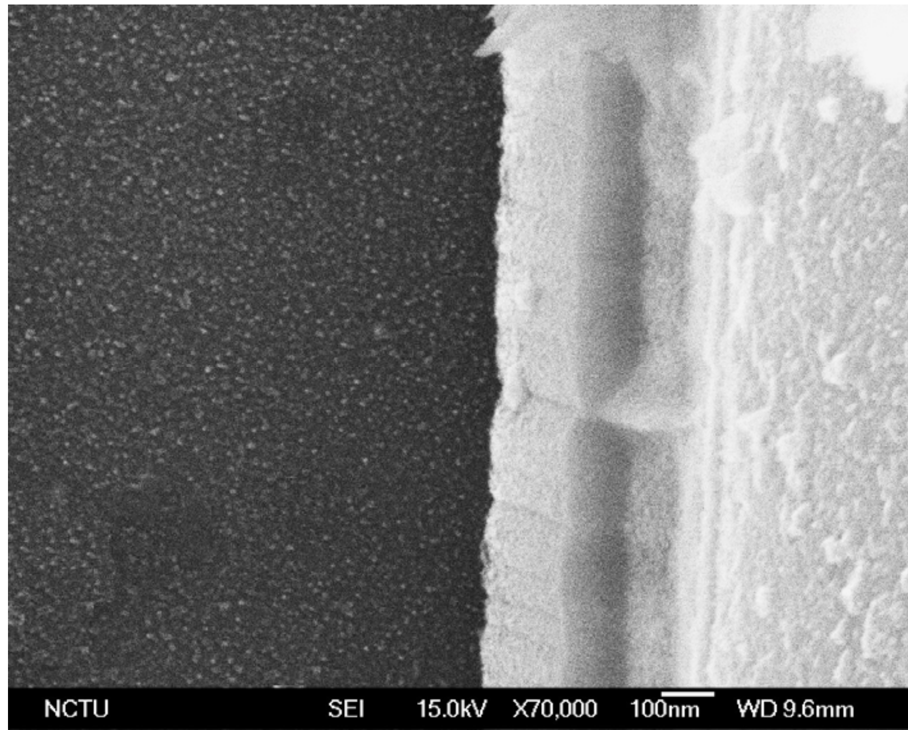


(c)

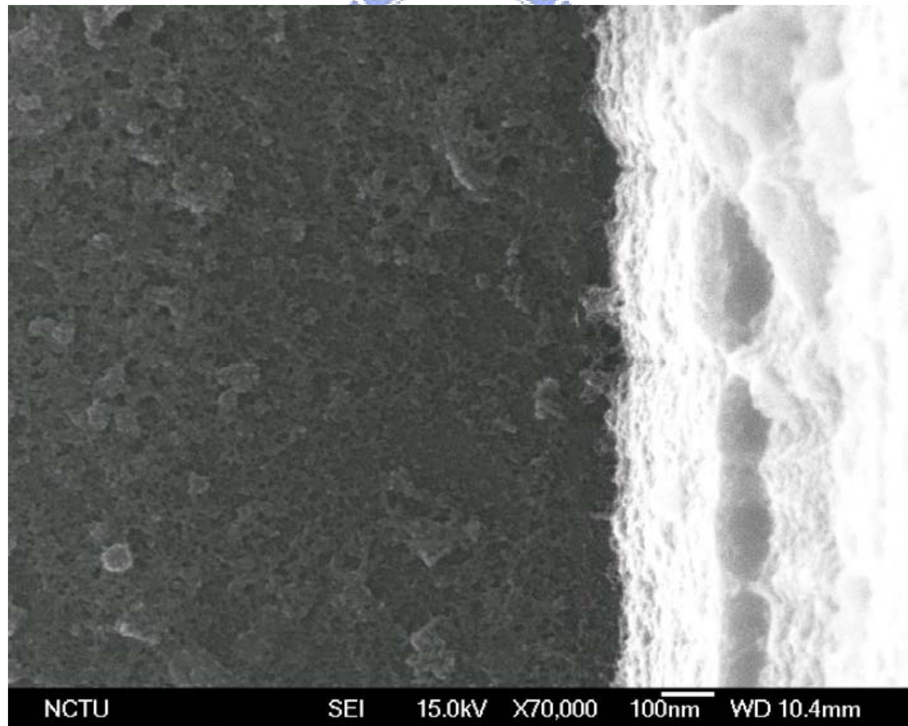


(d)

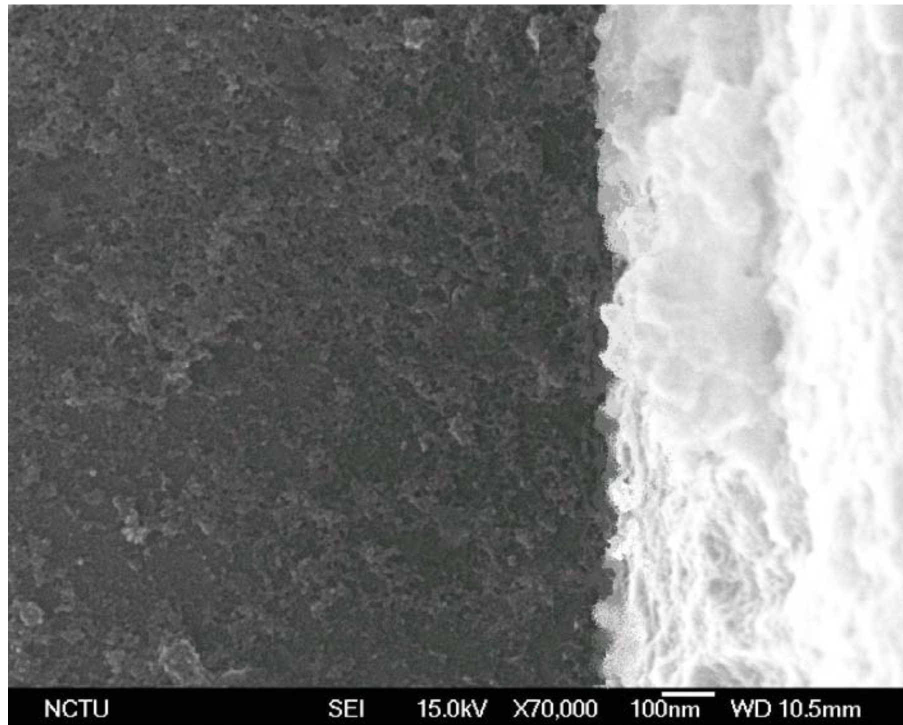
Fig. 4.11 The SEM images (70k magnification) of the edge part of Au / AET-CdSe/ZnS NPs modified electrodes. (a) 1-layered nanostructure, (b) 4-layered nanostructure, (c) 8-layered nanostructure, (d) 12-layered nanostructure.



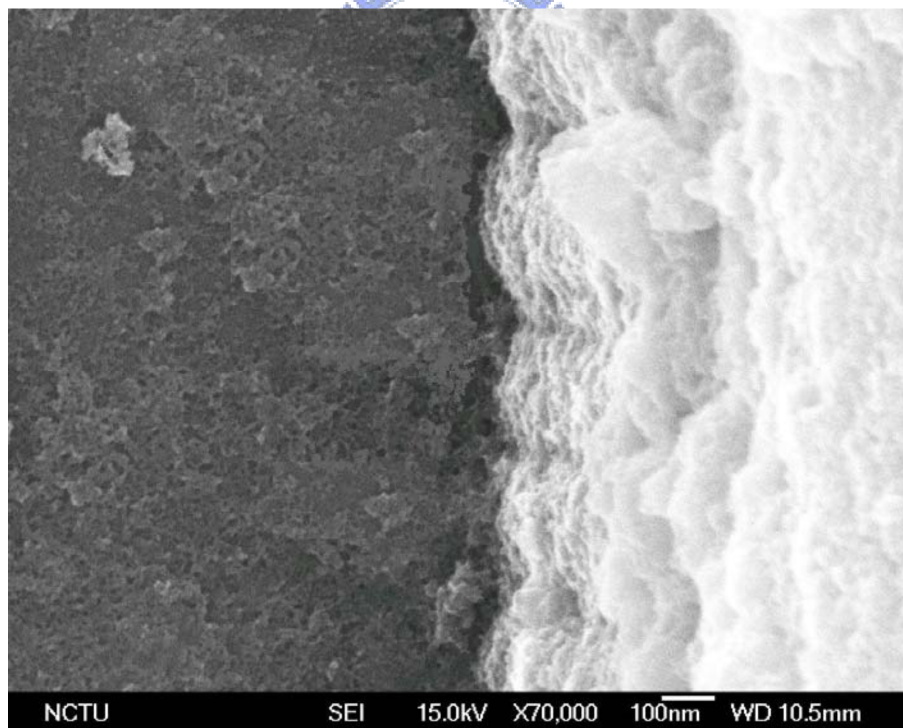
(a)



(b)

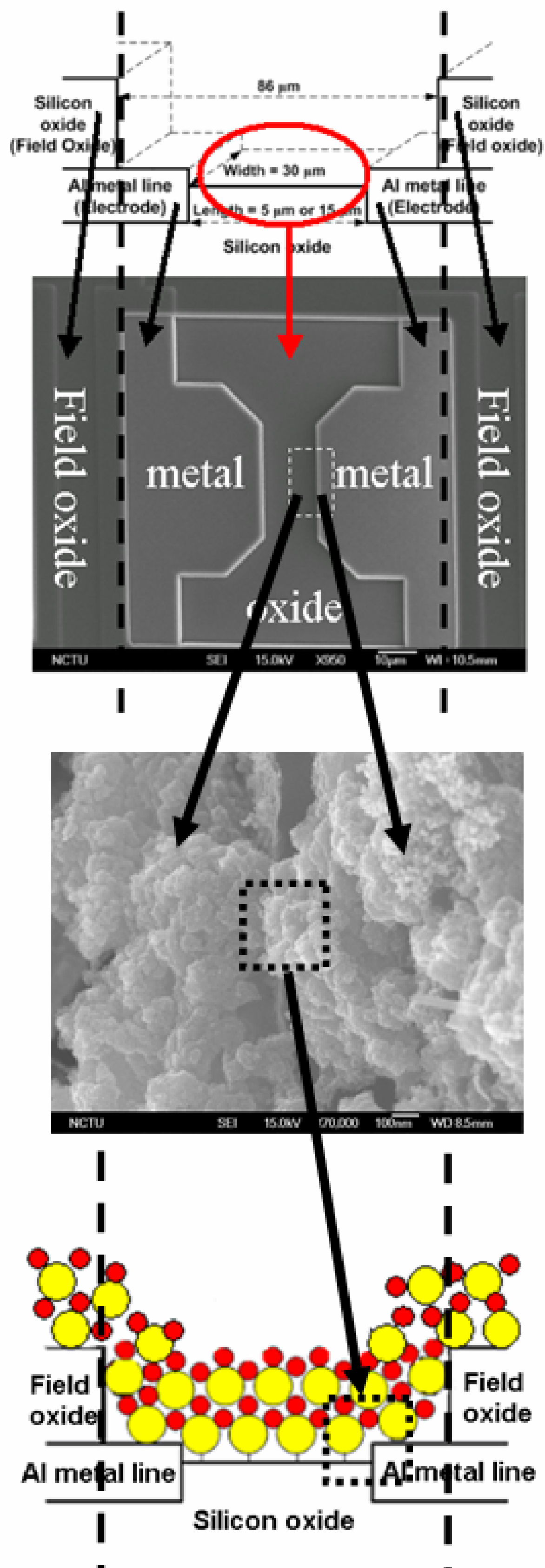


(c)

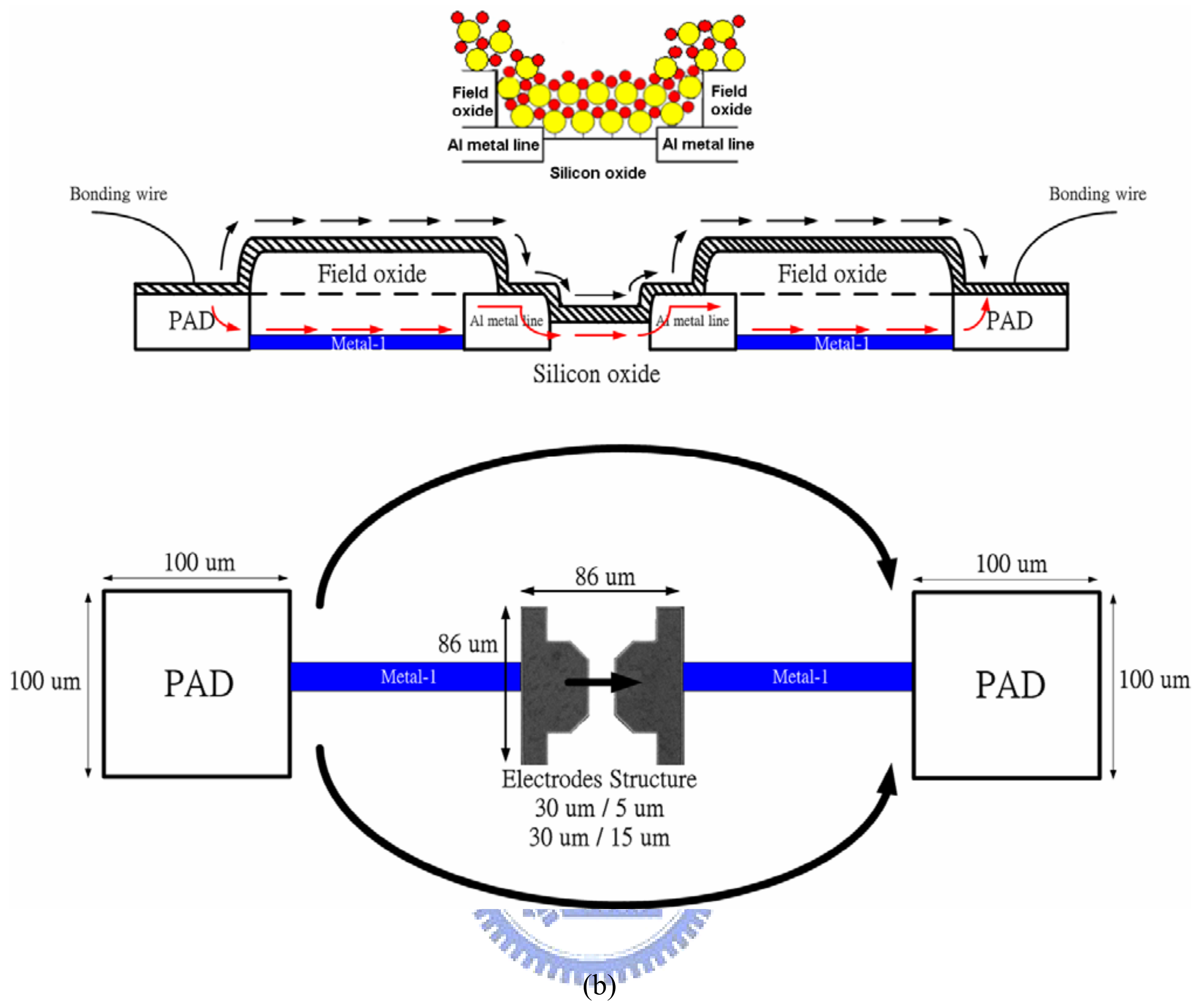


(d)

Fig. 4.12 The SEM images (70k magnification) of the edge part of MSA-CdSe/ZnS / AET-CdSe/ZnS NPs modified electrodes. (a) 1-layered nanostructure, (b) 4-layered nanostructure, (c) 6-layered nanostructure, (d) 12-layered nanostructure.

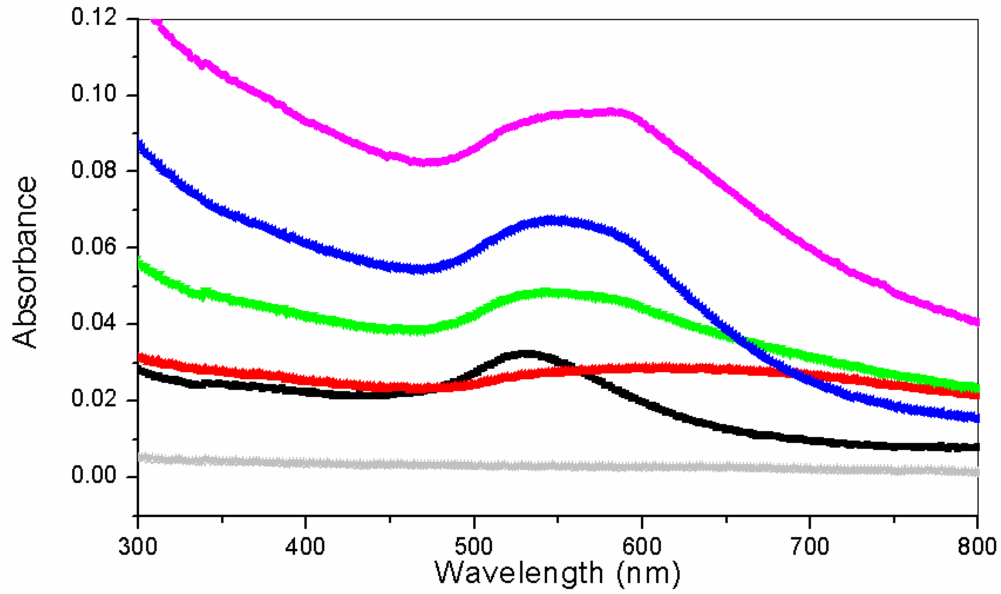


(a)

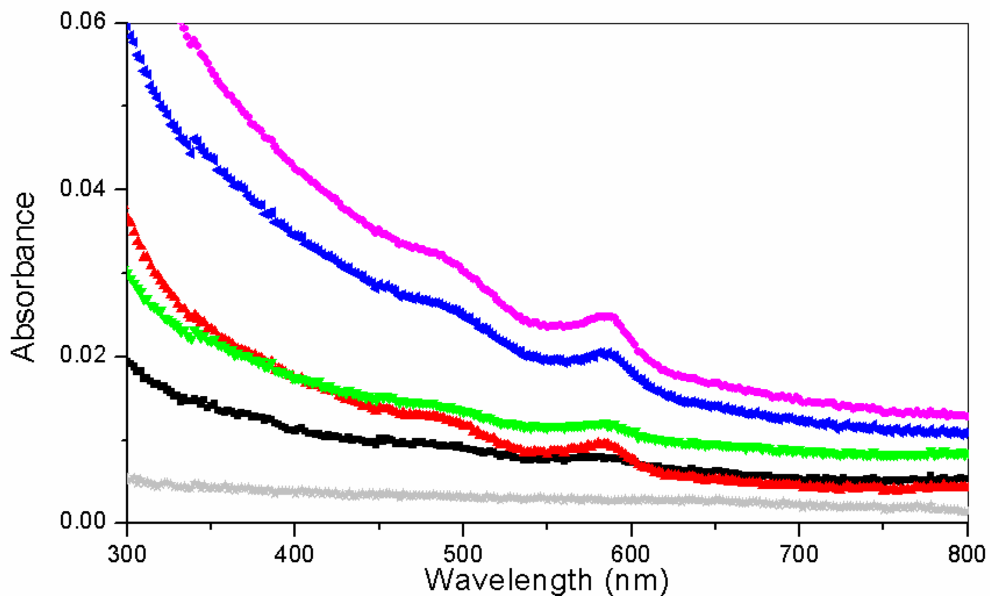


(b)

Fig. 4.13 (a) The cross section figure of the electrodes structure corresponds to SEM image of the nanodevice-modified silicon chip. (b) The current flow trend of the nanodevice structure, and the electrodes dominated the source of the generated current. In the worse case, we must consider the whole chip area for calculation, not the area of the electrodes. (The twill line means the thin film structure composed of NPs).

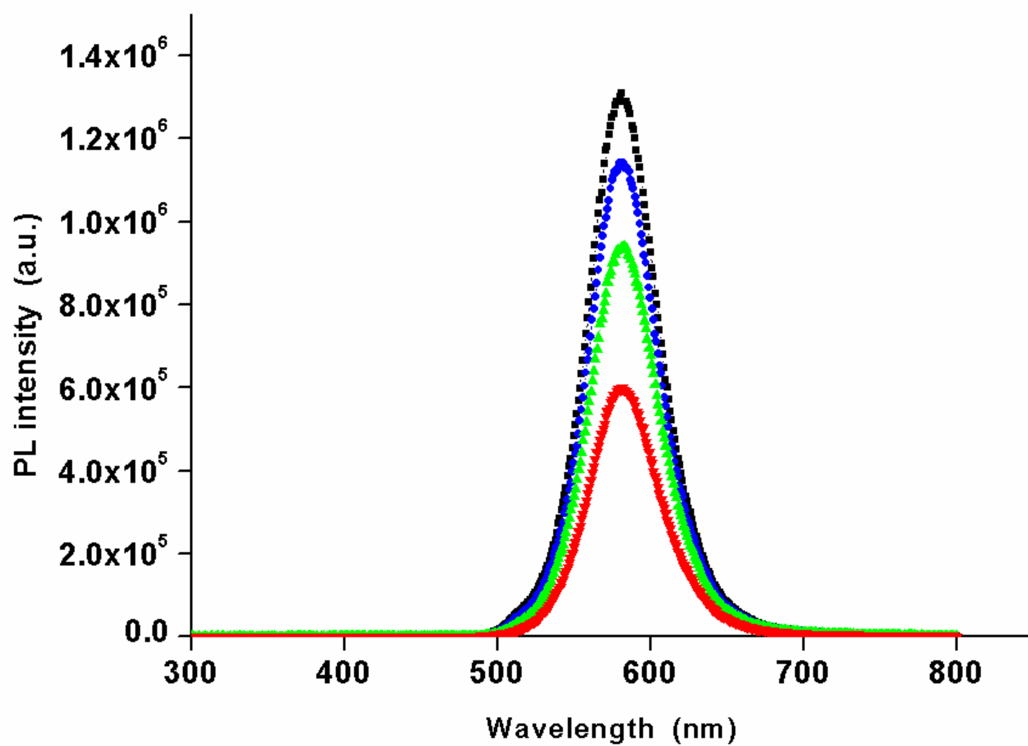


(a)

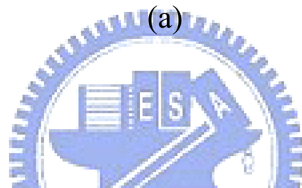


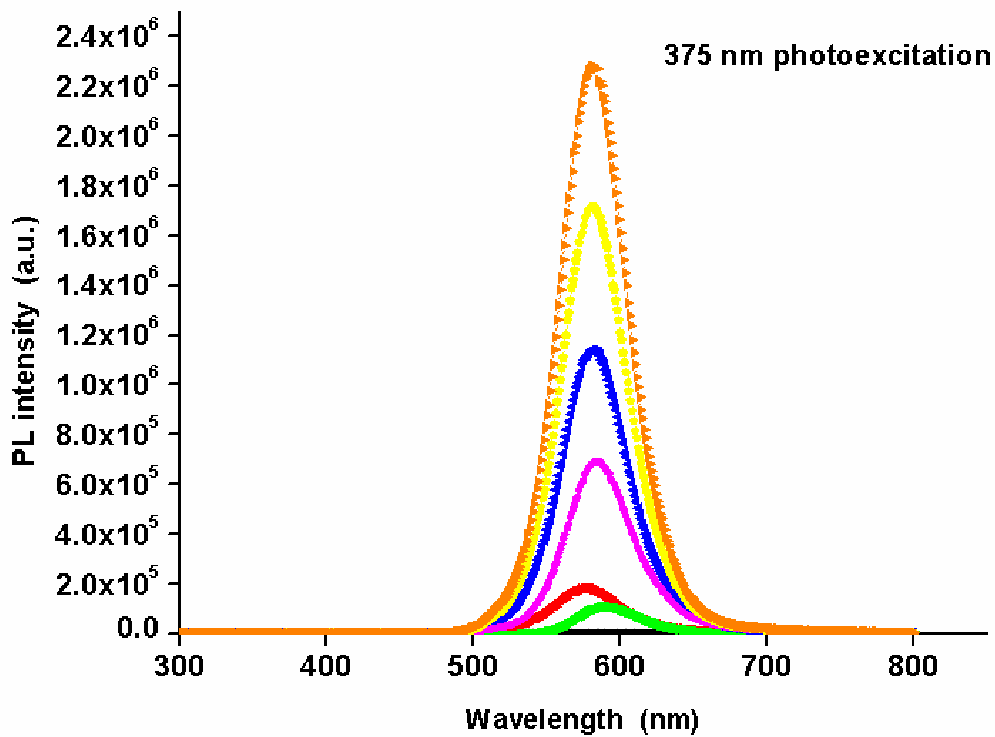
(b)

Fig. 4.14 The UV-visible absorption spectrum of multi-layered nanostructure on quartz glass. (a) Au / AET-CdSe/ZnS (b) MSA-CdSe/ZnS / AET-CdSe/ZnS**.** The Light Gray Line: 10% TMSPED/methanol ->quartz glass. The Black Line: 1-layered nanostructure. The Red Line: 2-layered nanostructure. The Green Line: 3-layered nanostructure. The Blue Line: 4-layered nanostructure. The Magenta Line: 5-layered nanostructure.

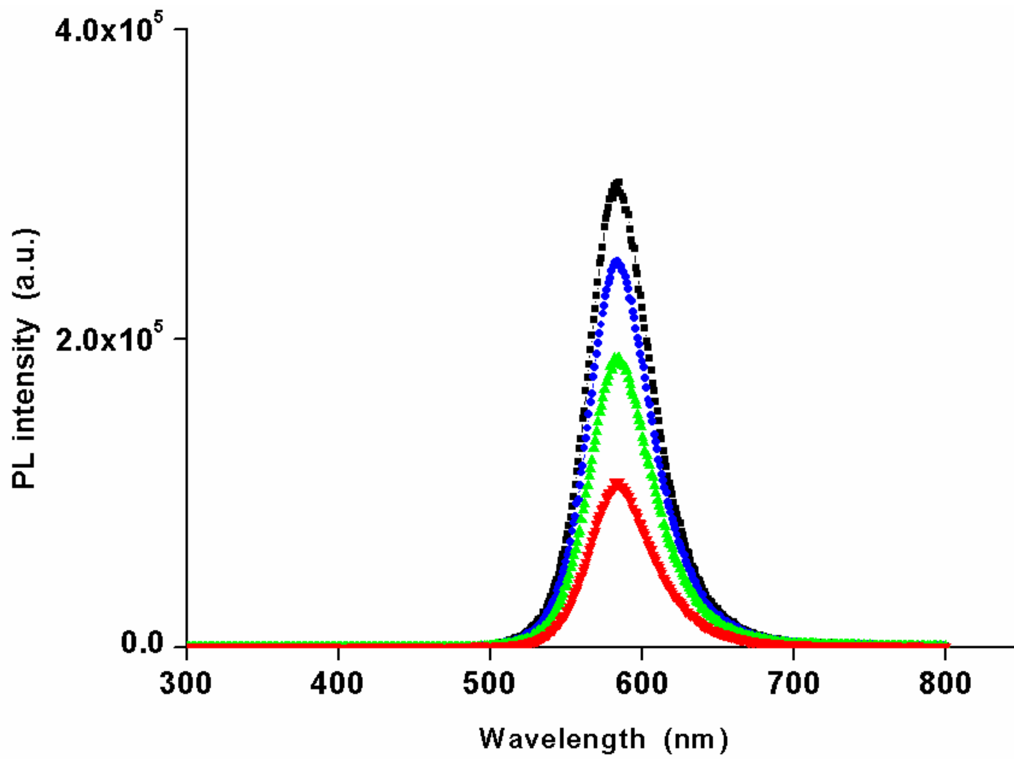


(a)

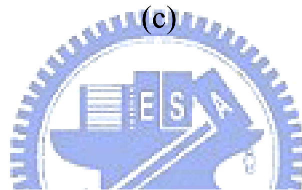


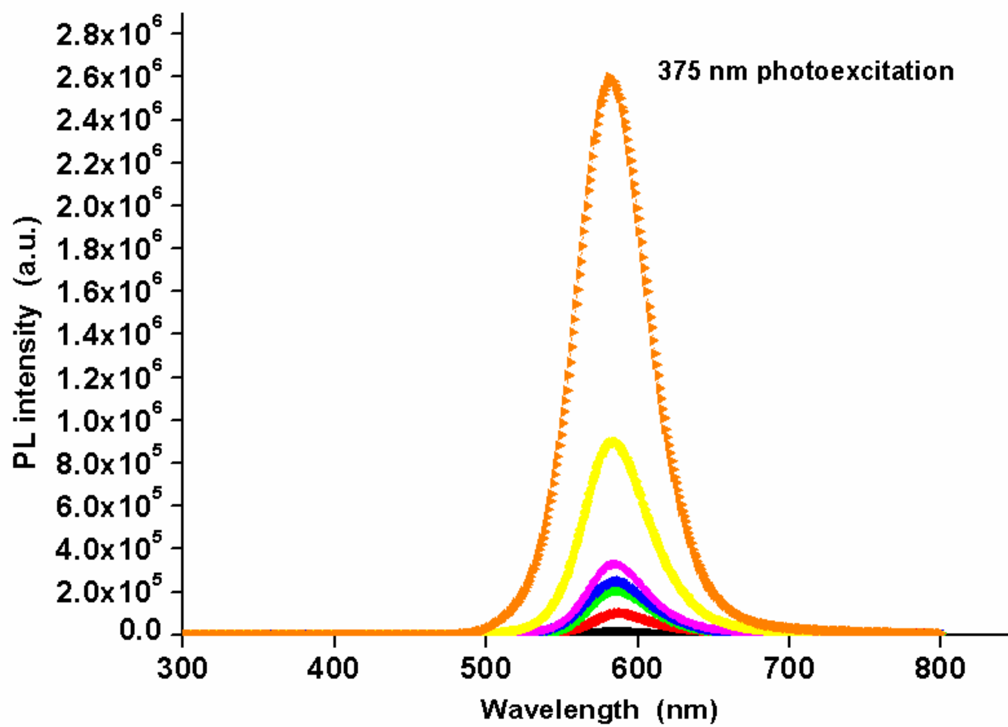


(b)



(c)





(d)

Fig. 4.15 The PL emission spectrum of multi-layered nanostructures on quartz glass. (a)(c) The PL intensity of Au / AET-CdSe/ZnS and MSA-CdSe/ZnS / AET-CdSe/ZnS, 4-layered nanostructure. The Red Line: photo-excitation with 435nm wavelength; The Green Line: photo-excitation with 400 nm wavelength; The Blue Line: photo-excitation with 375 nm wavelength; The Black Line: photo-excitation with 365 nm wavelength. (b)(d) The PL intensity of Au / AET-CdSe/ZnS and MSA-CdSe/ZnS / AET-CdSe/ZnS, multi-layered nanostructure under 375 nm photo-excitation. The Black Line: 1-layered nanostructure; The Red Line: 2-layered nanostructure; The Green Line: 3-layered nanostructure; The Blue Line: 4-layered nanostructure; The Magenta Line: 5-layered nanostructure; The Yellow Line: 8-layered (b) and 6-layered (d) nanostructure; The Orange Line: 12-layered nanostructure.

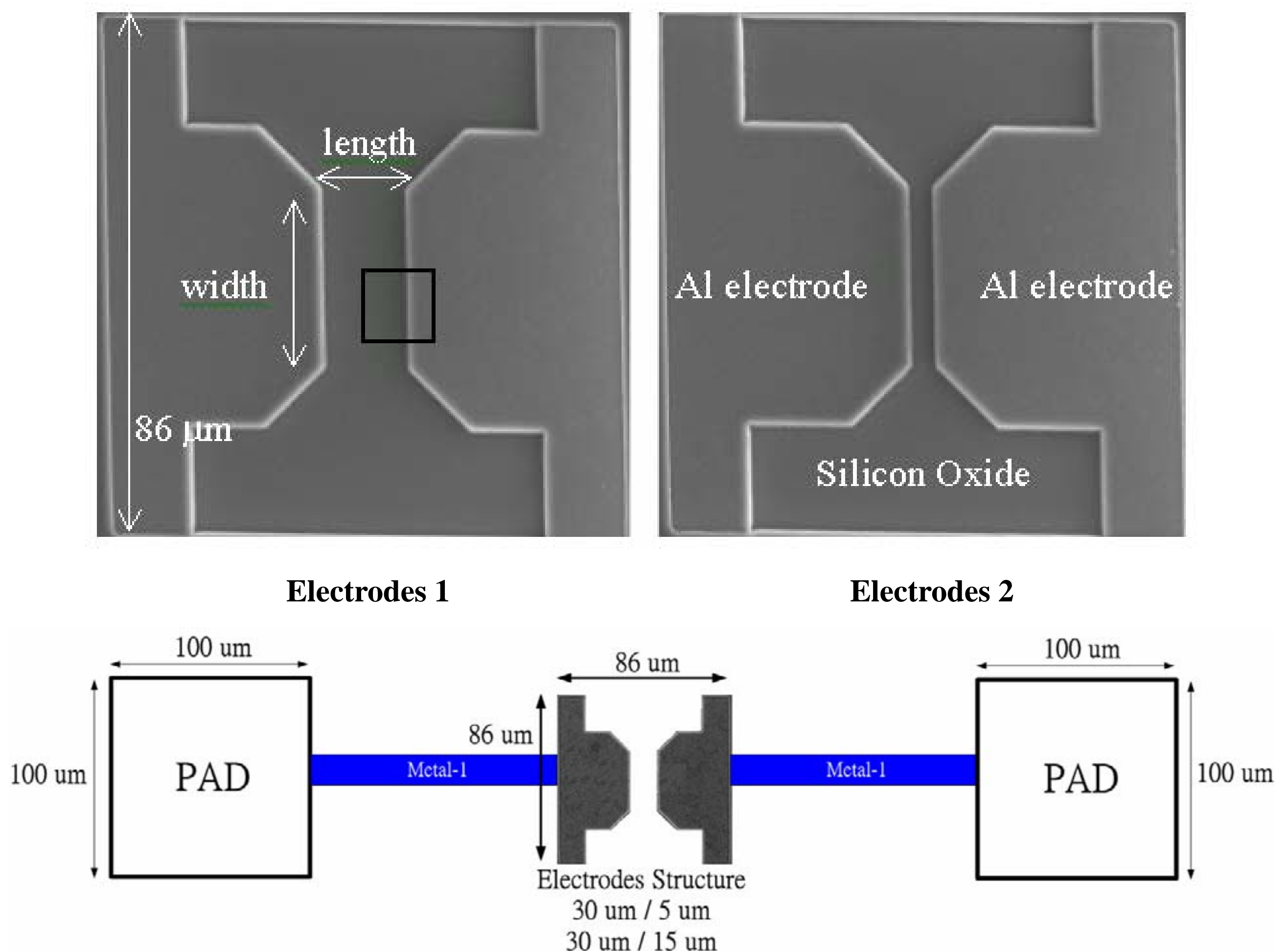
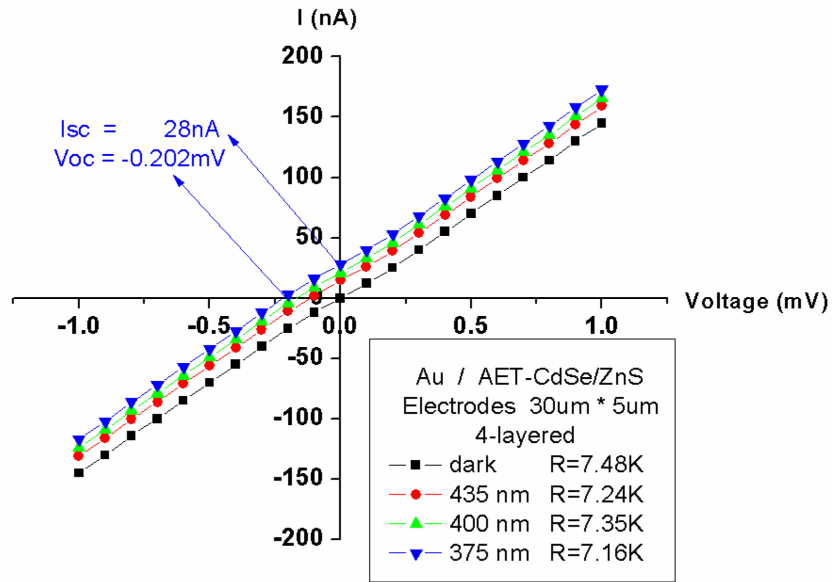
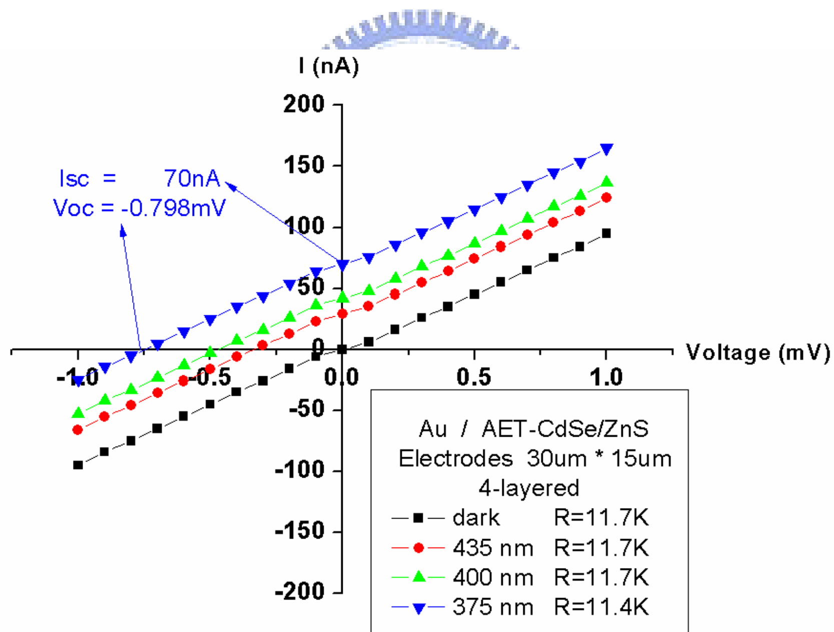


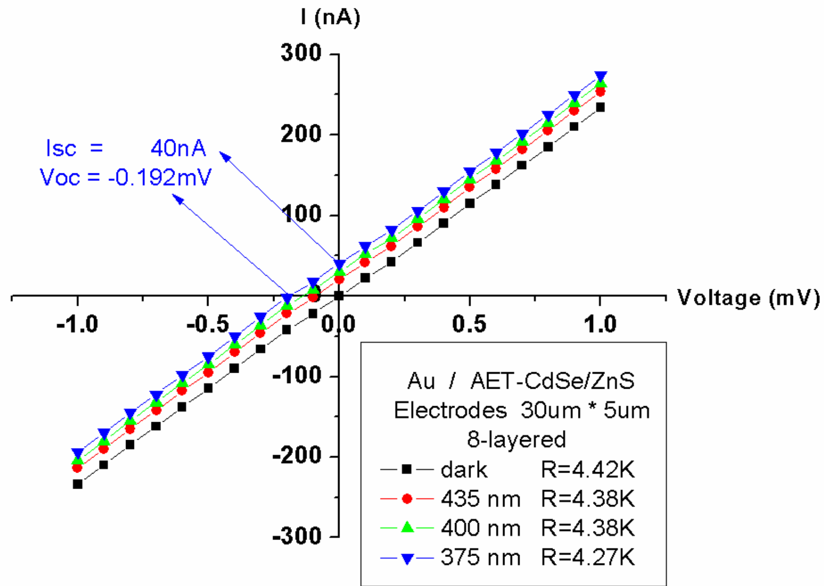
Fig. 4.16 The electrodes under measuring are shown above. Electrodes 1 and 2 have silicon oxide region of 30 μm * 15 μm and 30 μm * 5 μm (width * length), respectively.



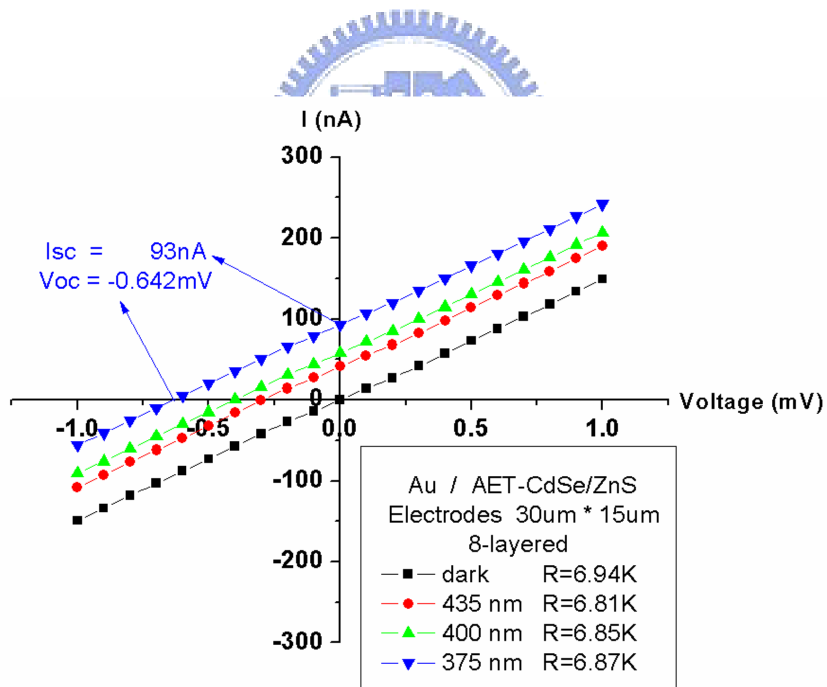
AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / SiO_2
4-layered, 30 μm * 5 μm electrodes



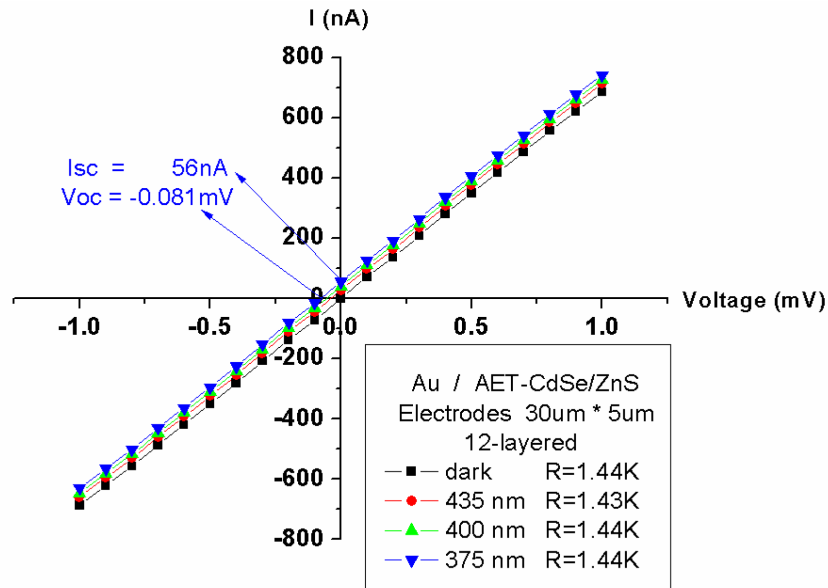
AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / SiO_2
4-layered, 30 μm * 15 μm electrodes



AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / SiO_2
8-layered, 30 μm * 5 μm electrodes

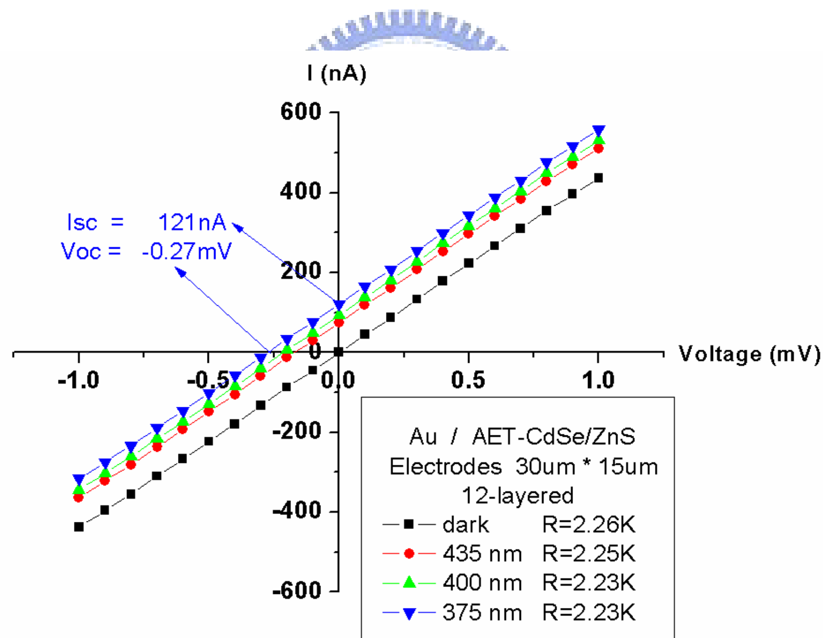


AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / SiO_2
8-layered, 30 μm * 15 μm electrodes



AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / SiO_2

12-layered, 30 μm * 5 μm electrodes



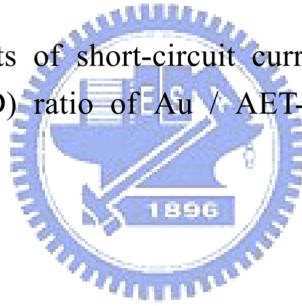
AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / AET-CdSe/ZnS / Au / SiO_2

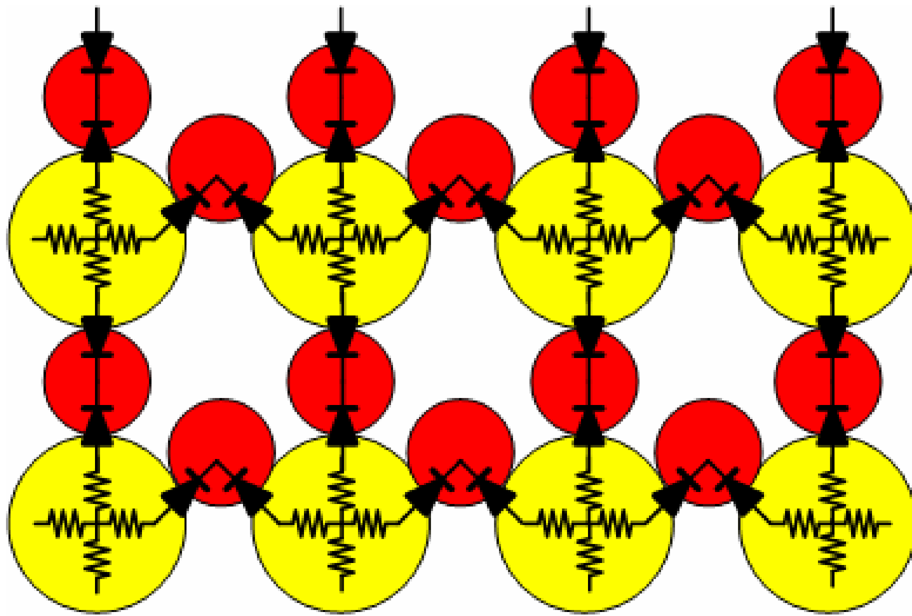
12-layered, 30 μm * 15 μm electrodes

Fig. 4.17 The I-V curves of the multi-layered Au / AET-CdSe/ZnS photo-sensing nanodevice when in dark (black line) or illumination with 375 nm (blue line), 400 nm (green line), 435 nm (red line) laser diode.

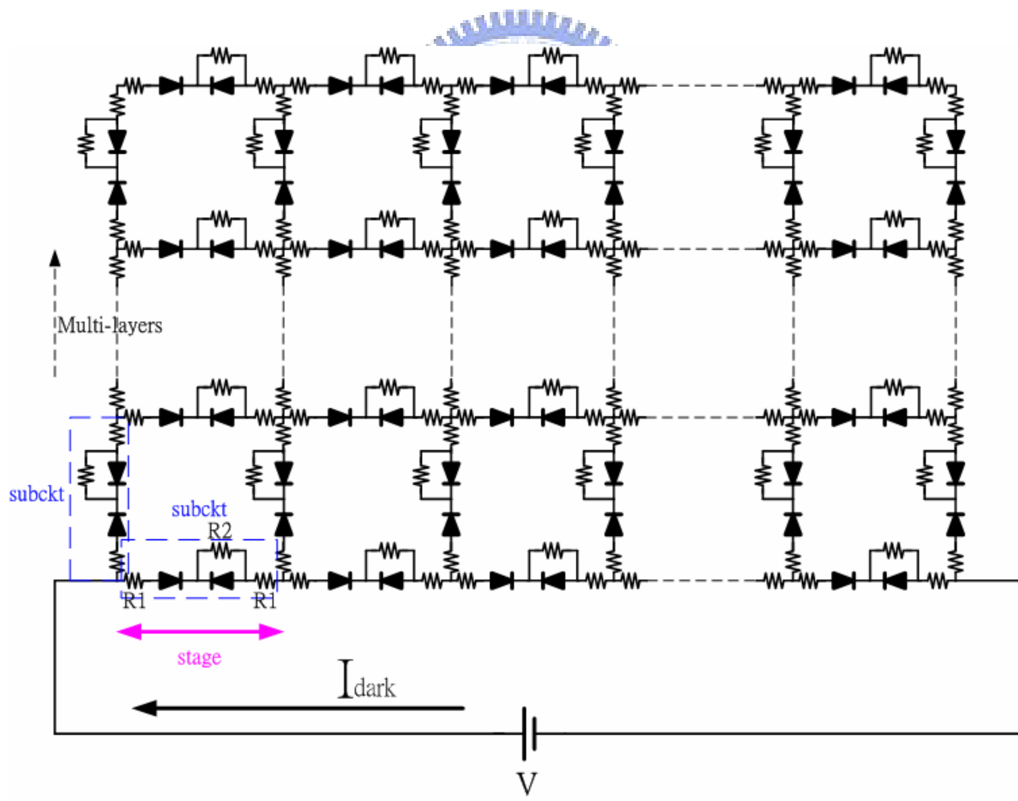
	30μm * 5μm Electrodes			30μm * 15μm Electrodes		
Req	4-layered 7.2KΩ	8-layered 4.8KΩ	12-layered 1.44KΩ	4-layered 11.4KΩ	8-layered 6.9KΩ	12-layered 2.23KΩ
Isc Voc PVD Ratio **(375 nm)**	**28nA** **-0.202mV** **473**	**40nA** **-0.192mV** **338**	**56nA** **-0.081mV** **315**	**70nA** **-0.798mV** **1183**	**93nA** **-0.642mV** **787**	**121nA** **-0.27mV** **682**
Isc Voc PVD Ratio **(400 nm)**	**21nA** **-0.151mV** **355**	**30nA** **-0.144mV** **253**	**40nA** **-0.058mV** **225**	**42nA** **-0.48mV** **710**	**71nA** **-0.49mV** **600**	**94nA** **-0.21mV** **529**
Isc Voc PVD Ratio **(435 nm)**	**15nA** **-0.108mV** **253**	**20nA** **-0.096mV** **169**	**27nA** **-0.039mV** **152**	**29nA** **-0.331mV** **490**	**55nA** **-0.38mV** **465**	**74nA** **-0.165mV** **417**

Table. 4.1 The measurement results of short-circuit current I_{sc}, open-circuit voltage V_{oc}, and photocurrent volume dendity (PVD) ratio of Au / AET-CdSe/ZnS, multi-layered nanodevice.





(a)



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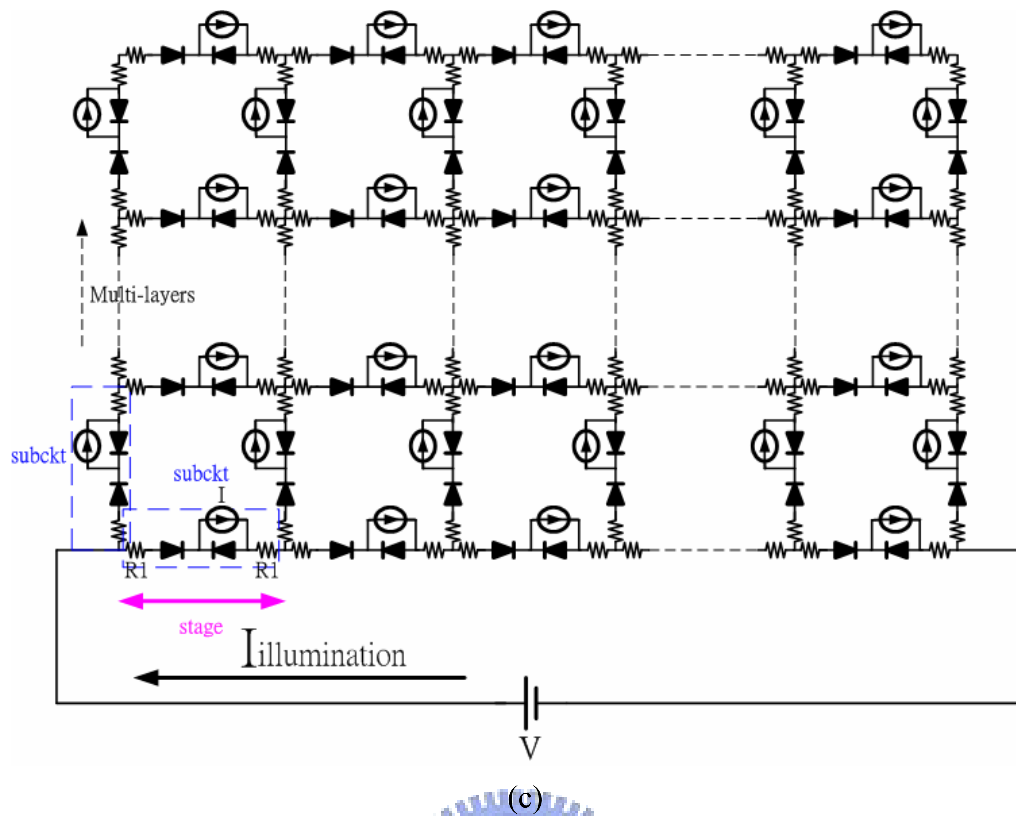
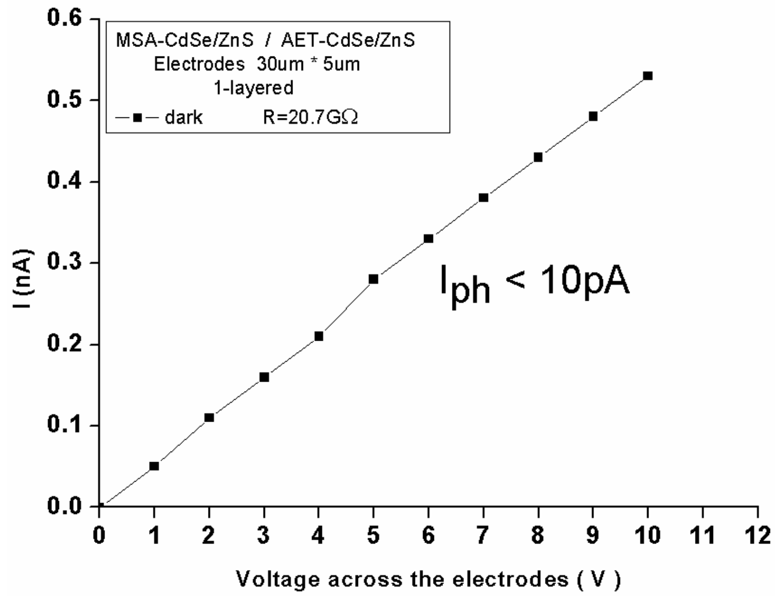


(c)

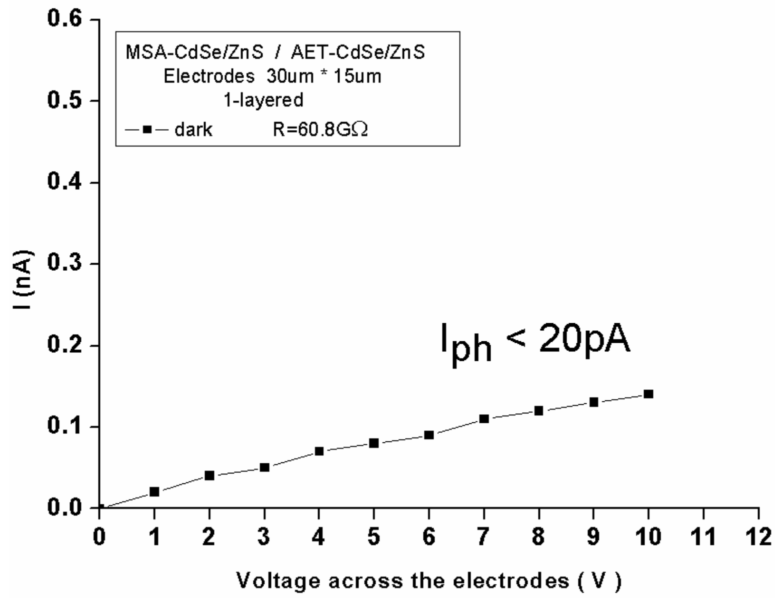
Fig. 4.18 (a) Two-dimensional array of resistors and nano-Schottky-diodes. (b) (c) The models for nanodevice in dark and under illumination. For HSPICE simulation, Metal-Insulator-Semiconductor diode model was employed, V = 0.4 V, R1 = 0.25 MΩ, R2 = 5 MΩ and I = 5 pA.

4-layered nanostructure	I_{dark}	$I_{illumination}$	I_{ph}
30 μm * 5 μm (15 stages)	**6.38 pA**	**9.62 pA**	**3.24 pA**
30 μm * 15 μm (45 stages)	**0.53 pA**	**6.95 pA**	**6.42 pA**
8-layered nanostructure	I_{dark}	$I_{illumination}$	I_{ph}
30 μm * 5 μm (15 stages)	**9.63 pA**	**15.86 pA**	**6.23 pA**
30 μm * 15 μm (45 stages)	**0.95 pA**	**12.62 pA**	**11.67 pA**
12-layered nanostructure	I_{dark}	$I_{illumination}$	I_{ph}
30 μm * 5 μm (15 stages)	**10.98 pA**	**19.82 pA**	**8.84 pA**
30 μm * 15 μm (45 stages)	**1.26 pA**	**17.16 pA**	**15.9 pA**

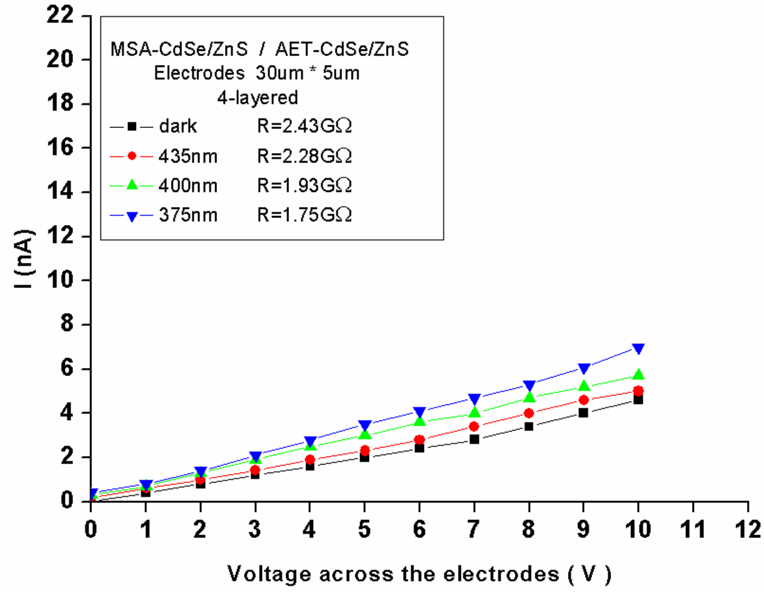
Table. 4.2 The simulation results of multi-layers, two-dimensional nano-Schottky-diode arrays model by using HSPICE software.



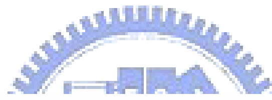
MSA-CdSe/ZnS / SiO_2
1-layered, 30 μm * 5 μm electrodes

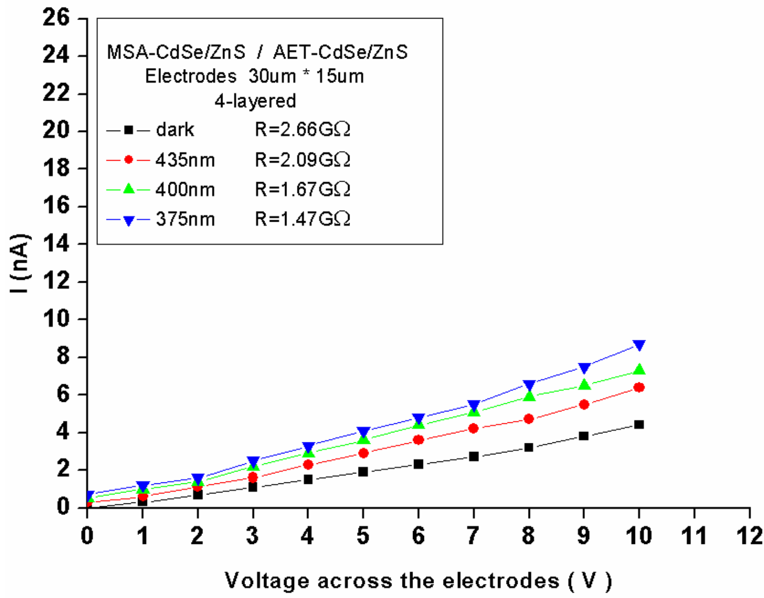


MSA-CdSe/ZnS / SiO_2
1-layered, 30 μm * 15 μm electrodes

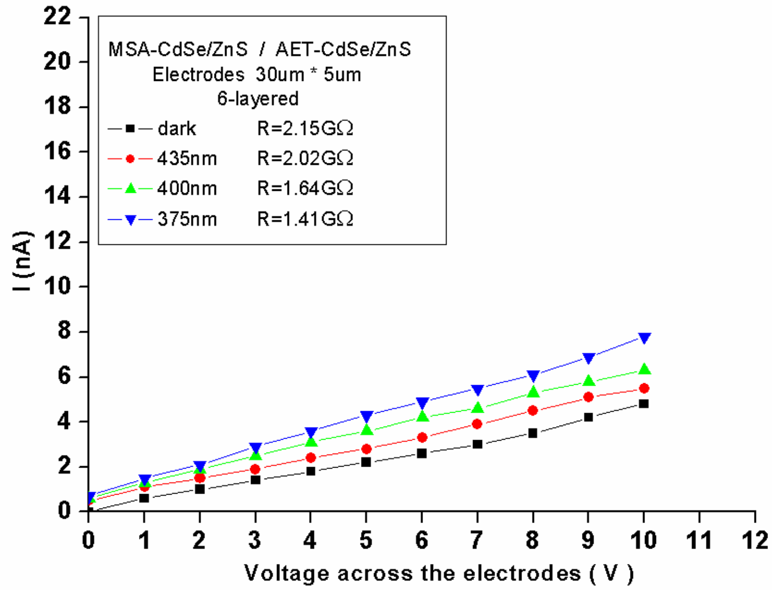


AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / SiO_2
4-layered, 30 μm * 5 μm electrodes



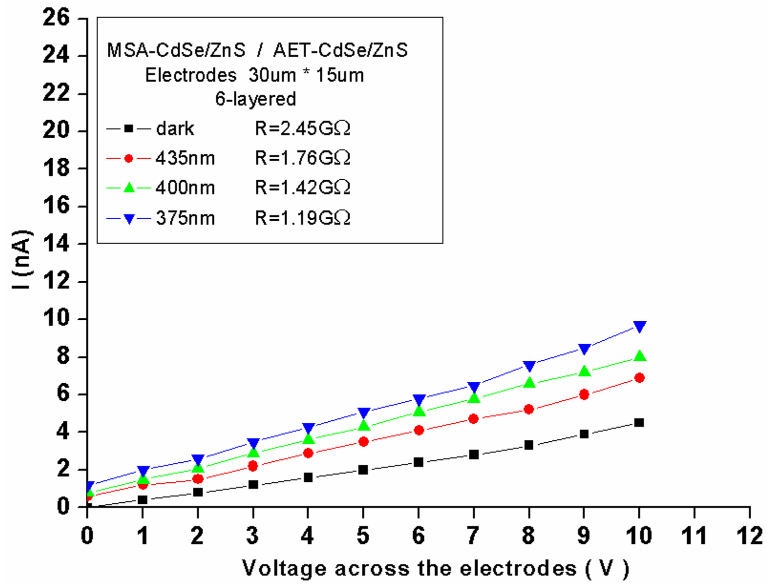


AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / SiO_2
4-layered, 30 μm * 15 μm electrodes



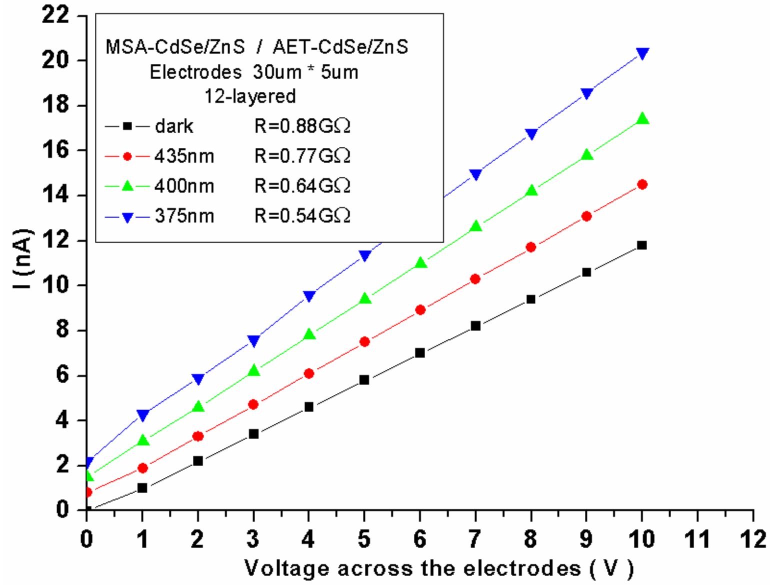
AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / SiO_2

6-layered, 30 μm * 5 μm electrodes



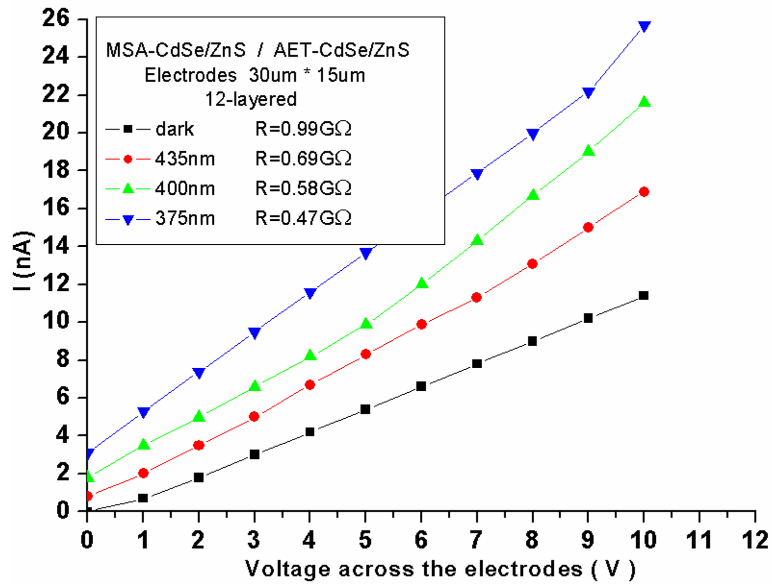
AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / SiO_2

6-layered, 30 μm * 15 μm electrodes



AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / SiO_2

12-layered, 30 μm * 5 μm electrodes



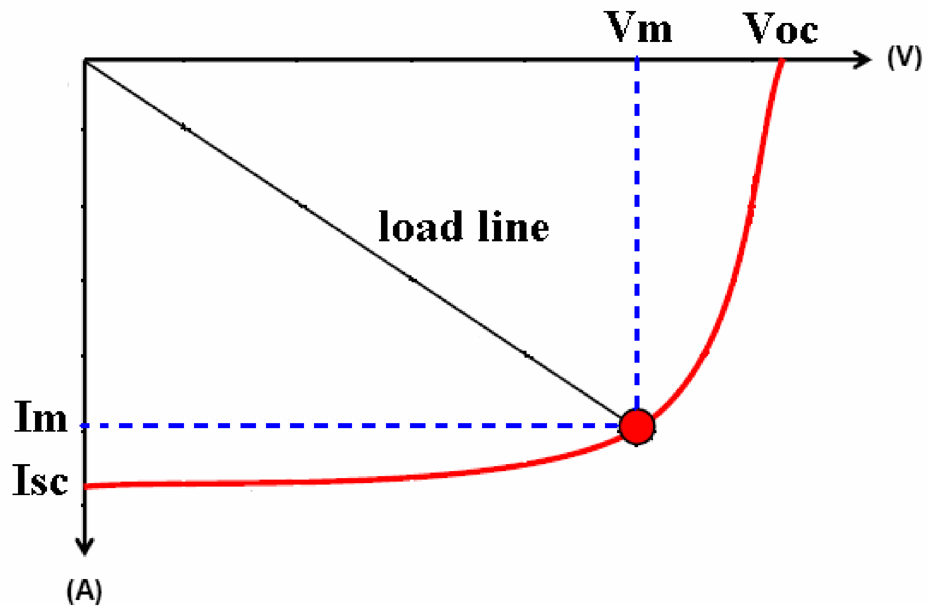
AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / AET-CdSe/ZnS / MSA-CdSe/ZnS / SiO_2

12-layered, 30 μm * 15 μm electrodes

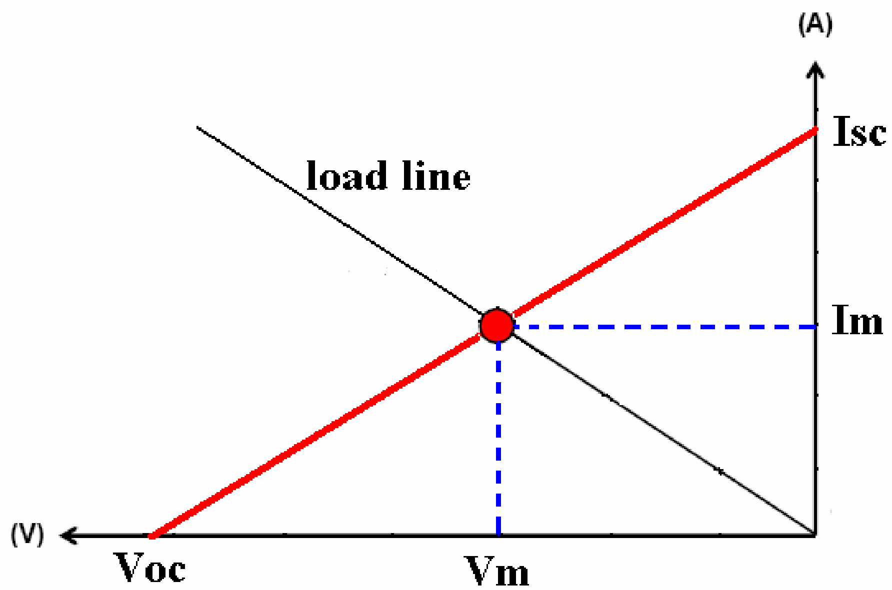
Fig. 4.19 The I-V curves of the multi-layered MSA-CdSe/Zn / AET-CdSe/ZnS photo-sensing nanodevice when in dark (black line) or illumination with 375 nm (blue line), 400 nm (green line), 435 nm (red line) laser diode.

	30μm * 5μm Electrodes			30μm * 15μm Electrodes		
	4-layered	6-layered	12-layered	4-layered	6-layered	12-layered
Isc PVD Ratio **(375 nm)**	**0.4nA** **13**	**0.7nA** **15**	**2.2nA** **24**	**0.7nA** **23**	**1.2nA** **26**	**3.1nA** **34**
Isc PVD Ratio **(400 nm)**	**0.3nA** **10**	**0.6nA** **13**	**1.7nA** **19**	**0.5nA** **17**	**1nA** **22**	**2.3nA** **25**
Isc PVD Ratio **(435 nm)**	**0.2nA** **6**	**0.5nA** **11**	**1.3nA** **14**	**0.3nA** **9**	**0.7nA** **15**	**1.9nA** **22**

Table. 4.3 The measurement results of short-circuit current I_{sc}, and photocurrent volume dendity (PVD) ratio of MSA-CdSe/ZnS / AET-CdSe/ZnS, multi-layered nanodevice.



(a)



(b)

Fig. 4.20 I-V characteristics of an illuminated solar cell. (a) Typical p-n junction solar cell in the fourth quadrant. (b) Au / AET-CdSe/ZnS solar cell in the second quadrant.

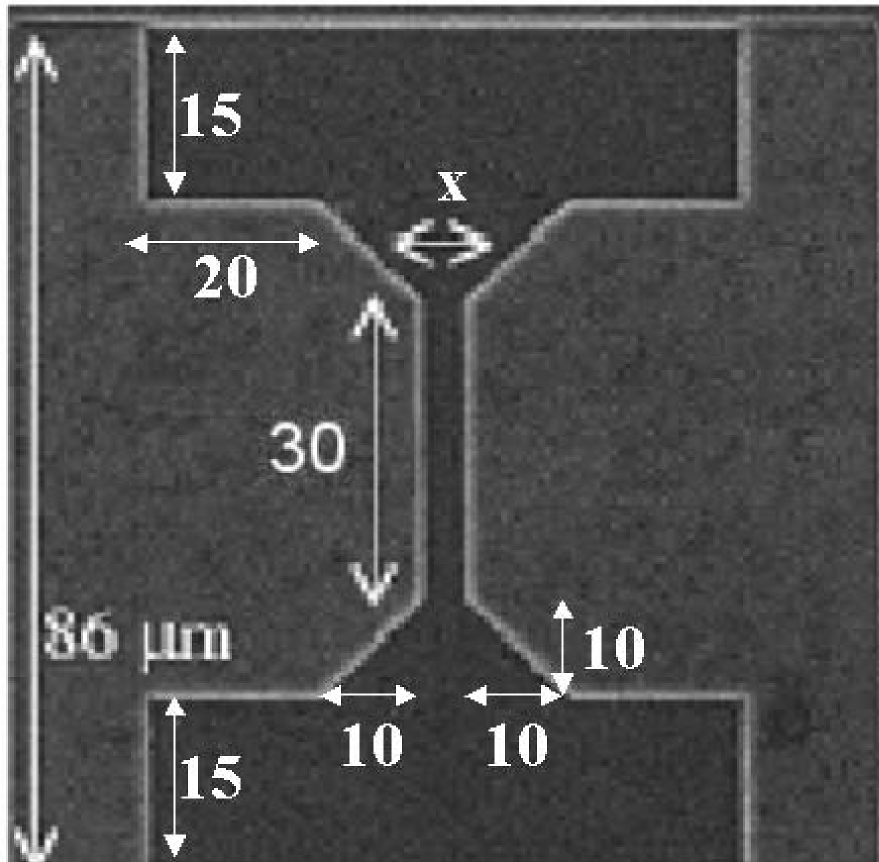
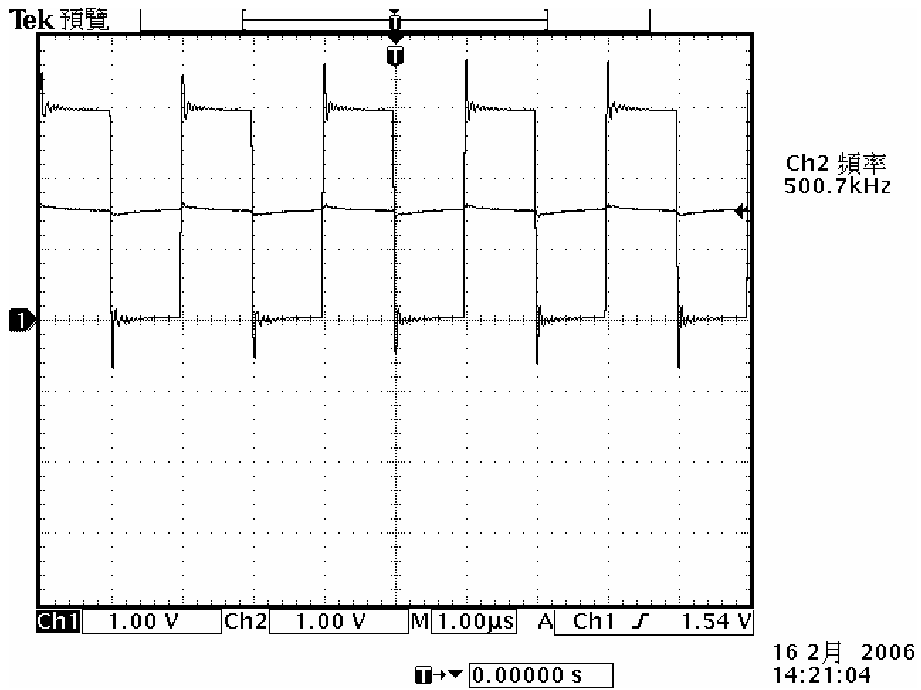


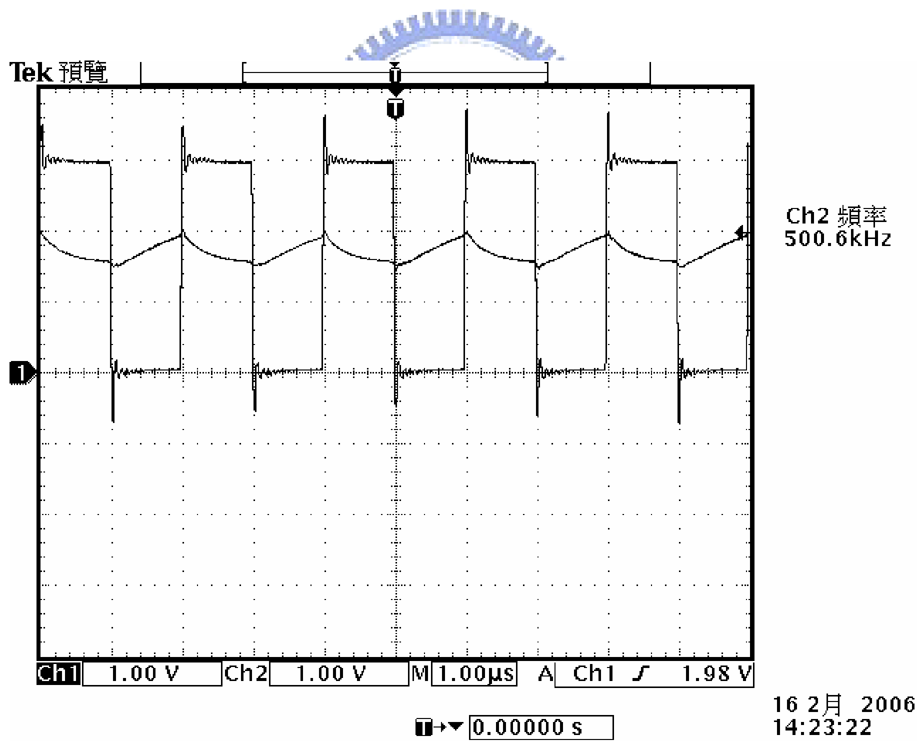
Fig. 4.21 The electrodes of size 30 µm / X µm (width / length)

Vdd	3.3 V
Vop	2 V
Vin	1.7 V
Vbias	~ 1.70118V
Ioffset	6 µA
Reset	Square wave, 3~0 V, 500 kHz
Rd	~ 7.5 kΩ
Laser source (2.5mW / cm^2)	375 nm，400 nm，435 nm

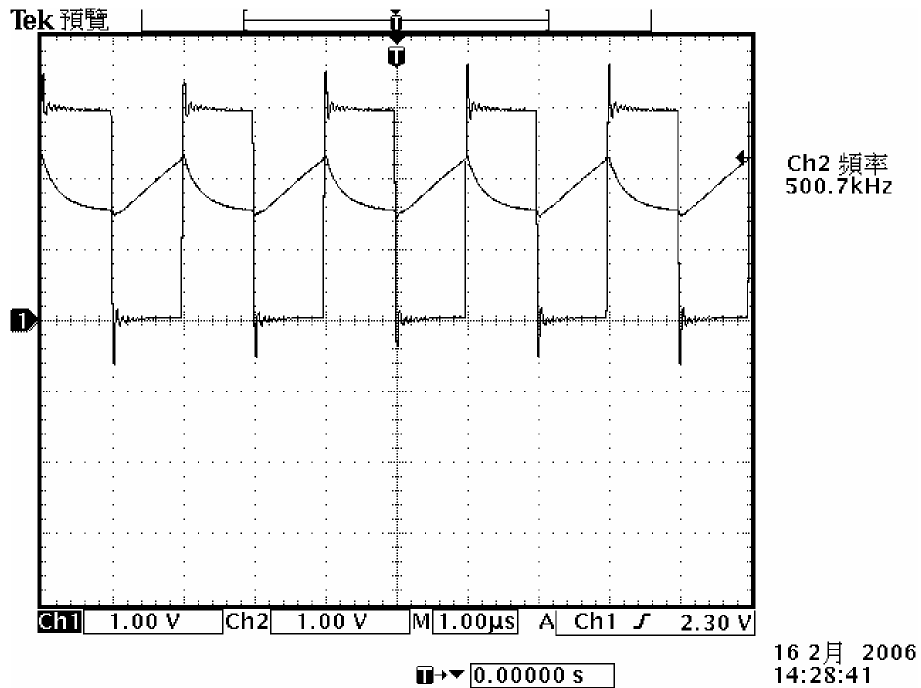
Table. 4.4 The measurement conditions for measure the Au / AET-CdSe/ZnS, 4-layered nanodevice, 30µm * 5µm electrodes combined with CMOS sensing circuit.



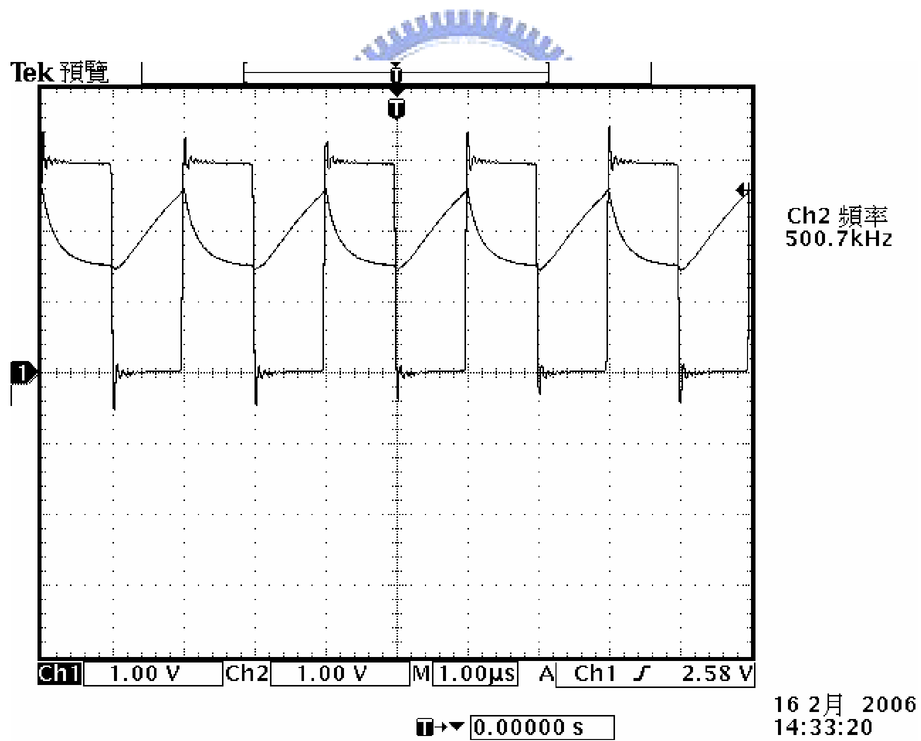
(a) In dark condition, I_d ~ 50 nA, Output = 1.54 V



(b) Under 435 nm illumination, I_d ~ 63 nA, Output = 1.98 V



(c) Under 400 nm illumination, I_d ~ 72 nA, Output = 2.3 V



(d) Under 375 nm illumination, I_d ~ 81 nA, Output = 2.58 V

Fig. 4.22 The measurement results of 4-layered, 30µm * 5µm electrodes, Au / AET-CdSe/ZnS nanodevice combined with CMOS sensing circuit are shown above (a)~(d), where I_d means the current following through the R_d ~ 7.5kΩ. In this measurement, we fixed the V_{bias} ~ 1.70118V and then illuminated with laser source or under dark condition.

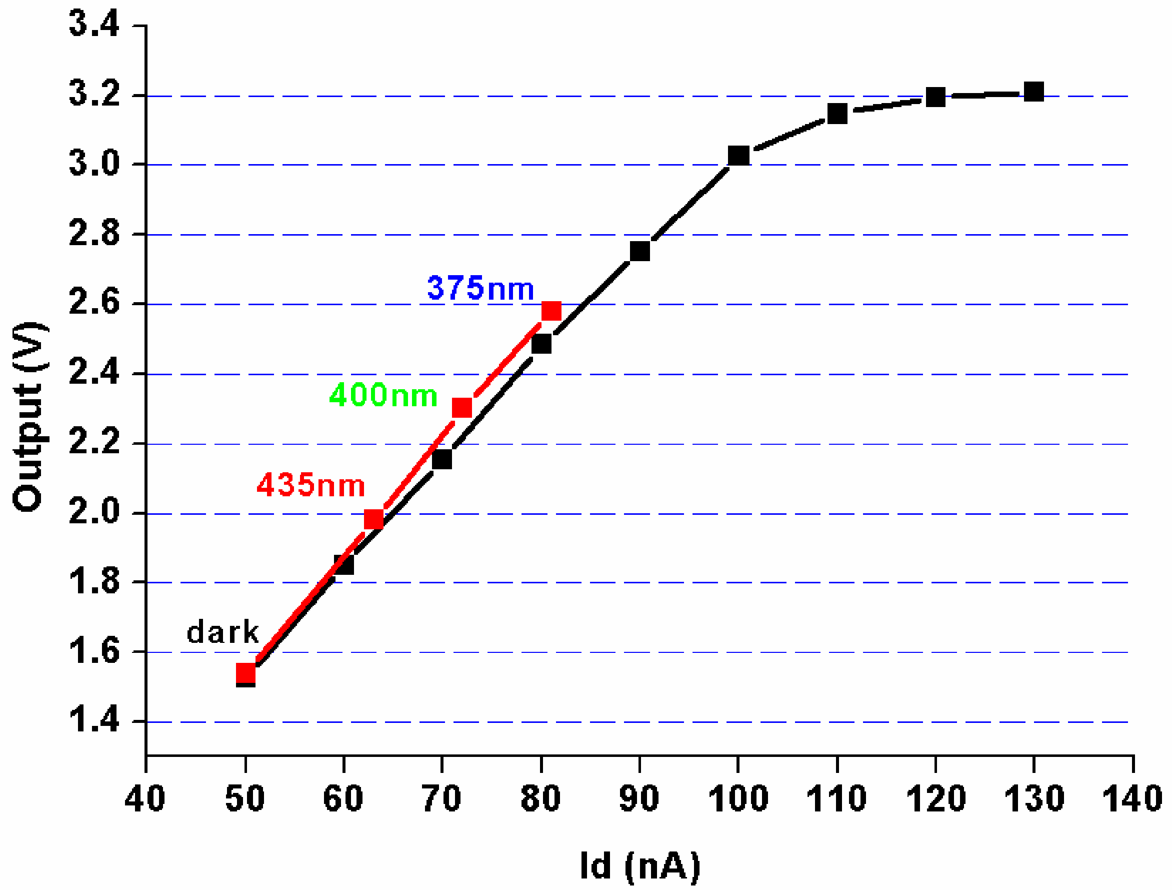


Fig. 4.23 The result of output versus I_d in both HSPICE simulation (dark line) and this measurement of photo-sensing circuit (red line). The power intensity of the laser diodes (375, 400, 435 nm) is $2.5 mW / cm^2$.