國立交通大學

電子工程學系　電子研究所碩士班

碩　士　論　文

具有電壓迴轉率控制之混合式電壓輸入/輸出緩衝器設計

Mixed-Voltage I/O Buffers with Slew-Rate Control in Nanoscale CMOS Processes

研 究 生　：　胡芳綾

指導教授　：　柯明道　教授

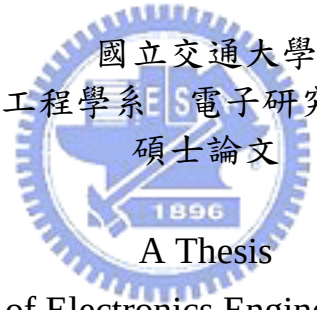
中華民國九十五年七月

具有電壓迴轉率控制
之混合式電壓輸入/輸出緩衝器設計

Mixed-Voltage I/O Buffers with Slew-Rate Control in Nanoscale CMOS Processes

研 究 生： 胡芳綾　　Student ：Fang-Ling Hu

指導教授： 柯明道 教授　　Advisor ：Prof. Ming-Dou Ker



國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master

in

Electronics Engineering

July 2006

Hsin-Chu, Taiwan, Republic of China

中華民國九十五年七月

具有電壓迴轉率控制
之混合式電壓輸入/輸出緩衝器設計

學生: 胡 芳 綾　　指導教授: 柯 明 道 教授

國立交通大學

電子工程學系　電子研究所碩士班

摘要

隨著製程的進步，電晶體所能承受的最大節點電壓，包括閘極-源極電壓 (V_{gs})，閘極-汲極電壓 (V_{gd}) 及汲極-源極電壓 (V_{ds})，必須隨著變小以確保電路有足夠大的生存時間。此外電路的操作速度越來越快，使得接地彈跳 (ground bounce) 越來越嚴重，影響電路的操作表現變差。

在微電子系統中，以較早的 CMOS 製程技術所設計的電路，使用相對於先進製程所能容忍的較大工作電壓。因此在傳輸介面上，以先進製程設計的晶片可能會接收比它正常工作電壓更大的電壓訊號。而混合電壓輸出入緩衝器 (mixed-voltage I/O buffers) 普遍的應用在傳輸介面上，在確保生存時間的情況下接收較高電壓的訊號，並且以較低的操作電壓工作來達到高速、低功率的電路需求。而在製程中使用具較薄閘極氧化層 (gate-oxide) 的電晶體來設計混合電壓輸出入緩衝器可以有較低的成本、較短的電路製造時間以及較高的操作速度。雖然這樣的混合電壓輸出入緩衝器在傳送及接收模式下，不會遭受到閘極氧化層劣化 (gate-oxide degradation) 、熱載子效應 (hot-carrier effect) 的問題，但是當電路在接收高電壓訊號模式轉換為傳送模式的過程，電晶體可能會因熱載子效應劣化。在深次微米製程下，電晶體通道越來越短，使得電場強度變強，因而熱載

子效應更加嚴重，成為設計穩定可靠電路的重要議題之一。

在本篇論文當中，提出了兩個混壓電路設計，無論在接收、傳送模式，或是接收轉傳送的過程都不會有閘極氧化層劣化及熱載子效應的問題。其中一個電路具有抑制熱載子效應的電路，並且可以維持原本電路的電流驅動能力。另一個則是應用阻絕的 NMOS 電晶體 (blocking NMOS) 來避免熱載子效應造成劣化。此兩電路以 0.18-μm 1P6M CMOS 製程技術實現，操作速度高至 266 MHz，並且接收 1.5-V/3.3-V 輸入訊號，傳送 1.5-V 輸出訊號，可與具 PCI-X 2.0 規格應用相容。

在論文最後，提出在混壓介面電路上的控制電壓迴轉率 (slew-rate control)的電路設計。這樣的電路設計可以幫助改善在電源線上的接地彈跳效應，藉此達到較高表現的高速輸出入電路設計 (high speed I/O circuit)。此外，進一步改善接地彈跳效應的電路設計技巧在此篇論文中做了討論及整理。

Mixed-Voltage I/O Buffers with Slew-Rate Control in Nanoscale CMOS Processes

Student: Fang-Ling Hu Advisor: Prof. Ming-Dou Ker

Department of Electronics Engineering & Institute of Electronics
National Chiao-Tung University

ABSTRACT

Transistors fabricated with thin gate oxides are vulnerable to dielectric damage and reliability problems due to excessive electric fields. The difference between operating voltage and maximum allowed terminal voltages including gate-source voltage (V_{gs}), gate-drain voltage (V_{gd}) and drain-source voltage (V_{ds}) of MOS transistors have decreased drastically with the advancement of CMOS process. Also, the ground bounce effects get worse with increasing operating speed. These present special challenges for I/O designers.

With compatibility to the earlier defined standards or interface protocols of CMOS ICs in a microelectronics system, the chips fabricated in the advanced CMOS processes will face to the interface of input signals with voltage levels higher than their normal supply voltage (VDD). As a result, mixed-voltage I/O buffers with only thin-oxide devices have been designed with advantages of less fabrication time in process, less cost and higher operating speed to communicate the advanced circuits with the earlier ones.

Although such mixed-voltage I/O buffers have overcome several problems, such as gate-oxide reliability [1], hot-carrier degradation [2], and the undesired circuit leakage paths between chips [3], in receive mode and transmit mode, they often suffer from hot-carrier degradation during the transition from receiving high-level voltage to transmitting low-level voltage. The hot-carrier induced degradation, however, becomes one of the most important reliability concerns since the MOSFET devices feature extremely short channel length and high electric field in the nano-meter CMOS technologies.

In this thesis, two mixed-voltage I/O buffers realized with only thin-oxide devices to receive 2xVDD-tolerant input signals without suffering the hot-carrier reliability issue are proposed. The mixed-voltage I/O buffer using two-stacked NMOS transistors are designed with new proposed hot-carrier prevented circuit. In this design, the driving capacity will be sustained. The other I/O buffer is designed with two blocking NMOS devices and dynamic gate-controlled circuit to overcome gate-oxide reliability problem and hot-carrier degradation. These two I/O buffers have been fabricated in a 0.18-μm 1P6M CMOS process. From experimental results, the fabricated 2xVDD-tolerant I/O buffers can support the operating speed of up to 266 MHz, which can meet the applications of PCI-X 2.0.

Furthermore, the mixed-voltage I/O buffers with slew-rate control are proposed to reduce ground bounce and achieve high circuit performance in high-speed interfaces. The design based on the mixed-voltage I/O buffer with blocking NMOS devices and dynamic gate-controlled circuit has been fabricated in a 0.18-μm 1P6M CMOS process. The other circuit techniques to further reduce ground bounce are also introduced in last part of the thesis.

誌謝

碩士二年轉眼間就要畢業了，在這二年當中，首先要感謝的是我的指導教授，柯明道博士的殷殷教誨，在研究上給予指導與建議，遇到挫折時給予我鼓勵，使我對自己更有信心；教導我們做事情要抱持嚴謹的態度，待人處事要圓融等，平常也會關心我們的生活狀況，亦師亦友，讓我獲益良多。此外，由於老師的努力，讓我們常有晶片驗證的機會，在研究上不會有後顧之憂，也常常為了修改我們的論文而廢寢忘食。因此，我要向柯明道博士致上我最深的謝意，謝謝您讓我有今天的成長。

其次我要感謝已經從本實驗室畢業的莊凱嵐學長，在我剛進實驗室時，耐心地指導我量測、電路設計等，給予我很大的幫助，使我在碩士生涯一開始不至於手足無措。特別感謝陳世倫博士這二年來給予我研究上最大的幫助，指導我電路設計、模擬與量測，給予我建議使我不限於瓶頸，謝謝您的幫助使得我能夠順利完成碩士論文。而在這段求學的過程中，『工研院系統晶片技術發展中心』的『電路設計部』、『混合式積體電路設計部』及『高頻積體電路設計部』，給予我許多研究資源，從實驗晶片的下線及量測設備的支援協助，使我實驗順利完成。在此特別感謝吳文慶組長、簡丞星副組長、陳世宏、黃柏獅、徐育達、張伯瑋、梁詠智、洪項彬、黃清吉、甘瑞銘、劉嘉俊、林崇偉、吳思賢、余永凌等諸位學長以及田季平小姐、熊櫻霞及劉玉珠女士，在實驗、量測設備的協助以及量測上遇到困難時，所給予我的幫忙。也感謝『奈米晶片與系統實驗室』的許勝福、顏承正、陳榮昇、陳世宏、張瑋仁、蕭淵文、吳建樺、周宗信、黃靖驊、王資閔、李宇軒、廖宏泰等諸位實驗室學長以及學弟們，在各方面給予我許多幫助使我能順利完成碩士論文。感謝『奈米晶片與系統實驗室』及助理卓慧貞小姐給予我在研究上的資源及行政上的幫助，讓我完成學業。

接著要感謝的是一起打拼的同學們，怡凱、佳惠、泰翔、志遠、宛儀、豪傑、汝玉、志賢、立龍、國慶、允斌、仲朋及必超，大家一起修課、熬夜，出遊、拍照玩鬧，讓我的碩士生活充滿歡樂；互相扶持，加油打氣讓我能充電再繼續努力。謝謝蘭友會的伙伴們，毛龍、小黑、柏村、黃帝、阿睿、卡球和胖中，謝謝你們一直以來的陪伴。

最後要致上萬分的感謝，謝謝我的父母、家人，感謝他們一直以來的關心與支持，栽培我讀書讓我有今天的成就。最後祝福我的師長、家人、朋友及學弟妹們事事順心、身體健康。

胡芳綾

九十五年七月

CONTENTS

TABLE CAPTIONS

FIGURE CAPTIONS


E
S
A
1896

Chapter 1
Introduction

1.1 MOTIVATION

With new generations of CMOS technologies, the transistors' dimensions have been scaled down to reduce the silicon cost, as well as, to increase circuit performance and operating speed. The thickness of gate oxide becomes much thinner in order to reduce the core power supply voltage (VDD) for resulting in lower power consumption. In the meanwhile, the maximum tolerable voltage across the transistor terminals (drain, source, gate, and bulk) should be correspondingly decreased to ensure lifetime.

With compatibility to the earlier defined standards or interface protocols of CMOS ICs in a microelectronics system, the chips fabricated in the advanced CMOS processes will face to the interface of input signals with voltage levels higher than their normal supply voltage (VDD). Such mixed-voltage I/O interfaces must be designed to overcome several problems, such as gate-oxide reliability [1], hot-carrier degradation [2], and the undesired circuit leakage paths between chips [3]. Since the mixed-voltage I/O buffer communicates ICs in advanced process with those in earlier process, the mixed-voltage I/O buffers in this thesis will be designed to meet PCI-X 2.0 specification which is compatible with the prior PCI standards.

The hot-carrier induced degradation, however, becomes one of the most important reliability concerns since the MOSFET devices feature extremely short channel length and high electric field in the deep sub-micron technologies. In the hot carrier effect, carriers are accelerated by the channel electric fields and become trapped in the oxide.

Such hot-carried induced degradation causes a lot of device degradation, such as the deviation of threshold voltage (V_{th}), transconductance (g_m), and linear (I_{DLIN}) and saturation (I_{DSAT}) drain current [4]. In time, substantial device parameter degradation can occur, resulting in device failure. Thus, it is an important issue to provide a robust circuit design in circuit techniques with sufficient lifetime.

In high-speed interface, the output buffer is a major contributor to the pin-to-pin delays because of output loading as well as package and board parasitics. The channel widths of output buffer are always increased to have high driving capacity and high speed, which results in large power/ground noise due to outputs switching simultaneously. Since the input pads are connected to the same power/ground bus, power/ground noise must be well controlled to avoid any false switching. Even though the internal power/ground buses are separated from the external (I/O buffers) power/ground buses, they are connected through a VDD/VSS package plane in multilayer package. Therefore, the out buffer must be designed with considerations of power/ground noise to achieve high performance.

1.2 MIXED-VOLTAGE I/O BUFFERS

Fig. 1.1 shows the block diagram of a bidirectional input/output (I/O) buffer in general. As the output enable signal OE is high (VDD), the mixed-voltage I/O buffer is operating in transmit mode to transmit output signals from Dout to I/O PAD. On the other hand, the mixed-voltage I/O is operating in receive mode to receive input signals from I/O PAD to Din (internal circuit) if the OE is low (0V). In dual-oxide (thin-oxide and thick oxide) CMOS process, the core circuits usually use thin-oxide devices using low power supply voltage to reduce power consumption and silicon area while the interface circuits use thick-oxide to tolerant higher voltages and prevent

reliability problems in traditional mixed-voltage I/O buffers. A mixed-voltage I/O buffer with dual-oxide devices and an external n-well bias voltage is shown in Fig. 1.2. The mixed-voltage I/O buffer transmits GND-to-VDD (low voltage level) output signals and receives GND-to-VDDH (high voltage level) input signals. The pre-driver circuit generates control signals of output transistors MN and MP. In the mixed-voltage I/O buffer, the output transistors, gate-tracking circuits, and input circuit, INV, are thick-oxide devices to overcome reliability problems. The pre-driver circuit uses thin-oxide devices since the input data come from internal core circuit which uses low voltage level. In order to avoid leakage current path from the I/O PAD to the power supply (VDD) through the parasitic drain-to-well pn-junction diode in the pull-up PMOS device, MP, a higher external voltage (VDDH) is used to bias the bulk of the MP. In addition, a gate-tracking circuit is required to avoid the leakage current path induced by the incorrect conduction of the MP. Such mixed-voltage interface applications with dual-oxide devices can successfully overcome the gate-oxide reliability and hot-carrier degradation problem [5]-[6].

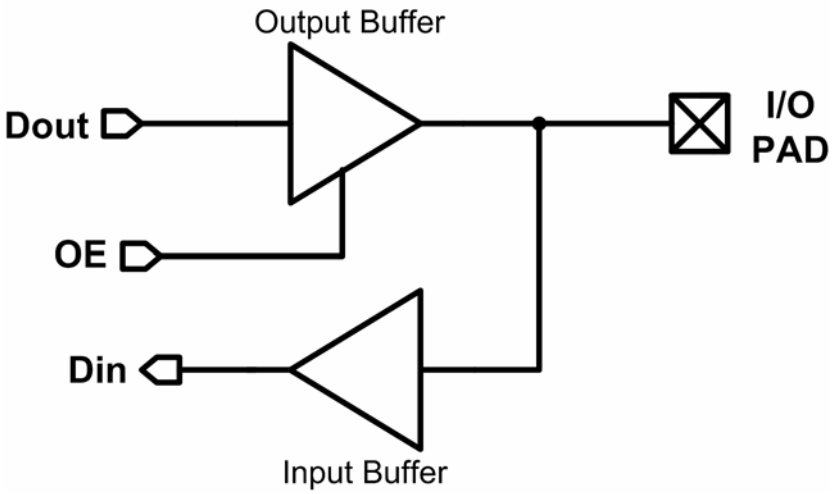


Fig. 1.1 Block diagram of bidirectional I/O buffer.

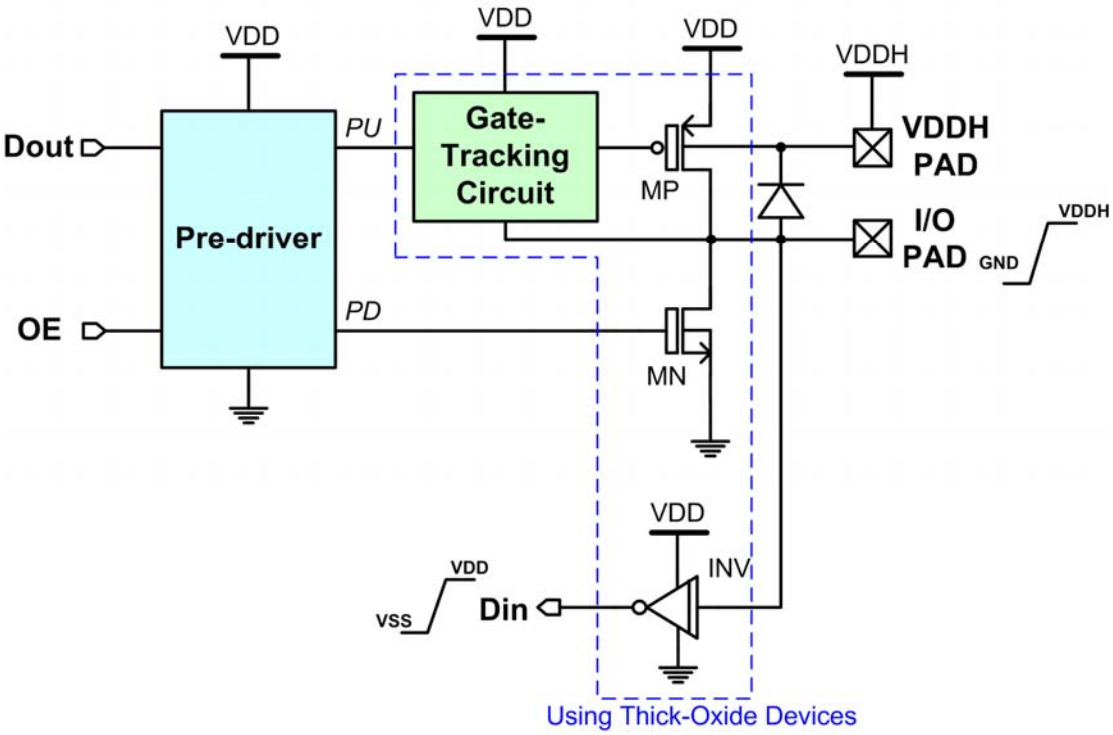


Fig. 1.2 Block diagram of a mixed-voltage I/O buffer with dual-oxide devices and an external n-well bias voltage.

Although the mixed-voltage I/O buffers with dual-oxide devices can successfully solve aforementioned problems, there are some drawbacks in these mixed-voltage I/O buffers. Fist of all, an extra pad and another power supply (VDDH) are required for the external bias voltage, which results in the increase of silicon area and cost. Second, the driving capacity is decreased due to higher threshold voltage of thick-oxide device when the gates of output transistors are controlled by pre-driver circuit with thin-oxide devices. Thirdly, the threshold voltage of the pull-up PMOS device (MP) is also increased since the bulk of the pull-up PMOS device (MP) is connected to a higher voltage (VDDH), which results in body effect. Because the driving capacity is decreased, the larger device dimension is required for the pull-up PMOS device to achieve the desired driving specifications. As a result, the silicon area in such I/O buffers is increased. Moreover, the manufacturing time of thick-oxide device is even

three times large than that of thin-oxide device. For these aforementioned reasons, the mixed-voltage I/O buffer with dual-oxide devices and an external n-well bias is unsuitable for the low-cost commercial ICs. Considering these limitations, several mixed-voltage I/O buffers with only thin-oxide devices have been reported in [7]-[10]. A mixed-voltage I/O buffer with a 2xVDD tolerant voltage is often designed using cascode transistors without thick-oxide devices. Fig. 1.3 shows a simplified mixed-voltage I/O buffer with two-stacked transistors to be tolerant of 2xVDD, where pull-down signal (PD) and pull-up signal (PU) are the controlled signals from pre-driver. In Fig. 1.3, the input circuit and pull-up network of the mixed-voltage I/O circuit are simplified into block diagrams for convenience. The 2xVDD tolerant mixed-voltage I/O buffers typically receive 2xVDD input signals and transmit 1xVDD output signals.

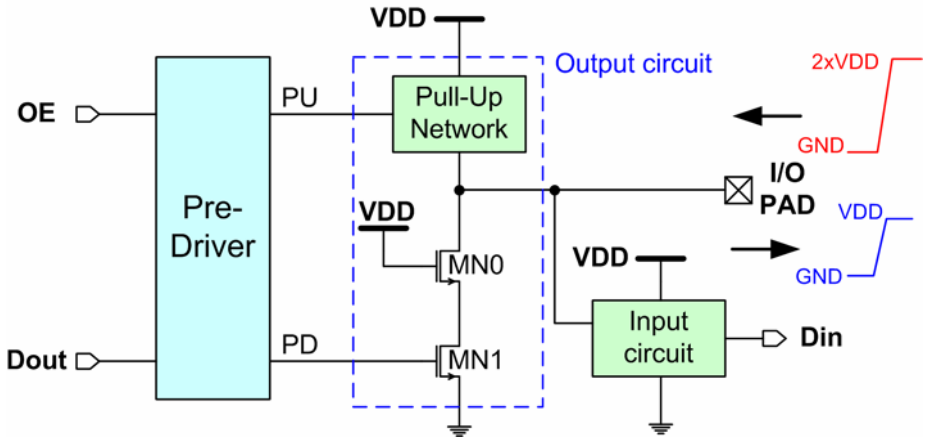


Fig. 1.3 Simplified mixed-voltage I/O buffer with two-stacked transistors.

1.3 HOT-CARRIER EFFECT

The mechanism of hot-carrier effect and the hot-carrier issue in the mixed-voltage I/O buffers are described in the following.

1.3.1 The Mechanism of Hot-Carrier Effect

A cross section of a typical enhancement-mode n-channel MOS (NMOS) transistor is shown in Fig. 1.4 where the source terminal is connected to ground. Heavily doped n-type source and drain regions are fabricated in a p-type substrate. A thin layer of silicon dioxide is grown over the substrate material and a conductive gate material covers the oxide between source and drain. In operation, the gate-source voltage modifies the conductance of the region under the gate, allowing the gate voltage to control the current following between source and drain. Now in Fig. 1.4, the positive voltages, V_G and V_D, are applied to the gate and drain, respectively. An inversion layer is produced as the V_G is equal to or larger than the V_{th} of NMOS device. When the value of V_D is increased, the induced conducting channel narrows at the drain end. The induced electron charge at the drain end approaches zero as VD approaches (V_G - V_{th}). That is, the channel is no longer connected to the drain when $V_D > V_G - V_{th}$, which is known as pinch-off. At this time, the electric field starts rise dramatically at the pinch-off point of the NMOS device. In the high electric field, carriers are accelerated to high velocities, reaching a maximum kinetic energy (hot) near the device drain. If the carrier energy is high enough, impact ionization can occur, creating electron-hole pair. The generated electrons called secondary electrons tend to be swept to the drain and generated holes called secondary holes swept into the substrate in the NMOS device.

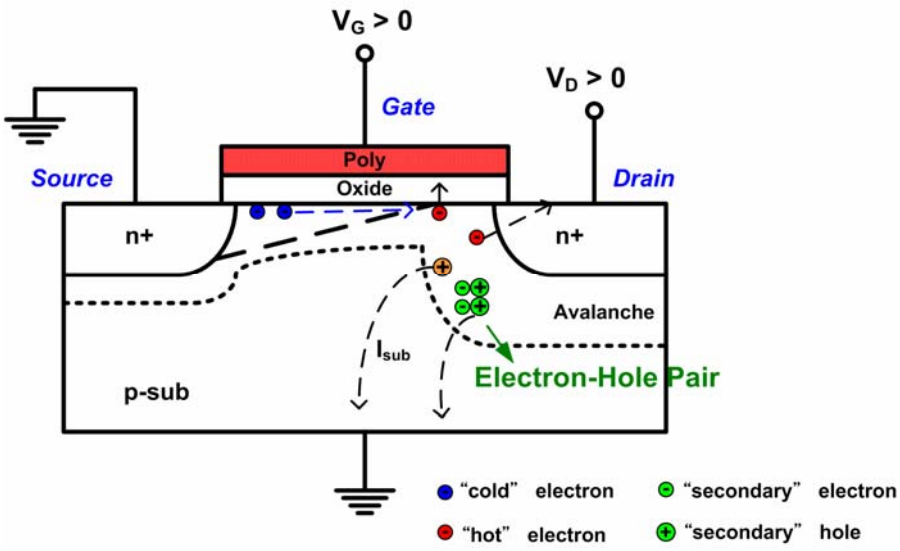


Fig. 1.4 The diagram of hot-carrier effect.

Some of the electrons generated in the space charge region are attracted to the oxide due to the electric field induced by the positive gate voltage, V_G. These generated electrons have energies far greater than the thermal-equilibrium value and are called hot electrons (or hot carriers) [11]. If the electrons have energies on the order of 1.5 eV, they may be able to tunnel into the oxide. In some cases the generated holes and electrons can attain enough energy to surmount the Si–SiO_2 barrier and become trapped in the gate oxide. In general, injection from Si into SiO_2 is much more likely for hot electrons than for hot holes because (a) electrons can gain energy from the electric field much more readily than holes due to their smaller effective mass, and (b) the interface energy barrier is larger for holes (≈4.6 eV) than for electrons (≈3.1 eV) [12]. The charge trapping in interface states causes a shift in threshold voltage, additional surface scattering, and reduced mobility. The hot electron charging effects are continuous processes, so the device degrades over a period of time. There are several techniques used to reduced maximum electric field in process and device structures, such as the lightly doped drain (LDD) structure [11]

and grooved gate MOSFETs [13]. In this thesis, the mixed-voltage I/O buffers are designed without suffering hot-carrier effect in circuit techniques.

1.3.2 Hot-Carrier-Induced Lifetime Issue

The hot-carrier degradation effect depends among others on the transistor's length and its biasing conditions [14]:

- The relation between the drain–source voltage and lifetime is exponential:

$$\tau_{life} \propto \exp(A/V_{ds}) \tag{1-1}$$

  , where A is 80-120 V for deep submicron processes. This relation assumes worst-case settings of the gate-source voltage.

- The length-lifetime dependency is relatively weak:

$$\tau_{life} \propto L^{B} \tag{1-2}$$

  , where B = 1-5.

- The relation between gate-source voltage and lifetime is more complex. For low gate-source voltages the transistor is "off" resulting in no current and hence in no hot carriers. For very high gate-source voltages (and fixed rain–source voltage) the transistor is in the linear region resulting in no hot carriers either. Somewhere in the middle, both the drain current is large and the transistor is well in saturation. In this region, the hot-carrier degradation is worst and hence the lifetime is poorest.

A typical hot-carrier-based lifetime versus biasing plot for a minimum length transistor is given in Fig. 1.5, where $V_{dd,nom}$ is the normal power supply voltage in a given process. Note that especially the drain-source voltage of a MOS transistor

strongly affects the lifetime. It is recommended that the maximum terminal voltages of a MOS transistor (V_{gs}, V_{gd} and V_{ds}) which can be applied to the device at worst case DC stress conditions are below $V_{dd,nom}$ to ensure a device lifetime of 10 years [15].

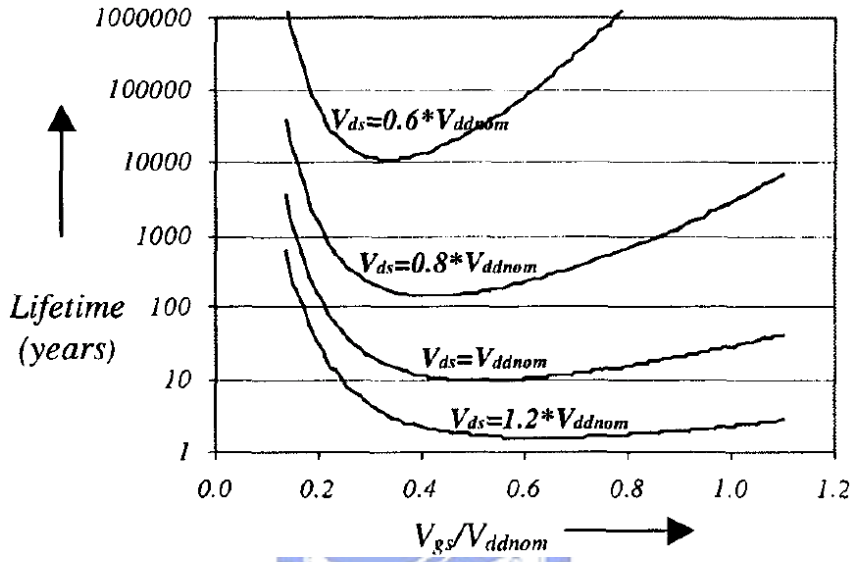


Fig. 1.5 Channel-hot-carrier lifetime as a function of V_{ds} and V_{gs}. (typical behavior for 0.25-μm CMOS process)

1.3.3 Hot-Carrier Issue in Typical Mixed-Voltage I/O Buffers

The hot-carrier induced degradation or gate-oxide reliability in typical 2xVDD-tolerant I/O buffer shown in Fig. 1.3 may exist in the following two states: (1) the state of receiving 2xVDD input signal, and (2) the state of a transition from receiving 2xVDD input signal to transmitting 0-V output signal.

When such 2xVDD-tolerant I/O buffer receives 2xVDD input signals, PU and PD signals are kept at VDD and 0 V, respectively, to disable the output circuit. Since the transistor MN1 in Fig. 1.3 is turned off, the transistor MN0 is weakly "on". This results in a voltage of about VDD at the source of MN0. In each of these two-stacked transistors, the voltages drop across the gate-oxide and the drain-source voltage are

both lower than or equal to the supply voltage (VDD). Therefore, there is neither hot-carrier degradation nor gate-oxide overstress issues in the mixed-voltage I/O buffer when receiving 2xVDD input signal.

When the 2xVDD-tolerant I/O buffer has the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the I/O PAD originally has a voltage of 2xVDD before being pulled down. At this transition moment, the transistor MN1 is turned on by PD signal from pre-driver, and the transistor MN0 is subsequently switched on when its source is pulled down by the MN1. The voltage at the drain of MN1 can be approximated as the saturation drain voltage (V_{DSAT}) [16]. For example, the voltage at the source of the transistor MN0 is about ~0.5V in a 0.18-μm CMOS process. Since the original 2xVDD voltage at I/O PAD is not pulled down immediately, the drain-source voltage of MN0 would be larger than the normal supply voltage (VDD) during this transition, which results in the significant hot-carrier degradation on the transistor MN0. From this point, the traditional I/O buffer with two-stacked transistors in Fig. 1.3 is difficult to build a reliable 2xVDD-tolerant I/O buffer with only 1xVDD devices in a given CMOS technology, unless an additional circuit is provided to prevent such hot-carrier degradation during signal transition.

There are several ways to boost the voltage handling capabilities of the circuit in Fig. 1.3 without using any process modification include:

- using different aspect ratios for the lower and for the cascode transistor;
- using longer transistors to limit channel hot-carrier degradation;
- using a nonstationary gate voltage for the cascode transistor;
- using more stacked transistors.

In this thesis, an external circuit is proposed to suppress hot-carried degradation without increasing the number of stacked transistors.

1.4 BRIEF INTRODUCTION TO PCI-X 2.0 [17]

PCI-X 2.0 is a new, higher speed version of the conventional PCI standard, which supported signaling speeds up to 533 megatransfers per second (MTS). Migration to PCI-X 266 and PCI-X 533 is further simplified by retaining hardware and software compatibility with previous generations of PCI and PCI-X. As a result, new designs can immediately connect with hundreds of PCI and PCI-X products that are currently available.

There are 4 speed grades in the PCI-X 2.0 specification: PCI-X 66, PCI-X 133, PCI-X 266, and PCI-X 533. The PCI-X 66 and PCI-X 133 speed grades were included in the PCI-X 1.0 specification. 100MHz PCI-X has been implemented in the market by using PCI-X 133 adapter cards. Both PCI-X 266 and PCI-X 533 are new to PCI-X 2.0; they are the 266MHz and 533MHz versions of the specification. PCI-X 266 and PCI-X 533 devices are electrically compatible with 3.3V and 1.5V I/O buffers only. They are not compatible with 5V PCI. The specification for PCI-X 266 in the mixed-voltage I/O buffer designed in this thesis is summarized in Table 1.1.

Table 1.1
The specification for PCI-X 266 in mixed-voltage I/O buffer

Operating Modes	Voltage swing at I/O PAD
Receive mode	1.5V/3.3V
Transmit mode	1.5V

1.5 THESIS ORGANIZATION

In chapter 2, two prior designs of mixed-voltage I/O buffers which tolerate 2xVDD signals will be introduced. Thesis two mixed-voltage I/O buffers are designed

with only thin-oxide devices in a given CMOS process and do not suffer gate-oxide degradation and hot-carrier degradation in both steady states of receive mode and transmit mode. The I/O buffers, however, suffer hot-carrier degradation in transitions from switching receive mode to transmit mode which will be pointed out in chapter 2. Two new mixed-voltage I/O buffers without suffering hot-carrier degradation in transitions will be proposed in chapter 3. The simulation and experimental results are also shown in this chapter. In chapter 4, the mixed-voltage I/O buffers proposed in chapter 3 are redesigned with slew-rate control to improve ground bounce effects. Besides, some techniques for further improving ground bounce are pronounced. The last chapter recapitulates the major consideration of this thesis and concludes with suggestion for future investigation.

Chapter 2

Prior Designs on Mixed-Voltage I/O Buffer with a Tolerant Voltage of 2xVDD

In this chapter, two mixed-voltage I/O buffers reported in [10] and [18] are introduced before the proposed reliable mixed-voltage I/O buffers in the thesis. These two mixed-voltage I/O buffers are designed to be tolerant of 2xVDD.

2.1 PRIOR DESIGN I: A MIXED-VOLTAGE I/O BUFFER WITH GATE-TRACKING CIRCUIT AND DYNAMIC N-WELL BIAS CIRCUIT

2.1.1 Design Concept

Fig. 2.1 shows the mixed-voltage I/O buffer realized with thin-oxide devices, a dynamic n-well bias circuit, and a gate-tracking circuit [7]-[8], [19]-[22]. The stacked NMOS devices, MN0 and MN1, are used to avoid the high-voltage overstress on their gate oxide. The gate-tracking circuit shown in Fig. 2.1 is used to prevent the leakage current path which is resulted from the incorrect conduction of the pull-up PMOS device when the input signal is higher than VDD. As the mixed-voltage I/O buffer is operating in the transmit mode, the gate-tracking circuit must transfer the signal from the pre-driver circuit to the gate terminal of the pull-up PMOS device, MP0, exactly. In the receive mode (tri-state input mode) with an input signal of 2xVDD, the gate-tracking circuit will charge the gate terminal of the MP0 to 2xVDD to turn off the MP0 completely, and to avoid the leakage current from the I/O pad to the power supply (VDD). On the contrary, the gate-tracking circuit will keep the gate terminal of the MP0 at VDD to turn off the MP0 completely, and to prevent the overstress on the

gate oxide of the MP0 when the 0-V input signal is received from I/O PAD. Moreover, the dynamic n-well bias circuit shown in Fig. 2.1 is designed to prevent the leakage current path due to the parasitic drain-to-well pn-junction diode in the pull-up PMOS device MP0. In the transmit mode, the dynamic n-well bias circuit must keep the floating n-well bias at VDD so that the threshold voltage of the pull-up PMOS device isn't increased due to the body effect. In the receive mode with an input signal of 2xVDD, the dynamic n-well bias circuit will charge the floating n-well to 2xVDD to prevent the leakage current from the I/O pad to the power supply (VDD) through the parasitic pn-junction diode. On the other hand, the dynamic n-well bias circuit will bias the floating n-well at VDD when the input signal at the I/O pad is 0V.

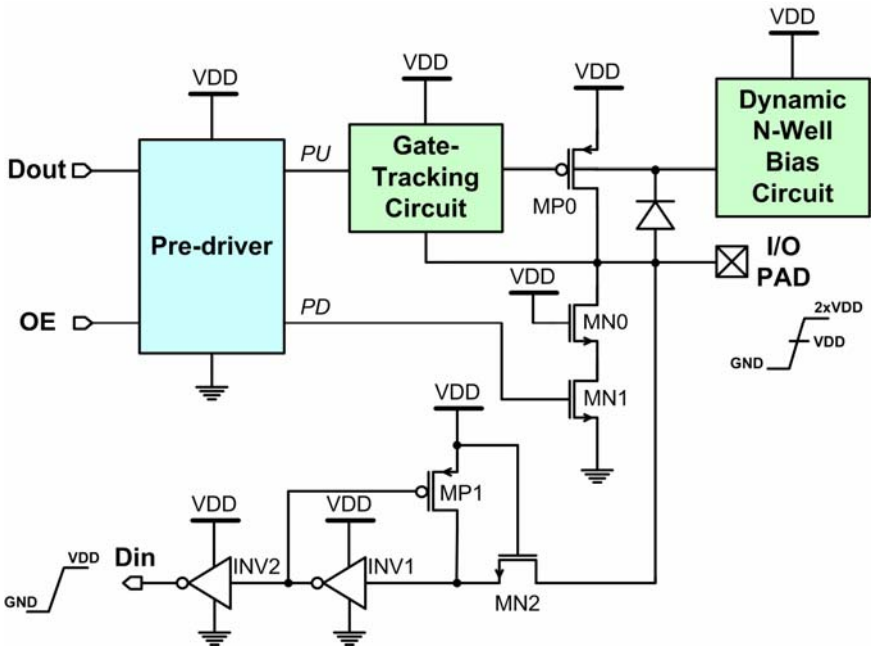


Fig. 2.1 Basic design concept for mixed-voltage I/O buffer realized with only thin-oxide devices.

As shown in Fig. 2.1, the extra transistors, MN2 and MP1, which are compared to Fig. 1.2, are added in the input circuit. The transistor MN2 is used to limit the voltage level of input signal reaching to the gate oxide of inverter INV1. The

transistor MP1 is used to prevent unnecessary leakage current in the inverter INV1. Because the gate terminal of transistor MN2 is connected to the power supply voltage (VDD), the input terminal of inverter INV1 will rise up to "VDD-V_{th}" when the input signal at the I/O pad is 2xVDD in the receive mode. The transistor MP1 will pull the input node of inverter INV1 up to VDD when the output node of inverter INV1 is pulled down to 0V. Therefore, the gate-oxide reliability problem of the input buffer can be solved. Moreover, the circuit implementation of pre-driver composed of a NAND gate and NOR gate is shown in Fig. 2.2. The operations of pre-driver are list in Table 2.1. When the output enable signal OE is 0V, the mixed-voltage I/O buffer is operated in receive mode. The pull-up signal (*PU*) and pull-down signal (*PD*) are set to VDD and 0V, respectively, to turn off pull-up device and pull-down devices. On the contrary, both *PU* and *PD* are set to VDD to turn off pull-up device and turn on pull-down devices, respectively, in transmitting 0-V output signal, and they are set to 0V to switch on pull-up device and switch off pull-down devices, respectively, in transmitting VDD output signal.

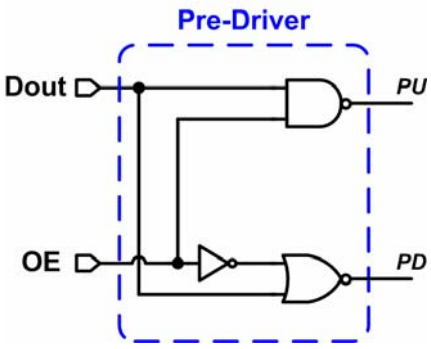


Fig. 2.2 The circuit implementation of pre-driver.

Table 2.1
Operations of the pre-driver

Operating Modes	OE	Signals at I/O PAD	PU	PD
Receive	0V	X	VDD	0
Transmit	VDD	Low (0V)	VDD	VDD
Transmit	VDD	High (VDD)	0V	0V

2.1.2 Circuit Description

Fig. 2.3 shows the mixed-voltage I/O buffer with the dynamic n-well bias circuit and gate-tracking circuit proposed in [10]. For clear illustration, this mixed-voltage I/O buffer is called GTCMXIO in this thesis. When the output control signal OE is at VDD (logic "1"), the mixed-voltage I/O buffer is operated in the transmit mode. The signal at the I/O pad rises or falls according to signal Dout, which is controlled by the internal circuits of IC. The pull-down signal, *PD*, produced by pre-driver is directly connected to the gate terminal of the pull-down NMOS device, MN1. The pull-up signal, *PU*, is connected to the gate terminal of the pull-up PMOS device, MP0, through the gate-tracking circuit which is composed of NMOS transistors MN2-MN4 and PMOS transistors MP2, MP3 and MP5. The transistors MN2 and MP2 comprise a transmission gate. The transistor MN3 in Fig. 2.3 is used to protect the transistor MN4 from gate-oxide reliability problem. The dynamic n-well bias circuit is composed of transistors MP4 and MP6. If the mixed-voltage I/O buffer is operating in transmit mode (OE = VDD), the gate terminal of MP4 will be biased at 0V to bias the floating n-well at VDD by turning on the transistor MP4. At this time, the *PU* signal is fully transmitted to the gate terminal of the pull-up PMOS device MP0 through the

transmission gate, MN2 and MP2. As 0-V output signal is transmitted, the *PD* signal is set to VDD to turn on the transistor MN1. In the meanwhile, the *PU* signal is set to VDD to turn off the pull-up device MP0. Consequently, the voltage at the I/O pad and the gate voltage of transistor MP5 are discharged to 0V through transistors MN0 and MN1. Transistor MP5 is turned on until the gate terminal of transistor MP2 is discharged to $|V_{tp}|$, where V_{tp} is the threshold voltage of PMOS device, through transistors MN3 and MN4.

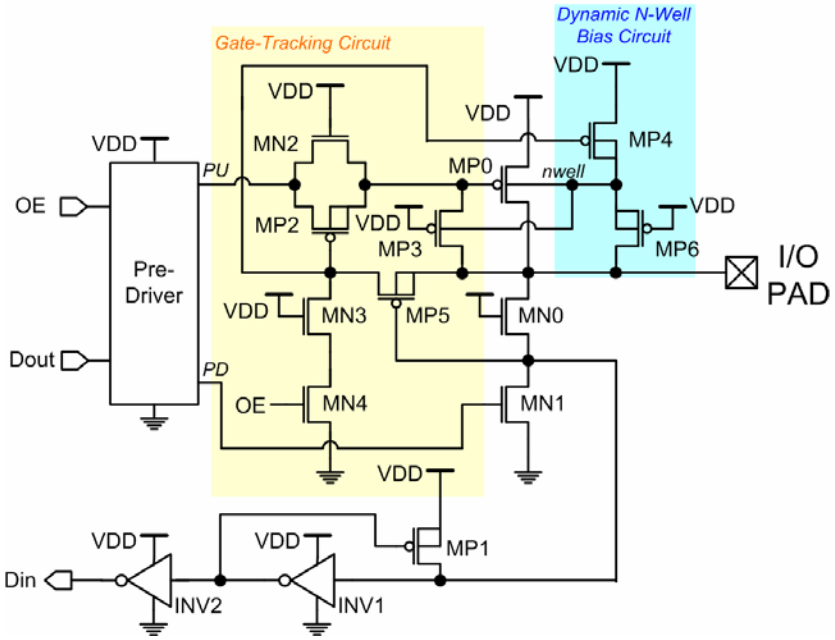


Fig. 2.3 The mixed-voltage I/O buffer with gate-tracking circuit and dynamic n-well bias circuit proposed in [9].

When the proposed I/O buffer is operated in the receive mode, the *PU* and *PD* signals are kept at VDD and 0V, respectively, to turn off transistors MP0 and MN1. Signal Din rises or falls according to the signal at the I/O pad in the receive mode. In order to prevent the undesired leakage current from the I/O pad to the power supply (VDD) through the pull-up PMOS device MP0, transistor MP3 is used to track the signal at the I/O pad and to control the gate voltage of transistor MP0. When the

voltage level at the I/O pad exceeds "VDD+$|V_{tp}|$," such as 2xVDD, transistor MP3 is turned on to charge the gate terminal of transistor MP0 up to 2xVDD. Thus, transistor MP0 is completely turned off to prevent the leakage current through its channel. If a 0-V input signal is received at I/O PAD, the floating n-well is biased at VDD through the transistor MP4. As the mixed-voltage I/O is operating in the receive mode with an input signal of 2xVDD, another PMOS device MP6 is turned on to bias the floating n-well at 2xVDD. Also, transistor MP4 is turned off to prevent the leakage path by pulling up the gate terminal of MP4 to 2xVDD through transistor MP5. As a result, there is no leakage current path from the I/O pad to the power supply (VDD). Whenever the proposed mixed-voltage I/O buffer is in the transmit mode or the receive mode, the floating n-well is biased at VDD or 2xVDD directly. Thus, the subthreshold leakage problems do not occur in this proposed I/O buffer. Besides, transistor MP5 is also turned on to keep transistor MP2 off in order to prevent another leakage path from the gate terminal of transistor MP0 to the *UP* signal when the signal at the I/O pad is 2xVDD.

Transistors MN0 and MP1 with inverters INV1 and INV2 are used to transfer the input signal from the I/O pad to the internal node Din in the receive mode. Transistor MN0 is used to limit the voltage level of input signal reaching to the gate oxide of inverter INV1. The signal at the I/O pad can be successfully transferred to the internal input node Din. This I/O buffer can be correctly operated with neither gate-oxide reliability problem nor any circuit leakage issue in the receive mode.

2.1.3 Hot-Carrier Issues in GTCMXIO

Although the mixed-voltage I/O buffer proposed in [10] does not suffer gate-oxide degradation and leakage issue, it still suffers hot-carrier degradation under the I/O signal transitions. During the transition from receiving 2xVDD input signal to

transmitting 0-V output signal, the transistor MN0 suffers the hot-carrier degradation mentioned in chapter 1. The hot-carrier degradation will also occur on MN3 device in this traditional 2xVDD-tolerant I/O buffer during this transition since the gate terminal of MP4 is originally biased at 2xVDD through transistor MP5. Besides, the transistors MN2 and MP2 also suffer hot-carrier degradation during the transition from receiving 2xVDD input signal to transmitting VDD output signal since the gate terminal of transistor MP0 is initially kept at 2xVDD but the *PU* signal has been pull down to 0V by the pre-driver to turn on transistor MP0.

2.2 PRIOR DESIGN II: A MIXED-VOLTAGE I/O BUFFER WITH BLOCKING NMOS AND DYNAMIC GATE-CONTROLLED CIRCUIT

2.2.1 Circuit Description

Fig. 2.4 depicts the mixed-voltage I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit proposed in [18], which is called SBNMXIO in this thesis. In Fig. 2.4, VDDH has a high voltage of 2xVDD, which can be generated by the on-chip charge pump circuit [23] or other high-voltage generators. Transistor MNS1 is used to protect the conventional I/O buffer from the high-voltage overstress. The operations of the dynamic gate-controlled circuit in the I/O buffer with blocking NMOS are listed in Table 2.2. When the I/O buffer is in the receive mode, the gate terminal of MNS1 (node 2) is biased at VDD by the dynamic gate-controlled circuit, whereas the pull-up device MP0 and pull-down device MN0 are both turned off by the pre-driver. At this moment, if an input signal of logic ‘0’ (0V) is received from the I/O PAD, node 1 is discharged to 0 V through the transistor MNS1, and this input signal can be successfully transferred to the node Din. When a logic ‘1’ (VDDH) signal is received at the I/O pad, the gate terminal of transistor MNS1 is still biased at VDD, so the

voltage on node 1 is pulled to "VDD−V_{th}". A feedback device MP1 is added to restore the voltage level on node 1 to VDD, which avoids the undesired static dc current through the inverter INV1. In this design, MNS1, MP1, and inverter INV1 can convert the VDDH input signal to VDD signal successfully. Therefore, MNS1 can protect the I/O buffer without suffering high-voltage overstress in both steady states of transmit mode and receive mode.

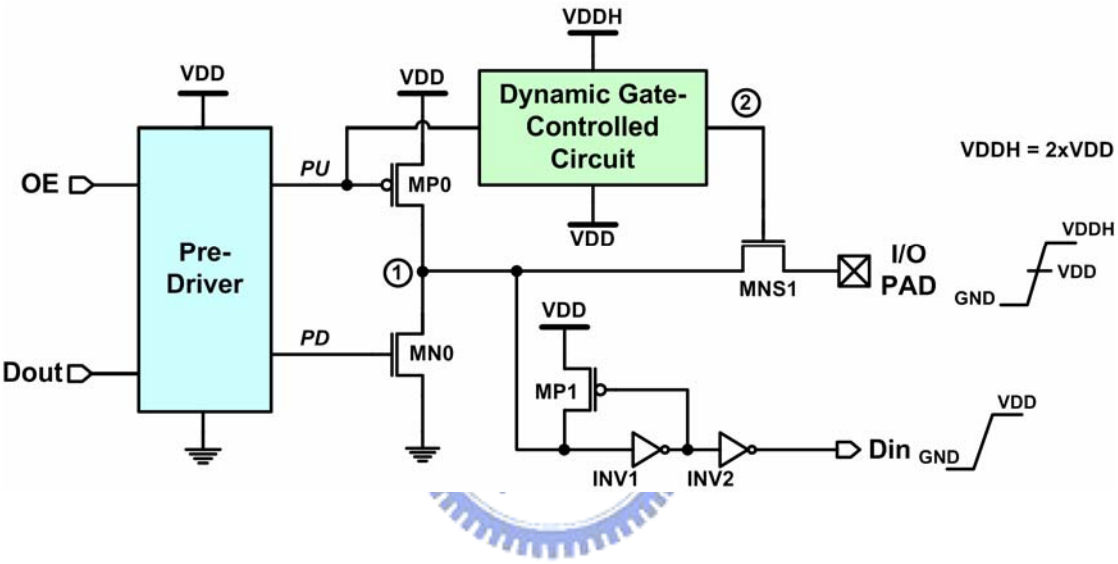


Fig. 2.4 The mixed-voltage I/O buffer with a blocking NMOS and a dynamic gate-controlled circuit.

Table 2.2
Operations of the dynamic gate-controlled circuit in the mixed-voltage I/O buffer with blocking NMOS [18].

Operating Modes	Signals at I/O PAD	V_g of MP0 (*PU*)	V_g of MNS1 (Node 2)
Receive	X	VDD	VDD
Transmit	Low (0V)	VDD	VDD
Transmit	High (VDD)	0V	VDDH (2xVDD)

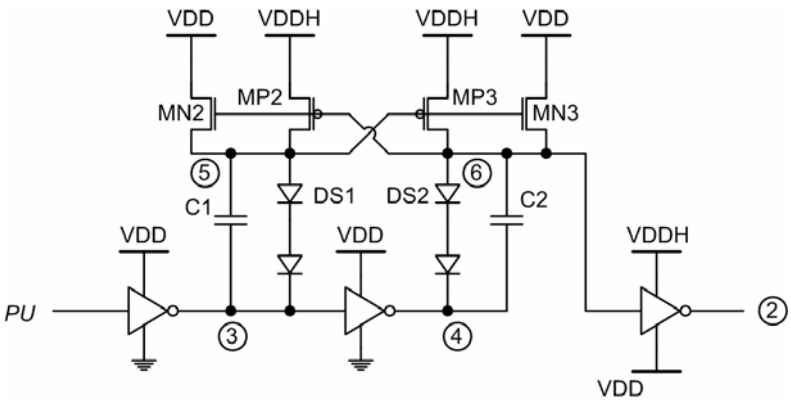


Fig. 2.5 Circuit implementation of the dynamic gate-controlled circuit in the SBNMXIO.

Fig. 2.5 depicts the dynamic gate-controlled circuit of the I/O buffer in Fig. 2.4, where MP2 and MP3 are designed with the cross-coupled structure. If the gate voltage of MP2 (or MP3) is pulled down, this transistor is turned on and pulls up the gate voltage of the other transistor to VDDH (2xVDD) to turn it off. For example, if the voltage on node 5 is lower than "VDDH−$|V_{tp}|$" and the voltage on node 6 is VDDH, MN2 is turned on to keep the node 5 at VDD. Capacitors C1 and C2 are used to couple the signals from nodes 3 and 4 to nodes 5 and 6, respectively. The voltages across these capacitors are always VDD, because the voltage levels on the top plate and bottom plate of capacitors C1 and C2 are either VDD and 0V or 2xVDD and VDD. With these capacitors, when node 3 converts the voltage level from VDD to 0V, the voltage on node 5 is pulled down to VDD and then the voltage level on node 6 is pulled up to 2xVDD by transistor MP3. On the contrary, when the voltage level on node 4 is converted from VDD to 0V, the voltage on node 6 is pulled down to VDD, and that on node 5 is pulled up to 2xVDD by MP2. Initially, the voltages on nodes 3, 4, 5, and 6 could be unknown. If the voltages on nodes 5 and 6 are 2xVDD and VDD, and the voltages on nodes 3 and 4 are 0V and VDD, the voltages across capacitors C1 and C2 are 2xVDD and 0V, respectively, instead of both VDD. In order to overcome this

problem, diode strings DS1 and DS2 are added. The turn-on voltages of the diode strings are designed to a little higher than VDD by using multiple diodes in stacked configuration. In order to prevent the leakage current path to the grounded p-type substrate, the diode-connected MOSFET or poly diode [24] is suggested. With these diode strings, if the voltage on node 3 is at 0V and that on node 4 is at VDD initially, the voltage on node 5 is clamped at the turn-on voltage (~VDD) of DS1. Therefore, MP3 is turned on to pull up the voltage on node 6 to 2xVDD. Thus, the voltages across capacitors C1 and C2 are both VDD.

In this mixed-voltage I/O buffer, the bulk of the blocking NMOS MNS1 can be coupled to 0V (GND) without any gate-oxide reliability problem, even if the gate voltage of MNS1 may be as high as VDDH (2xVDD). The reason is that this blocking NMOS MNS1 is always turned on and the voltage across the gate oxide of MNS1 is from the gate to the conducting channel, but not from the gate to its bulk. The gate oxides of all NMOS devices in the dynamic gate-controlled circuit are also safe because these NMOS devices are turned on when their gates are pulled up to VDDH.

2.2.2 Hot-Carrier Issues in SBNMXIO

There is no reliability issue for this mixed-voltage I/O buffer proposed in [18] in the steady states of receive mode and transmit mode. However, when the mixed-voltage I/O buffer has a transition from receiving 2xVDD input signal to transmitting 0-V output signal, the I/O PAD originally has an initial voltage of 2xVDD before being pulled down. At this transition moment, the transistor MN0 is turned on by *PD* signal from pre-driver, and the transistor MNS1 is subsequently switched on when its source is pulled down by the MN0. Since the original 2xVDD voltage at I/O PAD is not pulled down immediately, the drain-source voltage of MNS1 would be larger than the normal supply voltage (VDD) during this transition, which results in the

hot-carrier degradation on the transistor MNS1. With consideration of hot-carrier reliability for long-time reliable applications in microelectronic products, the 2xVDD I/O buffer designed with single blocking NMOS device in Fig. 2.4 with only 1xVDD devices is somewhat weak to reliably receive the 2xVDD-tolerant input signals in a given CMOS technology.

Chapter 3

Reliability Design on Mixed-Voltage I/O Buffers with Consideration of Hot-Carrier Effect

3.1 INTRODUCTION

Since the hot-carrier degradation threats the lifetime of ICs more seriously with newer CMOS generations, the mixed-voltage I/O buffers must be designed not only with consideration of gate-oxide reliability but also with consideration of hot-carrier effect. A 2xVDD-tolerant I/O buffer fabricated in 0.25-μm CMOS process was reported in [14]. This 2xVDD-tolerant I/O buffer uses double-cascode structure to overcome hot-carrier degradation although it consumes larger silicon area and propagation delay. In this chapter, two robust mixed-voltage I/O buffers based on the prior designs, GTCMXIO and SBNMXIO, mentioned in chapter two have been proposed. The reliable designs of mixed-voltage I/O buffers do not suffer gate-oxide degradations and hot-carrier degradations in both transmit mode and receive mode and the transitions.

3.2 2XVDD-TOLERANT I/O BUFFER WITH DOUBLE-CASCODE STRUCTURE [14], [25]

Fig. 3.1 shows a circuit using three-stacked (double-cascode) transistors to suppress hot-carrier degradation for the 2xVDD-tolerant I/O buffer [14], [25]. The transistors MPT0 and MPT1 comprise a tracking circuit for gate terminal of transistor MN2. The corresponding voltages of the 2xVDD-tolerant I/O buffer in two operating modes

(transmit and receive modes) are list in Table 3.1. When the I/O buffer receives 2xVDD input signal, the gate terminal of transistor MN2 is biased at 2xVDD through transistor MPT0. Consequently, the source terminal is biased at "2xVDD-ΔV" due to the diode-connected MN2. On the contrary, the gate terminal of transistor MN2 is biased at VDD through transistor MPT1 if a 0-V signal is received or transmitted at I/O PAD. When the I/O buffer transmits VDD output signal to I/O PAD, the gate terminal of transistor MN2 is biased at ~VDD due to weakly turn-on transistors MPT0 and MPT1. Therefore, this 2xVDD-tolerant I/O buffer using three-stacked NMOS transistors suffers neither gate-oxide degradation nor hot-carrier effect in both transmit and receive modes. As the I/O buffer has a transition from receiving 2xVDD input signal to transmitting 0-V output signal, the source terminal is biased at "2xVDD-ΔV" initially. In the meanwhile, the source terminal of MN0 is pulled down to ~0.5V by the MN1 in a 0.18-μm technology. The ΔV can be controlled such that all the drain-source voltages of MN0, MN1 and MN2 are below maximum operating voltage, $V_{dd,nom}$ in a give COMS process. Thus, this 2xVDD-tolerant I/O buffer proposed in [14] can successfully solve the hot-carried degradation during the transition from receiving 2xVDD input signal to transmitting 0-V output signal.

According to logic transistor sizing, each of the stacked transistors in Fig. 3.1 is 1.5 times larger in device size than that of the two-stacked transistors in Fig. 1.3 for equal driving capacity. As a result, the 2xVDD-tolerant I/O buffer with three-stacked transistors can solve the hot-carrier degradation with the extra penalty of increased silicon area and longer propagation delay. The circuit technique using three-stacked transistors is applied into the mixed-voltage I/O buffer in Fig. 3.2 as a comparison with new proposed circuit in this these. The mixed-voltage I/O buffer using three-stacked transistors is shown in Fig. 3.2 and denoted as TSTMXIO. Note that the gate terminals of the MN5 and MN6 are floating when the I/O buffer is transmitting

VDD output signal.

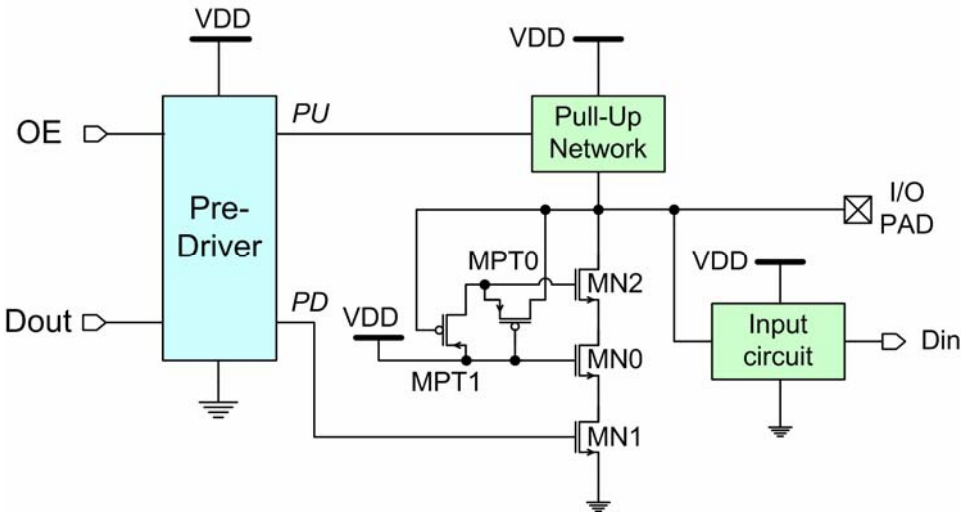


Fig. 3.1 The brief schematic of 2xVDD-tolerant I/O buffer with three-stacked transistors to overcome hot-carrier issue.

Table 3.1
The operations of the 2xVDD-tolerant I/O buffer using three-stacked NMOS transistors.

Operating Modes	Signals at I/O PAD	*PD*	V_g of MN2
Receive	Low (0V)	0V	VDD
Receive	High (2xVDD)	0V	2xVDD
Transmit	Low (0V)	VDD	VDD
Transmit	High (VDD)	0V	~VDD

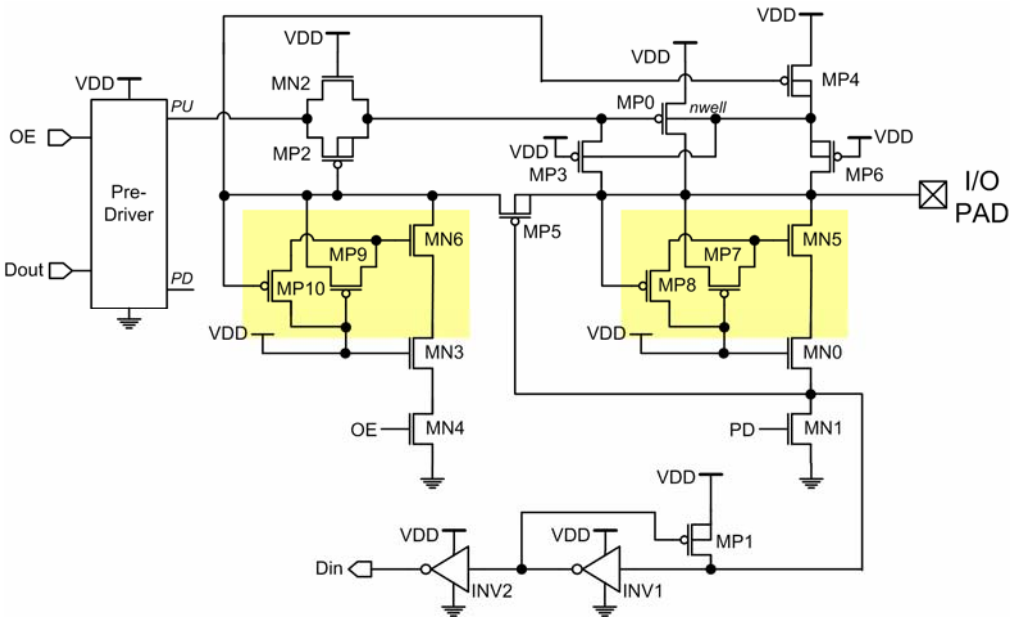


Fig. 3.2 The mixed-voltage I/O buffer using three-stacked NMOS transistors (TSTMXIO).

3.3 NEW DESIGN I:MIXED-VOLTAGE I/O BUFFER WITH NEW PROPOSED HOT-CARRIER-PREVENTED CIRCUIT

3.3.1 Design Concept

A new hot-carrier-prevented circuit t in 2xVDD-tolerant I/O buffer with only two-stacked transistors is proposed in Fig. 3.3. The gate-controlled signal on transistor MN1 is a delay version of PD signal from the pre-driver. The tracking circuit controlled by OE signal generates control signal V_{CTRL} to control switch SW0 During the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the switch SW0 will be turned on by the control signal V_{CTRL} to pull down I/O PAD to VDD. The delay should be long enough to have I/O PAD pulled down to VDD before the MN1 is switched on. Thus, the drain-source voltage of MN0 during such transition is not larger than its maximum normal operation voltage range (VDD) in the given CMOS technology. Note that this delay somewhat results in increasing delay during the transition from receiving 2xVDD input signal to transmitting 0-V

output signal, but has no effect in the steady states of transmit and receive modes. Hence, the 2xVDD-tolerant I/O buffer with the new proposed hot-carrier-prevented circuit in Fig. 3.3 does not suffer the hot-carrier degradation. The switch SW0 must be kept off in all states except the high-to-low transition, so that this 2xVDD-tolerant I/O buffer can be operated correctly in both receive mode and transmit mode.

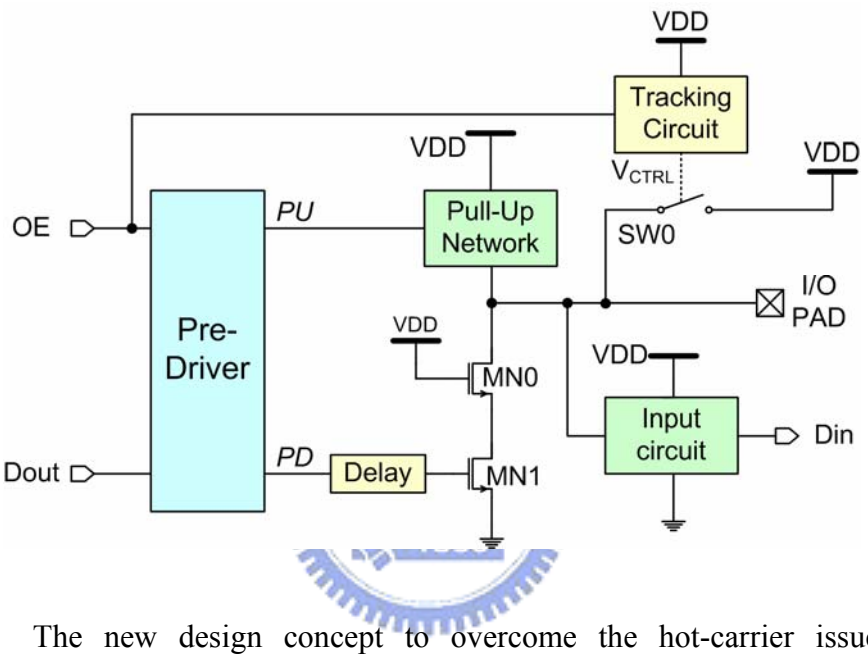


Fig. 3.3 The new design concept to overcome the hot-carrier issue in the 2xVDD-tolerant I/O buffer with only two-stacked transistors.

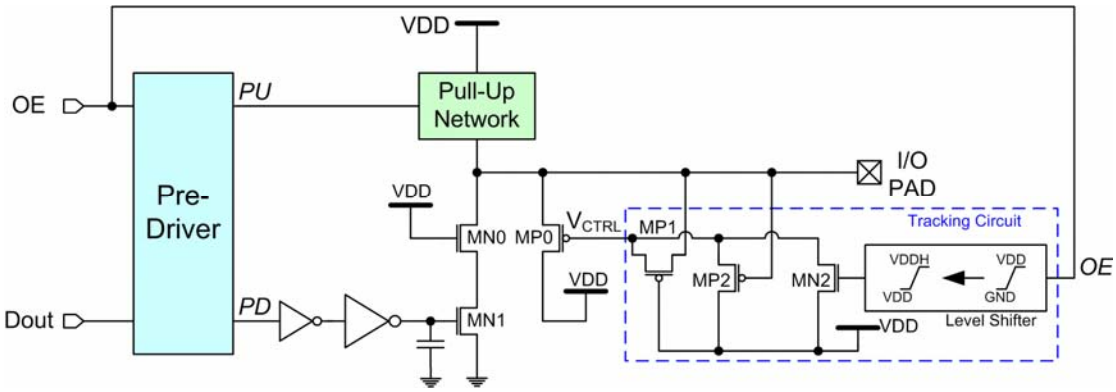


Fig. 3.4 The implementation of the new proposed hot-carrier-prevented circuit for 2xVDD-tolerant I/O buffer with two-stacked transistors.

The desired delay time Δt can be estimated as following equation:

$$\Delta Q = C_L \Delta V = I_{SW0} \Delta t \qquad (3 - 1)$$

The C_L is the output loading, ΔV is "VDDH-VDD", and I_{SW0} is the driving current of switch SW0.

3.3.2 Circuit Implementation

Fig. 3.4 depicts the circuit implementation of the new proposed hot-carrier-prevented circuit. Note that the input circuit has been omitted for convenience. The delay cell can be implemented simply by inverter chain. Besides, a small capacitor can be inserted into the output of the inverter chain to meet the desired delay time. The switch SW0 in Fig. 3.3 is realized by the PMOS transistor MP0 with a tracking circuit which is composed of transistors MP1, MP2, MN2 and a level shifter. The level shifter in tracking circuit shifts a voltage level of 0/VDD to VDD/2xVDD and can be implemented by using the circuit in Fig. 2.5 [18]. The tracking circuit makes the V_{CTRL} turn off the MP0 in receive and transmit modes, but turn it on in the transition (from receiving 2xVDD input signal to transmitting 0-V output signal).

Table 3.2
The operations of the proposed hot-carrier-prevented circuit in 2xVDD-tolerant I/O buffer.

Operating Modes	Signals at I/O PAD	*PD*	V_{CTRL}
Receive	Low (0V)	0V	VDD
Receive	High (2xVDD)	0V	2xVDD
Transmit	Low (0V)	VDD	VDD
Transmit	High (VDD)	0V	VDD

The corresponding voltages in two operating modes (transmit and receive modes) of the proposed hot-carrier-prevented circuit are list in Table 3.2. The detailed operations of this hot-carrier-prevented circuit are described in the following. When the mixed-voltage I/O buffer is in the receive mode, the output enable signal, OE, is set to 0V, and PU and PD signals are VDD and 0V, respectively. The transistor MP1 is switched on to set V_{CTRL} to 2xVDD thus there is no leakage path to VDD through transistor MP0 when receiving 2xVDD input signals. The transistor MP2 is switched on to set V_{CTRL} to VDD when receiving 0-V input signals. As the 2xVDD-tolerant I/O buffer is operating in the transmit mode (OE=VDD), the gate voltage of MN2 will be pulled up to 2xVDD by the level shifter. Then, the transistor MP0 is switched off by setting V_{CTRL} to VDD. As a result, the switch MP0 is turned off in both the steady-state receive mode and transmit mode and has no effect on the correct operations. In steady states, there is neither gate-oxide degradation nor hot-carrier degradation in this 2xVDD-tolerant I/O buffer.

When the 2xVDD-tolerant I/O buffer has the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the gate terminal of MN1 originally stays at 0V while the PD signal is changing from 0V to VDD by the pre-driver. In the meanwhile, the V_{CTRL} is set to VDD by switching on the MN2, and consequently the MP0 is turned on to discharge the initial voltage of 2xVDD at the I/O PAD. After hundreds of picoseconds, the voltage at I/O PAD has been pulled down to about VDD, and the gate voltage of MN1 increases to VDD after the delay induced by the inverter chain. Therefore, the drain-source voltage of MN0 can be kept within the maximum normal operating voltage ($V_{dd,nom}$) range during the transition, that resulting in no hot-carrier degradation.

3.3.3 Whole 2xVDD-Tolerant I/O Buffer With Hot-Carrier-Prevented Circuit

As mentioned in chapter two, the 2xVDD-tolerant I/O buffer shown in Fig. 2.3 suffers hot-carrier degradation under the I/O signal transitions. During the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the transistor MN0 suffers the hot-carrier degradation. The hot-carrier degradation will also occur on MN3 device in this traditional 2xVDD-tolerant I/O buffer during this transition. The transistors MN2 and MP2 also suffer hot-carrier degradation during the transition from receiving 2xVDD input signal to transmitting VDD output signal, since the gate terminal of transistor MP0 is initially kept at 2xVDD but the *PU* signal has been pull down to 0V by the pre-driver to turn on transistor MP0. In Fig. 3.5, the mixed-voltage I/O buffer with three hot-carrier-prevented circuits is proposed to solve the hot-carrier reliability issues on MN0, MN3, MN2, and MP2 in the 2xVDD-tolerant I/O buffer shown in Fig. 2.3. This new mixed-voltage I/O buffer with hot-carrier-prevented circuit is so called HCPMXIO in this thesis. The corresponding hot-carrier-prevented circuits in HCPMXIO are shown in Fig. 3.6. Note that all the bulks of PMOS transistors in hot-carrier-prevented circuits are connected to the self-biased n-well (*nwell*) marked in Fig. 3.5 to avoid leakage paths. The delay added in the gate terminal of MN1 shown in Fig. 3.3 has been changed to the output enable signal. As a result, the gate-controlled signals of MN1 and MN4 and *PU* signal are the delay versions of that in the original I/O buffer shown in Fig. 2.3.

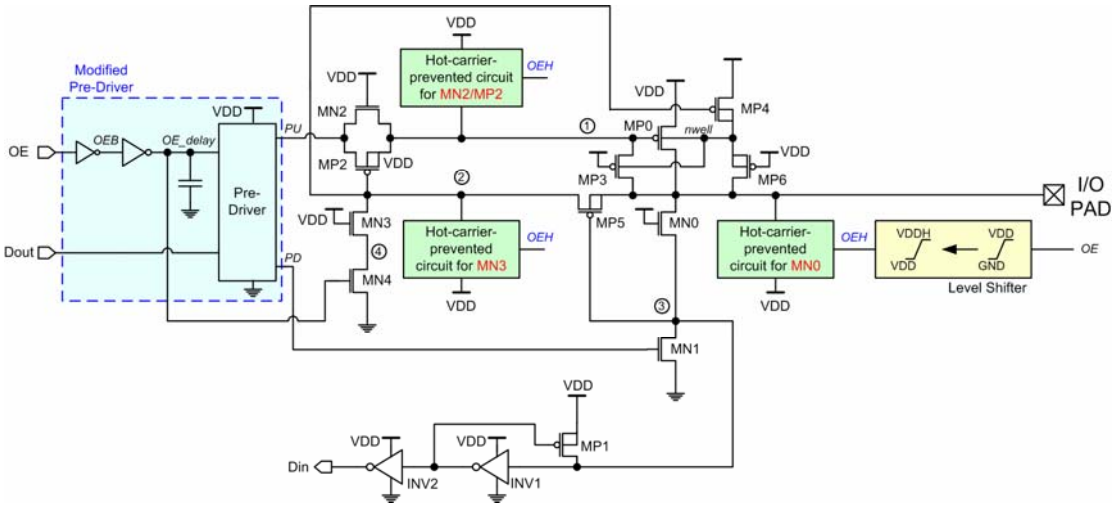


Fig. 3.5 The new mixed-voltage I/O buffer with hot-carrier-prevented circuits (HCPMXIO).

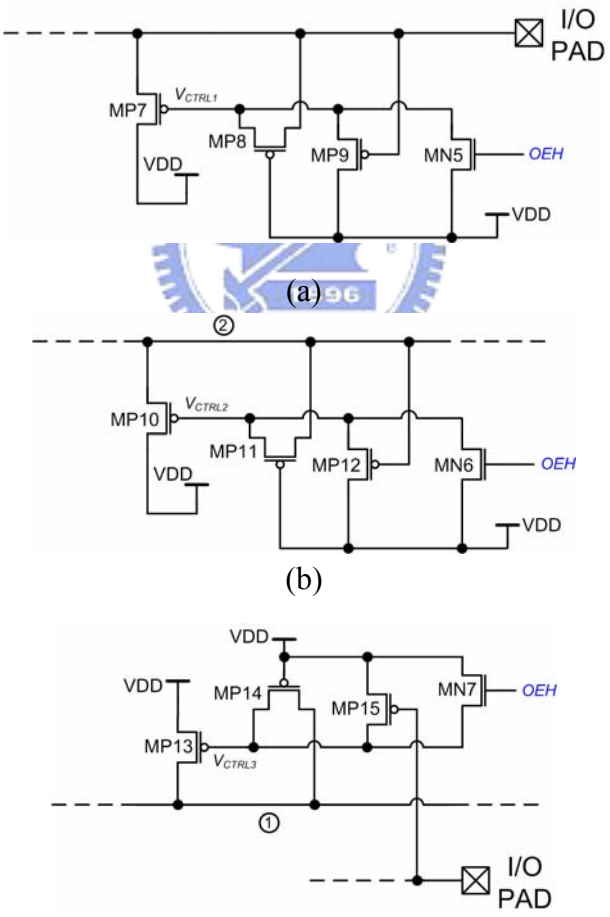


Fig. 3.6 The corresponding hot-carrier-prevented circuits in HCPMXIO. (a) The hot-carrier-prevented circuit for the MN0. (b) The hot-carrier-prevented circuit for the MN3. (c) The hot-carrier-prevented circuit for the MN2 and MP2.

3.3.4 Simulation Results

The new proposed 2xVDD-tolerant I/O buffer with the hot-carrier-prevented circuits (HCPMXIO) shown in Fig. 3.5 is designed to meet the PCI-X 2.0 applications in a given 0.18-μm CMOS process, thus the HCPMXIO transmits 0V-to-1.5V output signals and receives 0V-to-3.3V input signals. Besides, the HCPMXIO has an operating speed up to 266 MHz. It is difficult to observe the long term behavior of hot-carrier effect in mixed-voltage I/O buffers unless the saturation currents or turn-on resistances are measured under overstress conditions for a long time. Therefore, the hot-carrier effect is verified by SPICE simulation in a 0.18-μm CMOS process for convenience. For measuring consideration, a load capacitance of 10 pF is added in the outputs of mixed-voltage I/O buffer shown in Fig. 3.7. In this thesis, all the mixed-voltage I/O buffers are simulated with a temperature of 85°C at TT corner, which can result in close results to actual conditions.

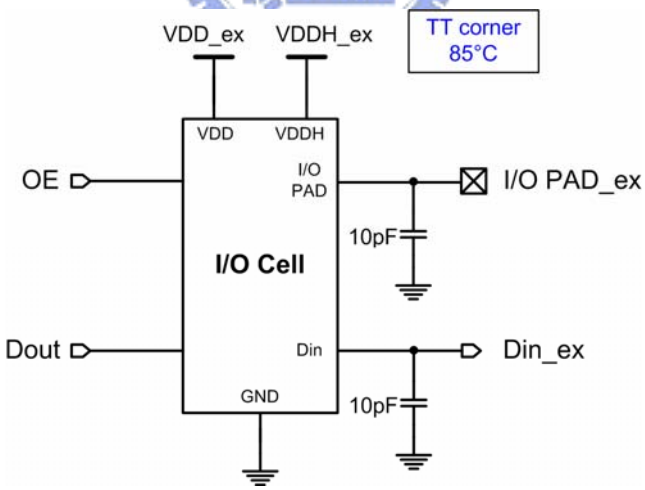


Fig. 3.7 The simulation environment.

Fig. 3.8 shows the simulation waveforms of the HCPMXIO in receive mode to receive the input signal of 0-to-3.3V with a frequency of 266 MHz. The

gate-controlled signals V_{CTRL1}, V_{CTRL2} and V_{CTRL3} are biased at 3.3V in receiving 3.3-V input signal, and they are biased at 1.5V in receiving 0-V input signal. In Fig. 3.9, the simulation waveforms of the I/O circuit in transmit mode to transmit a signal of 0-to-1.5V with a frequency of 266 MHz are shown. All the gate-controlled control signals are biased at 1.5V to turn off transistors MP7, MP10 and MP13 in transmit mode. As shown in Fig. 3.8 and Fig. 3.9, the proposed mixed-voltage I/O circuit with hot-carrier-prevented circuits can be operated correctly in both receive mode and transmit mode.

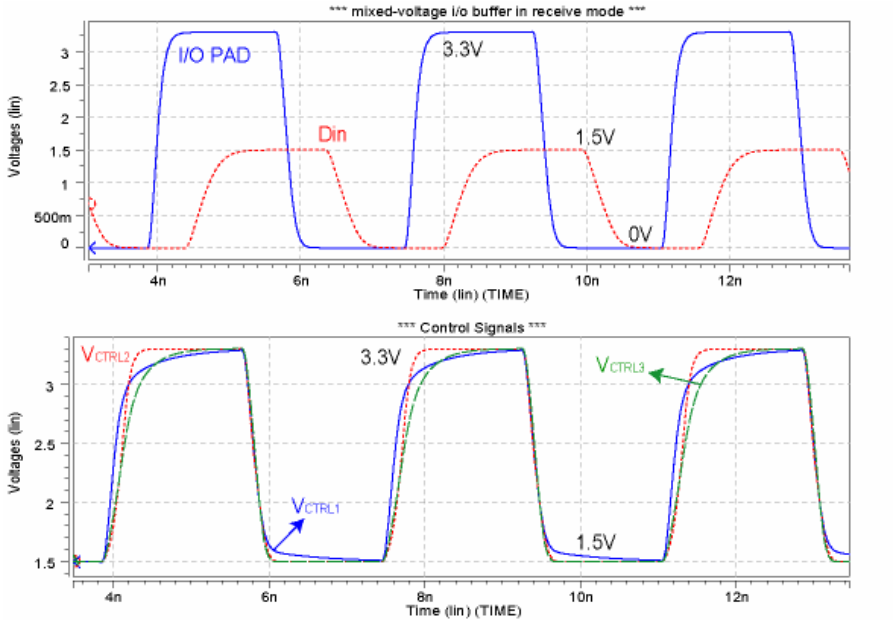


Fig. 3.8 Simulation waveforms of the HCPMXIO in receiving mode with 3.3-V 266-MHz input signals.

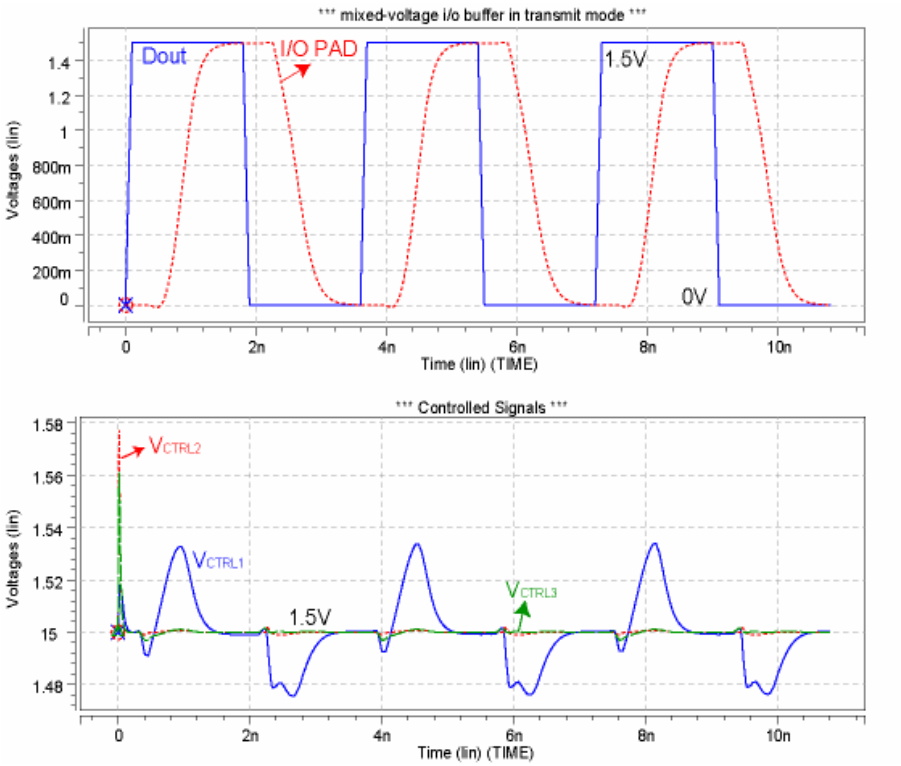
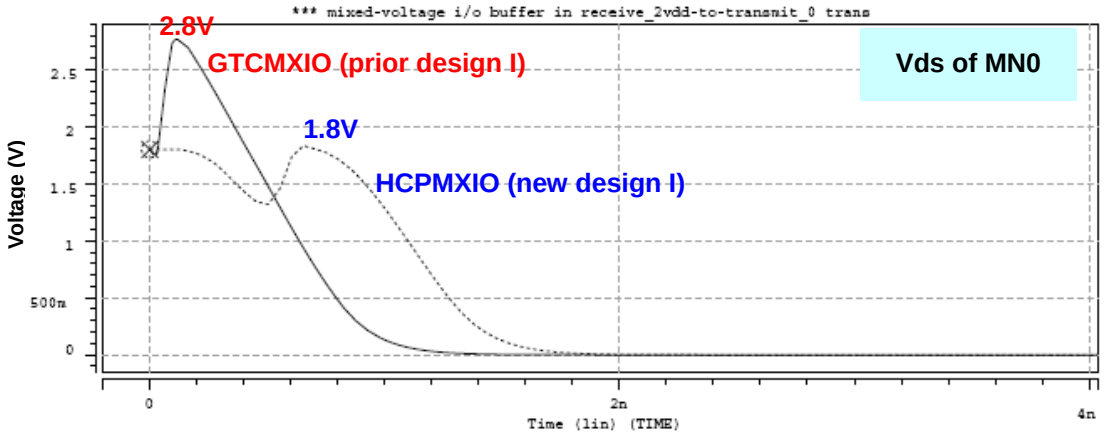


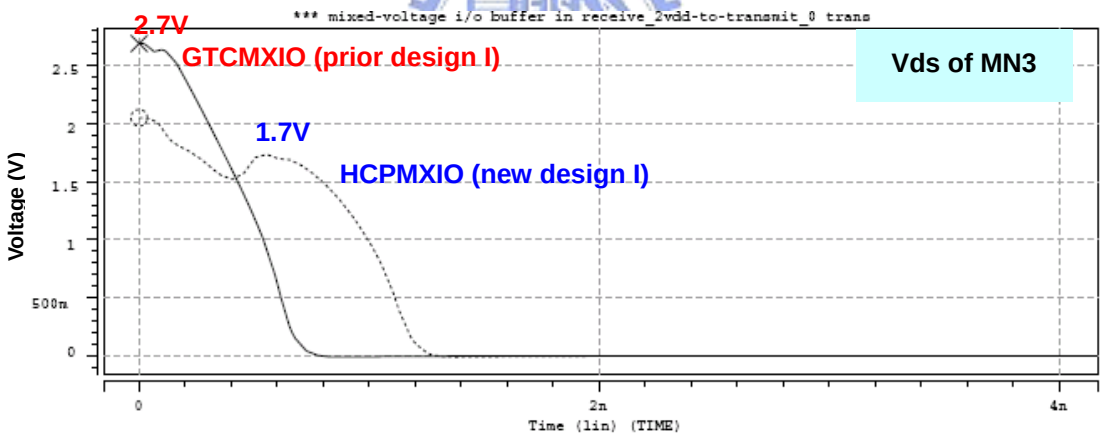
Fig. 3.9 Simulation waveforms of the HCPMXIO in transmitting mode with 266-MHz output signals.

The drain-source voltages of the transistors MN0, MN3, MN2 and MP2 in HCPMXIO are compared to that in GTCMXIO (Fig. 2.3) during the transition from receiving 3.3-V input signal to transmitting 0-V or 1.5-V output signal. The drain-source voltages of MN0 and MN3 during the transition from receiving 3.3-V input signal to transmitting 0-V output signal are shown in Fig. 3.10. In Fig. 3.10 (a), the peak of drain-source voltage on MN0 in this work (HCPMXIO) is only ~1.8V, but that of the original design (GTCMXIO) is as high as 2.8V. As shown in Fig. 3.10 (b), the peak of drain-source voltage on MN3 is 1.7V in this work, but that in the GTCMXIO is 2.7V. Besides, the drain-source voltages of the transistor MN2 (or MP2) in this work and the original design during the transient from receiving 3.3-V input signal to transmitting 1.5-V output signal are compared in Fig. 3.11. The drain-source voltage across the transistor MN2 (or MP2) is lower than the maximum normal

operating voltage (1.8V) in the HCPMXIO. However, the drain-source voltage across the transistor MN2 (or MP2) in the original design is still as high as ~2.8V. Therefore, the hot-carrier effect has been suppressed by the proposed hot-carrier-prevented circuits in this work.



(a)



(b)

Fig. 3.10 The drain-source voltages of the MN0 and MN3 during the transition from receiving 3.3V input signal to transmitting 0-V output signal. (a) The drain-source voltage of the MN0. (b) The drain-source voltage of the MN3.

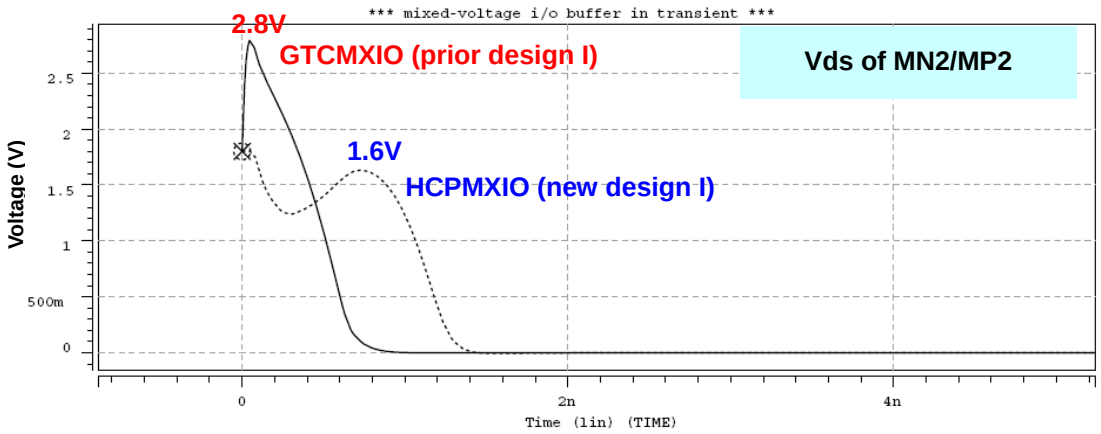


Fig. 3.11 The drain-source voltages of MN2 during the transition from receiving 3.3-V input signal to transmitting 1.5-V output signal.

Moreover, a delay of 1.166ns is required in GTCMXIO when the 2xVDD-tolerant I/O buffer switches from receive mode to transmit mode. A corresponding delay of 1.692ns is required in the HCPMXIO under the same switching condition. It should be noted that the additional delay in the HCPMXIO would result in undesired glitch at I/O PAD which may cause logic error in the following circuit if the additional delay resulted from inverter chain is too large. As shown in Fig. 3.12, the glitch gets serious with increasing the delay of high level at OE signal. Therefore, the delay in gate-controlled signal of MN1 in Fig. 3.4 should be carefully controlled.

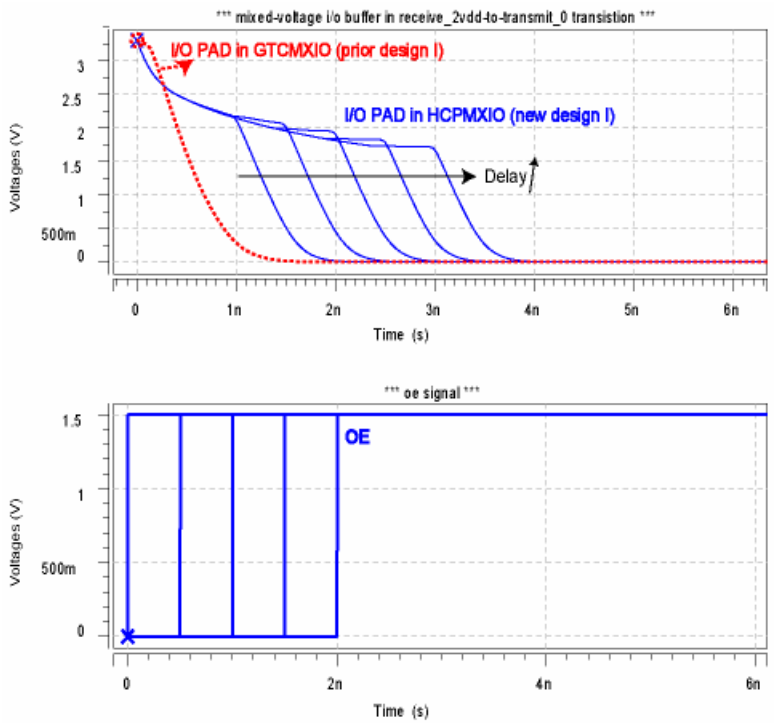


Fig. 3.12 Simulation waveforms of the HCPMXIO in transition with increasing the delay of high level at OE signal.

3.3.5 Summary for Simulation Results

The comparisons of new proposed mixed-voltage I/O buffer with prior designs are list in Table 3.3. The parameters of mixed-voltage I/O buffers are simulated with an operating speed of 266 MHz at TT corner and 85°C. Several parameters are defined in this thesis as follows:

- I_{OH}: The source current of mixed-voltage I/O buffer when the voltage at I/O pad is pulled up to 0.9xVDD.
- I_{OL}: The sink current of mixed-voltage I/O buffer when the voltage at I/O pad is pulled down to 0.1xVDD.
- T_{pr}: The propagation delay signal with a voltage swing of 3.3 V received from I/O PAD to Din.
- T_{pt}: The propagation delay signal transmitted from Dout to I/O PAD in the mixed-voltage I/O buffer.

- T_{drt}: The delay time for the voltage at I/O PAD pulled down from 3.3V to 0V when the mixed-voltage I/O buffer has a transition from receiving 3.3V input signal to transmitting 0-V output signal.

Table 3.3
The simulation results of mixed-voltage I/O buffers with/without hot-carrier-prevented mechanisms.

Parameters		GTCMXIO (Fig. 2.3)	TSTMXIO (Fig. 3.2)	HCPMXIO (Fig. 3.6)
Hot-Carrier Degradation		Yes (387 ps)	No	No
T_{drt}		1.166 ns	1.205 ns	1.692 ns
I_{OL} at V_{OL}=0.15 V		9.6 mA	7.2 mA	9.4 mA
I_{OH} at V_{OH}=1.35 V		11.4 mA	10.5 mA	11.8 mA
Receive Mode	T_{rise}	446 ps	446 ps	458 ps
	T_{fall}	417 ps	414 ps	411 ps
	T_{pr}	724 ps	765 ps	728 ps
	Power Consumption	29 μW/MHz	30 μW/MHz	28 μW/MHz
Transmit Mode	T_{rise}	467 ps	495 ps	478 ps
	T_{fall}	604 ps	771 ns	616 ps
	T_{pt}	793 ps	837 ps	804 ps
	Power Consumption	71 μW/MHz	74 μW/MHz	70 μW/MHz

As shown in Table 3.3, the GCTMXIO suffers hot-carrier degradation in the transition from receiving 3.3-V input signal to transmitting 0-V output signal. The drain-source voltage of transistor are larger than the maximum operating voltage ($V_{dd,nom}$) for 387 ps in a given 0.18-μm CMOS process. The TSTMXIO and HCPMXIO with hot-carrier mechanisms solve the hot-carrier degradation successfully. The propagation delays and rise/fall time of TSTMXIO, however, are larger than that of HCPMXIO in this thesis due to three-stacked transistors.

3.4 NEW DESIGN II: MIXED-VOLTAGE I/O BUFFER WITH TWO BLOCKING NMOS DEVIES AND DYNAMIC GATE-CONTROLLED CIRCUIT

3.4.1 Design Concept

As mentioned in chapter two, the SBNMXIO (Fig. 2.4) suffers hot-carried degradation during the transition from receiving 2xVDD input signal to transmitting 0-V output signal. A new mixed-voltage I/O buffer with two blocking NMOS devices (called TBNMXIO) is proposed in Fig. 3.13 to tolerate 2xVDD I/O signals. Fig. 3.13 depicts the new proposed 2xVDD-tolerant I/O buffer with two blocking NMOS devices and dynamic gate-controlled circuit, where VDDH represents a voltage of 2xVDD and can be implemented by on-chip charge pump with only 1xVDD devices [26] or other high-voltage generators. This 2xVDD-tolerant I/O buffer is designed to receive 0V-to-2xVDD input signals and transmit 0V-to-VDD output signals. The 0V-to-2xVDD input signals will be transferred into core circuits with a voltage swing of only VDD. The blocking NMOS devices, MNS1 and MNS2, in Fig. 3.13 are used to protect the 2xVDD-tolerant I/O buffer from gate-oxide and hot-carrier reliability issues. The corresponding node voltages in the dynamic gate-controlled circuit during the two operating modes (transmit and receive) are list in Table 3.4.

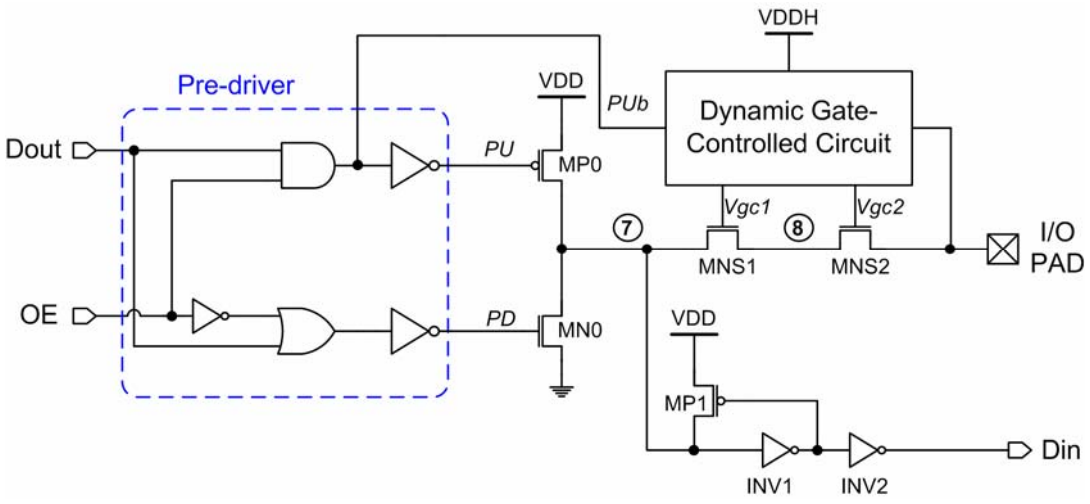


Fig. 3.13 The new proposed 2xVDD-tolerant I/O buffer with two blocking NMOS devices and dynamic gate-controlled circuit to solve the hot-carrier reliability issue (TBNMXIO).

Table 3.4
The operations of the dynamic gate-controlled circuit in TBNMXIO

Operating Modes	Signals at I/O PAD	Vg of MNS1 (*Vgc1*)	Vg of MNS2 (*Vgc2*)
Receive	Low (0 V)	VDD	VDD
Receive	High (2xVDD)	VDD	High (2xVDD)
Transmit	Low (0 V)	VDD	VDD
Transmit	High (VDD)	2xVDD	2xVDD

When the 2xVDD-tolerant I/O buffer is operating in the receive mode (OE=0), the gate-controlled signal (V_{gc2}) on MNS2 will be changed corresponding to the voltage at I/O PAD. In the meanwhile, the V_{gc1} on MNS1 is always biased at VDD by gate-controlled circuit. The V_{gc2} is biased at VDD to receive 0-V input signal, but it will be biased at 2xVDD to receive 2xVDD input signal. Besides, the output transistors MP0 and MN0 are turned off by pre-driver in the receive mode. If an input signal of logic low (0V) is received at I/O PAD, nodes 7 and 8 will be discharged to 0

V through the transistors MNS1 and MNS2. Therefore, the input signal of 0V will be successfully transmitted to Din (internal circuit). On the other hand, if an input signal of 2xVDD is received from I/O PAD, the node 8 is biased at "2xVDD-ΔV" due to the diode-connected transistor MNS2. The node 7 will be restored to VDD after the feedback operation of MP1. As a result, the input signal can be transmitted to Din successfully. As the 2xVDD-tolerant I/O buffer transmits 0-V output signal from Dout to I/O PAD, both V_{gc1} and V_{gc2} are biased at VDD. At the same time, the transistors MN0 and MP0 are turned on and off, respectively, by pre-driver. V_{gc1} and V_{gc2} are biased at 2xVDD if an output signal of VDD will be transmitted to the I/O PAD. The transistors MN0 and MP0 are simultaneously switched off and on, respectively, and the node 7 is pulled to VDD. Thus, the output signals sent from Dout can be transmitted to I/O PAD. The proposed 2xVDD-tolerant I/O buffer does not suffer the gate-oxide and hot-carrier reliability issues in both steady states and transition between the transmit mode and receive mode.

3.4.2 Circuit Implementation

The dynamic gate-controlled circuit of TBNMXIO is implemented in Fig. 3.14. When the I/O buffer is in the receive mode, the signal *PUb* in Fig. 3.14 is set to 0V and then *PUH* is set to VDD through the level shifter which can be implemented by the circuit in Fig. 2.5. The gate voltage of MNS1 is consequently biased at VDD by switching on the transistor MNTC1. The transistors MPTC1 and MPTC2 comprise a gate-tracking circuit of MNS2, therefore the voltage at *Vgc2* is dependent on the voltage at I/O PAD in the receive mode. Note that the bulks of transistors MPTC1 and MPTC2 are connected to the same node of the gate of MNS2 in order to avoid leakage path. If an input signal of logic high (2xVDD) is received, *Vgc2* is biased at 2xVDD through the switch MPTC2. On the contrary, if a logic low (0V) is received, *Vgc2* is biased at VDD

through the switch MPTC1. When the 2xVDD-tolerant I/O buffer is transmitting a 0-V output signal, *PUb* is set to 0V and both *Vgc1* and *Vgc2* are consequently set to VDD by the transistors MNTC1 and MPTC1. When an output signal of VDD is transmitted, *PUb* is set to VDD and *PUH* is set to 2xVDD, whereas *Vgc1* is biased at 2xVDD and *Vgc2* is set to 2xVDD through the switch MPTC1.

When TBNMXIO has a transition from receiving 2xVDD input signal to transmitting 0-V output signal, the node 7 and node 8 are originally biased at VDD and "2xVDD-ΔV," respectively. At this transition moment, the transistor MN0 is turned on by *PD* signal from pre-driver, and the transistor MNS1 is subsequently switched on when its source is pulled down by MN0. Then, the transistor MNS2 is switched on and the voltage at I/O PAD is pulled down. The voltage drops across the terminals of the transistors MNS1 and MNS2 are below the maximum operating voltage in the given process. As a result, this new proposed 2xVDD-tolerant I/O buffer with two blocking NMOS devices does not suffer hot-carrier degradation during the transition from receiving 2xVDD input signal to transmitting 0-V output signal.

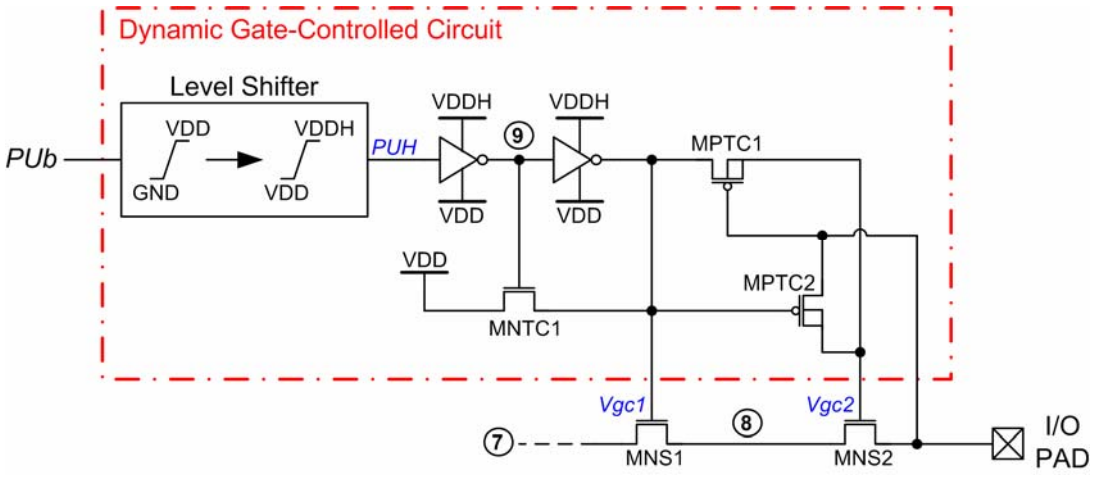


Fig. 3.14 Circuit implementation of the dynamic gate-controlled circuit in the TBNMXIO.

3.4.3 Simulation Results

The proposed 2xVDD-tolerant I/O buffer with two blocking NMOS devices and dynamic gate-controlled circuit (TBNMXIO) has been designed to meet the PCI-X 2.0 applications, therefore VDD is 1.5V and VDDH is 3.3V in this work. The TBNMXIO has been verified by SPICE simulation in a 0.18-μm CMOS process. Moreover, the transistors MN0, MNS1 and MNS2 in this TBNMXIO are 1.5 times bigger in device size than the transistors MN0 and MNS1 in SBNMXIO (Fig. 2.4) for equal driving capacity. Fig. 3.15 and Fig. 3.16 show the simulation waveforms of the new proposed 2xVDD-tolerant I/O buffer (TBNMXIO) with an operating speed of 266 MHz in the receive mode and transmit mode, respectively.

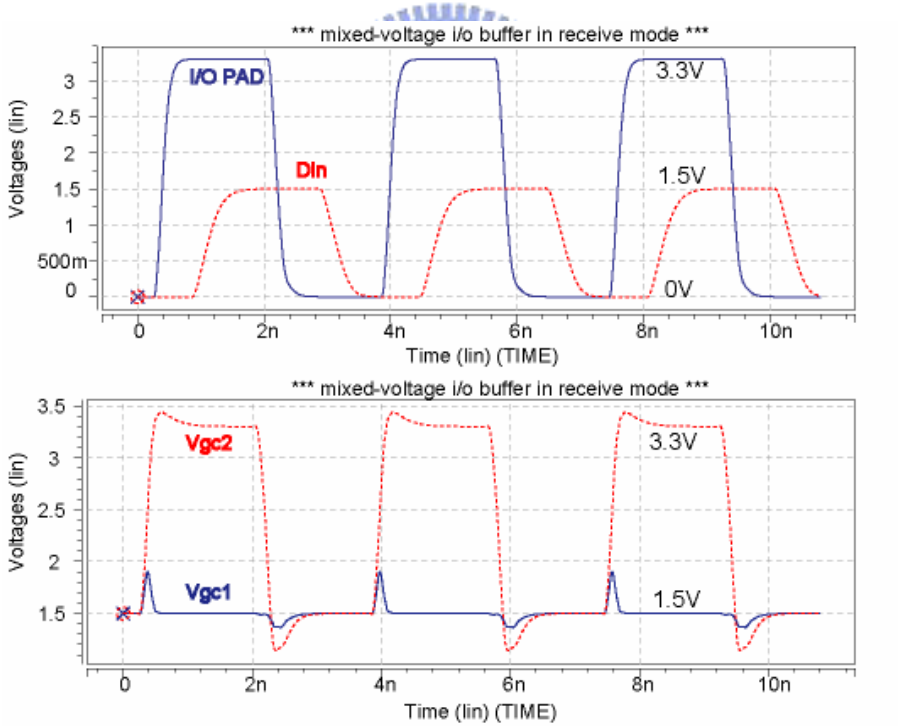


Fig. 3.15 Simulation waveforms of the TBNMXIO operating at 266 MHz when receiving 0V-to-3.3V input signals at I/O PAD.

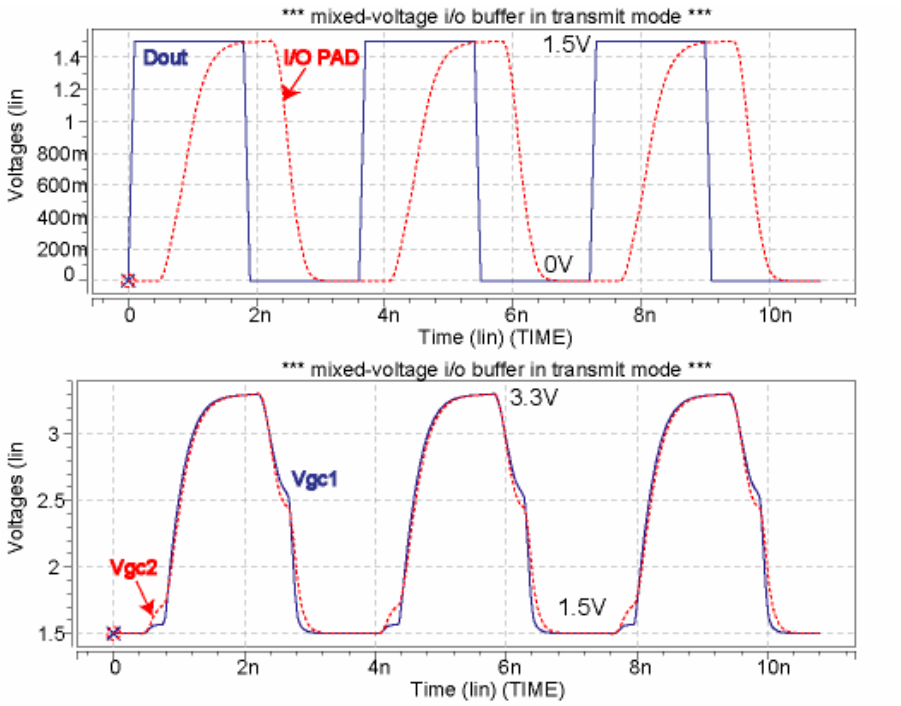


Fig. 3.16 Simulation waveforms of the TBNMXIO operating at 266 MHz when transmitting 0V-to-1.5V output signals to I/O PAD.

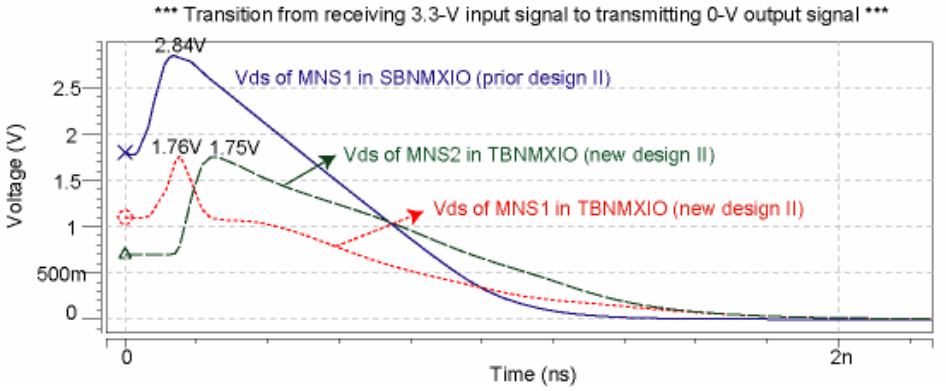


Fig. 3.17 Comparisons of drain-source voltages between the prior design SBNMXIO and new design TBNMXIO during the transition from receiving 2xVDD input signal to transmitting 0-V output signal.

When an input signal of 3.3V is received at I/O PAD, the gate-controlled signal of MNS2, *Vgc2*, is 3.3V as well. In the meanwhile, the gate-controlled signal of MNS1, *Vgc1*, is 1.5 V as shown in Fig. 3.15. Both *Vgc1* and *Vgc2* are biased at 1.5V if an output signal of 0V is received at I/O PAD. The input data received at I/O PAD are successfully

transmitted to Din. In Fig. 3.16, when the 2xVDD-tolerant I/O buffer is operating in the transmit mode, both *Vgc1* and *Vgc2* are biased at 3.3V to transmit 1.5-V output signal. But, it will be biased at 1.5V to transmit 0-V output signal, as shown in Fig. 3.16 with a full swing of 1.5 V at I/O PAD.

Table 3.5
The simulated results of mixed-voltage I/O buffers with blocking NMOS devices.

Parameters		SBNMXIO (Fig. 2.4)	TBNMXIO (Fig. 3.13)
Hot-Carrier Degradation		Yes (459 ps)	No
T_{drt}		1.918 ns	1.809 ns
I_{OL} at V_{OL}=0.15 V		7.2 mA	5.6 mA
I_{OH} at V_{OH}=1.35 V		5.4 mA	5.9 mA
Receive Mode	T_{rise}	453 ps	453 ps
	T_{fall}	418 ps	417 ps
	T_{pr}	754 ps	888 ps
	Power Consumption	29 μW/MHz	31 μW/MHz
Transmit Mode	T_{rise}	739 ps	664 ps
	T_{fall}	615 ps	627 ps
	T_{pt}	746 ps	784 ps
	Power Consumption	62 μW/MHz	67 μW/MHz

Fig. 3.17 shows the comparisons on the drain-source voltage (V_{ds}) of the blocking NMOS devices in the TBNMXIO to that in the SBNMXIO shown in Fig. 2.4 during the transition from receiving 3.3-V input signal to transmitting 0-V output signal. As shown in Fig. 3.17, the peaks of V_{ds} on MNS1 and MNS2 in TBNMXIO are only 1.76V and 1.75V, respectively, which are below the maximum operating voltage of 1.8-V devices, but the peak voltage of MNS1 in the SBNMXIO is as high as 2.84V. Therefore, the new proposed 2xVDD-tolernat I/O buffer with two blocking NMOS devices and dynamic gate-controlled circuit can successfully solve the hot-carrier

reliability issue during the transition from receiving 3.3-V input signal to transmitting 0-V output signal. The simulation results of the SBNMXIO and TBNMXIO are list in Table 3.5. The transistor MNS1 in SBNMXIO suffers hot-carrier degradation for 459 ps when the mixed-voltage I/O buffer switches from receiving 3.3-V input signal to transmitting 0-V output signal. The TBNMXIO successfully solves hot-carrier degradation at the cost of slightly larger propagation delays and rise/fall time.

3.5 EXPERIMENTAL RESULTS

3.5.1 Measurement Settings

The proposed HCPMXIO and TBNMXIO in this thesis have been fabricated in the 0.18-μm CMOS process with only thin-oxide (1.8-V) devices. The photographs of fabricated circuits are shown in Fig. 3.18 and Fig. 3.19. Fig. 3.18 shows the fabricated circuit of new proposed 2xVDD-tolerant I/O buffer with hot-carrier-prevented circuit and the layout area is 191.6 μm × 51.4 μm. Fig. 3.19 shows the fabricated of new proposed I/O buffer with two blocking NMOS devices and dynamic gate-controlled circuit and the layout area is 169.2 μm × 53.8 μm. The measurement setting of mixed-voltage I/O buffers are shown in Fig. 3.20 and the printed circuit board (PCB) of tested mixed-voltage I/O buffers is shown in Fig. 3.21. As shown in Fig. 3.20 (a), the signals at Dout, which are generated by a pulse generator, are transmitted to I/O PAD, and can be observed by a digital phosphor oscilloscope. In Fig. 3.20 (b), the signals are received at I/O PAD, and can be observed at Din by voltage probe when the mixed-voltage I/O buffers are operated in receive mode.

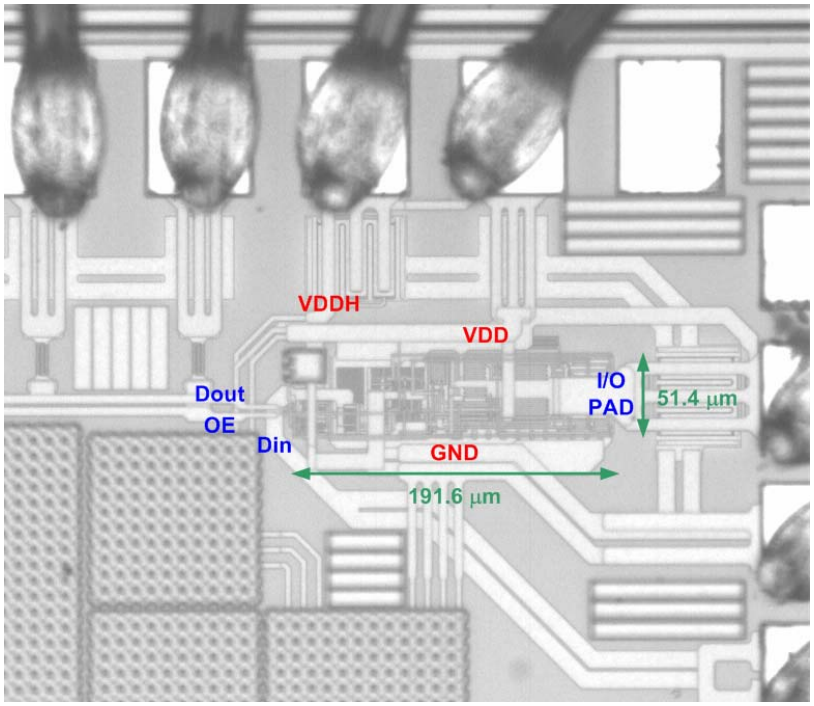


Fig. 3.18 The photograph of the new proposed 2xVDD-tolerant I/O buffer with hot-carrier-prevented circuits (HCPMXIO) in a 0.18-μm 1.8-V CMOS process.

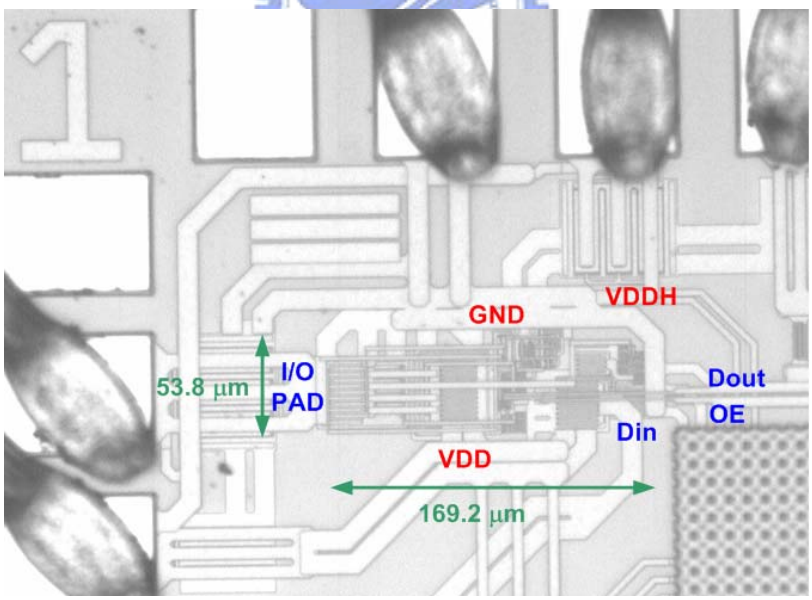
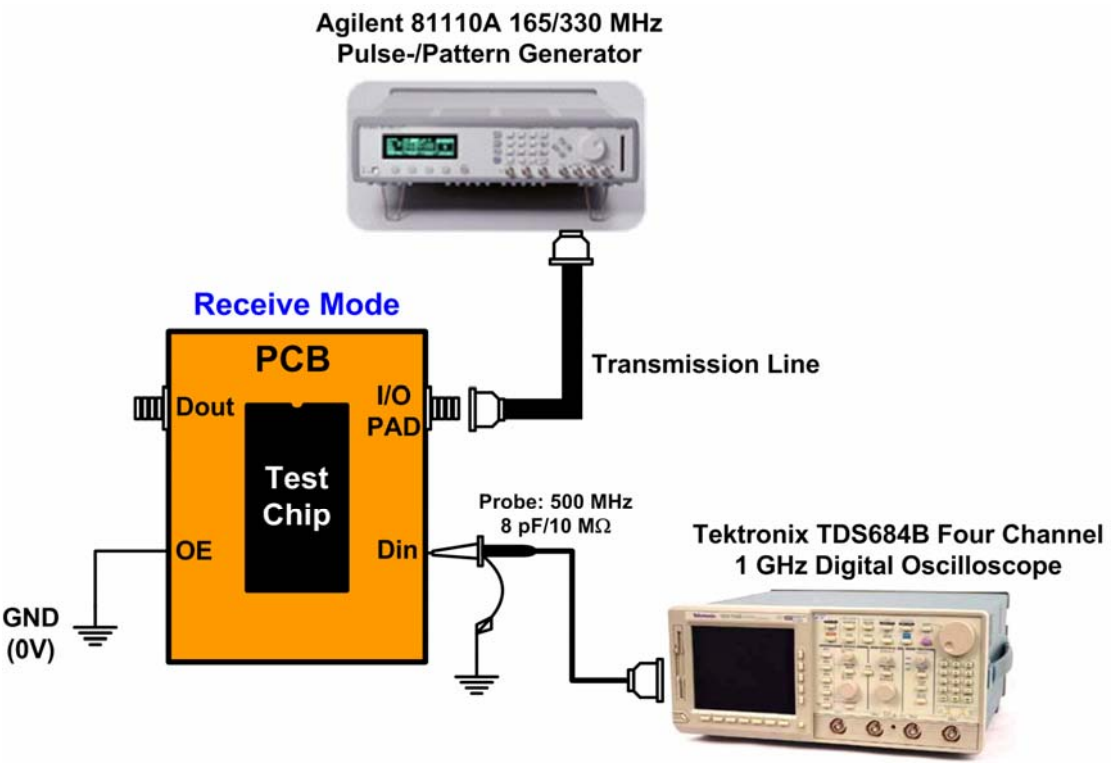
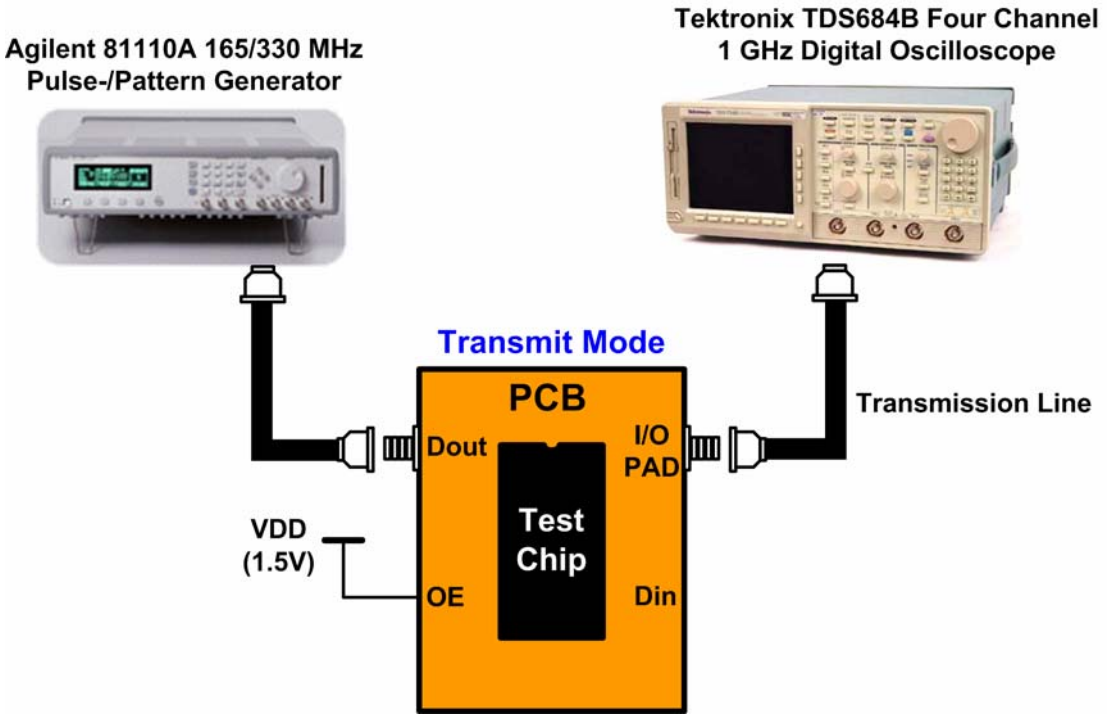


Fig. 3.19 The photograph of the new proposed 2xVDD-tolerant I/O buffer with blocking NMOS devices (TBNMXIO) in a 0.18-μm 1.8-V CMOS process.



(a)



(b)

Fig. 3.20 The measurement setup of mixed-voltage I/O buffer (a) in receive mode and (b) in transmit mode.

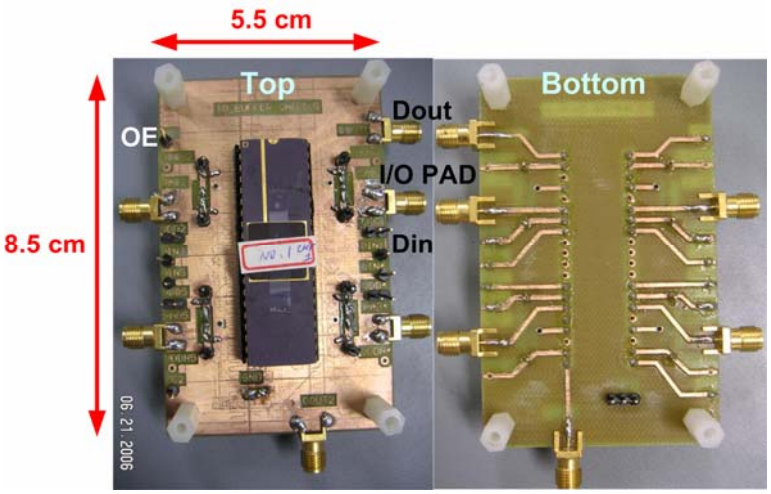
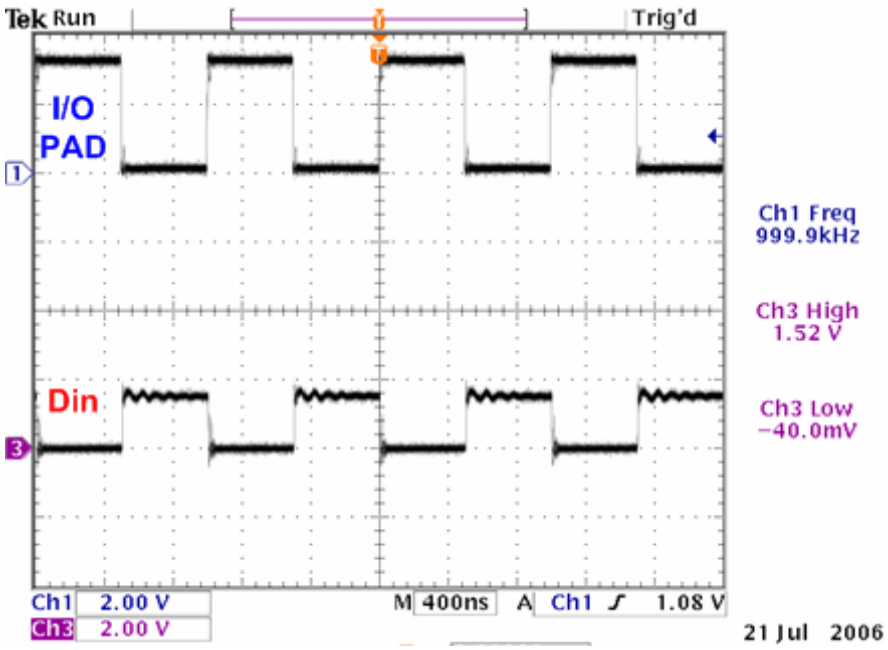


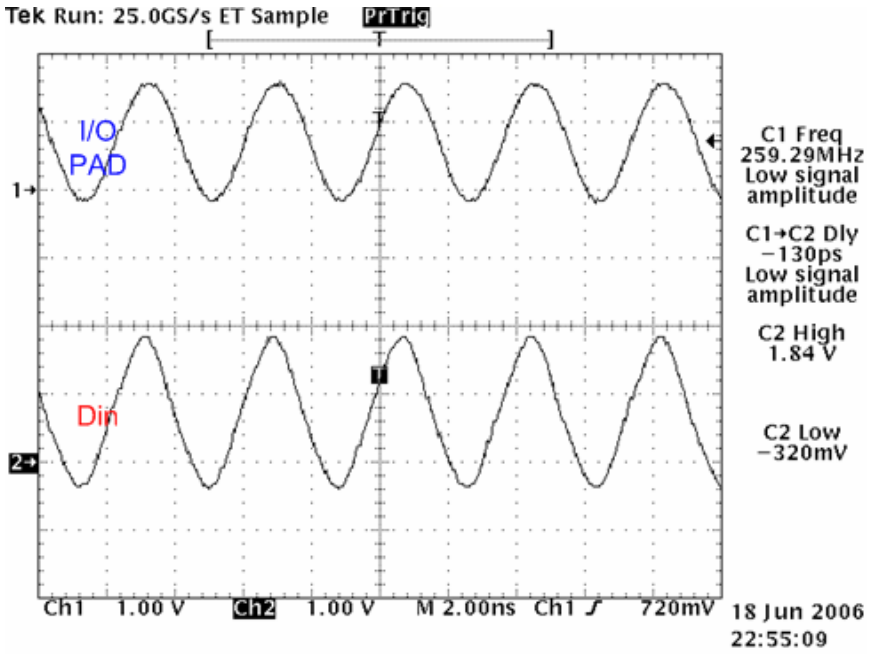
Fig. 3.21 The PCB view of tested mixed-voltage I/O buffers.

3.5.2 Experimental Results for HCPMXIO

Fig. 3.22 and Fig. 3.23 show the measured waveforms of the proposed 2xVDD-tolerant I/O buffer with hot-carrier-prevented circuit (HCPMXIO) in the receive mode to receive the 1-MHz and 266-MHz input signals with voltage swings of 0-to-1.5V and 0-to-3.3V, respectively, at I/O PAD, where the input data can be successfully transmitted to Din with a voltage swing of 0-to-1.5V. The measured waveforms of the HCPMXIO in the transmit mode to transmit 1-MHz and 266-MHz signals with a voltage swing of 0-to-1.5V from Dout to I/O PAD are shown in Fig. 3.24, where the signals at Dout can be successfully transmitted to the I/O PAD with the same voltage swing. The input signals at Dout and I/O PAD are like sine waves due to the constraint of the driving ability in the pulse generator. From the measured results in Fig. 3.22 ~ Fig. 3.24, the new proposed 2xVDD-tolerant I/O buffer with hot-carrier-prevented circuit can be correctly operated in both receive mode and transmit mode. Finally, the measured parameters and layout area of prior designs, GTCMXIO and TSTMXIO, and HCPMXIO are list in Table 3.6. The new proposed design, HCPMXIO, has better performance than the TSTMXIO in timing delay.

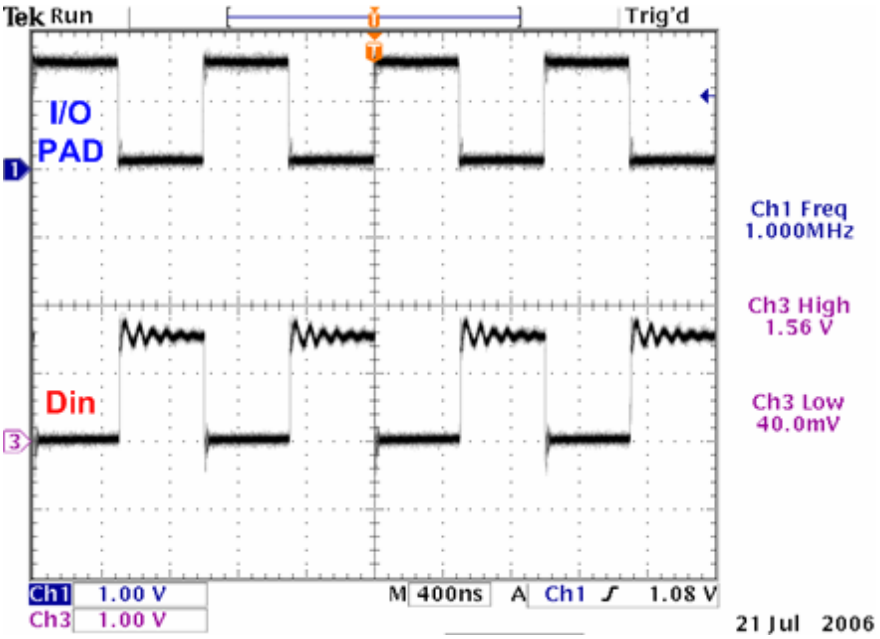


(a)

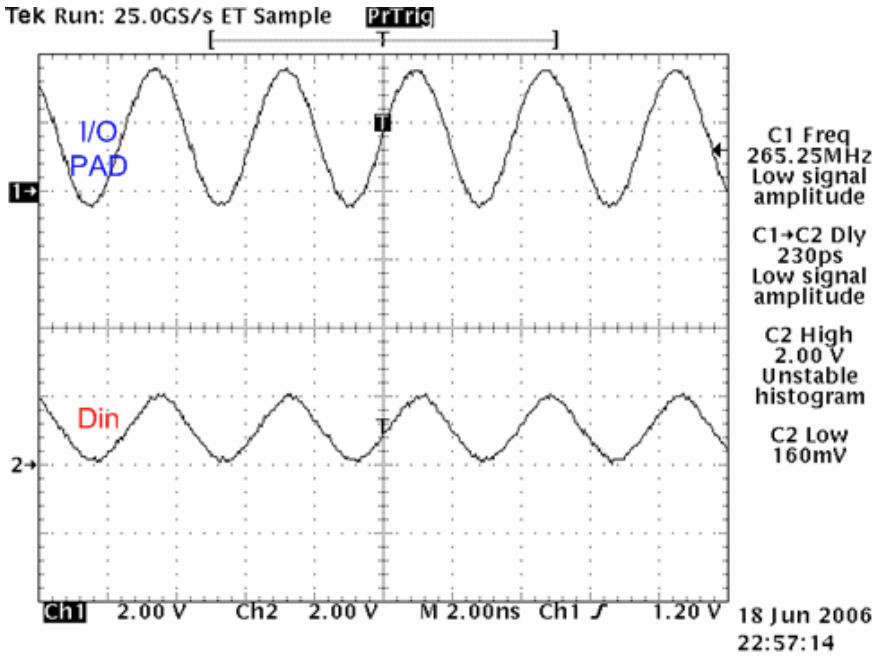


(b)

Fig. 3.22 Measured waveforms of the HCPMXIO operating at (a) 1 MHz and (b) 266 MHz when receiving 0V-to-1.5V input signals at I/O PAD.

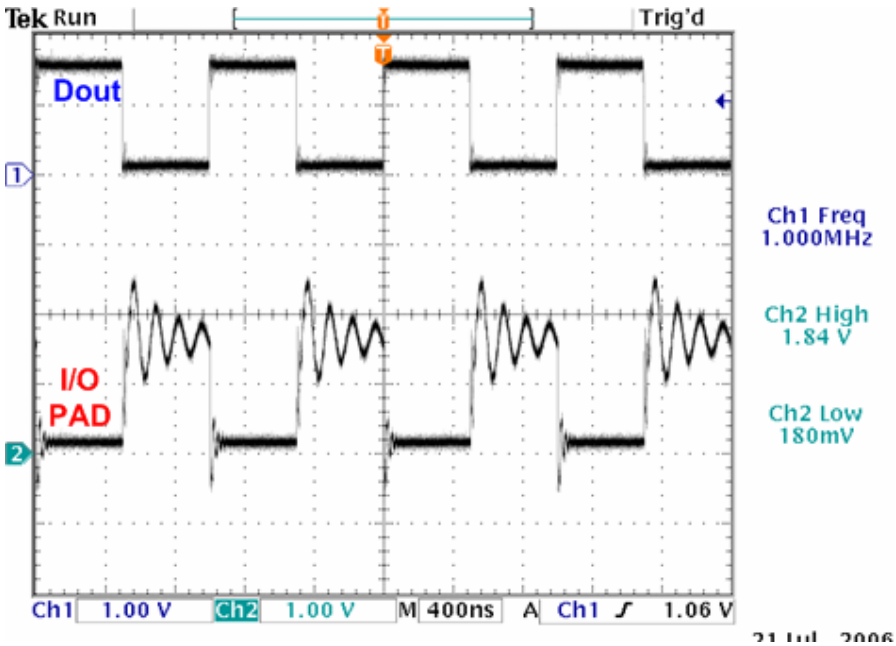


(a)

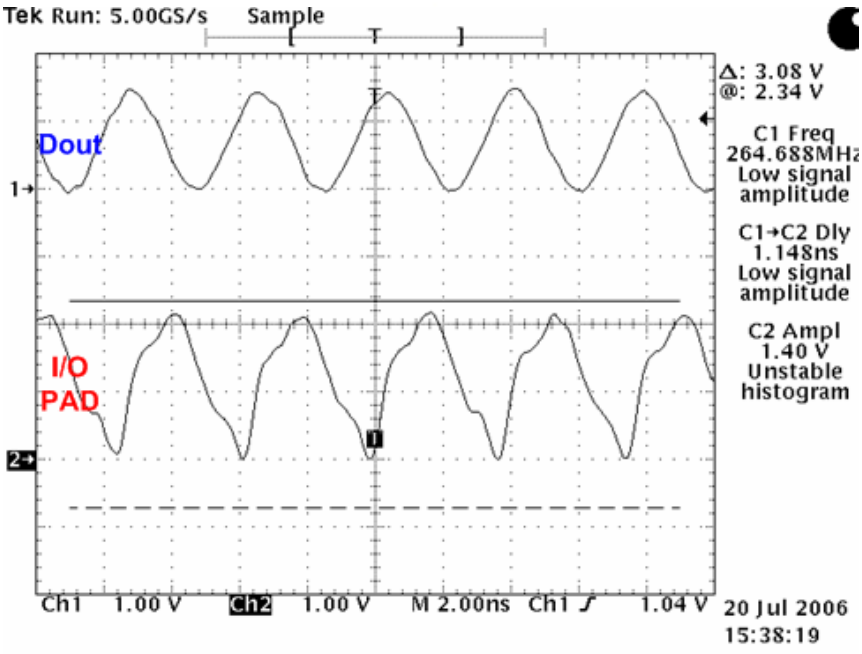


(b)

Fig. 3.23 Measured waveforms of the HCPMXIO operating at (a) 1 MHz and (b) 266 MHz when receiving 0V-to-3.3V input signals at I/O PAD.



(a)



(b)

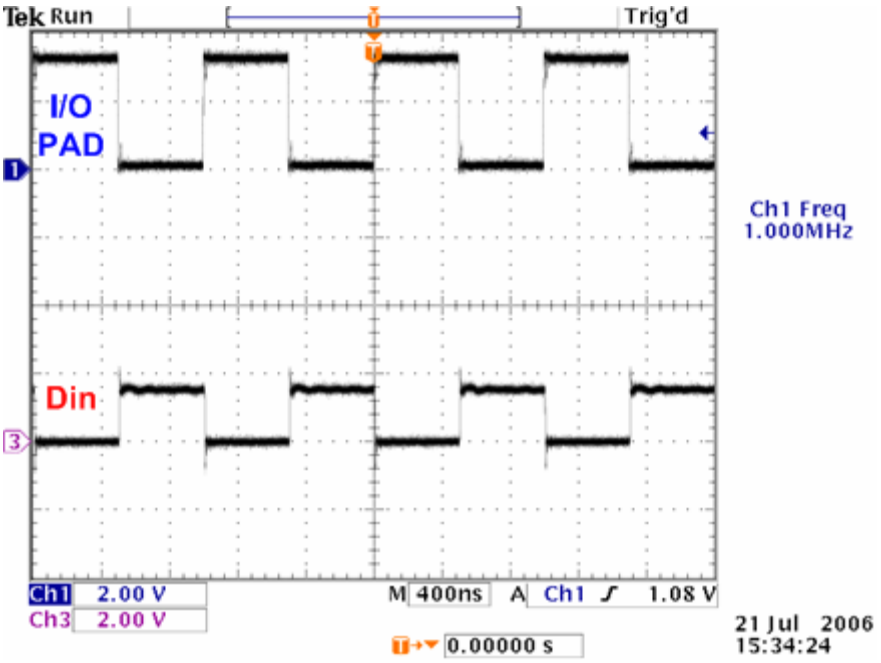
Fig. 3.24 Measured waveforms of the HCPMXIO operating at (a) 1 MHz and (b) 266 MHz when transmitting 0V-to-1.5V output signals to I/O PAD.

Table 3.6
The measured parameters of prior designs, GTCMXIO and TSTMXIO, and HCPMXIO.

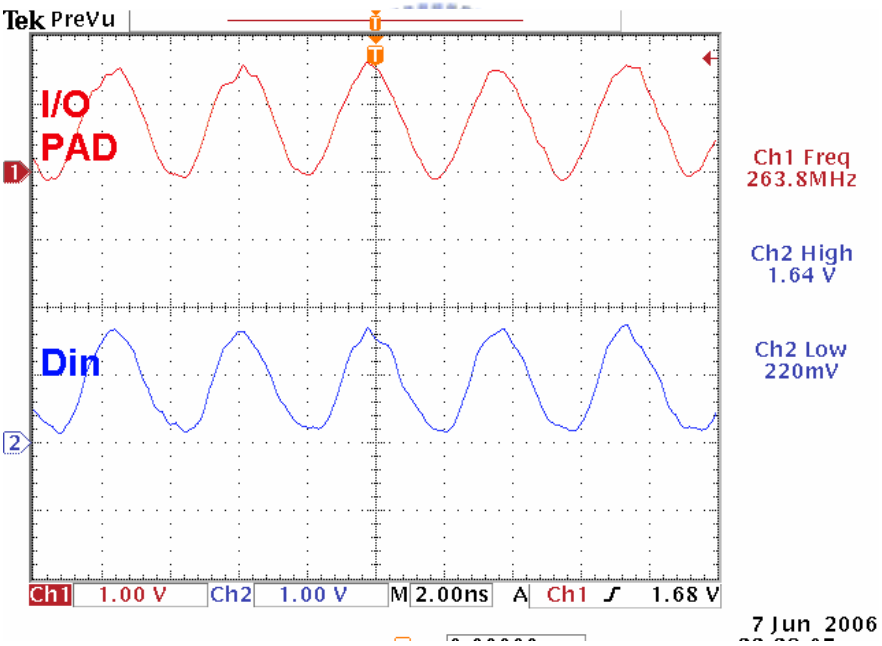
Parameters		GTCMXIO (Fig. 2.3)	TSTMXIO (Fig. 3.2)	HCPMXIO (Fig. 3.6)
Layout Area		140.6 μm × 48 μm	183.7 μm × 48 μm	191.6 μm × 51.4 μm
Receive Mode	T_{pr}	450 ps	200 ps	230 ps
	Power Consumption	30 μW/MHz	15 μW/MHz	47 μW/MHz
Transmit Mode	T_{pt}	2.29 ns	2.63 ns	2.45 ns
	Power Consumption	59 μW/MHz	58 μW/MHz	60 μW/MHz

3.5.3 Experimental Results for TBNMXIO

Fig. 3.25 and Fig. 3.26 show the measured waveforms of new proposed TBNMXIO in the receive mode to receive the 1-MHz and 266-MHz input signals with voltage swing of 0-to-1.5V and 0-to-3.3V at I/O PAD, respectively, where the input data are successfully transmitted to Din with a voltage swing of 0-to-1.5V. The measured waveforms of the HCPMXIO in the transmit mode to transmit 1-MHz and 266-MHz signals with a voltage swing of 0-to-1.5V from Dout to I/O PAD are shown in Fig. 3.27, where the signals at Dout are successfully transmitted to the I/O PAD with the same voltage swing. The measured parameters are summarized in Table 3.7 comparing the TBNMXIO with prior design SBNMXIO. The power consumption of the TBNMXIO is almost double than that of the SBNMXIO since the long rise/fall time of input signals causes large dc power consumption in dynamic gate-controlled circuit.

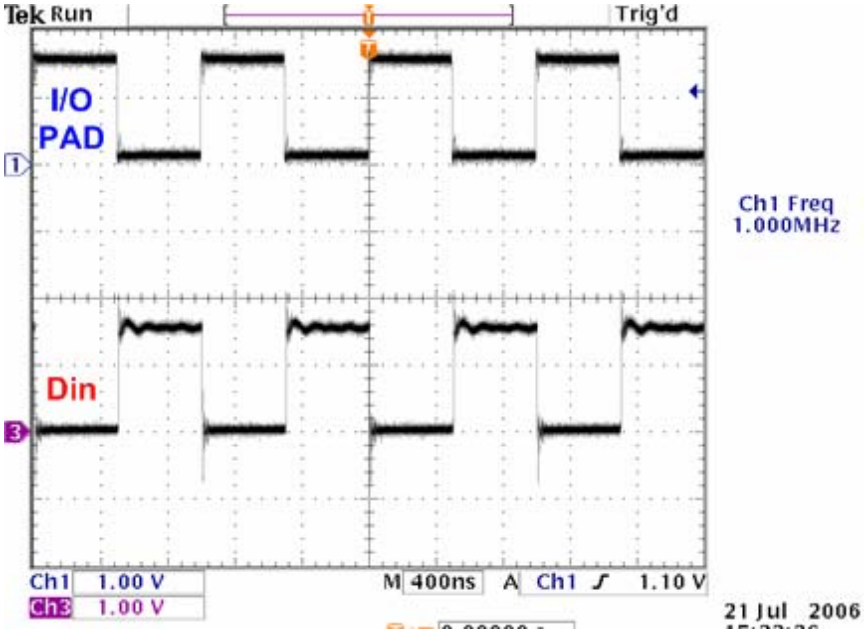


(a)

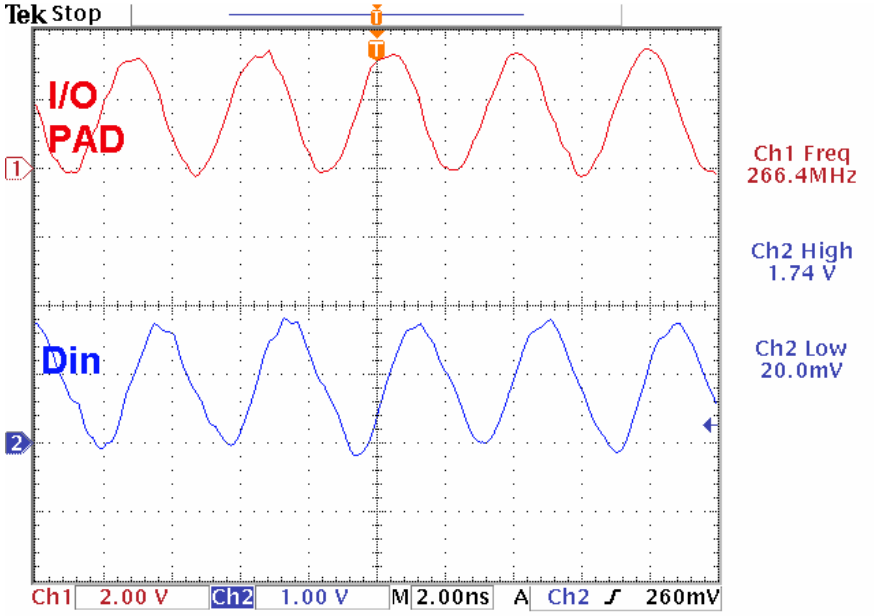


(b)

Fig. 3.25 Measured waveforms of the TBNMXIO operating at (a) 1 MHz and (b) 266 MHz when receiving 0V-to-1.5V input signals at I/O PAD.

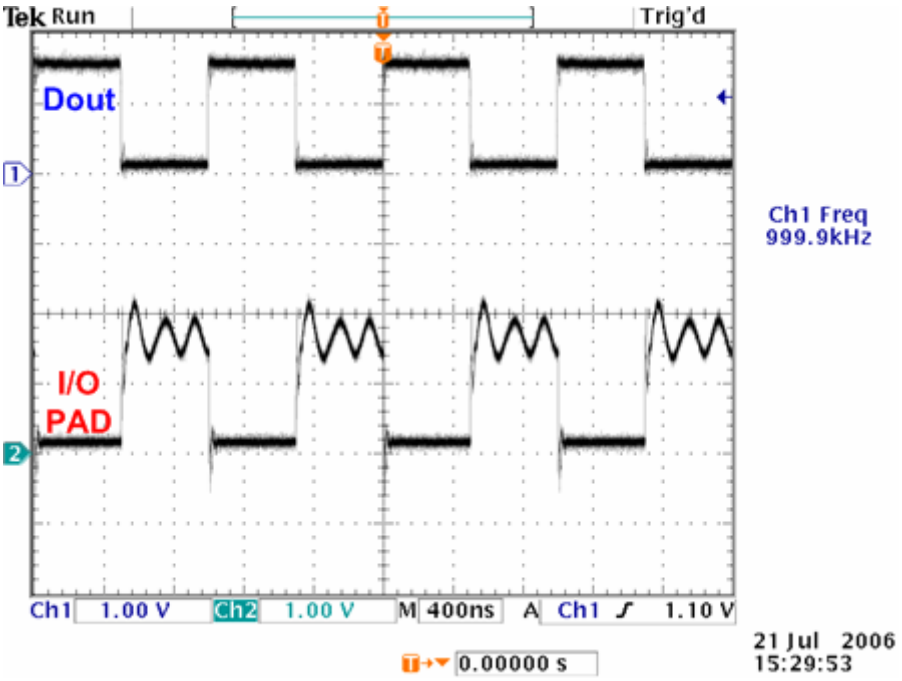


(a)

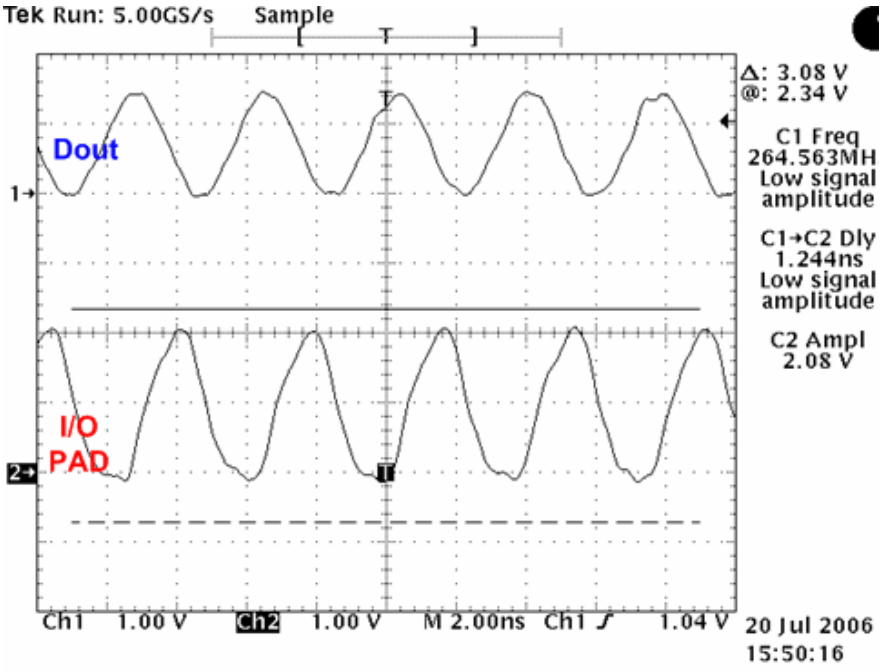


(b)

Fig. 3.26 Measured waveforms of the TBNMXIO operating at (a) 1 MHz and (b) 266 MHz when receiving 0V-to-3.3V input signals at I/O PAD.



(a)



(b)

Fig. 3.27 Measured waveforms of the TBNMXIO operating at (a) 1 MHz and (b) 266 MHz when transmitting 0V-to-1.5V output signals to I/O PAD.

Table 3.7
The measured parameters of SBNMXIO and TBNMXIO.

Parameters		SBNMXIO (Fig. 2.4)	TBNMXIO (Fig. 3.13)
Layout Area		139.6 μm × 49.3 μm	169.2 μm × 53.8 μm
Receive Mode	T_{pr}	583 ps	663 ps
	Power Consumption	15 μW/MHz	30 μW/MHz
Transmit Mode	T_{pt}	2.55 ns	2.75 ns
	Power Consumption	67 μW/MHz	121 μW/MHz

3.6 DISCCUSION AND SUMMARY

3.6.1 Discussion

In section 3.5, it is found that the measured waveforms of mixed-voltage I/O buffers do not conform to the simulation results. This is because the measured waveforms are shaped by the transmission line effect. A transmission line model which comprises an internal capacitive load of 2 pF, wire bond inductance of 7 nH and output load of 10 pF should be added into the SPICE simulation. The simulation model of I/O cell with transmission line models and wire bond inductance on power pads is shown in Fig. 3.28. For example, the simulation waveforms of the HCPMXIO (new design I) in transmit mode with an operating speed of 266 MHz are shown in Fig. 3.29. As Fig. 3.29 shows, the output waveform on I/O PAD overshoots and undershoots due to the transmission line and bounding wire effects.

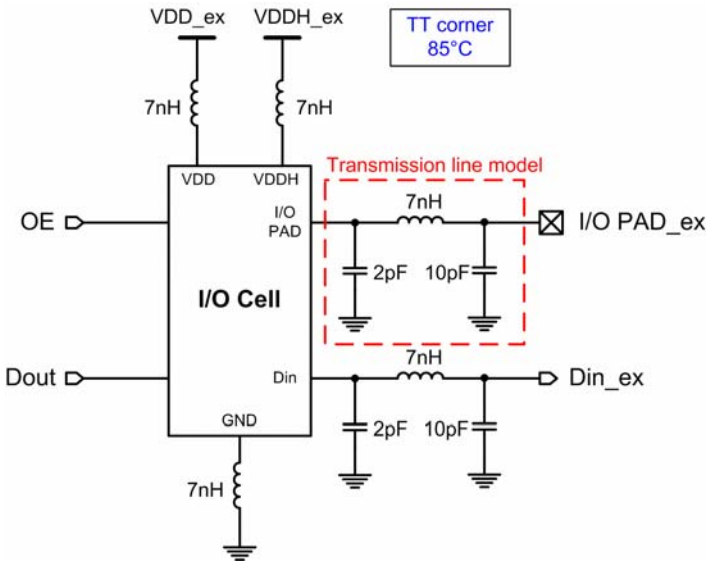


Fig. 3.28 Modified simulation model with bonding wire and transmission line effects.

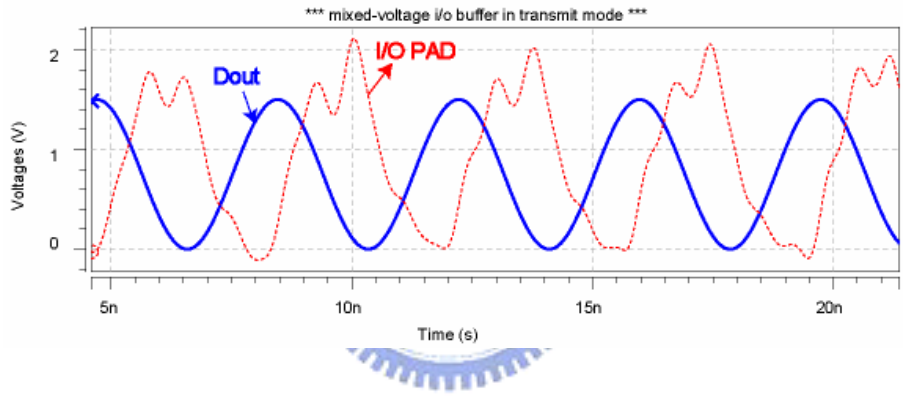


Fig. 3.29 Simulation waveforms of the HCPMXIO with transmission line effect in transmit mode with an operating speed of 266 MHz.

3.6.2 Summary

Two new mixed-voltage I/O buffers, HCPMXIO and TBNMXIO, have been proposed in this chapter without suffering hot-carrier degradation. Both two designs have been fabricated in a 0.18-μm CMOS process with only thin-oxide devices and designed to meet PCI-X 2.0 applications. The hot-carrier degradation on mixed-voltage I/O buffers is eliminated by using circuit technique. The circuit techniques to solve hot-carrier degradation can be applied to the general 2xVDD-tolerant I/O buffers.

Chapter 4

Mixed-Voltage I/O Buffers with Slew-Rate Control

4.1 INTRODUCTION

Signal and power integrity are crucial problems in VLSI systems. Modern trends in deep sub-micron circuit designs, such as high operating frequencies, short rise/fall times, and lower supply voltage, exacerbate this problem. Output buffers provide an interface for driving mainly capacitive and inductive external loads. The capacitive load typically consists of the bonding wire, the pin, the conductors on the PCB and the input capacitances of the connected gates. The inductive load usually comprises the package parasitic series inductances of the power and ground lines supplying the output buffer, connected to the external power and ground rails on the PCB. A major component of the circuit noise is the inductive noise. Ground bounce, also known as simultaneous switching noise (SSN) or delta-I noise, is a voltage glitch induced at power/ground (P/G) distribution connections due to switching currents passing through either wire/substrate inductance or package lead inductance associated with power or ground rails. When the current flows through the inductance L, a voltage drop as eq. (4-1 is induced.

$$V = L\frac{di}{dt} \tag{4-1}$$

In output buffer design, the transistors sizing is imposed by DC interfacing constraints. This leads to several problems [27]:

- unacceptable high current peaks which occur with the simultaneous

switching of many output buffers;

- inductive power supply noise which results in large voltage drops;
- electromagnetic interference (EMI) due to high output edge switching rates.

The resulting noise voltage can potentially cause spurious transitions at the inputs of devices sharing the same power and ground rails. Therefore, controlling the output voltage variations is generally required to limit the crosstalk and reduce the inductive power supply noise to an acceptable value. Besides, the effect of ground bounce in output buffer can be simply modeled as an inductor shown in Fig. 4.1 [28].

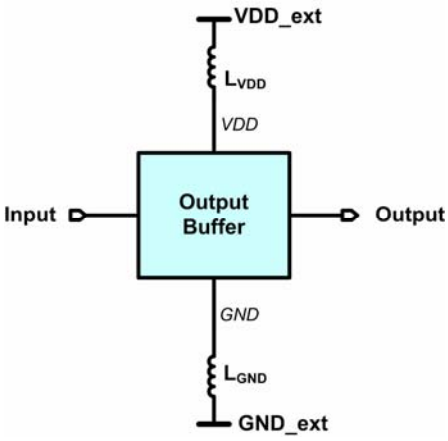


Fig. 4.1 The model for ground bounce effect.

4.2 SLEW-RATE CONTROL IN TYPICAL I/O BUFFERS

4.2.1 Conventional Slew-Rate Control

To solve these problems, a reduction of the slew rate in the output edges is preferred as far as the speed specification is satisfied [29]. A simple approach is to slow down the turn-on time of the output switching transistor through an access resistor to the transistor gate. Furthermore, the output driver can be divided into

several parallel output drivers for ground bounce reduction and slew-rate control. An output buffer with conventional slew-rate control, which is a three-step slew-rate control circuit, is shown in Fig. 4.2 [19]. The parallel output transistors of slew-rate controlled output buffer turn on progressively through delay elements implemented by resistors or transmission gates. This helps reduce the slew rate of output buffer and therefore the ground and power bounce. However, the output transistors turn off step by step as output transistors turn on. Therefore, the circuit consumes unnecessary power resulting from short-circuit current. For low power consideration, another slew-rate controlled topology should be introduced.

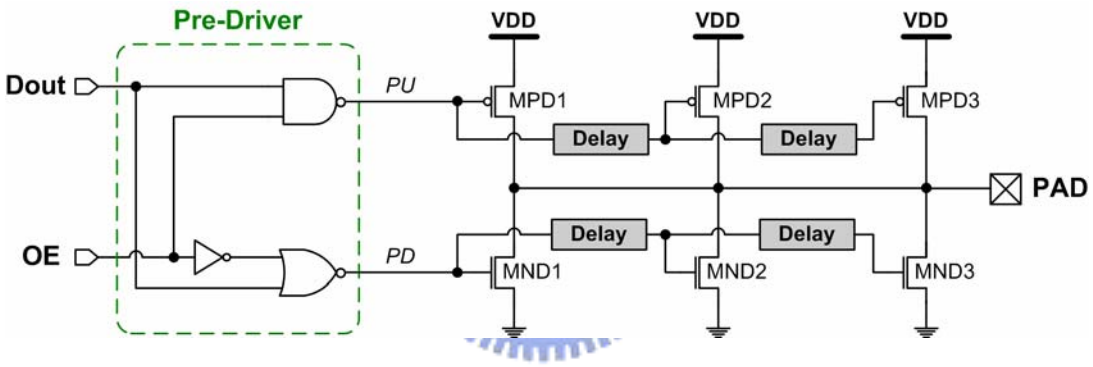


Fig. 4.2 Output buffer with conventional slew-rate control.

4.2.2 Improved slew-rate control to reduce short-circuit current

Fig. 4.3 shows an output buffer with improved slew-rate control to reduce short-circuit current [19]. The output transistors are divided into three parts with their corresponding gate-controlled signals generated by slew-rate control. The transistors MN1 and MP1 in Fig. 4.3 are used to control CMOS output driver to turn it on. Note that the pull-up signal (*PUb*) and pull-down signal (*PDb*) are the inverse of those (*PU* and *PD*) in previously mentioned designs, such as the designs in Fig. 3.5 and Fig. 3.13. When the output buffer is operating in transmit mode (OE=VDD), the transmission

gates are used as resistive elements to turn on each individual output transistor gradually. As the output buffer is operating in tri-state mode, the output transistors are quickly turned off by the transistors MP2-MP4 and MN2-MN4. As a result, this slew-rate control is compatible for low power design. This structure of slew-rate control is redesigned for mixed-voltage I/O buffers proposed in this thesis.

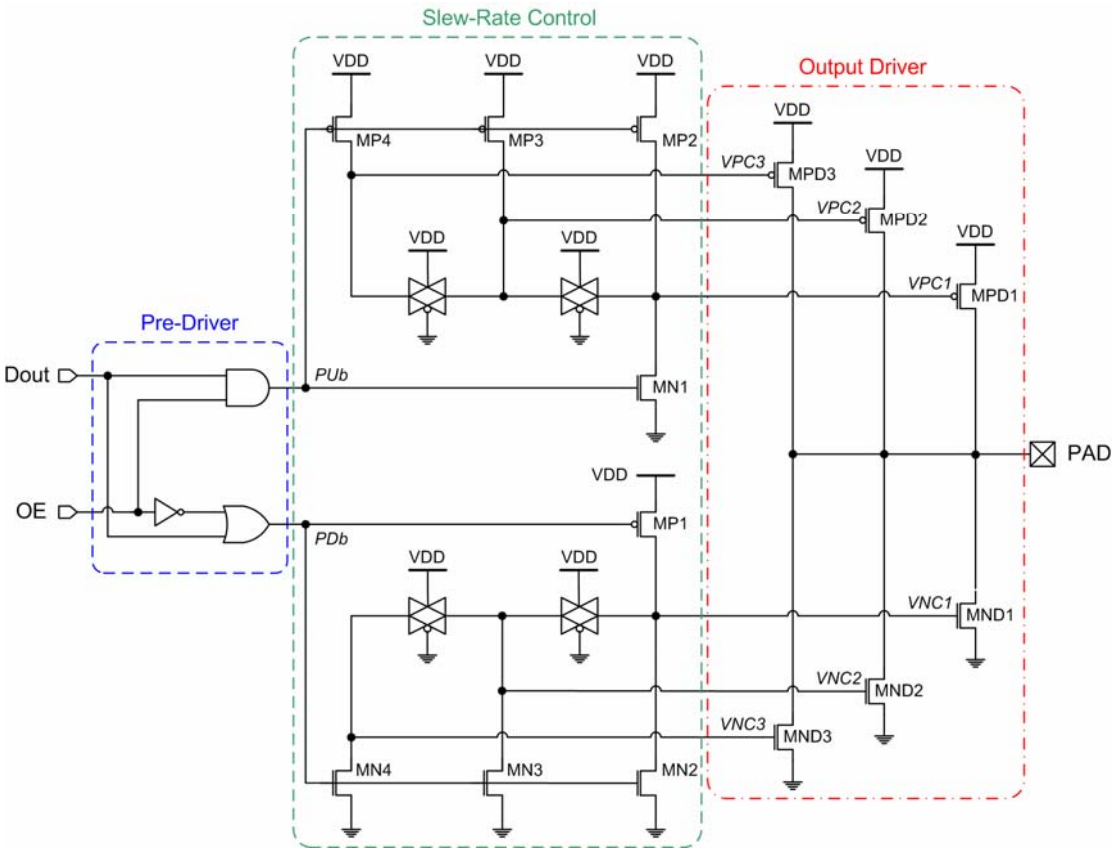


Fig. 4.3 Output buffer with an improved slew-rate control to reduce short-circuit current.

4.3 SLEW-RATE CONTROL ON THE TBNMXIO

4.3.1 Circuit Implementation

In section 3.4, a 2xVDD-tolerant I/O buffer with two blocking NMOS devices and dynamic gate-controlled circuit (TBNMXIO) has been proposed without

hot-carrier degradation. The blocking NMOS devices protect the I/O buffer from gate-oxide degradation and hot-carrier degradation. In Fig. 3.13, since the gate terminals of transistor MP0 and MN0 are switched either to VDD or to 0V, the mechanism of slew rate control in Fig. 4.3 can be applied into TBNMXIO without modifications. The TBNMXIO with slew-rate control is shown in Fig. 4.4 and its dynamic gate-controlled circuit has been shown in Fig. 3.14. This 2xVDD-tolerant I/O buffer with slew-rate control is labeled as TBNMXIO-SR to be a contrast with TBNMXIO, which has no slew-rate control.

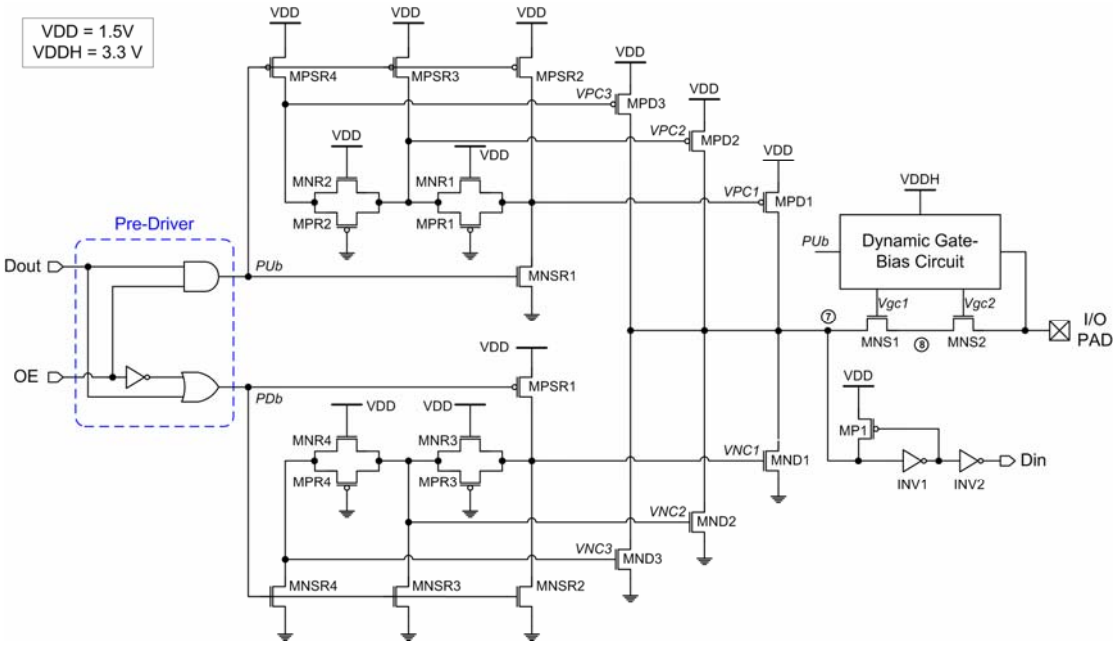


Fig. 4.4 The TBNMXIO with slew-rate control.

4.3.2 Simulation Results

Again, this I/O buffer with slew-rate control is designed to meet PCI-X 2.0 applications, thus VDD is 1.5V and VDDH is 3.3V. The TBNMXIO-SR has been verified in a 0.18-μm CMOS process by SPICE simulation. The simulation waveforms of the TBNMXIO-SR with an operating speed of 266 MHz in transmit

mode are shown in Fig. 4.5. The gate-controlled signals of MPD1-MPD3, *VPC1*, *VPC2* and *VPC3*, are pulled to 0V one by one as the 2xVDD-tolerant I/O buffer transmits VDD output signal to I/O PAD. On the contrary, when 0-V output signal is transmitted to I/O PAD, the *VPC1*, *VPC2* and *VPC3* are quickly pulled up to VDD to turn off transistors MPD1-MPD3. Similarly, the gate-controlled signals of MND1-MND3, *VNC1*, *VNC2* and *VNC3*, are progressively pulled up to VDD in transmitting 0-V output signal and quickly pulled down to 0V to turn off transistors MND1-3 in transmitting VDD output signal. As a result, the TBNMXIO-SR transmits data with mitigated switching current and consumes extra power a little for slew-rate controlled circuit.

Table 4.1 summarizes the simulation results of the TBNMXIO-SR with the TBNMXIO, which has no slew-rate control. The timing specifications of mixed-voltage I/O buffer with slew-rate control are some what larger than those of mixed-voltage I/O buffer without slew-rate control. Also, the driving currents of TBNMXIO-SR are smaller than those of TBNMXIO due to the slew-rate control. As shown in Table 4.1, the slew rate control in TBNMXIO-SR does not consume extra power too much.

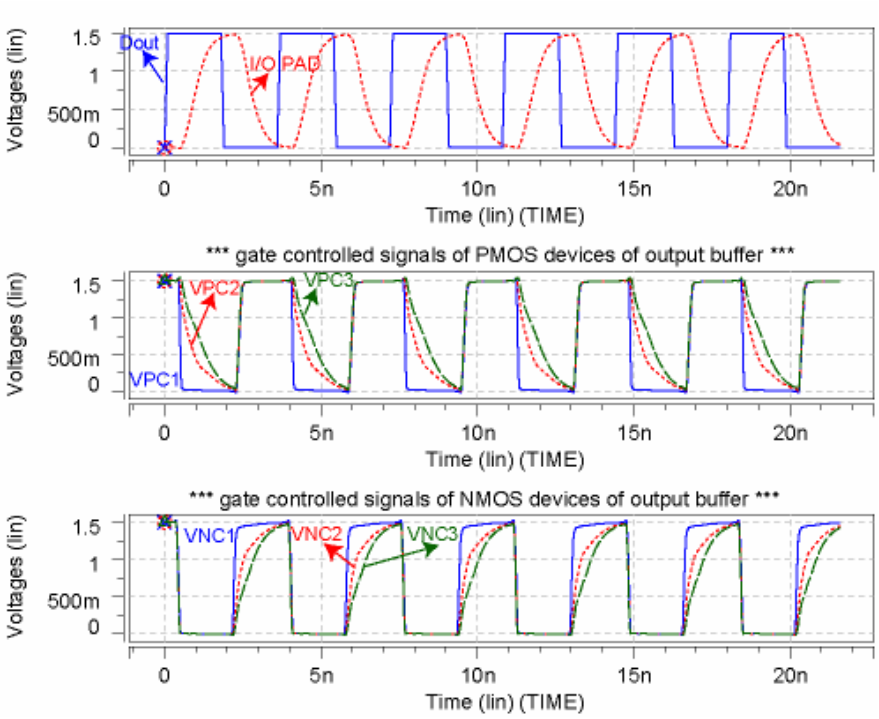


Fig. 4.5 Simulation waveforms of the TBNMXIO-SR operating at 266 MHz when transmitting 0V-to-1.5V output signals to I/O PAD.

Table 4.1

The simulation results of TBNMXIO with/without slew-rate control.

Parameters		TBNMXIO (Fig. 3.13)	TBNMXIO-SR (Fig. 4.4)
Slew-Rate Control		No	Yes
I_{OL} at V_{OL}=0.15 V		5.6 mA	5.0 mA
I_{OH} at V_{OH}=1.35 V		5.9 mA	5.8 mA
Receive Mode	T_{rise}	453 ps	452 ps
	T_{fall}	417 ps	416 ps
	T_{pr}	888 ps	885 ps
	Power Consumption	31 μW/MHz	31 μW/MHz
Transmit Mode	T_{rise}	664 ps	846 ps
	T_{fall}	627 ps	825 ps
	T_{pt}	784 ps	925 ps
	Power Consumption	67 μW/MHz	68 μW/MHz

4.3.3 Ground Bounce

In order to verify the reduction of ground bounce by slew-rate control, a model for ground bounce effects is shown in Fig. 4.6. The inductances of wire bonds vary from 7 nH to 15 nH in the simulation for typical cases. Since the switching currents of mixed-voltage I/O buffers in transmit mode are much larger than that in receive mode, the ground bounce effects are simulated in transmit mode for clear illustration. The simulation waveforms of ground bounce effects on power lines are shown in Fig. 4.7 and several parameters are defined as follows:

- VDD_ext/GND_ext: External power supply;
- VDD_max/VDD_min: maximum/minimum value of VDD power line;
- GND_max/GND_min: maximum/minimum value of GND power line;
- ΔV_{VDD_over}: overshoot on VDD power line (VDD_max-VDD_ext);
- ΔV_{VDD_under}: undershoot on VDD power line (VDD_ext-VDD_min);
- ΔV_{GND_over}: overshoot on GND power line (GND_max-GND_ext);
- ΔV_{GND_under}: undershoot on GND power line (GND_ext-GND_min).

The ΔV_{VDD_under} and ΔV_{GND_over} among these parameters are the major concerns since these two terms may result in increasing timing delay and even logic errors on transmitted signals.

The simulation waveforms of TBNMXIO-SR which is operated in transmit mode with an operating speed of 266 MHz are shown in Fig. 4.8. The signals on I/O PAD are like sine wave due to the ground bounce effect. The simulation results with variation of wire bond inductance on VDD power line and GND power line are shown in Fig. 4.9 and Fig. 4.10, respectively. Since the current supplied from VDDH is much smaller than that from VDD, only ground bounce effect on VDD is shown. As shown in Fig. 4.9 and Fig. 4.10, the TBNMXIO-SR improves the ground bounce effects greatly.

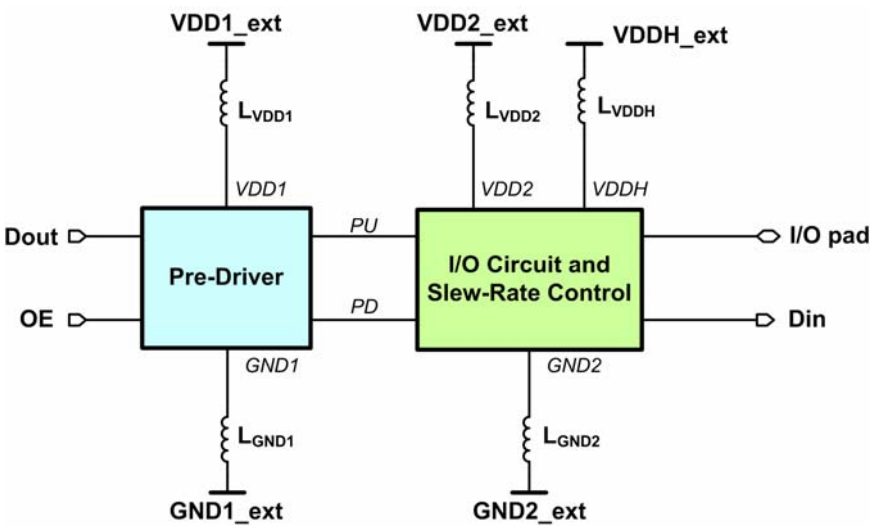


Fig. 4.6 Simulated model of ground bounce.

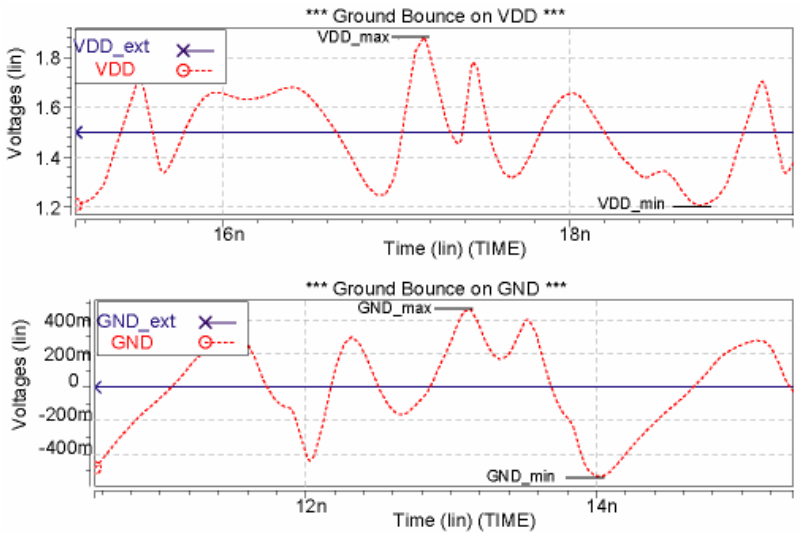


Fig. 4.7 Simulation waveforms of ground bounce effects on power lines.

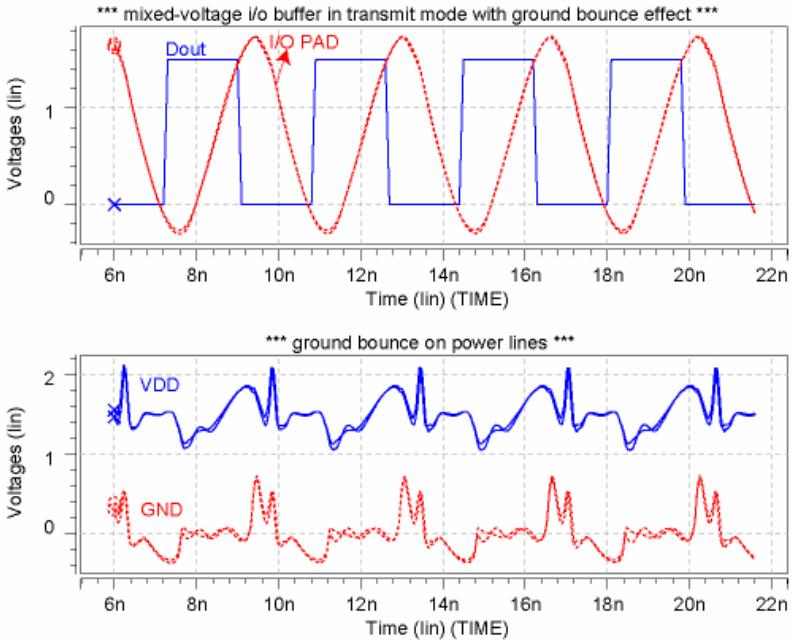
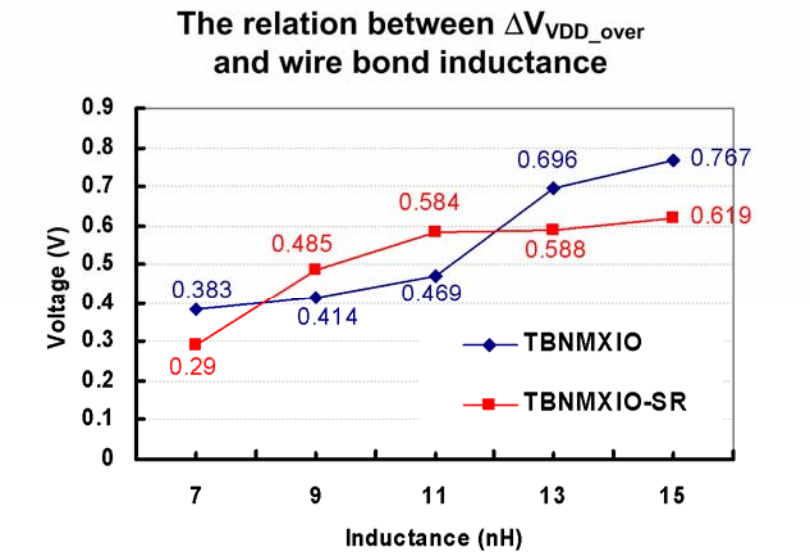
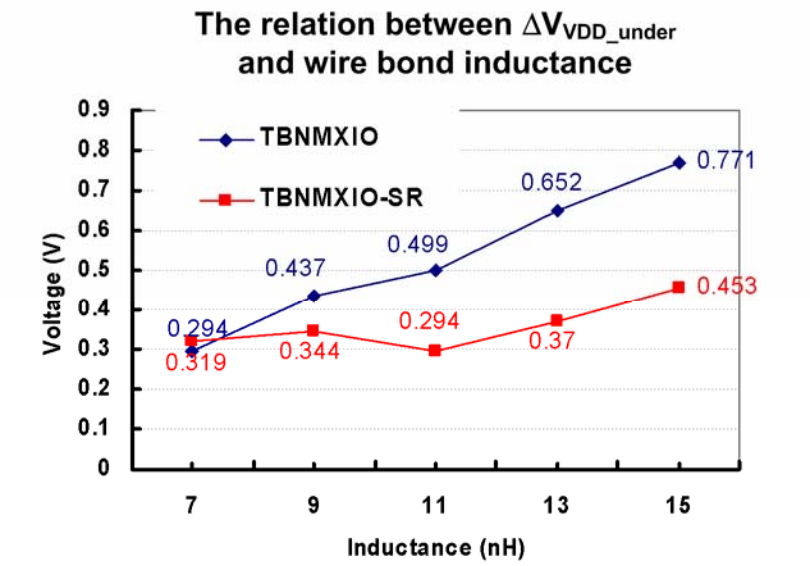


Fig. 4.8 Simulation waveforms of the TBNMXIO-SR with ground bounce effect in transmit mode.

The simulation waveforms of TBNMXIO-SR which is operated in transmit mode with an operating speed of 266 MHz are shown in Fig. 4.8. The signals on I/O PAD are like sine wave due to the ground bounce effect. The simulation results with variation of wire bond inductance on VDD power line and GND power line are shown in Fig. 4.9 and Fig. 4.10, respectively. Since the current supplied from VDDH is much smaller than that from VDD, only ground bounce effect on VDD is shown. As shown in Fig. 4.9 and Fig. 4.10, the TBNMXIO-SR improves the ground bounce effects greatly. From Fig. 4.9, it is found that the overshoot of power noise in the TBNMXIO-SR was not improved greatly since the PMOS devices in output driver were turned off simultaneously by slew-rate control.

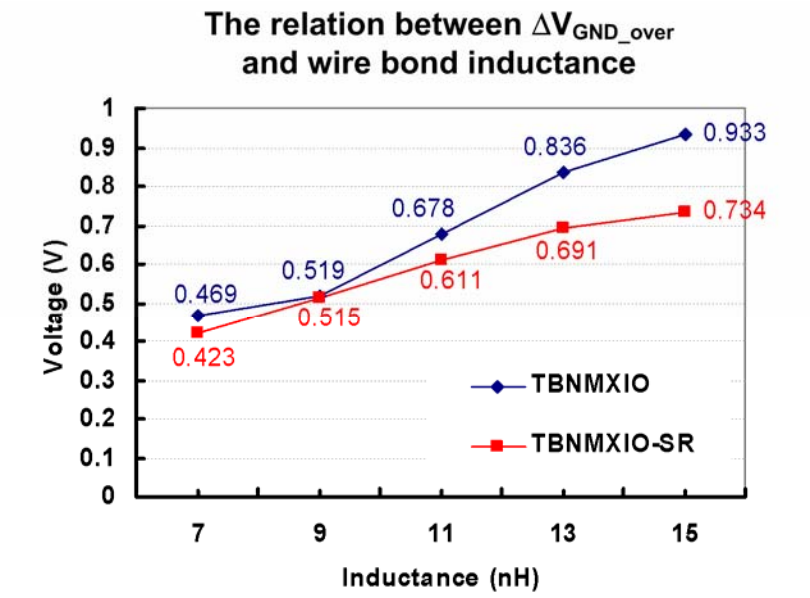


(a)

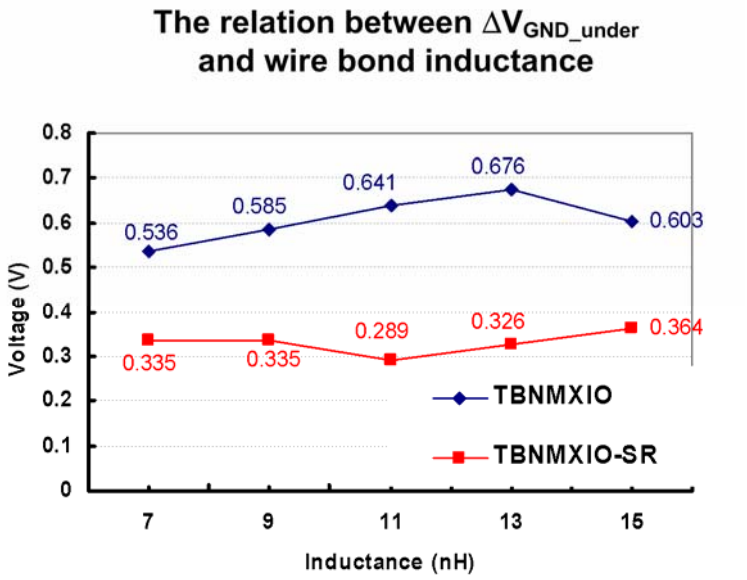


(b)

Fig. 4.9 The relation between ground bounce on VDD power line and wire bond inductance on the TBNMXIO and TBNMXIO-SR. (a) The overshoot and (b) the undershoot on VDD power line.



(a)



(b)

Fig. 4.10 The relation between ground bounce on GND power line and wire bond inductance on the TBNMXIO and TBNMXIO-SR. (a) The overshoot and (b) the undershoot on GND power line.

4.4 SLEW-RATE CONTROL ON THE HCPMXIO

4.4.1 Reliability Issues

Fig. 4.11 shows the HCPMXIO with the structure of slew rate control in Fig. 4.3. Also, the output transistors MN0, MN1 and MP0 are divided into three individual parts. The transistors MN2 and MP2 in Fig. 3.5 are omitted since the gate terminal of transistor MP0 has been connected to the slew-rate control. The hot-carrier-prevented circuit for transistors MN0 and MN3 are shown in Fig. 4.11 (b) and (c), respectively. Note that the bulks of the PMOS transistors MPSR2-MPSR4 in slew-rate control are connected to the floating n-well bias circuit (nwell) to avoid leakage paths from drain terminals of transistors MPSR2-4 to power supply (VDD) through the parasitic drain-to-well pn-junction diode in the MPSR2-4.

When the 2xVDD signal is received at I/O PAD, the gate-controlled signals of transistors MPD1-MPD3 are pulled up to 2xVDD through transistors MP31-MP33. However, the gate-controlled signal of transistors MPSR2-MPSR4, *PUb*, is set to 0V by pre-driver at this time. Thus, the absolute gate-drain voltages ($|V_{gd}|$) of transistors MPSR2-MPSR4 are as high as 2xVDD resulting in gate-oxide degradation. Besides, the transistors MPR1 and MPR2 suffer gate-oxide degradation as the I/O buffer receives 2xVDD input signals. In the transition from receiving 2xVDD input signal to transmitting VDD output signal the MPR1, MPR2, MNR1, and MNR2 suffer hot-carrier degradation. Since the gate-controlled signal of transistor MPD1 is pulled up to 2xVDD through transistor MP31 and *PUb* is set to 0V in this condition, the transistor MNSR1, which is used to control CMOS output driver, suffers gate-oxide degradation and hot-carrier degradation, too. As a result, the slew-rate control should be redesigned to be compatible with the HCPMXIO without suffering gate-oxide degradation and hot-carrier degradation.

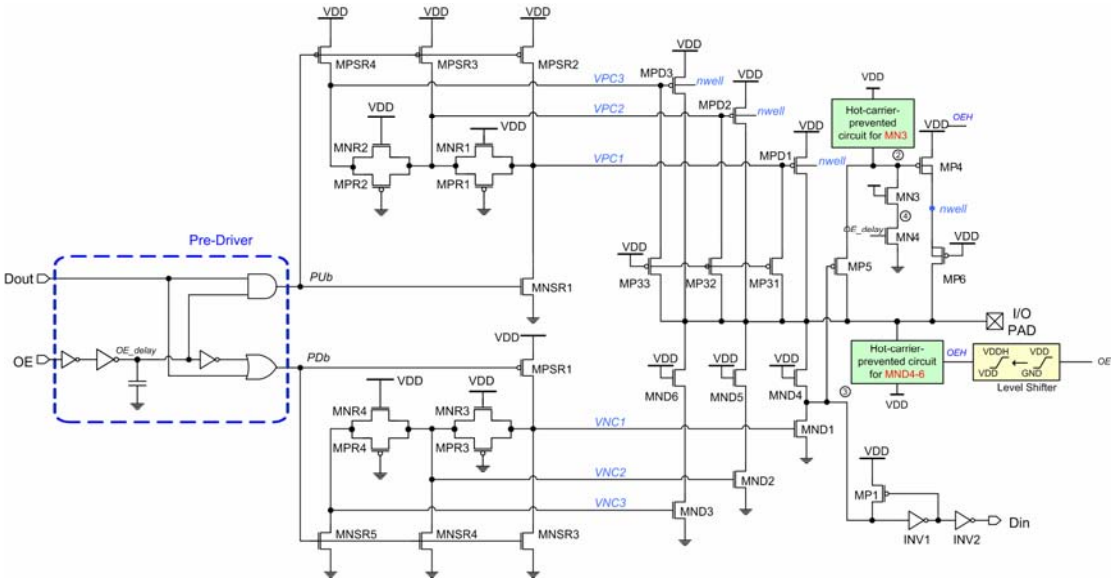


Fig. 4.11 (a) The mixed-voltage I/O buffer based on the HCPMXIO with slew-rate control. (b) The hot-carrier-prevented circuit for transistor MN0 ,and (c) the hot-carrier-prevented circuit for transistor MN3.

4.4.2 New Slew-Rate Control on Mixed-Voltage I/O Buffer

A robust mixed-voltage I/O buffer with modified slew-rate control is proposed in Fig. 4.12 and called HCPMXIO-SR. The hot-carrier-prevented circuits for transistors

MN0 and MN3 have been shown in Fig. 4.11 (b) and (c). The NMOS transistors MNSR6-MNSR8 are used to protect transistors MPSR2-MPSR4 from gate-oxide degradation and avoid leakage currents as the HCPMXIO-SR receives 2xVDD input signals. The gate-controlled signal of transistors MPSR6-MPSR8, *PDH*, is high-level version of pull down signal, *PD*, shifted by the level shifter. Furthermore, the transistor MNSR2 is used to protect transistor MNSR1 from gate oxide degradation and hot-carrier degradation as the mixed-voltage I/O buffer receives 2xVDD input signal. Since the transmission gates MNR1/MPR1 and MNR2/MPR2 are mainly used to propagate 0-V signal to turn on PMOS output transistors, MPD1-MPD3, one by one, the PMOS transistors MPR1 and MPR2 can be omitted and consequently only NMOS transistors are used as resistive elements. As a result, the resistive elements do not suffer gate-oxide degradation mentioned in the previous section. Similarly, the transistors MNR3 and MNR4 can be omitted. When the mixed-voltage I/O buffer receives 0-V input signal at I/O PAD, the *PD* signal is set to 0V and consequently *PDH* signal is set to VDD. At this time, the gate-controlled signals of transistors MPD1-MPD3, *VPC1-VPC3*, are biased at "VDD-V_{th}" due to weakly turned-on transistors MPSR6-8, thus results in subthreshold leakage currents on transistors MPD1-MPD3. To avoid this problem, the gate-controlled signals of transistors MPD1-MPD3 are pulled up to VDD through the transistors MP34-MP36 in Fig. 4.12 as 0-V input signal is received at I/O PAD. Note that the bulks of PMOS devices and NMOS devices in the new slew rate control are connected to VDD and GND, respectively. The bulks of transistors from MP31 to MP36 are connected to the n-well bias circuit (nwell).

The operations of this HCPMXIO-SR are list in Table 4.2. When the HCPMXIO-SR is operated in receive mode, the *PUb* and *PDb* signal are 0V and VDD, respectively, to turn off output driver. In the meanwhile, the *PDH* signal is set

to VDD by level shifter. The transistors MP31 and MP34 comprise the gate tracking circuit of transistor MPD1 as the I/O buffer is operating in receive mode. Similarly, transistors MP32/MP35 and MP33/MP36 are the gate-tracking circuit of transistor MPD2 and MPD3, respectively. As 2xVDD input signal is receive at I/O PAD, the *VPC1*, *VPC2* and *VPC3* are set to 2xVDD through transistors MP31, MP32 and MP33. On the contrary, the *VPC1*, *VPC2* and *VPC3* are set to VDD through transistors MP34, MP35 and MP36. As a result, the input signals can be received successfully without gate-oxide reliability problem and leakage currents. If the mixed-voltage I/O buffer is transmitting 0-V output signal, the *PDb* signal is set to 0V, and consequently transistor MPSR1 is turned on to propagate VDD signal to gate terminals of transistors MND1-MND3 through transistors MPR3 and MPR4. In the meanwhile, the PDH signal is set to 2xVDD, thus the VDD signals can be transmitted to the gate terminals of transistors MPD1-MPD3 through transistors MNSR6-MNSR8 successfully. As a result, transistors MPD1-MPD3 are quickly turned off. On the other hand, if VDD output signal is transmitted from Dout to I/O PAD, the *PUb* signal is pulled up to VDD to turn on transistor MNSR1. The 0-V signal consequently is propagated to *VPC2* and *VPC3* through transistors MNR1 and MNR2. The PMOS transistors MPD1, MPD2 and MPD3 are turned on one by one to pull up I/O PAD to VDD. In the same condition, the *PDb* signal is set to VDD to turn on transistors MNSR3-MNSR5, thus NMOS transistors MND1, MND2 and MND3 are quickly turned off. As the foregoing descriptions, this HCPMXIO-SR can be successfully operated in both receive mode and transmit mode without gate-oxide degradation and hot-carrier degradation. Furthermore, the mechanism of hot-carrier-prevented circuit in Fig. 3.4 can be applied in transistor MNSR2 to avoid hot-carrier degradation during the transition from receiving 2xVDD input signal to transmitting VDD output signal.

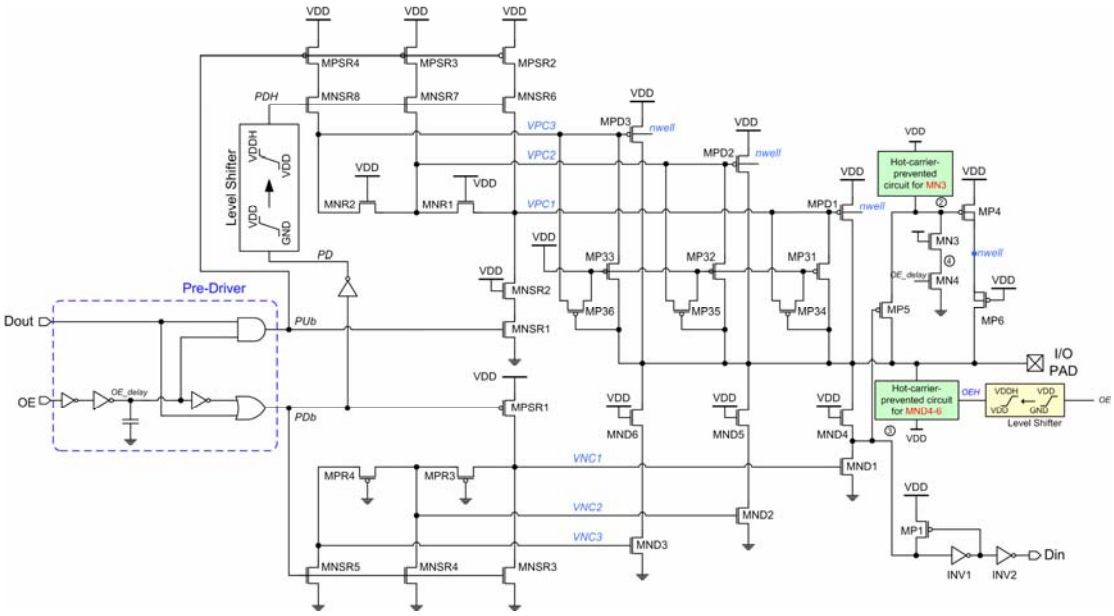


Fig. 4.12 The HCPMXIO with modified slew-rate control.

Table 4.2

The operations of the HCPMXIO-SR

Operating Modes	Signals at I/O PAD	*PUb*	*PDb*	*PDH*	*VPC1-VPC3*	*VNC1-VNC3*
Receive	Low (0V)	0V	VDD	VDD	VDD	0V
Receive	High (2xVDD)	0V	VDD	VDD	2xVDD	0V
Transmit	Low (0V)	0V	0V	2xVDD	VDD	VDD
Transmit	High (VDD)	VDD	VDD	VDD	0V	0V

4.4.3 Simulation Results

This HCPMXIO with slew-rate control is designed to meet PCI-X 2.0 applications, thus VDD is 1.5V and VDDH is 3.3V. The HCPMXIO-SR has been verified in a 0.18-μm CMOS process by SPICE simulation. The simulation waveforms of the new HCPMXIO-SR with an operating speed of 266 MHz in transmit mode are shown in Fig. 4.13. When the I/O buffer transmits VDD output

signal to I/O PAD, the gate-controlled signals of MPD1-MPD3, *VPC1*, *VPC2* and *VPC3*, are pulled to 0V one by one. In the meanwhile, the gate-controlled signals of MND1-MND3, *VNC1*, *VNC2* and *VNC3*, are pulled down to 0V to turn off transistors MND1-MND3 quickly. On the contrary, when 0-V output signal is transmitted to I/O PAD, the *VPC1*, *VPC2* and *VPC3* are quickly pulled up to VDD to turn off transistors MPD1-MPD3. The *VNC1*, *VNC2* and *VNC3* are progressively pulled up to VDD to turn on transistors MND1-MND3. As a result, the HCPMXIO-SR successfully transmits data with a reduced slew rate.

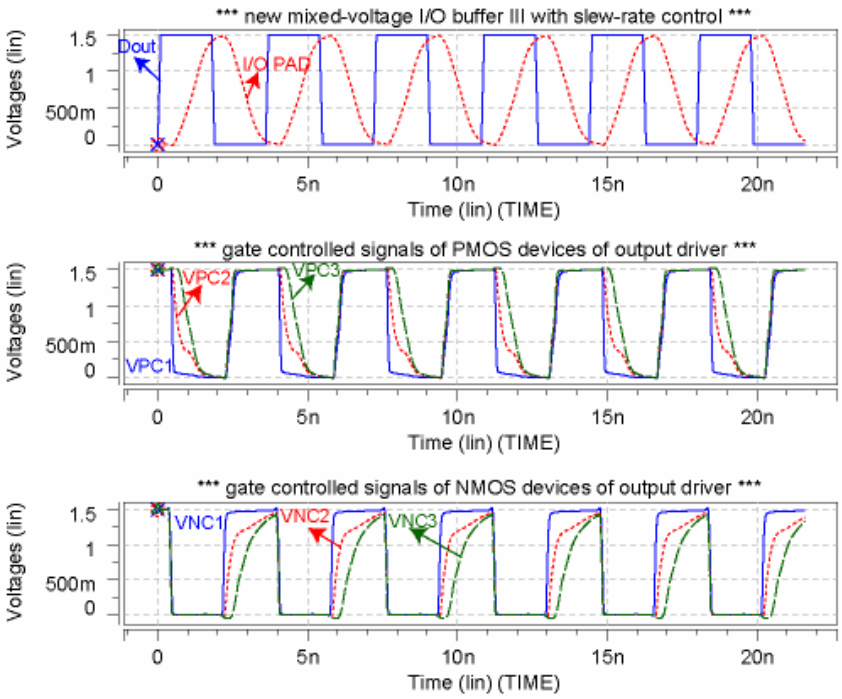


Fig. 4.13 Simulation waveforms of the HCPMXIO-SR operating at 266 MHz when transmitting 0V-to-1.5V output signals to I/O PAD.

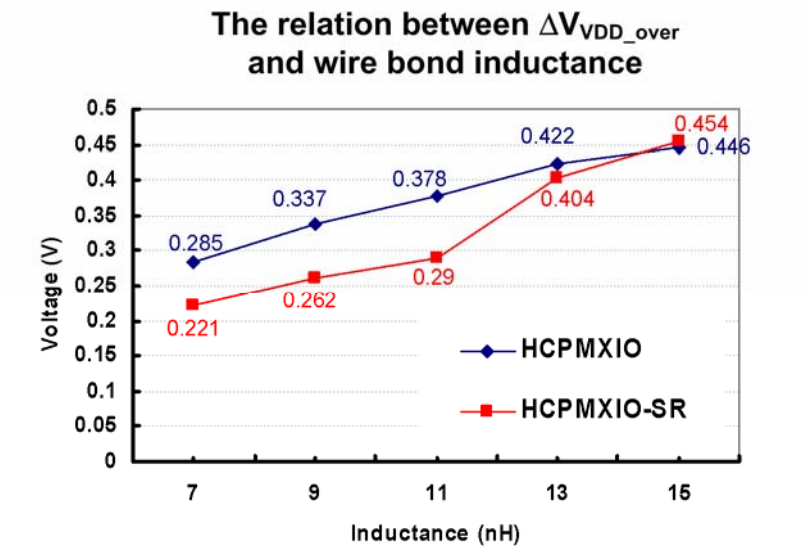
The simulation results of the HCPMXIO-SR and HCPMXIO, which has no slew-rate control, are summarized in Table 4.3. The propagation delay and rise/fall time of this HCPMXIO-SR are larger than those of the HCPMXIO. Also, the driving currents of HCPMXIO-SR are smaller than those of the HCPMXIO due to the

slew-rate control. The power consumption of this HCPMXIO-SR is larger than that of HCPMXIO due to the slew-rate controlled circuit, which is more complex than the slew-rate control circuit in the TBNMXIO-SR.

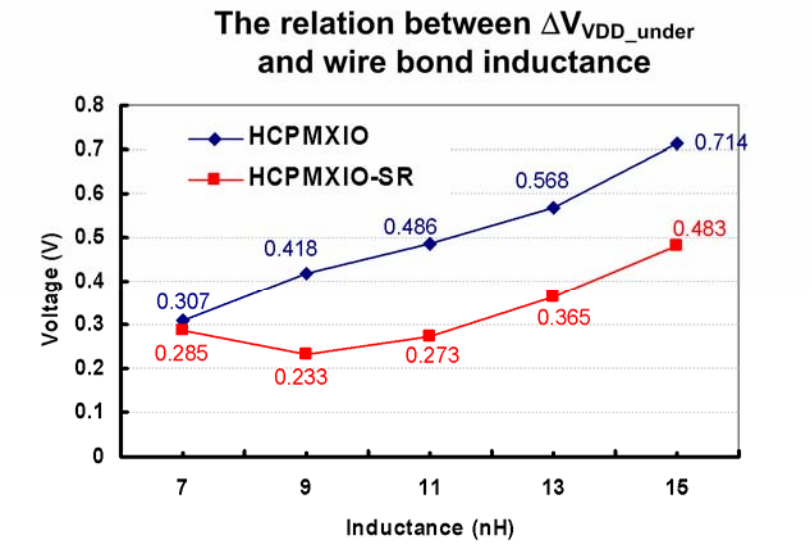
The ground bounce effects on GND and VDD power lines are shown in Fig. 4.14 and Fig. 4.15, respectively, which are the comparisons between the HCPMXIO and HCPMXIO-SR. As shown in Fig. 4.14 and Fig. 4.15, the ground bounce effects are reduced by the HCPMXIO-SR.

Table 4.3
The simulation results of the HCPMXIO and HCPMXIO-SR.

Parameters		HCPMXIO (Fig. 3.6)	HCPMXIO-SR (Fig. 4.12)
Slew-Rate Control		No	Yes
I_{OL} at V_{OL}=0.15 V		7.1 mA	6.7 mA
I_{OH} at V_{OH}=1.35 V		6.4 mA	6.2 mA
Receive Mode	T_{rise}	453 ps	454 ps
	T_{fall}	417 ps	420 ps
	T_{pr}	715 ps	702 ps
	Power Consumption	28 μW/MHz	29 μW/MHz
Transmit Mode	T_{rise}	702 ps	958 ps
	T_{fall}	708 ps	938 ps
	T_{pt}	815 ps	925 ps
	Power Consumption	59 μW/MHz	66 μW/MHz

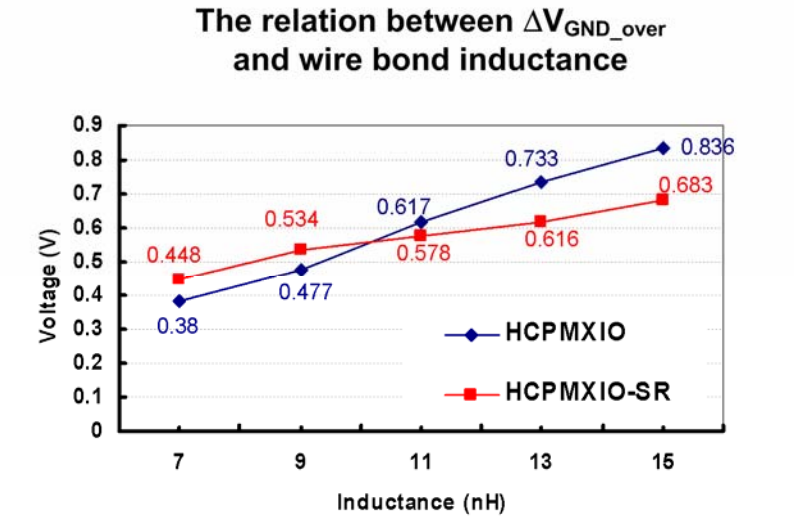


(a)

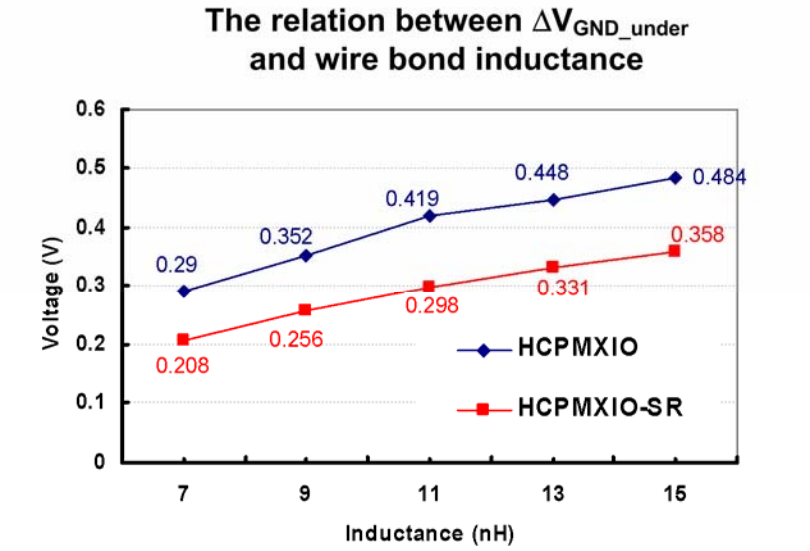


(b)

Fig. 4.14 The relation between ground bounce on VDD power line and wire bond inductance on the HCPMXIO and HCPMXIO-SR. (a) The overshoot and (b) the undershoot on VDD power line.



(a)



(b)

Fig. 4.15 The relation between ground bounce on GND power line and wire bond inductance on the HCPMXIO and HCPMXIO-SR. (a) The overshoot and (b) the undershoot on GND power line.

4.5 PRINCIPLES FOR FURTHER REDUCING GROUND BOUNCE

From the simulation results above, we have known that the circuit technique of

slew-rate control on mixed-voltage I/O buffers can greatly reduce the ground bounce effects. There are several extra techniques to further reduce ground bounce effects in this section.

4.5.1 Distributed Technique

The mechanism of slew-control in this thesis reduces the ground bounce by turning on output transistors one by one. The distributed number of parallel output transistors affects the operating speed of output buffer, and consequently the peak of switching current in transmitting data. The switching current and ground bounce get small with increasing distributed number of parallel output driver. In the meanwhile, however, the operating speed of mixed-voltage I/O buffer becomes slow and more gate-controlled signals of output transistors are required, which results in larger silicon area and power consumption in slew-rate controlled circuit. Therefore, an appropriate number of parallel output drivers should be applied in the mixed-voltage I/O buffer.

The ground bounce effects on TBNMXIO-SR with different number of parallel output drivers are verified by SPICE simulation in a 0.18-μm CMOS process. Also, the mixed-voltage I/O buffers are operating in transmit mode with 266-MHz operating speed. Some simulated parameters are list in Table 4.4 without adding wire bond model. The simulation results of ground bounce effects on both VDD and GND power lines are shown in Fig. 4.16 and Fig. 4.17. The ground bounce effects are further reduced with increasing parallel number of output drivers. As shown in Table 4.4, however, the propagation delay and rise/fall time is increased as the parallel number of output drivers is increased. The power consumption doest not increase with the increase of slew-rate controlled signals, since the driving capacity is reduced. It should be noted that the reduced percentage of ground bounce is decreased as the

parallel number of output drivers is increased. This is because the minimum switching currents of mixed-voltage I/O buffer are limited while the operating speed is maintained. Reduced percentage of the switching current by slew-rate control is consequently confined.

Table 4.4
Simulation results of the HCPMXIO-SR with different number of parallel output drivers in transmit mode.

Parameters		Parallel number		
		2	3	4
Output Transistor Size	MPDx	225μm/0.25μm	150μm/0.25μm	112.5μm/0.25μm
	MNDx	75μm /0.25μm	50μm /0.25μm	37.5μm /0.25μm
I_{OL} at V_{OL}=0.15 V		5.4 mA	5.0 mA	4.7 mA
I_{OH} at V_{OH}=1.35 V		5.9 mA	5.8 mA	5.6 mA
T_{rise}		721 ps	846 ps	960 ps
T_{fall}		683 ps	825 ps	941 ps
T_{pt}		823 ps	925 ps	1.028 ns
Power Consumption		69 μW/MHz	68 μW/MHz	68 μW/MHz

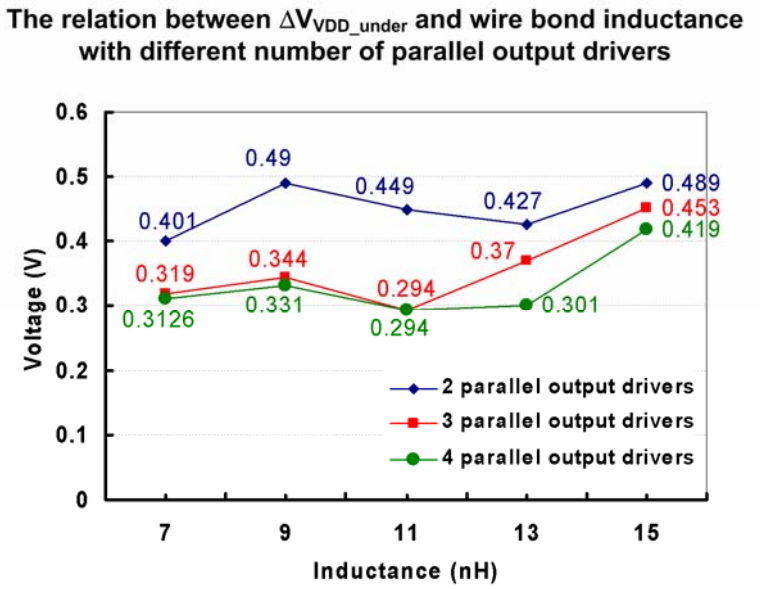


Fig. 4.16 The undershoot on VDD power line with different number of parallel output drivers.

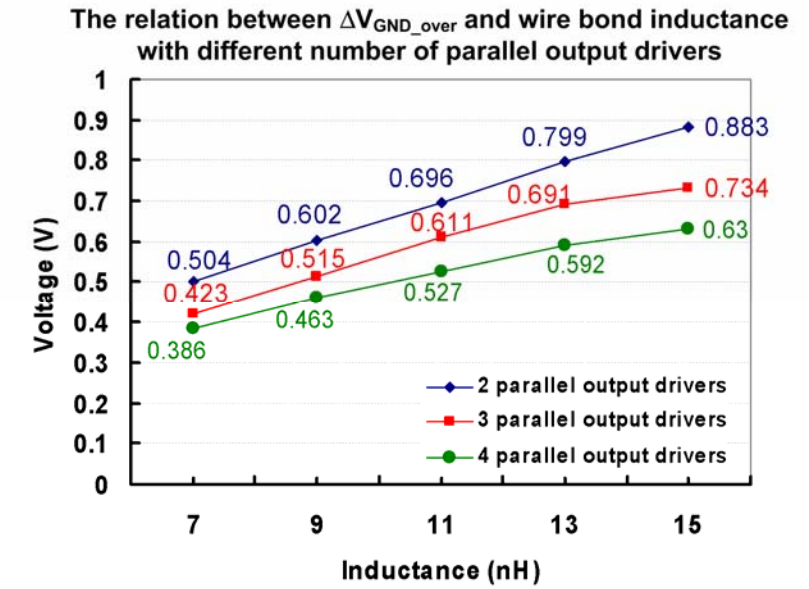


Fig. 4.17 The overshoot on GND power line with different number of parallel output drivers.

4.5.2 Weighted Technique

According to the eq. 4-1, the direct way to reduce ground bounce is to minimize the instantaneous current (di/dt) of the output transistors in mixed-voltage I/O buffer. Fig. 4.18 shows the current distributions of output transistors in the TBNMXIO-SR operated in transmit mode. In this case, the output driver is divided into three parts shown in Fig. 4.4, and the transistors MPD1-MPD3 in output driver are equal in device size. So are the transistors MND1-MND3. As shown in Fig. 4.18, the instantaneous currents of first branch of output drivers which are turned on first are largest. Therefore, smaller transistor size on the branch of output driver which is turned on first is recommended to reduce the instantaneous current. The transistors in the other branches of output driver which are turned on later are consequently larger in device size. The overall instantaneous currents are reduced, thus smaller ground bounce was resulted. To maintain the output impedance of mixed-voltage I/O buffer, the overall transistor sizes should be the same as the original transistor sizes.

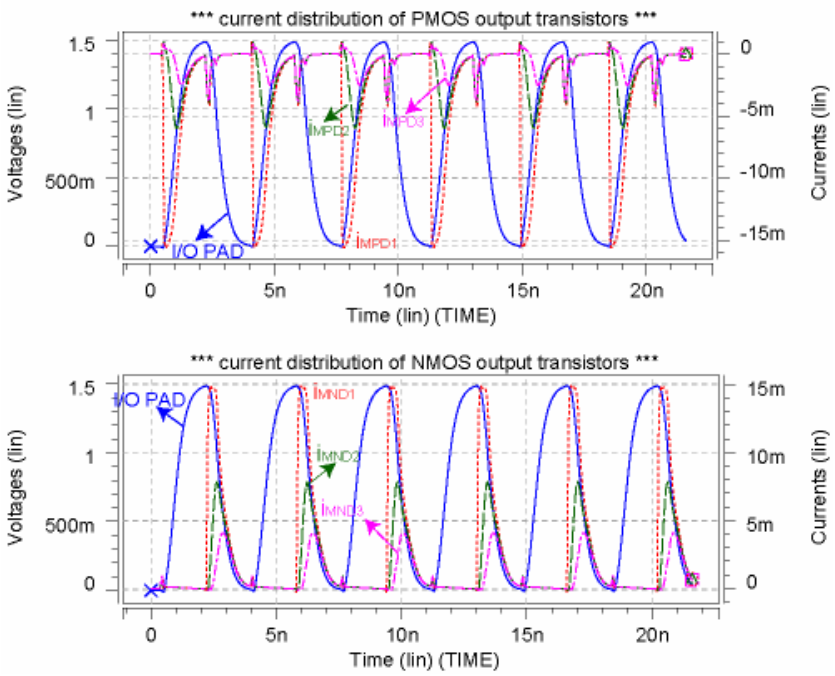


Fig. 4.18 Current distributions of output transistors in the TBNMXIO-SR operated in receive mode.

The TBNMXIO-SR is simulated with different transistor sizes of parallel output drivers, and the simulation results with the different transistor size are list in Table 4.5. The parameters I_{peak_MPD} and I_{peak_MND} are the maximum current peak among the transistors MPD1-MPD3 and MND1-MND3, respectively. As shown in Table 4.5, the version 2 and version 3 designs have about 50% and 40% reductions, respectively, on the current peak compared to the version 1 design (with equal output transistor in device size). Thus, increasing device size of output transistor gradually is preferred to reduce the ground bounce further. Finally, the simulation results of ground bounce with various wire bond inductance are shown in Fig. 4.19 and Fig. 4.20.

Table 4.5
Simulation results of the TBNMXIO-SR with different transistor sizes of output transistors in transmit mode.

Parameters	TBNMXIO-SR		
	Ver. 1	Ver. 2	Ver. 3
channel width (μm) MPD1/MPD2/MPD3	150/150/150	75/150/225	90/180/180
channel width (μm) MND1/MND2/MND3	50/50/50	25/50/75	30/60/60
I_{OL} at V_{OL}=0.15 V	5.0 mA	4.8 mA	4.9 mA
I_{OH} at V_{OH}=1.35 V	5.8 mA	5.7 mA	5.7 mA
T_{rise}	846 ps	960 ps	926 ps
T_{fall}	825 ps	903 ps	869 ps
T_{pt}	925 ps	1.088 ns	1.038 ns
I_{peak_MPD}	15.59 mA	8.06 mA (**48.3%** ↓)	9.61 mA (**38.3%** ↓)
I_{peak_MND}	14.92 mA	7.55 mA (**49.4%** ↓)	9.02 mA (**39.5%** ↓)

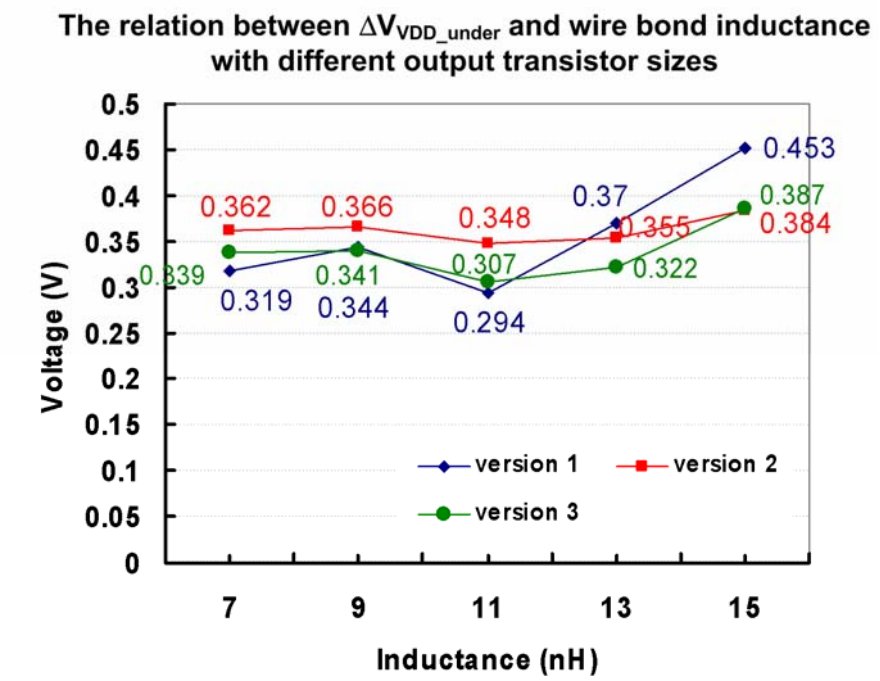


Fig. 4.19 The undershoot on VDD power line with different transistor sizes of output driver.

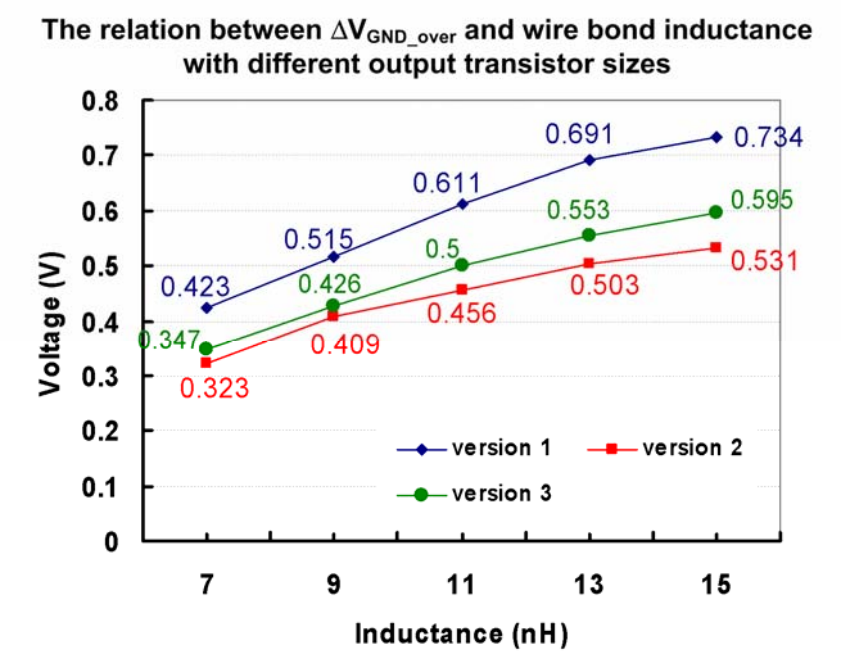


Fig. 4.20 The overshoot on GND power line with different transistor sizes of output driver.

4.5.3 Separate Power Pad

Often, the power pads of core circuit are separated from those of I/O circuit. The reduction of instantaneous currents on power lines are accompanied with separating power pads. Although the extra power pad results in larger cost, this method indeed reduces the ground bounce effects. The second model for ground bounce using two separate VDD pads is shown in Fig. 4.21. The simulated results of ground bounce are shown in Fig. 4.22 and Fig. 4.23 which compare simulation using the ground bounce model 2 with that using ground bounce model in Fig. 4.6. However, the ground bounce on VDD power line with two power pads is not reduced as we expect. This results from the cancellation between the instantaneous current on the pre-driver (i(VDD1)) and that on the I/O circuit (i(VDD2)) shown in Fig. 4.24. The major instantaneous current is induced by the I/O circuit, thus ground bounce would be mitigated greatly if another power pad is available in the I/O circuit.

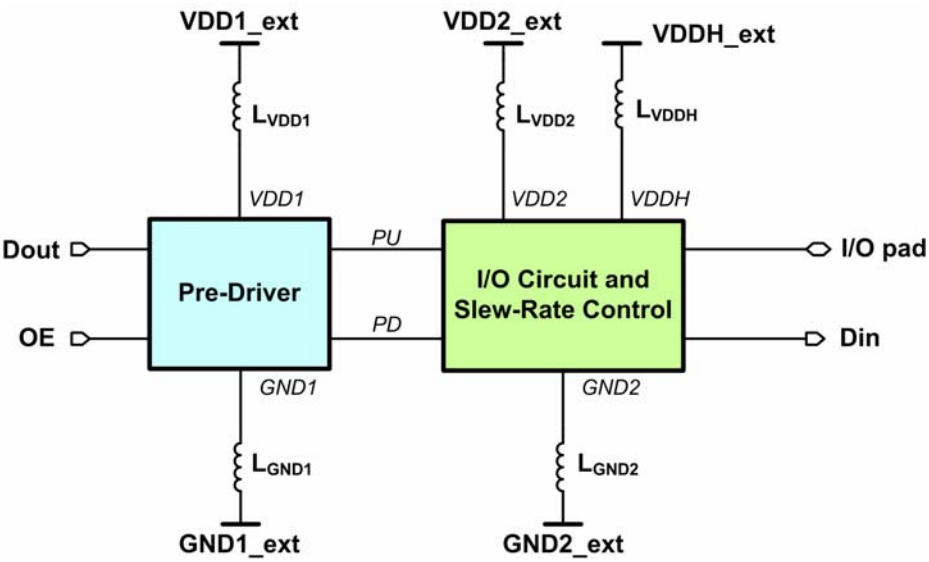


Fig. 4.21 The second simulation model of ground bounce using two separate VDD pads.

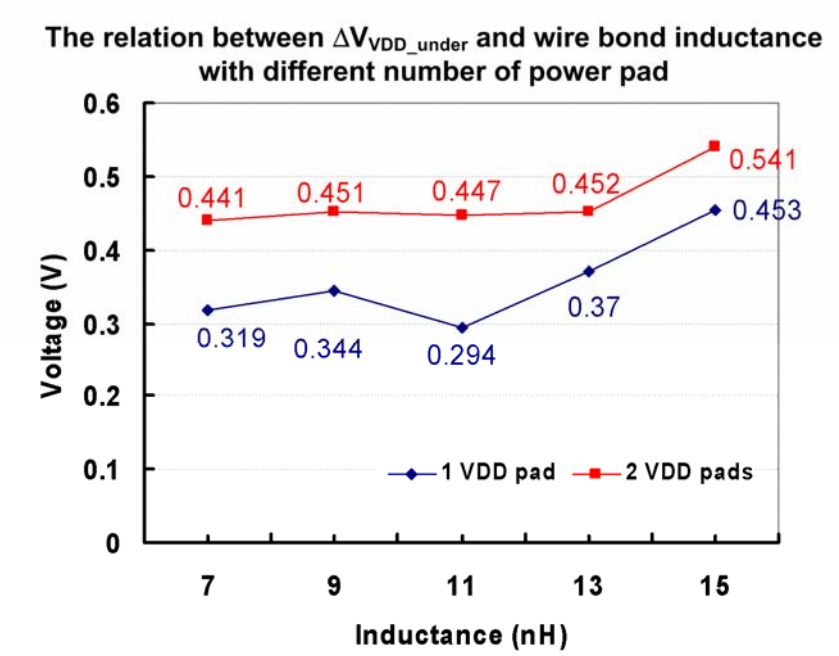


Fig. 4.22 The undershoot on VDD power line with different number of power pad.

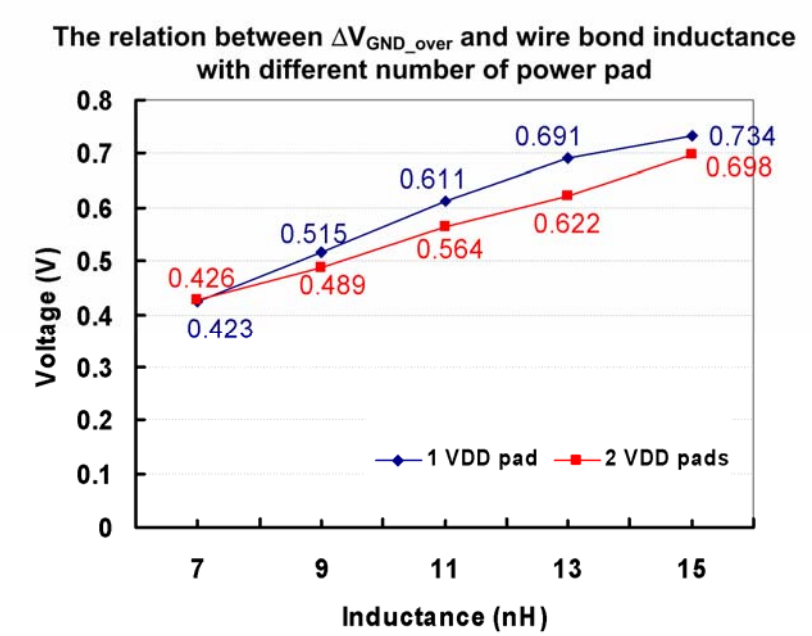


Fig. 4.23 The overshoot on GND power line with different number of power pad.

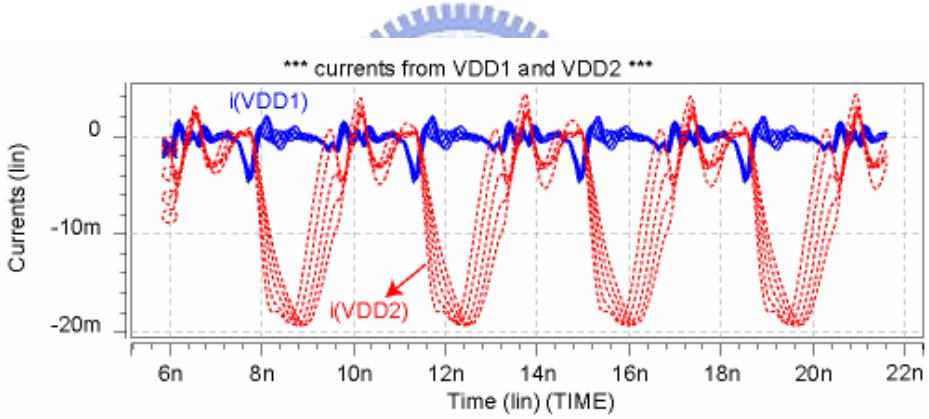


Fig. 4.24 Simulated currents from VDD1 and VDD2 power supply.

4.6 EXPERIMENTAL RESULTS

The TBNMXIO-SR shown in Fig. 4.4 has been fabricated in the 0.18-μm CMOS process with only thin-oxide devices. The photograph of fabricated circuit is shown in Fig. 4.25 with the corresponding pin names. Fig. 4.26 and Fig. 4.27 show the measured waveforms of TBNMXIO-SR in the receive mode to receive the 1-MHz and 266-MHz input signals with voltage swings of 0-to-1.5V and 0-to-3.3V, respectively,

at I/O PAD, where the input data can be successfully transmitted to Din with a voltage swing of 0-to-1.5V. The measured waveforms of the TBNMXIO-SR in the transmit mode to transmit 1-MHz and 266-MHz signals with a voltage swing of 0-to-1.5V from Dout to I/O PAD are shown in Fig. 4.28, where the signals at Dout can be successfully transmitted to the I/O PAD with the same voltage swing. The measured parameters and layout area of the TBNMXIO and TBNMXIO-SR are list in Table 4.6.

To observe the ground bounce effects, the power pads of TBNMXIO-SR are connected to external power supply through inductors shown in Fig. 4.29. The external inductance is 100 nH. The measured results of the TBNMXIO and TBNMXIO-SR are shown in Fig. 4.30 and Fig. 4.31, respectively. Both the ground bounce effects in these two designs are such small that the advantage of slew-rate control is indistinct. Most of power noises on VDD pads are resulted from the external environment. Actually, a test circuit for measuring ground bounce should be developed.

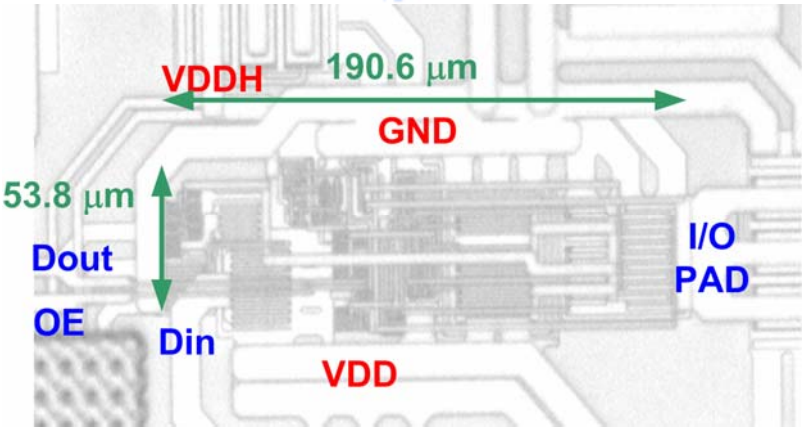
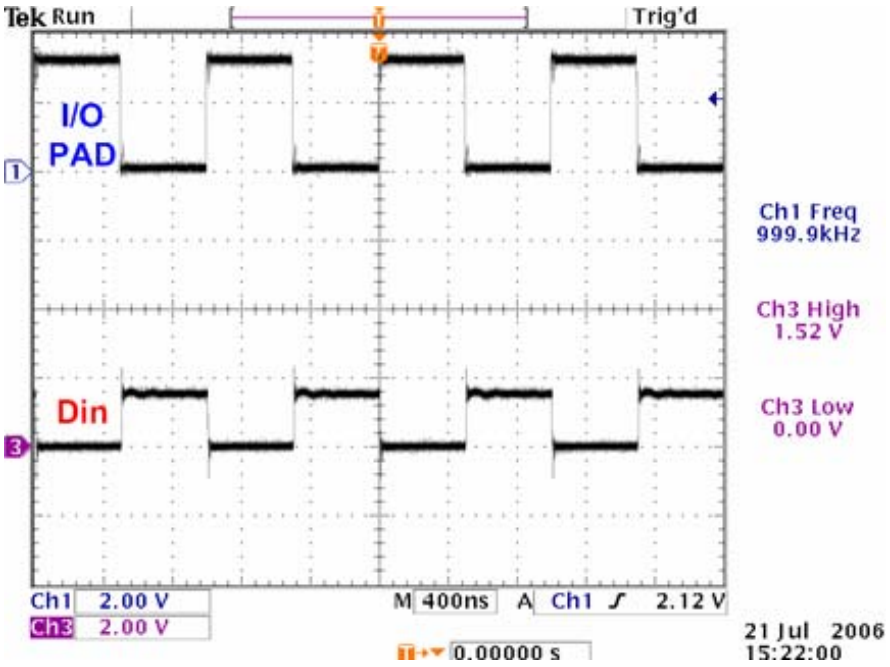
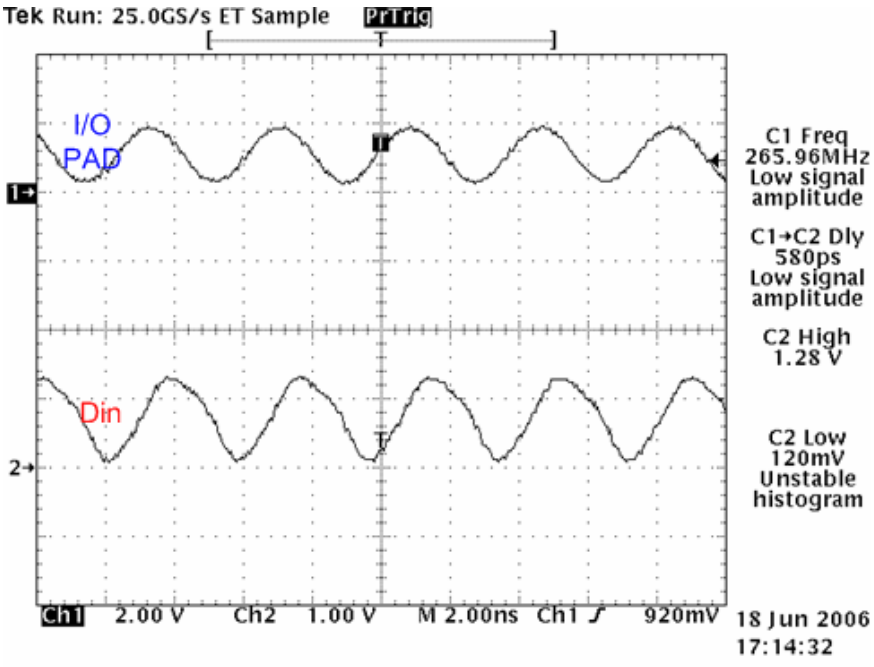


Fig. 4.25 The photograph of the TBNMXIO-SR in a 0.18-μm 1.8-V CMOS process.

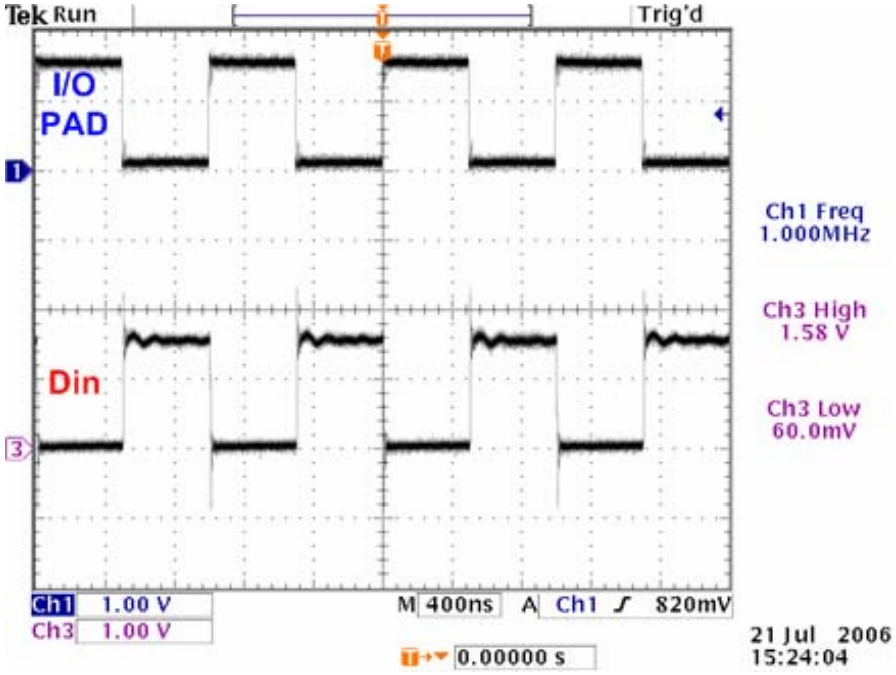


(a)

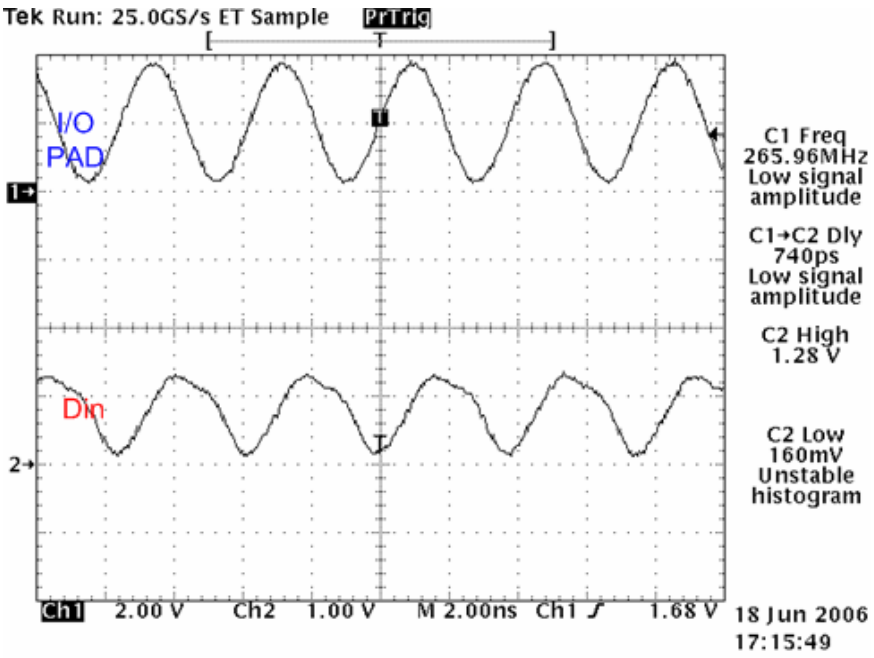


(b)

Fig. 4.26 Measured waveforms of the TBNMXIO-SR operating at (a) 266 MHz and (b) 1 MHz when receiving 0V-to-1.5V input signals at I/O PAD.

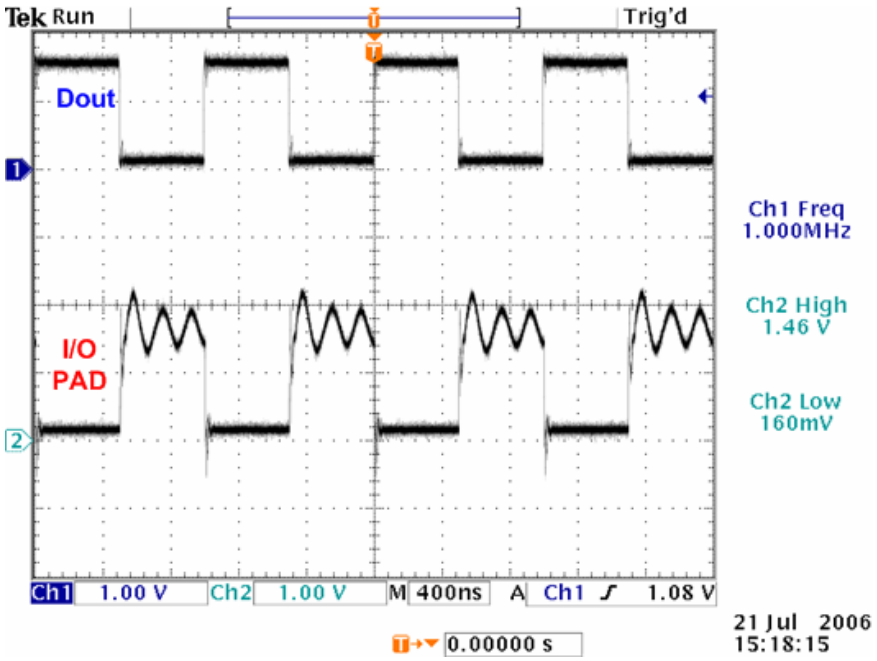


(a)

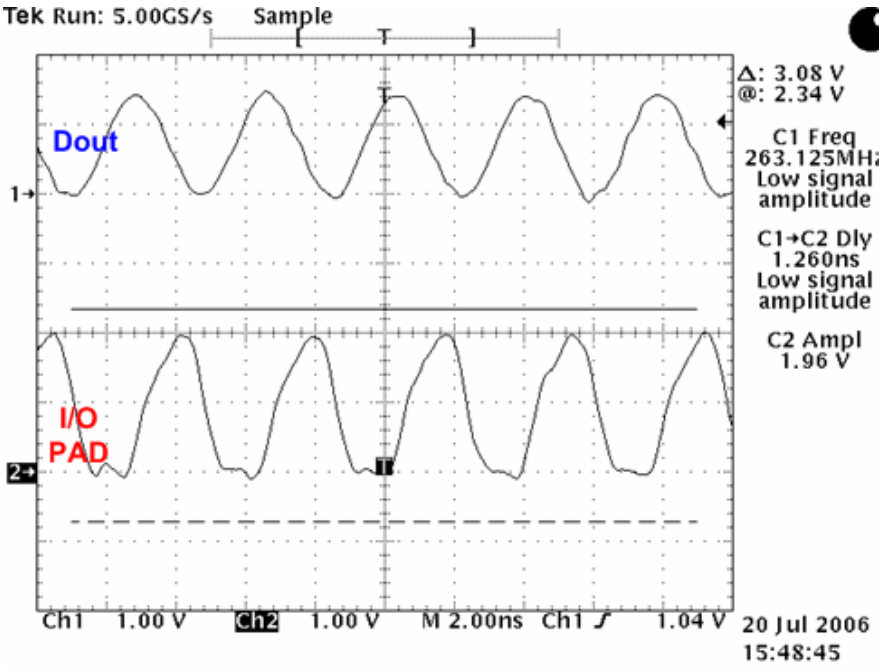


(b)

Fig. 4.27 Measured waveforms of the TBNMXIO-SR operating at (a) 266 MHz and (b) 1 MHz when receiving 0V-to-3.3V input signals at I/O PAD.



(a)



(b)

Fig. 4.28 Measured waveforms of the TBNMXIO-SR operating at 266 MHz when transmitting 0V-to-1.5V output signals to I/O PAD.

Table 4.6
The measured parameters of the TBNMXIO and TBNMXIO-SR.

Parameters		TBNMXIO (Fig. 3.13)	TBNMXIO-SR (Fig. 4.4)
Layout Area		169.2 μm × 53.8 μm	190.6 μm × 53.8 μm
Receive Mode	T_{pr}	663 ps	740 ps
	Power Consumption	30 μW/MHz	22 μW/MHz
Transmit Mode	T_{pt}	2.75 ns	2.89 ns
	Power Consumption	121 μW/MHz	121 μW/MHz

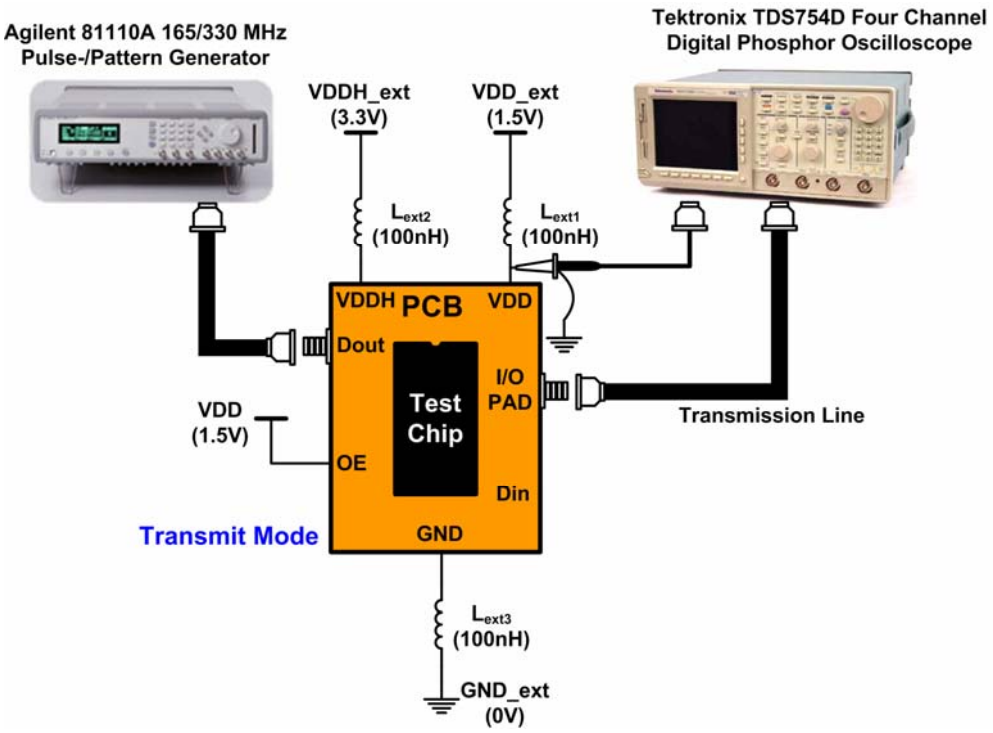


Fig. 4.29 The setup for ground bounce measurement.

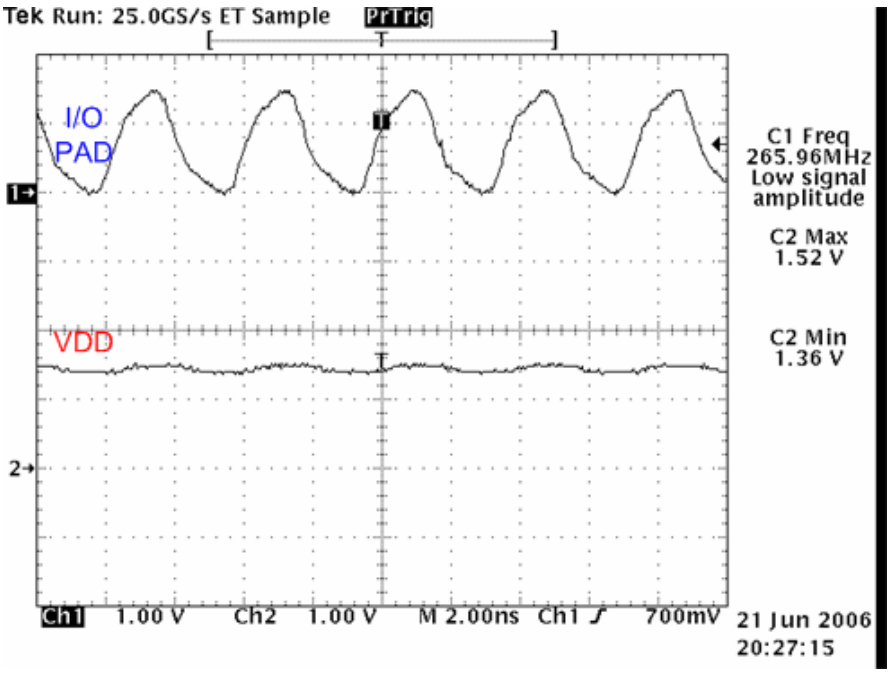


Fig. 4.30 Measured ground bounce on VDD pad of TBNMXIO (without slew-rate control).

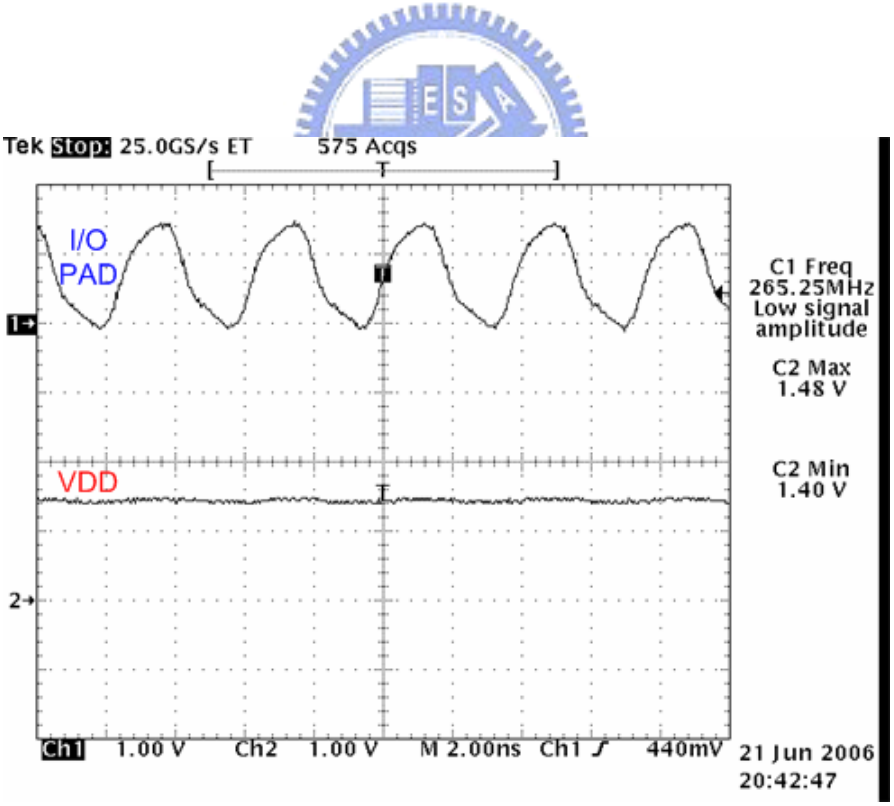


Fig. 4.31 Measured ground bounce on VDD pad of TBNMXIO-SR (with slew-rate control).

4.7 DISCUSSION AND SUMMARY

4.7.1 Discussion

In this chapter, the measured ground bounce effects are not reduced greatly by the slew-rate control. For experimental measurement of ground bounce effect, seven or eight I/O buffers must be switched on simultaneously resulting in large instantaneous current [29]. Fig. 4.32 shows the connecting diagram for measuring ground bounce. Moreover, a test circuit for measuring ground bounce should be developed.

In this thesis, tapper buffers were used to drive Din pads in this thesis as the mixed-voltage I/O buffers are operated in receive mode. As a result, the switching current may be dominated by the tapper buffer such that the difference of switching currents induced by output transistors between the mixed-voltage I/O buffer with slew-rate control and that without slew-rate control is indistinct. A better method to measure the receiving operation is shown in Fig. 4.33 where one I/O cell is connected as in receive mode and the other is connected as in transmit mode. Therefore, the silicon area and power consumption of one mixed-voltage I/O buffer will be reduced. The ground bounce effect will not be affected by the tapper buffer, too. There is another way to eliminate the effect of tapper buffer on ground bounce. That is adding an enable pin (IE) to input buffer. As the mixed-voltage I/O buffer is operated in transmit mode, the IE is set to 0V to disable input circuit. Therefore, the tapper buffer can drive Din pad successfully without affecting ground bounce in transmit mode at a cost of extra pad and silicon area.

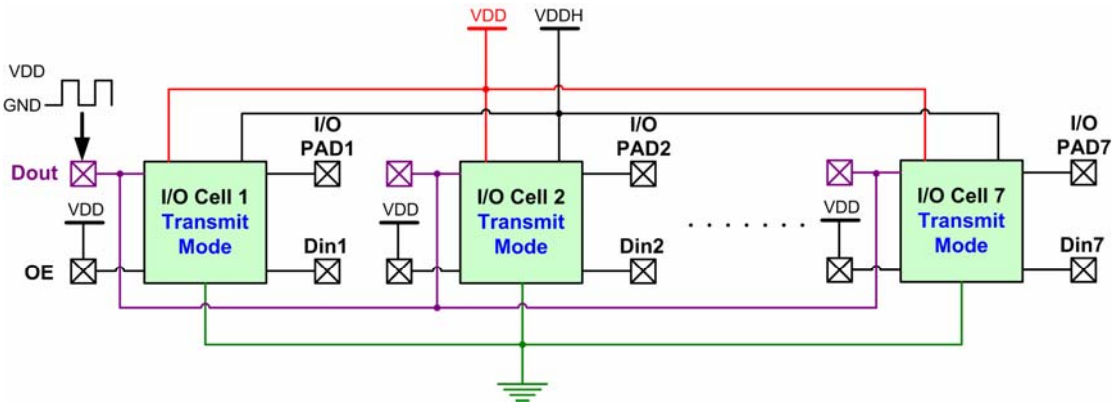


Fig. 4.32 The measurement method of ground bounce effect where seven I/O cells switch simultaneously.

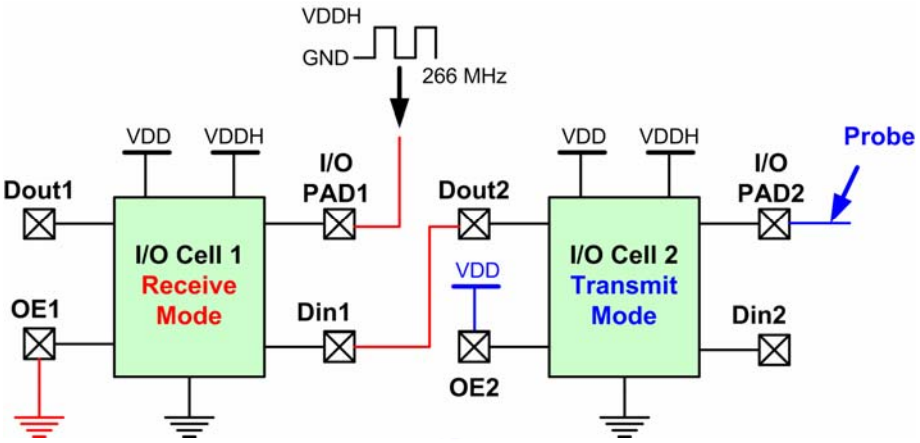


Fig. 4.33 The measurement setting for testing the receiving operations of mixed-voltage I/O buffer.

4.7.2 Summary

In this chapter, two new mixed-voltage I/O buffers with slew-rate control have been proposed with only thin-oxide devices. The reduction on ground bounce effects by slew-rate control has been verified in a 0.18-μm CMOS process. The TBNMXIO-SR has been fabricated in a 0.18-μm CMOS process. Several circuit techniques for further reducing ground bounce are summarized in this chapter.

Chapter 5

Conclusion and Future Works

5.1 CONCLUSION

A hot-carrier-prevented circuit with only-thin oxide devices which can successfully solve the hot-carrier degradation during the transitions was proposed in chapter 3. This circuit can be applied in the general 2xVDD-tolerant I/O buffer to solve hot-carrier degradation on devices without reducing the driving capacity. The whole mixed-voltage I/O buffer with hot-carrier-prevented circuits was designed in chapter 3 without suffering hot-carrier degradation in both steady states of receive mod and transmit mode and the transitions. Furthermore, a new 2xVDD-tolerant I/O buffer with two blocking NMOS devices and dynamic gate-controlled circuit was proposed without hot-carrier degradation in both steady states of receive mode and transmit mode and the transition from receiving 2xVDD input signal to transmitting 0-V output signal. Although the stacked number of output transistors in mixed-voltage I/O buffer was increased, the overall circuit design is less complex than the mixed-voltage I/O buffers with floating n-well bias circuit. Both proposed designs have been fabricated in a 0.18-μm 1P6M CMOS process and are suitable for the PCI-X 2.0 applications.

In chapter 4, two mixed-voltage I/O buffers based on the prior designs in chapter 3 with slew rate control were proposed. The slew-rate controls on mixed-voltage I/O buffers can effectively reduce the ground bounce effects without gate-oxide reliability problems and hot-carrier degradation issues. Several technique including distributed and weighted technique and separate power pad were discussed to further reduce

ground bounce. The mixed-voltage I/O buffer using two blocking NMOS devices and dynamic gate-controlled circuit with slew-rate control has been fabricated in a 0.18-μm 1P6M CMOS process.

5.2 FUTRUE WORKS

Since the proposed mixed-voltage I/O buffers in this thesis are designed with an operating speed of up to 266 MHz, the transmission line effect should be considered. Thus transmission model should be added into simulation to have more accurate results. Besides, the circuit techniques for reducing short circuit current can be applied in the designs to further reduce the power consumption induced by short current. Also, the slew-rate control in mixed-voltage I/O buffer should be carefully designed without hot-carrier degradation during the transitions from receiving high input signal to transmitting low output signal. Finally, the measured methods for verifying the operations of mixed-voltage I/O buffer which have been mentioned in 4.7 should be used to have clear verifications.

REFERENCES

[1] T. Furukawa, D. Turner, S. Mittl, M. Maloney, R. Serafin, W. Clark, L. Longenbach, and J. Howard, "Accelerated gate-oxide breakdown in mixed-voltage I/O buffers," in *Proc. IEEE Int. Reliability Physics Symp.*, 1997, pp. 169−173.

[2] I.-C. Chen, J. Y. Choi, and C. Hu, "The effect of channel hot-carrier stressing on gate-oxide integrity in MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, pp. 2253−2258, Dec. 1988.

[3] S. Voldman, "ESD protection in a mixed voltage interface and multrial disconnected power grid environment in 0.5- and 0.25-μm channel length CMOS technologies," in *Proc. EOS/ESD Symp.*, 1994, pp. 125−134.

[4] M.-S. Liang, C. Chang. W. Yang, C. Hu and R. W Brodersen, "Hot-carriers induced degradation in thin gate oxide MOSFETs," in *International Electron Devices Meeting (IEDM) Tech. Digest*, 1983, pp. 186.

[5] S. Poon, C. Atwell, C. Hart, D. Kolar, C. Lage, and B. Yeargain, "A versatile 0.25 micron CMOS technology," in *IEDM. Tech. Dig.*, 1998, pp. 751−754.

[6] M. Hargrove, S. Crowder, E. Nowak, R. Logan, L. K. Han, H. Ng, A. Ray, D. Sinitsky, P. Smeys, F. Guarin, J. Oberschmidt, E. Crabbé, D. Yee, and L. Su, "High-performance sub-0.08 μm CMOS with dual gate oxide and 9.7 ps inverter delay," in *IEDM. Tech. Dig.*, 1998, pp. 627−630.

[7] M. Takahashi, T. Sakurai, K. Sawada, K. Nogami, M. Ichida, and K. Matsuda, "3.3V-5V compatible I/O circuit without thick gate oxide," in *Proc. Of IEEE Custom Integrated Circuits Conference*, 1992, pp. 23.3.1-23.3.4.

[8] M. J. M. Pelgrom and E. C. Dijkmans, "A 3/5-V compatible buffer", *IEEE J. Solid-State Circuits*, vol.30, pp. 823-825, July 1995.

[9] C.-H. Chuang and M.-D. Ker, "Design on mixed-voltage-tolerant I/O interface with novel tracking circuits in a 0.13-μm CMOS technology." *IEEE Int. Symp. on Circuits and Systems*, 2004, vol. 2, pp .577-580.

[10] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of mixed-voltage I/O buffer with gate-tracking circuit and dynamic n-well bias circuit," *IEEE Trans. On Circuits and Systems I: Regular Paper,* in press, 2006.

[11] D. A. Neamen, *Semiconductor Physics and Devices – Basic Principles*, 3rd ed., New York: McGraw-Hill, 2003.

[12] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, New York: Cambridge University Press, 1998.

[13] J. Tanaka, S. Kimura, H. Noda, T. Toyabe, and S. Ihara, "A sub-0.1-μm grooved gate MOSFET with high immunity to short-channel effect," in *IEDM. Tech. Dig.*, 1993, pp. 537-540.

[14] A.-J. Annema, G. J. G. M. Geelen, and P. C. de Jong, "5.5-V I/O in a 2.5-V 0.25-μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 528-538, March 2001.

[15] P. Woerlee, P. Damink, M. van Dort, C. Juffermans, C. de Kort, H. Lifka, W. Manders, G. Paulsen, H. Pomp, J. Slotboom, G. Streutker, and R. Woltjer, "The impact of scaling on hot-carrier degradation and supply voltage of deep-submicron NMOS transistors," in *IEDM. Tech. Dig.*, 1991, pp. 537−540.

[16] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits – A Design Perspectiv*e, 2nd ed., Prentice Hall, 2003.

[17] J. Brewer and J. Sekel (2004, Jun.). White paper: PCI Express Technology. Dell Inc., US. [Online]. Available: http://www.dell.com/content/topics/global.aspx /vectors/en/2004_pciexpress?c=us&l=en&s=corp

[18] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design on mixed-voltage I/O circuit with blocking NMOS and dynamic gate-controlled circuit for high-voltage-tolerant applications," *IEEE Int. Symp. on Circuits and Systems*, 2005, pp. 1859-1862.

[19] S. Dabral and T. Maloney, *Basic ESD and I/O Design*, John Wiley & Sons, 1998.

[20] H.-C. Chow, "Bidirectional buffer for mixed-voltage applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 1999, vol. 1, pp. 270−273.

[21] R. D. Adams, R. C. Flaker, K. S. Gray, and H. L. Kalter, "CMOS off-chip driver circuit," U.S. Patent 4782250, Nov. 1, 1988.

[22] D.-Y. Chen, "Design of a mixed 3.3 V and 5 V PCI I/O buffer," in *Proc. IEEE Int. ASIC Conf.*, 1996, pp. 336−339.

[23] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS processes," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1100-1107, May 2006.

[24] M.-D. Ker, C.-Y. Chang, and H.-C. Jiang, "Design of negative charge pump circuit with polysilicon diodes in a 0.25-μm CMOS process," in *Proc. IEEE Asia-Pacific Conf. Advanced System Integrated Circuits*, 2002, pp. 145−148.

[25] A. J. Annema, Govert J. G. M. Geelen, "High-voltage level tolerant transistor circuit," New York, U.S. Patent 6320414B1, Nov. 20, 2001.

[26] M.-D. Ker, S.-L. Chen, and C.-S. Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS processes," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1100-1107, May 2006.

[27] F. Garcia, P. Coll, and D. Auvergne, "Design of a Slew Rate Controlled Output Buffer," in *Proc. IEEE Int. ASIC Conf.*, 1998, pp. 147−150.

[28] M. S. Haydt, R. Owens, and S. Mourad, "Modeling the Effect of Ground Bounce on Noise Margin," in *Proc. IEEE International Test Conf.*, Oct. 1994, pp. 279-285.

[29] B. Deutschmann and T. Ostermann, "CMOS output drivers with reduced ground bounce and electromagnetic emission," in *Proc. of European Solid-State Circuits Conf.*, Sep. 2003, pp. 537-540.

簡歷

姓　　名：胡芳綾

學　　歷：

台灣省立蘭陽女子高級中學　　(86年9月~89年6月)

國立交通大學電機與控制工程學系　　(89年9月~93年6月)

國立交通大學電子研究所碩士班　　(93年6月~95年6月)

研究所修習課程：

類比積體電路 I	吳介琮教授
類比積體電路 II	吳介琮教授
數位積體電路	柯明道教授
有線傳輸通訊積體電路設計	陳巍仁教授
低功率與高速積體電路設計	周世傑教授
積體電路之靜電放電防護設計特論	柯明道教授
計算機結構	黃俊達教授
顯示電子電路	戴亞翔教授

永久地址：宜蘭縣礁溪鄉礁溪路六段 128 號

Email： fangling.ee93g@nctu.edu.tw

fangling.ece89@nctu.edu.tw

m9311593@alab.ee.nctu.edu.tw