Chapter 1

Introduction

1.1 Motivation

The charge pump circuit is usually used to generate voltages higher than the available supply voltage. It is applied widely in EEPROM or flash memories to program the floating-gate device. In the I/O interface, it also needs a charge pump circuit to generate a higher voltage than the nominal supply voltage.

In many applications such as EEPROMs and switched capacitor transformers, charge pumps are frequently used to provide a voltage higher than a power supply because high voltage level in a charge pump is generated by transferring charges to a capacitive load without any amplifiers or regular transformers. The conventional applications have required a high voltage with only limited current drivability. Many approaches to the charge pump have focused on the design of Dickson charge pump.

However recent applications like USB OTG (On-The-Go), require not only the high voltage level but also high current drivability. The internal charge pump circuit of the dual-role transceiver supplies VBUS power and signaling that is required by the transceiver.

1.2 Organization

This thesis is organized into seven chapters and this introduction is the first one.

Chapter 2 introduces design background for charge pump circuit used in USB on-the-go (OTG) dual-role transceiver. Chapter 3 introduces the design and the history of prior art. Chapter 4 presents the two new ideas of charge pump circuit dealing with gate-oxide reliability issue in low voltage processes and introduces three unsuitable implementation. In chapter 5, the charge pump circuit, the single-ended coupled ring oscillator and the source-coupled differential-pair comparator integrate the new charge pump circuit with the feedback loop. In chapter 6, the simulation waveforms and the measurement results are shown. Finally, in chapter 7, we summarize this work and discuss the further development.

Chapter 2

Background

2.1 Introduction of USB OTG

USB (Universal Serial Bus) allows a portable device to take on the role of a limited USB host, without the burden of supporting all the above functions of a PC. USB communication can only take place between a host and a peripheral. The software running on a device can control the behavior or actions of the USB port(s) on a device. The USB OTG (on-the-go) dual-role device can facilitates the direct connection of peripherals and mobile devices such as PDAs, cellular phones, MP3 players, and digital cameras to one another without a host PC.

Now, in the USB communication, we can use two kinds of devices and differentiate them as fallow. A device with a Standard-A or Mini-A plug inserted into its receptacle is A-device. An A-device supplies power to VBUS and is host at the start of a session. If the device is dual-role, it may be granted the role of peripheral from the B-device. A device with a Standard-B or Mini-B plug inserted into its receptacle is B-device. The B-device is a peripheral at the start of a session. If the device is dual-role, it may be granted the role of host from the A-device.

2.2 Operation of USB OTG Device

This chapter lists and defines terms and abbreviations used throughout the

On-the-Go Supplement to the USB 2.0 Specification, Revision 1.0 [1]. The operation of USB OTG is simply divided into four parts below.

A. Identification

Identification (ID) denotes the pin on the Mini connectors that is used to differentiate a Mini-A plug (ID pin resistance to ground < 10Ω) from a Mini-B plug (ID pin resistance to ground greater than 100 kΩ).

B. Targeted Peripheral List

When acting as Host, a dual-role device is not required to support operation with all other types of USB peripherals. It is up to the manufacturer of each dual-role device to determine what peripherals the dual-role device will support and provide a list of those peripherals. The peripheral would need to exhibit the electrical and software characteristics defined for that OTG peripheral type. We can know that the Targeted Peripheral List is simply a list of peripherals; a manufacturer, the kind of the device and a model number, identifies each peripheral.

C. Session Request Protocol

Session is the period of time that VBUS is above a device's session valid threshold. The OTG supplement defines a Session Request Protocol (SRP), which allows a B-device to request the A-device to turn on VBUS and start a session. In order to conserve power, the protocol allows an A-device, which may be battery powered, to leave VBUS turned off when the bus is not being used while still providing a means for the B-device to initiate bus activity. Any A-device, including a PC or laptop, is allowed to respond to SRP. Any B-device, including a standard USB peripheral, is allowed to initiate SRP. A dual-role device is required to be able to initiate and respond to SRP.

If the B-device wants to use the bus when VBUS is turned off, then it requires some way of requesting the A-device to supply power on VBUS. The OTG

supplement defines two methods that are used by the B-device to request that the A-device begin a session. They are called “data-line pulsing” and “VBUS pulsing”. These two methods comprise the Session Request Protocol (SRP). The B-device shall first perform data-line pulsing, followed by VBUS pulsing. An A-device is only required to respond to one of the two SRP signaling methods. A B-device shall use both methods when initiating SRP to insure that the A-device responds. After initiating SRP, the B-device is required to wait at least 5 seconds for the A-device to respond, before informing the user that the communication attempt has failed. For this reason, it is recommended that the A-device respond to SRP in less than 5 seconds.

The B-device may not attempt to start a new session until it has determined that the A-device should have detected the end of the previous session. The A-device detects the end of a session by sensing that VBUS has dropped below its session valid threshold. Since the A-device Session Valid threshold may be as low as VA_SESS_VLD min, the B-device must insure that VBUS is below this level before requesting a new session. The B-device may ensure that VBUS is below the B-device Session End threshold either by direct measurement of VBUS or by timing the discharge. The B-device may initiate the SRP any time the initial conditions discussed above are met.

D. Host Negotiation Protocol

The Host Negotiation Protocol (HNP) allows the Host function to be transferred between two directly connected dual-role devices and eliminates the need for a user to swap the cable connection in order to change the roles of the connected devices. Since dual-role devices have a Mini-AB receptacle, a dual-role device can default to being either Host or Peripheral, depending up which type of plug (Mini-A plug for Host, Mini-B plug for Peripheral) is inserted. By utilizing the Host Negotiation Protocol (HNP), a dual-role B-device, which is the default Peripheral, may make a request to

be Host.

HNP is used to transfer control of a connection from the default Host (A-device) to the default Peripheral (B-device). After the A-device sends a command, the A-device may suspend the bus to signal the B-device that it may now take control of the bus. If the B-device wants to use the bus at that time, it signals a disconnect command to the A-device. If the A-device has enabled the B-device to become Host, then the A-device will interpret this disconnect during suspend as a request from the B-device to become Host. When the B-device has finished using the bus, it starts the process of returning control to the A-device simply by stopping all bus activity. When the A-device detects the connection from the B-device, it will resume bus operation as Host.

2.3 USB OTG Dual-Role Transceiver

An USB on-the-go (OTG) dual-role transceiver as defined in On-the-Go Supplement to the USB 2.0 Specification, Revision 1.0 [1] is shown in Fig. 2.1. A charge pump circuit, comparators, level shifters and a current source integrate this dual-role transceiver.

In the USB communication, we have known that two kinds of devices A and B used to be host and peripheral respectively. The dual-role device can play the role of either A-device or B-device by ID_IN detection. Configure this dual-role transceiver as device A by connecting ID_IN to GND and as device B by leaving ID_IN open (Table 2.2). ID_IN is internally pulled up to VCC. ID_IN is level translated to V_L (V_L< VCC) and provided as an output at ID_OUT, where V_L sets the logic output high level ensuring compatibility with low voltage ASICs.

According to the statement in the chapter 2.2, the output voltage value of VBUS is used during negotiation for the USB according to the Session Request Protocol (SRP) and Host Negotiation Protocol (HNP). The USB on-the-go (OTG) dual-role transceiver shown in Fig. 2.1 provides power for the VBUS line using an internal charge pump circuit. A dual-role device must be able to source a minimum of 8mA on VBUS when it is the A-device and a session is in progress. The charge pump circuit provides an OTG-compliant output on VBUS while sourcing 8mA load current. VBUS provides a nominal +5.0V output when ID_IN is low and $\overline{\text{OFFVBUS}}$ is high. The charge pump circuit is active if $\overline{\text{OFFVBUS}}$ is connected to VL and the USB OTG dual-role transceiver is configured as device A (ID_IN connected to GND).

It also provides internal comparators for monitoring the output voltage value of VBUS in the USB OTG dual-role transceiver. There are two status outputs of VBUS: STATUS1 and STATUS2. The status outputs can be used to negotiate for the USB OTG bus according to the session request protocol (SRP) and host negotiation protocol (HNP). The two VBUS status outputs are conveyed for the two protocols according to Table 2.3(a).

We can see that it has three threshold voltages in Table 2.3(a). When an A-device is providing power to VBUS on a port, it is required to maintain an output voltage value of VBUS ($V_{TH,BUSVLD}$) between 4.4 V and 5.25 V, under loads of 0mA up to the rated per port output of the device's supply. It must be able to detect when VBUS falls below the value ($V_{TH,BUSVLD}$) necessary for proper operation of a B-device. Any voltage below $V_{TH,BUSVLD}$ shall be detected as a low-voltage condition.

The B-device may not attempt to start a new session until it has determined that the A-device should have detected the end of the previous session. The A-device continuously monitors the output voltage value of VBUS as long as power is available on the A-device. The A-device detects the end of a session by sensing that VBUS has

dropped below its session valid threshold ($V_{TH,SESVLD,A}$). Since the A-device Session Valid threshold may be as low as $V_{TH,SESVLD,A}$ min, the B-device must insure that VBUS is below this level before requesting a new session. The B-device may ensure that VBUS is below the B-device session end threshold ($V_{TH,SESEND}$) either by direct measurement of VBUS or by timing the discharge.

In addition, an A-device that is designed to detect the VBUS pulsing method will detect that VBUS has gone above the A-device session valid threshold ($V_{TH,SESVLD,A}$) and generate an indication that SRP has been detected. If a B-device detects that the voltage on VBUS is greater than the B-Device session valid threshold ($V_{TH,SESVLD,B}$), then the B-device shall consider a session to be in progress.

Connect $\overline{SHDN}$ to VL for normal operation. To enter shutdown mode, connect $\overline{SHDN}$ to GND. The shutdown mode of USB OTG dual-role transceiver reduces supply current less than 1μA. As shown in Table 2.4, shutdown mode disables the charge pump and comparators. While in shutdown mode, the STATUS2 output can be used to indicate VBUS voltage as shown in Table 2.3(b) and the STATUS1 output defaults to logic 0. During shutdown, if VBUS is externally driven above $V_{TH,\overline{SHDN}}$, the USB OTG dual-role transceiver sinks current from VCC.

As shown in Table 2.4, $\overline{OFFVBUS}$ can be used to turn the internal charge pump providing VBUS on and off. For normal VBUS operation, connect $\overline{OFFVBUS}$ to VL. On the contrary, connect $\overline{OFFVBUS}$ to GND to disable VBUS and the charge pump circuit. The current generator is connected to VBUS when $\overline{OFFVBUS}$ and $\overline{SHDN}$ are 1 and ID_IN is open.

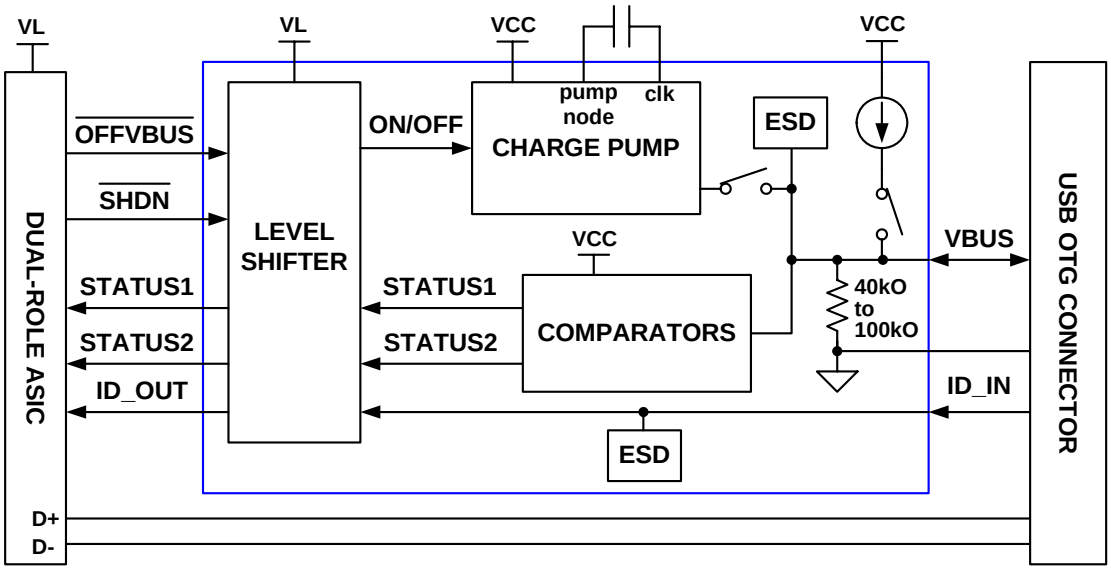


Fig. 2.1 An USB on-the-go (OTG) dual-role transceiver.

ID_IN	ID_OUT	CONFIGURATION
0	0	Device A
Open	V_L	Device B

Table 2.2 The identification detection of the USB on-the-go (OTG) dual-role transceiver.

STATUS1	STATUS2	SIGNIFICANCE
0	0	$V_{BUS} < V_{THSESEND}$
1	0	$V_{THSESEND} < V_{BUS} < V_{THSESVLD}$
0	1	$V_{THSESVLD} < V_{BUS} < V_{THVBUSVLD}$
1	1	$V_{BUS} > V_{THVBUSVLD}$

(a)

STATUS1	STATUS2	SIGNIFICANCE
0	1	$V_{BUS} < V_{TH,\overline{SHDN}}$
0	0	$V_{BUS} > V_{TH,\overline{SHDN}}$

(b)

Table 2.3 (a) The two status outputs of VBUS monitored by internal comparators. (b) The two status outputs of VBUS in shutdown mode.

$\overline{SHDN}$	$\overline{OFFVBUS}$	ID_IN	CHARGE PUMP	COMPARATORS
0	X	X	Inactive	Inactive
1	0	X	Inactive	Active
1	1	0	Active	Active
1	1	1	Inactive	Active

Table 2.4 The function selection of the USB on-the-go (OTG) dual-role transceiver.

Chapter 3

Prior Art

3.1 Dickson Charge Pump Circuit

In Fig. 3.1, there shows the 4-stage positive Dickson charge pump circuit using the pn-junction diode as the charge transfer device [2]. By pumping packets of charge along the diode chain as the coupling capacitors are successively charged and discharged during each half of the clock cycle. The voltages in the diode chain are not reset after each pumping cycle so that the average node potentials increase progressively from the input to the output of the diode chain. The nodes of diode chain are coupled to the inputs via capacitors in parallel instead of in series, so that the capacitors have to withstand the full voltages developed along the chain. As will be shown, the advantages of this configuration are that efficient multiplication can be achieved with relatively high values of stray capacitance, and that the current drive capability is independent of the number of multiplier stages.

As can be seen, the two clocks CLK and CLKB are in anti-phase with amplitude V_ϕ, and are capacitive coupled to alternate nodes along the diode chain. The output voltage of the diode charge pump circuit can be pumped high by the charges pushed from the power supply (VDD) to the output node (Vout) stage by stage. The voltage fluctuation of each pumping node is the same and can be expressed as

$$\Delta V = V_\phi \cdot \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_o}{f \cdot \left(C_{pump} + C_{par}\right)}$$

where V_ϕ is the voltage amplitude of the clock signals, C_{pump} is the pumping

capacitance, C_{par} is the parasitic capacitance at each pumping node, I_o is output loading current, and f is the clock frequency. In the above equation, the first item is shown the voltage swing at each node due to capacitive coupling from the clock. And the second item is shown the voltage by which the capacitors are charged and discharged when the multiplier is supplying an output current. If C_{par} and I_o are small enough and C_{pump} is large enough, C_{par} and I_o can be ignored. Because V_ϕ is usually the same as the normal power supply voltage (VDD), the voltage fluctuation of each pumping node can be simply expressed as $\Delta V = V_{DD}$.

The pumping gain of the charge pump circuit is expressed as

$$Gain = V_{n+1} - V_n = \Delta V - V_D$$

where V_D is the turn-on voltage of the pn-junction diode (the forward bias diode voltage or the diode cutoff voltage). Hence, the output voltage of the N-stage diode charge pump circuit can be expressed as

$$V_{out} - V_{dd} = N \cdot (\Delta V - V_D) - V_D = N \cdot \left(V_\phi \cdot \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_o}{f \cdot (C_{pump} + C_{par})} - V_D \right) - V_D .$$

It can be seen that voltage multiplication occurs, provided that

$$V_\phi \cdot \frac{C_{pump}}{C_{pump} + C_{par}} - \frac{I_o}{f \cdot (C_{pump} + C_{par})} - V_D > 0 .$$

In Fig. 3.2, there shows the 4-stage negative Dickson charge pump circuit using the pn-junction diode as the charge transfer device. As the above paragraph stated, the output voltage of the N-stage charge pump circuit without output loading current can be expressed as

$$V_{out} = 0 - [N \cdot (\Delta V - V_D) - V_D] = -N \cdot \left(V_\phi \cdot \frac{C_{pump}}{C_{pump} + C_{par}} - V_D \right) + V_D .$$

However, it is difficult to implement independent diodes in the same silicon substrate and the voltage drop across the diode is not scalable. In other words, the

diode charge pump circuit shown in Fig. 3.1 cannot be easily integrated into the standard CMOS process. Fig. 3.3 shows the 4-stage Dickson charge pump circuit in which the diode-connected MOSFETs are used to transfer the charges from this stage to the next stage. Thus, it can be easily integrated into standard CMOS processes. The gate and drain terminals of N-MOSFETs are connected and operated in saturation if it is on, while all the substrate terminals are grounded. And then, the charges are pushed from left to right.

The voltage difference between the drain terminal and the source terminal of the diode-connected MOSFET is its threshold voltage. As the voltage of each stage increases by the charge pumping, the threshold voltage of the diode-connected MOSFET increases due to the body effect. The maximum output voltage is limited by the body effect as N increases.

The voltage gain decreases and the output voltage becomes lower than the value obtained by the diode charge pump. Therefore, the output voltage of the charge pump cannot be a linear function of the number of stages and its efficiency decreases as the number of stage increases. The pumping gain of the charge pump circuit is expressed as

$$Gain = V_{n+1} - V_n = \Delta V - V_{th(Mi)}$$

where $V_{th(Mi)}$ is the threshold voltage of the diode-connected MOSFET *Mi*. Hence, the output voltage of the N-stage diode-connected MOSFET charge pump circuit can be expressed as

$$V_{out} - V_{dd} = \sum_{i=2}^{N} \left(\Delta V - V_{th(Mi)}\right) - V_{th(M1)}.$$

In the low voltage system, VDD (the supply voltage) and thus V_ϕ become smaller and smaller, so the impact of the latter two parameters gets worse and worse. It can be expected that when the supply voltage is decreased, the voltage of ΔV may also be

decreased. In addition, if the stage number is increased for high pumping voltages, the body effect is getting more seriously. Thus, the voltage pumping gain will be further reduced. It can be seen that voltage multiplication occurs, provided that

$$\Delta V - V_{th(Mi)} > 0 .$$

It should be noticed that the threshold voltage of the N-MOSFET is correlated with the voltage Vsb:

$$V_{th,n} = V_{T0,n} + \left[\sqrt{\left| -2\Phi_f \right| + V_{sb}} - \sqrt{\left| -2\Phi_f \right|} \right] \cdot \gamma .$$

Traditionally, the bulk terminals of the diode-connected MOSFET in the Dickson charge pump circuit are connected to ground. However, the threshold voltage ($V_{th(Mi)}$) of the diode-connected MOSFET becomes larger due to the body effect as the voltage on each pumping node is pumped higher. Therefore, the pumping efficiency of the Dickson charge pump circuit is degraded due to the body effect when the number of stages is increased. Since the threshold voltage cannot be scaled as much as the scaling trend of the supply voltage, the impact of threshold voltage increase to the output voltage lowering becomes more appreciable in the low supply voltage.

In Fig. 3.4, there shows the 4-stage negative Dickson charge pump circuit using the diode-connected MOSFETs as the charge transfer device. As the above paragraph stated, the output voltage of the N-stage charge pump circuit without output loading current can be expressed as

$$V_{out} = 0 - \sum_{i=2}^{N} \left(V_{\phi} \cdot \frac{C_{pump}}{C_{pump} + C_{par}} - V_{th(Mi)} \right) + V_{th(M1)} .$$

It should be noticed that the threshold voltage of the P-MOSFET is correlated with the voltage Vbs:

$$V_{th,p} = V_{T0,p} - \left[\sqrt{\left| -2\Phi_f \right| + V_{bs}} - \sqrt{\left| -2\Phi_f \right|} \right] \cdot \gamma .$$

3.2 Review of CMOS Charge Pump Circuits

3.2.1 Floating-Well Charge Pump Circuits

Several charge pump circuits based on the Dickson charge pump circuit were reported to enhance the pumping efficiency. In Fig. 3.5, there shows the floating-well charge pump circuit using the diode-connected P-MOSFETs as the charge transfer device [3]. In the triple-well process, the floating-well technique can be applied to eliminate the body effect issue on the diode-connected P-MOSFETs in the Dickson charge pump circuit. For proper operations with floating well condition, PMOS transistors are used with their body (n-well) floating. In the right part shown in Fig. 3.5, the n-well potential of (i+l)th stage, Vwell(i+l), is initially set to Vpp(i)-Vdiode during the phase 1, where Vdiode is the built-in potential of p+ to n-well diode. At the beginning of charge transfer, the source to bulk potential of (i+l)th PMOS transistor is equal to Vdiode (>0V), which means the effective threshold voltage (Vte) of the PMOS transistor is even slightly lower than the body-effect free threshold voltage (Vt0).

$$V_{te} = V_{T0,p} - \left[\sqrt{\left|-2\Phi_f\right| + \left(-V_{diode}\right)} - \sqrt{\left|-2\Phi_f\right|}\right] \cdot \gamma \Rightarrow 0 > V_{te} > V_{T0,p} \Rightarrow \left|V_{te}\right| < \left|V_{T0,p}\right|$$

$$V_{out}(Dickson) = V_{dd} + \sum_{i=2}^{N}\left(\Delta V - V_{th(Mi)}\right) - V_{th(M1)}$$

$$V_{out}(FWCP) = V_{dd} + \sum_{i=2}^{N}\left(\Delta V - \left|V_{te}\right|\right) - \left|V_{te}\right|$$

Due to their unique operating conditions, body effect is completely eliminated with a control circuit as simple as that of traditional two-phase Dickson charge pump circuit. We can know the same that the negative charge pump circuit utilizing the

same floating well concept with NMOS transistors. Each NMOS transistor is fabricated in a separated pocket p-well. However, the floating-well technique may generate substrate current in the floating-well devices to influence other circuits in the same chip and the voltage pumping gain per stage is still reduced by the threshold voltage.

3.2.2 Source-Bulk Connected Charge Pump

Several charge pump circuits based on the Dickson charge pump circuit were reported to enhance the pumping efficiency. In the triple-well process, the source-bulk connected devices can be applied to eliminate the body effect issue on the diode-connected MOSFETs in the Dickson Charge pump circuit [4]. Fig. 3.6 shows the charge pump circuit with the auxiliary MOSFETs to dynamically bias the body terminals of the diode-connected MOSFETs. Two auxiliary MOSFET's are introduced to control the body bias as shown in the figure. The source-side auxiliary MOSFET shares the source and the gate with the charge-transfer MOSFET and the drain-side auxiliary MOSFET shares the drain with the charge-transfer MOSFET. For each charge-transfer block, two auxiliary MOSFET’s and one charge-transfer MOSFET share the body separated from the body of other blocks.

When the charge-transfer MOSFET is ON, the source-side auxiliary MOSFET always turns on. Then the source and the body of the charge-transfer MOSFET are connected through the source-side auxiliary MOSFET, so that no reverse bias exists between the source and the body of the charge-transfer MOSFET preventing threshold voltage increase. When the charge transfer MOSFET is OFF, the drain-side

auxiliary MOSFET turns on so that the drain and the body of the charge transfer MOSFET are connected to prevent the body from floating.

When the ith charge-transfer MOSFET is ON, the source-side auxiliary MOSFET of the ith charge transfer MOSFET turns on so that the source and the body of the ith charge-transfer MOSFET are connected. According to the above argument, the threshold voltage of the ith charge-transfer MOSFET stays with Vt0 (threshold voltage at zero back bias) during the charge transfer state. In the steady state, the source, drain, and body voltage of the ith charge-transfer MOSFET according to the clock state is shown in Fig. 3.7. As shown in the figure, the body voltage of the charge-transfer MOSFET keeps track of higher value of the source or the drain voltage at each clock state by the auxiliary MOSFETs.

The source-bulk connected charge pump is proposed where the body of the MOSFET is used as an active terminal to avoid the problem associated with the threshold voltage increase in the charge transfer device. But this source-bulk connected technique increases the parasitic capacitance at each pumping node due to the large bulk-to-well pn-junction capacitance, so the pumping capacitors have to be enlarged. To make matter worse, it may also generate the substrate current in the floating-well devices.

3.2.3 Charge Transfer Switches (CTS's) Charge Pump

Fig. 3.8 shows a new charge pump (NCP-2) that can assign the control inputs for the CTS's dynamically by using pass transistors MN's and MP's [5]. The CTS's in NCP-2 can be turned off completely when required and can be turned on easily by the backward control. The expression for the single-stage voltage pumping gain is

$$Gain = V_{n+1} - V_n = \Delta V$$

When ck1 is high and ck2 is low, both the voltages at node 1 and node 2 are V_2, and the voltage at node 3 is 2ΔV above. If

$$2\Delta V > V_{tp} \quad and \quad 2\Delta V > V_{tn}(V_2)$$

where V_{tp} is the threshold voltage of P-MOSFET, then MP2 is turned on, causing MS2 being turned on by the voltage at node 3. In this period, MN2 is always off since its gate-to-source voltage is zero.

On the other hand, when ck1 is low and ck2 is high, the voltage at node 1 is V_1, both the voltages at node 2 and node 3 are 2 △ V above. If

$$2\Delta V > V_{tn}(V_1),$$

MN2 can be turned on and MS2 can be turned off completely. In this period, MP2 is also off, disengaging MS2 from the control of node 3.

This technique generates pretty good pumping gain at certain ranges of supply voltages, for example 2V to 3V, but becomes worse at some other ranges, such as about 1V. However, the output voltage of the NCP-2 is less than that predicted due to additional parasitic capacitors and switching delay. The NCP-2 circuit still suffered by the body effect. MOS transistors MDi are used as the diode-connecting path, which increases the parasitic capacitance. Moreover, the MD5 will drop a Vtn because it is diode-connected characteristic. Thus, it will reduce the output voltage gain.

3.2.4 Charge Pump for Low Supply Voltages

The four-stage positive charge pumping circuit using N-MOSFET's based on p-well/n-type substrate or triple-well technology is demonstrated in Fig. 3.9 [6]. The

new charge pumping circuit utilizes two new techniques to overcome the previous mentioned problems. The first is using small MOSFET's (Ms1 to Ms5) connected on the substrates of M1 to M5. The bottom part under the dash line in Fig. 3.9 is called the major pumping circuit. Ms1, Ms3 and Ms5 are turned on or off simultaneously with M1, M3 and M5. Similarly, Ms2 and Ms4 as well as M2 and M4 are on and off simultaneously. When M1 to M5 are on, their source voltages are equal to substrate voltages, so the body effect can be eliminated. The small pumping circuit controls gates of the major pumping circuit. The small pumping circuit is pumped simultaneously with the major pumping circuit. Since the channel widths of the transistors and the capacitors are very small, it only occupies very small area on a chip. The stage number of small pumping circuit can be adjusted to get the optimal voltages to control the gates of major pumping circuit. The last stage of small pumping circuit is connected to the output node, which is to balance the control signals of the major pumping circuit when the output node has load current. Because the gate voltages of M1 to M5 can be adjusted higher than the threshold voltage, $\Delta V > Vto$ is not the limit to make M1 to M5 turn on. Therefore, the pumping efficiency can be improved.

With these two new techniques, we can eliminate body effects and enhance charge transfer efficiency at low supply voltages (about 1V to 1.5V). The four-stage negative charge pumping circuit using P-MOSFET's is based on N-well/p-type substrate or triple-well technology. The similar idea can be also applied to the negative charge pumping circuit using all P-MOSFET's based on n-well/p-type substrate or triple-well technology. The stage number of the small pump has been optimized for the technology we adopted. The new charge pumping circuit can obtain excellent pumping gain and is more appropriate for pumping circuits with high stage number operated at very low supply voltage.

3.2.5 Charge Pump without Gate-Oxide Reliability Issue

Fig. 3.10 shows the 4-stage charge pump circuit without gate-oxide reliability issue [7]. Because the gate-source voltage (Vgs) and gate-drain voltage (Vgd) of all MOSFETs in this charge pump circuit will not exceed VDD, there is no high-voltage overstress on the gate oxide of the devices in this new proposed charge pump circuit.

There are two charge transfer branches named branch A and branch B in the proposed charge pump circuit. The difference between branches A and B is that the clock signals are out-of-phase. Branches A and B can be seen as two independent charge pump circuits and their output nodes are connected together. Because the clock signals of branch A and those of branch B are out-of-phase, the waveforms of nodes 1-4 and those of nodes 5-8 are also out-of-phase. Thus, branches A and B pump the output voltage high alternately.

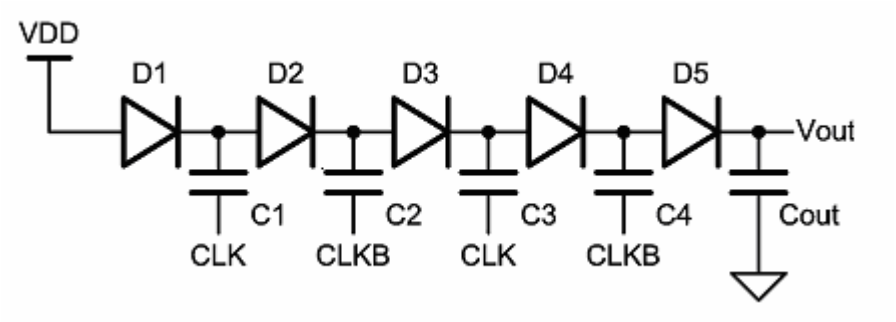


Fig. 3.1 The 4-stage positive Dickson charge pump circuit using the pn-junction diode as the charge transfer device.

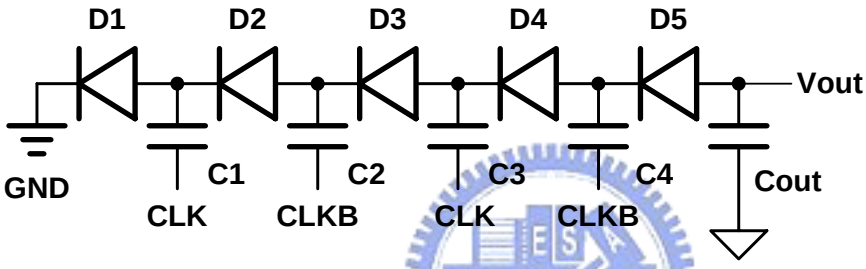


Fig. 3.2 The 4-stage negative Dickson charge pump circuit using the pn-junction diode as the charge transfer device.

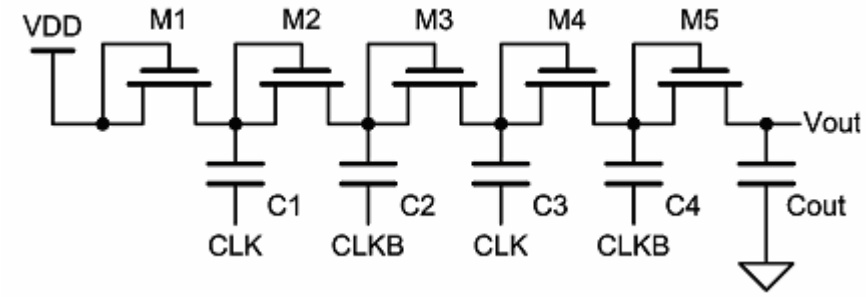


Fig. 3.3 The 4-stage positive Dickson charge pump circuit using the diode-connected MOSFETs as the charge transfer device.

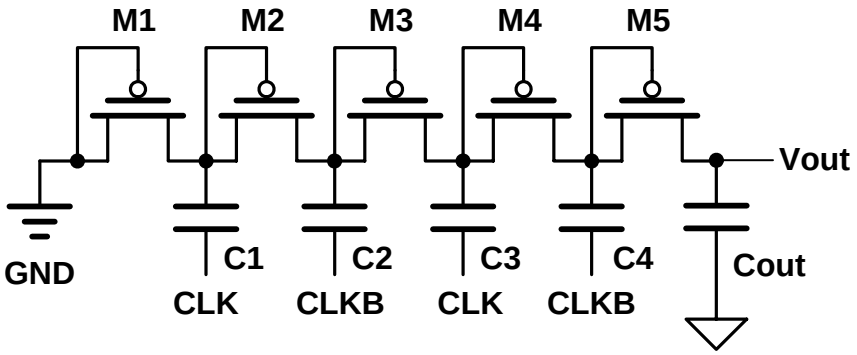


Fig. 3.4 The 4-stage positive Dickson charge pump circuit using the diode-connected MOSFETs as the charge transfer device.

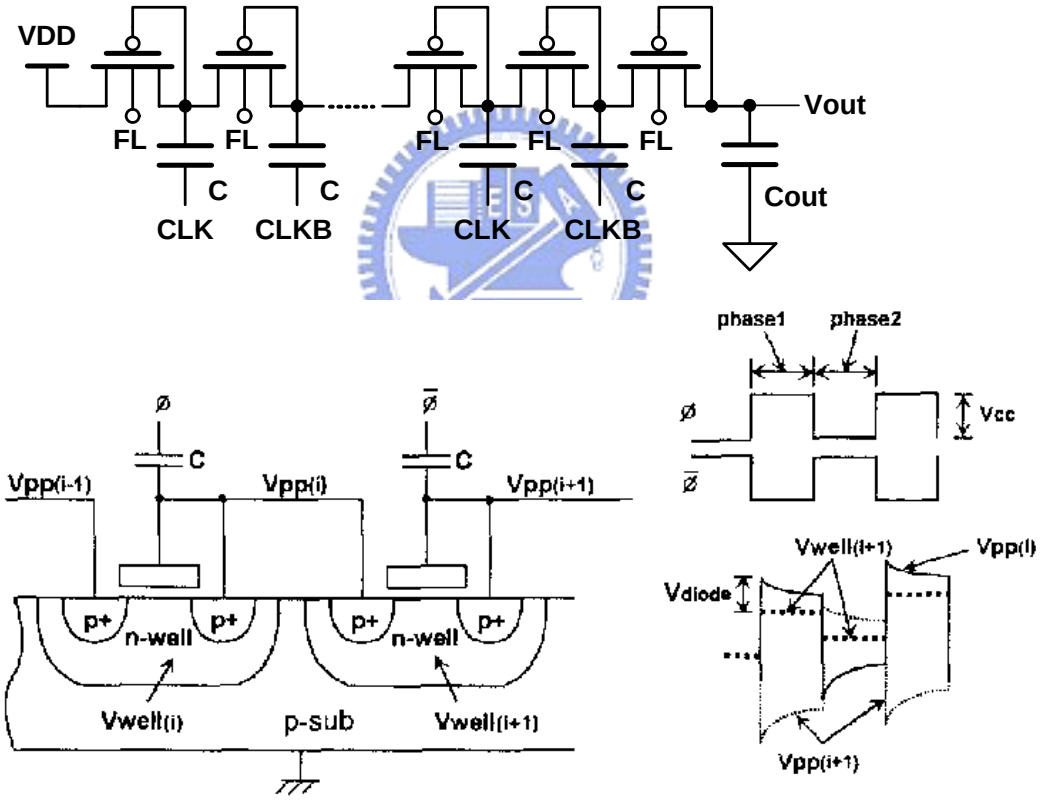


Fig. 3.5 The floating-well charge pump circuit using the diode-connected P-MOSFETs as the charge transfer device.

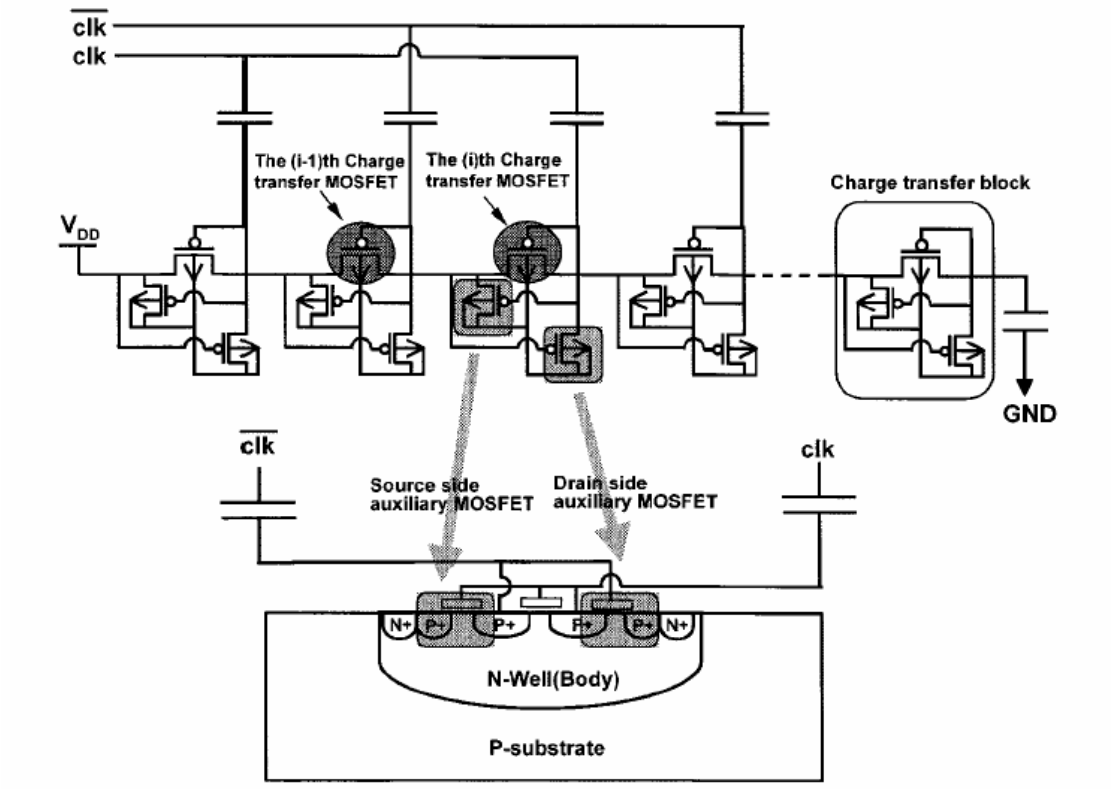


Fig. 3.6 The charge pump circuit with the auxiliary MOSFETs.

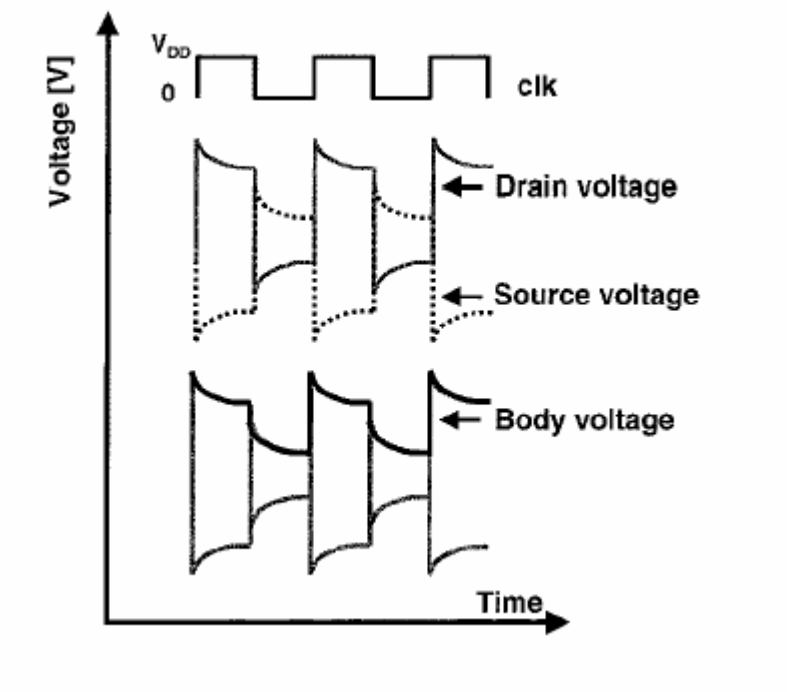


Fig. 3.7 At the steady state, the source, drain, and body voltage of the ith charge-transfer MOSFET according to the clock state.

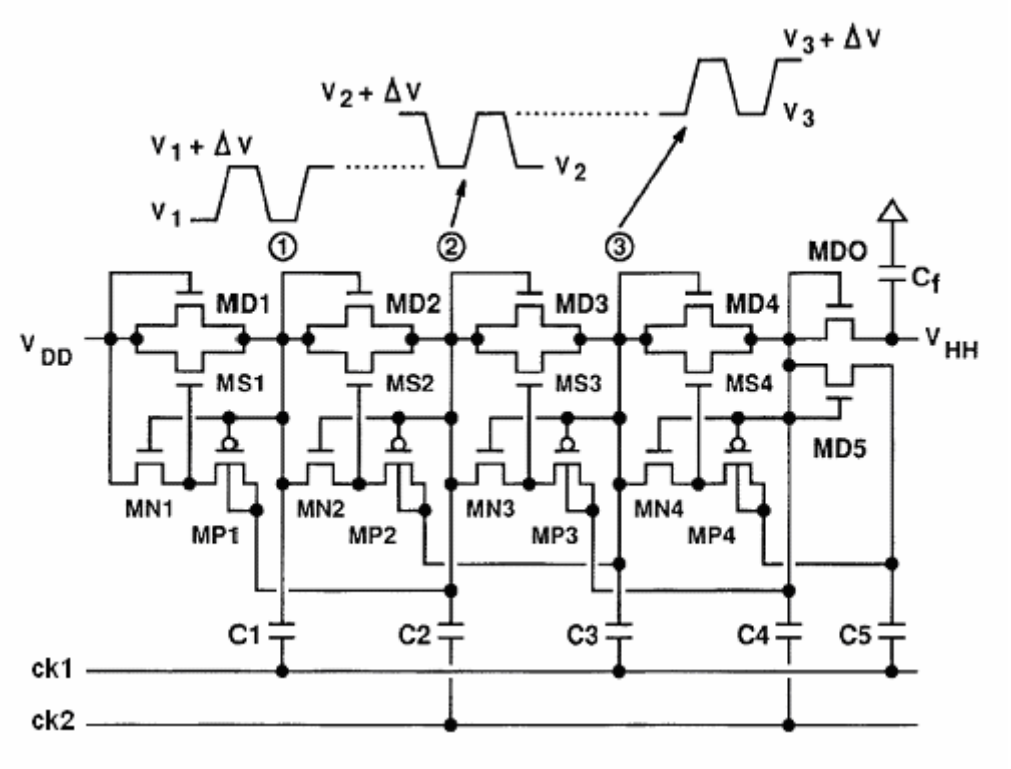


Fig. 3.8 The charge pump (NCP-2) that can assign the control inputs for the CTS's dynamically by using pass transistors MN's and MP's.

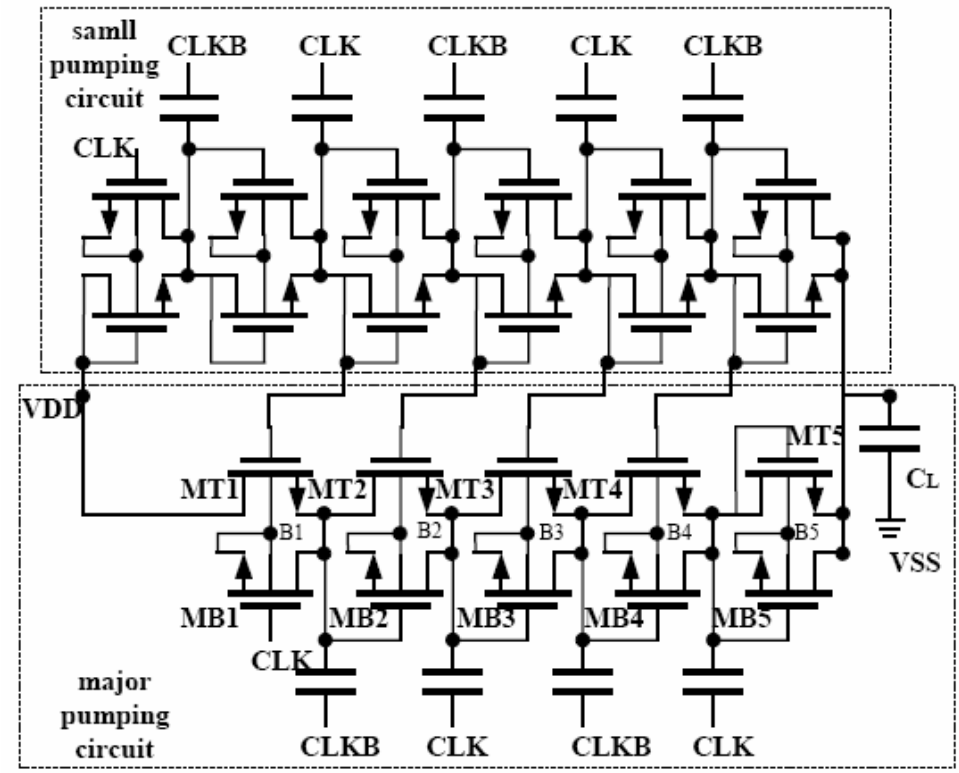
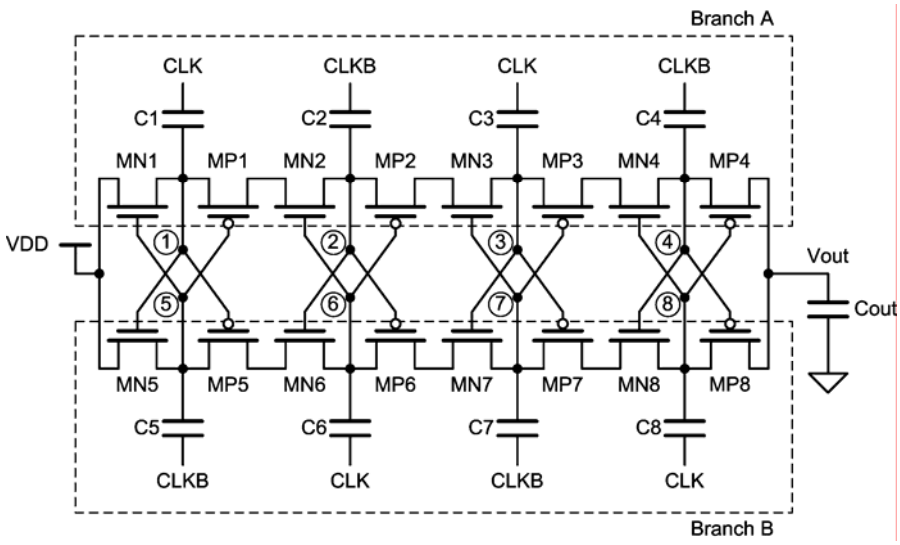
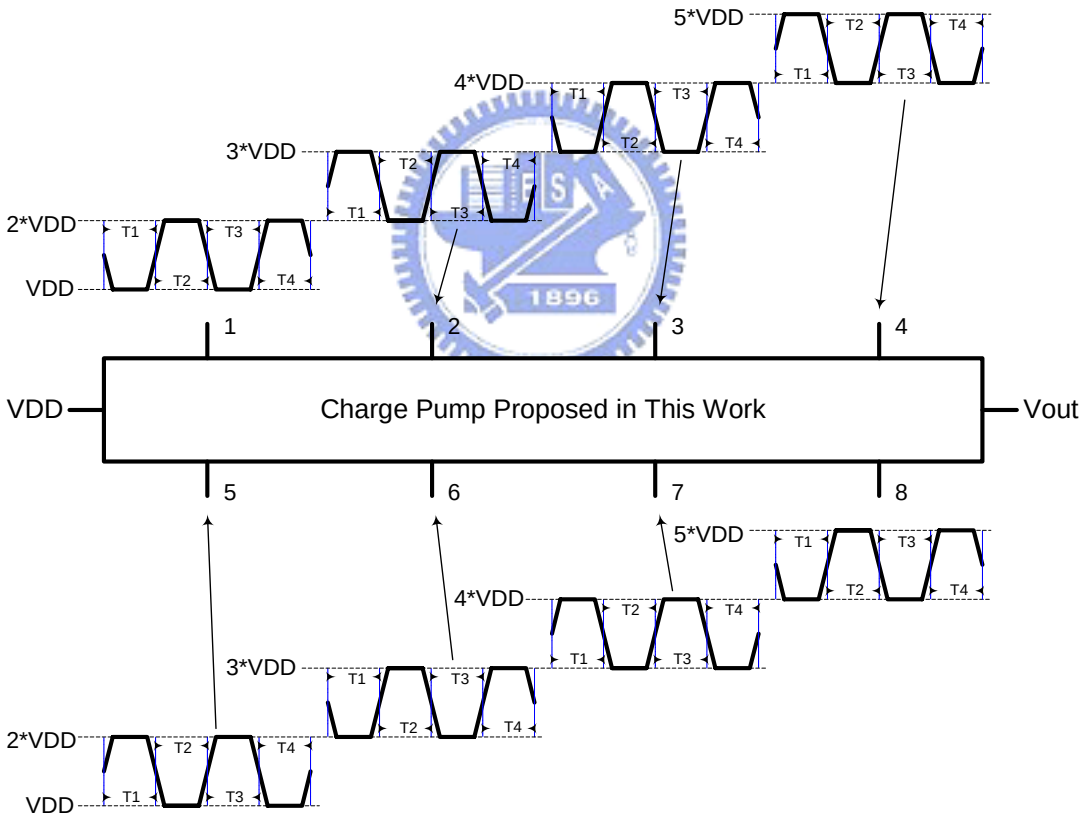


Fig. 3.9 The four-stage positive charge pump circuit for low supply voltages.



(a)



(b)

Fig. 3.10 (a) Scheme and (b) voltage waveforms of the 4-stages charge pump circuit without gate-oxide reliability.

Chapter 4

New Charge Pump Circuit Dealing with Gate-Oxide Reliability Issue in Low Voltage Processes

4.1 Consideration of Charge Pump Circuit Design

In previous chapter, we can know that Dickson charge pump used Diode-connected MOSFET to push charges to the next stage. When the diode is cut off to prevent the charges flowing back, the voltage across the diode, or the gate-oxide voltage of the diode-connected MOSFET, is almost 2*VDD-V_t. If VDD is the nominal supply voltage of the process, the diode-connected MOSFET is damaged in a short time.

In J. T. Wu's charge pump [5], not only these diode-connected MOSFET but also CTS's and their control circuits are suffered overstress. The only way for them to work safely in the low voltage process is to reduce the operating supply voltage to about 0.5*VDD.

4.1.1 Drawback of The Design Method (I)

In previous chapter 3.2.5, a new circuit design was presented. We can know that

this circuit dealing with gate-oxide reliability issue by controlling the voltage values of Vgs and Vds of CTS's within VDD. If we need to provide large output current loading or hope to have high efficiency of the output voltage, we always increase our value of pumping capacitors. But the large enough pumping capacitors may cost large area of the chip. Due to that reason, we will expect the circuit can be able to operate with fewer pumping capacitors. As shown in Fig. 4.1, there is a new charge pump circuit which almost the same with the one shown in Fig. 3.10(a), where the signal ck1 and the signal ck2 is also out of phase. Although in this design, the number of MOSFETs is increased, the pumping capacitors are decreased.

In Fig. 4.1, PMOS Mpx is considered to transfer the voltage of node a to node b. When ck1 is high and ck2 is low, the ideal voltage of node 1 is 2*VDD and the ideal voltage of node 2 is 2*VDD. At this moment, we hope the ideal voltage of node 3 is VDD transferred from node VDD to node 3 through Mna3, and the ideal voltage of node 4 is 3*VDD transferred from node Vo to node 4 through Mpa4. When ck1 is low and ck2 is high, the ideal voltage of node 1 is VDD and the ideal voltage of node 2 is 3*VDD. At this moment, we hope the ideal voltage of node 3 is 2*VDD transferred from node a to node 3 through Mpx and Mpa3, and the ideal voltage of node 4 is 2*VDD transferred from node a to node 4 through Mpx and Mna4.

The larger MOSFET's size can transfer the charge from node to node better. But the increasing of the MOSFET's size will cause the current flow in or out and then let the voltage of node to be unexpectedly. According to another view, to decrease the MOSFET's size is also not a good method about timing. If the MOSFET's size is smaller, the voltage of node 1 cannot change simultaneously with node 3. And with the same reason, the voltage of node 2 cannot change simultaneously with node4. The two statement described above might be worse in the situation of large output current loading or the clock signal with large rise time and fall time.

4.1.2 Drawback of The Design Method (II)

In previous chapter 3.2.5, a new circuit design was present to deal with gate-oxide reliability issue by controlling the voltage values of Vgs and Vds of CTS's within VDD. In conventional method, the clock generator is composed of an oscillator and some inverter buffers. In the prior designs described in chapter 3, this kind of generator is not suitable. The reason is illustrated in Fig. 4.2. Considering the first stage of the charge pump circuit in Fig. 3.10(a), when φ1 (CLK) is rising and φ2 (CLKB) is falling, it is expected that the voltages at node 1 and node 5 are respectively rising and falling as well. In fact, because the MOST switch Mna1 is not totally turned off immediately, the voltage at node 1 holds at VDD until the voltage at node 5 is falling to VDD+Vt to turn Mna1 off. Thus the performance is much worse than expected.

To prevent the leakage path, we propose new clock generator to replaces the conventional one. As shown in Fig. 4.3, there is a new charge pump circuit using the similar structure with the one shown in Fig. 3.10(a), where the clock signal and the output stage are different. If we use the structure shown in Fig. 3.10(a) with new clock generator, not including four MOSFETs M1, M2, M3 and M4, We can judge that the MOSFETs Mpa1, Mpa2, Mpa3 and Mpa4 are turned on during both ck1 and ck2 are LOW directly. Now, we divide the clock signal into four phases, the second and forth phases are for the normal operation discussed in the chapter 3.2.5. We no longer explain it in this chapter but just discuss the operation of the output stage.

During the second phase, the ideal voltage of node 2 is 3*VDD and the ideal voltage of node 4 is 2*VDD. At this moment, we hope the NMOS M1 turn on and let the voltage 2*VDD transferred from node 4 to node x. So, Mpa2 turns on and let the ideal voltage 3*VDD transferred from node 2 to node Vo and M3 turns off with

$|Vgs,_{M3}|=0$. On the other hand, we hope the PMOS M4 turn on and let the voltage 3*VDD transferred from node Vo to node y. So, Mpa4 turns off with $|Vgs,_{Mpa4}|=0$ and M2 turns off with $|Vgs,_{M2}|<|Vth,_{M2}|$. During the forth phase, the operation is in the same way as the one during the second phases.

Besides, the first and third phases are for the leakage preventing discussed above in this chapter. During the first and third phases, ck1 and ck2 are LOW; the voltages of node 2 and node 4 are 2*VDD. At this moment, we hope the PMOS M3 (M4) turn on and let the voltage 3*VDD transferred from node Vo to node x (node y). So, Mpa2 (Mpa4) turns off with $|Vgs,_{Mpa2}|=0$ ($|Vgs,_{Mpa4}|=0$) and NMOS M1 (M2) also turns off with $|Vgs,_{M1}|=0$ ($|Vgs,_{M2}|=0$). The signal ck1 and the signal ck2 are also out of phase. Although in this design, the number of MOSFETs is increased, the pumping capacitors are decreased.

The larger MOSFET's size can transfer the charge from node to node better. But the increasing of the MOSFET's size will not only cost chip area but also cause the current flow in or out and then let the voltage of node we want to be unexpectedly. To summarize above-mentioned two kinds of designs, we can find that the CTS's gate voltage source must use direct and simple way not complicated one.

4.2 A Proposed Charge Pump Circuit (I)

In conventional method, the clock generator composed of an oscillator and some inverter buffers generator two out of phase clock ck1 and ck2. In previous chapter 3.2.5, a new circuit design dealing with gate-oxide reliability issue is not suitable for this kind of generator. The reason is illustrated in Fig. 4.2 and discussed in previous chapter 4.1.2 before. As we known, the performance is much worse than expected. To prevent the leakage path, we propose new clock generator to replaces the

conventional one.

4.2.1 The Description of This Design

In order to enhance the pumping gain, it is necessary that CTS's be used in the proposed charge pump circuit. The problems are how we should design the control circuit of CTS's to eliminate overstress on their gate-oxide. The proposed charge pump circuit presented in this work is illustrated in Fig. 4.4(a).

In Fig. 4.4(a), clock signals ck1, ck2, ck3 and ck4 are shown and have its amplitude as high as the supply voltage VDD. There are two identical branches, labeled to branch A and branch B in the charge pump circuit. The only difference between them is the order of the clock signals. That means, if the clock signals of the first and the second pumping stages in the up part of branch A are ck1 and ck2, the clock signals in the up part of branch B must be ck2 and ck1; similarly, if the clock signal of the first and the second pumping stages in the down part of branch A is ck3 and ck4, the clock signals in the down part of branch B must be ck4 and ck3. The clock generator is described in detail in the chapter 7.

Assuming the CTS's in this design are turned on/off properly, each branch can be seen as an independent charge pump circuit. Similarly, each part of the branch can be seen as an independent charge pump circuit respectively. Because the clock signals of branch A and branch B are out of phase, the waveforms at node 1-4 and node 5-8 are out of phase, either. The expected waveforms at node 1-8 are shown in Fig. 4.4(b). Now, let us check if the CTS's work properly.

1) For the 1st stage: As illustrated in Fig. 4.4(b), at time interval T1, clock ck1 is LOW, clock ck2 is HIGH, clock ck3 is LOW, and clock ck4 is HIGH. At this moment, V15 and V35 (V15 and V17) are –VDD for nominal operation. Thus MOSFET switch Mna1 and Mna3 are turned on to push the charges from power supply to node 1 and

node 3, and Mnb1 and Mnb3 are turned off to block the path from node 5 and node 7 back to power supply. On the other hand, at time interval T3, clock ck1 is HIGH, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is LOW. At this moment, V15 and V35 (V15 and V17) are VDD for ideal operation. Mna1 and Mna3 are turned off in order to prohibit the path from node 1 and node 3 back to power supply, and Mnb1 and Mnb3 are turned on to push the charges from power supply to node 5 and node 7. In addition, at time interval T2 and T4, clock ck1 is LOW, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is HIGH. At this moment, V15 is 0, V35 is VDD and V17 is –VDD for ideal operation. Mna1, Mna3, Mnb1 and Mnb3 are turned off in order to prohibit the path from node 1, node 3, node 5 and node 7 back to power supply.

2) For the other pumping stages: Consider the 2nd stage for example. At time interval T1, clock ck1 is LOW, clock ck2 is HIGH, clock ck3 is LOW, and clock ck4 is HIGH. At this moment, V17 and V26 (V37 and V46) are respectively –VDD and VDD for nominal operation. Mpa1 and Mna2 (Mpa3 and Mna4) are turned off in order to prohibit the path from node 2 (node 4) back to node 1 (node 3). V35 and V26 (V37 and V28) are respectively –VDD and VDD for nominal operation, so Mpb1 and Mnb2 (Mpb3 and Mnb4) are turned on to push the charges from node 5 (node 7) to node 6 (node 8). On the other hand, at time interval T3, clock ck1 is HIGH, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is LOW. At this moment, V35 and V26 (V37 and V28) are respectively VDD and –VDD for ideal operation. Thus MOSFET switches Mpb1 and Mnb2 (Mpb3 and Mnb4) are turned off in order to prohibit the path from node6 (node 8) to node 5 (node 7). V17 and V26 (V37 and V46) are respectively VDD and –VDD for nominal operation, so Mpa1 and Mna2 (Mpa3 and Mna4) are turned on to push the charges from node 1 (node 3) to node 2 (node 4). In addition, at time interval T2 and T4, clock ck1 is LOW, clock ck2 is LOW, clock ck3

is HIGH, and clock ck4 is HIGH. At this moment, Mpa1, Mna2, Mpa3 and Mna4 (Mpb1, Mnb2, Mpb3 and Mnb4) are turned off in order to prohibit the path from node 2 (node 6) back to node 1 (node 5) and from node 4 (node 8) back to node 3 (node 7).

3) For the output stages: At time interval T1, clock ck1 is LOW, clock ck2 is HIGH, clock ck3 is LOW, and clock ck4 is HIGH. At this moment, V28 and V48 are VDD for nominal operation. Thus MOSFET switch Mpa2 and Mpa4 are turned on to push the charges from node 2 and node 4 to the output node. Mpb2 and Mpb4 are turned off to block the path from the output node back to node 6 and node 8 due to the voltage across the output node and the node 4 is 0. On the other hand, at time interval T3, V46 and V48 are -VDD for ideal operation. Mpb2 and Mpb4 are turned on to push the charges from node 6 and node 8 to the output node. Mpa2 and Mpa4 are turned off to block the path from the output node back to node 2 and node 4 due to the voltage across the output node and the node 8 is 0. In addition, at time interval T2 and T4, clock ck1 is LOW, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is HIGH. At this moment, Mpa2, Mpa4, Mpb2 and Mpb4 are turned off in order to prohibit the path from output node back to node2, node 4, node 6 and node 8.

4.2.2 Body Connection of Branches in This Design

The analysis above verifies that the CTS's in the proposed charge pump circuit work as expected. By observing carefully, we can find that branch A and branch B are like two charge pump circuits, but their operations separate by half a period. Thus, branch A and branch B should pump the output voltage high alternately.

We have known that the circuit structures of branch A and branch B are the same, but their operations separate by half a period. So, we give an example for branch A to explain the body connection of the CTS's. As shown in Fig. 4.4(c), there is a

complete structure of branch A. At time interval T1, clock ck1 is LOW, clock ck2 is HIGH, clock ck3 is LOW, and clock ck4 is HIGH. The NMOS Mna1 and Mna3 are turned on to push the charges from node VDD to node 1 and node 3. At this moment, the body terminal of Mna1 and Mna3 are connected with the source terminal of Mna1 and Mna3 by turn on the right part NMOS and turn off the left part NMOS. Similarly, the PMOS Mpa2 and Mpa4 are turned on to push the charges from node 2 and node 4 to node Vo. At this moment, the body terminal of Mpa2 and Mpa4 are connected with the source terminal of Mpa2 and Mpa4 by turn on the left part PMOS and turn off the right part PMOS. So, no reverse bias exists between the source and the body terminal of the charge transfer MOSFET preventing threshold voltage increase. The PMOS Mpa1, Mpa3 and the NMOS Mna2, Mna4 are turned off to block the path from the node 2 to node 1 and node 4 to node 3. At this moment, the body terminal of Mpa1 and Mpa3 are connected with the source terminal of Mpa1 and Mpa3 by turn on the right part PMOS and turn off the left part PMOS. And the body terminal of Mna2 and Mna4 are connected with the source terminal of Mna2 and Mna4 by turn on the left part NMOS and turn off the right part NMOS.

On the other hand, at time interval T3, clock ck1 is HIGH, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is LOW. The PMOS Mpa1, Mpa3 and the NMOS Mna2, Mna4 are turned on to push the charges from node 1 to node 2 and node 3 to node 4. At this moment, the body terminal of Mpa1 and Mpa3 are connected with the source terminal of Mpa1 and Mpa3 by turn on the left part PMOS and turn off the right part PMOS. And the body terminal of Mna2 and Mna4 are connected with the source terminal of Mna2 and Mna4 by turn on the right part NMOS and turn off the left part NMOS. So, no reverse bias exists between the source and the body terminal of the charge transfer MOSFET preventing threshold voltage increase similarly. The NMOS Mna1, Mna3 and PMOS Mpa2, Mpa4 are turned off to block the path from

the node 1, 3 to node VDD and node Vo to node 2, 4. At this moment, the body terminal of Mna1 and Mna3 are connected with the source terminal of Mna1 and Mna3 by turn on the left part NMOS and turn off the right part NMOS. And the body terminal of Mpa2 and Mpa4 are connected with the source terminal of Mpa2 and Mpa4 by turn on the right part PMOS and turn off the left part PMOS.

In addition, at time interval T2 and T4, clock ck1 is LOW, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is HIGH. At this moment, the body terminal of PMOS Mpa1, Mpa3, Mpa2 and Mpa4 are connected with the source terminal of Mpa1, Mpa3, Mpa2 and Mpa4 by turn on the right part PMOS and turn off the left part PMOS. Due to the clock design, the body terminal of NMOS Mna1, Mna3, Mna2 and Mna4 are floating during time interval T2 and T4.

As shown in Fig. 4.4(d), the performance of charge pump circuit (I) compares with the prior arts in chapter 3. We can confirm that charge pump circuit (I) has better performance than the prior one.

4.3 A Proposed Charge Pump Circuit (II)

We have designed the charge pump circuit illustrated in Fig. 4.4(a) with CTS's to eliminate overstress on their gate-oxide. If we need to provide large output current loading or hope to have high efficiency of the output voltage, we always increase our value of pumping capacitors. But the large enough pumping capacitors may cost large area of the chip, so does the large number of MOSFETs. Due to that reason, we will expect the proposed charge circuit (I) can be able to operate with fewer or smaller pumping capacitors and do the pumping work with just one branch under normal operation.

4.3.1 Drawback of The Design Method (III)

According to the discussion in the chapter 4.1, both two methods have the drawbacks about the control signals of the gate terminal of MOSFETs. So, we may try every possible means to solve this problem. In the chapter 4.2.1, the charge pump circuit illustrated in Fig. 4.4(a) has two branches A and B which are like two charge pump circuits and their operations separate by half a period. Due to the feature of the charge pump circuit illustrated in Fig. 4.4(a), we can hope to decrease the size of branch B, and regard branch B as the auxiliary charge pump of the branch A. We will expect the control signals of the gate terminal of MOSFETs of branch A can be generated by the smaller branch B. Fig. 4.5(a) and (b) show the pumping speed of branch A and B without and with the output current loading, in this simulation the output node of branch A and B are not connected with each other. In Fig. 4.5(a), we can know that the smaller branch B will transfer the charges quickly to achieve the output voltage we wanted. And in Fig. 4.5(b), we can know that the smaller branch B may not suffer the large output current loading so that to the output voltage level we wanted will decrease. Although we try the different value of the MOSFETs and the pumping capacitors sizes, two branches A and B will not be able to pump high simultaneously due to their different sizes. So, the overstress on their gate-oxide cannot be eliminated at all time during the pumping progress.

4.3.2 The Description of This Design

As the discussion in the chapter 4.1, we can find that the control signals of the gate terminal of MOSFETs must be driven directly by the stable clock source. In order to enhance the pumping gain [8], it is necessary that CTS's be also used in the

proposed charge pump circuit (II). We should design the control circuit of CTS's to eliminate overstress on their gate-oxide. The proposed charge pump circuit (II) presented in this work is illustrated in Fig. 4.6(a).

In Fig. 4.6(a), clock signals ck1, ck2, ck3 and ck4 are shown and have its amplitude as high as the supply voltage VDD. There are two identical branches, labeled to branch A and branch B in the charge pump circuit. The only difference between them is the order of the clock signals. That means, if the clock signals of the first and the second pumping stages in the up part of branch A are ck1 and ck2, the clock signals in the up part of branch B must be ck2 and ck1. Similarly, if the clock signal of the branch A is ck3, the clock signals in the branch B must be ck4 that is out of phase with ck3. The clock generator is described in detail in the chapter 7.

Assuming the CTS's in this design are turned on/off properly, each branch can be seen as an independent charge pump circuit respectively. Because the clock signals of branch A and branch B are out of phase, the waveforms at node 1, 2, x and node 3, 4, y are out of phase, either. The expected waveforms at node 1-4, x and y are shown in Fig. 4.6(b). Now, let us check if the CTS's work properly.

1) For the 1st stage: As illustrated in Fig. 4.6(b), at time interval T1, clock ck1 is LOW, clock ck2 is HIGH, clock ck3 is LOW, and clock ck4 is HIGH. At this moment, V13 is –VDD for nominal operation. Thus MOSFET switch Mn1 is turned on to push the charges from power supply to node 1, and Mn4 is turned off to block the path from node 3 back to power supply. On the other hand, at time interval T3, clock ck1 is HIGH, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is LOW. At this moment, V13 is VDD for ideal operation. Mn1 is turned off in order to prohibit the path from node 1 back to power supply, and Mn4 is turned on to push the charges from power supply to node 3. In addition, at time interval T2 and T4, clock ck1 is LOW, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is HIGH. At this moment, V13 is 0,

for ideal operation. Mn1 and Mn4 are turned off in order to prohibit the path from node 1 and node 3 back to power supply.

2) For the other pumping stages: Consider the 2nd stage for example. At time interval T1, clock ck1 is LOW, clock ck2 is HIGH, clock ck3 is LOW, and clock ck4 is HIGH. At this moment, V13 and V24 are respectively –VDD and VDD for nominal operation. Mp1, Mn2 and Mn3 are turned off in order to prohibit the path from node 2 back to node 1; Mp3, Mn5 and Mn6 are turned on to push the charges from node 3 to node 4. On the other hand, at time interval T3, clock ck1 is HIGH, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is LOW. At this moment, V13 and V24 are respectively VDD and –VDD for ideal operation. Thus, MOSFET switches Mp1, Mn2 and Mn3 are turned on to push the charges from node 1 to node 2; Mp3, Mn5 and Mn6 are turned off in order to prohibit the path from node 4 to node 3. In addition, at time interval T2 and T4, clock ck1 is LOW, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is HIGH. At this moment, V13 and V24 are both 0 for ideal operation. Mp1, Mn2, Mn3, Mp3, Mn5 and Mn6 are turned off in order to prohibit the path from node 2 back to node 1 and from node 4 back to node 3.

3) For the output stages: At time interval T1, clock ck1 is LOW, clock ck2 is HIGH, clock ck3 is LOW, and clock ck4 is HIGH. At this moment, V2a is VDD for nominal operation. NMOS Mnx is turned on to push the charges from node a to node x. The voltage value of node x is 2*VDD for nominal operation and V2x is VDD. Mp2 is turned on to push the charges from node 2 to the output node. V4b is 0 for nominal operation, so NMOS Mny is turned off to block the path from node y to node b. Now, the voltage value of node y is 3*VDD and Vy4 is VDD for nominal operation. Mp4 is turned off to block the path from the output node back to node 4 due to the voltage across the output node and the node y is 0. On the other hand, at time interval T3, clock ck1 is HIGH, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is LOW.

At this moment, V4y is VDD for nominal operation. NMOS Mny is turned on to push the charges from node b to node y. The voltage value of node y is 2*VDD for nominal operation and V4y is VDD. Mp4 is turned on to push the charges from node 4 to the output node. V2a is 0 for nominal operation, so NMOS Mnx is turned off to block the path from node x to node a. Now, the voltage value of node x is 3*VDD and Vx2 is VDD for nominal operation. Mp2 is turned off to block the path from the output node back to node 2 due to the voltage across the output node and the node x is 0. In addition, at time interval T2 and T4, clock ck1 is LOW, clock ck2 is LOW, clock ck3 is HIGH, and clock ck4 is HIGH. At this moment, V2a and V4b are 0 for nominal operation, so NMOS Mnx and Mny arte turned off to block the path from node x (node y) to node a (node b). V2x and V4y are -VDD for nominal operation, so PMOS Mp2 and Mp4 arte turned off to block the path from the output node to node 2 (node 4) due to the voltage across the output node and the node x (node y) is 0.

The analysis above verifies that the CTSs in the proposed charge pump circuit (II) work as expected. By observing carefully, we can find that the circuit structures of branch A and branch B are the same, but their operations separate by half a period. Thus, branch A and branch B should pump the output voltage high alternately.

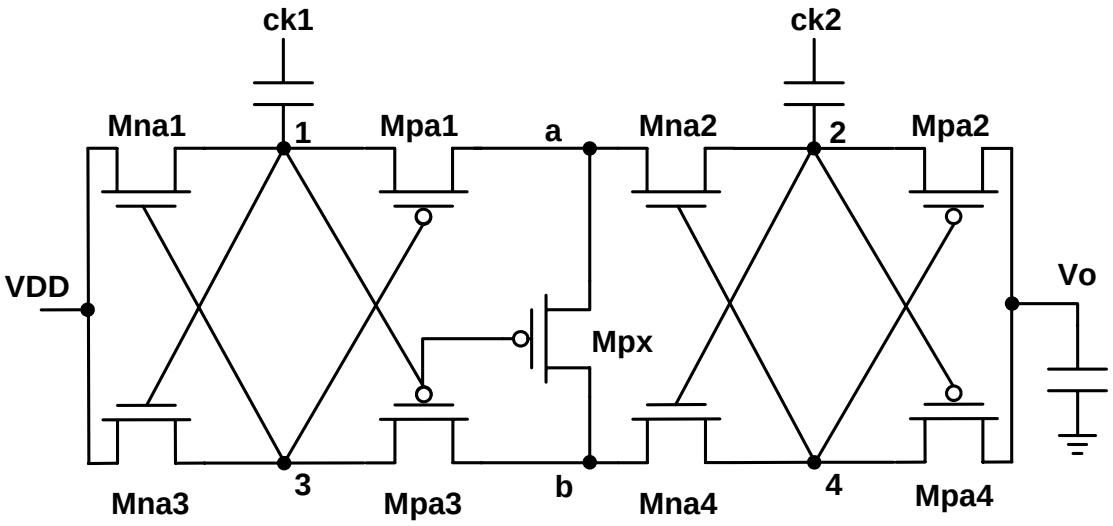


Fig. 4.1 The charge pump circuit dealing with gate-oxide reliability issue with fewer pumping capacitors.

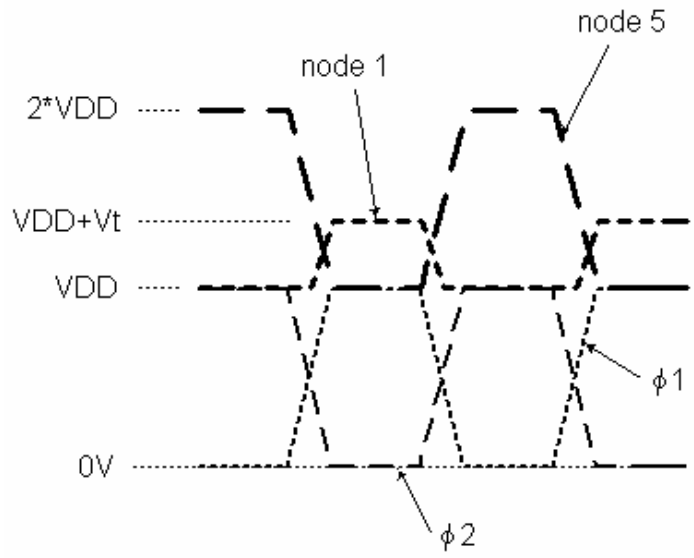


Fig. 4.2 The expected clock waveforms of the charge pump circuit shown in Fig. 3.12.

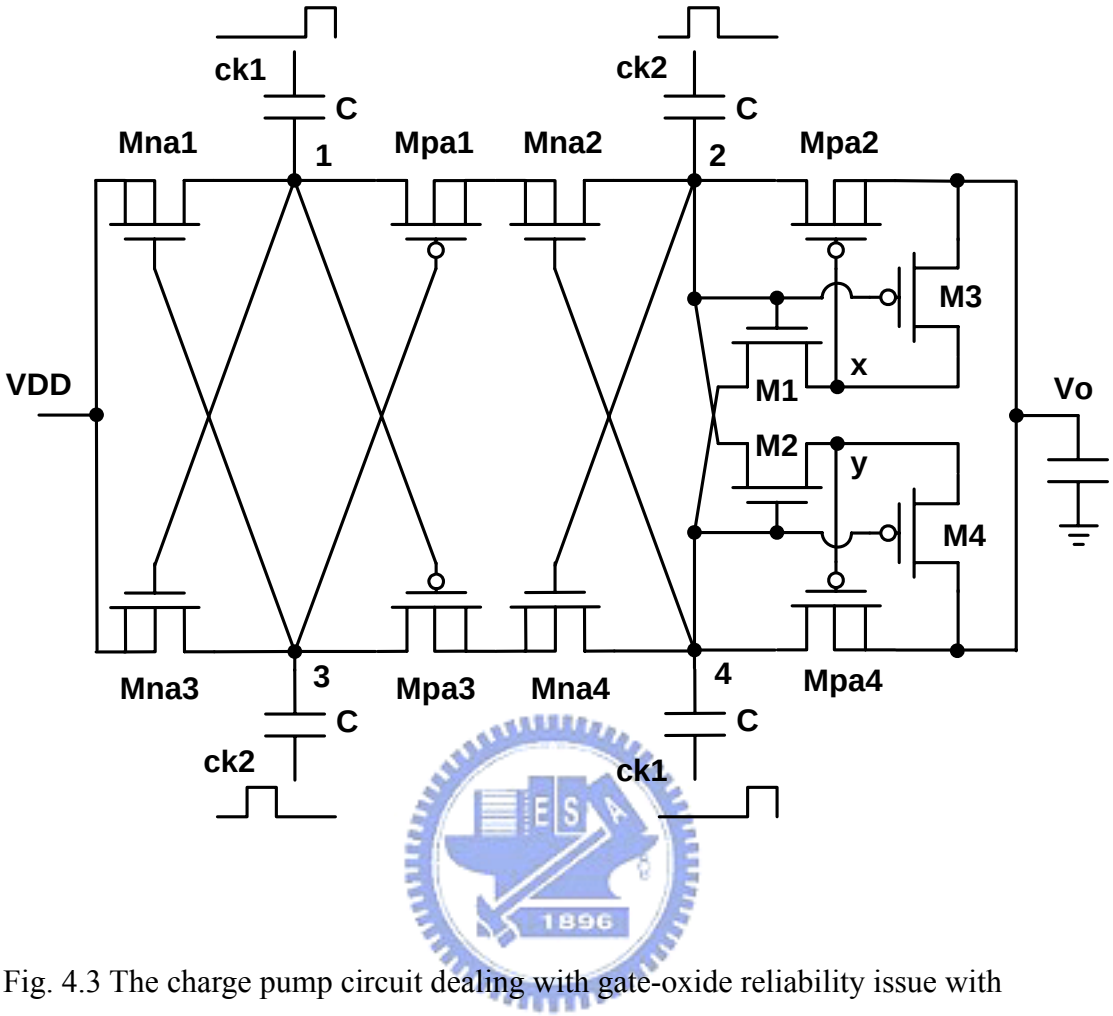
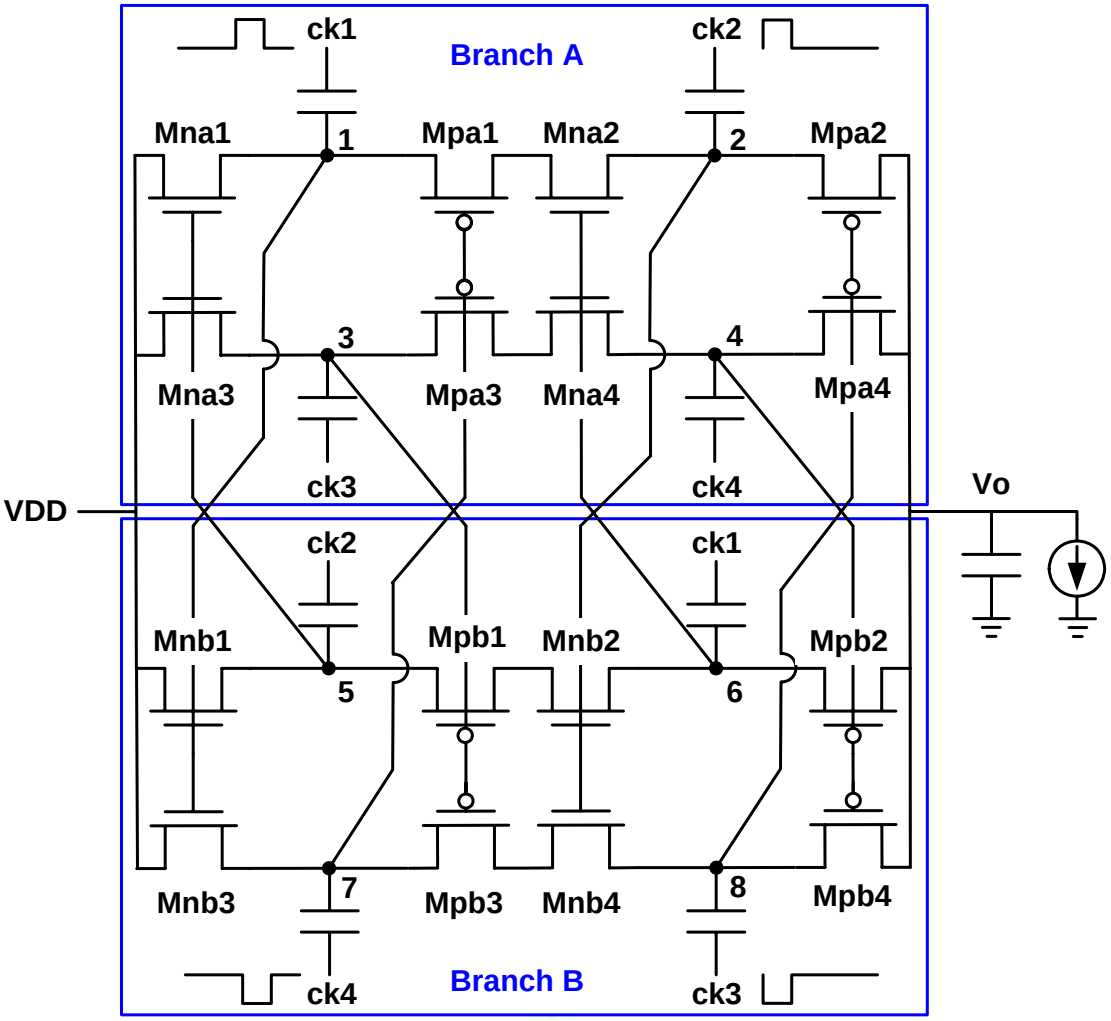
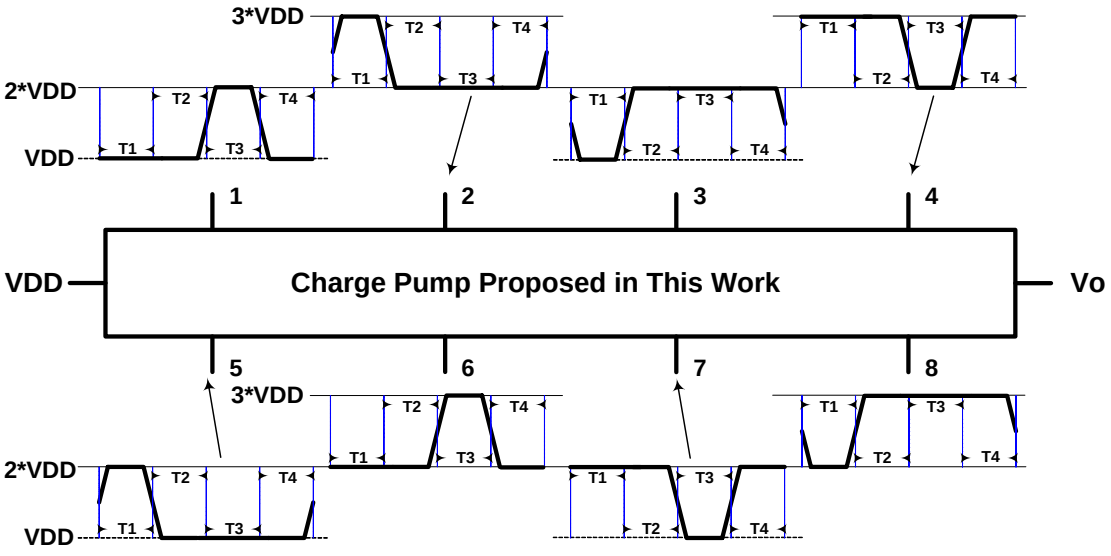


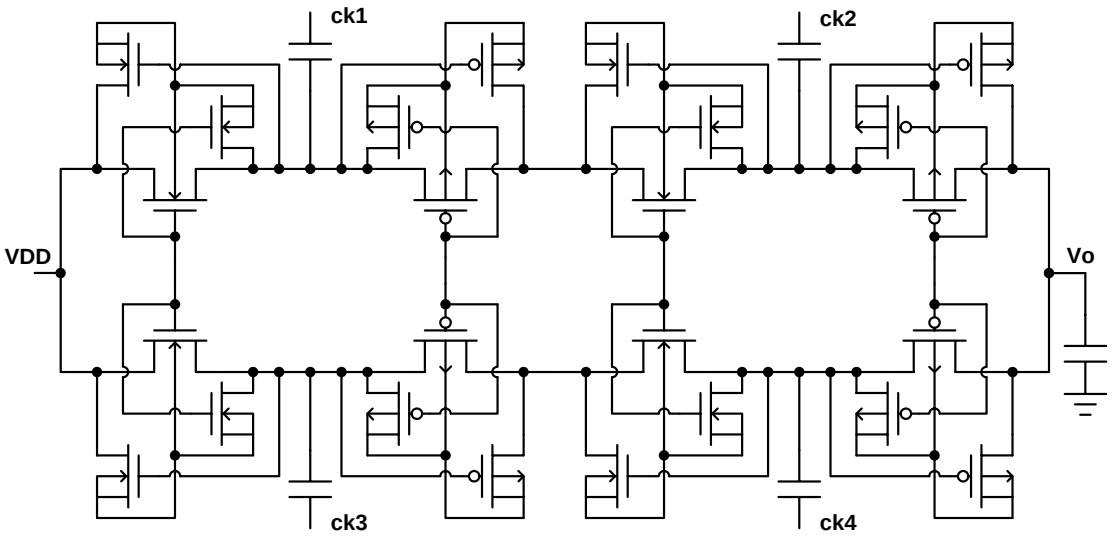
Fig. 4.3 The charge pump circuit dealing with gate-oxide reliability issue with different clock signal and output stage.


ck1
Branch A
ck2
Mna1
1
Mpa1
Mna2
2
Mpa2
3
4
Mna3
Mpa3
Mna4
Mpa4
ck3
ck4
VDD
Vo
ck2
ck1
Mnb1
Mpb1
Mnb2
Mpb2
5
6
7
8
Mnb3
Mpb3
Mnb4
Mpb4
ck4
Branch B
ck3

(a)


3*VDD
2*VDD
VDD
T1
T2
T3
T4
1
2
3
4
VDD
Charge Pump Proposed in This Work
Vo
5
6
7
8
3*VDD
2*VDD
VDD

(b)

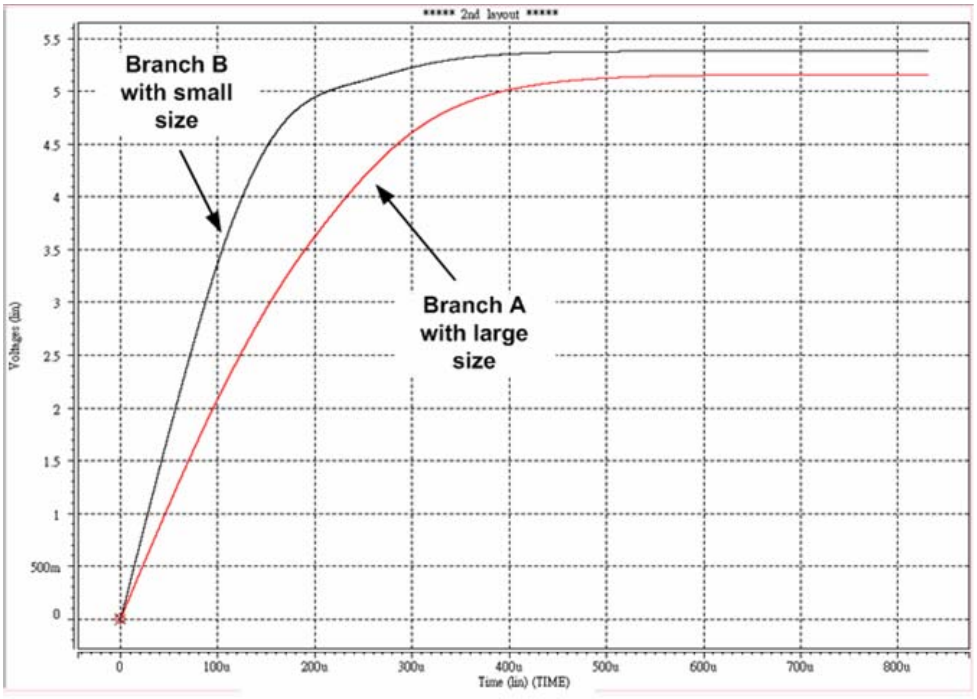


(c)

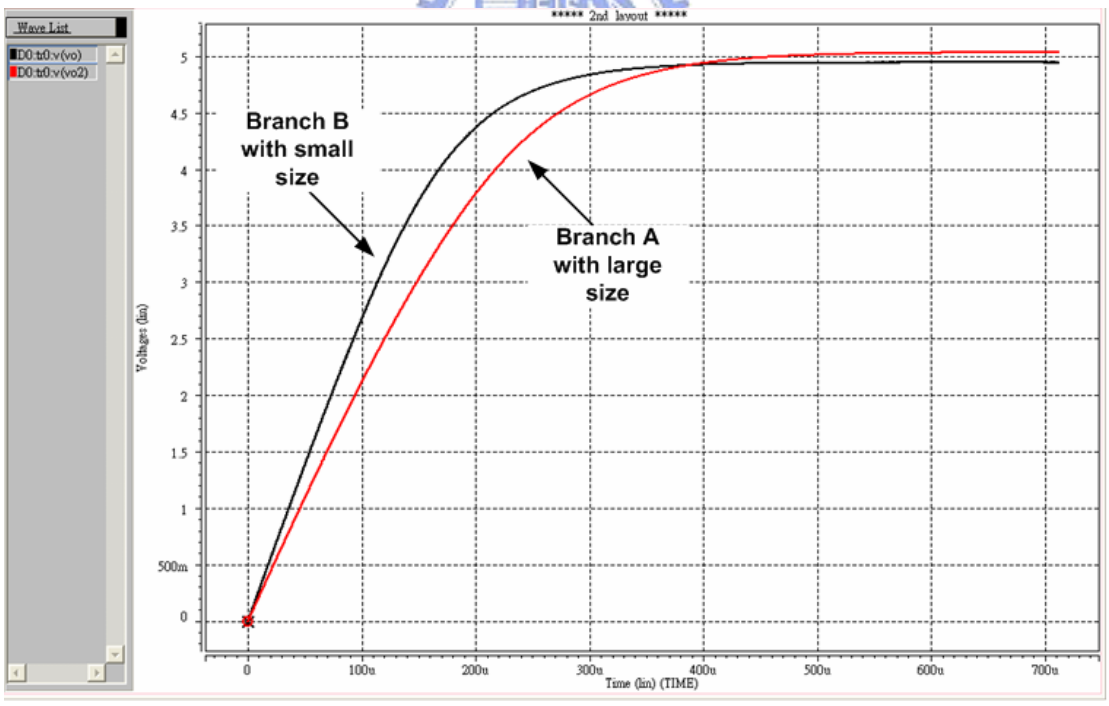
Charge Pump Designs	Pumping Gain	Body Effect	Suffer Gate-Oxide Reliability Issue	Suitable for Low-Voltage Process	Circuit Performance
JSSC'76 [2]	VDD–Vth	Yes	With	No	bad
VLSI-Circuits'97 [3]	VDD–|Vte|	No	With	No	bad
JSSC'00 [4]	VDD–Vt0	No	With	No	bad
JSSC'98 [5]	VDD	Yes	With	No	good
ISCAS'99 [6]	VDD	No	With	Yes	good
ISCAS'04 [7]	VDD	Yes	Without	No	good
This Work 1	VDD	No	Without	Yes	better

(d)

Fig. 4.4 (a) The charge pump circuit (I) dealing with gate-oxide reliability issue with four different clock signals. (b) The expected waveforms at node 1-8. (c) The complete structure of branch A for example. (d) The performance of charge pump circuit (I) comparing with the prior arts in chapter 3.

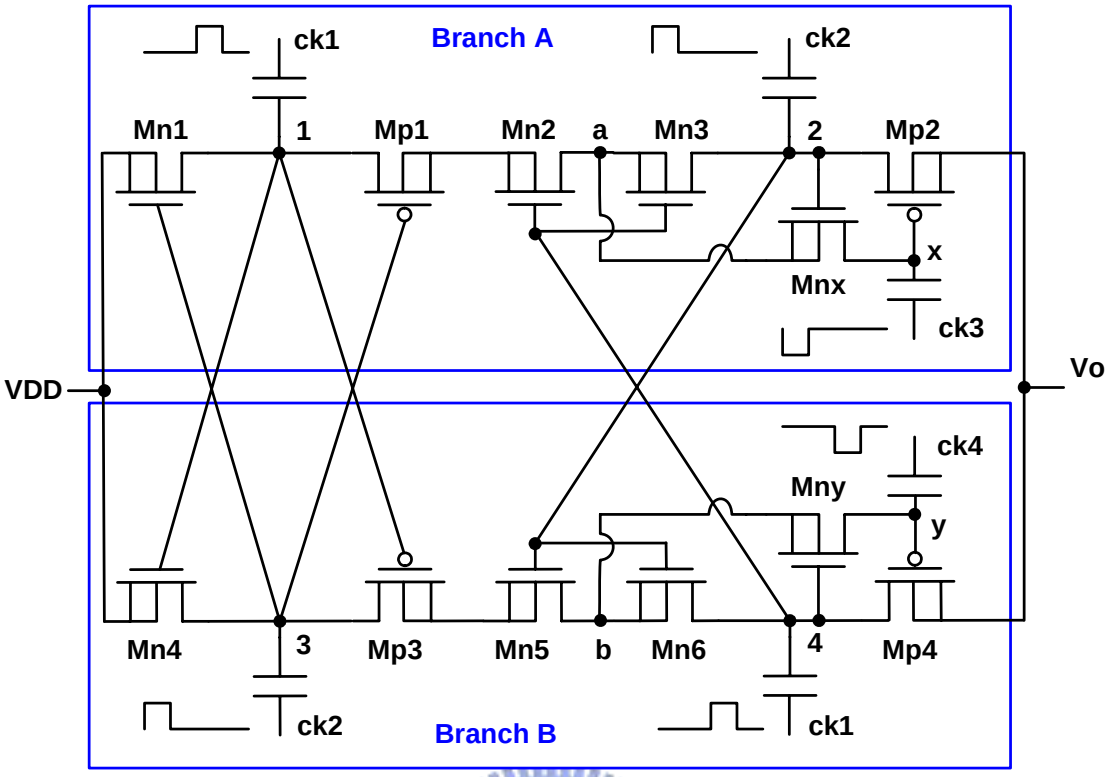


(a)

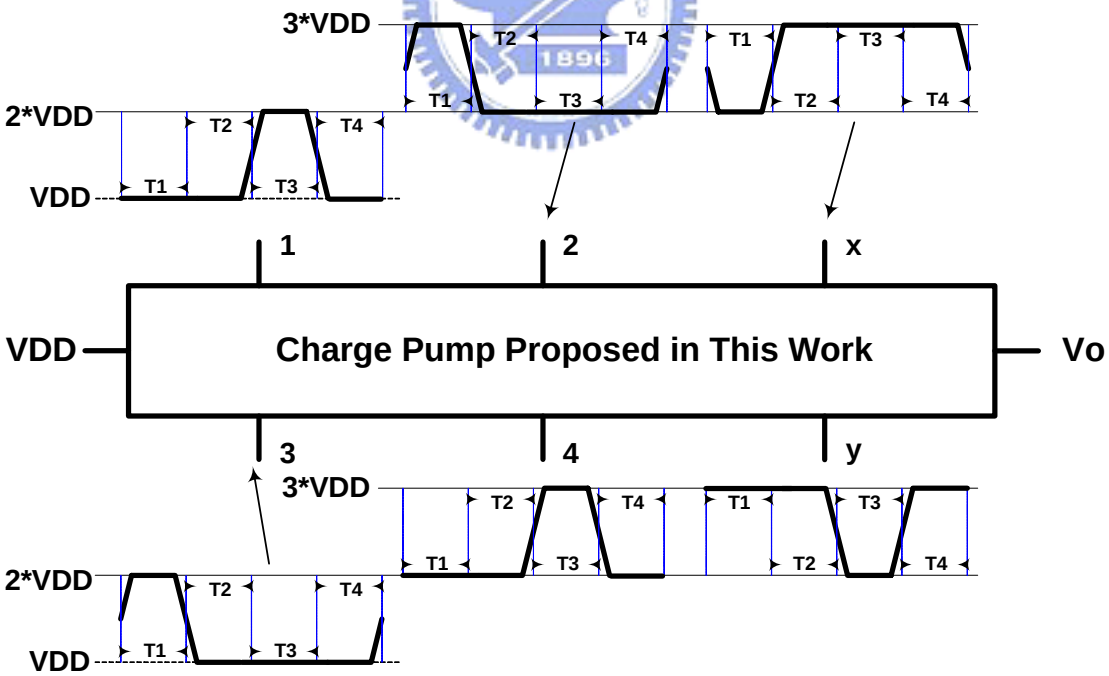


(b)

Fig. 4.5 (a) The pumping speed of branch A and B without the output current loading. (b) The pumping speed of branch A and B with the output current loading,



(a)



(b)

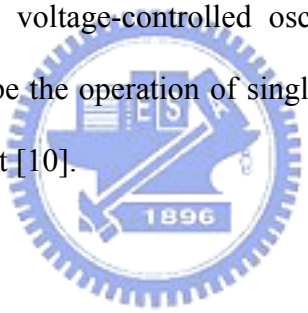
Fig. 4.6 (a) The charge pump circuit (II) dealing with gate-oxide reliability issue with four different clock signals. (b) The expected waveforms at node 1-4 and node x-y.

Chapter 5

New Charge Pump Circuit with The Feedback Loop

5.1 Oscillators

Oscillators are an integral part of many electronic systems. In charge pump circuit the oscillator can be used to be the clock generator. In this chapter, we introduce the concept of the voltage-controlled oscillator and the ring oscillator briefly [9]. Finally, we describe the operation of single-ended coupled ring oscillator used in the charge pump circuit [10].



5.1.1 Voltage-Controlled Oscillator

Most applications require that the output frequency of oscillators can be a function of a control input, usually a voltage. An ideal voltage-controlled oscillator (VCO) [9] is a circuit whose output frequency is linear function of its control voltage:

$$\omega_{out} = \omega_0 + K_{VCO} \cdot V_{ctl}$$

where ω_0 represents the intercept corresponding to V_{ctl}=0 and K_{VCO} denotes the gain or sensitivity of the circuit. The achievable range, $\omega_2 - \omega_1$, is called the tuning range.

A. Center Frequency:

The center frequency (i.e., the midrange value in Fig. 5.1) determined by the environment in which the VCO is used.

B. Tuning Range:

The required tuning range is dictated by two parameters: (1) the variation of the VCO center frequency with process and temperature and (2) the frequency range necessary for the application. The center frequency of some CMOS oscillators may vary by a factor of two at the extremes of process and temperature. Thus, a sufficiently wide (≧2×) tuning range is needed to guarantee that the VCO output frequency can be driven to the desired value. Also, some applications incorporate clock frequencies that must vary by one to two orders of magnitude depending on the operation, demanding a proportionally wide tuning range.

An important concern in the design of VCOs is the variation of the output phase and frequency as a result of noise on the control line. For a given noise amplitude, the noise in the output frequency is proportional to K_{VCO} because $\omega_{out} = \omega_0 + K_{VCO} \cdot V_{ctl}$. Thus, to minimize the effect of noise in V_{ctl}, the VCO gain must be minimized, a constraint in direst conflict with the required tuning range. In fact, if, as shown in Fig. 5.1, the allowable range of V_{ctl} is from V_1 to V_2 (e.g., from 0 to VDD) and the tuning range must span at least ω_1 to ω_2, then K_{VCO} must satisfy the following requirement:

$$K_{VCO} = \frac{\omega_2 - \omega_1}{V_2 - V_1}$$

Note that, for a given tuning range, K_{VCO} increases as the supply voltage decreases, making the oscillator more sensitive to noise on the control line.

5.1.2 Ring Oscillator

The ability to generate multiple phases is a very useful property of ring oscillators [9]. A simple implementation of ring oscillators that does not require

resistors is depicted in Fig. 5.2. Suppose the circuit is released with an initial voltage at each node equal to the input voltage that results in an equal output voltage of the inverters. The circuit would remain in this state indefinitely with identical stages and no noise in the devices. But, when noise components disturb each node voltage, yielding a growing waveform, the signal eventually exhibits rail-to rail swing

Now, assuming the circuit of three-stages ring oscillator shown in Fig. 5.2(a) begins with Vx=VDD, then Vy=0 and Vz=VDD. Thus, when the circuit is released, Vx begins to fall to zero, forcing Vy to rise to VDD after one inverter delay, T_D, and Vz to fall to zero after another inverter delay. In Fig. 5.2(b), the circuit therefore oscillates with a delay of T_D between consecutive node voltages, yielding a period of $6*T_D$. We can know that the oscillation frequency, f_{osc}, of an N-stage ring equals $(2*N*T_D)^{-1}$, where T_D denotes the large-signal delay of each stage. Thus, to vary the frequency, T_D can be adjusted. Ring oscillators employing more than three stages also feasible. The total number of inverters in the loop must be odd so that the circuit does not latch up. For example, a ring can incorporate five inverters which providing a frequency of $1/(10*T_D)$.

5.1.3 Single-Ended Coupled Ring Oscillator

The three-stage single-ended coupled ring oscillator is shown in Fig. 5.3. In Fig. 5.3(a), there is one stage of the single-ended coupled ring oscillator integrated by a fast inverter, a slow inverter and the transmission gates [10]. The operation of this stage is described below. If the control signal Vctl is HIGH, the above part of transmission gates is turned on, and then the fast output signal of the fast inverter will be transmitted to the output node. The below part of transmission gates is turned off in

order to prevent the slow output signal of the slow inverter from transmitting to the output node. The opposite one is come to say that if the control signal Vctl is LOW, the below part of transmission gates is turned on, and then the slow output signal of the slow inverter will be transmitted to the output node. The above part of transmission gates is turned off in order to prevent the fast output signal of the fast inverter from transmitting to the output node.

In Fig. 5.3(b), due to the discussion above, we can know that when the control signal Vctl is HIGH, $\overline{V_{ctl}}$ is LOW, the three-stage single-ended coupled ring oscillator can generate the fast frequency clock. This single-ended coupled ring oscillator might operate like the three-stage ring oscillator with wide MOSFET width or narrow MOSFET length inverter. The opposite one is come to say that when the control signal Vctl is LOW, $\overline{V_{ctl}}$ is HIGH, the three-stage single-ended coupled ring oscillator can generate the slow frequency clock. This single-ended coupled ring oscillator might operate like the three-stage ring oscillator with narrow MOSFET width or wide MOSFET length inverter.

5.2 Comparators

A voltage comparator [11] is a circuit that compares the instantaneous value of an input signal Vin(t) with a reference voltage Vref and produces a logic output level depending on whether the input is larger or smaller than the reference level. A comparator is therefore essentially a high-gain op-amp designed for open-loop operation. But unlike an op-amp it dies not require frequency compensation. After operational amplifiers, it is the second most widely used components in electronic circuits.

5.2.1 Differential-Input Comparator

The transfer curve of the ideal differential comparator is shown in Fig. 5.4(a) [11]. The negative input of the comparator in Fig. 5.4(a) is tied to a reference voltage Vref. The ideal transfer curve shown in Fig. 5.4(b) corresponds to a differential gain of infinity. When the positive input is greater than Vref, the output is high (V_{OH}). When the positive input is less than Vref, the output is low (V_{OL}). In actuality the differential gain has a finite value equal to Av and the transfer curve of such a comparator is shown in Fig. 5.4(c), where V_{iL} and V_{iH} are the input excess voltages called the overdrive. The overdrive is the input level that drives the comparator from some initial saturated input condition to an input level barely in excess of that required to cause the output to switch state.

5.2.2 Source-Coupled Differential-Pair Comparator

The method in source-coupled differential-pair comparator shown in Fig. 5.5 is using a controlled amount of positive feedback to effectively increase the driver devices transconductance [11]. The gain of the positive feedback gain stage is given by

$$A_d = \sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_3}} \cdot \frac{1}{1-\alpha}$$

where $\alpha = (W/L)_5 / (W/L)_3$ is the positive feedback factor that is responsible for increasing the gain.

Often, comparators are used to convert a very slowly varying input signal into an output with abrupt edges, or they are used in a noisy environment to detect an input signal crossing a threshold level. If the response time of the comparator is much faster

than the variation of the input signal around the threshold level, the output will chatter around the two stable levels as the input crosses the comparison voltage. By employing positive (regenerative) feedback in the circuit, it will exhibit a phenomenon called hysteresis, which will eliminate the chattering effects. The regenerative comparator is commonly referred to as a Schmitt trigger.

At the switching point, assume that the current through transistors Q1 and Q2 are i1 and i2, respectively. Then we have

$$\begin{cases} i_1 + i_2 = I_O \\ i_2 = i_5 = i_3 \cdot \alpha = i_1 \cdot \alpha \end{cases}$$

or

$$\begin{cases} i_1 = \dfrac{I_O}{1+\alpha} \\ i_2 = \dfrac{I_O \cdot \alpha}{1+\alpha} \end{cases}.$$

In the situation that the gate of Q1 is tied to ground, the difference between Vgs2 and Vgs1 is the positive trigger level, equal to

$$V_{trig+} = V_{GS2} - V_{GS1} = \sqrt{\frac{i_2}{k'\cdot(W/L)_2}} - \sqrt{\frac{i_1}{k'\cdot(W/L)_1}} = \sqrt{\frac{I_O}{k'\cdot(W/L)_1}} \cdot \frac{\sqrt{\alpha}-1}{\sqrt{1+\alpha}}.$$

Similarly, it can be shown that the negative trigger point is given by

$$V_{trig-} = \sqrt{\frac{I_O}{k'\cdot(W/L)_1}} \cdot \frac{1-\sqrt{\alpha}}{\sqrt{1+\alpha}}.$$

The hysteresis can be calculated as

$$V_H = V_{trig+} - V_{trig-} = 2 \times \sqrt{\frac{I_O}{k'\cdot(W/L)_1}} \cdot \frac{\sqrt{\alpha}-1}{\sqrt{1+\alpha}}$$

where $\alpha = (W/L)_5/(W/L)_3 = (W/L)_6/(W/L)_4$.

5.3 Charge Pump Circuit with Feedback

To prevent the value of output voltage from varying with the charging of output current loading. The proposed charge pump circuit with feedback loop is shown in Fig. 5.6. Here, we use the single-ended coupled ring oscillator described in chapter 5.1.3 and the source-coupled differential-pair comparator described in chapter 5.2.2 in this feedback loop. The operation of this circuit will be discussed below.

The input signal of comparator is the output voltage divided by the resistor divider. During the initial pumping state, the voltage value of output is very small, so the input signal of comparator is smaller than Vref. The Vctl, the output voltage of the comparator, is HIGH in order to let the VCO circuit works as the three-stage fast ring oscillator. This method can speed up the pumping progress and let the output voltage achieve the level we want quickly.

After the pumping progress, the voltage value of output is as high as we want, so the input signal of comparator is larger than Vref now. The Vctl, the output voltage of the comparator, is LOW in order to let the VCO circuit works as the three-stage slow ring oscillator. This method can lower the pumping efficiency let the output voltage maintain the level we want.

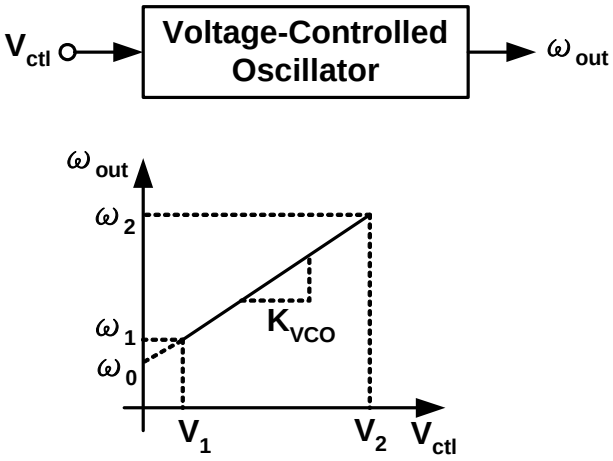
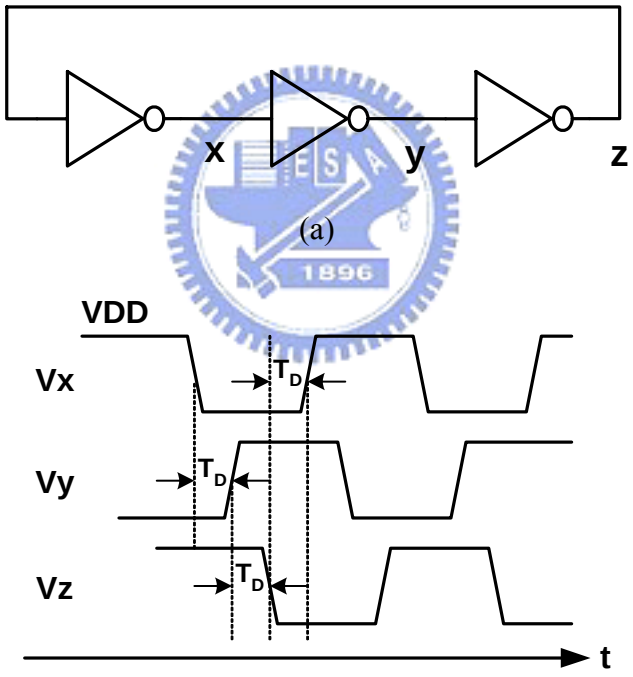
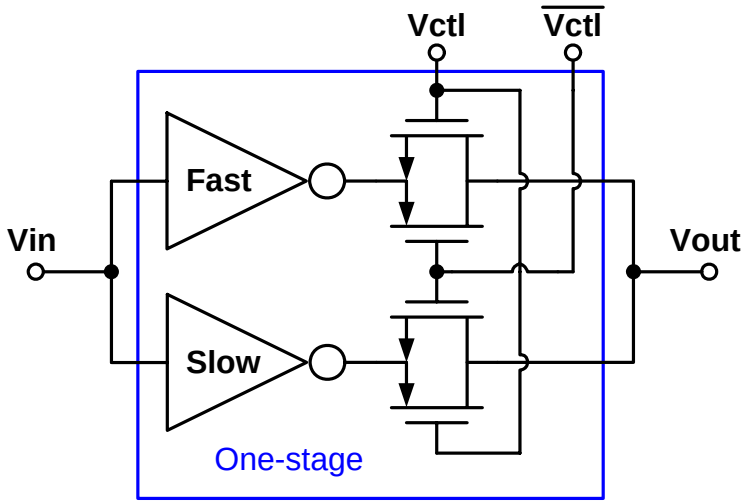


Fig. 5.1 Definition of a VCO.

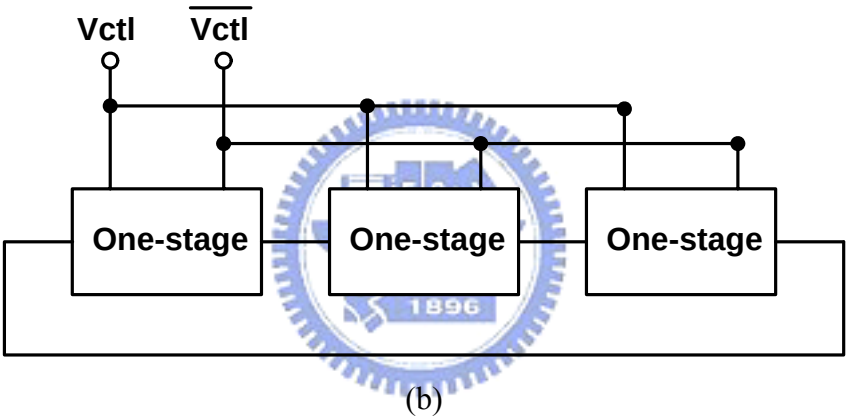


(b)

Fig. 5.2 (a) Ring oscillator using CMOS inverters. (b) Waveforms of ring oscillator when Vx is initialized at VDD.

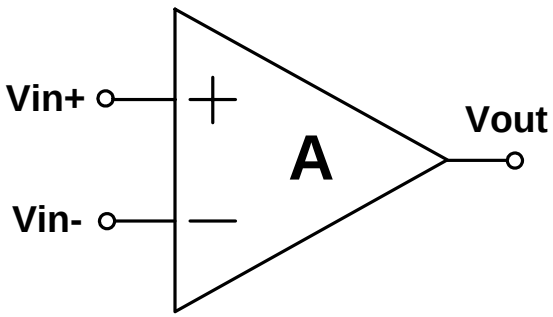


(a)

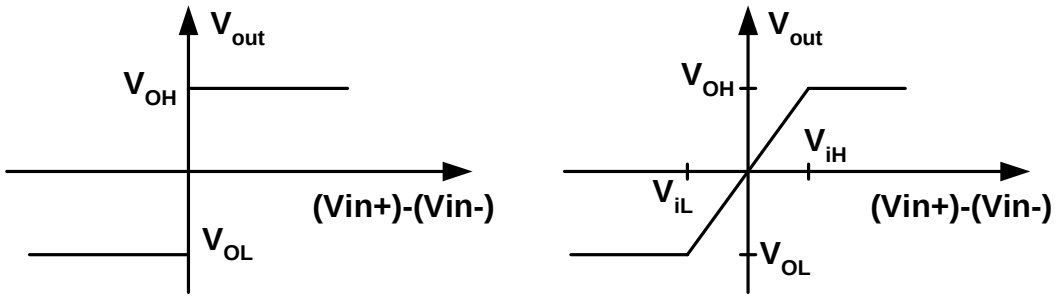


(b)

Fig. 5.3 (a) The one stage of single-ended coupled ring oscillator. (b) The three-stage of single-ended coupled ring oscillator.



(a)



(b) (c)

Fig. 5.4 (a) The differential-input comparator. (b) Transfer curve of ideal comparator. (c) Transfer curve of comparator with finite gain.

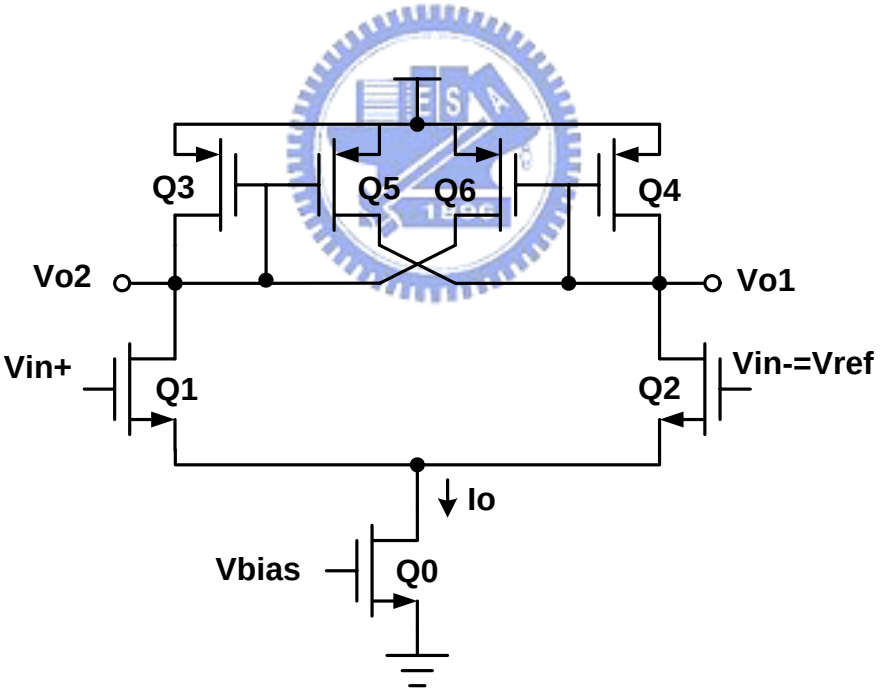


Fig. 5.5 Source-coupled differential pair that uses positive feedback to provide increased gain.

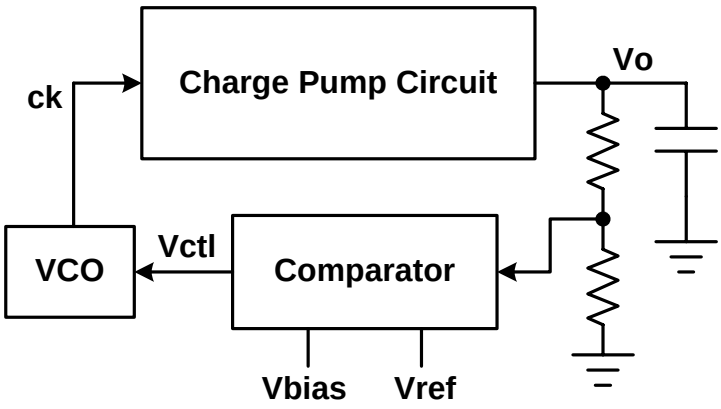


Fig. 5.6 The proposed charge pump circuit with feedback loop.

Chapter 6

Simulation and Measurement

6.1 Proposed Charge Pump Circuit (I)

Due to the inconsideration of layout drawing, the chip of proposed charge pump circuit (I) cannot be operate at higher frequency which we want. So, we decrease the frequency in the new simulation and the measurement. The problem of 4 phases clock generator will be discussed in the chapter 7.2.

The simulation waveforms with 0.18um Mixed Signal SALICIDE (1P6M, 1.8V/3.3V) SPICE model is shown in this section. Fig. 6.1 shows the simulated waveforms of the output voltage when the 833kHz (period=1200ns) clock signal is transmitted to the proposed charge pump circuit (I). With the value of the pumping capacitors are 1nF and the output capacitor is 1 μF, Fig. 6.1(a)-(e) show the output voltage of charge pump circuit (I) at five corners without output loading current. Fig. 6.2(a)-(e) show the output voltage of charge pump circuit (I) at five corners with output loading current 0.5mA.

The measurement setup to test the proposed charge pump circuit (I) is shown in Fig. 6.3. Here, we use 8131A to generate four clock signals into the charge pump circuit directly without using the taper buffer in the chip. In Fig. 6.4(a)-(d) shows the simulated waveforms of the ck1 to ck4 and the node 1-8. In Fig. 6.5(a)-(b) shows the measurements of the ck1 to ck4 and the node 1-8. The measurement of proposed charge pump circuit (I) output voltage with Rout=22kΩ and the clock signal ck1 is

shown in Fig. 6.6(a). In Fig. 6.6(b) and (c), here are Vout-Rout curve and Vout-Iout curve with 833kHz (period=1200ns) clock signal. The Vout-Cpump curve with period=4μs (f=0.25MHz) is shown in Fig. 6.7. The Vout-f curve with Cpump=1nF is shown in Fig. 6.8.

6.2 Proposed Charge Pump Circuit (II)

Due to the inconsideration of layout drawing, the chip of proposed charge pump circuit (II) cannot be operate at higher frequency which we want. So, we decrease the frequency in the new simulation and the measurement. The problem of 4 phases clock generator will be discussed in the chapter 7.2. The simulation waveforms with 0.18um Mixed Signal SALICIDE (1P6M, 1.8V/3.3V) SPICE model is shown in this section. Fig. 6.9 shows the simulated waveforms when the 2.5MHz (period=400ns) clock signal is transmitted to the proposed charge pump circuit (II). With the value of the pumping capacitors are 680pF and the output capacitor is 1 μF, Fig. 6.9(a)-(e) show the output voltage of charge pump circuit (II) at five corners without output loading current. Fig. 6.10(a)-(e) show the output voltage of charge pump circuit (II) at five corners with output loading current 0.8mA.

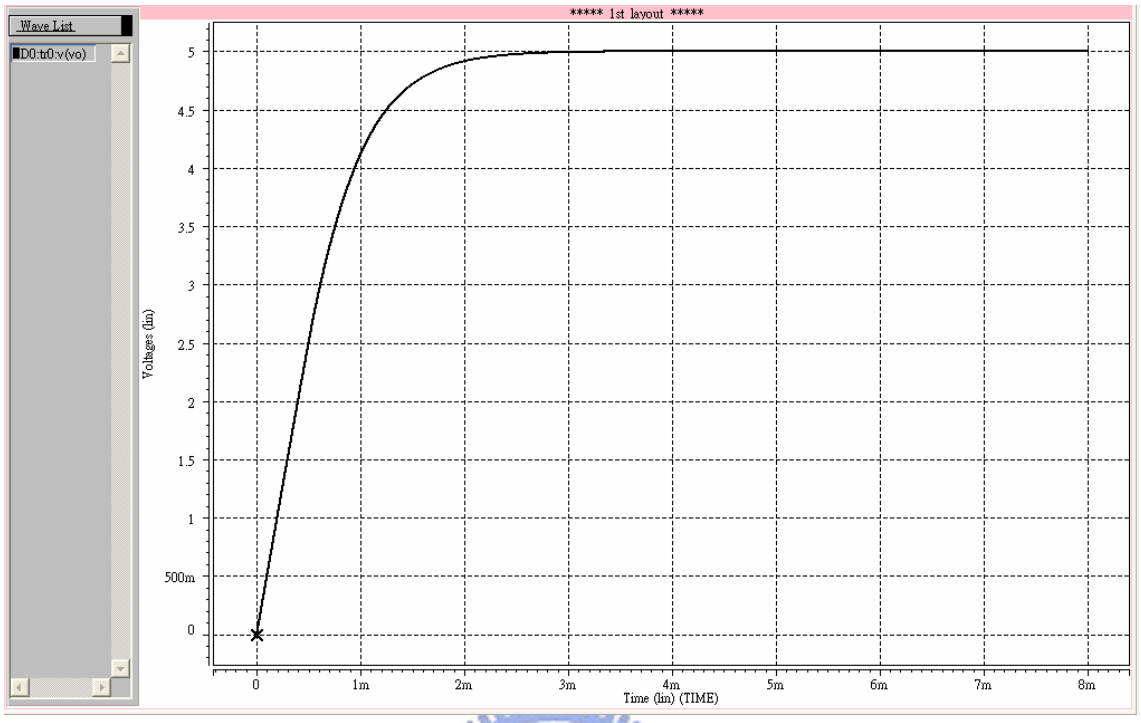
The measurement setup to test the proposed charge pump circuit (II) is shown in Fig. 6.11. Here, we use AWG520 to generate clock signal into the taper buffer in the chip, two clock signals ck1 and ck2 drive four external capacitors in order to make the pump circuit function. The simulated waveforms of the ck, node 1 and node 2 with the 2.5MHz (period=400ns) clock signal are shown in Fig. 6.12. In Fig. 6.13(a)-(b) shows the measurements of the ck1, ck2, ck, Vout and the node 1-2 at 2.5MHz (period=400ns) for example. We can find the difference obviously between the

simulated waveforms and the measurements. This problem of the difference will also be discussed in the next chapter 7.1.

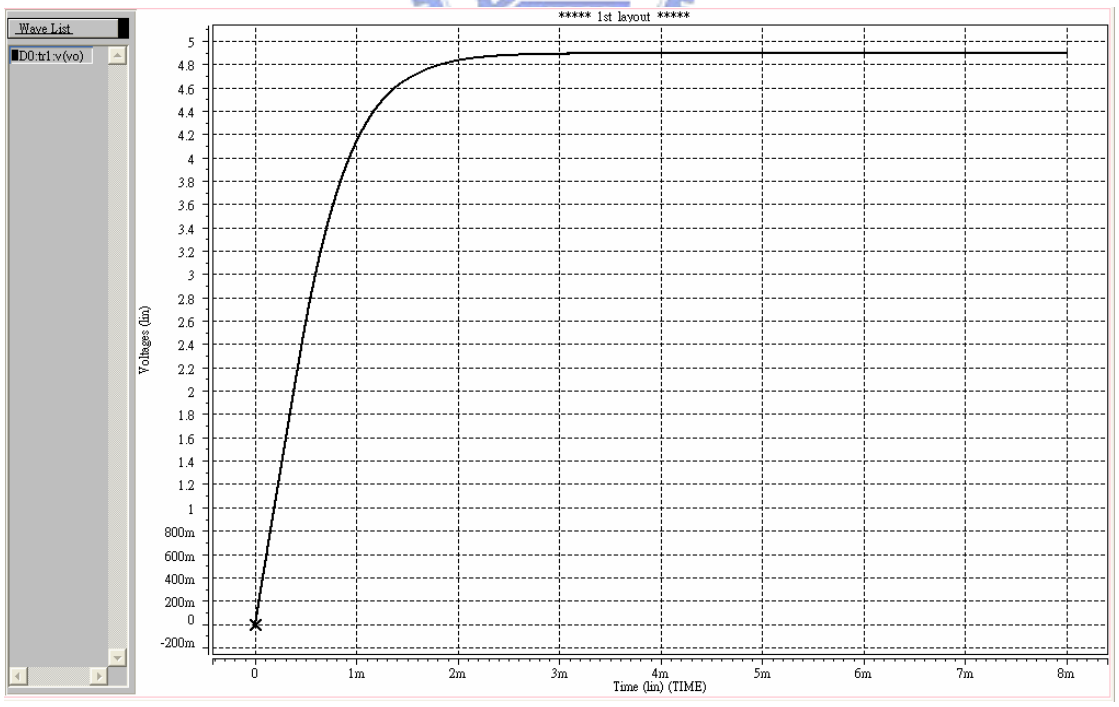
The measurement of proposed charge pump circuit (II) output voltage with Rout=68kΩ and the clock signal ck is shown in Fig. 6.14(a). In Fig. 6.14 (b) and (c), here are Vout-Rout curve and Vout-Iout curve. The Vout-Cpump curve with f=1MHz. is shown in Fig. 6.15. The Vout-f curve with Cpump=680pF is shown in Fig. 6.16.

6.3 Proposed Charge Pump Circuit (II) with Feedback Loop

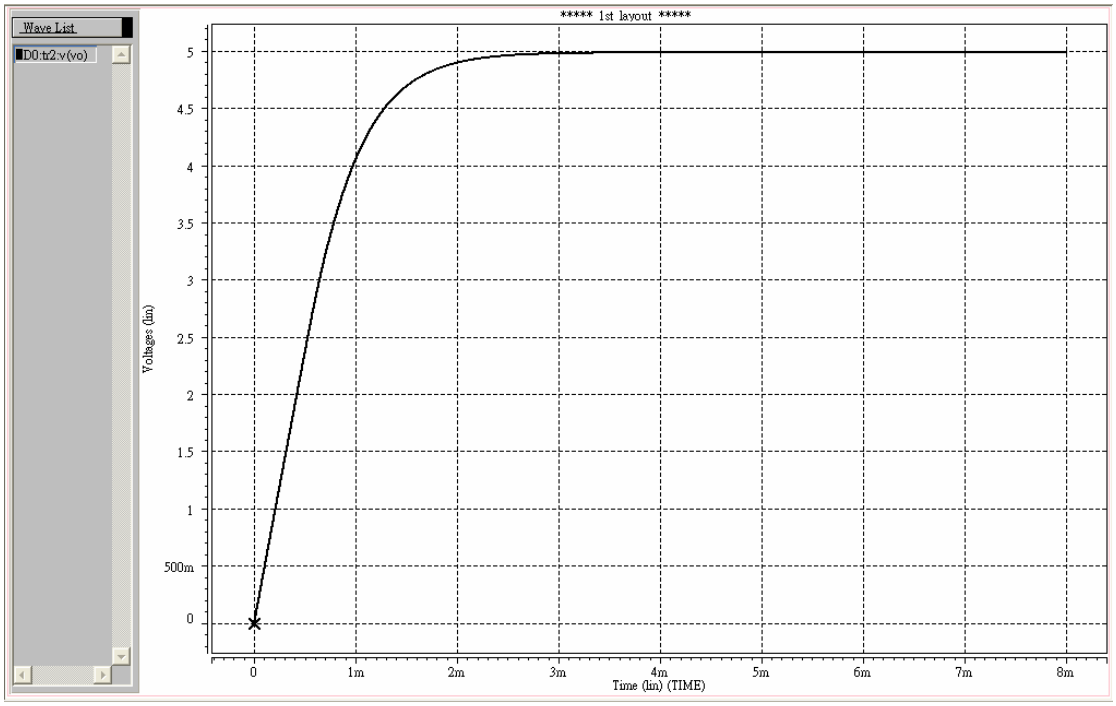
The simulation waveforms with 0.18um Mixed Signal SALICIDE (1P6M, 1.8V/3.3V) SPICE model is shown in this section. The proposed charge pump circuit with feedback loop is shown in Fig. 5.6, where the Cpump=680pF and f=7MHz (at Vctl is LOW) or 25MHz (at Vctl is HIGH), Vref=1.25V, Vbias=0.7V. In Fig. 6.17, the simulation waveforms show Vout and Vctl curves in the five corners with Cpump=680pF and f=7 or 25MHz. In Fig. 6.18(a) and (b), there are the measurement setup to test the proposed charge pump circuit (II) with feedback loop and the measurement of ck1 (Ch1) and Vout (Ch2) curves with Cpump=680pF and f=7 or 25MHz. The Vout-Rout curve with Cpump=680pF and f=7 or 25MHz is shown in Fig. 6.19. The Vout-Iout curve with Cpump=680pF and f=7 or 25MHz is shown in Fig. 6.20.


Wave List
D0:tr0:v(vo)
***** 1st layout *****
Voltages (lin)
Time (lin) (TIME)
0
500m
1
1.5
2
2.5
3
3.5
4
4.5
5
1m
2m
3m
4m
5m
6m
7m
8m

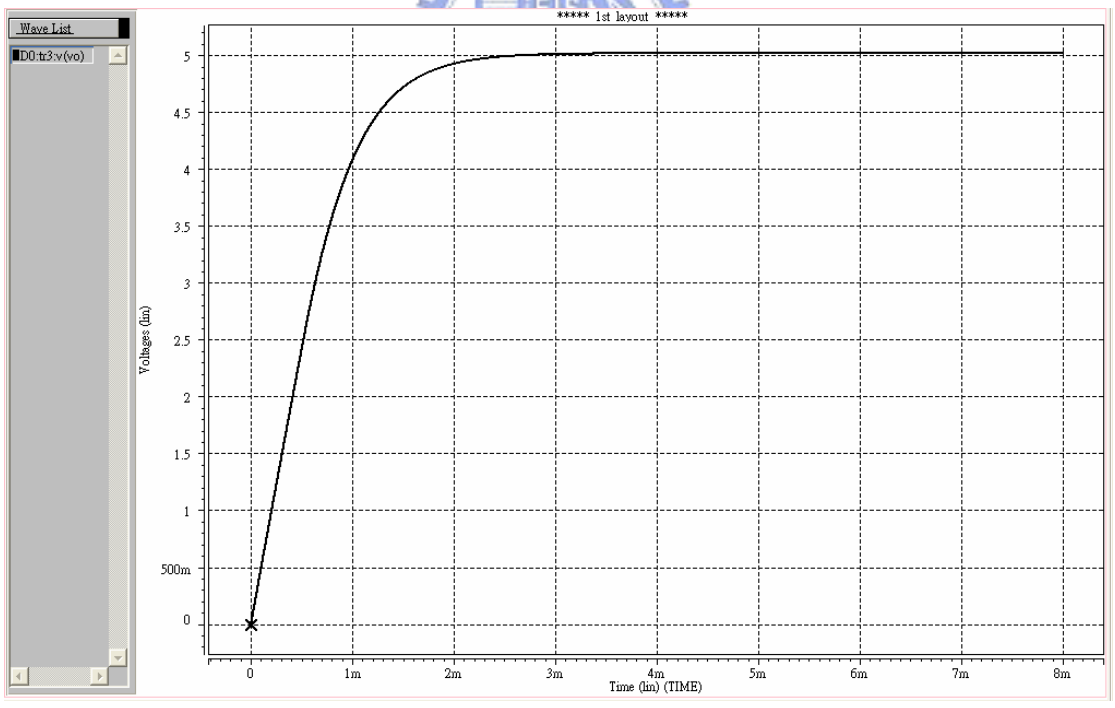
(a)


Wave List
D0:tr1:v(vo)
***** 1st layout *****
Voltages (lin)
Time (lin) (TIME)
-200m
0
200m
400m
600m
800m
1
1.2
1.4
1.6
1.8
2
2.2
2.4
2.6
2.8
3
3.2
3.4
3.6
3.8
4
4.2
4.4
4.6
4.8
5
1m
2m
3m
4m
5m
6m
7m
8m

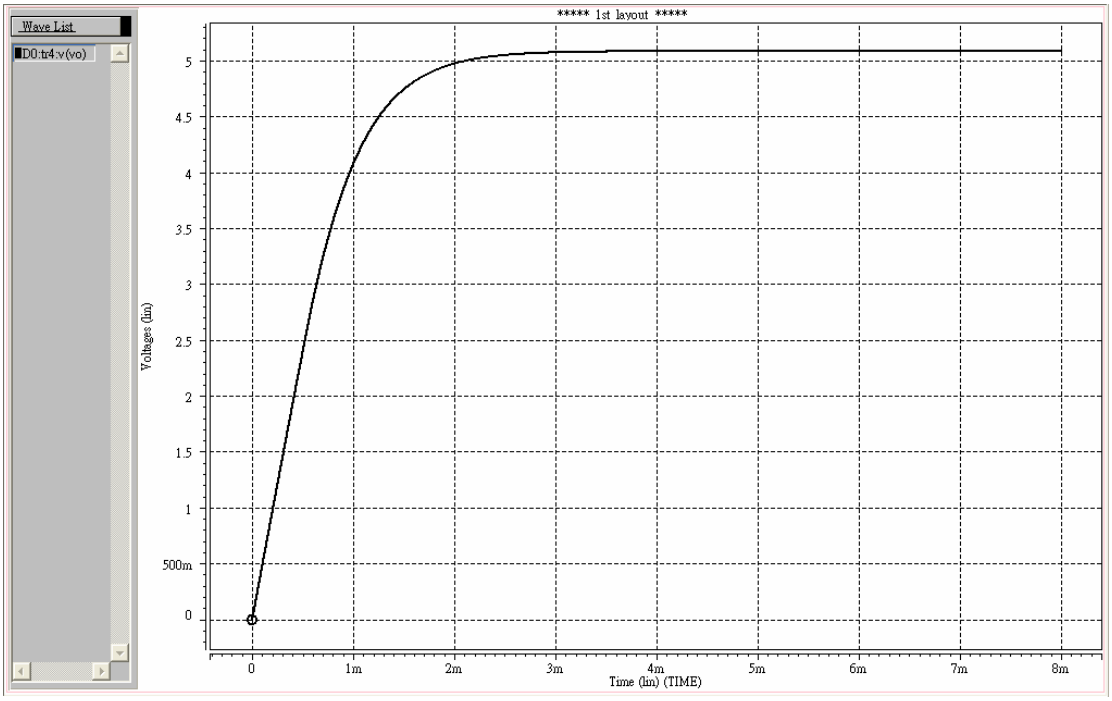
(b)


Wave List
D0:tr2:v(vo)
***** 1st layout *****
Voltages (lin)
5
4.5
4
3.5
3
2.5
2
1.5
1
500m
0
0
1m
2m
3m
4m
5m
6m
7m
8m
Time (lin) (TIME)

(c)

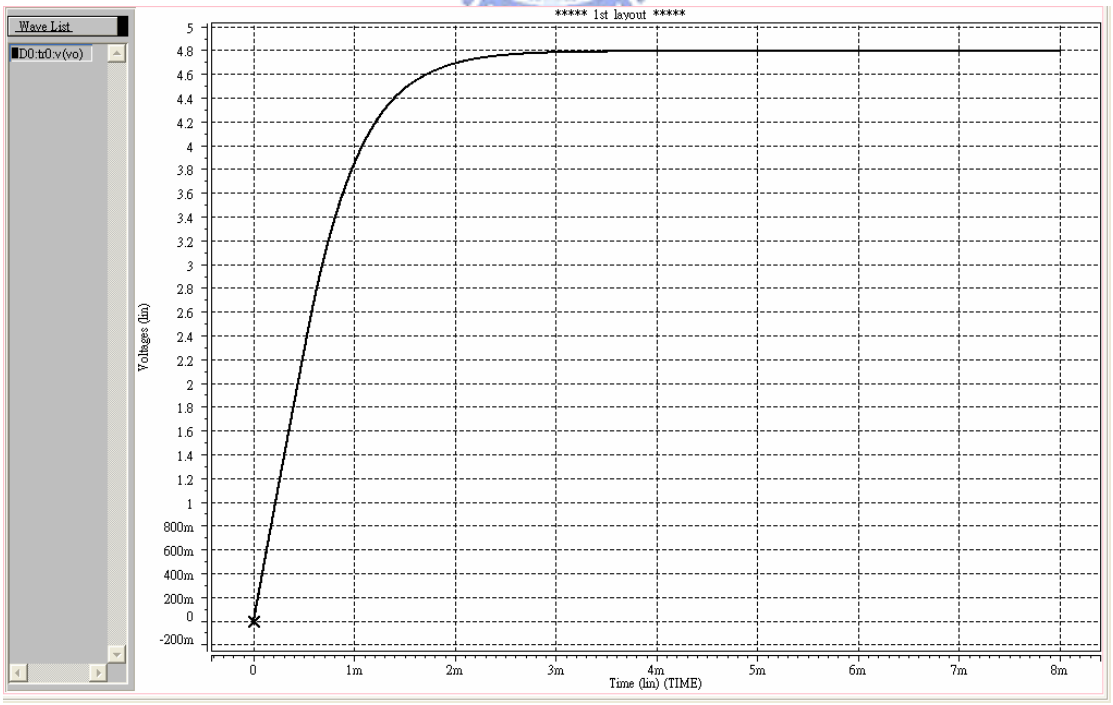

Wave List
D0:tr3:v(vo)
***** 1st layout *****
Voltages (lin)
5
4.5
4
3.5
3
2.5
2
1.5
1
500m
0
0
1m
2m
3m
4m
5m
6m
7m
8m
Time (lin) (TIME)

(d)

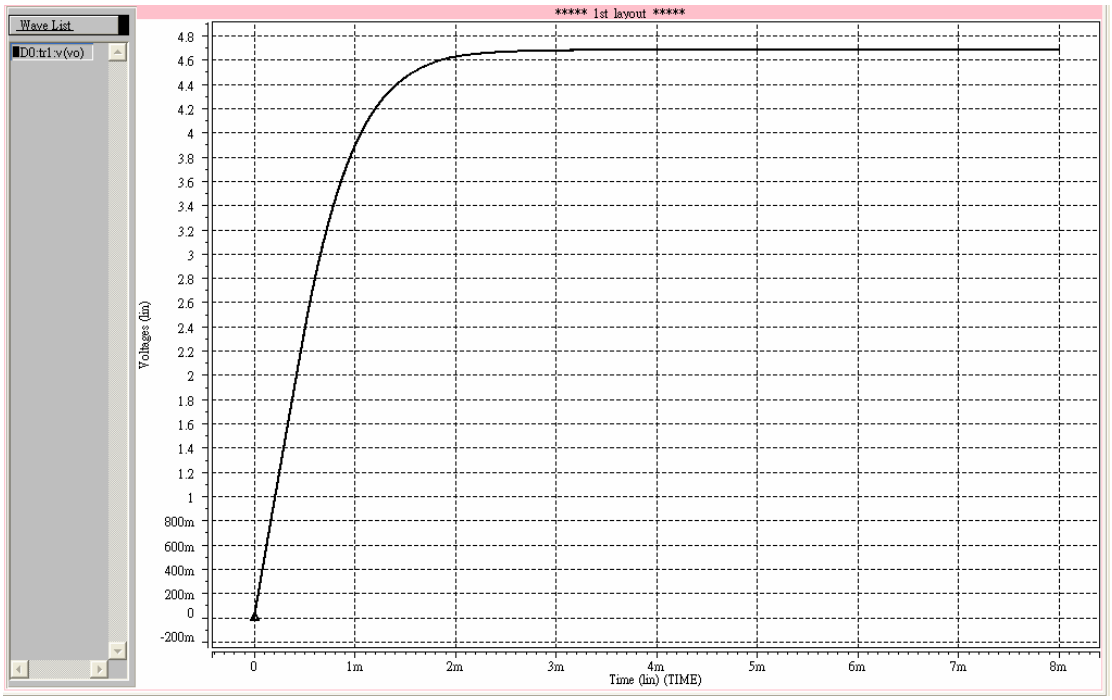


(e)

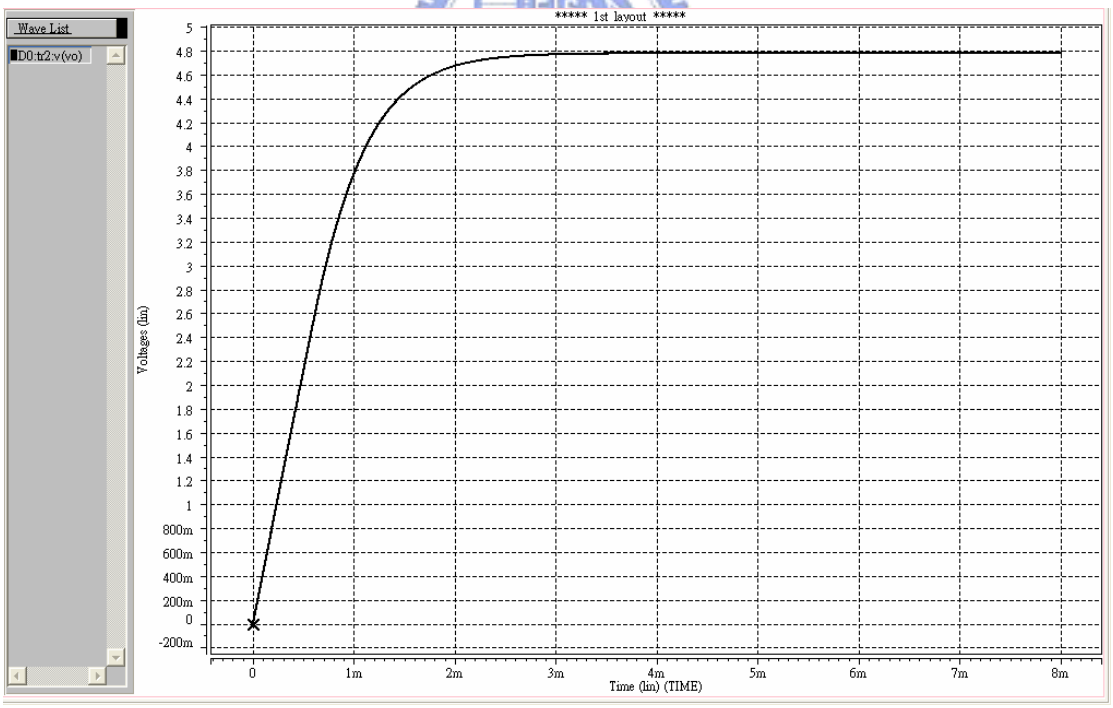
Fig. 6.1 The output voltage of charge pump circuit (I) at (a) TT corner, (b) FF corner, (c) FS corner, (d) SF corner and (e) SS corner, without output loading current with f=833kHz (period=1200ns).



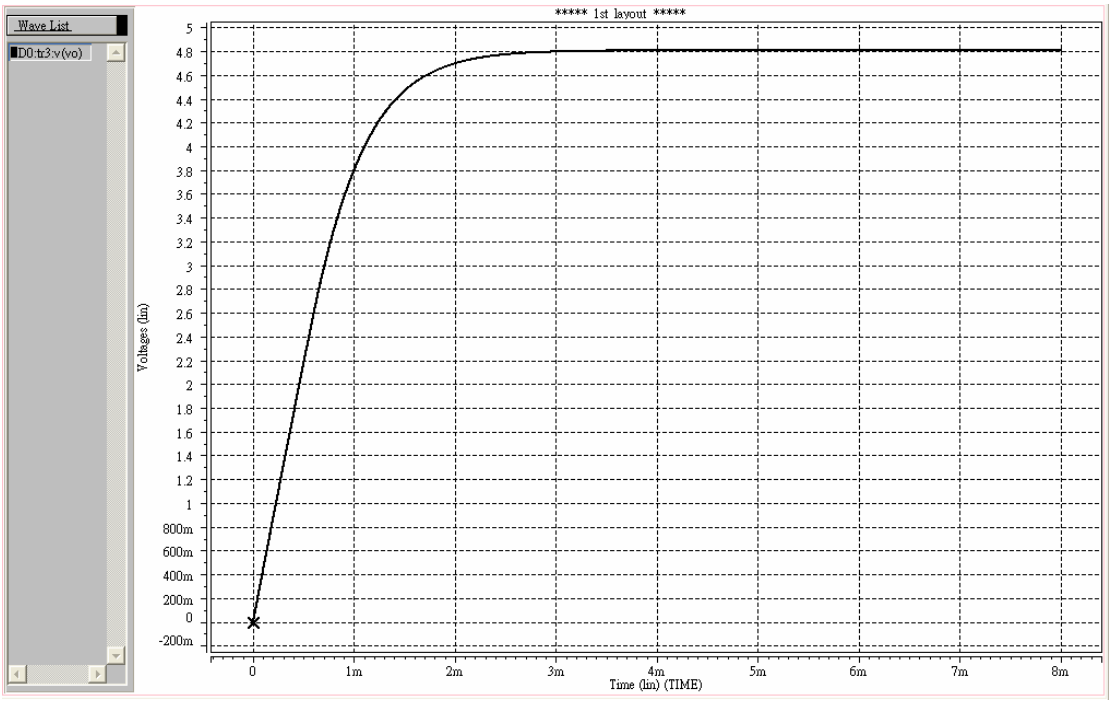
(a)


Wave List
D0:tr1:v(vo)
***** 1st layout *****
Voltages (lin)
Time (lin) (TIME)

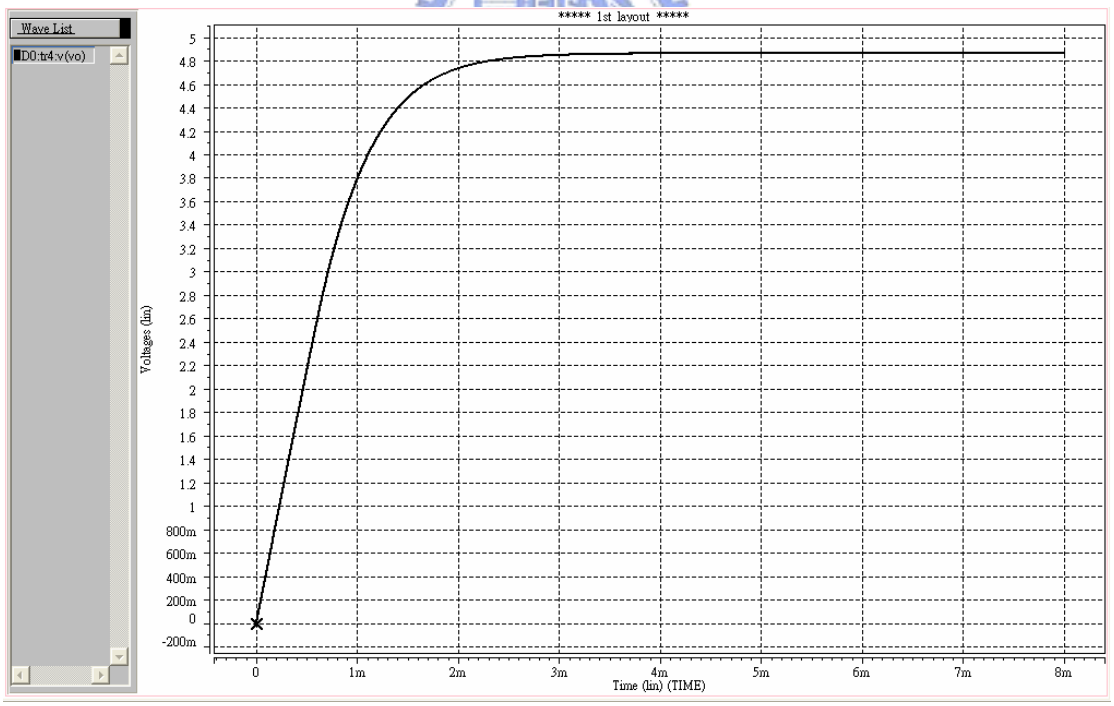
(b)


Wave List
D0:tr2:v(vo)
***** 1st layout *****
Voltages (lin)
Time (lin) (TIME)

(c)



(d)



(e)

Fig. 6.2 The output voltage of charge pump circuit (I) at (a) TT corner, (b) FF corner, (c) FS corner, (d) SF corner and (e) SS corner, with the output loading current 0.5mA.

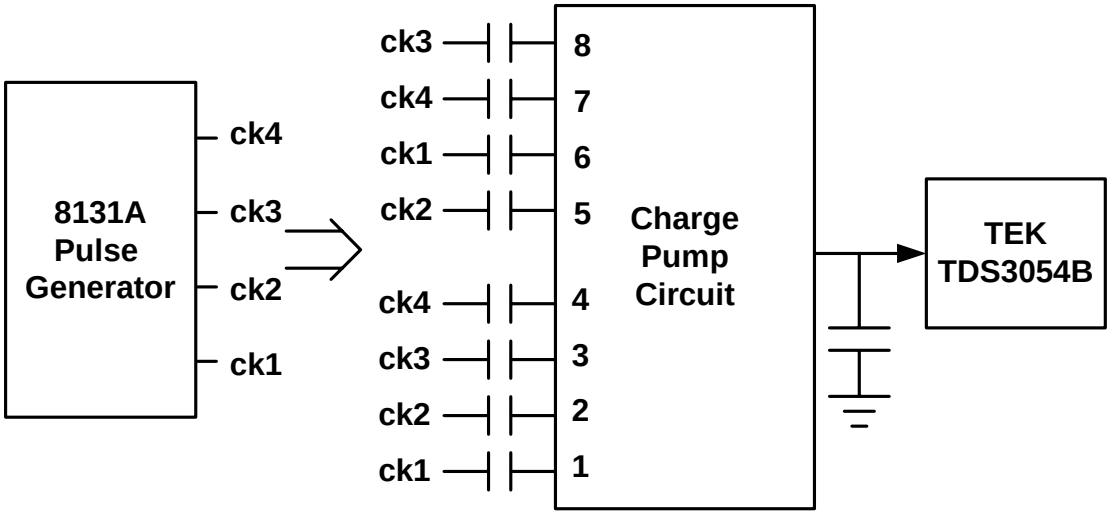
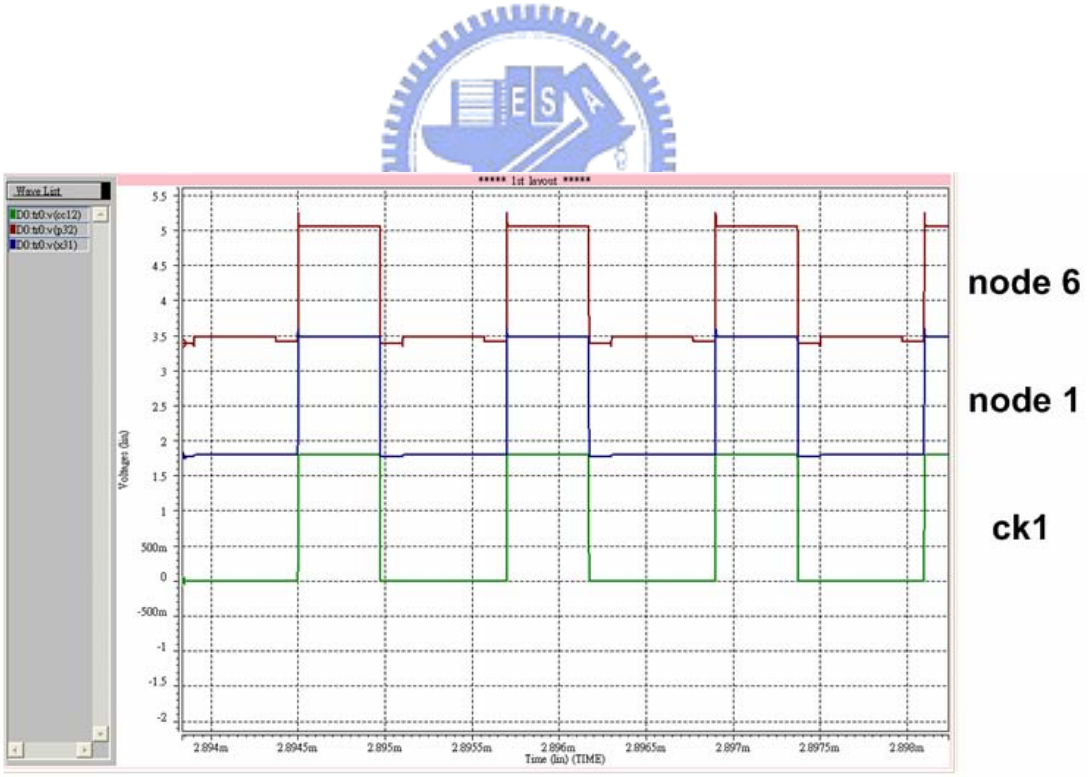
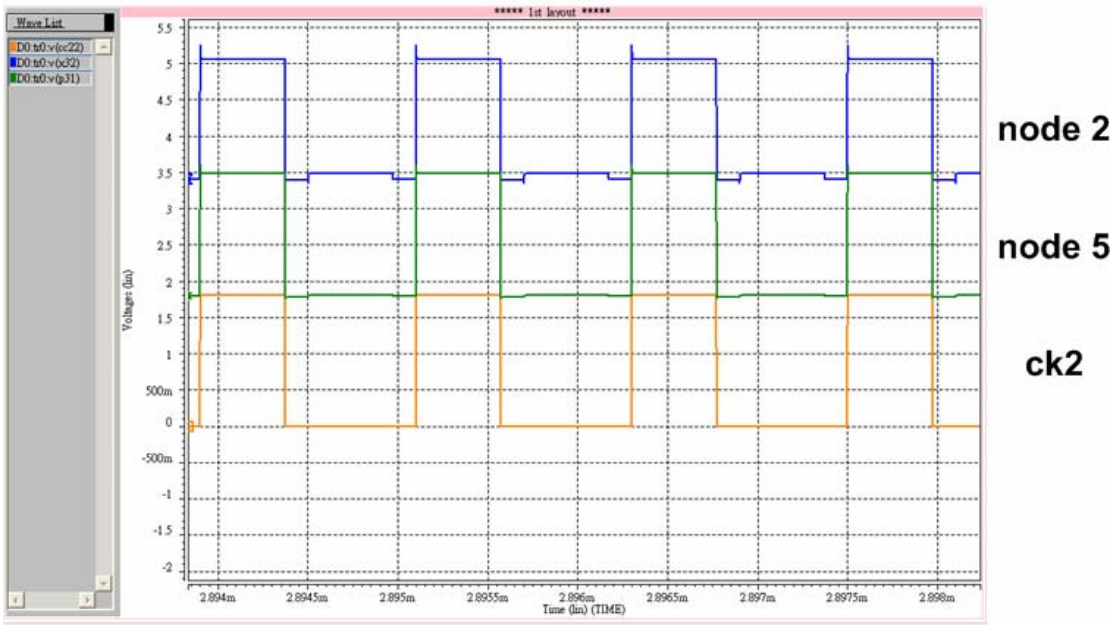


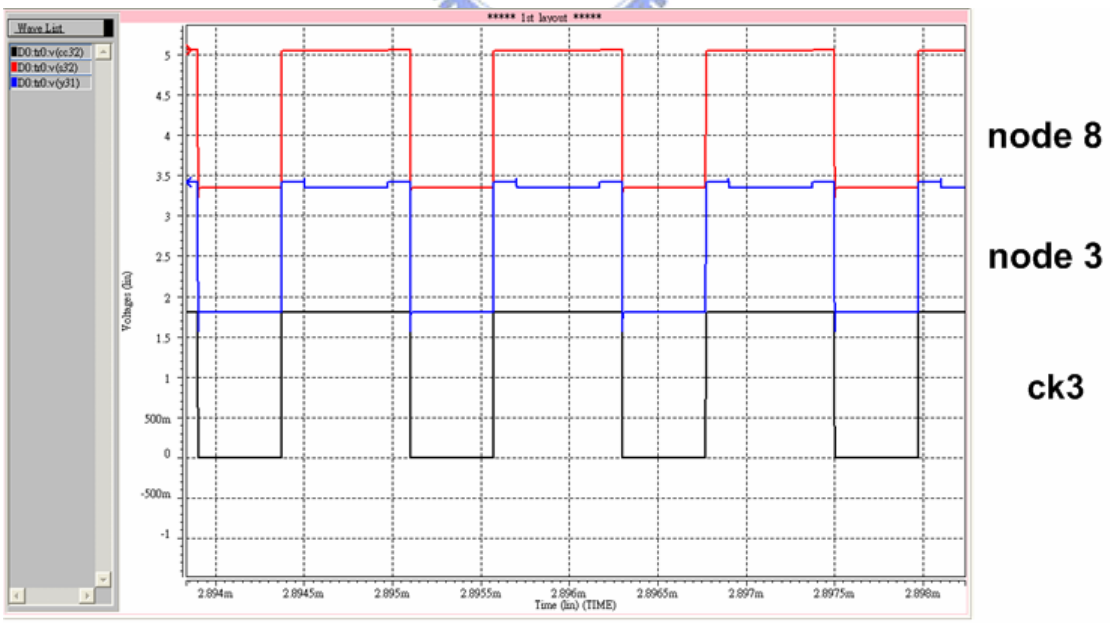
Fig. 6.3 The measurement setup to test the proposed charge pump circuit (I).



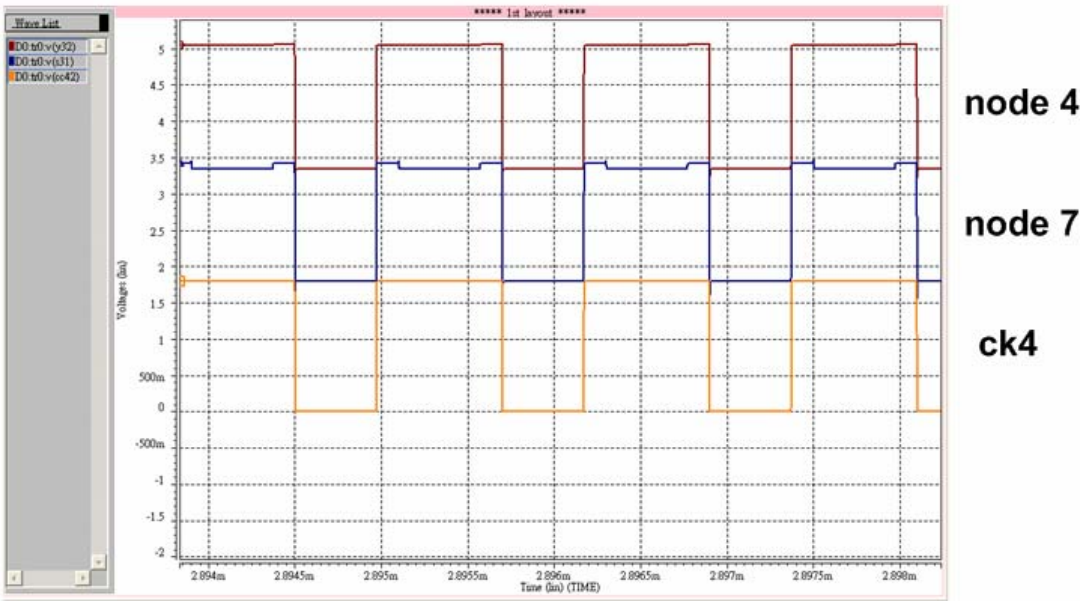
(a)


Wave List
D0:tr0:v(cc22)
D0:tr0:v(x32)
D0:tr0:v(y31)
***** 1st layout *****
Voltages (lin)
Time (lin) (TIME)
node 2
node 5
ck2

(b)

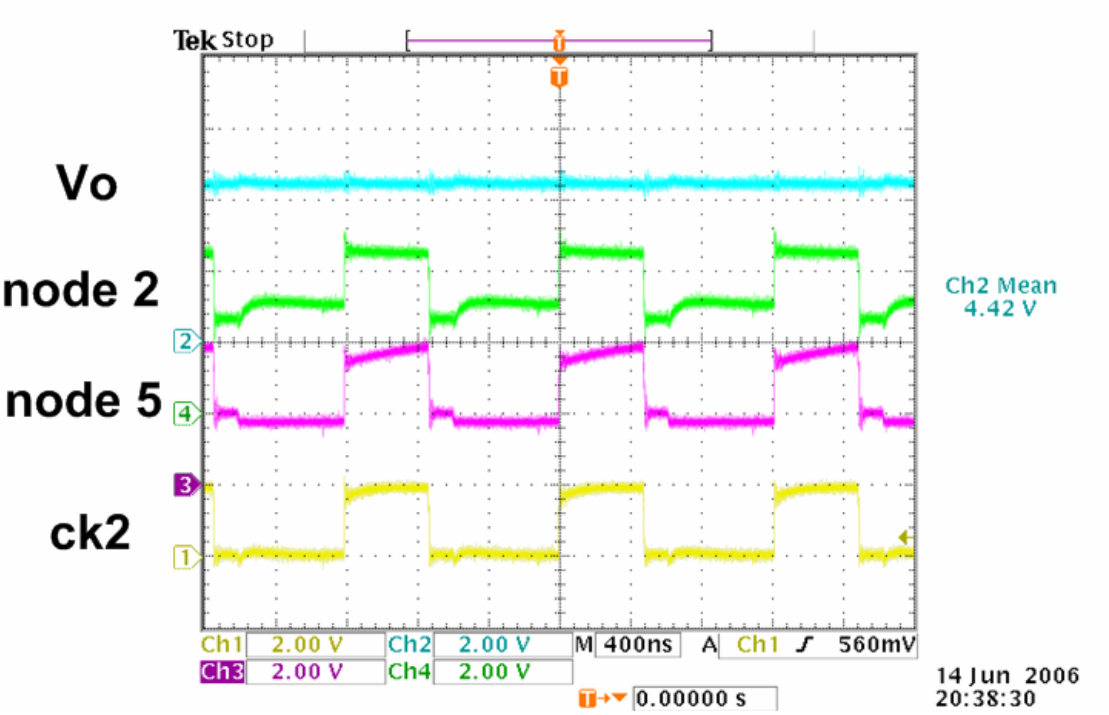

Wave List
D0:tr0:v(cc32)
D0:tr0:v(x32)
D0:tr0:v(y31)
***** 1st layout *****
Voltages (lin)
Time (lin) (TIME)
node 8
node 3
ck3

(c)

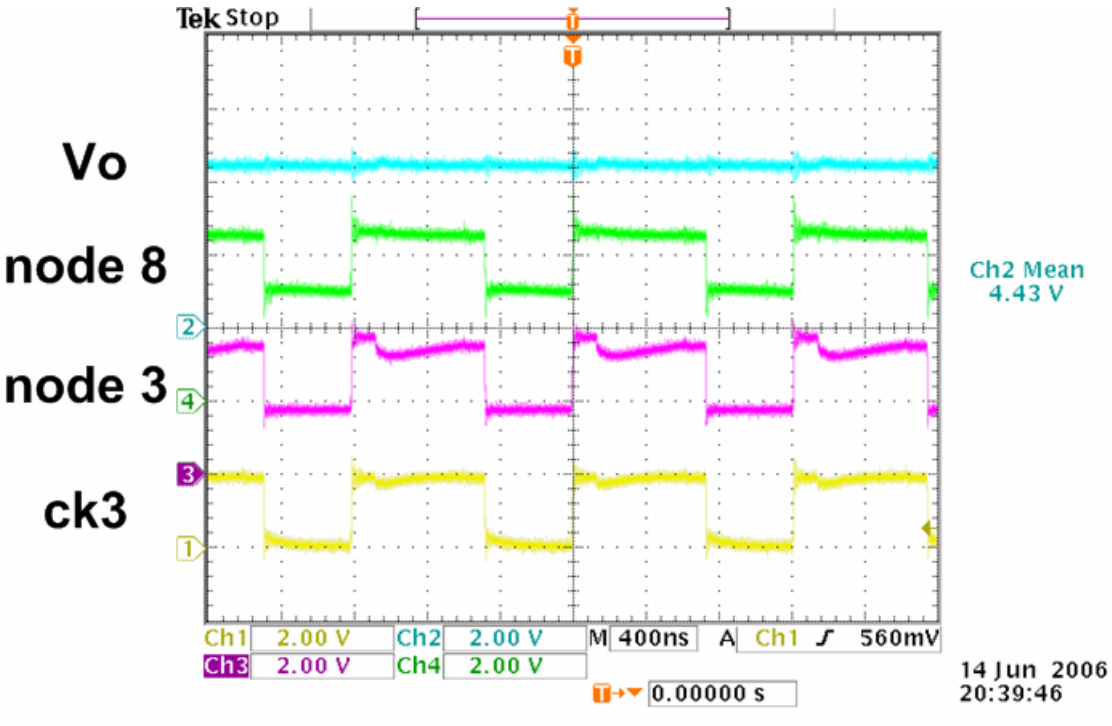


(d)

Fig. 6.4 The simulated waveforms of the (a) ck1, node 1, node 6, (b) ck2, node 2, node 5 (c) ck3, node 3, node 8 and (d) ck4, node 4, node 7 with f=833kHz (period=1200ns).

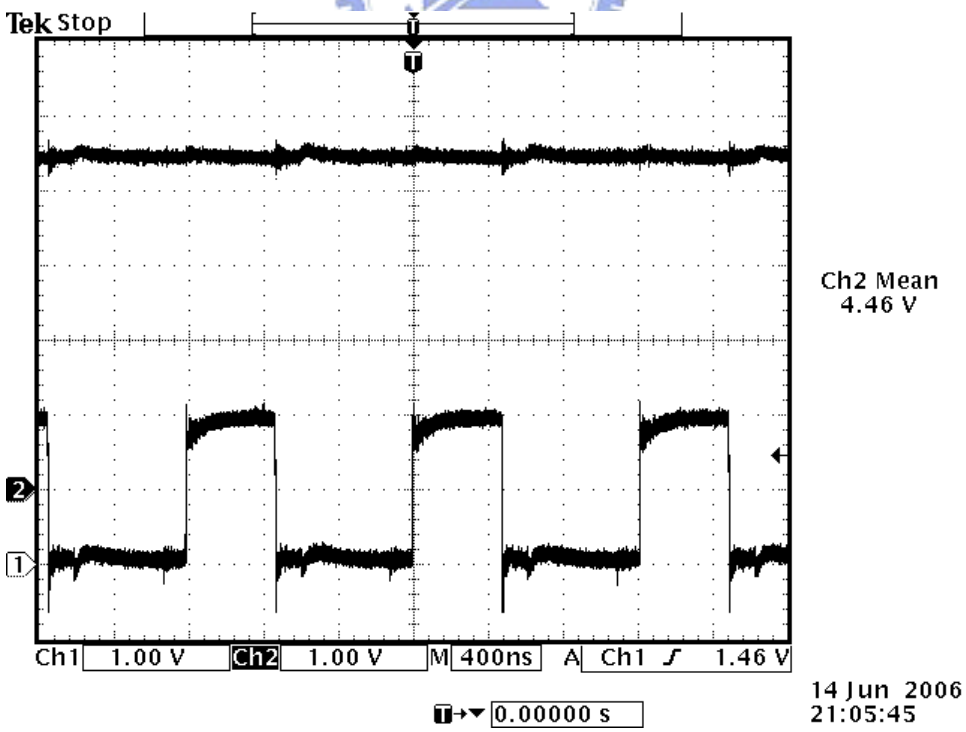


(a)

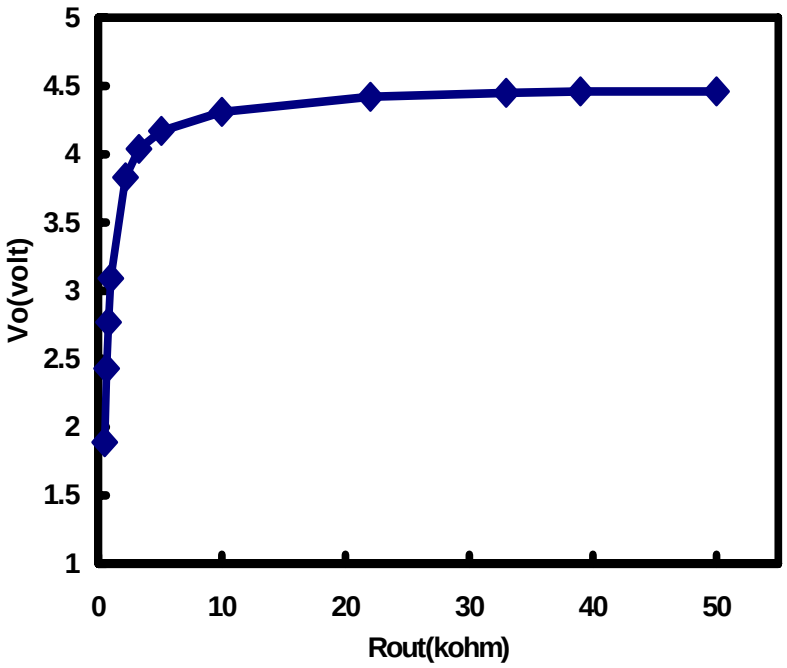


(b)

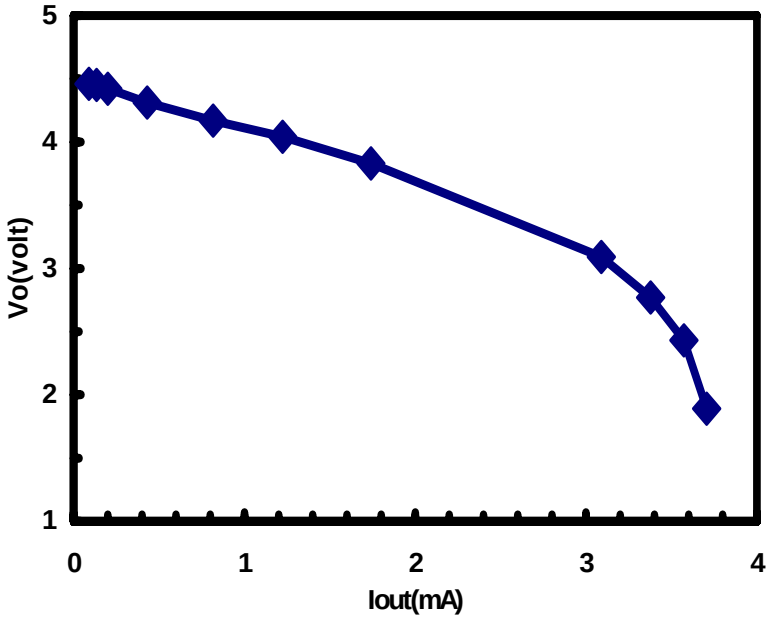
Fig. 6.5 The measurements of the (a) ck2, node 2, node 5 and (b) ck3, node 3, node 8.



(a)



(b)



(c)

Fig. 6.6 (a) The measurement of proposed charge pump circuit (I) output voltage with Rout=22kΩ and the clock signal ck1. (b) Vout-Rout curve. (c) Vout-Iout curve.

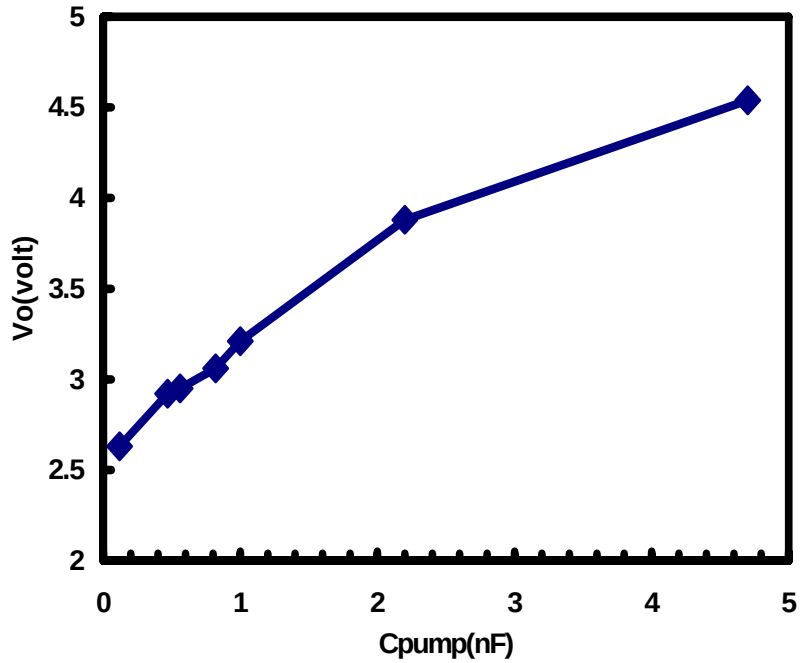


Fig. 6.7 The Vout-Cpump curve with period=4 μ s (f=0.25MHz).

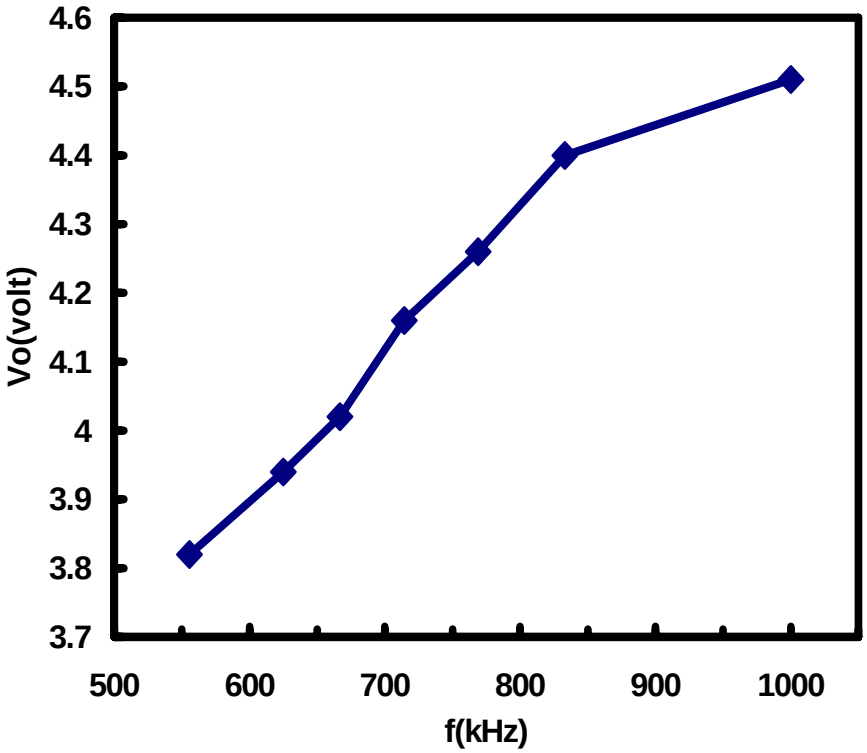
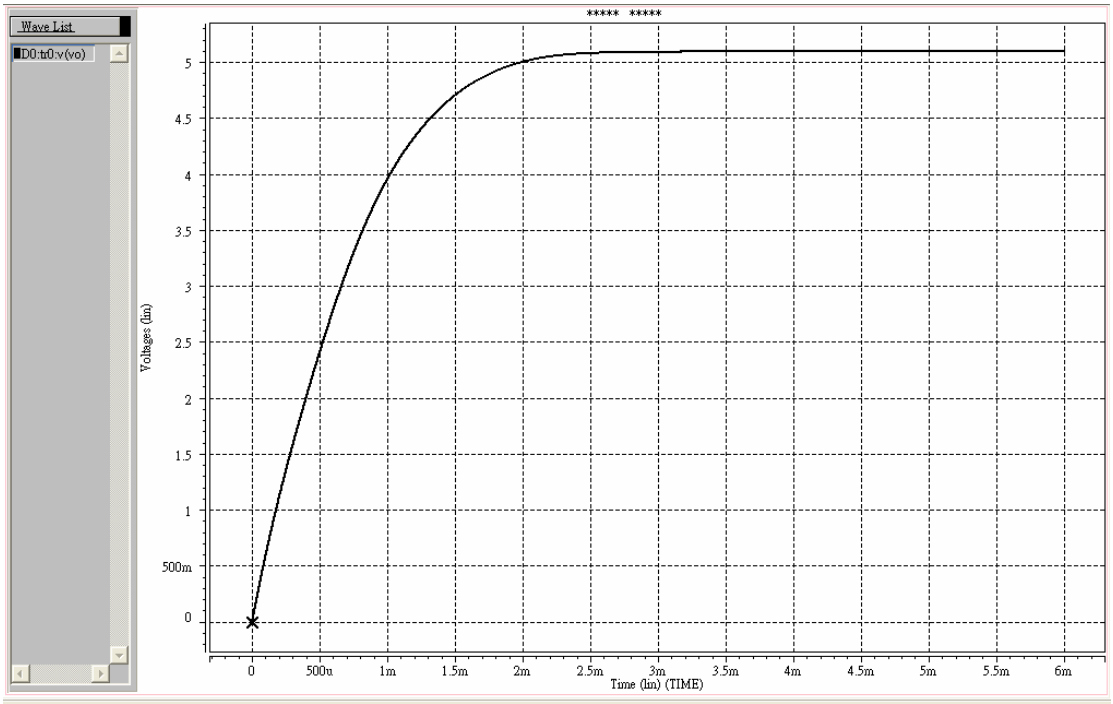
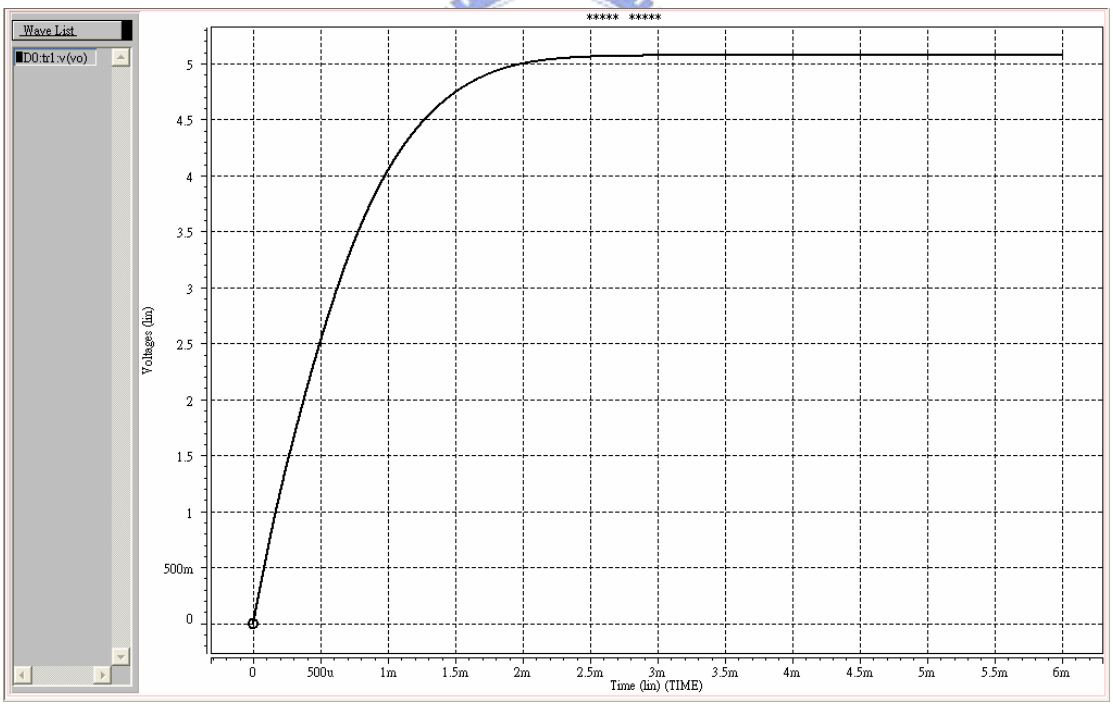


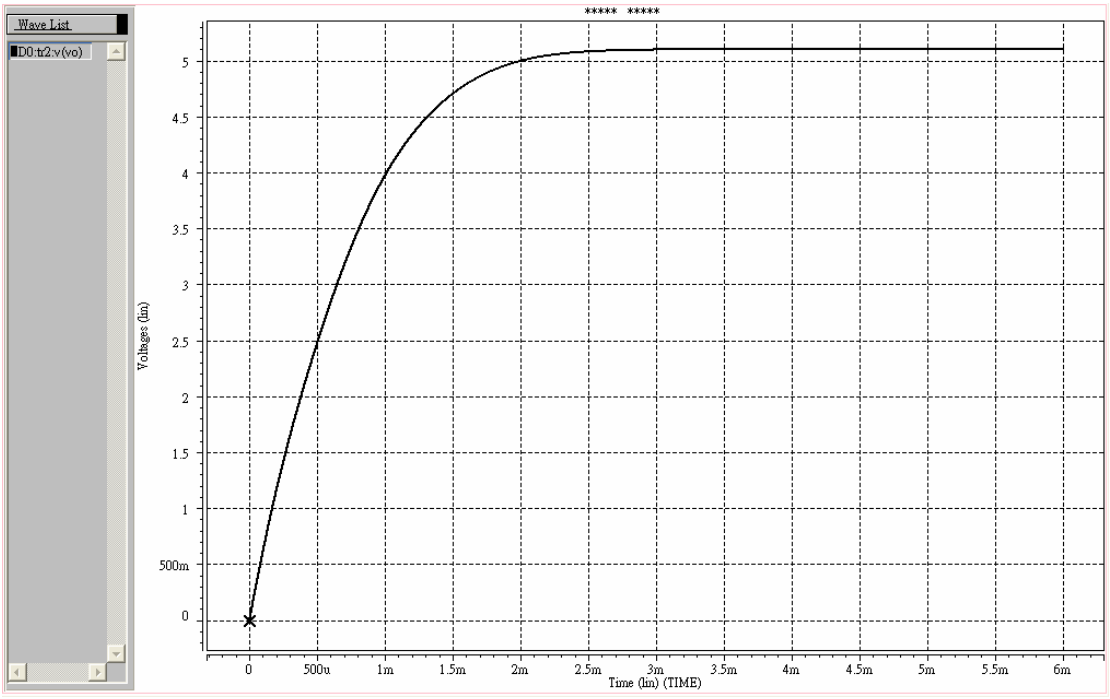
Fig. 6.8 The Vout-f curve with Cpump=1nF.


Wave List
D0:tr0:v(vo)
***** *****
Voltages (lin)
Time (lin) (TIME)
0
500u
1m
1.5m
2m
2.5m
3m
3.5m
4m
4.5m
5m
5.5m
6m
500m

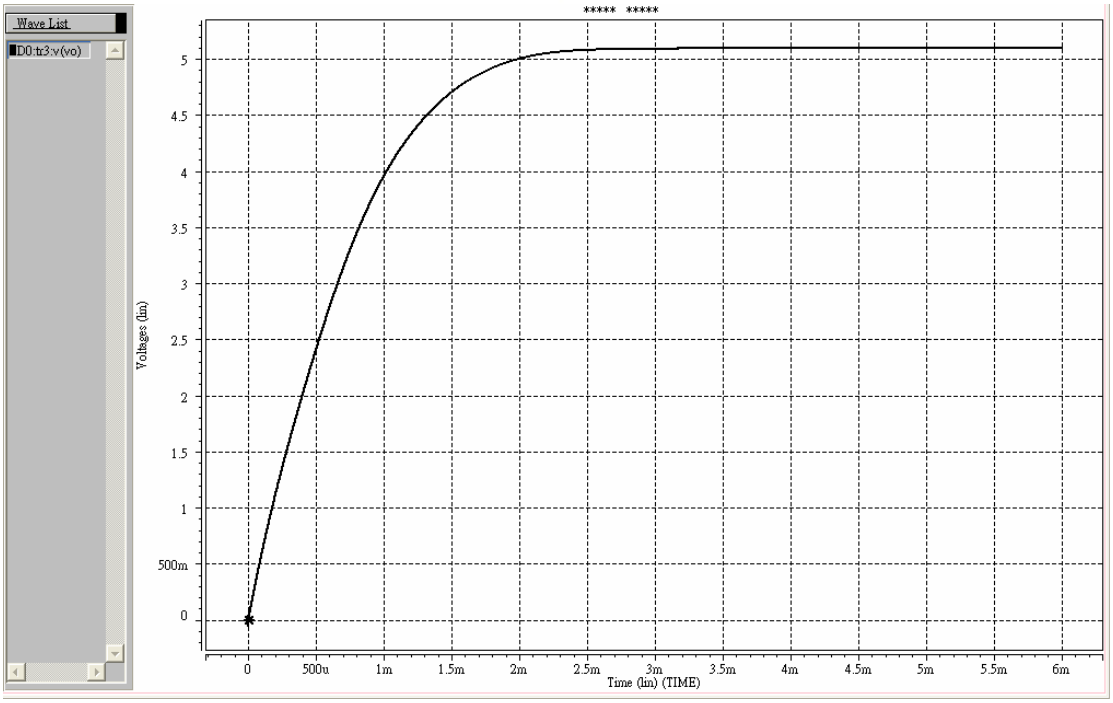
(a)


Wave List
D0:tr1:v(vo)
***** *****
Voltages (lin)
Time (lin) (TIME)
0
500u
1m
1.5m
2m
2.5m
3m
3.5m
4m
4.5m
5m
5.5m
6m
500m

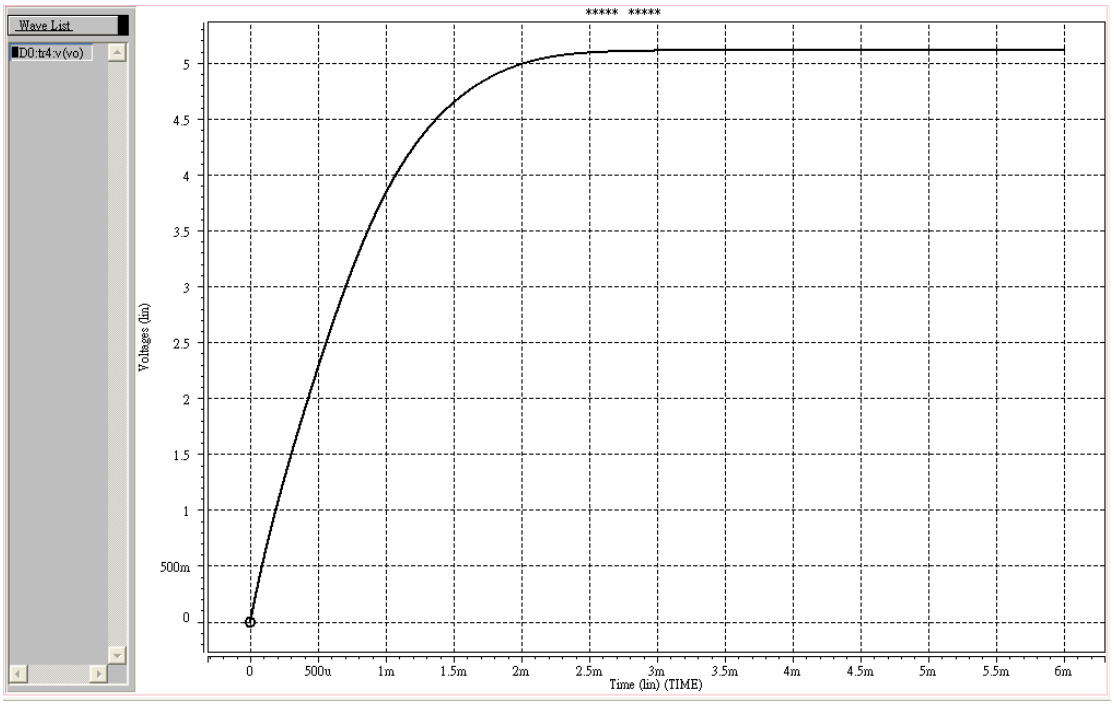
(b)


Wave List
D0:tr2:v(vo)
***** *****
Voltages (lin)
Time (lin) (TIME)
0
500u
1m
1.5m
2m
2.5m
3m
3.5m
4m
4.5m
5m
5.5m
6m
500m
1
2
3
4
5

(c)

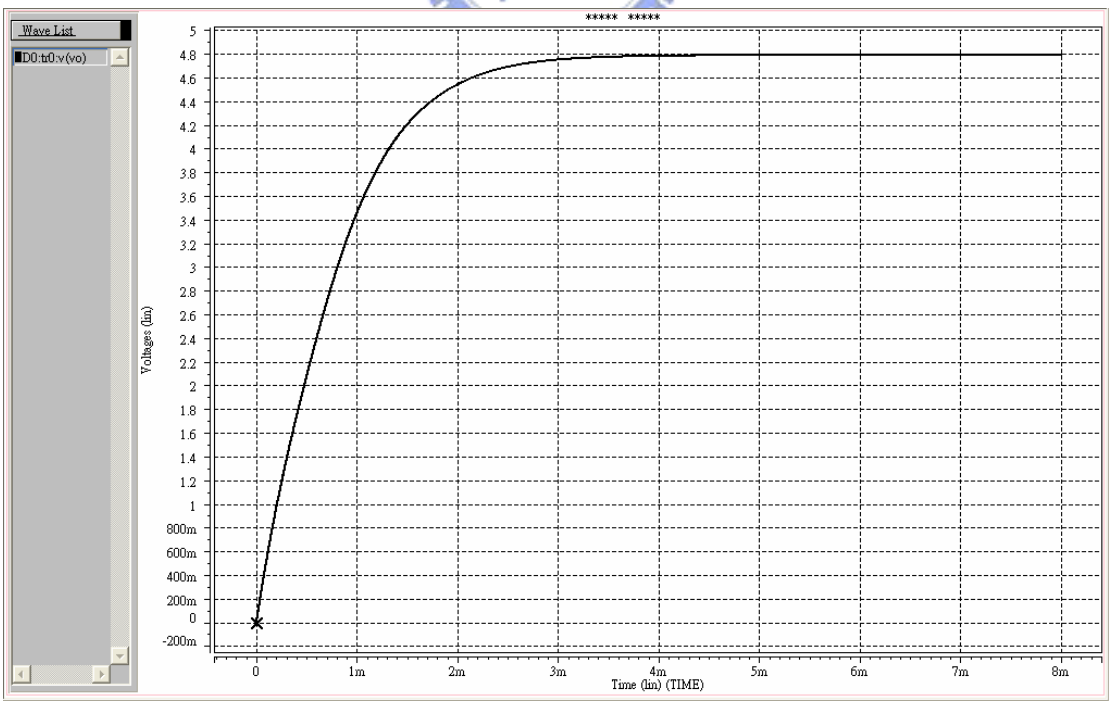

Wave List
D0:tr3:v(vo)
***** *****
Voltages (lin)
Time (lin) (TIME)
0
500u
1m
1.5m
2m
2.5m
3m
3.5m
4m
4.5m
5m
5.5m
6m
500m
1
2
3
4
5

(d)

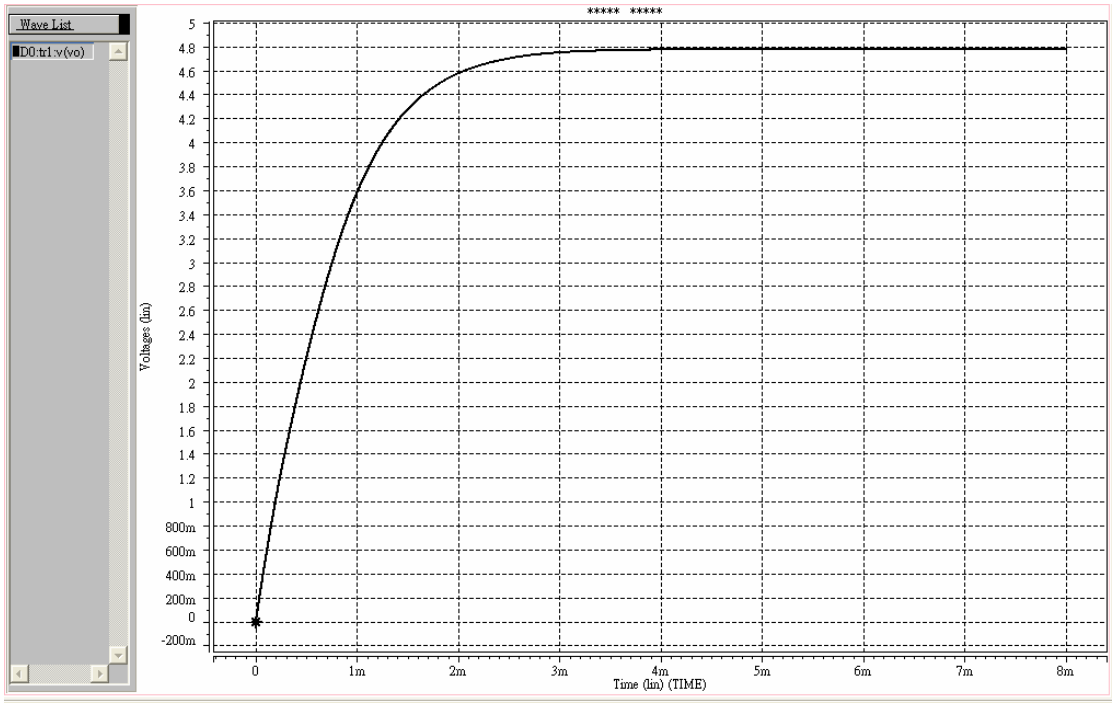


(e)

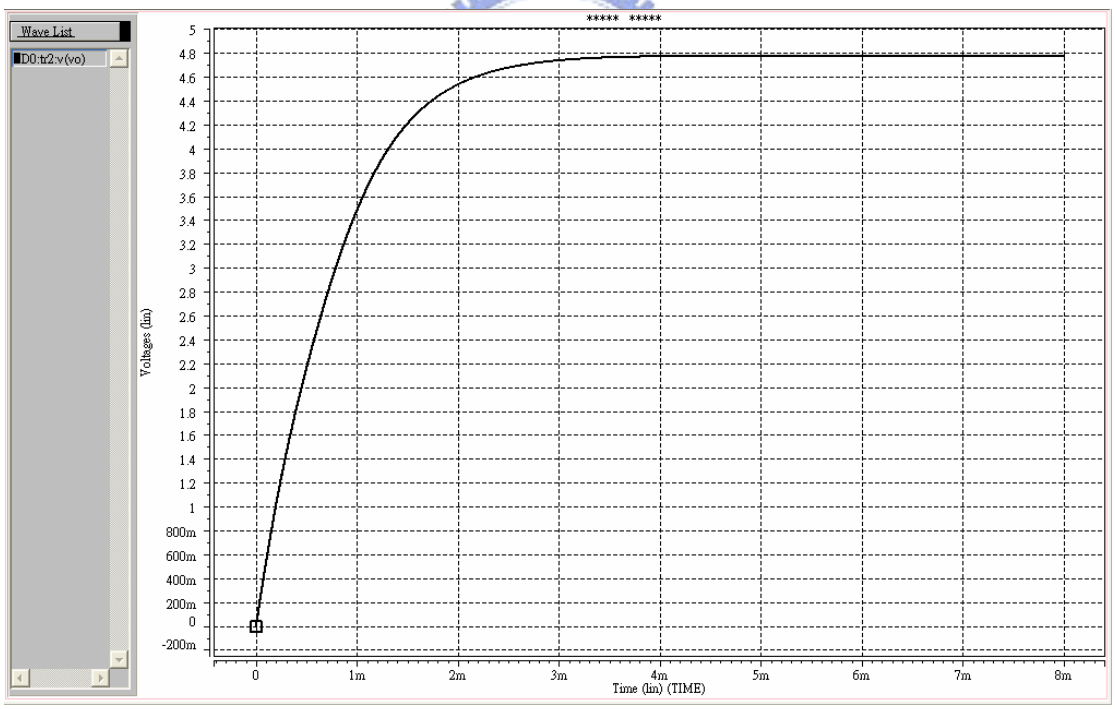
Fig. 6.9 The output voltage of charge pump circuit (II) at (a) TT corner, (b) FF corner, (c) FS corner, (d) SF corner and (e) SS corner, without output loading current with f=2.5MHz (period=400ns).



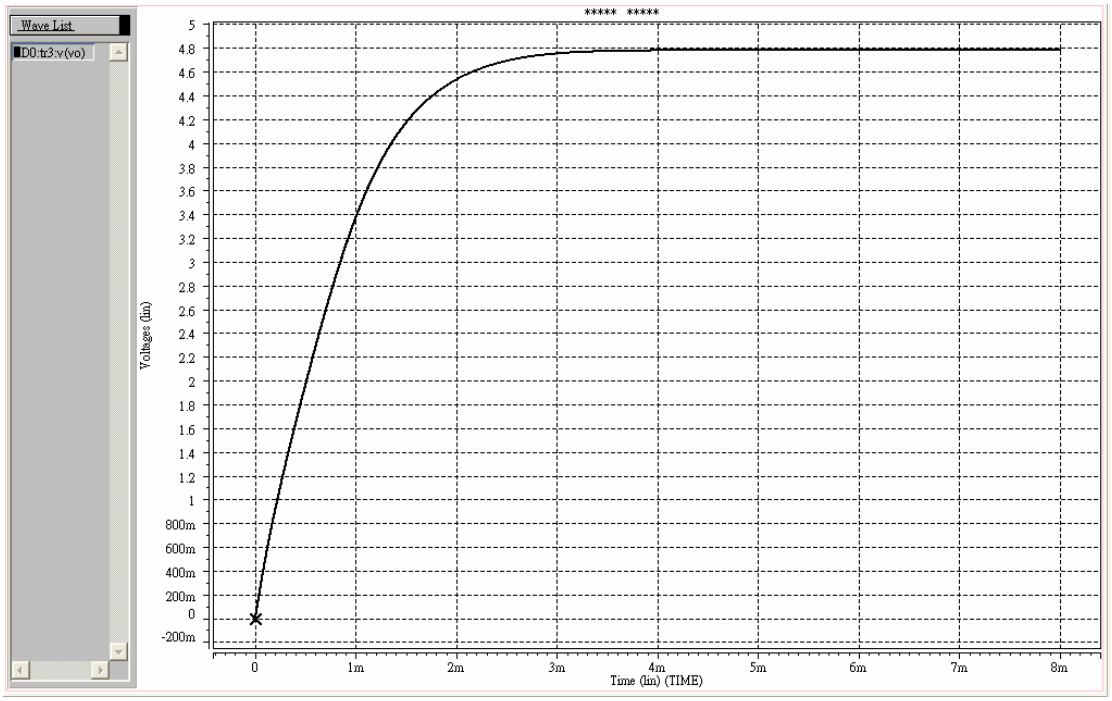
(a)


Wave List
D0:tr1:v(vo)
***** *****
Voltages (lin)
Time (lin) (TIME)

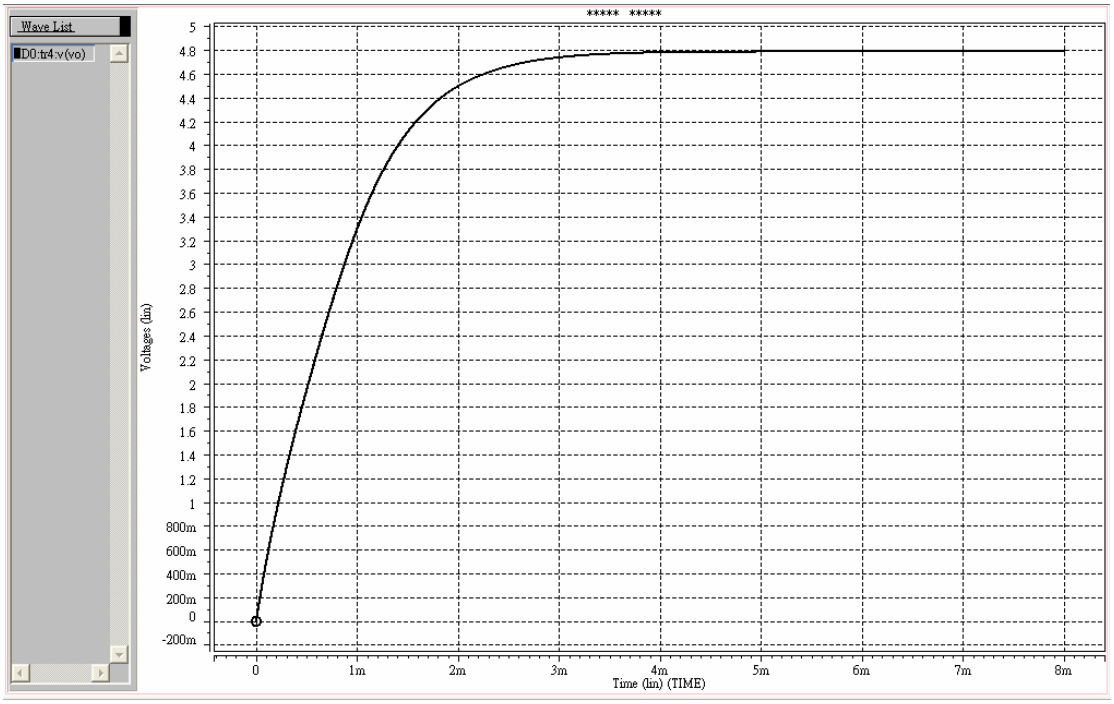
(b)


Wave List
D0:tr2:v(vo)
***** *****
Voltages (lin)
Time (lin) (TIME)

(c)



(d)



(e)

Fig. 6.10 The output voltage of charge pump circuit (II) at (a) TT corner, (b) FF corner, (c) FS corner, (d) SF corner and (e) SS corner, with the output loading current 0.8mA.

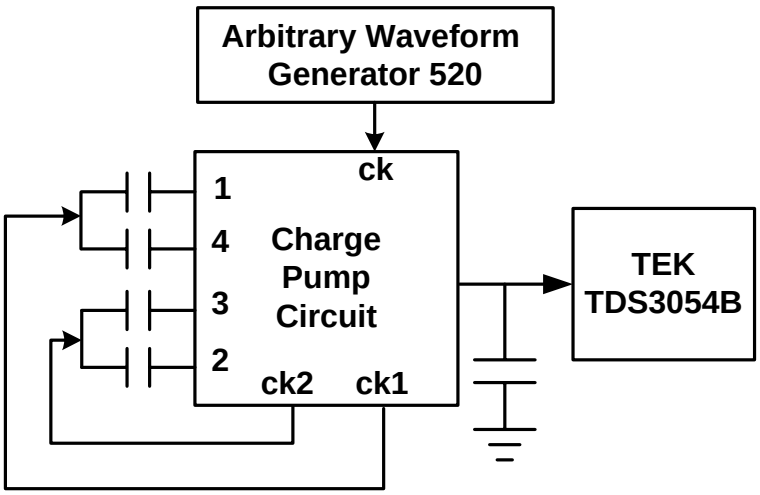


Fig. 6.11 The measurement setup to test the proposed charge pump circuit (II).

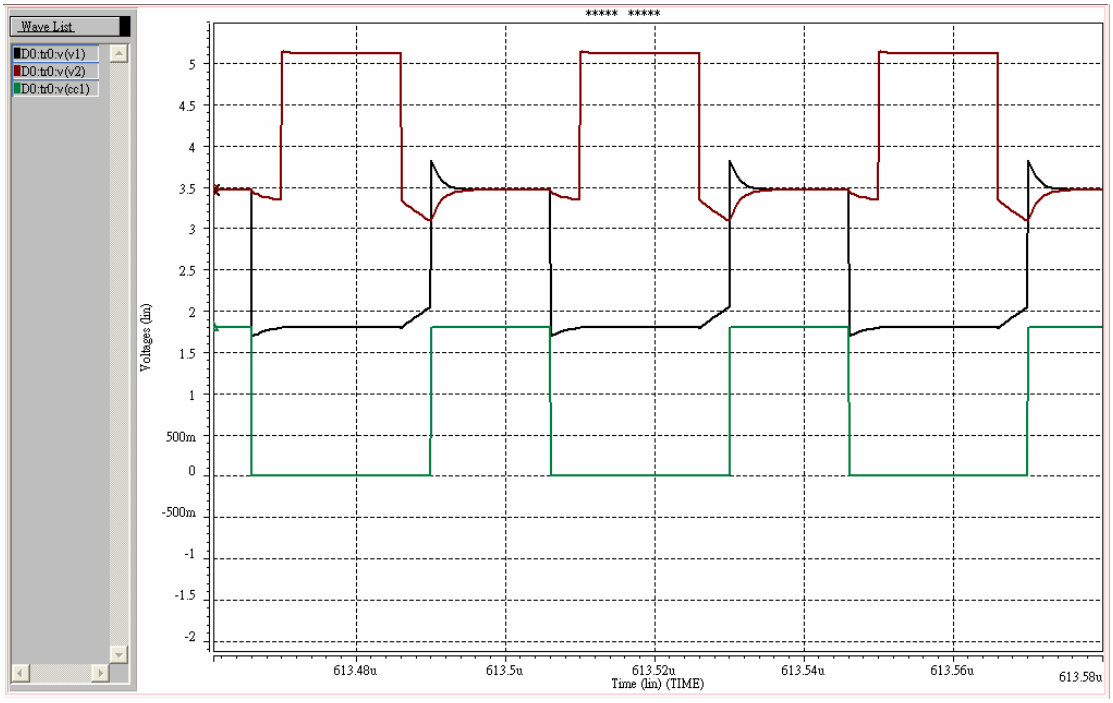
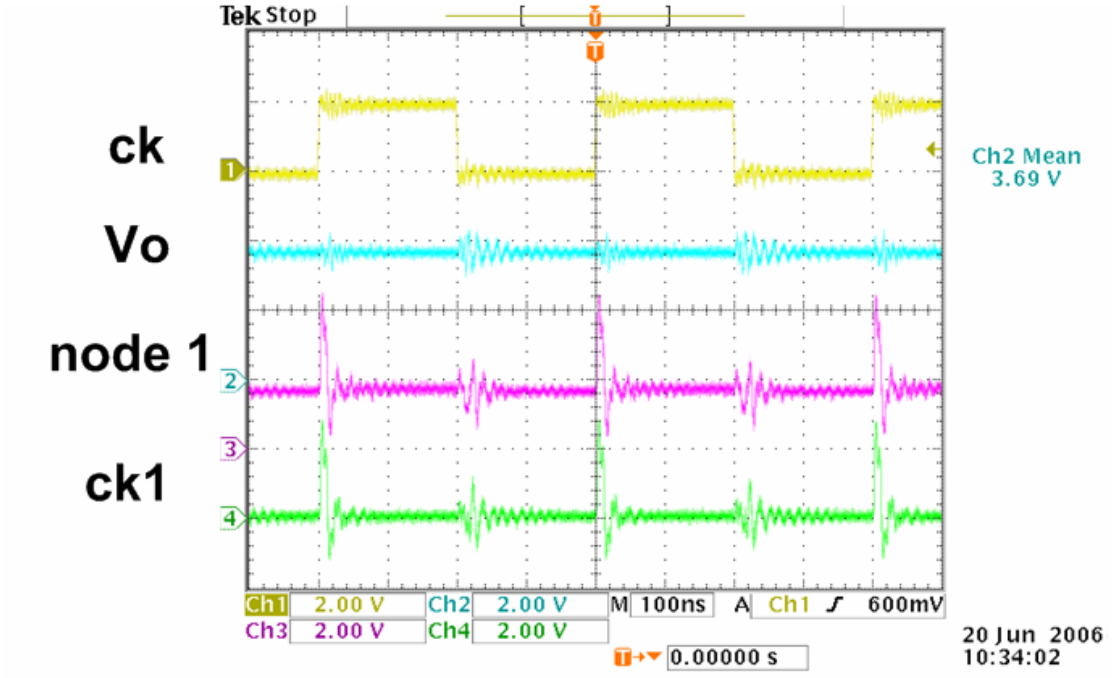
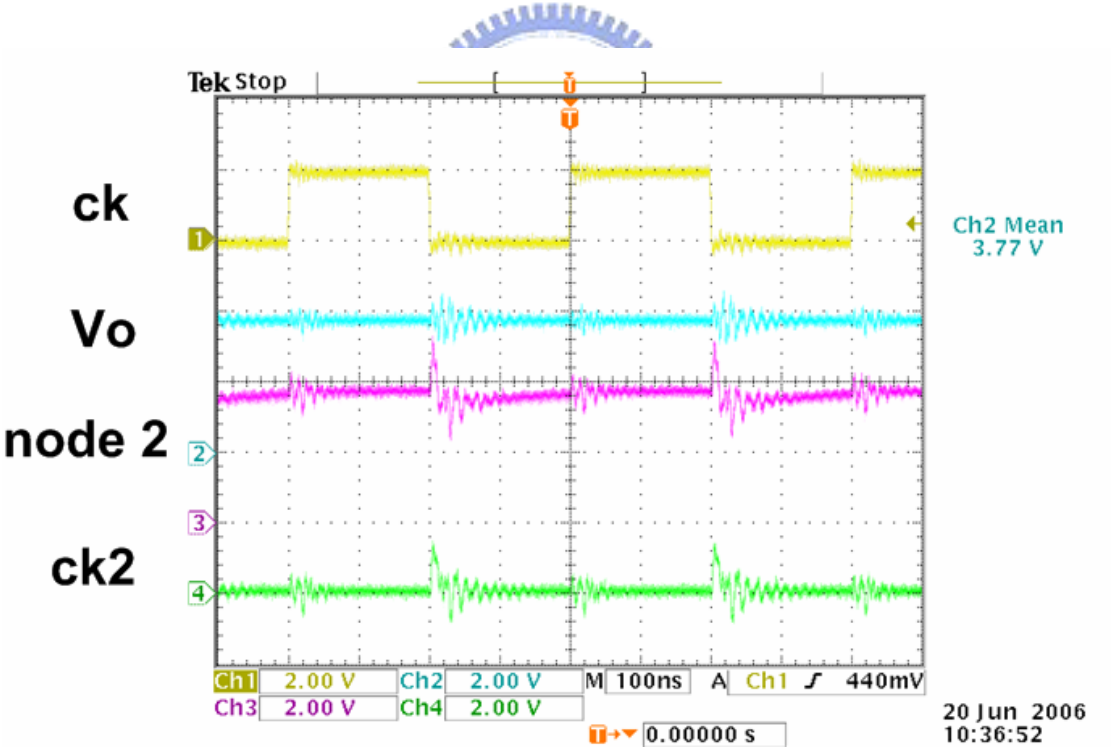


Fig. 6.12 The simulated waveforms of the ck, node 1 and node 2 with f=25MHz.

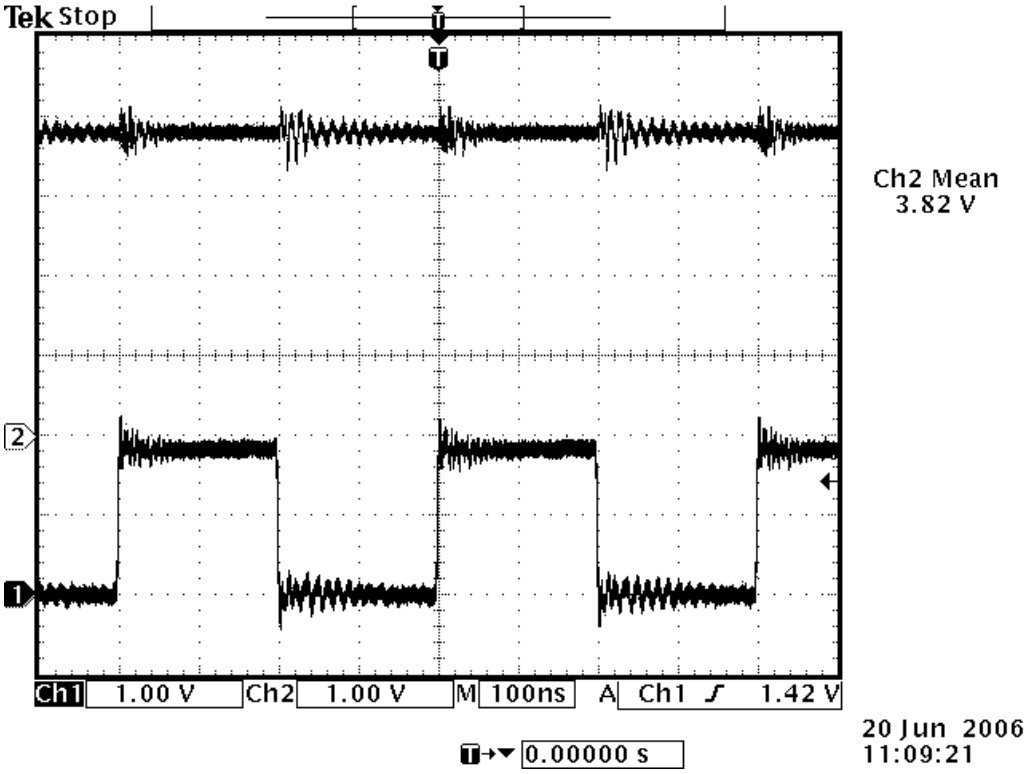


(a)

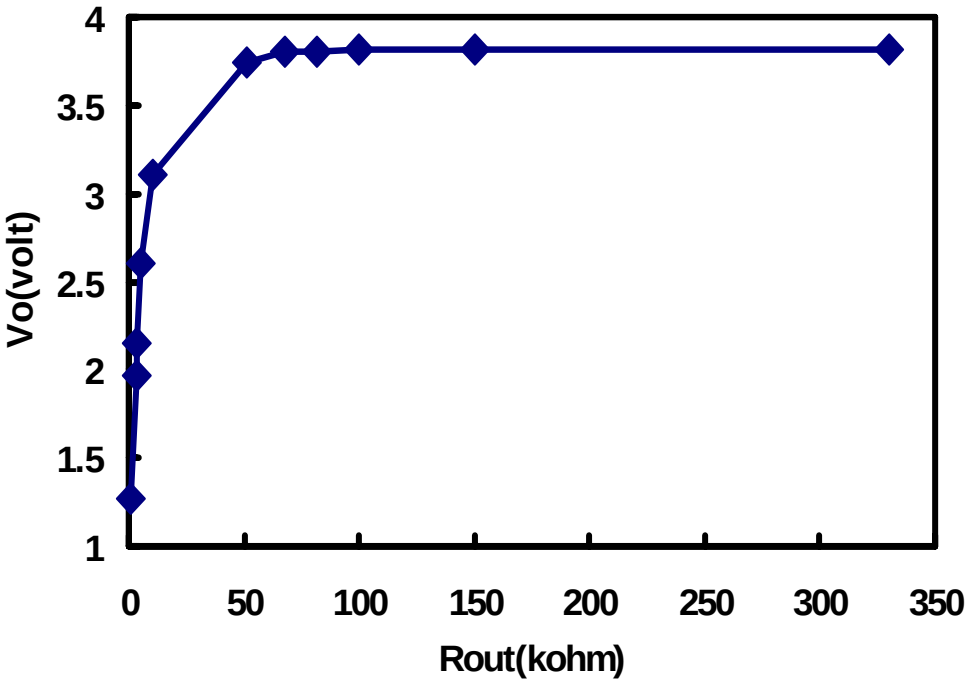


(b)

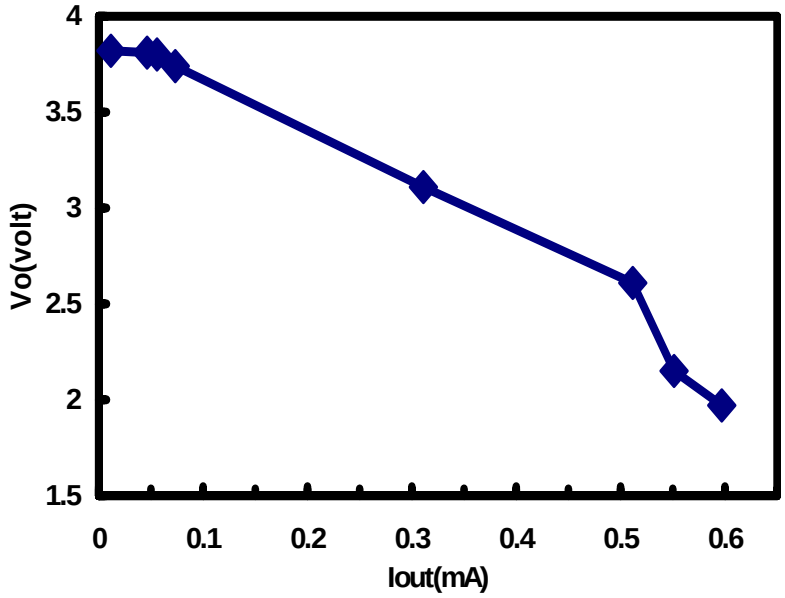
Fig. 6.13 The measurement of (a) the ck, Vo, node 1, ck1 and (b) the ck, Vo, node 2, ck2 for example.


Tek Stop
Ch2 Mean
3.82 V
Ch1 1.00 V
Ch2 1.00 V
M 100ns
A Ch1 1.42 V
0.00000 s
20 Jun 2006
11:09:21

(a)


Vo(volt)
Rout(kohm)
4
3.5
3
2.5
2
1.5
1
0
50
100
150
200
250
300
350

(b)



(c)

Fig. 6.14 (a) The measurement of proposed charge pump circuit (II) output voltage with Rout=68kΩ and the clock signal ck. (b) Vout-Rout curve. (c) Vout-Iout curve.

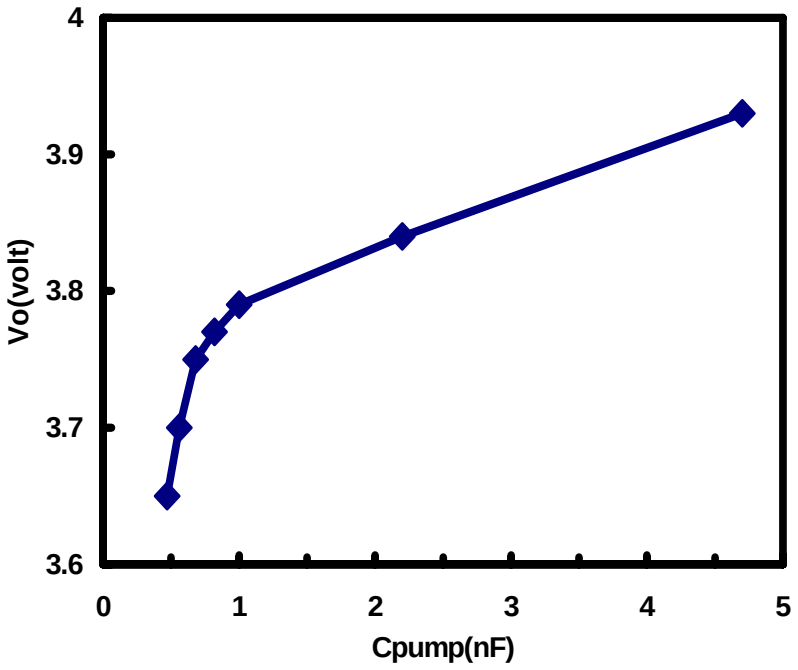


Fig. 6.15 The Vout-Cpump curve with f=1MHz.

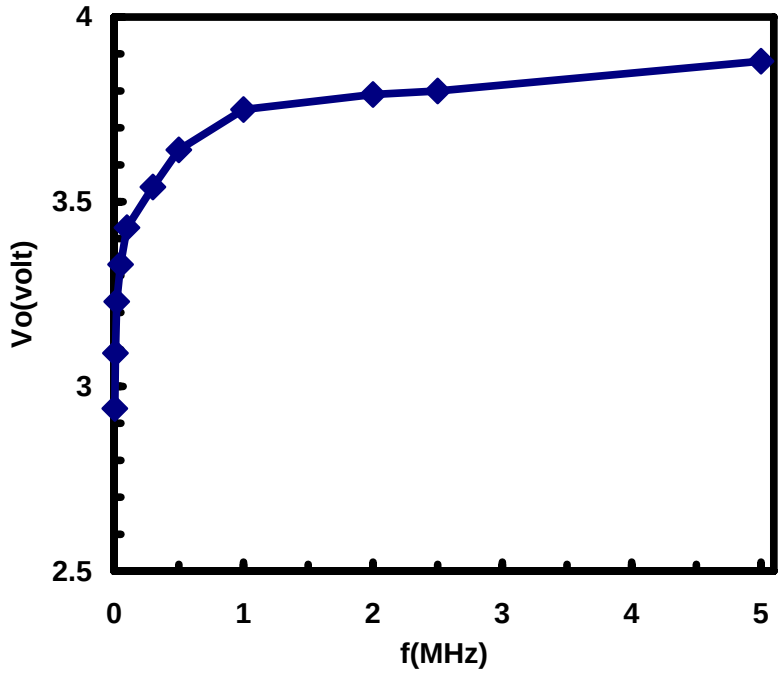


Fig. 6.16 The Vout-f curve with Cpump=680pF.

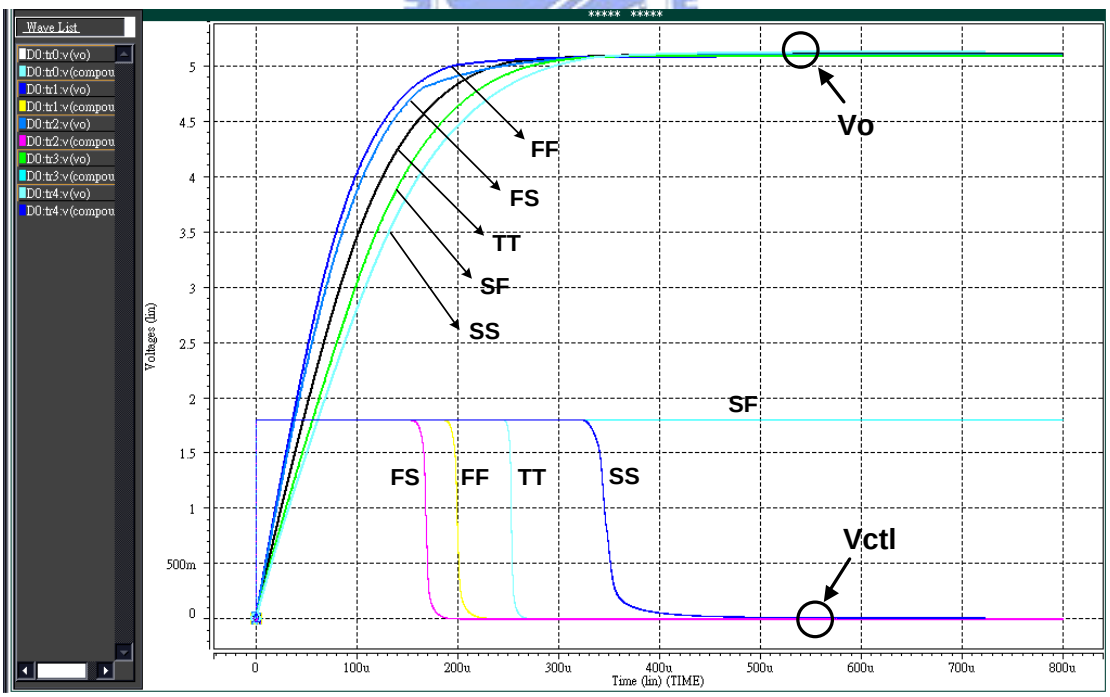
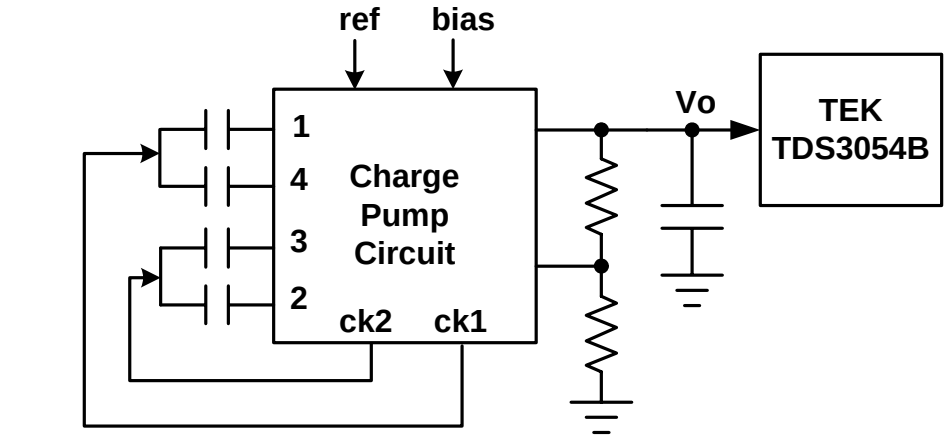
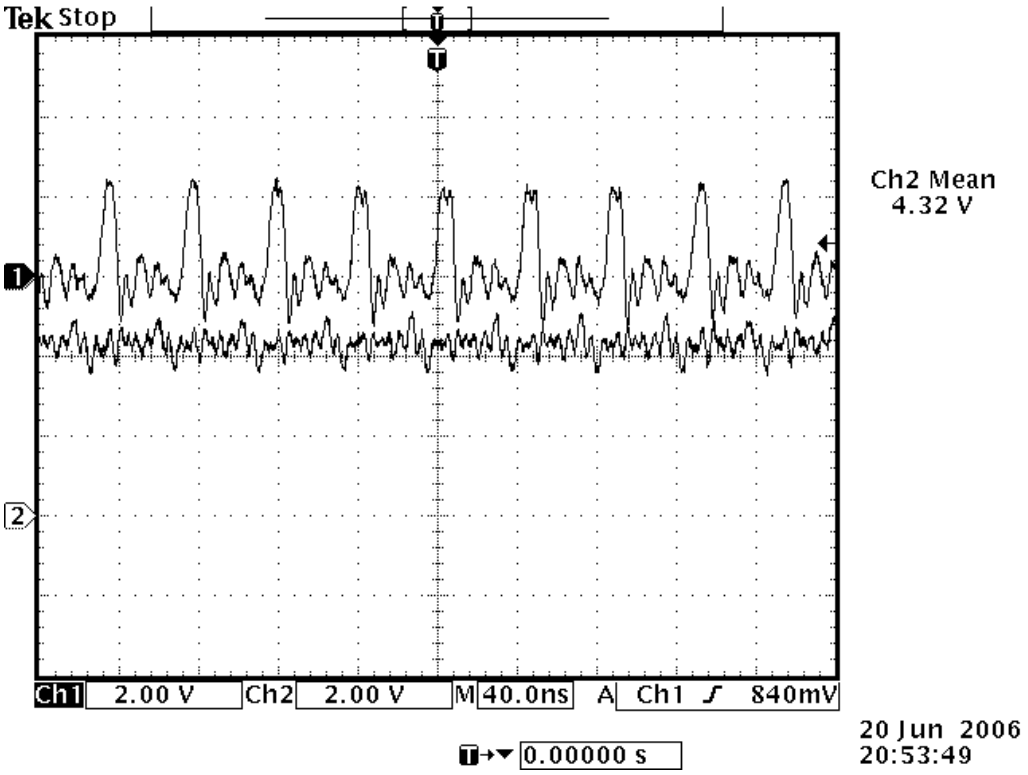


Fig. 6.17 The Vout and Vctl curves in the five corners with Cpump=680pF and f=7 or 25MHz.



(a)



(b)

Fig. 6.18 (a) The measurement setup to test the proposed charge pump circuit (II) with feedback loop. (b) The measurement of ck1 (Ch1) and Vout (Ch2) curves with Cpump=680pF and f=7 or 25MHz.

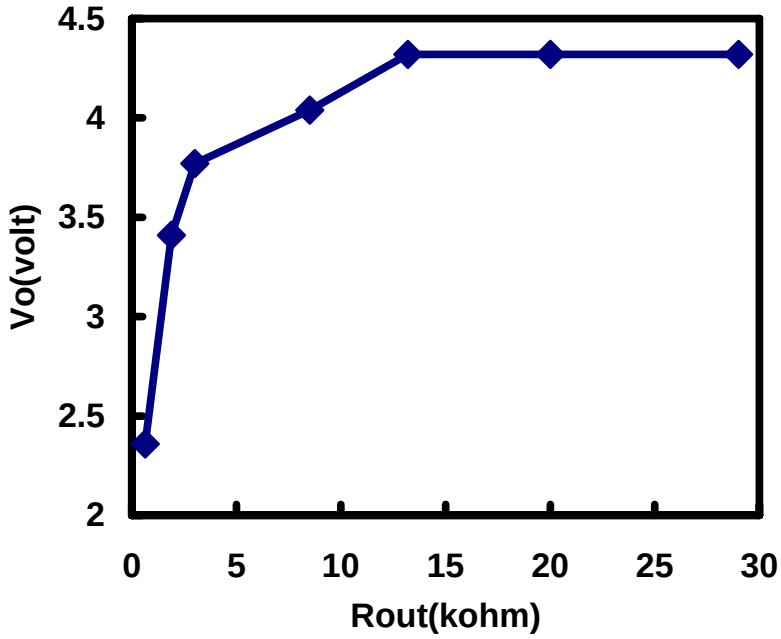


Fig. 6. 19 The Vout-Rout curve with Cpump=680pF and f=7 or 25MHz.

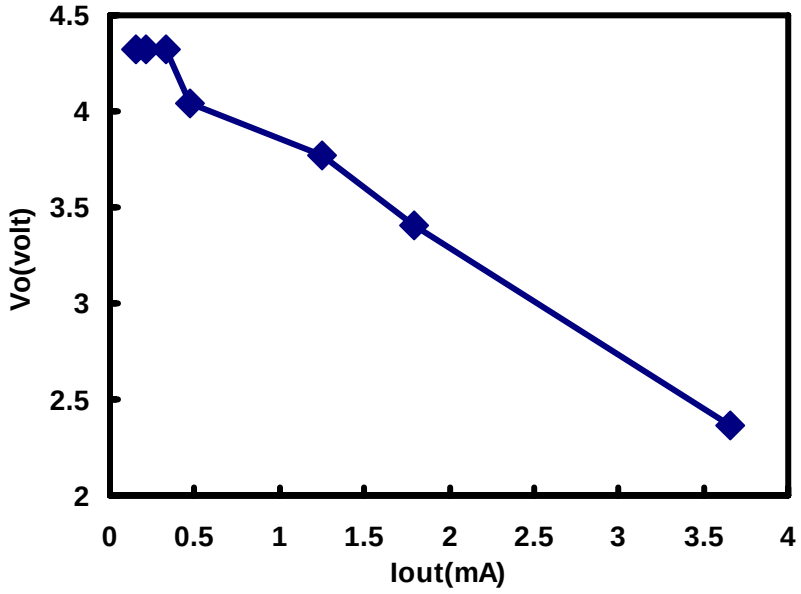


Fig. 6.20 The Vout-Iout curve with Cpump=680pF and f=7 or 25MHz.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

A. Proposed Charge Pump Circuit (I):

The proposed charge pump circuit (I) without gate-oxide reliability problem uses four-phase clocks to solve the old problem shown in Fig. 4.2. Although the proposed charge pump circuit (I) use as twice area of MOSFETs and capacitors as the old one shown in Fig. 3.10. The pumping efficiency will increase due to the gate terminal signals provided directly by the stable clock source and the using of the charge transfer switches. This design eliminates the body effect by biasing the body terminals dynamically, so it is suitable for low-voltage process. This design has four branches to maintain the output voltage, when the output loading current increases. Layout of the proposed charge pump circuit (I) is shown in Fig. 7.1. The photograph of the measured PCB is shown in Fig. 7.6.

B. Proposed Charge Pump Circuit (II):

The proposed charge pump circuit (II) without gate-oxide reliability problem also uses four-phase clocks to solve the old problem shown in Fig. 4.2. It needs less chip area compared to the proposed charge pump circuit (I). The pumping efficiency will increase due to the gate terminal signals provided directly by the stable source and the using of the charge transfer switches. When the output loading current is

increases, this design has two branches to maintain the output voltage. Layout of the proposed charge pump circuit (II) is shown in Fig. 7.2.

Let us discuss the simulation waveform below. In Fig. 7.3, the interval T of the 2^{nd} stage in the proposed charge pump circuit (II) will turn on slowly and the charge will also leak back slowly. It is unfavorable to the pumping efficiency. But, in Fig. 7.3, the 2^{nd} stage in the proposed charge pump circuit (II) cannot turn on immediately in the interval T, and the waveforms of node 1 and node 2 is expected to us. So, we can know that the proposed charge pump circuit (II) is suitable for high frequency or the operation with narrow interval T.

C. Proposed Charge Pump Circuit (II) with Feedback Loop:

The proposed charge pump circuit (II) with feedback loop stabilizes the output voltage level. To compare Fig. 6.18(b) (with 25MHz) with Fig. 6.13 (with 2.5MHz), it appear that the clock signal generated by the oscillator in the feedback loop is better than the one generated by the external clock. It is proved again that the proposed charge pump circuit (II) is suitable for high frequency or the operation with narrow interval T. Layout of the proposed charge pump circuit (II) with feedback loop is shown in Fig. 7.4. The total layout of the proposed charge pump circuit in thesis is shown in Fig. 7.5.

7.2 Future Work

The clock generator is an important part of the charge pump circuit. Now, we divide the clock generator into two parts, one is the oscillator and some digital logic circuit, the other one is the taper buffer driving the large capacitors. As we known, the more ideal the clock waveforms, the better efficiency of the charge pump circuit. So,

the layout drawing of the paths of clock signals is the most important things.

The cross coupling effect due to layout drawing is shown in Fig. 7.7. The clock signal lines in the chip usually draw from one node to another node. But the distance between these two nodes may be very long or very short. It might also pass through many metal layers. So, the cross coupling effect has many chances to occur in the course of the clock signal transmission. The solutions of the coupling effect discussed above are using power line shielding, the parallel signal lines separated from each other for a certain distance or using separated power lines for different circuit blocks. Although this shielding work may increase the layout area, it can get the better efficiency of the charge pump circuit.

As we known, the inductances of bonding wires will cause the ground bounce. The larger value of the charge pump circuit frequency will cause the worsen ground bounce. The worsen ground bounce by inconsiderable layout drawing is shown in Fig. 7.8. Due to the power lines of VDD and GND stretch horizontally and paralleled, the cross coupling effect has many chances to occur in the course of the clock signal transmission. This situation will let the ground bounce worsen. The solutions are using separated power lines for different circuit blocks and decreasing the frequency of the charge pump circuit.

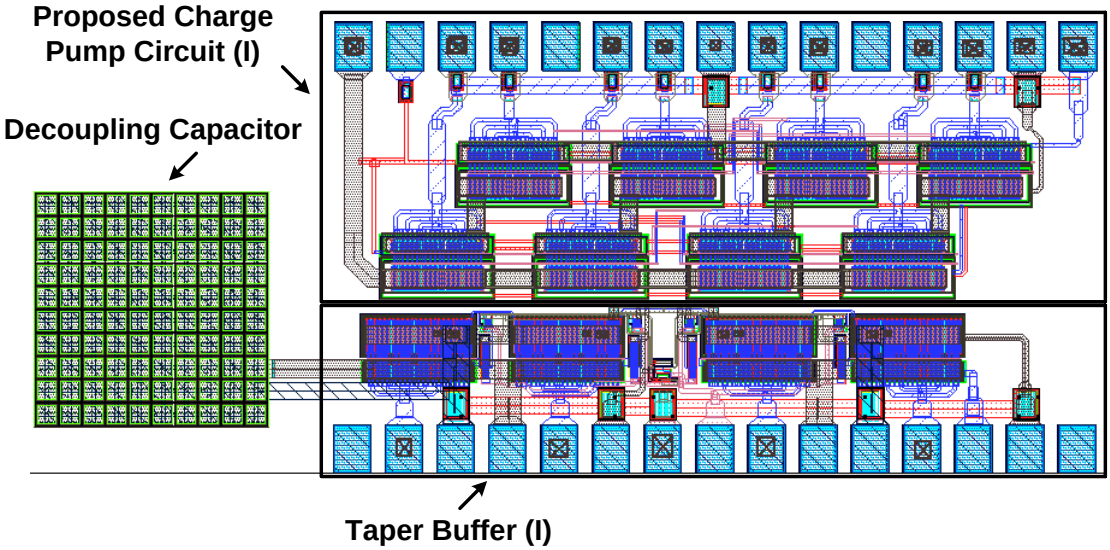


Fig. 7.1 Layout of the proposed charge pump circuit (I).

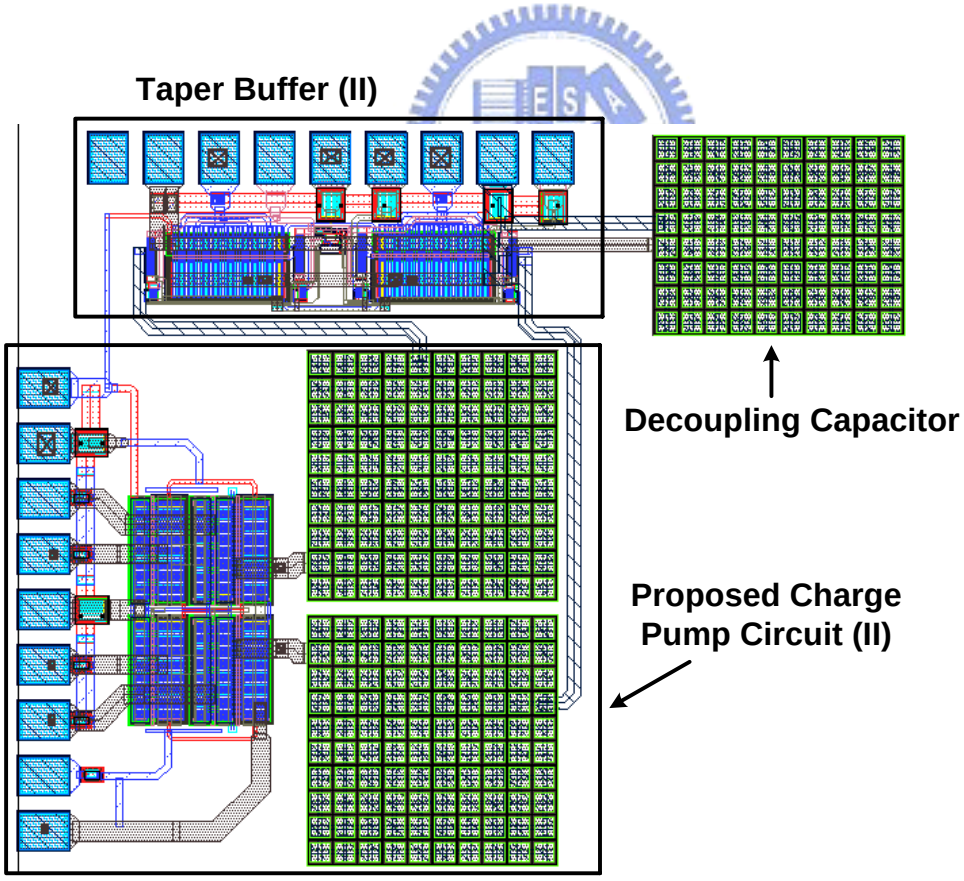


Fig. 7.2 Layout of the proposed charge pump circuit (II).

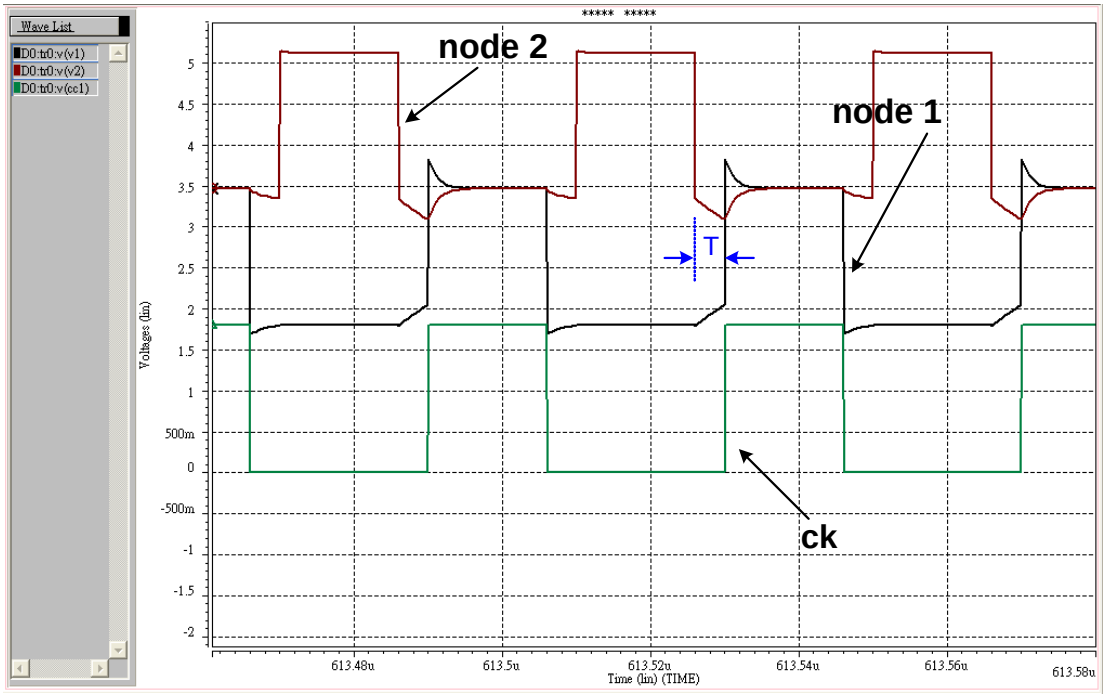


Fig. 7.3 The simulated waveforms of the ck, node 1 and node 2 in proposed charge pump circuit (II) at the 25MHz.

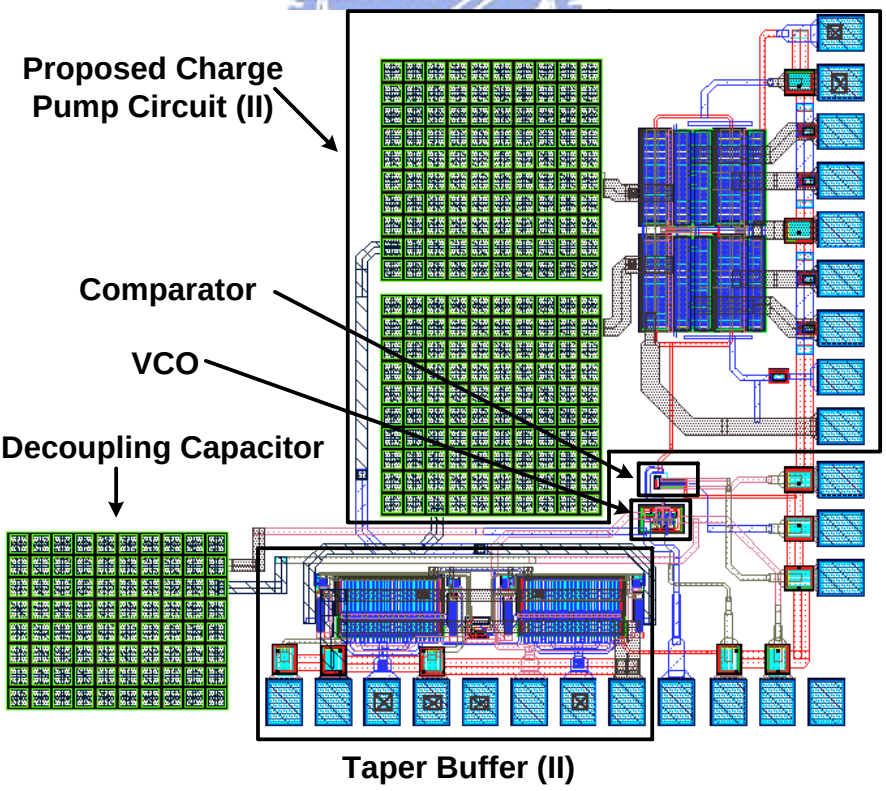


Fig. 7.4 Layout of the proposed charge pump circuit (II) with feedback loop.

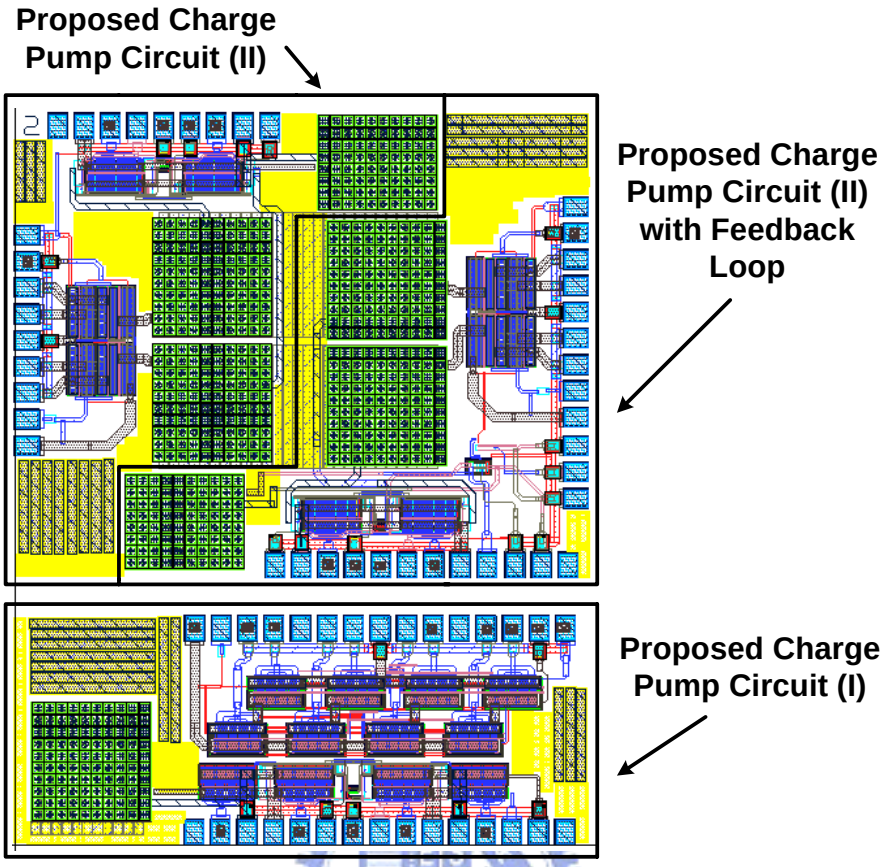


Fig. 7.5 Total layout of the proposed charge pump circuit in thesis.

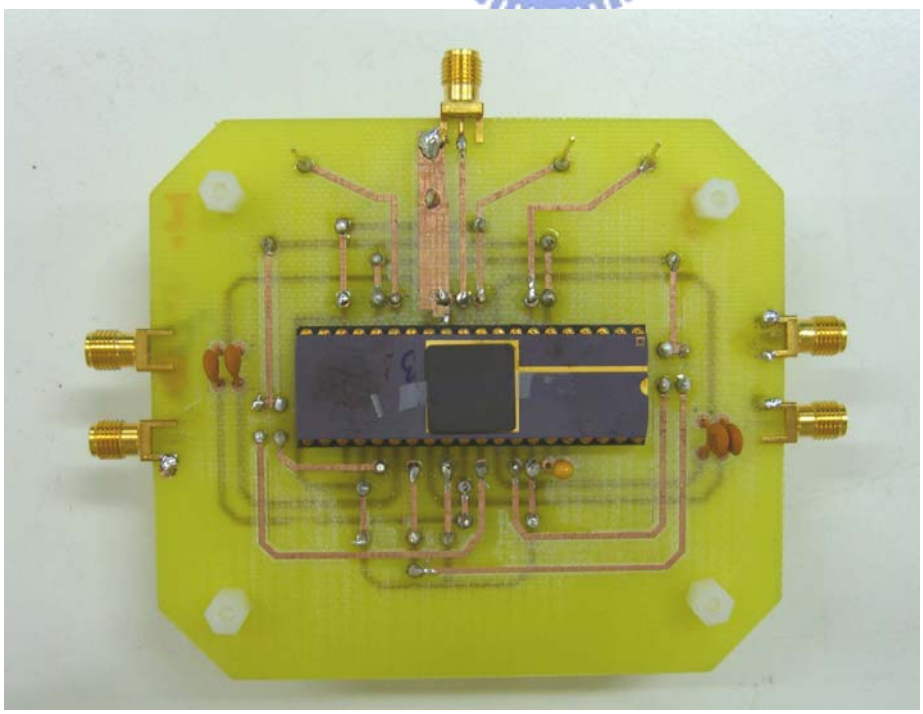


Fig. 7.6 The photograph of the measured PCB.

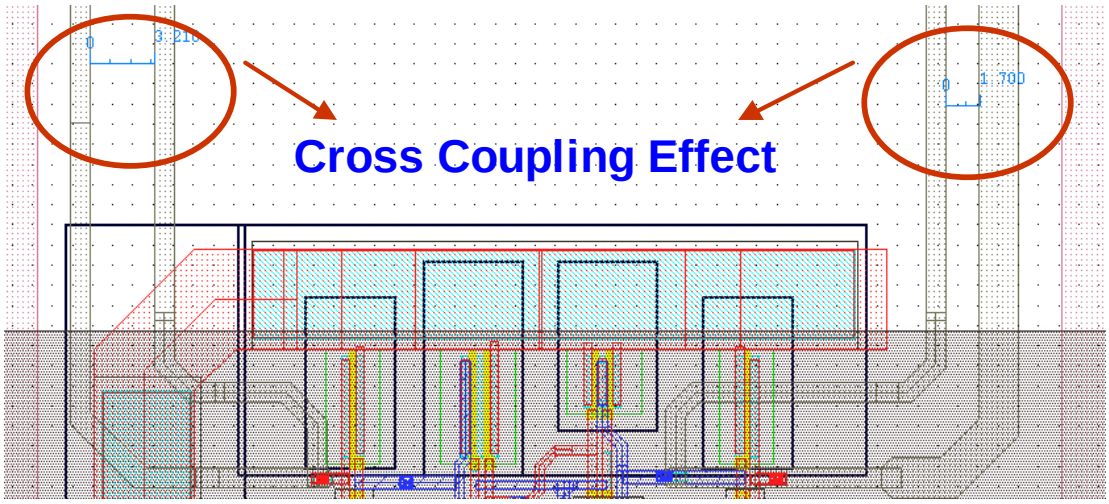


Fig. 7.7 The cross coupling effect due to layout drawing.

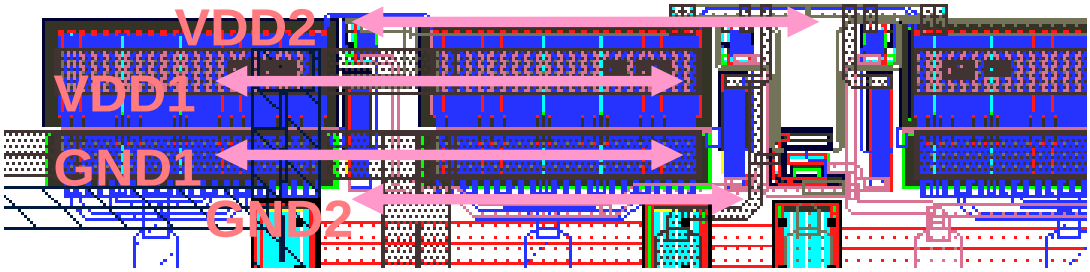


Fig. 7.8 The worsen ground bounce due to layout drawing.

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