

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

一個操作在 1.25 到 6 Gbps

脈衝式時脈資料回復電路



**A 1.25~6 Gbps Burst-Mode
Clock and Data Recovery Circuit**

研究生：徐國慶

指導教授：陳巍仁 博士

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Advisor : Prof. Wei-Zen Chen



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積體電路技術的快速進步早已經鞭策著低價又便宜的寬頻存取服務的發展，對於發展經濟型高速的光纖用戶網路來說，以被動光纖網路為基礎的光纖到家系統被認為是前景一片看好的。在被動光纖網路中，時脈與資料回復電路在收發機裡扮演一個非常重要的角色，因此，在此應用中，如何實現一個具有快速鎖定的脈衝式時脈與回復電路是一個關鍵性的課題。此外，如何利用較便宜的互補式金屬氧化半導體製程來實現高速的時脈與資料回復器將是可以用相對較低的成本而達到更高傳輸頻寬的不二法門。

在本論文，我們提出一操作在 1.25 到 6 Gbps 且使用「四分之一速率」「四通道」架構的脈衝式時脈與資料回復電路。我們藉由在晶片上結合了一個寬範圍可以供頻帶選擇的鎖相迴路，來達到四分之一時脈技術，鎖相迴路時脈頻率減少四倍，使得壓控震盪器操作頻率設計上可以更加彈性。由於使用四個通道的架構，接收到的串列式資料會自動被回復並

且解多工成四筆平行式資料，此架構不需要額外的解多工器以降低功率消耗。此外，我們會在時脈與資料回復電路前端整合一個寬頻限制放大器讓輸入資料的振福小到 30mV 也可以處理。

在時脈與資料回復器的追蹤迴路裡面，我們使用一個創新的亞歷山大型的相位偵測器來改善操作速度到 6GHz。在動態式數位濾波器裡面利用二位元搜尋法來達到快速的相位校正，二位元和線性雙模式的搜尋法的操作方式不但可以降低鎖定時間，同時也可以降低追蹤時的抖動量，這在傳統的鎖相迴路式脈衝式時脈與資料回復器是必須有所取捨的。此外，相位內差器的取樣相位精準度高達 1/32 位元時間使得靜態相位誤差最小化。

測試晶片使用標準 0.18 μm 互補式金氧半製程技術來製造，量測到的鎖相迴路輸出頻率範圍為 280MHz 到 1.7GHz，峰對峰抖動值分別為 79.6 到 20.2 ps。在操作電壓為單一 1.8V 之下，整個時脈與資料回復器包含輸出緩衝電路的總功率消耗為 78mW。



A 1.25~6 Gbps Burst-Mode Clock and Data Recovery Circuit

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Abstract

The rapid progress in integrated circuit (IC) techniques has spurred the development of low-cost and convenient broadband access services. Fiber-to-the-home (FTTH) system based on passive optical network (PON) is considered as a promising technology for deploying economically high-speed subscriber networks. In the passive optical network, clock and data recovery (CDR) circuit plays an important role in the transceiver. Thus, how to realize a burst-mode CDR with rapid lock time is a critical issue in this application. Besides, implementing the high speed CDR in an inexpensive CMOS technology is the key to enable higher bandwidth communications at a relatively lower cost.

In this thesis, a 1.25~6 Gbps burst-mode CDR circuit with quarter-rate four-channel architecture is proposed. Quarter-rate clocking technique is exploited by incorporating the on-chip wide-range phase locked-loop (PLL). The clock frequency can be reduced by a factor of 4 so as to relax the operating speed of the VCO. By means of four-channel topology, the received serial data stream can be recovered and demultiplexed into four parallel channels. Thus no extra de-multiplexer is needed to save power consumption. Besides, incorporating with a broad-band

limiting amplifier in the front-end, the input sensitivity level of the CDR can be as low as 30mV.

In the CDR tracking loop, a novel Alexander phase detector (PD) is proposed to improve the operation frequency up to 6GHz. Rapid phase acquisition is achieved by employing binary search algorithm along with the dynamic digital loop filter. The dual-mode operation of the loop filter not only reduces the lock time but also the tracking jitter, which must be severely compromised in a conventional PLL-based CDR. Moreover, the sampling phase resolution in the phase interpolator (PI) can be up to $1/32UI$ to minimize the static phase error.

The test chip is fabricated in a standard $0.18\text{-}\mu\text{m}$ CMOS technology. The measured PLL output frequency ranges from 280MHz to 1.7GHz, whose peak-to-peak jitter is about 79.6 ps and 20.2 ps respectively. The whole CDR circuit, including output buffers, dissipates 78mW from a single 1.8V power supply.



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徐國慶
于 風城交大
96 年 春

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