Chapter 4

Phase-Locked Loop with Automatic Band Selection

4.1 The Topology of Phase-Locked Loop

The function of Phase-Locked Loop (PLL), which is also called Clock Multiple Unit (CMU) in high speed link system, is to generate a precise reference clock and provide to the whole Clock and Data Recovery (CDR) system. Our quarter-rate four-channel CDR operates at 1.5~6 Gbps, so we need to provide 375MHz~1.5GHz

eight-phase wide-range precise clock due to the quarter-rate architecture.

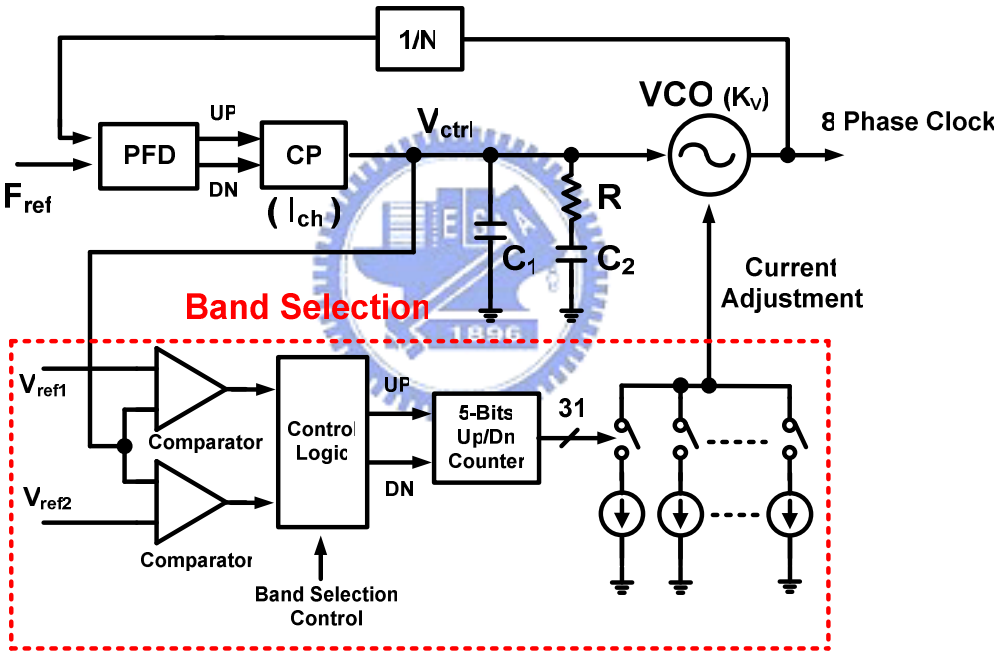
Fig. 4-1(a) demonstrates the topology of phase-locked loop with band selection. The upper block is a conventional PLL architecture. It is composed of a phase and frequency detector (PFD), a charge pump (CP), second-order low pass filter (LPF, or called loop filter (LF)), a voltage-controlled oscillator (VCO), and a divided-by-4 divider. The clock signal oscillated from VCO is divided by four and feedback to the PFD. By comparing phase relationship with the external reference clock f_{ref}, PFD outputs UP or DN signal to the charge pump (CP). CP further charges or discharges the loop filter (LF) to generate the DC control voltage V_{ctrl}. V_{ctrl} is revised and the output frequency of VCO becomes four times of the reference clock f_{ref}. Simultaneously, keep the PLL loop stable by utilizing loop filter (LF) to filter out the high frequency noise. While the output phase tracks the reference clock phase, this PLL is in the lock condition. Moreover, it is to deserve to be mentioned that all the schematic blocks are fully-differential implemented for the sake of providing more immunity to the common-mode noise than single-end architecture.

The output frequency range is from 375MHz to 1.5GHz. This is a broad-band approach. The method of achieving a wide frequency tuning range with small VCO gain (also called K_{VCO})[39-42], as shown in Fig. 4-1(b). The 31 frequency bands with low K_{VCO} cover desired frequency range. This low-K_{VCO} approach is necessary to suppress phase noise rather than a large VCO gain in whole wide range desired frequency range [39]. Analytically, the magnitude of the reference spurs can be approximated by narrow-band frequency modulation (FM) and is determined by the VCO gain [(Hz/V)], expressed as:

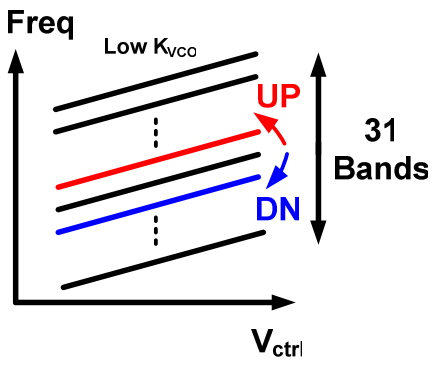
$$\frac{A_{spur}}{A_{carrier}} = \frac{1}{2}\frac{K_{VCO}V_m}{2\pi F_{ref}} \tag{4.1}$$

where A_{spur} is the amplitude of reference spur. $A_{carrier}$ is the amplitude of approximated narrow-band FM carrier. V_m is the voltage of FM signal. We can simply observe the amplitude of reference spur is proportional to K_{VCO}.

The underneath block illustrated in Fig. 4-1(a) is the topology of Band Selection. Determining the output frequency is locked on which frequency band and band-hopping is monitored by this scheme. It exploits the difference between the DC control voltage V_{ctrl} and the external reference frequency V_{ref} to adjust the current tail in the delay cell of VCO. For this reason, the scheme arrives at the function of the automatic band-hopping to lock the PLL loop.



(a)



(b)

Fig. 4-1 (a) The Topology of Phase-Locked Loop with Band Selection

(b) 31 Frequency Bands with Low K_{VCO} for Band Selection

The stability of whole PLL loop must be carefully considered for the wide-range approach. While the output frequency increases from low to high, the reference frequency f_{ref}, which is one-fourth of the output frequency, also increases. In order to keep the stability of PLL loop, we let the PLL loop bandwidth increase in proportion to the reference frequency f_{ref}. Thus, the relationship between the other parameters are expressed as:

$$C_1 \propto \frac{1}{f_{ref}} \tag{4.2}$$

$$I_{ch} \propto f_{ref} \tag{4.3}$$

$$\omega_n = \sqrt{\frac{1}{N} \times I_{ch} \times K_V \times \frac{1}{C_1}} \propto f_{ref} \tag{4.4}$$

$$\zeta = \frac{1}{2} \times \omega_n \times R \times C_1 \tag{4.5}$$

where C_1 is in the loop filter. Ich denotes the charge pump current. ω_n is the natural frequency and ζ is the damping factor. We can observe that the damping factor ζ is kept for a constant whatever the output frequency is arbitrarily changed.

Fig. 4-2 illustrates simulated open loop frequency response of PLL by Simulink behavior model. The phase margin of PLL > 60°.

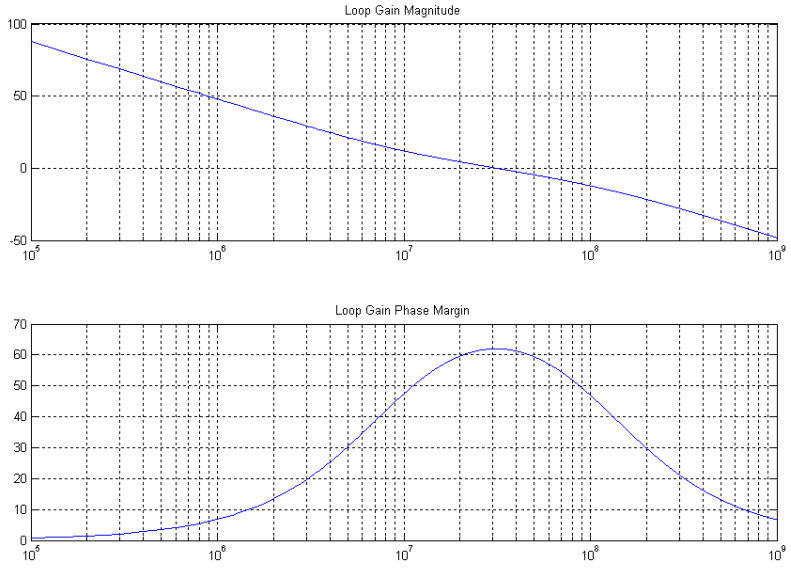


Fig. 4-2 Simulated Open Loop Frequency Response of Phase-Locked Loop

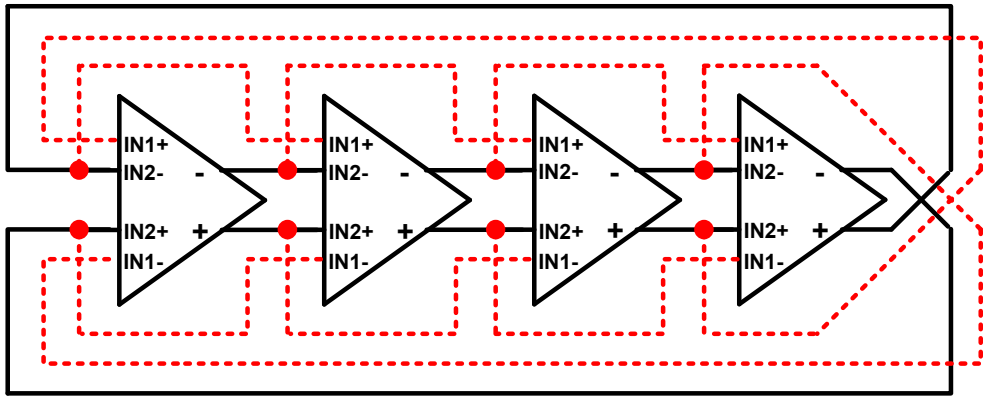
4.2 Voltage-Controlled Oscillator

4.2.1 Voltage-Controlled Oscillator Core

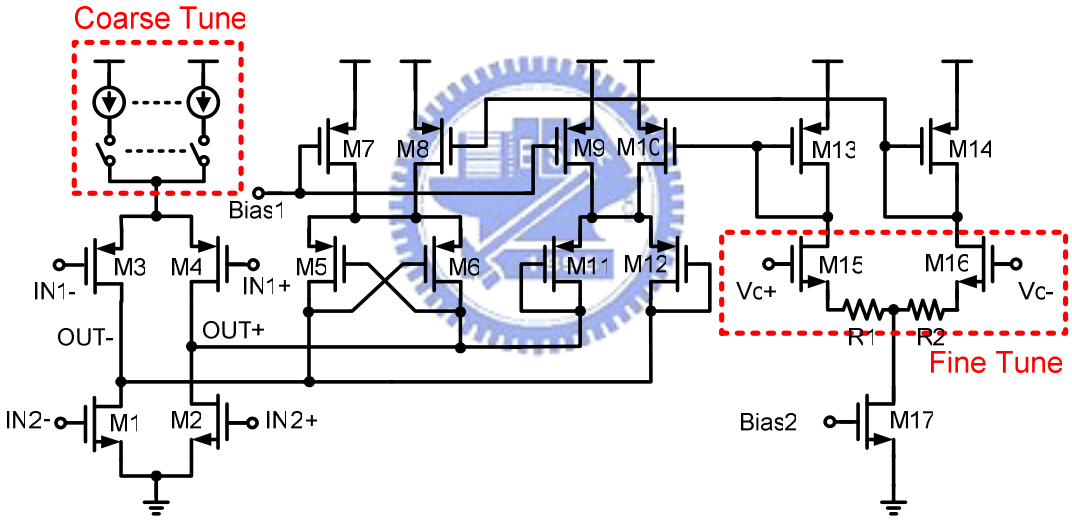
The topology of four-stage ring oscillator is demonstrated in Fig 4-3(a). It utilizes two delay paths so that each delay cell has two differential inputs. One input is NMOS-input for primary delay path (real line) and the other input is PMOS-input for secondary delay path (dash line). Negative skew compensation method is used in the secondary delay path in order to precharge PMOS in each input of delay cell and then the operating frequency of VCO increases.

Fig 4-3(b) introduces the circuit schematic of each delay cell. Both coarse tuning and fine tuning scheme are used for frequency tuning. The control voltage V_{ctrl} changes for fine tuning. It makes the output frequency vary on a fixed band. However, the tail current of M1-M4 is controlled for coarse tuning. It makes the output

frequency hop to the adjacent up or down frequency band by switching on or off a current source of the current-steering DAC.



(a)



(b)

Fig 4-3 (a) The Topology of Four-Stage Negative-Skew Ring Oscillator

(b) The Circuit Schematic of Each Delay Cell in (a)

4.2.2 Voltage-Controlled Oscillator Buffer

Fig 4-4 illustrates the circuit schematic of VCO buffer. The buffer makes each output frequency have the same loading. Hence, the oscillation frequency is not affected by the loading of the next circuit block.

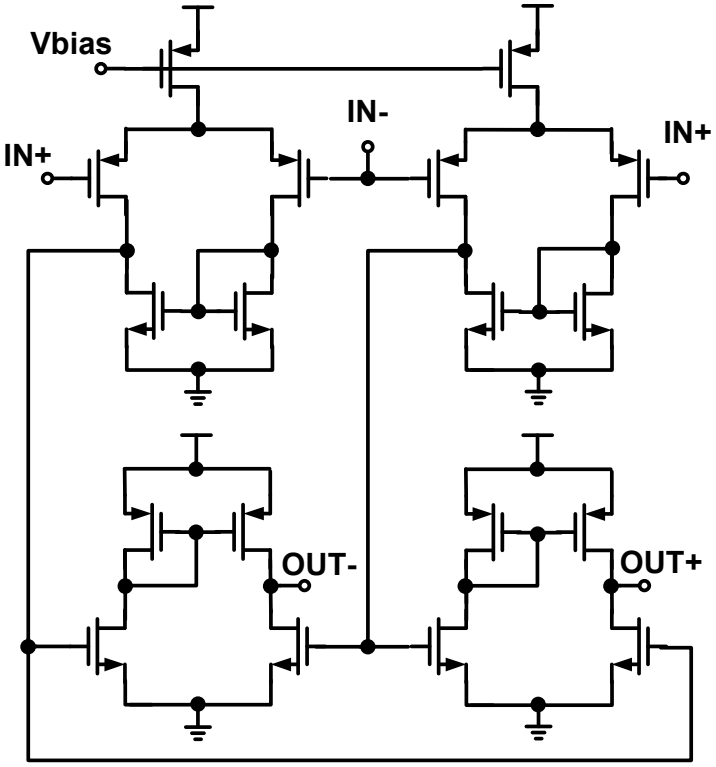
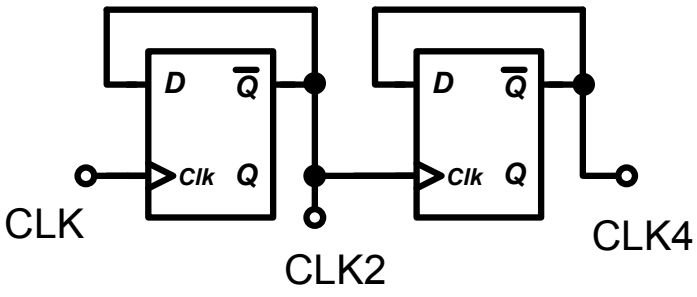


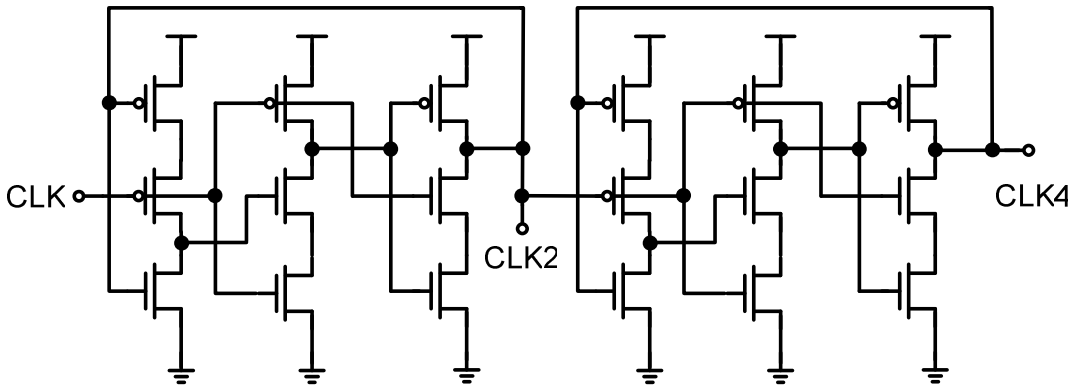
Fig 4-4 The Circuit Schematic of Voltage-Controlled Oscillator Buffer

4.3 Divider

The topology of divided-by-4 divider is introduced in Fig. 4-5(a). This architecture is a static frequency divider. It consists of two cascade divided-by-2 dividers. Each cell is TSPC-type (True Single Phase Clock) D-Flip-Flops and the output connects to the input of DFF, as shown in Fig. 4-5(b). The output changes while the input changes twice. Therefore, The output frequency is half the input frequency.



(a)



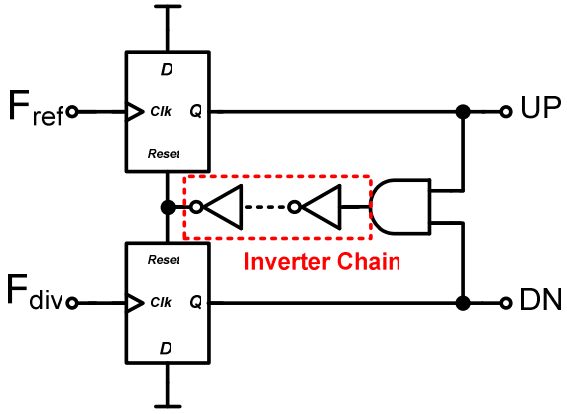
(b)

Fig. 4-5 (a) The Topology of TSPC-type Divided-by-4 Divider

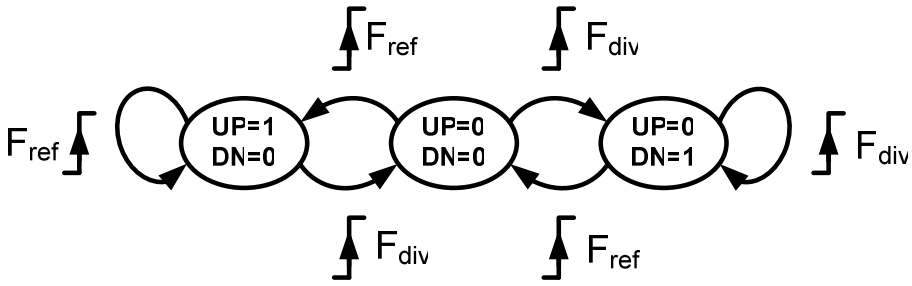
(b) The Circuit Schematic of (a)

4.4 Phase and Frequency Detector

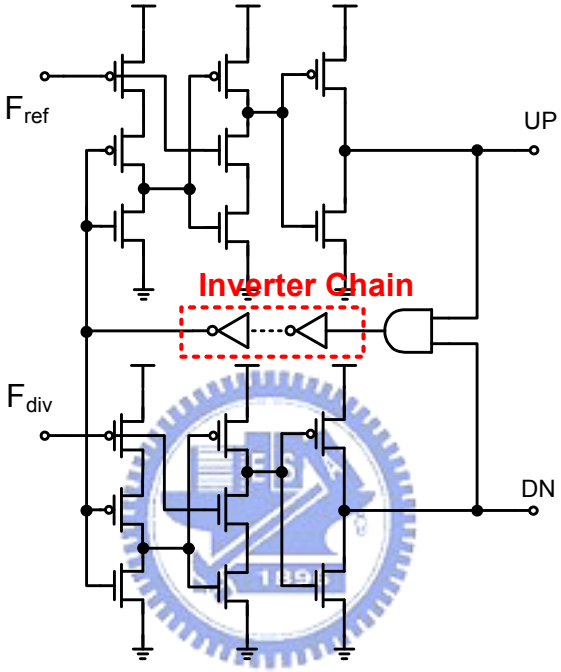
Fig. 4-6(a) shows the topology of conventional tri-state phase and frequency detector (PFD) and (b) is the state diagram of the PFD. The inverter chain is used to eliminate the appearance of dead zone. The circuit schematic is demonstrated in Fig.4-6(c) and the DFFs is a pre-charge type TSPC. At last, the characteristic output of PFD illustrated in (d) is nice owing to no appearance of dead zone.



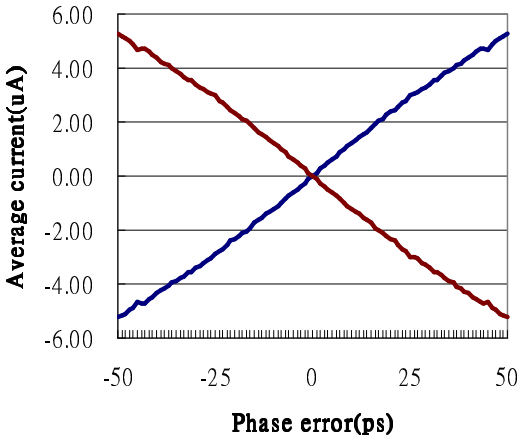
(a)


Fref
Fdiv
Fref
UP=1
DN=0
UP=0
DN=0
UP=0
DN=1
Fdiv
Fdiv
Fref

(b)


Fref
UP
Inverter Chain
Fdiv
DN

(c)


6.00
4.00
2.00
0.00
-2.00
-4.00
-6.00
Average current(uA)
-50
-25
0
25
50
Phase error(ps)

(d)

Fig. 4-6 (a) The Topology of Tri-state Phase and Frequency Detector

(b) The State Diagram of Tri-state Phase and Frequency Detector

(c) The Circuit Schematic of (a)

(d) The Characteristic Output of Tri-state Phase and Frequency Detector

4.5 Charge Pump and Loop Filter

Fig. 4-7 demonstrates the schematic of charge pump with loop filter. The fully-differential architecture makes no static current while charge mode or discharge mode.

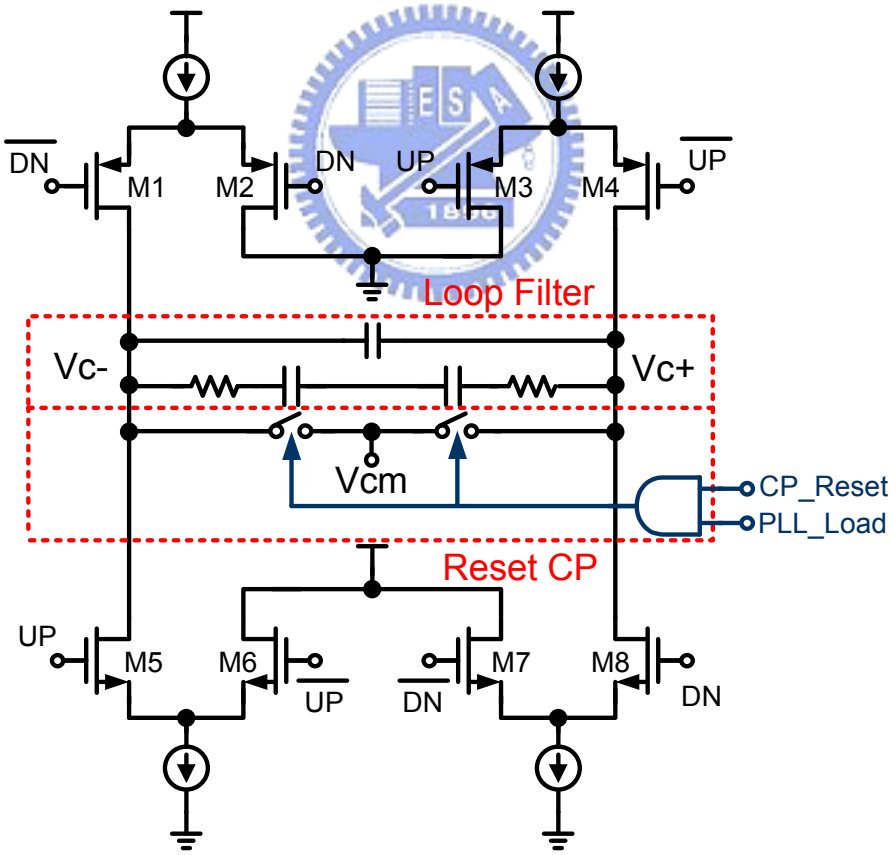


Fig. 4-7 The Circuit Schematic of Charge Pump with Loop Filter

4.6 Band Selection Method

Band selection method is indispensable to execute band-hopping. Determining the output frequency is locked on which frequency is monitored by this scheme. This scheme is implemented and shown in Fig.4-8. It judges whether the immediate frequency is in the desired frequency band or not.

After comparing the control voltage V_{ctrl} with two external assigned reference voltages V_{ref1} and V_{ref2}, the comparator sends UP or DN signal to a 5-bit up/down counter. The UP signal is sent if differential V_{ctrl} is larger than V_{ref1}, and that means the band should hop to the adjacent upper band. At the same time, the DN signal is sent if differential V_{ctrl} is smaller than V_{ref2}, and that means the band should hop to the adjacent lower band (Default $V_{ref1} > V_{ref2}$). If V_{ctrl} is in the among of V_{ref1} and V_{ref2}, neither UP nor DN is sent and keep the immediate band.

The 5-bit up/down counter calculates the UP/DN number and further outputs 31 thermometer codes to control a 5-bit current-steering digital-to-analog converter (DAC). The output current tail feeds back to each delay cell of 4-stage ring oscillator and then adjusts the output frequency to the desired frequency band.

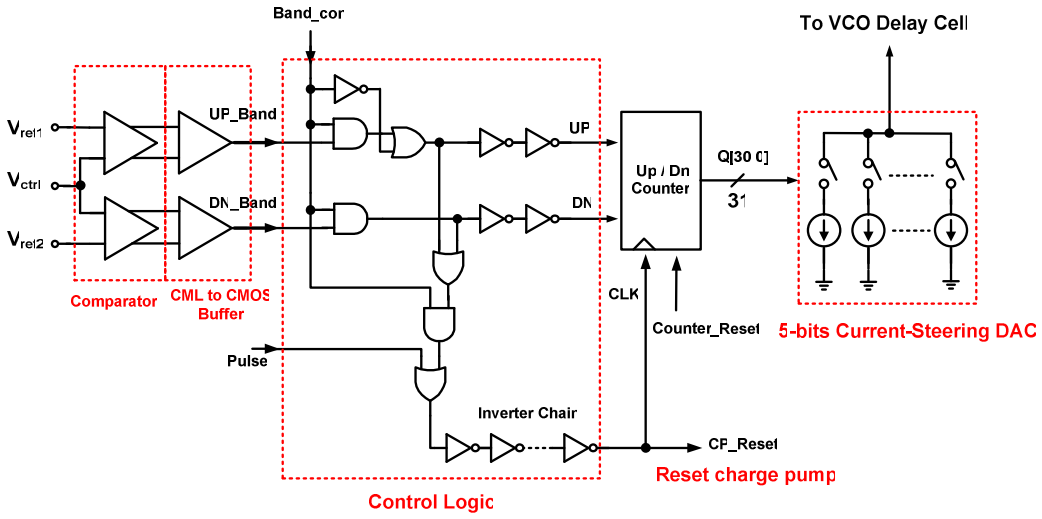


Fig. 4-8 The Topology of Band Selection Implementation

4.7 Comparator

Fig. 4-9(a) and (b) show the circuit schematic of comparator and CML-to-CMOS buffer. The CML-to-CMOS buffer reshapes the compared UP or DN signal to full swing.

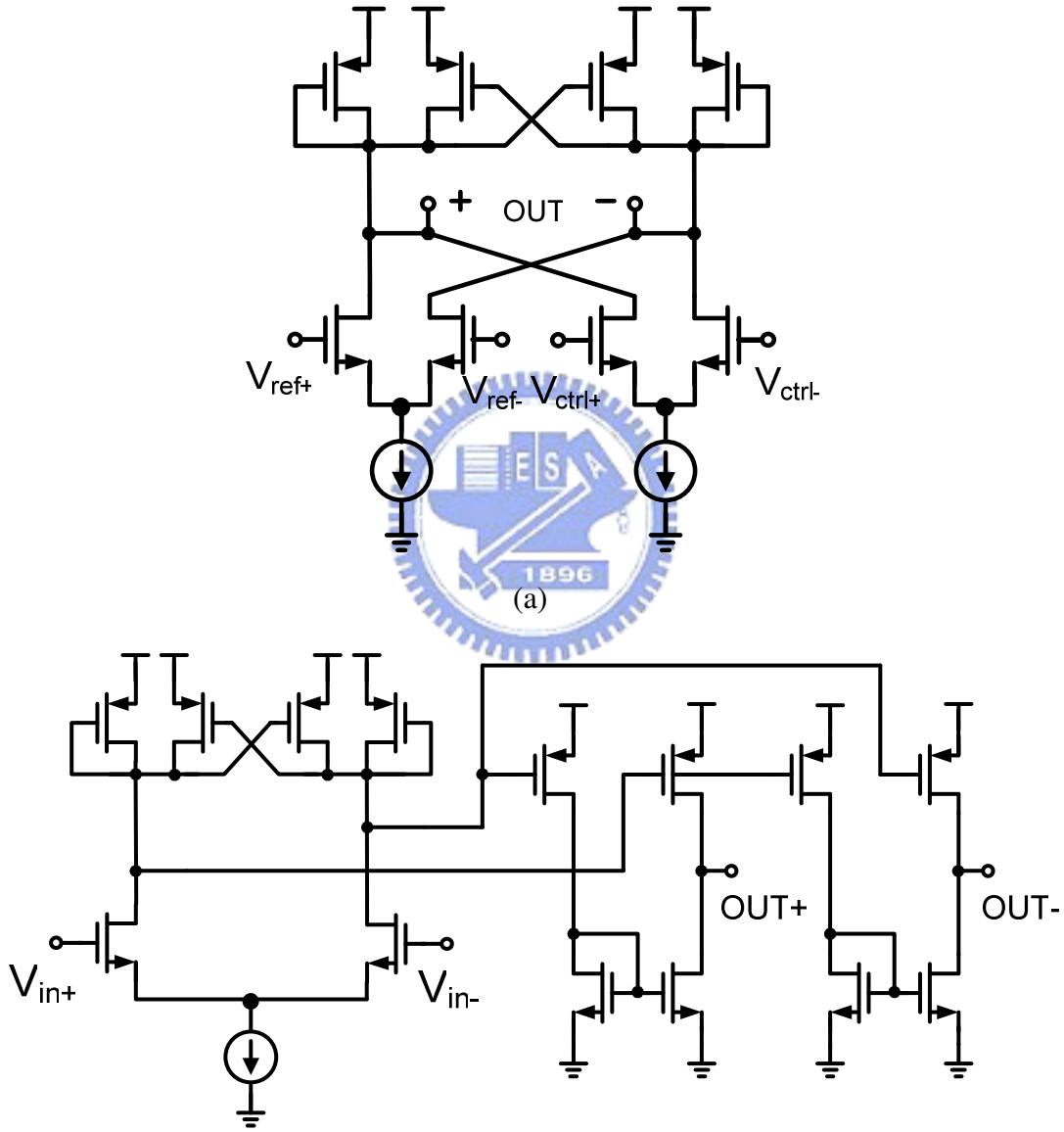
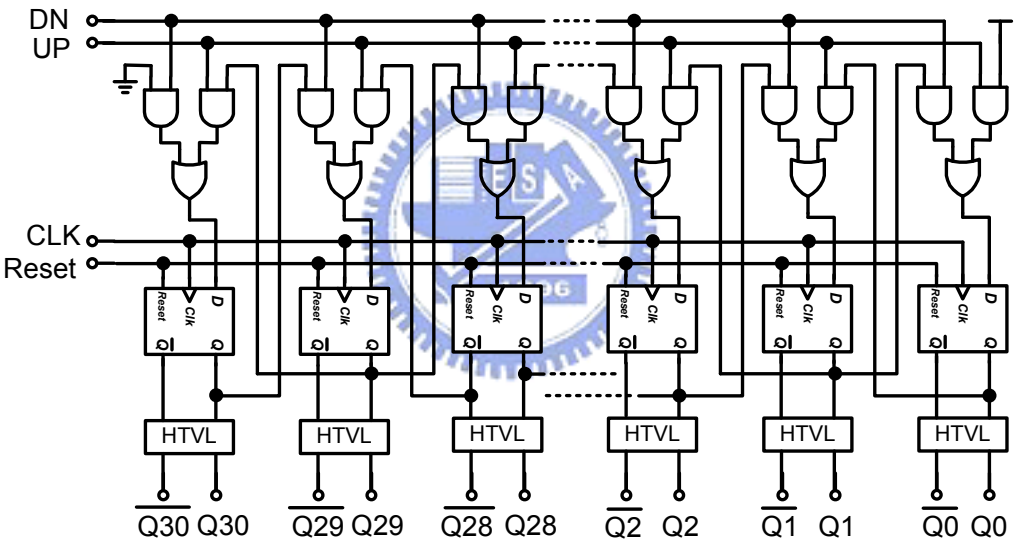


Fig. 4-9 (a) The Circuit Schematic of Comparator

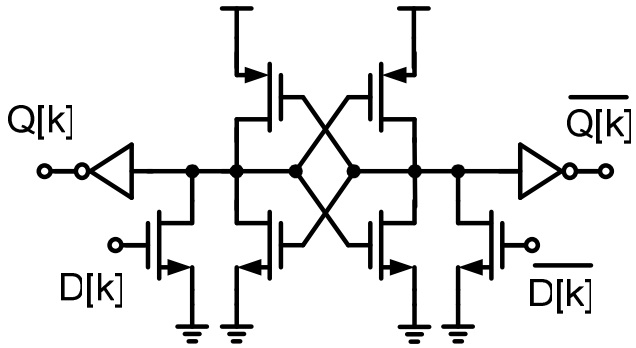
(b) The Circuit Schematic of CML-to-CMOS Buffer

4.8 Up / Down Counter

The schematic of 5-bit up/down counter is introduced in Fig. 4-10(a). Conventional Implementation is to exploit 5 registers only and the output is 5-bit binary codes with a complicated binary-to-thermometer codes (or 5-to-31-bit decoder). It costs a lot of gate delay time and wastes larger chip area. Unlike conventional architecture, our 5-bit Up/Down counter outputs directly 31 thermometer codes with 31 registers. Furthermore, the following high threshold voltage level (HTVL) revises the crossing point of rising and falling edge. The circuit schematic of HTVL is shown in Fig.4-10(b).



(a)



(b)

Fig. 4-10 (a) The Circuit Schematic of 5-bit Up/Down Counter

(b) The Circuit Schematic of High Threshold Voltage Level (HTVL)

4.9 Current-Steering DAC

Fig. 4-11 shows the schematic of current-steering Digital-to-analog converter (DAC). The output tail current is adjusted by 31 thermometer-code-controlled switching pairs. Each current cell is uniformly designed.

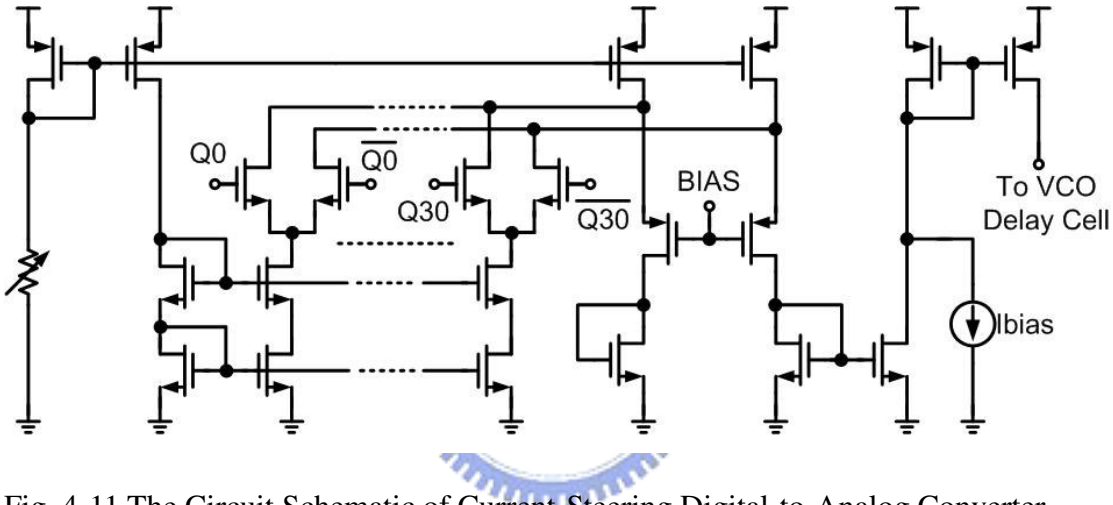
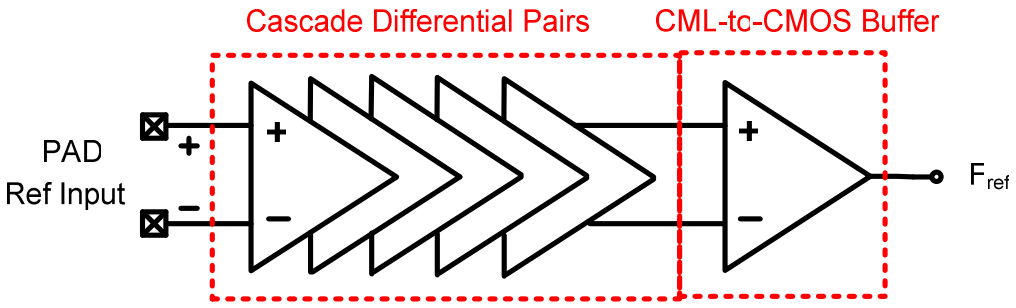


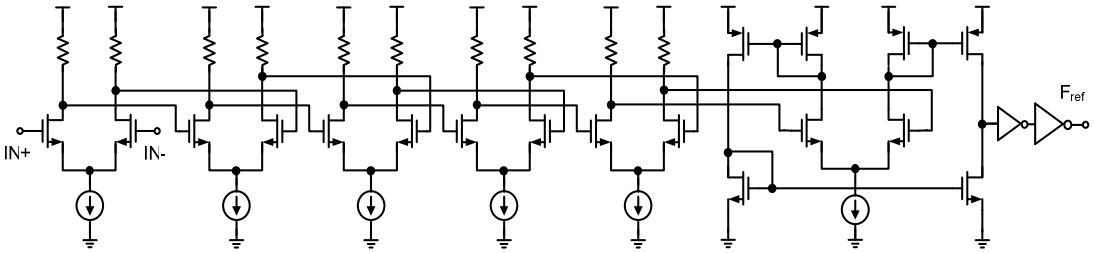
Fig. 4-11 The Circuit Schematic of Current-Steering Digital-to-Analog Converter

4.10 Reference Frequency Pre-Amplifier

The topology of reference frequency pre-amplifier, introduced in Fig. 4-12(a), acts as a input buffer while the external clock comes into the chip. The external clock weakened by passing through the input pad must be enlarged. The pre-amplifier is composed of cascade differential pairs and CML-to-CMOS buffer. The former amplifies the signal and the latter reshapes it to the full swing digital signal. The circuit schematic is illustrated in Fig. 4-12 (b).



(a)



(b)

Fig. 4-12 (a) The Topology of Reference Frequency Pre-Amplifier

(b) The Circuit Schematic of (a)

4.11 Simulation Result

Voltage-controlled oscillator (VCO) with 31 bands simulation result (TT) is shown in Fig. 4-13. By considering process variation, simulation for three corners is listed in Table II. The simulated frequency range of all three corners cover the desired output frequency. The average K_{VCO} is about 108 MHz/V. In order to guarantee the continuity of the wide-range frequency, the adjacent two bands overlap to each other up to about 50%.

Fig. 4-14 demonstrates 8 phase transient simulation result. Fig. 4-15 and Fig. 4-16 respectively show FFT simulation result @ 1.8 GHz (TT , FF, SS) and transient simulation result for whole PLL. Finally, Table III lists the performance summary for the whole PLL.

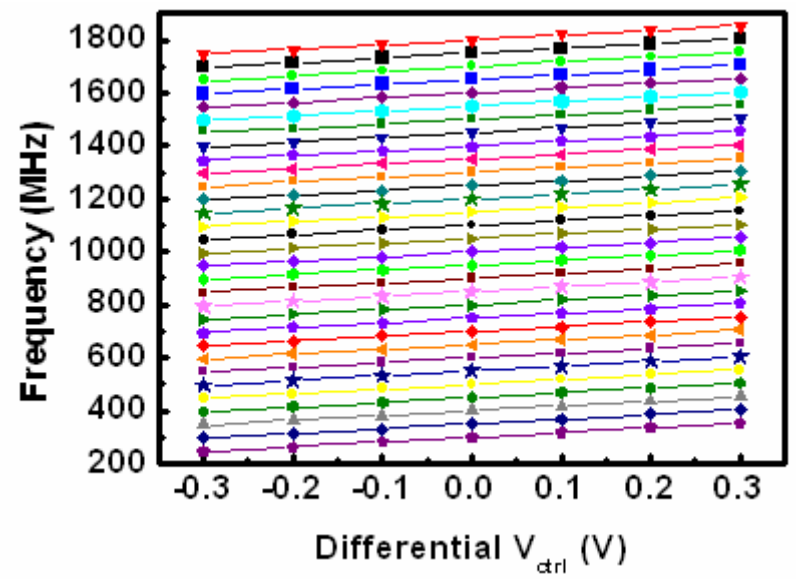


Fig. 4-13 Voltage-controlled oscillator with 31 Bands Simulation Result (TT)

Corner	Frequency Range (MHz)	K_{VCO} (MHz/V)	Overlap (%)
TT	246~1854	108	48%
FF	295~1923	121	52%
SS	193~1766	95	43%

Table 4-1 Simulation Result List for Three Corners (TT , FF , SS)

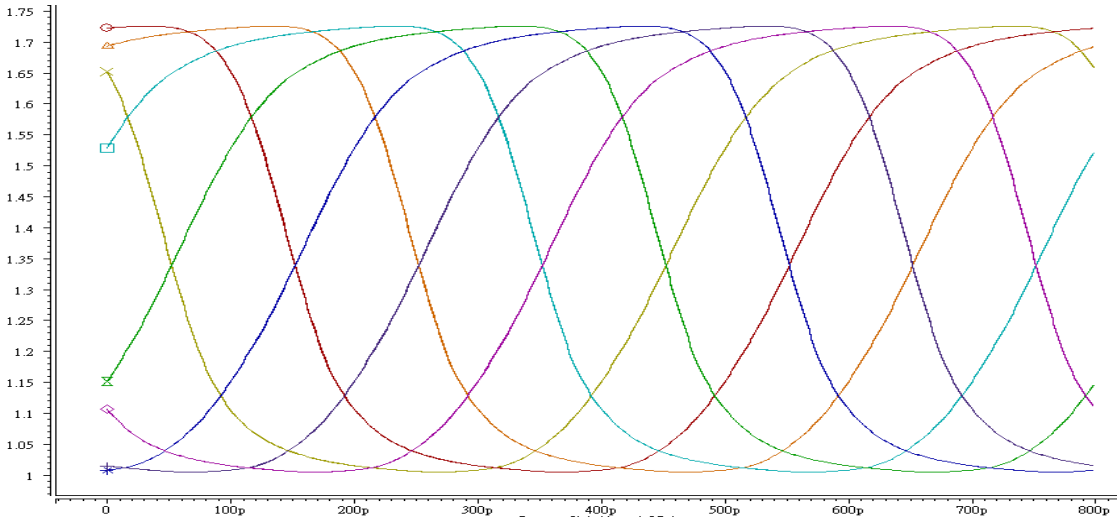


Fig. 4-14 8 Phase Transient Simulation Result

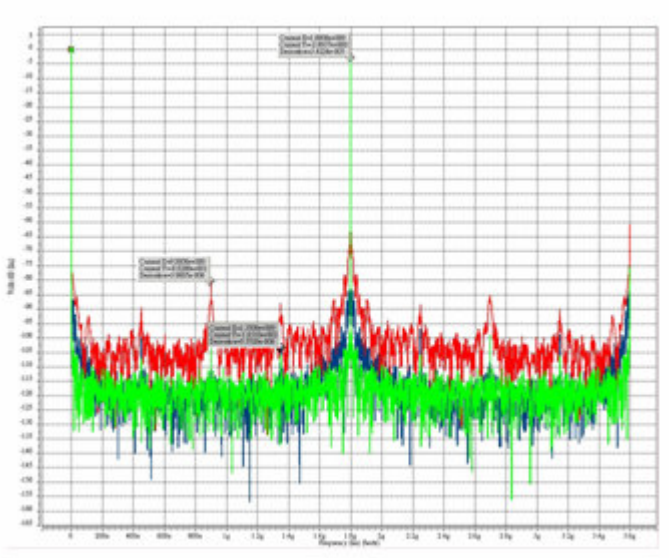


Fig. 4-15 FFT Simulation Result for Whole PLL @ 1.8 GHz (TT , FF , SS)

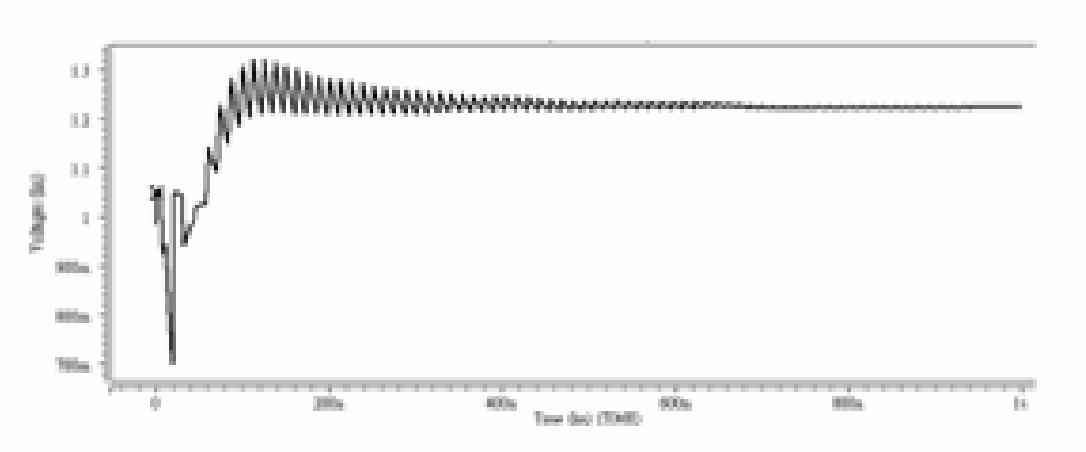


Fig. 4-16 Transient Simulation Result for Whole PLL

Function	Value
Tuning Range	246 ~ 1854 MHz (TT)
Average K_{VCO}	108 MHz/V
Power Consumption	45 mW
Lock Time	3.5 μS
Charge Pump Current	100 μA
Damping Factor	0.95

Loop Bandwidth	4~16 MHz
Control Voltage Noise	1.3 mV
Single Phase Jitter	0.2 psec
8 Phase Jitter	2.63 psec
Loop Filter	R1=5kΩ C1=25pF C2=1.68pF
Process	TSMC 0.18 μm CMOS

Table 4-2 Performance Summary for the Whole PLL