Chapter 5

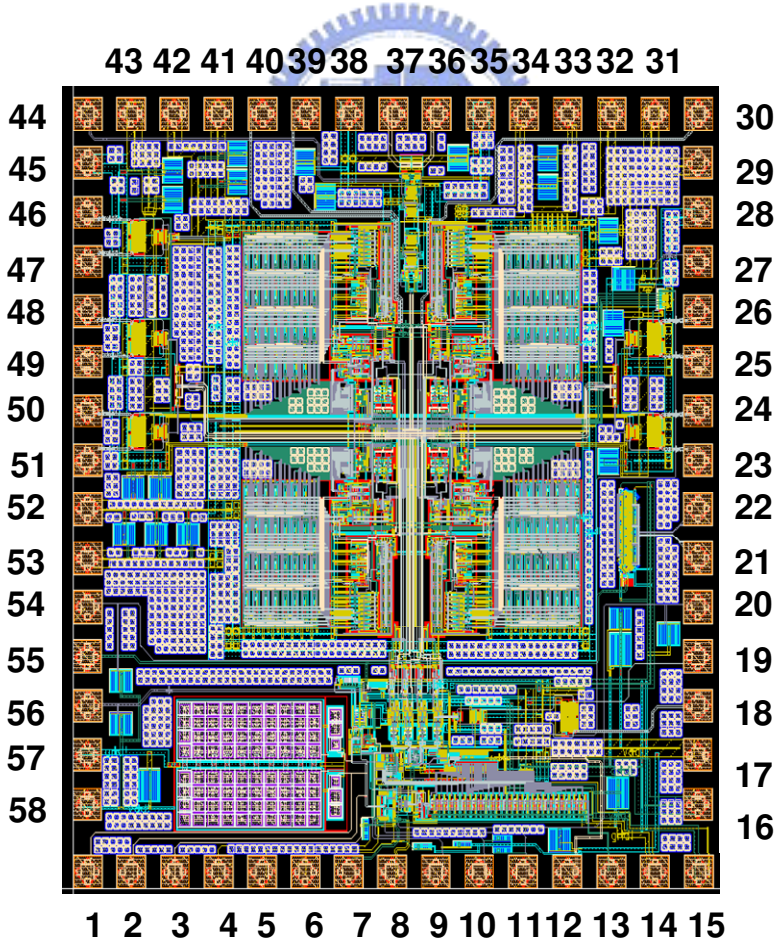
Experimental Result

5.1 Layout

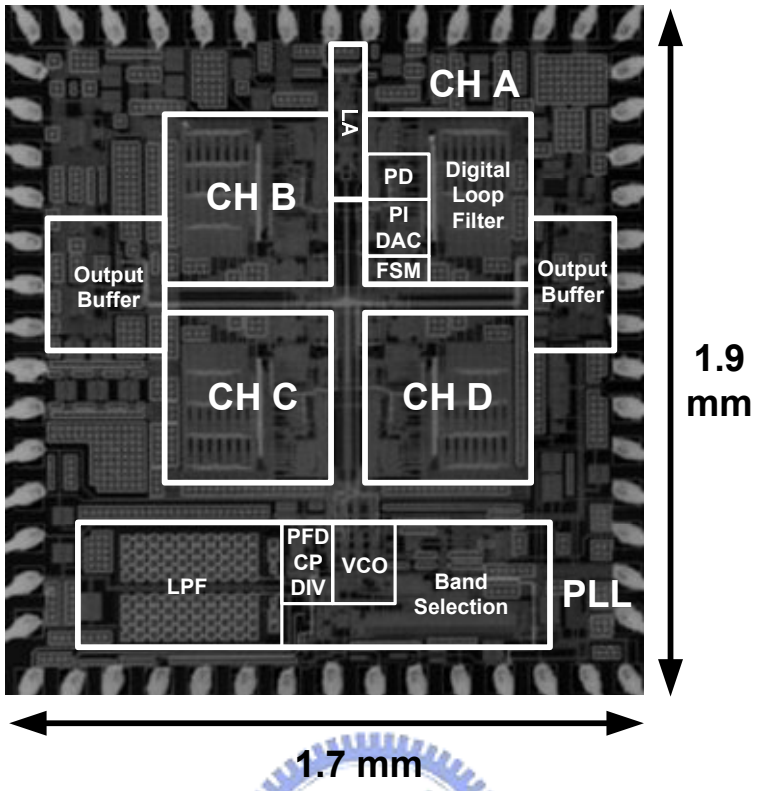
Our proposed burst-mode clock and data recovery circuit with an on-chip wide-range phase locked-loop is fabricated in standard 0.18-μm CMOS technology. Fig. 5-1(a) shows the layout for tape-out and Fig. 5-1(b) illustrates the chip photo with floor plan. The total chip area is 1.9×1.7 mm^2 including 58 pads. The chip must be

filled with the dummy cells in order to pass the DRC (design rule check) rule. Floor plan and routing must be considered carefully. This chip divides into two parts. The upper part is main CDR circuit while the lower part is PLL with band selection.

The received data is sent into chip by pad 36 and 37, and then amplify in LA. CDR core circuit has four channels to cope with data. The route of the received data, sent into each channel, should be identical in order to contribute the same delay. The recovered data is sent to the right-hand-side for channel 1 and channel 4 and is sent to the left-hand-side for channel 2 and channel 3. Moreover, PLL generates 8-phase clocks and provides whole CDR. The route of the 8-phase clocks should be identical in order to contribute the same delay to each channel in CDR core. Table 5-1 gives the pin assignment for each pad.



(a)



(b)

Fig. 5-1 (a)The Chip Layout View with 58 pins

(b) The Chip Photo View with Floor Plan

Pin	Function
1,2,3	Charge+ , Charge- , Cm
6,9,10,11,12,20,27,44,54,56	DC Bias
14,15,28,29,35,38,43,44	Analog VDD / GND
16,17,31,32,41,42,52,53	Digital VDD / GND
33,34,57,58	Guard Ring VDD / GND
4,5	CompRef+ , CompRef-
7,8,13	Band_Control , Pulse , PLL_Load
18,19	PLLout+ , PLLout-

23,24	CDRout3+ , CDRout3-
25,26	CDRout2+ , CDRout2-
46,47	CDRout+ , CDRout-
48,49	CDRout1+ , CDRout1-
50,51	CDRout4+ , CDRout4-
30,39,40	CDR Program , Loop_Pro , Load
36,37	CDR Rx Data In+ , In-
21,22,55	Div4+ , Div4- , PLL_Ref

Table 5-1 Pin Assignment

5.2 Test Consideration

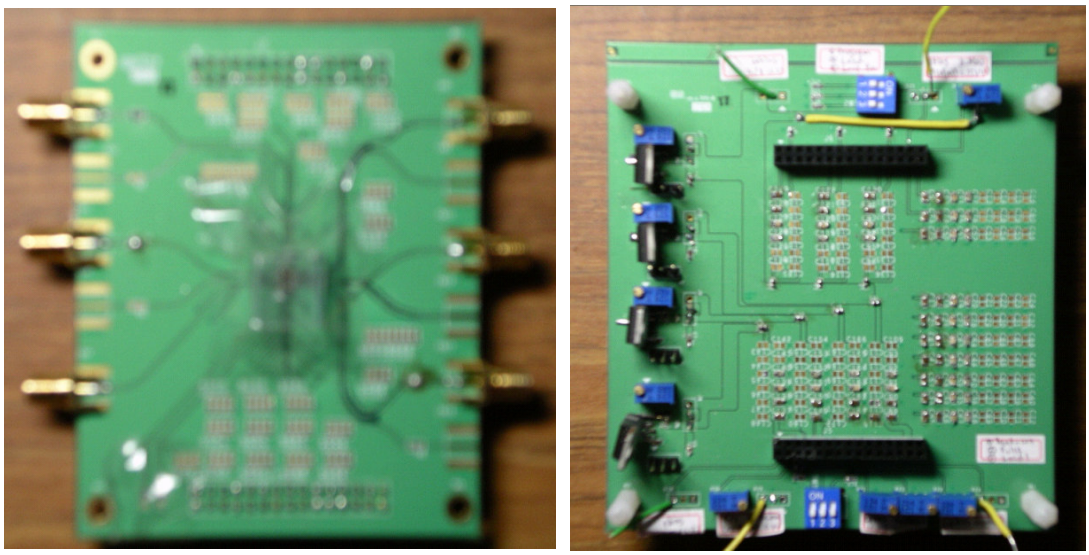
5.2.1 Testing Board

Fig. 5-2 shows the photograph of the testing board, including AC board in Fig. 5-2(a) and DC board in Fig. 5-2(b). The critical high-speed signal path, from the chip to the instruments, must be routed as short as possible in order to avoid much more parasitic effects. However, the chip needs a lot of DC bias and digital control signals, provided by the variable resistors and switches. The testing board must unavoidably occupy large area and then the high-speed signal paths increase. That is the reason why the testing board separates into two boards. The high-speed signal inputs and outputs are transmitted in the AC board. The DC board provides all DC sources for the whole chip. Thus, the critical path of high-speed signal can be shorten to eliminate

the parasitic effects. Because DC board is larger than AC board, DC board is below AC board.

AC board, demonstrated in Fig. 5-2(a), includes all AC signal tracks. Our chip is located at the center of the AC board. The bonding wires connect the chip with AC board and their inductive characteristic must be considered carefully in the whole circuit simulation. The critical high-speed or high-frequency signal paths, including CDR received data input, CDR recovered data output, PLL frequency output, and PLL reference frequency input, are routed as short as possible. The SMA terminal is utilized to send in or out the high-speed signal from the PCB board to the instrument. The track width for high-speed signal must be chosen for 17 mils, according to our board material, in order to match the 50Ω transmission line. The high-frequency signal is differential output. We can transfer differential output to single-ended output to enhance the signal by the Balun.

DC board, illustrated in Fig. 5-2(b), includes all DC signal tracks, such as power (VDD), a lot of DC bias, and digital control signal. In order to eliminate noise coupling and interference, we divide the power line into four parts. PLL has the only one power line, and then the power line of analog, digital, and guard ring are separated by inductor. All DC sources have several bypass capacitors to let the voltage stable. Moreover, the voltage regulator (LDO) is utilized for more important power line. Each DC bias is adjusted by using a variable resistor and each digital control signal is controlled by a switch, which is on for “1” or off for “0” . All DC sources on the lower DC board are provided for the chip on the upper AC board by two 30-pins jumpers.



(a) (b)

Fig. 5-2 The Top View of (a) AC Board (b) DC Board

5.2.2 Testing Environment Setup

Fig. 5-3 describes the testing environment setup. All DC sources are administered by Agilent E3610A Power Supply. Agilent N4901B Serial BERT, which has the function like an arbitrary waveform generator (AWG) and a PRBS generator, provides a data source to the chip to test. Simultaneously, a synchronized reference clock for PLL is needed in order to synchronize this PLL reference clock with the input testing data. Once the phase is locked, in other words, the phase-locked loop works, the PLL output clock phase is in-phase with reference clock phase. Therefore, it also synchronize with the input data to make the CDR system work validly. PLL output frequency is measured by Agilent E4440A Spectrum Analyzer in frequency domain. PLL output waveform and jitter performance can be demonstrated by Agilent 86100C Broadband Oscilloscope. In addition, the eye diagram of recovered data can be observed by Agilent 86100C Broadband Oscilloscope, too.

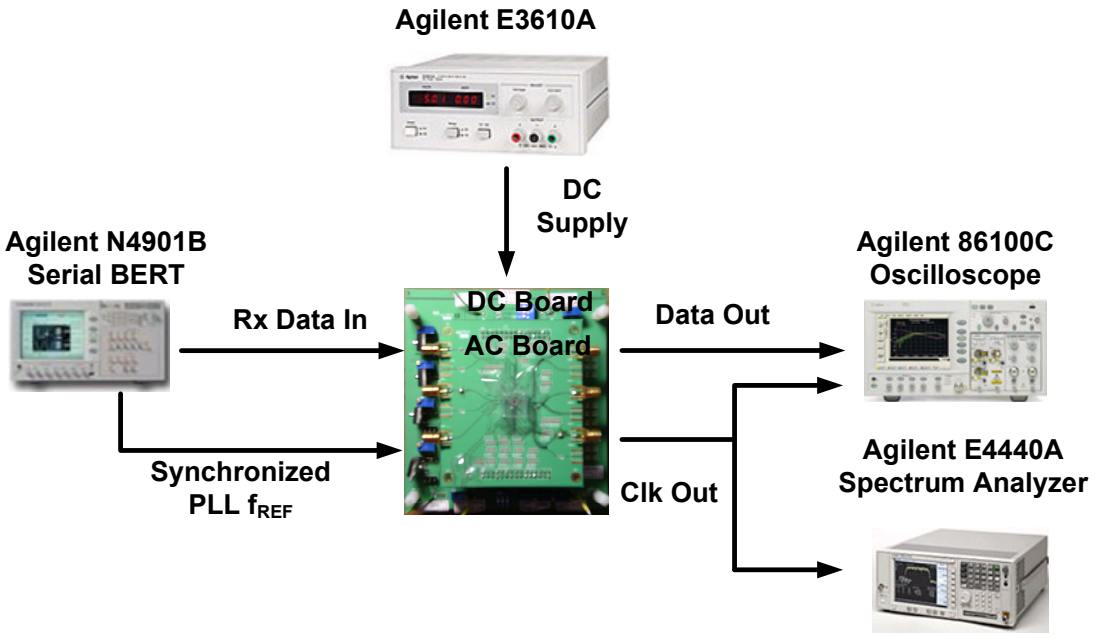


Fig. 5-3 Testing Environment Setup

5.3 Experimental Result

We show the PLL experimental result first. Our proposed PLL has a 280~1750MHz frequency range by simulation. Fig. 5-4(a) to Fig. 5-10(a) demonstrates the PLL output spectrum while PLL locks at 312MHz, 625MHz, 750MHz, 1GHz, 1.25GHz, 1.5GHz, and 1.7GHz. In order to observe the reference input spectrum, span must be adjusted to large enough. The time-domain jitter performance is measured in Fig. 5-4(b) to Fig. 5-10(b). Finally, the PLL output waveform is illustrated in Fig. 5-11(a) and Fig. 5-11(b) demonstrates the PLL output is locked with the reference input clock. The reference frequency is one-fourth the PLL output frequency.