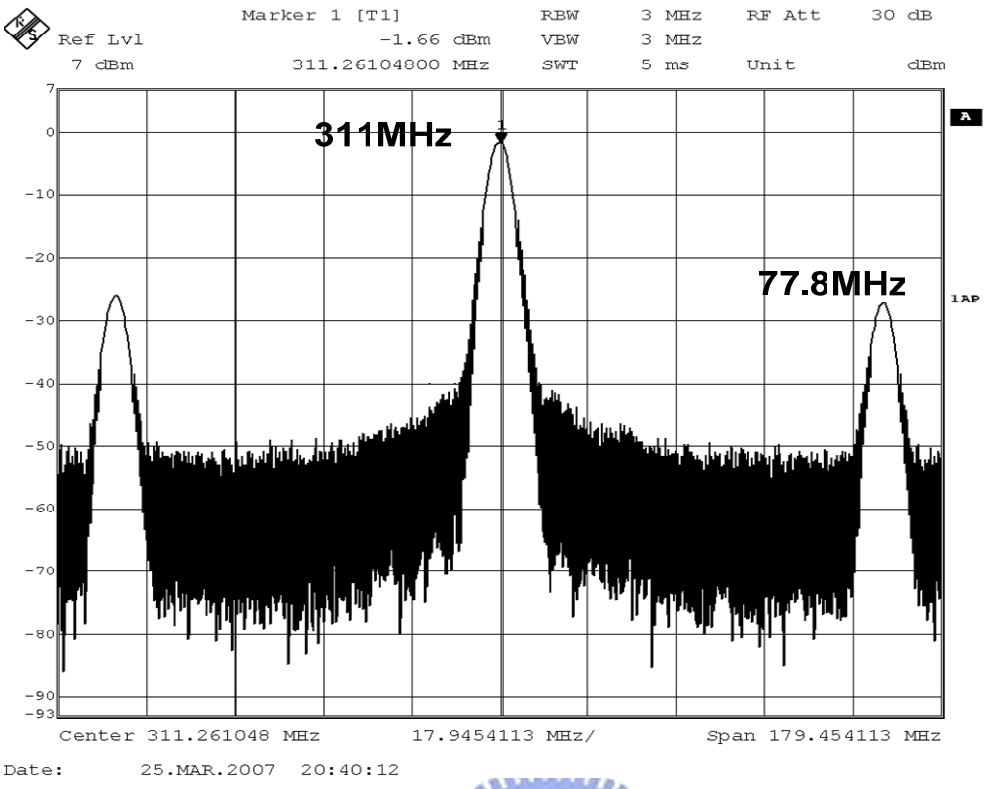
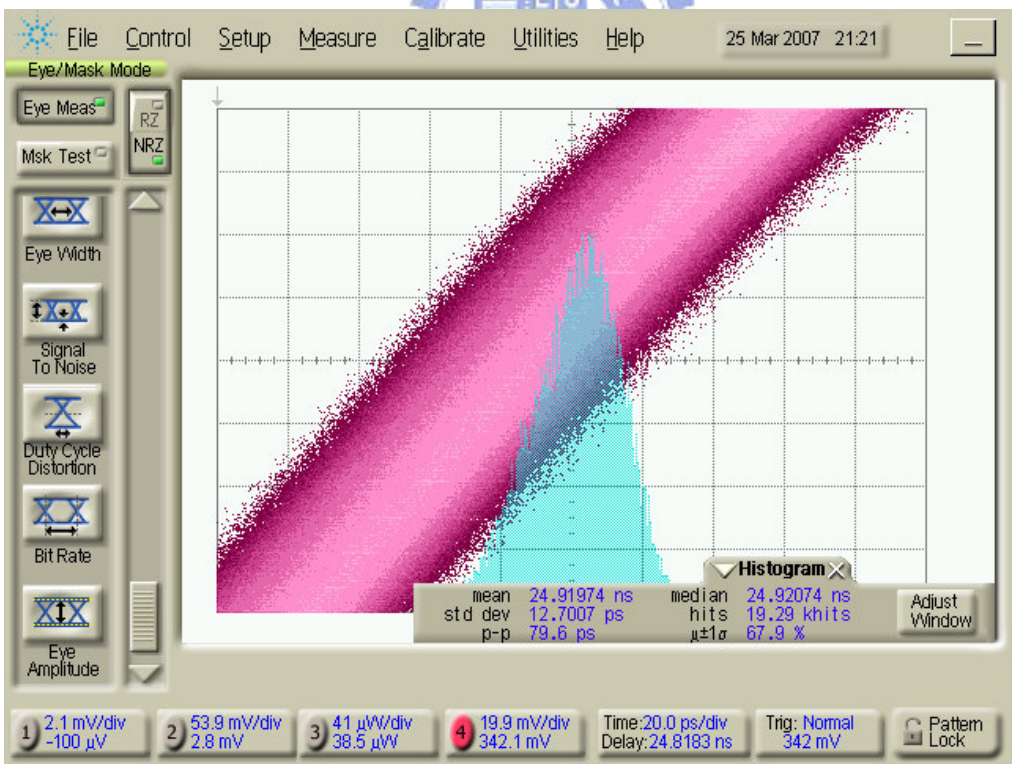
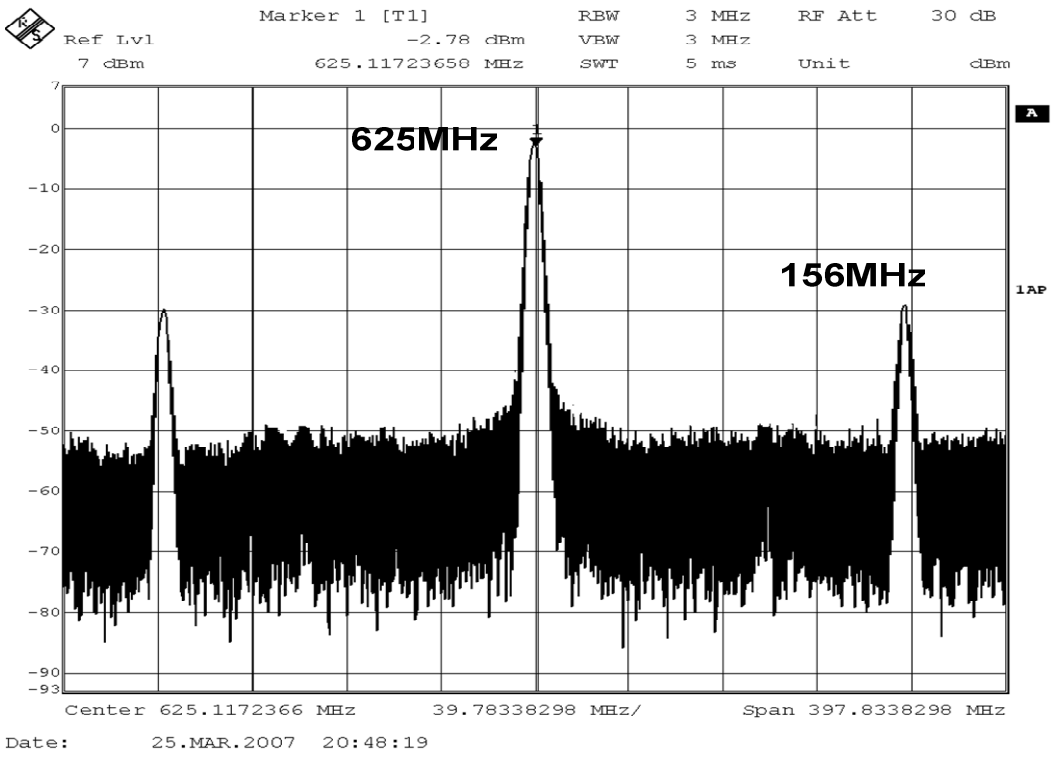


(a)

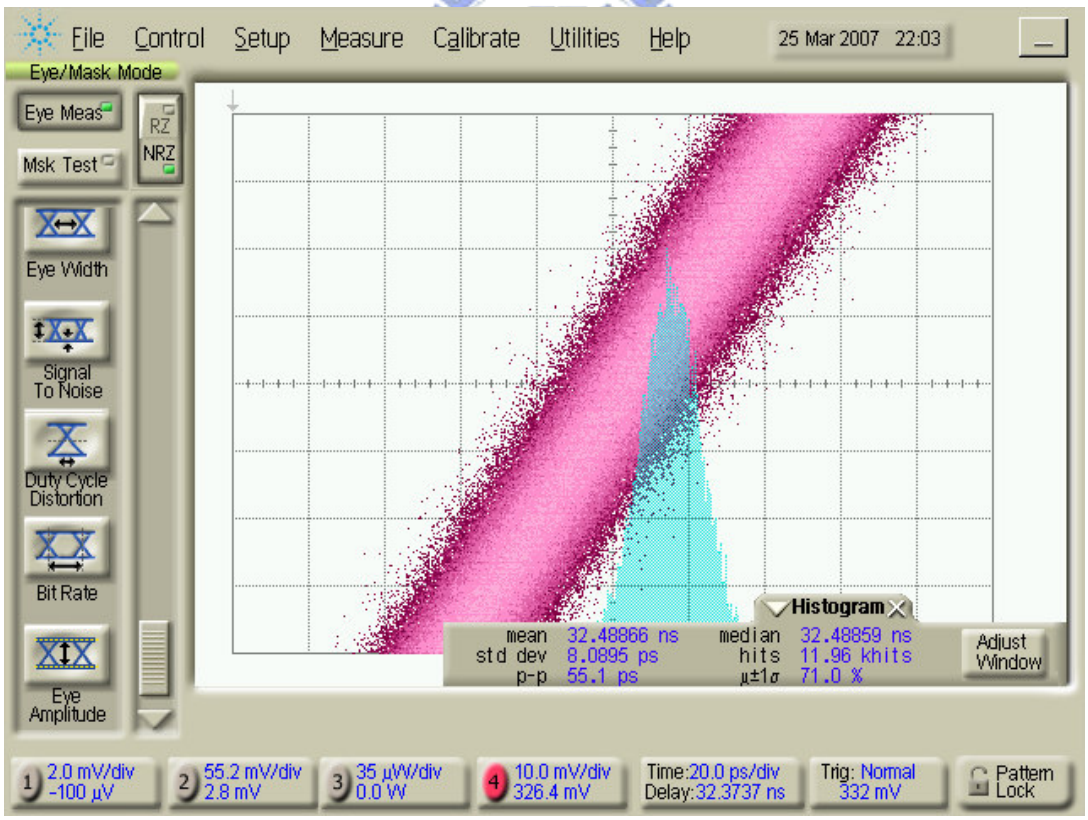


(b)

Fig. 5-4 (a) PLL Output Spectrum @ 311MHz (b) Peak-to-peak Jitter : 79.6 psec

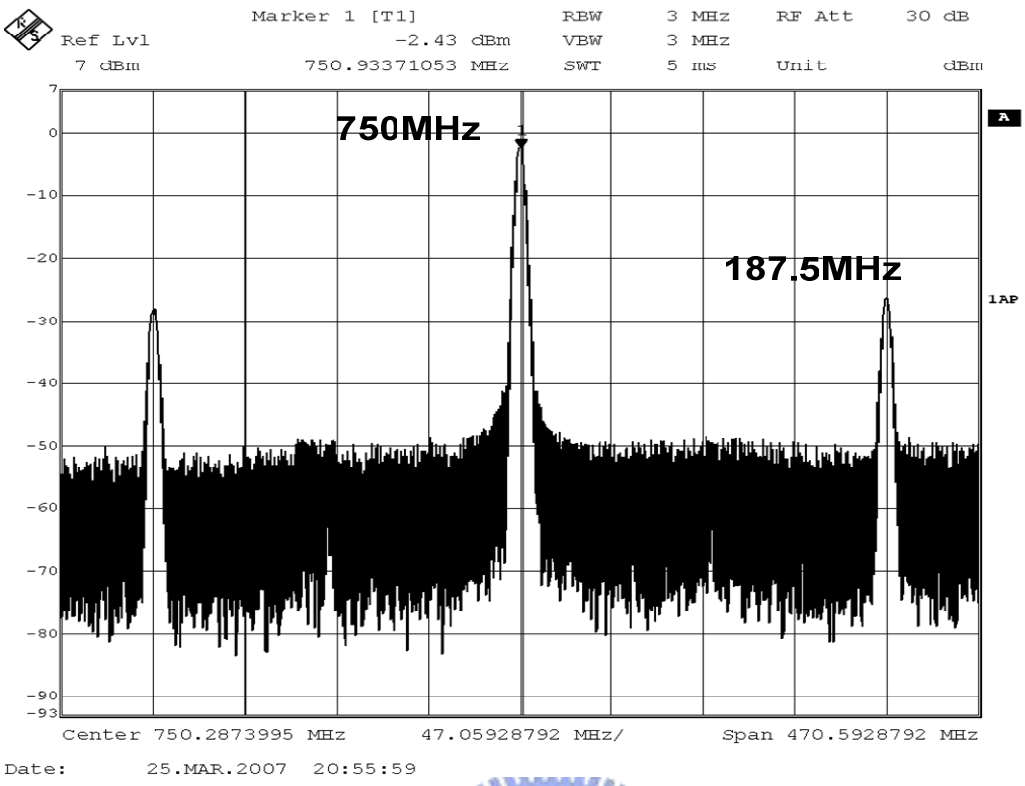


(a)

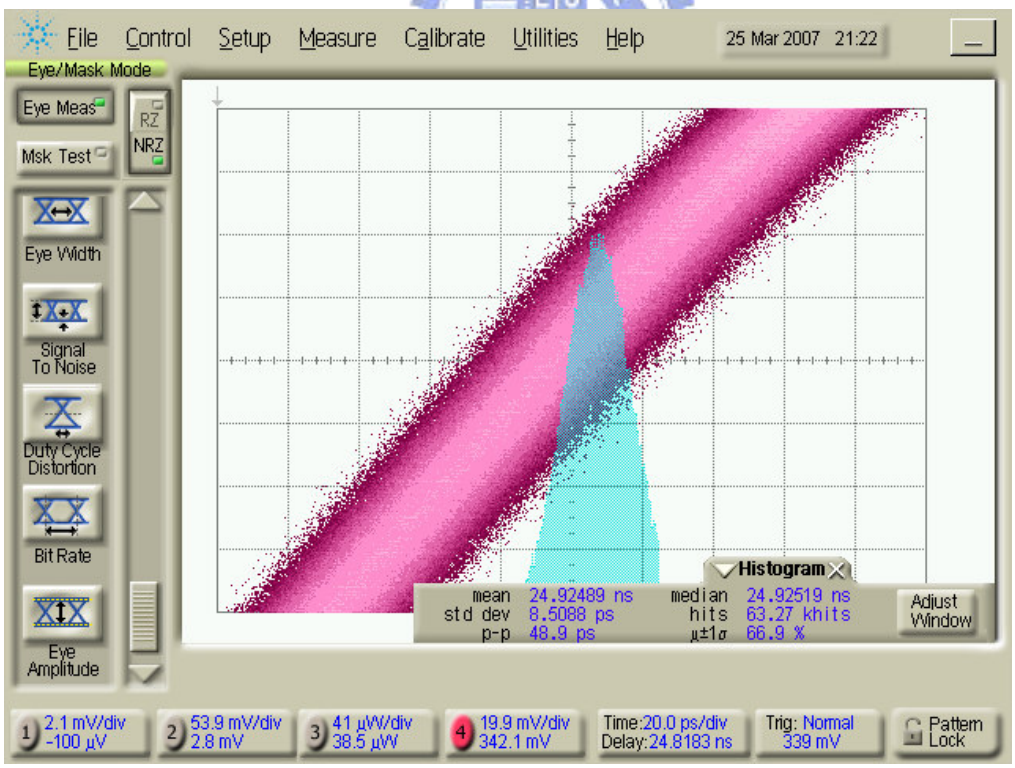


(b)

Fig. 5-5 (a) PLL Output Spectrum @ 625MHz (b) Peak-to-peak Jitter : 55.1 psec

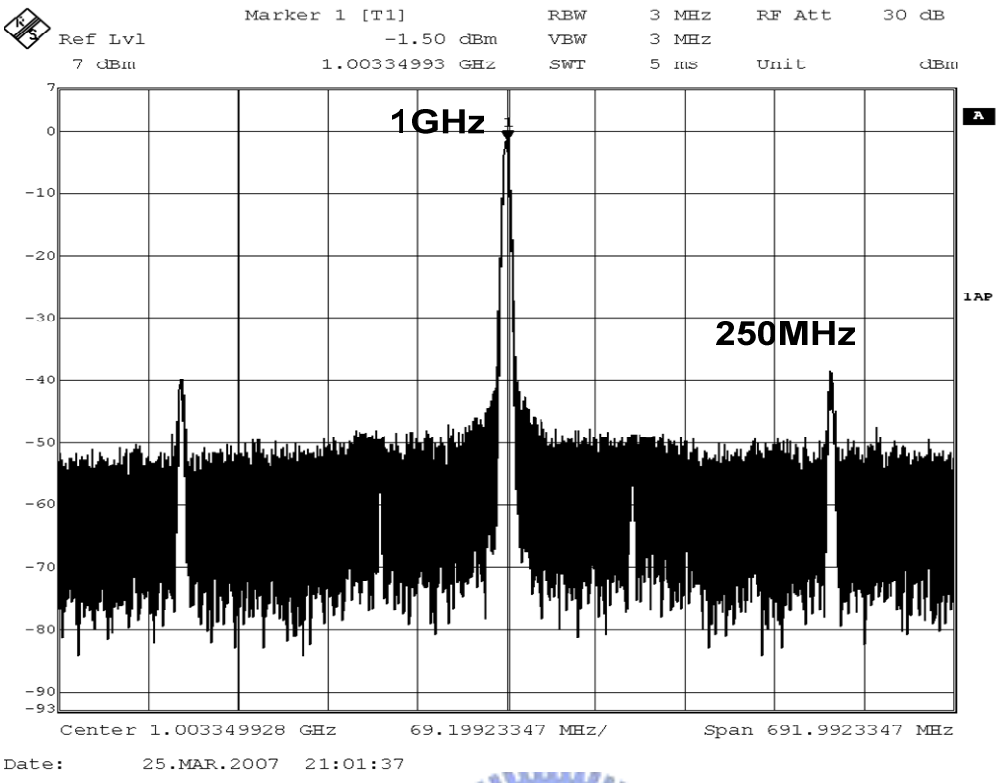


(a)

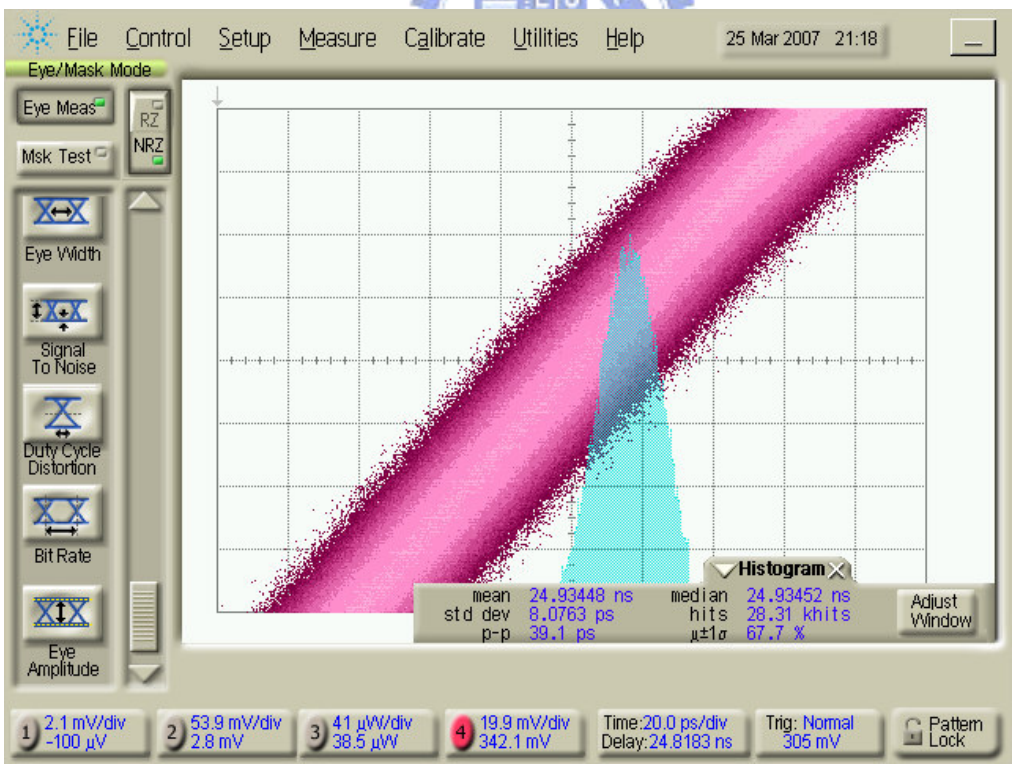


(b)

Fig. 5-6 (a) PLL Output Spectrum @ 750MHz (b) Peak-to-peak Jitter : 48.9 psec

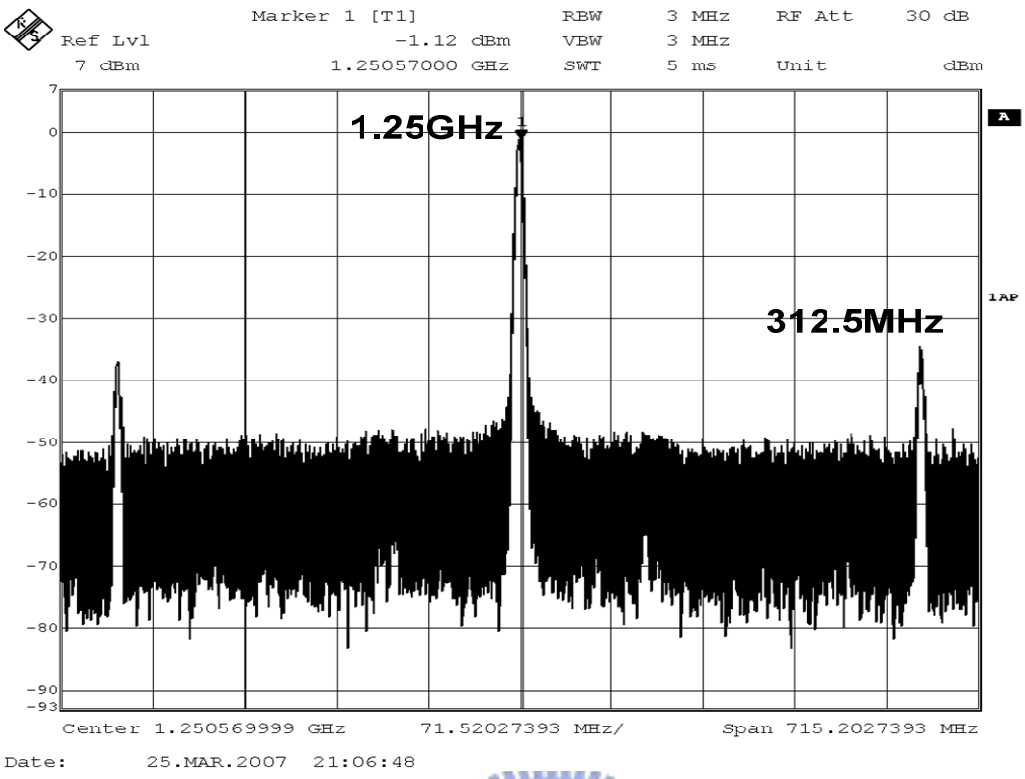


(a)

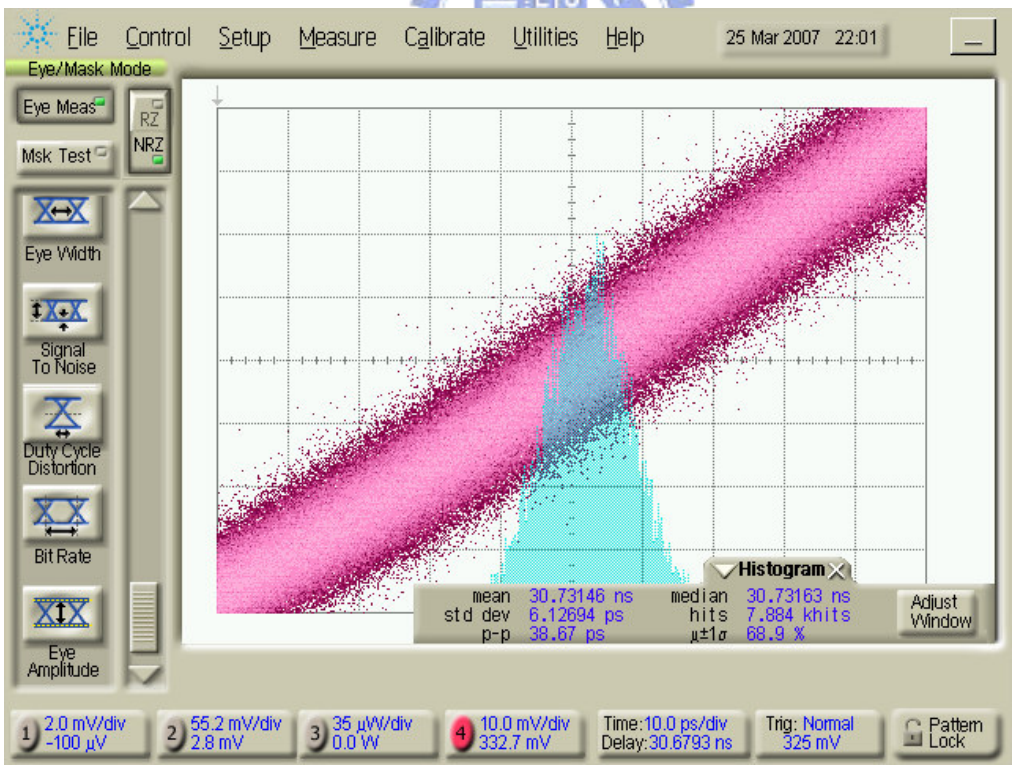


(b)

Fig. 5-7 (a) PLL Output Spectrum @ 1GHz (b) Peak-to-peak Jitter : 39.1 psec

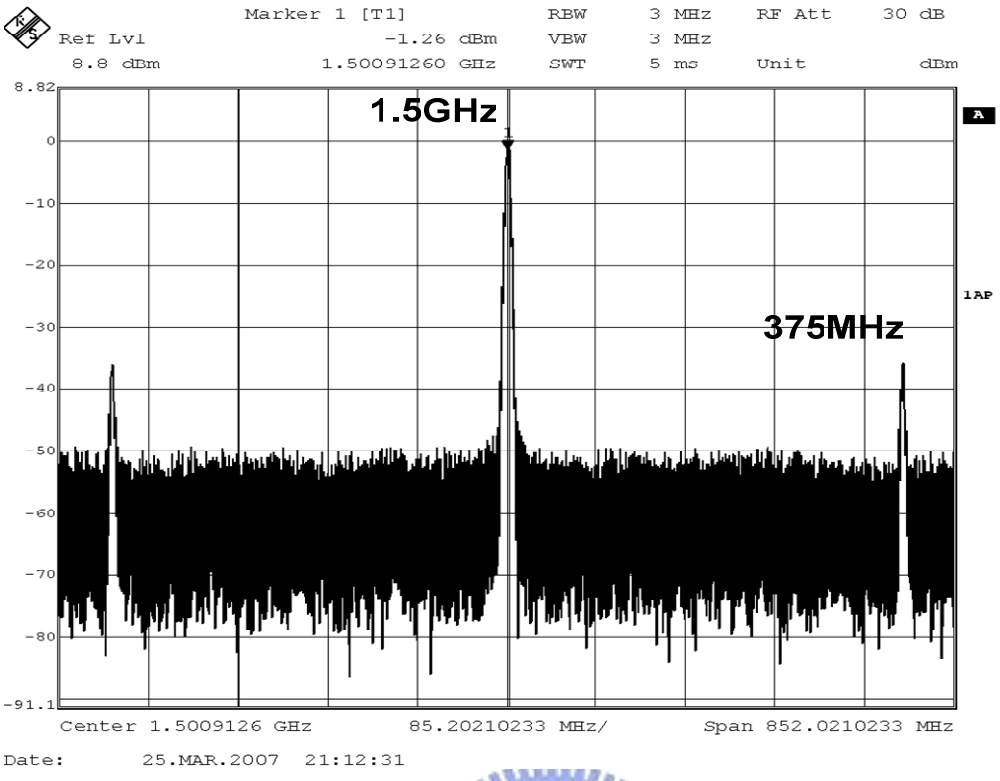


(a)

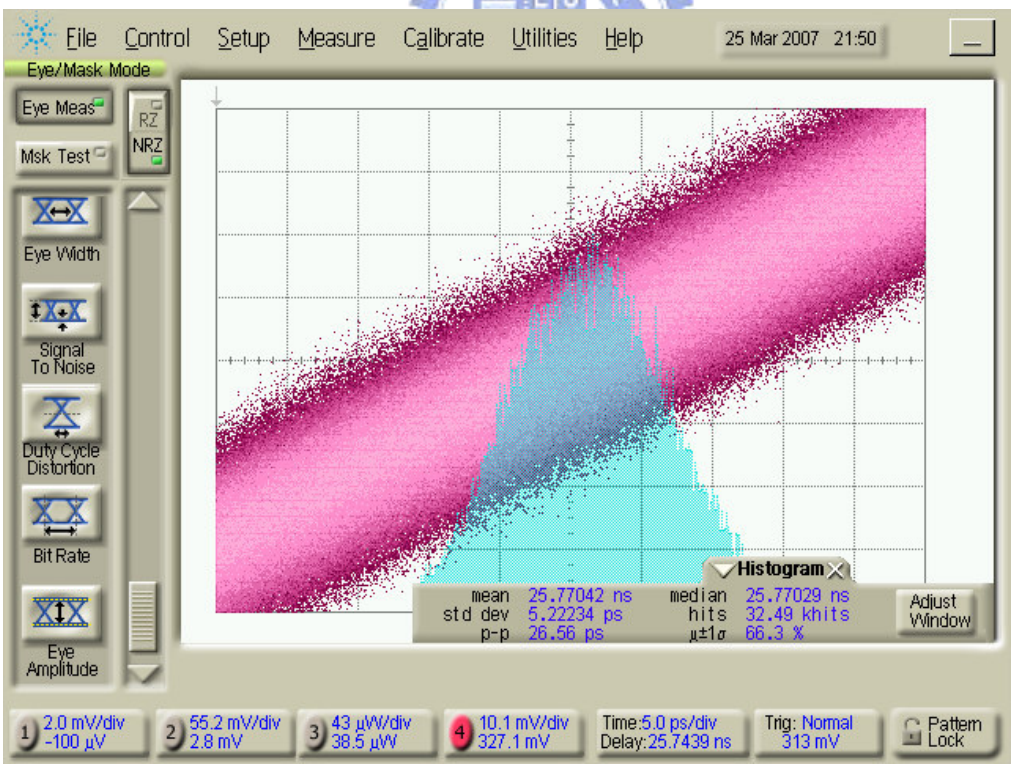


(b)

Fig. 5-8 (a) PLL Output Spectrum @ 1.25GHz (b) Peak-to-peak Jitter : 38.7 psec

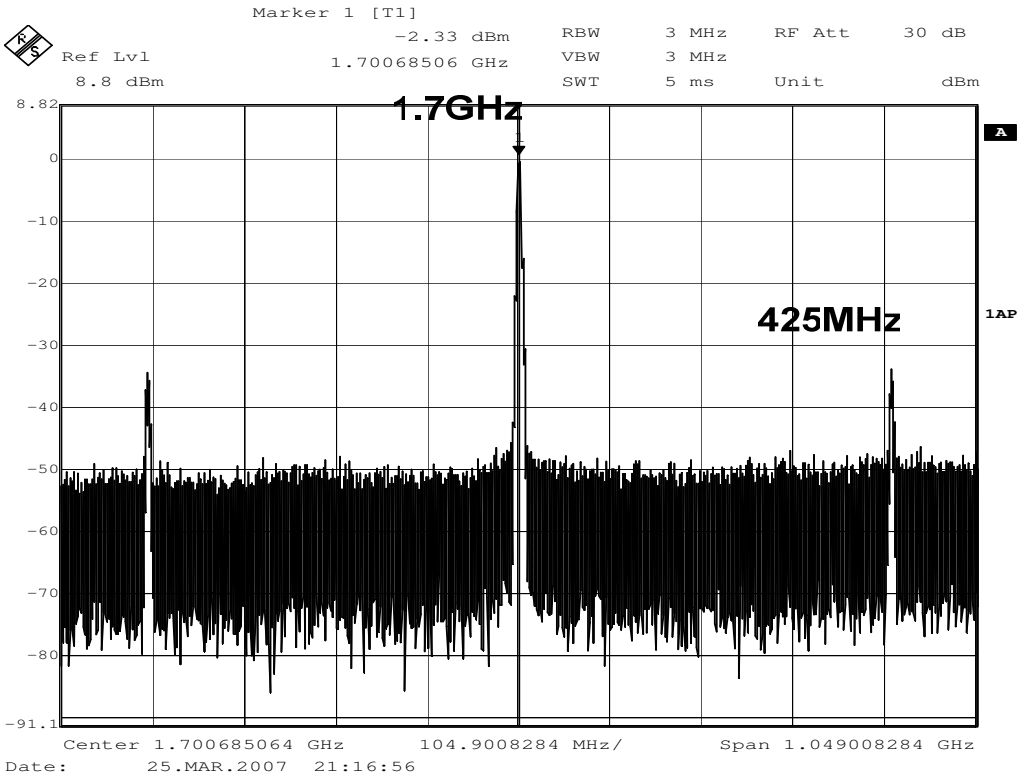


(a)

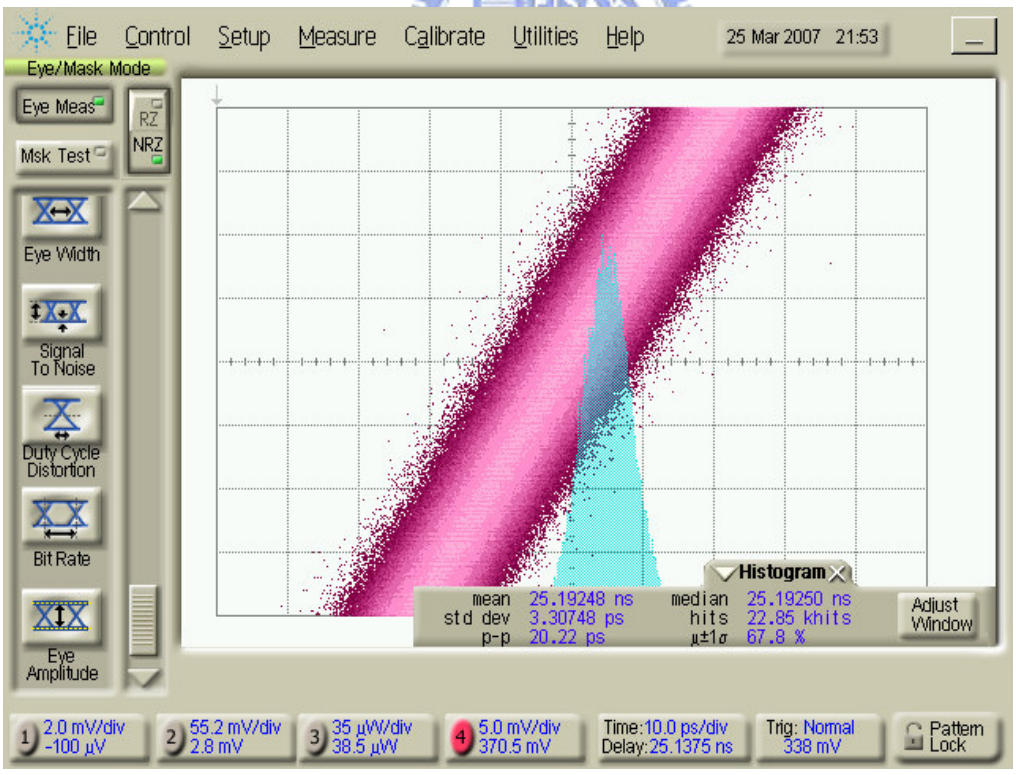


(b)

Fig. 5-9 (a) PLL Output Spectrum @ 1.5GHz (b) Peak-to-peak Jitter : 26.6 psec

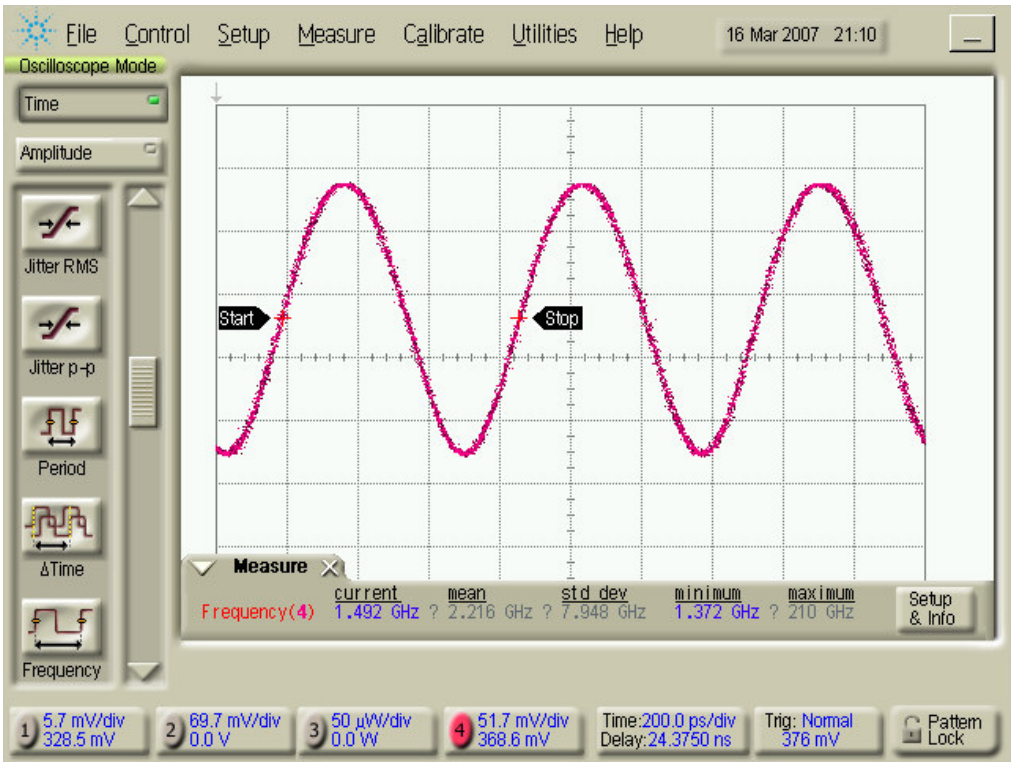


(a)

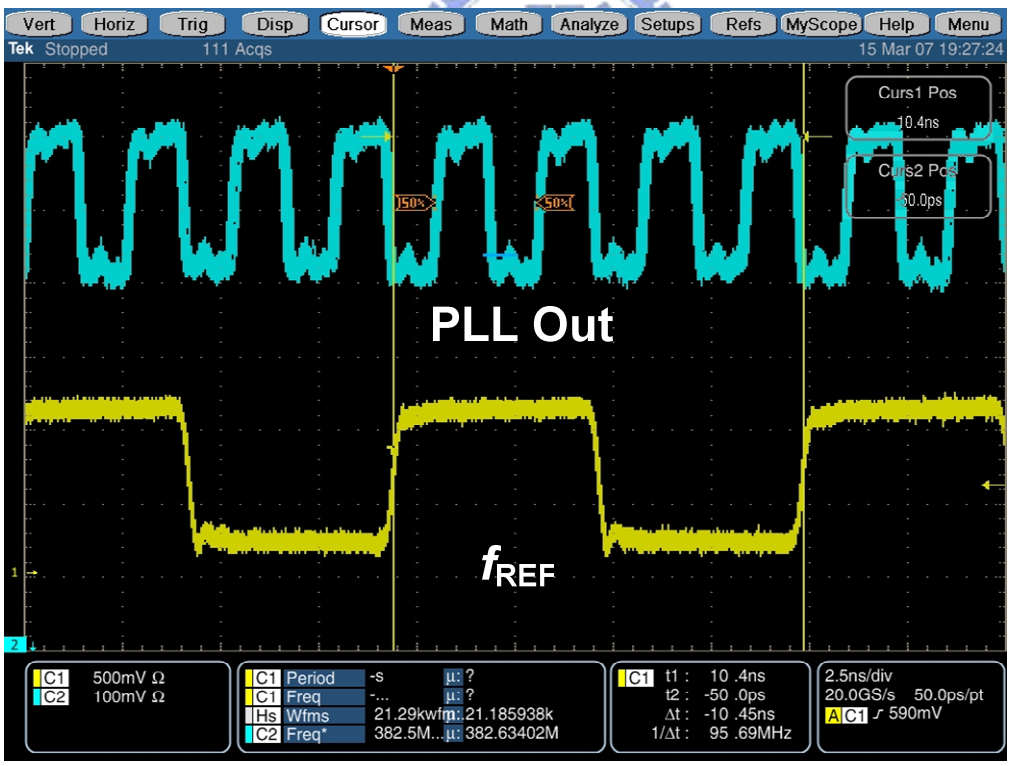


(b)

Fig. 5-10 (a) PLL Output Spectrum @ 1.7GHz (b) Peak-to-peak Jitter : 20.2 psec



(a)



(b)

Fig. 5-11 (a) PLL Output Waveform @ 1.5GHz (b) PLL Output is locked with f_{REF}

According to experimental results, the measured PLL frequency range is from 280MHz to 1.7GHz and peak-to-peak jitter range is from 20.2 psec to 79.6 psec. The higher frequency the smaller jitter performance. This trend can be explained by analyzing the PLL loop behavior. Due to PLL stability consideration, we let PLL loop bandwidth increase in proportion to the reference frequency f_{ref}. Besides , the whole PLL loop acts as a low pass filter (LPF). Thus, the higher frequency, the higher PLL loop bandwidth and naturally frequency results in the better filter performance with the fixed loop filter (LP). Table 5-2 summarizes the jitter performance and the peak-to-peak jitter to period ratio. It shows that the ratios in all frequency bands are rarely different.

Frequency (MHz)	311	625	750	1000	1250	1500	1700
Jp-p (psec)	79.6	55.1	48.9	39.1	38.7	26.6	20.2
Period (nsec)	3.22	1.6	1.33	1	0.8	0.667	0.588
Jp-p to Period Ratio	2.47%	3.4%	3.68%	3.91%	4.84%	3.99%	3.44%

Table 5-2 Jitter Performance

Chapter 6
Conclusion and Future Work

6.1 Benchmark

Table 6-1 shows the benchmark of our proposed burst-mode clock and data recovery circuit , compared with several papers.

Our CDR can operate at 1.25~6 Gbps, which is a continuous data rate. Although Ref.[44] can operate at a continuous data rate, it has a large lock time due to its

PLL-based CDR topology, as mentioned in Chapter 2. In addition, Ref.[20] is the GVCO-based CDR topology and operates at a higher data rate because it is manufactured in standard 0.13 μm CMOS technology. However, Ref.[20] utilizes a lot of inductors and has a huge occupied chip area. Its power consumption is large, too. Moreover, Ref.[43] is the oversampling-based CDR topology, so its data rate cannot be too fast due to its complexity hardware implementation, as mentioned in Chapter 2. In summary, our proposed CDR is a well-done work.

	JSSC'04 [7]	**ASSCC'05 [43]**	**ISSCC'05 [20]**	**JSSC'06 [44]**	**This Work**
Process	CMOS 0.18 μm	CMOS 0.18 μm	CMOS 0.13 μm	CMOS 0.18 μm	CMOS 0.18 μm
Power Supply	1.8 V	1.8 V	2.5 V	1.8 V	1.8 V
Data Rate (Gbps)	3.125	2.5	10	0.155~3.125	1.25~6
PLL Clock Jitter (p-p)	N.A.	N.A.	N.A.	50 ps @3125MHz	20.2 ps @1500MHz
CDR Jitter (rms)	N.A.	11.44ps @2.5Gbps	N.A.	6.4ps @3.125Gbps	N.A.
BER	$<10^{-9}$	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$	N.A.
Lock Time	>100 Bit Time	<7 Bit Time	3 Bit Time	>100 Bit Time	< 4 Bit Time
ZeroBlock(Max)	N.A.	N.A.	N.A.	N.A.	17 bits

Power Consumption	83 mW (CDR core)	70 mW (CDR core)	1.2W	95mW @3.125Gbps	45mW(PLL) 78mW(CDR) @3.125Gbps
Chip Area (mm^2)	0.6 × 0.8	1.48 × 0.92	2.5 × 2.5	1.1 × 0.8	1.7 × 1.9

Table 6-1 Burst-Mode Clock and Data Recovery Benchmark

6.2 Conclusion

A 1.25~6 Gbps Burst-Mode Clock and Data Recovery circuit is proposed. This work has R.O.C. patent granted [29] and U.S. patent pending. Its characteristics is summarized below:

(1) This burst-mode CDR is a proposed "Quarter-rate" "Four-channel" architecture. By means of "Four-channel" topology, the received serial data stream can be recovered and demultiplexed into four parallel channels. Thus no extra de-multiplexer is needed to save power consumption. "Quarter-rate" clocking technique is exploited by incorporating the on-chip wide-range phase locked-loop (PLL). The clock frequency can be reduced by a factor of 4 so as to relax the operating speed of the VCO.

(2) Sampling phase resolution in the phase interpolator (PI) is up to 1/32UI to achieve the static phase error is less than 1/32UI.

(3) Rapid phase acquisition is implemented by utilizing binary search algorithm in the dynamic digital loop filter. Binary/Linear search dual-mode operation not only reduces the lock time but also increase the data tracking ability,

which is the trade-off in the PLL-based CDR topology and GVCO-based CDR topology.

(4) We incorporate wide range PLL with bandwidth setting and band selection in our chip. All of the frequency range (300MHz~1.7GHz) can be locked. The jitter performances in all desired bands are also well.

(5) We integrate with broad-band limiting amplifier in our chip. The input sensitivity level is 30mV. Higher integration of the burst-mode receiver will be done in the future.

(6) The influence of the total jitter in our CDR system on the bit error rate (BER) is developed by jitter analysis. What is more, jitter tolerance and maximum zero blocks in our CDR system is also introduced. The mathematic model for BER and jitter tolerance is presented.

(7) Proposed bang-bang phase detector improves the operation frequency up to 6GHz while conventional architecture cannot do.

(8) Whole CDR loop behavior is verified by Verilog and Matlab Simulink and the total simulation time is saved, while only the transistor-level simulation in HSPICE costs too much time.

6.3 Future Work

In the future, burst-mode CDR with higher data rate or multi-gigabit data rate must be developed. Furthermore, high integration of the burst-mode receiver will be the trend to achieve SoC (system on chip).