Appendix A
Jitter Analysis

Bit error rate (BER) represents the quality of the communication in the communication system. It means the proportion of error occurrence while receiver receives data from transmitter. The reason of error occurrence is due to bad transmitter performance, cockamamie quality of channel, or bad receiver performance. Moreover, the main reason of bad receiver performance results from data jitter and clock jitter.

In this appendix, we will analyze the influence of jitter on our proposed CDR.

We discuss this issue into two parts. Part one introduces that the derived bit error rate due to the total jitter in our CDR influences the whole CDR performance while part two introduces that the maximum jitter tolerance performance in our CDR system with different zero block does not results in error. In addition, jitter transfer and jitter generation is also introduced.

According to the origin, jitter can be separated into two kinds: Random jitter (RJ) and deterministic jitter (DJ). Random jitter is represented as unbounded components and usually expressed its statistical behavior by Gaussian distribution. Oppositely, deterministic jitter is represented as bounded components and cannot be expressed by Gaussian distribution. Random jitter originates from thermal noise of the electronic devices while deterministic jitter originates from pattern jitter, Inter-Symbol Interference (ISI), or duty cycle distortion. Generally speaking, random jitter is represented by root-mean-square (RMS) value or standard variation while deterministic jitter is represented by peak-to-peak value. When we want to combine this two kinds of jitter to calculate the total jitter, we should do convolution with the probability density function (PDF) of random jitter and deterministic jitter instead of adding two values directly.

A.1 Bit Error Rate Analysis

First, we represent several non-ideal effects in our CDR architecture in Fig. A-1. Because of integrating two-stage limiting amplifier (LA) in the front of CDR loop, received data is amplified to digital signal. Amplitude noise and voltage variation eliminate and can be neglected. Thus, we analyze the bit error rate without considering only the timing error, or jitter. We can briefly observe our CDR suffers some jitter, such as data jitter (T_{jd}), clock jitter (T_{jc}), and sampling timing offset (T_{os}). We can define the timing margin (T_{margin}) as:

$$T_{margin} = \frac{T_{bit}}{2} - T_{os} - T_{jc} - T_{jd} \tag{A-1}$$

The larger the timing margin (T_{margin}), the smaller error probability of sampled data, and vice versa. Sampling timing offset (T_{os}) represents the phase offset between sampling phase and the center of the data. The larger the sampling timing offset, the smaller error occurrence. Data jitter (T_{jd}) depends on the performance of transmitter, channel, and receiver while clock jitter (T_{jc}) depends on the performance of phase-locked loop. Data jitter consists of both random jitter and deterministic jitter while clock jitter is composed of only random jitter. If the timing margin T_{margin} decreases due to these jitter, bit error rate will increase.

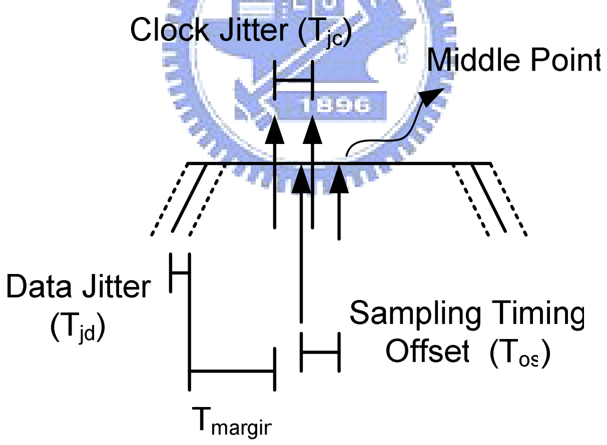


Fig. A-1 All Kinds of Jitter in Whole CDR System

The sampling timing offset T_{os} relates to the number of sampling phase in a bit time, or unit interval (UI). It also means the step number of our phase interpolator (PI) and called the resolution of the phase interpolator, k. The larger the resolution of the phase interpolator k, the smaller the sampling timing offset T_{os} and the smaller bit error rate. However, if k is larger, the more hardware complexity will be needed and power consumption and occupied area will be larger. That is a significant trade-off.

We discuss the influence of sampling timing offset on bit error rate first. The worst case of sampling data is that the center point of data falls on the center of optimum two sampling phases. We define as the maximum sampling timing offset $T_{os,max}$:

$$T_{os,\max} = \frac{T_{bit}}{2 \times k} \tag{A-2}$$

where k is the resolution of the phase interpolator. (A-2) is the expression while k is odd. If the center point of data does not fall on the center of optimum two sampling phases, CDR system will choose the sampling phase which is nearer the data center. If data rate in transmitter and receiver has some frequency offset, the value of T_{os} will be between 0 and T_{bit}/2k and its probability density function (PDF) is uniform distribution.

First, we discuss the influence of random jitter of the input data on bit error rate. we define random jitter as a Gaussian distribution with given mean and variance σ_d and normalize the bit time to one. Therefore, the bit error rate can be expressed as:

$$LBER = TD \times \int_{st}^{\infty} \frac{1}{\sqrt{2\pi\sigma_d^{\,2}}} \exp(-\frac{t^2}{2\sigma_d^{\,2}})dt \tag{A-3}$$

$$RBER = TD \times \int_{-\infty}^{st} \frac{1}{\sqrt{2\pi\sigma_d^{\,2}}} \exp(-\frac{(t-1)^2}{2\sigma_d^{\,2}})dt \tag{A-4}$$

$$TBER = LBER + RBER \tag{A-5}$$

where LBER and RBER represents the bit error rate caused by random jitter of the left-side boundary and the right-side boundary of the input data, respectively. TBER represents the total bit error rate caused by random jitter of the input data. St is the sample point and TD is the data transition density and yields a value of 1 for a

“1010 ….” and 1/2 for a PRBS pattern.

Next, we discuss deterministic jitter of the input data. The probability density function (PDF) of deterministic jitter can be defined as a dirac function (impulse response) in order to briefly analyze its characteristic. Therefore, the PDF of deterministic jitter can be expressed as:

$$DJ = a1 * \delta(t - w1) + a2 * \delta(t + w2) \qquad \text{(A-6)}$$

where w is deterministic peak-to-peak jitter and a1 and a2 are the right-side and left-side probability of dirac function, where a1+a2=1.

We can obtain the PDF of the input data jitter ($\mathrm{PDF}_{\mathrm{data}}$) by doing convolution with the PDF of deterministic jitter and random jitter, as illustrated in Fig. A-2.

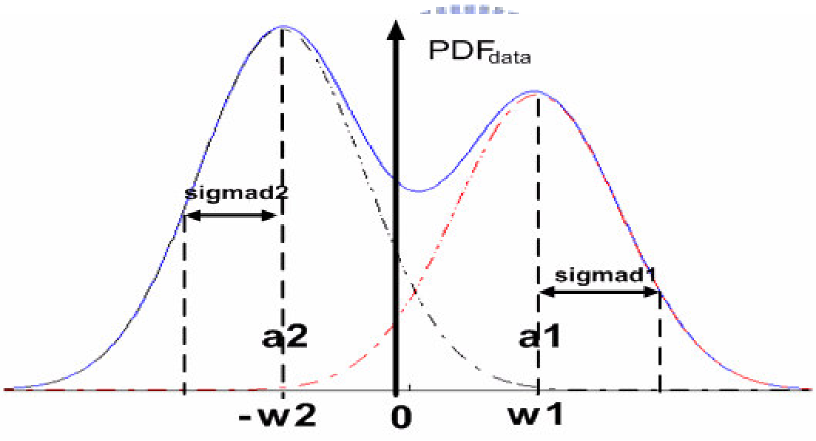


Fig. A-2 The Probability Density Function of the Input Data Jitter

After analyzing the influence of input data jitter on bit error rate, we discuss the influence of sampling clock jitter on bit error rate. Clock jitter can be represented as a random jitter. Thus, we describe the PDF of clock jitter ($\mathrm{PDF}_{\mathrm{clk}}$) as a Gaussian distribution and it is shown as:

$$PDF_{clk}(st, \sigma_c) = \frac{1}{\sqrt{2\pi\sigma_c^{\ 2}}} e^{-\frac{(st-0.5)^2}{2\sigma_c}} \qquad \text{(A-7)}$$

Furthermore, the sampling timing offset T_{os} which is caused by clock sampling also affects on bit error rate. The PDF of the sampling timing offset T_{os} ($\mathrm{PDF}_{\mathrm{os}}$) can be expressed as a Uniform distribution between 0 and 1/2k and shown as:

$$PDF_{os}(t,k)=\{\begin{matrix} k,-1/2k<t<1/2k \\ 0, \qquad others \end{matrix} \tag{A-8}$$

As the same as before, we can combine (A-7) and (A-8) by doing convolution with them . Then we express the PDF as:

$$u(st,k,\sigma_c)=PDF_{clk}*PDF_{os}=k\int_{\frac{-1}{2k}}^{\frac{1}{2k}}\frac{1}{\sqrt{2\pi}\sigma_c}e\frac{-(st-t-0.5)^2}{2\sigma_c{}^2}dt \tag{A-9}$$

Finally, after combining (A-3), (A-4), (A-6), and (A-9), we can calculate the total bit error rate, as shown below:

$$LBER=\frac{TD}{2}\cdot\int_{-\infty}^{\infty}\int_{st}^{\infty}\frac{1}{\sqrt{2\pi}}\left(\frac{a1}{\sigma_{d1}}e^{-\frac{(x-w1)^2}{2\sigma_{d1}^2}}+\frac{a2}{\sigma_{d2}}e^{-\frac{(x-w2)^2}{2\sigma_{d2}^2}}\right)u(st)dxdst \tag{A-10}$$

$$RBER=\frac{TD}{2}\cdot\int_{-\infty}^{\infty}\int_{-\infty}^{st}\frac{1}{\sqrt{2\pi}}\left(\frac{a1}{\sigma_{d1}}e^{-\frac{(x-1-w1)^2}{2\sigma_{d1}^2}}+\frac{a2}{\sigma_{d2}}e^{-\frac{(x-1-w2)^2}{2\sigma_{d2}^2}}\right)u(st)dxdst \tag{A-11}$$

$$TBER=LBER+RBER \tag{A-12}$$

We observe (A-10) and (A-11) preciously, where *u(st)* is derived from (A-9). The most important parameter in (A-9), which is explained the influence of sampling timing offset T_{os} on the total bit error rate (TBER), is phase interpolator resolution (k). For a specific transmission environment and a local clock generator with given performance, clock jitter and data jitter in the whole CDR system is almost fixed. It implies that phase interpolator resolution (k) dominates the total bit error rate. Thus, for a given and fixed data jitter and clock jitter, for example, a Gaussian distribution with 0.1UI variance respectively, we can describe the relationship between bit error rate BER and phase interpolator resolution (k), as shown in Fig. A-3. As our expectation, if phase interpolator resolution k is higher, bit error rate BER will be decrease. However, the trend approaches to saturation. In order to achieve the total bit error rate less than 10^{-12} and make reservation for some margin, we design k=32 for our CDR system. Therefore, when CDR is in the lock condition, the static phase offset, or called static phase error, will be less than 1/32UI, as mentioned in section 3.1. If we choose k=64, more hardware complexity and more power consumption is inevitable.

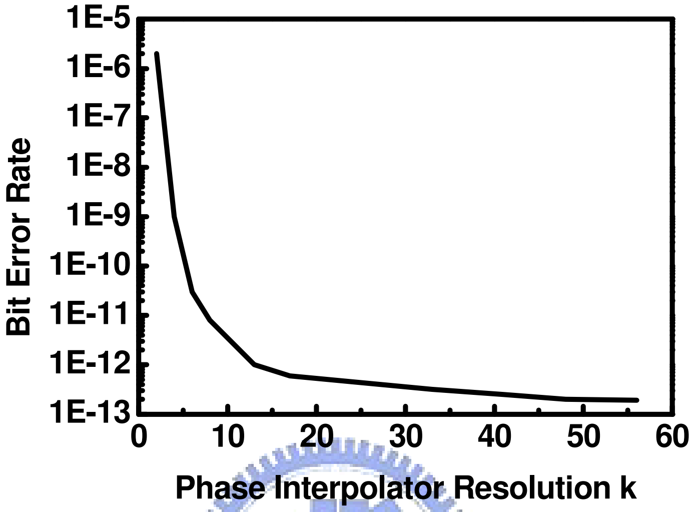


Fig. A-3 Bit Error Rate (BER) versus Phase Interpolator Resolution (k)

A.2 Jitter Tolerance

In this section, we discuss our CDR system can stand for how much jitter until error occurrence. We assume that the frequency of noise varies in the form of sinusoidal waveform and this jitter frequency modulates the input data rate by frequency modulation (FM), as illustrated in Fig. A-4. When the receiver receives sequential ones or zeros, CDR cannot change sampling phase because there is no data transition. CDR could make a mistake in this interval because data rate is affected by noise modulation.

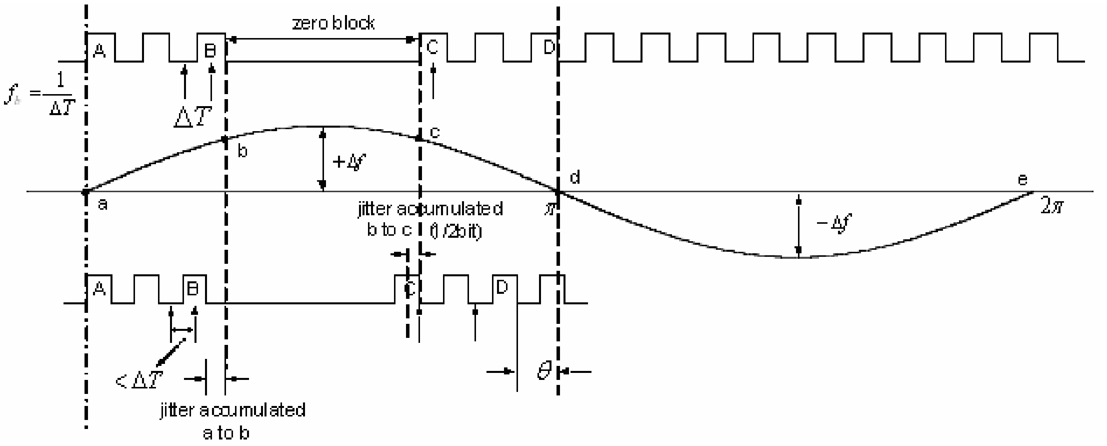


Fig. A-4 The Jitter Frequency modulates the Data Rate (I)

As shown in Fig. A-4, the top signal is the data which is not interfered by noise, the middle signal is noise, and the nethermost is the data which is modulated by jitter. In the interval a to d, the jitter frequency variation is positive and data rate becomes higher after data is modulated by jitter. On the other hand, in the interval d to e, the jitter frequency variation is negative and data rate becomes slower.

In the interval b to c, the transmitter transmits a stream of zero, called “zero block” or “zero run”. There is no data transition, so CDR cannot modify the sampling phase. For this reason, phase detector or sampler in CDR could sample the last data or the next data and CDR makes a mistake. In the interval a to b, even if data rate always changes, there is theoretically no error occurrence as long as frequency variation is not too fast. That is because the sampling phase always changes along with data rate. Hence, the sampling phase always falls on the data center . In the general condition, the sampling phase should fall on the data center when sampling the data C. Nevertheless, because there is no data transition in the interval b to c, the sampling phase cannot be modified and error could occur. If the timing margin of the data is over 1/2UI, the sampling phase will fall on another data.

After learning the above concepts, we start to calculate jitter tolerance. We separate into two conditions to discuss. The first condition is when the jitter frequency is just a little slower than the data rate or almost the same. Because there is no data transition in the half period where jitter frequency always varies, the error occurs if the peak-to-peak jitter is more than 1/2UI. Thus, in this condition, jitter tolerance is 1/2UI.

The second condition is when the jitter frequency is much slower than the data rate. Fig. A-5 describes the variation of data rate after modulated by jitter frequency. f_b is the original data rate and f_j is the jitter frequency. x represents the bit number of data among 0 to π while n represents the zero block number. The gray part is the region where is no data transition.

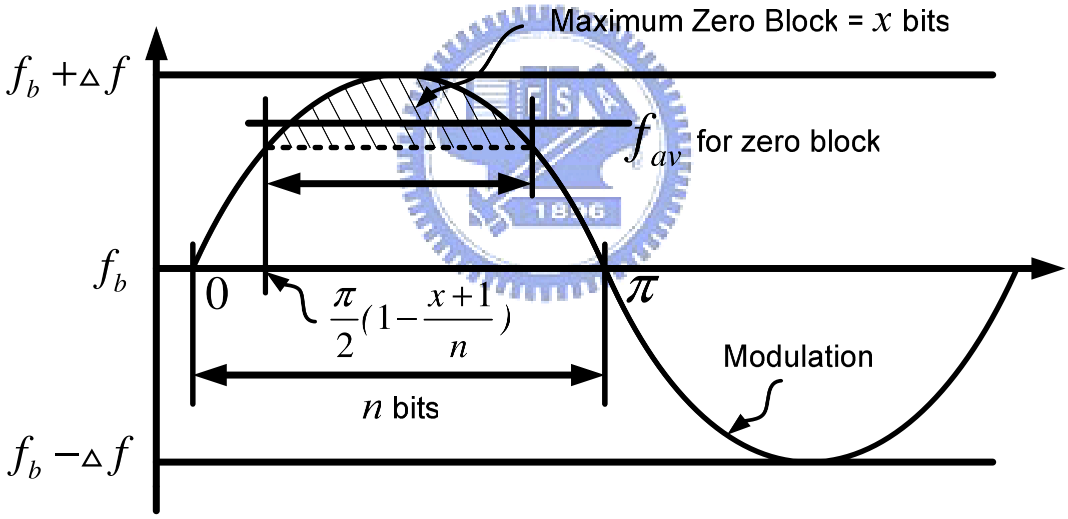


Fig. A-5 The Jitter Frequency modulates the Data Rate (II)

The data rate, which is modulated by the jitter frequency, can be expressed as:

$$Data \quad Rate = f_b - \Delta f \sin\theta \qquad \text{(A-12)}$$

If we integral (A-12), the result will be the average frequency of the period where is no data transition. Then we divide the result by (n+1)/x because there are n+1 bits in this region. CDR changes the sampling phase according to the (n+1)th bit which has data transition information until the (n+2)th bit. Hence, f_{av} represents the average frequency of the period where is no data transition and expressed as:

$$\begin{aligned} f_{av} &= f_b - \Delta f \cdot 2\int_{\pi/2[1-(n+1)/x]}^{\pi/2} \frac{sin\theta d\theta}{(n+1)/x} \\ &= f_b - \frac{x}{(n+1)} \cdot \Delta f \cdot 2\int_{\pi/2[1-(n+1)/x]}^{\pi/2} sin\theta d\theta \end{aligned} \qquad \text{(A-13)}$$

$f_b - f_{av}$ represents the average jitter of every bit of the period where is no data transition. Then we time it by (n+1) / f_b to express the total accumulated jitter in this interval. As mentioned before, error occurrence while the accumulated jitter is more than 1/2UI where is no data transition. Thus, we express as:

$$\frac{1}{2} = (f_b - f_{av}) \cdot \frac{n+1}{f_b} \qquad \text{(A-14)}$$

We put f_{av} in (A-13) to (A-14) and obtain that:

$$\frac{1}{2} = \frac{2\Delta f x}{\pi f_b} \cos\frac{\pi}{2}(1 - \frac{n+1}{x}) \qquad \text{(A-15)}$$

Then we derive the peak-to-peak jitter tolerance. The jitter accumulated in the interval a to d is the peak-to-peak jitter. Therefore, we calculate the average frequency of every bit among 0 to π in the interval a to d and denote as f_{av2}:

$$f_{av2} = f_b - \Delta f \cdot \frac{1}{\pi}\int_0^{\pi} \sin\theta d\theta = f_b - \frac{2}{\pi}\Delta f \qquad \text{(A-16)}$$

There are x bits in the interval a to d. Then we time $f_b - f_{av2}$ by x/ f_b to represent the jitter accumulated in the interval a to d, and it is also the peak-to-peak jitter, shown as:

$$J_{pp} = (f_b - f_{av2}) \cdot \frac{x}{f_b} \qquad \text{(A-17)}$$

We put f_{av2} in (A-16) to (A-17) and obtain that:

$$J_{pp} = \frac{2}{\pi}\Delta f \cdot \frac{x}{f_b} \qquad \text{(A-18)}$$

Then we put Δf in (A-15) to (A-18) and obtain the maximum jitter tolerance, describe as:

$$J_{pp} = \frac{1}{2} \cdot \frac{1}{\cos(\pi/2)[1-(n+1)/m]}$$

$$\Delta f = \frac{\pi}{4} \frac{f_b}{x\cos(\pi/2)[1-(n+1)/x]} \qquad \text{(A-19)}$$

where we can also obtain the amplitude of jitter frequency variation Δf, and $m = \frac{f_b}{2f_j}$. (A-19) comes into existence while $\frac{n+1}{m} \leq 1$. That is the condition when the jitter frequency is much slower than the data rate.

On the other hand, while $\frac{n+1}{m} \geq 1$, that is the condition when the jitter frequency is just a little slower than the data rate or almost the same, the maximum jitter tolerance describes as:

$$J_{pp} = \frac{1}{2} \quad for \frac{n+1}{m} \geq 1$$

$$\Delta f = \frac{\pi}{4} \cdot f_j \quad for \frac{n+1}{m} \geq 1 \qquad \text{(A-20)}$$

Because our CDR is quarter-rate architecture, clock generated by phase-locked loop is one-fourth the data rate, the maximum jitter tolerance is also one-fourth of the full-rate CDR architecture. Thus, peak-to-peak jitter shown in (A-19) and (A-20) must be modified as:

$$J_{pp} = \frac{1}{8} \cdot \frac{1}{cos(\pi/2)[1-(n+1)/x]} \quad for \frac{n+1}{m} \leq 1$$
$$J_{pp} = \frac{1}{8} \quad for \frac{n+1}{m} \geq 1 \tag{A-21}$$

The most important parameter in (A-21) is *n*, which represents the zero block number. We should consider jitter tolerance and maximum zero block tolerance simultaneously. Although there is no specification limitation on jitter tolerance for burst-mode PON system, we follow the specification for OC-48. We must ensure that how many numbers of zero block can be tolerated while our CDR passes the OC-48 mask. As shown in Fig. A-6, the more numbers of zero block tolerance, the less jitter can be tolerated. It implies a trade-off. By simulation result, we can observe while our CDR passes the OC-48 mask, the maximum zero block tolerance is 17 bits.

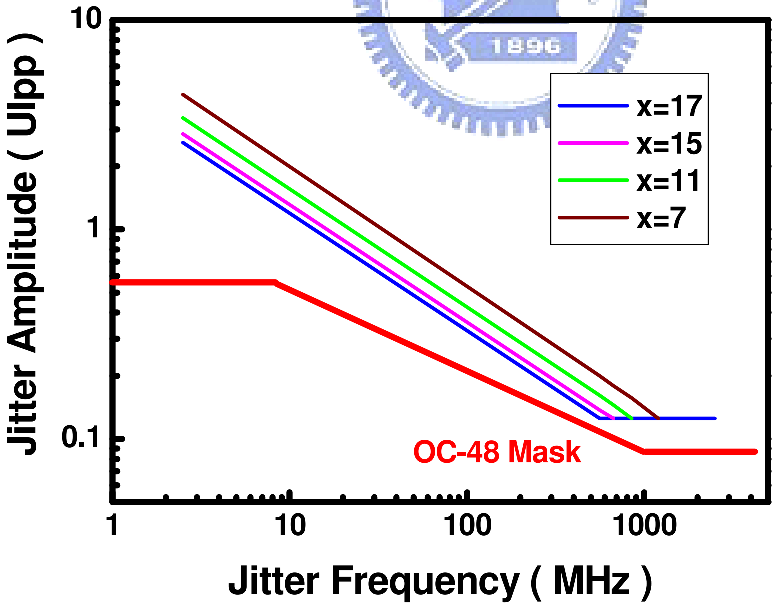


Fig. A-6 Jitter Tolerance with Different Zero Block Tolerance

A.3 Jitter Transfer

Jitter transfer means the output data jitter as the input data jitter is varied at different rates, so it presents the capacity of jitter filtering. For data repeaters, because they are connected in series, jitter transfer is an important specification to filter out accumulated jitter on the path, if not, after tens of repeaters, the signal must have been overwhelmed by a variety of noise sources.

What is the desirable jitter transfer function for CDR circuits? We note that if the input jitter varies very slowly, for example, if the zero crossings wander from their ideal points at a low rate, than the output must follow the input to ensure phase-locking. On the other hand, if the input jitter varies rapidly, the CDR circuit must filter out the jitter, for example, the output must track the input to a less extent. Thus, the jitter transfer exhibits a low-pass characteristic, as is the case with phase-locked loop.

Unlike jitter transfer, jitter tolerance, which is mentioned in the last section, is a measurement of tolerable jitter amplitude at a given frequency of jitter modulation. Hence, the faster the phase of recovered clock could be adjusted, the better the jitter tolerance would be. In summary, jitter tolerance is a test for phase tracking ability.

Compared jitter tolerance with jitter transfer, the slower the phase adjustment, the better the jitter filtering. It implies that jitter tolerance and jitter transfer form a trade-off problem. Faster tracking leads to better jitter tolerance but worse jitter transfer while slower tracking leads to better jitter transfer but worse jitter tolerance.

A.4 Jitter Generation

Jitter generation means the output jitter when there is no input jitter. In other words, the extra jitter is generated by the CDR system. This characteristic directly affects the timing margin of following circuits, so it is also important to a CDR system even though it is not particularly defined in the specification of PON system. This jitter stems from noise in the CDR itself, such as phase noise in VCO or supply noise.

Jitter generation is smaller in our CDR system theoretically because it operates in a closed-loop way. This closed tracking loop can filter out not only input jitter but also the noise in this CDR circuit. Besides, unlike conventional PLL-based CDR topology or Gated-VCO-based CDR topology, each phase adjustment is discrete-time instead of continuous-time. A few UI jitter appear at recovered clock and data while the output phase is changed each time. This is so called the static phase offset, as mentioned before. However, when our CDR is in the lock condition, the static phase offset is less than 1/32UI. This amount of jitter generation is quite small and can be neglected.

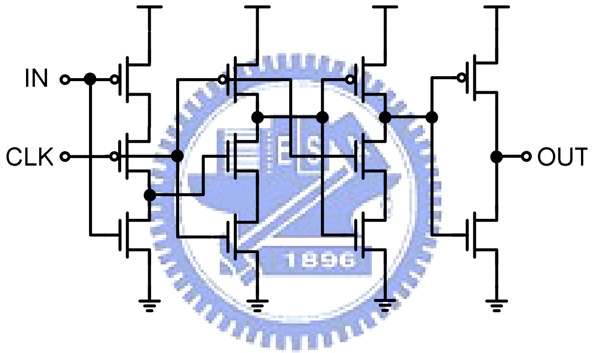
Appendix B

Logic Implementation

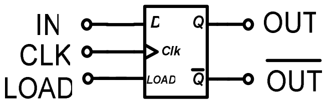
In our proposed CDR, almost all building blocks of circuits are digitally implemented. Thus, many logic gates and D-Flip-Flops must be utilized to make all function correct. In this appendix, we introduce the logic implementation.

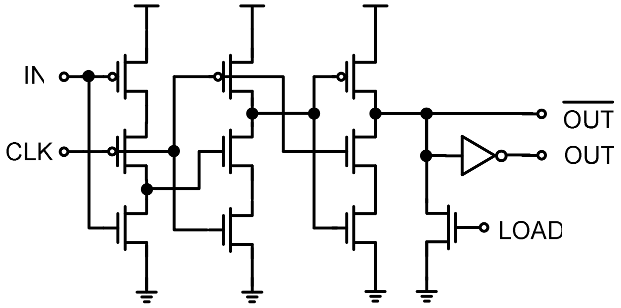
B.1 Conventional TSPC-Type DFF

We describe the conventional implementation for D-Flip-Flop. Our DFF is implemented by True-Single-Phase-Clock-type (TSPC-type) D-Flip-Flop and the circuit implementation is demonstrated in Fig. B-1(a). If our DFF must be given a initial value, we should exploit the DFF with “load” function. Our initial control signal varies from high to low. Thus, we utilize the DFF with LOAD if the initial value is “1” and logic symbol and circuit implementation are illustrated in Fig. B-1(b) and (c), respectively. On the contrary, we utilize the DFF with LOADB if the initial value is “0” and logic symbol and circuit implementation are illustrated in Fig. B-1(d) and (e), respectively. Moreover, logic symbol and circuit implementation of the DFF with “reset” function is described in Fig. B-1(f) and (g), respectively.



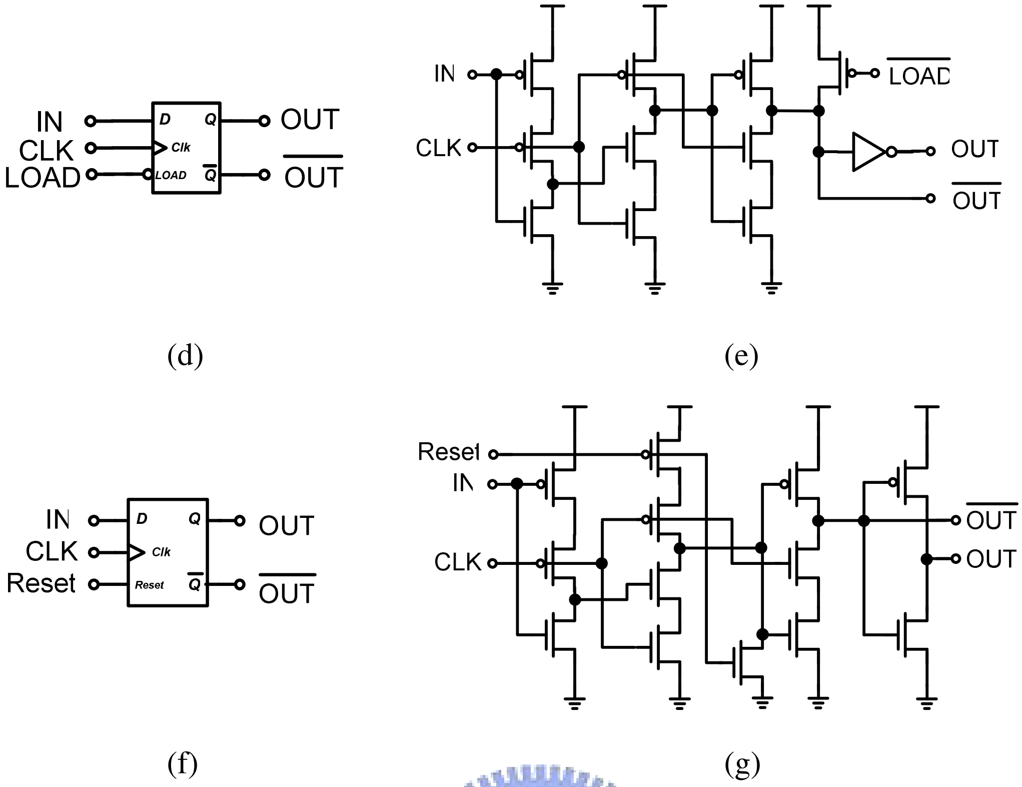
(a)





(b)

(c)



(d) (e)

(f) (g)

Fig. B-1 (a) Conventional DFF Circuit Implementation

(b) DFF with LOAD Logic Symbol

(c) DFF with LOAD Circuit Implementation

(d) DFF with LOADB Logic Symbol

(e) DFF with LOAD Circuit Implementation

(f) DFF with RESET Logic Symbol

(g) DFF with RESET Circuit Implementation

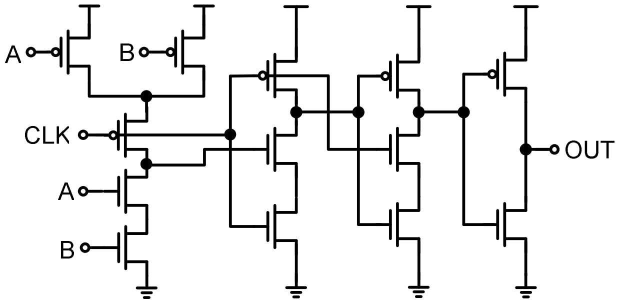
B.2 DFF with Embedded Logic Gate

There are many logic gates in our digital building blocks. However, our CDR operates at high speed so that we have to reduce the gate delay of all digital circuits.

The most critical delay path is the pass where must pass through the D-Flip-Flops. Our DFF is implemented by True-Single-Phase-Clock-type (TSPC-type) DFF. We can eliminate the delay path if we combine the TSPC-type DFF and logic gate which is in the front of the DFF together. In other words, The front-end logic gate is embedded into the TSPC-type DFF. Many kinds of logic gates can be embedded, such as NAND, NOR, XOR, and so on. We describe the detail circuit implementation below.

B.2.1 D-Flip-Flop with Embedded NAND

Fig. B-2(a) shows the circuit implementation of the DFF with embedded NAND. As mentioned before, if our DFF with embedded NAND must be given a initial value, we should exploit the DFF with "load" function. The logic symbol and circuit implementation of the DFF with embedded NAND and LOAD are illustrated in Fig. B-2(b) and (c), respectively. On the contrary, the logic symbol and circuit implementation of the DFF with embedded NAND and LOADB are demonstrated in Fig. B-2(d) and (e), respectively.



(a)

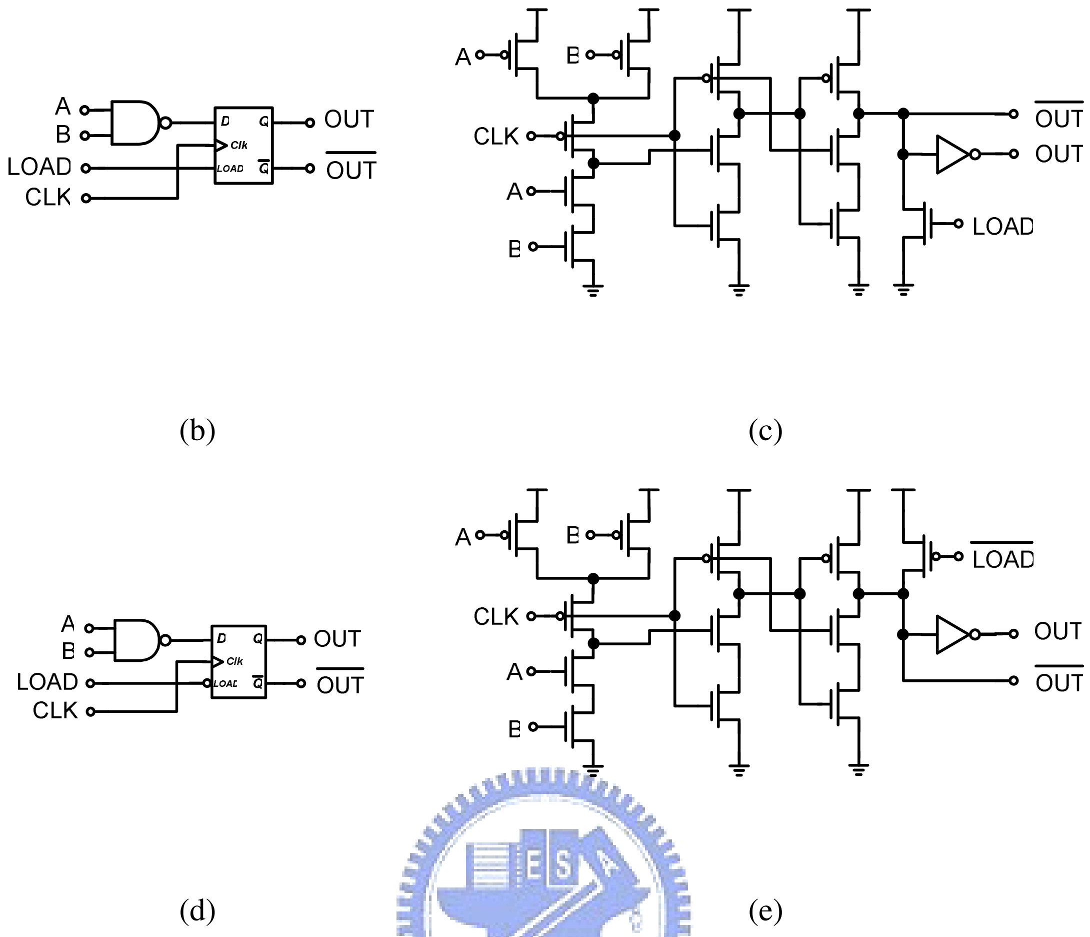


Fig. B-2 (a) DFF with embedded NAND Circuit Implementation

(b) DFF with embedded NAND and LOAD Logic Symbol

(c) DFF with embedded NAND and LOAD Circuit Implementation

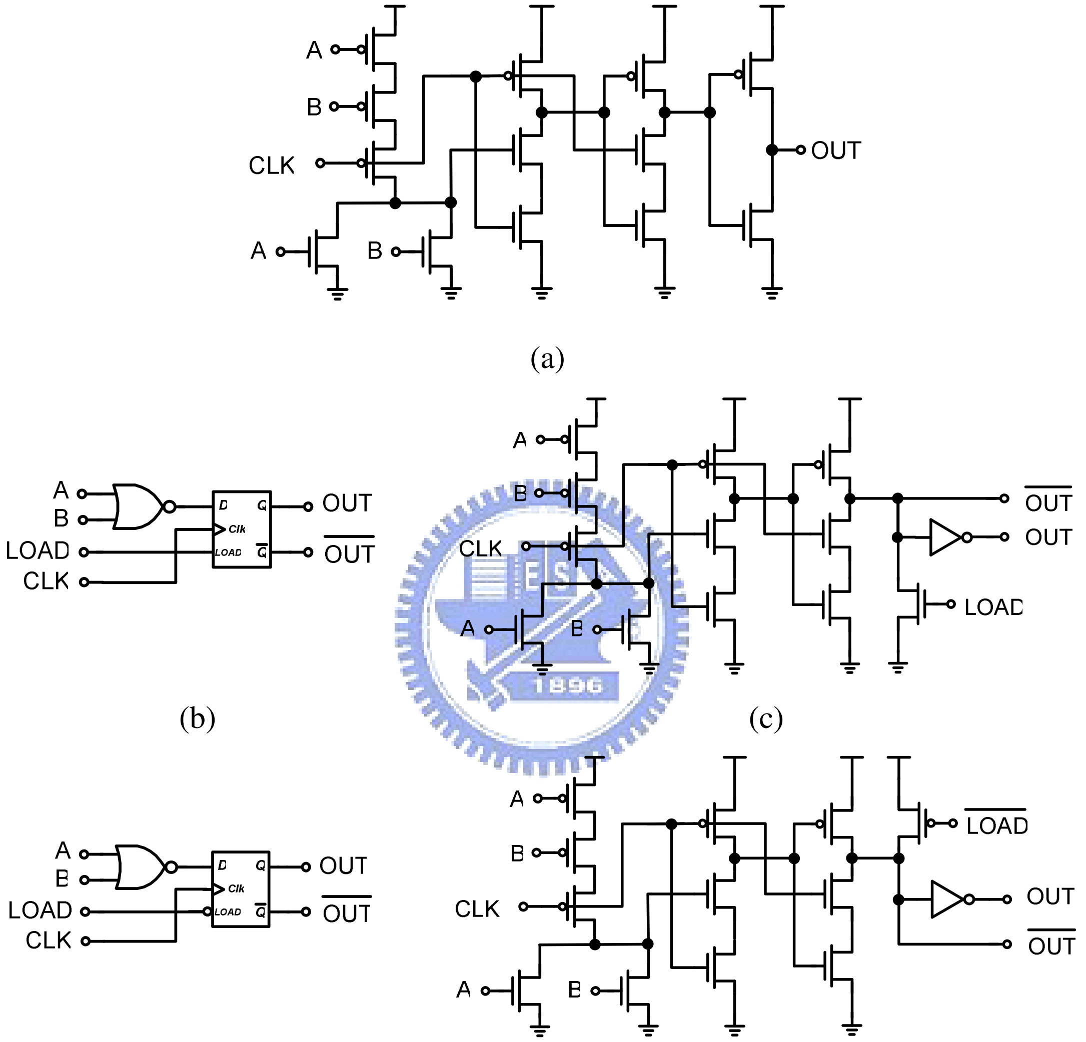
(d) DFF with embedded NAND and LOADB Logic Symbol

(e) DFF with embedded NAND and LOADB Circuit Implementation

B.2.2 D-Flip-Flop with Embedded NOR

Fig. B-3(a) shows the circuit implementation of the DFF with embedded NOR. The logic symbol and circuit implementation of the DFF with embedded NOR and

LOAD are illustrated in Fig. B-3(b) and (c), respectively. On the contrary, the logic symbol and circuit implementation of the DFF with embedded NOR and LOADB are demonstrated in Fig. B-3(d) and (e), respectively.



(a)

(b)

(c)

(d)

(e)

Fig. B-3 (a) DFF with embedded NOR Circuit Implementation

(b) DFF with embedded NOR and LOAD Logic Symbol

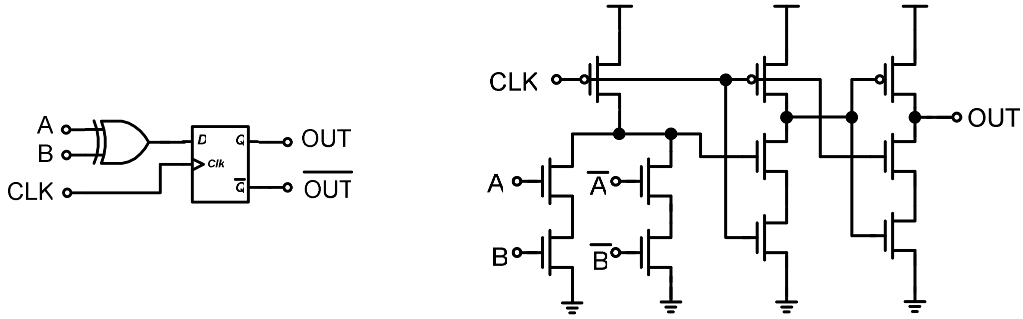
(c) DFF with embedded NOR and LOAD Circuit Implementation

(d) DFF with embedded NOR and LOADB Logic Symbol

(e) DFF with embedded NOR and LOADB Circuit Implementation

B.2.3 D-Flip-Flop with Embedded XOR

Fig. B-4(a) and (b) illustrates the logic symbol and circuit implementation of the DFF with embedded XOR, respectively.



(a) (b)

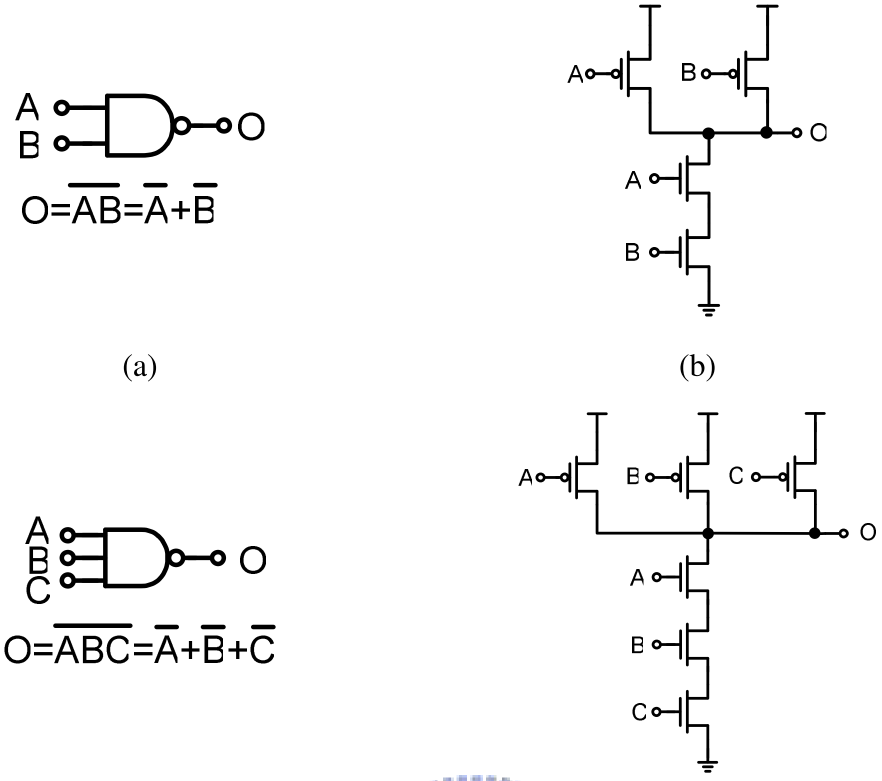
Fig. B-4 (a) DFF with embedded XOR Logic Symbol

(b) DFF with embedded XOR Circuit Implementation

B.3 Basic Logic Gate Implementation

B.3.1 NAND Logic

Fig. B-5(a) and (b) illustrates the logic symbol and circuit implementation of the 2-input NAND gate, respectively, while Fig. B-5(c) and (d) illustrates the logic symbol and circuit implementation of the 3-input NAND gate, respectively. Our NAND logic is all implemented by complementary CMOS type.


A
B
O
$O=\overline{AB}=\overline{A}+\overline{B}$
A
B
O
A
B
A
B
C
O
$O=\overline{ABC}=\overline{A}+\overline{B}+\overline{C}$
A
B
C
O
A
B
C

(a) (b)

(c) (d)

Fig. B-5 (a) 2-Input NAND Gate Logic Symbol

(b) 2-Input NAND Gate Circuit Implementation

(c) 3-Input NAND Gate Logic Symbol

(d) 3-Input NAND Gate Circuit Implementation

B.3.2 NOR Logic

Fig. B-6(a) and (b) demonstrates the logic symbol and circuit implementation of the 2-input NOR gate, respectively, while Fig. B-6(c) and (d) demonstrates the logic symbol and circuit implementation of the 3-input NOR gate, respectively. Our NOR logic is all implemented by complementary CMOS type.

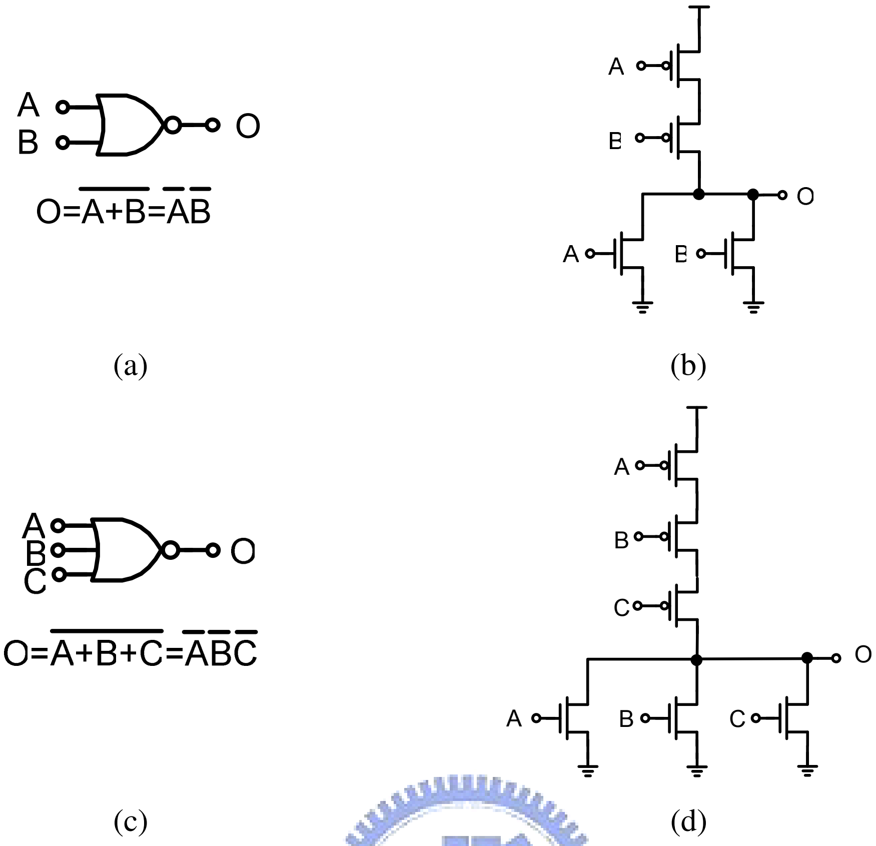


Fig. B-6 (a) 2-Input NOR Gate Logic Symbol

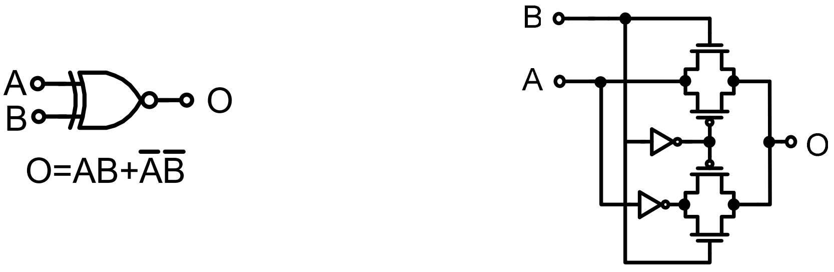
(b) 2-Input NOR Gate Circuit Implementation

(c) 3-Input NOR Gate Logic Symbol

(d) 3-Input NOR Gate Circuit Implementation

B.3.3 XOR Logic

Fig. B-7(a) and (b) demonstrates the logic symbol and circuit implementation of the 2-input XOR gate, respectively. Our XOR logic is all implemented by transmission-gate type.



(a) (b)

Fig. B-7 (a) 2-Input XOR Gate Logic Symbol

(b) 2-Input XOR Gate Circuit Implementation

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論文名稱 ： 一個操作在1.25到6 Gbps脈衝式時脈資料回復電路

A 1.25~6 Gbps Burst-Mode Clock and Data Recovery Circuit

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高等數位訊號處理	IEE7732	劉志尉教授	86
射頻積體電路	IEE5646	郭建男教授	92
微波工程(I)	ECM5501	郭仁財教授	86
展頻通訊	ECM5105	黃家齊教授	88
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類比積體電路(II)	IEE6736	吳介琮教授	90
數位積體電路	IEE7721	柯明道教授	92
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