High-Speed Viterbi Decoder Based on the
Two-Dimensional ACS Structure

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Abstract

A high-speed Viterbi decoder based on the high-radix trellis structures is presented. The proposed two-dimensional add-compare-select unit can result in much cost efficient design for a high-radix Viterbi decoder. Moreover, the decoding speed can be further enhanced through datapath retiming. The general retiming approach and the two-dimensional architecture are introduced, and the implementation of a 64-state Viterbi decoder is reported to verify the proposed methods. The simulation results indicate the present decoder can provide the maximum 1.1 Gb/s throughput in the 1.96 mm^2 0.13-μm silicon area. Furthermore, the smallest decoder chip in supporting the multiband orthogonal frequency division multiplexing (MB-OFDM) ultra-wideband system has an area of 0.9mm^2.