國 立 交 通 大 學

電子工程學系電子研究所碩士班

碩 士 論 文

應用於超寬頻系統之低功率主動性相位分離器與混波器之設計

Design Low Power Active Balun and Mixer for Ultra-Wideband Application

研究生: 徐達道

指導教授: 郭建男 教授

中華民國九十五年六月

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碩士論文

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摘要

本篇論文主旨在於利用標準 0.18um CMOS 製程設計適用於超寬頻系統前端接受器之低功率主動性相位分離器與混波器積體電路，此外並利用新設計的混波器架構結合低雜訊放大器組成低功率、低電壓窄頻接收器前端電路。2 顆低功率超寬頻主動性相位分離器、1 顆低功率、低電壓混波器結合主動性相位分離器與 1 顆低功率、低電壓接收器前端電路皆已經由晶片製作而被驗證。

主動性相位分離器方面採用全新的架構，不同於以往利用差動放大器架構來達成主動性相位分離器的方法，而是利用 NMOS 在上 PMOS 在下的串接方式，避免電流源的寄生效應，以大幅增加頻寬，且同時利用 Current Reuse 的方法，大幅降低了功率損耗，根據量測結果可以得到在 Gain Error 小於 2 dB 且 Phase Error 小於 3 度的條件下，可用頻寬高達 8 GHz，而整個電路的功率損耗僅為 1.44 mW 且 Supply Voltage 為 1.2 V，相較於傳統的主動性相位分離器功率損耗約為 12 mW，已大幅節省約 88%。

當主動性相位分離器其後接上混波器或其它可調式差動輸入電路時，將造成主動性相位分離器的輸出負載改變，故根據實際需要改良原本第一顆主動性相

位分離器，將 NMOS 的 Loading 由原本的電阻改為工作在三極體區的 PMOS，利用改變其 Gate 偏壓（Vtune）將其 Rds 改變，使其成為 0~10 GHz 抗製程變異與對應輸出負載變化的主動性相位分離器，根據模擬結果，在 Gain Error 小於 2 dB 且 Phase Error 小於 3 度的條件下，可用頻寬高達 10 GHz，而整個電路的功率損耗僅為 1.44 mW 且 Supply Voltage 為 1.2 V，Output Loading 在 25 ~ 200 歐姆的範圍下均可利用改變 Tunable Resister (Rds)來達成預期的效能，Vtune 每變化 0.1 V, Gain Difference 變化 1 dB 而 Phase Difference 變化 1.5 度。

混波器方面為了降低 Supply Voltage，而將原本的 Gilbert Mixer gm stage 與 switch stage 串接方式改為將 LO 與 RF DC 分流，使每個 MOS 接有足夠的 Vds 跨壓，並且為了在 Low Power 下工作，將 LO 由大訊號改為小訊號的方式，使得 Mixer 一直工作於 subthreshold region，因在工作期間並無 MOS turn off 利用兩倍的 Conversion Gain 且加上大 R_L 的方式來達到足夠的 Conversion Gain，利用此新設計的混波器分別完成了 Low Voltage 1.5 mW 6~10.6-GHz UWB CMOS Mixer With Active Balun 與 Low Voltage 0.86 mW 5~6 GHz Front End。

根據量測結果 Low Voltage 1.5 mW 6~10.6-GHz UWB CMOS Mixer With Active Balun 在功率損耗為 1.56 mW 且 V_{DD}=1.2 V 下提供平坦的 Conversion Gain 為 10 dB ± 1.5 dB from 6 GHz to 10 GHz， NF 約為 15 dB 而 IIP3 約為 3 dBm。

Low Voltage 0.86 mW 5~6 GHz Front End 量測結果則為，在 supply voltage 為 1 V 且功率損耗為 0.86 mW 下，最大的 conversion gain 為 25 dB at 5.3 GHz，3 dB 頻寬為 1 GHz， NF 約為 12 dB 而 IIP3 大約 -6 dBm。

Design Low Power Active Balun and Mixer for Ultra-Wideband Application

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ABSTRACT

The aim in this thesis is mainly based on the design of active balun and mixer in the receiver front end of ultra-wideband system using standard 0.18um CMOS process. Also, a low power low voltage narrow band front end is composed of a new mixer and a low noise amplifier. Two low power UWB active baluns, one low power mixer combined with a low power active balun and one low power low voltage front end were verified through 4 individual chips.

In the first chip, an 8 GHz Low Power Ultra-Wideband Active Balun is analyzed and designed. We employ a new topology to design active balun and greatly reduce power consumption and extend the available bandwidth. Measured data show that the bandwidth extends to 8 GHz, gain difference is less than 2 dB, phase difference is less than 3 degree and differential gain has flat gain about -2 dB while consuming 1.5mW.

In the second chip, an ultra wide band low power tunable active balun for process variation compensation is analyzed and designed. A tunable active resister is adopted to improve the first chip. Measured data show that the active balun has a tunable function for process variation compensation is its most important property.

In the third chip, a new design of a low power low voltage mixer is combined with an active balun of the first chip. All transistors in the mixer are biased in the subthreshold region to approach low power application. Use large resisters about 800 Ω as output loading to have high conversion gain and the gain of balun and mixer compensate each other to form a flat gain from 6 to 10 GHz. Measured data show that the flat conversion gain is 9.5 dB ± 1.5 dB from 6 GHz to 10 GHz, NF is about 15 dB and IIP3 is about 3 dBm while consuming 1.5mW.

In the final chip, a 5~6 GHz low power receiver front-end circuit is analyzed and designed. Employ the mixer of the third chip and modify the mixer from double balance to single balance. The single input mixer combines with a single output LNA and all supply voltages are reduced to 1 V to form the 5 ~ 6 GHz 1V low power receiver front-end circuit. Measured data show that the max conversion gain is 25 dB at 5 GHz, 3 dB bandwidth is about 1 GHz, NF is about 10 dB and IIP3 is about -6 dBm while consuming 0.8mW.

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徐達道

九十五年　六月

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Chapter 1

Introduction

1.1 System Overview

The Multi-band OFDM Alliance (MBOA) standard for UWB communications draws heavily upon prior research in wireless local area network (WLAN) systems. The UWB system is an emerging high-speed and low-power wireless communication approved by Federal Communication Commission (FCC). The multi-band UWB has greater flexibility in coexisting with other international wireless systems and future government regulators, and could avoid transmitting in already occupied bands. In a manner similar to IEEE 802.11 a/g, MOBA partitions the spectrum from 3 to 10 GHz into 825-MHz bands and employs OFDM in each band to transmit data rates as high as 480 Mb/s. Fig. 1.1 shows the structure of MOBA bands and the channelization within each band. The 13 bands span the range of 3.1 to 10.6 GHz. The frequency operation for Mode 1 device allocates in 3.1GHz to 5GHz and the one for Mode 2 device allots to 3.1-8GHz.

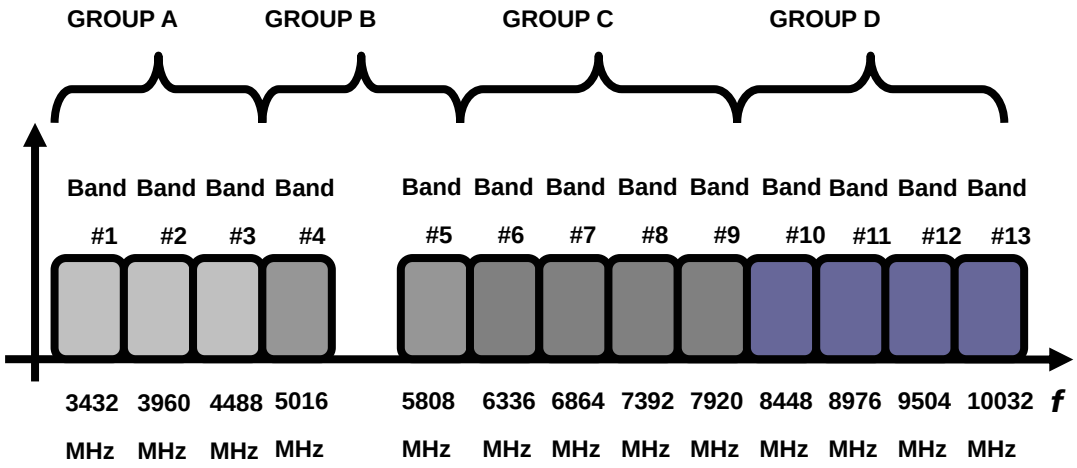


Fig 1.1 Multi-band spectrum allocation

1.2 Motivation

The balun circuits always play the critical component in RF system if they are necessary. For example, it is often between the single output LNA and the double balance mixer. Usually, the passive balun is adopted because of no power consumption. But the large physical size of the passive balun is hard to cost down. So, to design an active balun with limited power consumption even has flat gain is a critical challenge for design. How to do that is one of the main objects of this thesis

Typical, the first stage of the receiver is a low noise amplifier (LNA), which provides high gain and low noise to suppress the overall system's noise performance. After balun, the mixer transforms the radio-frequency (RF) signal into base-band directly and needs high linearity to avoid the distortion of the signal. Because there is a LNA to suppress the overall system's noise performance, the noise performance of the mixer is not the most important design target. So, how to decrease the power consumption as small as possible and this mixer has an acceptable linearity at the same time is the other main object of this thesis.

1.3 Thesis Organization

In the chapter 2, the fundamental designs of front-end will be introduced.

In the chapter 3, the 8 GHz low power ultra-wideband active balun is presented in section 3.2. And the modified active balun, 0~10 GHz ultra wide-band low power tunable active balun for loading variation and process variation compensation is discussed in section 3.3.

In the chapter 4, the low voltage 0.2-mW CMOS mixer is presented in section 4.2. And low voltage 2-mW 6~10.6-GHz ultra-wideband CMOS mixer with active balun is introduced in section 4.3.

In the chapter 5, to discuss the low-power front-end circuit design.

In the last chapter, the work is summarized and concluded.

Chapter 2

The Fundamental Designs of Front-End

The fundamental designs of the front-end architecture will be presented in this chapter. Section 2.1 gives the front-end architecture first. The design basic in LNA will be introduced in the section 2.3. The popular active balun at high frequency is discussed in section 2.4, and the end of this chapter will introduces the basic design of the mixer.

2.1 Front-End Architecture

In receiver architecture, input signals are translated into much lower frequencies by down-conversion mixer, and the active balun generates the differential output signals for double balance mixer from the signal input signal. Generally, the low noise amplifier is in the first stage for reducing noise from the active balun and the down-conversion mixer. A simple front-end architecture is shown in Fig. 2.1. I adopt the homodyne receiver due to the following reasons:

(1) The problem of image is removed due to $\omega_{IF} = 0$. Therefore no image filter is required, and the LNA need not drive a 50-Ω load.

(2) It is attractive for monolithic integration because this architecture needs less external components.

For the above reasons, this architecture is suitable for low-power and signal-chip design.

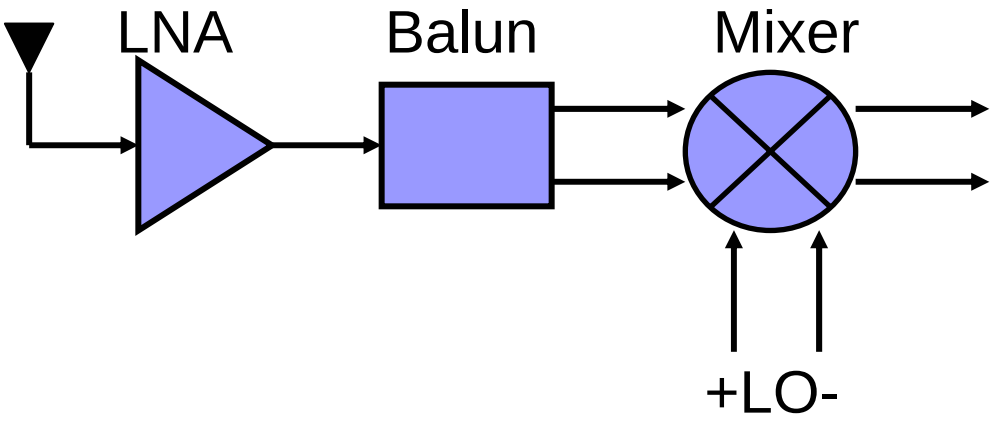


Fig. 2.1 Front-End

2.2 Low Noise Amplifier Basic

Low noise amplifier is the first gain stage in the receiver path so its noise figure directly adds to that of the system. Therefore, there are several common goals in the design of LNA. These include minimizing noise figure of the amplifier, providing enough gain with sufficient linearity and provide a stable 50Ω input impedance to terminate an unknown length of transmission line which delivers signal from antenna to the amplifier. Among LNA architectures, inductive source degeneration is the most popular method since it achieve noise and power matching simultaneously, as shown in Fig. 2.2. The following analysis is based on this architecture.

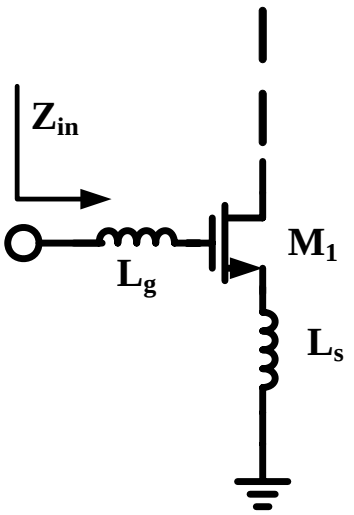


Fig. 2.2 Common-source input stage with inductive source degeneration

2.2.1 Low Noise Amplifier Architecture Analysis

In Fig. 3.1, the input impedance can be expressed as

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s$$

$$= (\frac{g_m}{C_{gs}})L_s \approx \omega_T L_s \quad \text{at} \quad \omega = \omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{2-1}$$

As shown in (2-1), the input impedance is equal to the multiplication of cutoff frequency of the device and source inductor at resonant frequency. Therefore it can be set to 50Ω for input matching while resonant frequency is designed to be equal to the operating frequency.

According to prior introduction, the equivalent noise model of common-source LNA with inductive source degeneration can be expressed as Fig. 2.3, where R_l is the parasitic resistance of the inductor, R_g is the gate resistance of the device. Note that the overlap capacitance C_{gd} has also been neglected in the interest of simplicity. Then the noise figure can be obtained by computing the total output noise power and output noise power due to input source. To find the output noise, we first evaluate the transconductance of the input stage. With the output current proportional to the voltage on C_{gs} and noting that the input circuit takes the form of series-resonant network, the transconductance at the resonant frequency can be expressed as

$$G_m = g_m Q_{in} = \frac{g_m}{\omega_0 C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{2\omega_0 R_s} \tag{2-2}$$

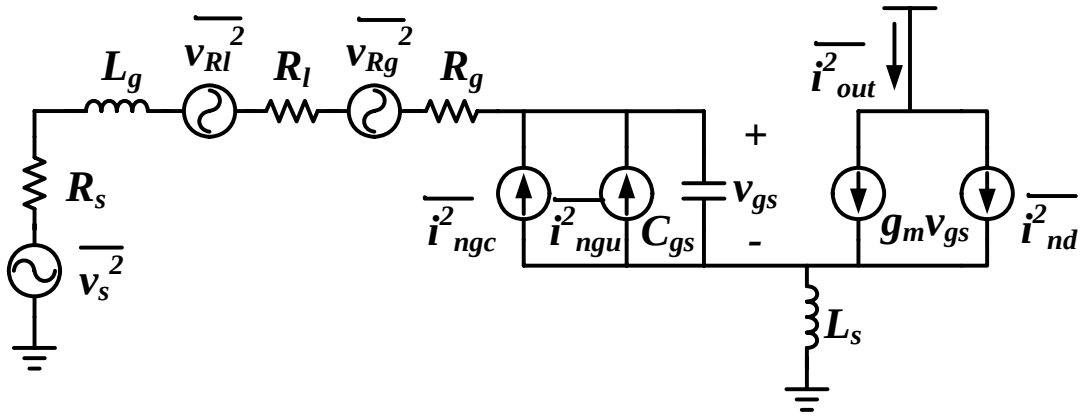


Fig. 2.3 Equivalent noise model of Figure 2.2

Q_{in} is the effective Q of the amplifier input circuit. So the output noise power density due to the source can be expressed as

$$S_{a,Rs}(\omega_0) = S_{Rs}G^2{}_{m.eff} = \frac{4kT\omega_T{}^2}{\omega_0{}^2 R_s(1+\frac{\omega_T L_s}{R_s})^2} \quad (2\text{-}3)$$

In the similar way, the output noise power density due to R_g and R_l is

$$S_{a,Rg,Rl}(\omega_0) = \frac{4kT(R_g+R_l)\omega_T{}^2}{\omega_0{}^2 R_s{}^2(1+\frac{\omega_T L_s}{R_s})^2} \quad (2\text{-}4)$$

Furthermore, channel current noise of the device is the dominant noise contributor, and its noise power density associated with the correlated portion of the gate noise can be expressed as

$$S_{a,i_{nd},i_{ngc}}(\omega_0) = \frac{4kT\gamma\kappa g_{do}}{(1+\frac{\omega_T L_s}{R_s})2} \quad (2\text{-}5)$$

Where γ is the coefficient of channel thermal noise, $\alpha = g_m / g_{do}$ and

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + \left[1 + |c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2 \tag{2-6}$$

$$Q_L = \frac{1}{\omega_0 R_s C_{gs}} \tag{2-7}$$

The last noise term is the contribution of the uncorrelated portion of the gate noise, and its output noise power density can be express as

$$S_{a,i_{ngu}}(\omega_0) = \frac{4kT\gamma\xi g_{do}}{(1+\frac{\omega_T L_s}{R_s})^2} \tag{2-8}$$

where

$$\xi = \frac{\delta\alpha^2}{5\gamma}(1-|c|^2)(1+Q_L{}^2) \tag{2-9}$$

According to (2-3),(2-4),(2-5) and (2-8), the noise figure at the resonant frequency can be expressed as

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma\chi}{\alpha Q_L}(\frac{\omega_0}{\omega_T}) \tag{2-10}$$

where

$$\chi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1+Q_L{}^2) \tag{2-11}$$

From (2-11), we observe that χ includes the terms which are constant, proportional to Q_L, and proportional to Q_{L2}. It follows that (2-11) will contain terms which are proportional to Q_L as well as inversely proportional to Q_L. A minimum noise figure, therefore, exits for a particular Q_L.

2.2.2 Optimizations of Low Noise Amplifier Design Flow

The analysis of the previous section can now be drawn upon in designing the LNA. In order to pick the appropriate device size and bias point to optimize noise performance given specific objectives for gain and power dissipation, a simple second-order model of the MOSFET transconductance can be employed which accounts for high-field effects in short channel devices. Assuming that the drain current, I_d, has the form

$$I_{DS} = WC_{ox}v_{sat}\frac{(V_{gs}-V_T)}{1+\frac{LE_{sat}}{V_{gs}-V_T}} = WC_{ox}v_{sat}LE_{sat}\frac{\rho^2}{1+\rho} \tag{2-12}$$

where $\rho \equiv \frac{V_{gs}-V_T}{LE_{sat}}$. And the (2-7) can be replace as

$$Q_L = \frac{3}{2\omega_0 WLC_{ox}R_s} \Rightarrow C_{ox} = \frac{3}{2R_sQ_L\omega_0 WL} \tag{2-13}$$

The power consumption of the LNA, therefore, can be expressed as

$$P_D = V_{DD}I_{DS} = \frac{3}{2}V_{DD}\frac{1}{Q_LR_s\omega_0}v_{sat}E_{sat}\frac{\rho^2}{1+\rho} \tag{2-14}$$

The noise figure can be expressed in terms of P_D and V_{gs}. Two parameters linked to power dissipation need to be accounted for.

$$\omega_T \approx \frac{g_m}{C_{gs}} = f_1(V_{gs}) \tag{2-15}$$

$$Q_L = \frac{3V_{DD}v_{sat}E_{sat}}{2P_D\omega_0R_s}\frac{\rho^2}{1+\rho} = \frac{P_0}{P_D}\frac{\rho^2}{1+\rho} = f_2(V_{gs},P_D) \tag{2-16}$$

where $P_0 = \frac{3V_{DD}v_{sat}E_{sat}}{2\omega_0R_s}$.

The noise figure of the LNA, therefore, can be expressed as

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha Q_L}\left(\frac{\omega_0}{\omega_T}\right)\left(1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}\left(1 + Q_L{}^2\right)\right) = f(V_{gs}, P_D) \quad (2\text{-}17)$$

In general, there are two approaches to optimize noise figure. The first approach assumes a fixed transconductance, G_m. The second approach assumes fixed power consumption.

(1) Fixed G_m optimization: To fix the value of the transconductance, G m ,we need only assign a constant value to ρ. Once ρ is determined, the optimization of the noise figure can be obtained by (2-17):

$$\left.\frac{\partial f(V_{gs}, P_D)}{\partial P_D}\right|_{fixedVgs} = 0 \Rightarrow P_{D.opt} \Rightarrow Q_{L.opt} \Rightarrow F = f(V_{gs}, P_{D.opt}) \quad (2\text{-}18)$$

From (2-13), we can obtain the optimal width to get the minimal noise figure for a given G_m under the assumption of matched input impedance. In this approach, the designer can achieve high gain and low noise performance by selecting the desired transconductance, but its disadvantage is that we must sacrifice the power consumption to achieve minimum noise figure.

(2) Fixed P_D optimization: An alternative method of optimization fixes the power dissipation and adjusts device size and bias point to minimize the noise figure. Once P_D is determined, the optimization of the noise figure can be obtained by (2-19):

$$\left.\frac{\partial f(V_{gs}, P_D)}{\partial V_{gs}}\right|_{fixedPD} = 0 \Rightarrow V_{gs.opt} \Rightarrow Q_{L.opt} \Rightarrow F = f(V_{gs.opt}, P_D) \quad (2\text{-}19)$$

Then the optimum device size can be obtained to get the best noise performance for fixed power dissipation. In this approach, the designer can specify the power dissipation and find the optimal noise performance, but its disadvantage is that the

transconductance is held up by the optimal noise condition.

2.3 Design Basic in Active Baluns

Differential baluns (or phase splitters) are basic cells required in microwave components such as balanced mixers, multipliers, and phase shifters. An ideal differential phase splitter will generate a pair of differential signals which have balanced amplitude and phase (0 dB gain difference and 180°) from a single input.

In RFIC there are passive and active differential phase splitter or baluns. LC networks can be used for narrow-band passive baluns; microstriplines can be used for wide-band passive baluns. However, the spiral inductors, MIM capacitors, and microstriplines in RFIC are too expensive due to their larger physical size at lower microwave frequencies. There are three categories of active balun circuits normally employed in lower microwave frequencies for wireless communications: single FET circuits, common-gate common-source circuits and differential amplifier circuits.

Fig. 2.4 shows the single FET circuits as active balun. It is probably the simplest. At low frequency the small signal circuit of this active balun can ignores all parasitic effect. Under this condition, this circuit can produces a pair of differential output signals at the drain and source of the FET respectively. At higher frequency range, this circuit is limited by imbalances caused by the imbalances caused by parasitic capacitance of FET. The best result obtained from this type of the structure is

1dB and 176° at 950 MHz. To make it applicable at higher frequency, a sophisticated imbalance cancellation technique was used to improve the performance beyond 1 GHz. It had 1 dB amplitude difference and 172° pahse difference (-8° unbalance) from 700 MHz to 1.7 GHz. However, the tradeoff was the increase of circuit complexity, die area, and dc current. For accurate results beyond 2 GHz, the application of the signal FET circuit is questionable.

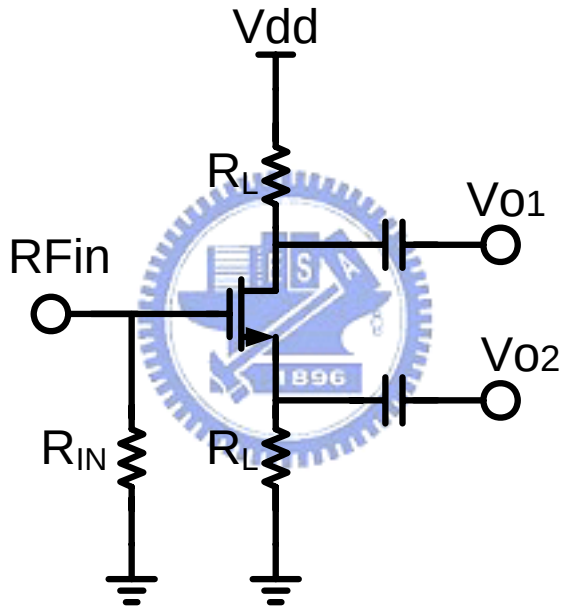


Fig.2.4 the single FET circuits as active balun

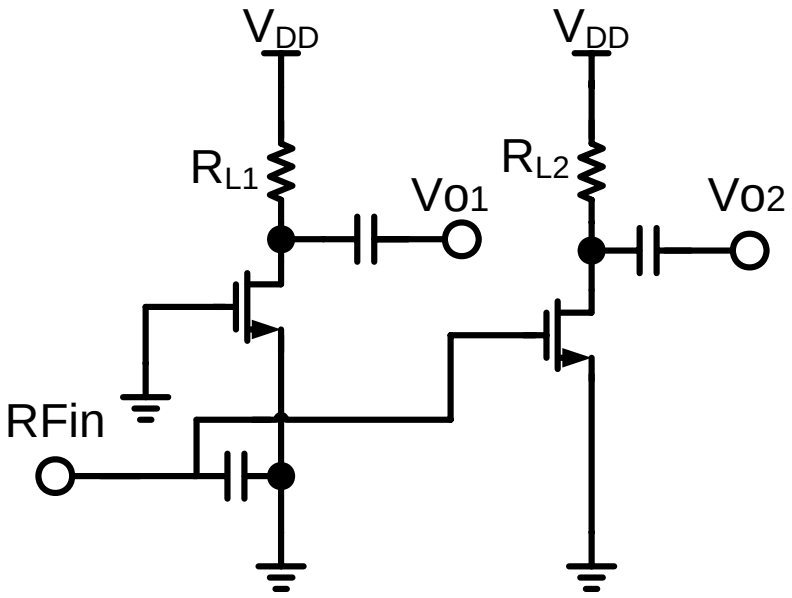


Fig. 2.5 common-gate common-source (CGCS) circuit as active balun

Fig.2.5 shows the common-gate common-source (CGCS) circuit as active balun. The common-gate common-source (CGCS) circuit provides equal amplitudes split with 180° phase difference. In this configuration, the ac coupling capacitance and bypass capacitance need to be adjusted separately to optimize at a specific frequency to achieve balanced differential signals. Therefore, this configuration is only good for narrow-band application are around 0.5-2 dB and 177-189° due to the process variation and asymmetric signal path.

The differential amplifier circuit is shown in Fig. 2.6. It is very popular to apply the differential amplifier as active balun at high frequency. Ideally, this circuit will provide equal amplitude (or gain) and 180° phase difference. However, due to the finite impedance at node “A” caused by strong parasitic at high frequency, the gain

and phase balance are poor.

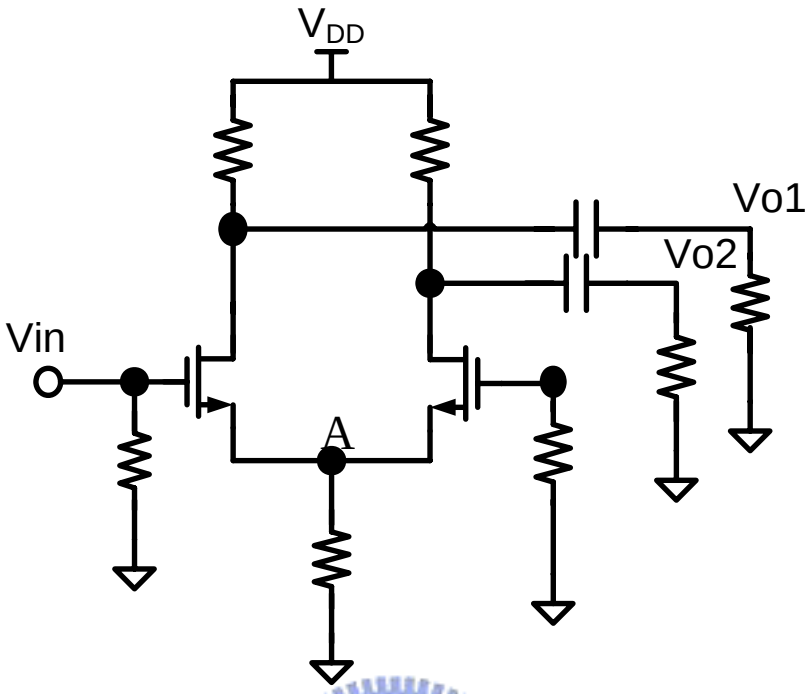


Fig. 2.6 Differential amplifier as active balun

An active device is often used as the current source. However, besides the finite impedance at node “A”, the voltage drop across the drain and source make it difficult to realize in low power supply circuit as required by the portable wireless applications (Vdd < 3V or even < 2V). According to simulation result, the output amplitude difference can be 2 dB or the phase difference can be poorer than 174°, within frequency range from dc to 6 GHz.

The active current source was replaced by an inductor to increase the impedance of S1 at high frequencies. When an ideal inductor with unlimited value (dc through and ac block) is used as the current source, excellent results can be obtained.

However, this extra large ideal inductor is not viable to be realized on-chip due to large physical size. This circuit obtained 1dB gain difference and 175° phase difference at the specific frequency, at other frequencies, the gain and phase balance are poor. Therefore, it is only applicable for narrow-band applications.

2.3.1 Differential Amplifier with a Series LCR Feedback as Active Balun Analysis

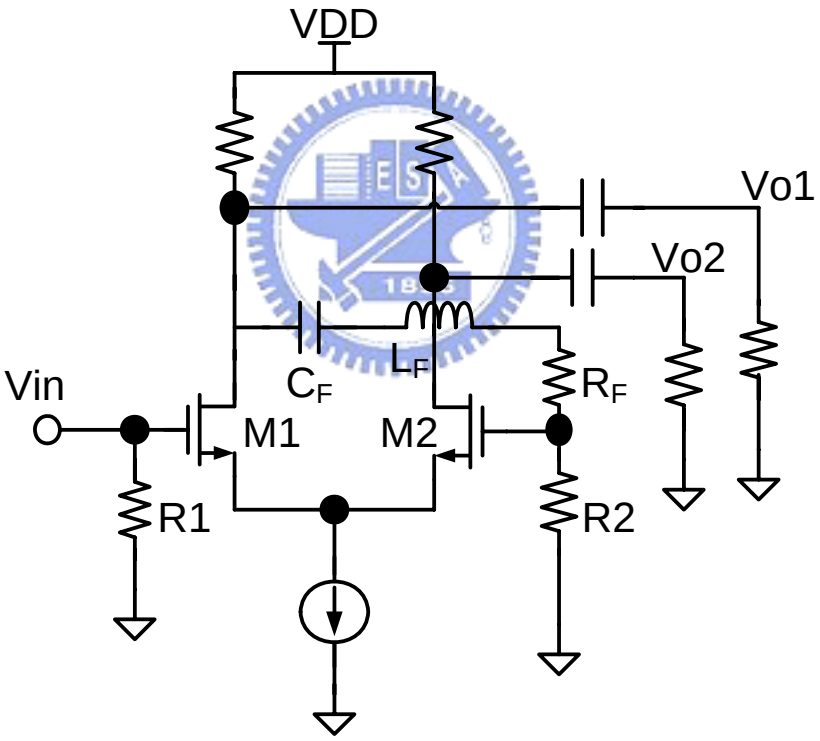


Fig. 2.7 Differential amplifier with LCR feedback as active balun

Fig. 2.7 shows the differential amplifier with LCR feedback as active balun. It is most popular to apply this circuit as an active balun at high frequency. The feedback circuit consists of twisters R2 and R_F, an inductor L_F, and a capacitor C_F.

This feedback circuit will helpo res to reduce the Vo1 power and increase the Vo2 power. The resister R2 plays two roles: it keeps dc bias of M2 the same as T1, at the same time it senses the signal fed back from the drain of M1. C_F provides a dc blocking function so that the feedback circuit will not shift dc bias of M2. At the application specific frequency ω, if C_F and L_F values are chosen in such a way that they follow the equation of

$$L_F \bullet C_F = \frac{1}{\omega^2} \qquad (2\text{-}20)$$

the phase delay from the drain of M1 to the gate of M2 is zero. This is because that the series LC circuit gives a zero reactance *AC* equivalent circuit will reduce to R_F, R_2 and z_2, where z_2 is M2's gate input impedance at ω. AC signals on the gate of M2 (v_{G2}) and on the drain of M1 (v_{D1}) have the following relationship:

$$v_{G2} = v_{D2} \bullet \frac{R_2 // z_2}{R_F + R_2 // z_2} \qquad (2\text{-}21)$$

From (2-2), v_{G2} can be changed by adjusting R_F and R_2.

The amplitude tuning of the phase splitter will be taken care of by the ratio of R_F and R_2. The phase unbalance can be adjusted by proper choice of reactance of the feedback circuit. The reactance X_F is given as

$$. \quad X_F = \omega L_F - \frac{1}{\omega C_F} \qquad (2\text{-}22)$$

X_F can be positive (inductive), zero (resistive), or negative (capacitive) by adjusting L_F and C_F values at the application frequency Ω. Thus, the phase unbalance at output

ports can be effectively cancelled. From (2-22), it is seen that the phase tuning can be done in a linear mode by changing L_F and keeping C_F constant since $X_F \propto L_F$, or in nonlinear mode by changing C_F and keeping L_F constant, or by changing both. The Q factor is not important in this design because the lossy part of the inductor can be treated as part of R_F in the feedback circuit. In RFIC design, the actual choice of L_F and C_F depends on the consideration of area consumption, phase tuning sensitivity, and process tolerances.

But like the conventional differential amplifier as active balun, the differential amplifier with RLC feedback as active balun needs twice DC current paths. It consumes twice DC power consumptions. High power consumption limits the value of this circuit. And RLC feedback is frequency depend to limit the bandwidth of this active balun.

2.5 Down-Conversion Mixer Basic

The purpose of the mixer is to convert a signal from one frequency to another. In a receiver, this conversion is from radio frequency to intermediate frequency or zero-IF. Mixing requires a circuit with a nonlinear transfer function, since nonlinearity is fundamentally necessary to generate new frequencies. Fig. 2.8 shows a simplified CMOS Gillbert cell mixer, which is composed of transconductance stage and switching stage.

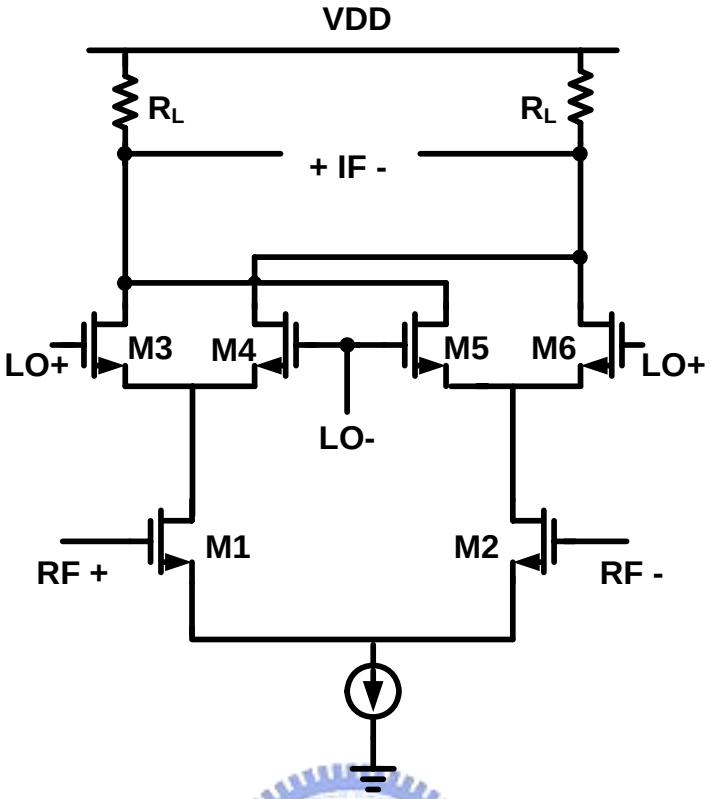


Fig. 2.8 Simplified CMOS Gilbert Cell mixer

The RF input must be linear, or adjacent channels could intermodulate and interfere with the desired channel. And the third-order intermodulation term from the two other signals will be directly on the top of the desired signal. The LO input need not be linear, since the LO is clean and of known amplitude. In fact, the LO input is usually designed to switch the upper quad so that for half the cycle M3 and M6 are on and taking all current to output loading. For the other half of the LO cycle, M3 and M6 are off and M4 and M5 are on. This stage will be, therefore, like switch to mixing RF signal to IF signal.

2.5.1 Conversion Gain

The gain of mixers must be carefully defined to avoid confusion. The voltage conversion gain of a mixer is defined as the ratio of the rms voltage of the IF signal and rms voltage of the RF signal. Note that the frequencies of these two signals are different. The power conversion gain of a mixer is defined as the IF power delivered to the load divided by the available RF power from the source. If the impedances are both matched to 50Ω, then the voltage conversion gain and power conversion gain of the mixer are equal when they are expressed in decibels.

Now, we assume that M3-M6 work like an ideal switch, and the conversion transconductance of the mixer can be expressed as

$$G_c = \frac{2}{\pi} g_m \tag{2-23}$$

where gm is the transconductance of M1 and M2, and $2/\pi$ is produced by switching stage.

2.5.2 Switching Stage

For small LO amplitude, the amplitude of the output depends on the amplitude of the LO signal. Thus, gain is larger for larger LO amplitude. For large LO signals, the upper quad switches and no further increase occur. Thus, at this point, there is no longer any sensitivity to LO amplitude. Besides, if upper quad transistors are alternately switched between completely off and fully on, the noise will be minimized. Since upper transistor contributes no noise when it is fully off, and when fully on, the upper transistor behaves like a cascade transistor which does not contribute significantly to noise.

The large LO signal is required to let upper quad transistors achieve complete switching. But if the LO voltage is made too large, a lot of current has to be moved

into and out of the transistors during transitions. This can lead to spikes in the signals and can actually reduce the switching speed and cause an increase in LO feed-through. Thus, too large a signal can be just as bad as too small a signal.

2.5.3 Mixer Noise

Noise figure for a mixer is defined as

$$\text{noise factor} = \frac{\text{total output noise power at the IF}}{\text{output noise power at IF due to input source}} \qquad (2\text{-}24)$$

In general, the noise figure of the mixer is divided to two categories, single-sideband (SSB) noise figure and double-sideband (DSB) noise figure. The difference between the two definition is the value of the denominator in (2-24). In the case of SSB noise figure, only the noise at the output frequency due to the source that originated at the RF frequency is considered, and it is usually used in heterodyne systems. In the case of DSB noise figure, all the noise at the output frequency due to the source is considered (noise of the source at input and image frequencies), and it is usually used in homodyne system.

Because of the added complexity and the presence of noise that is frequency translated, mixers tend to be much noisier than LNAs. In generally, mixers have three frequency bands where noise is important:

(1) Noise already presents at the IF: The transistors and resistors in the circuit will generate noise at the IF. Some of this noise will make it to the output and corrupt the signal.

(2) Noise at the RF and image frequency: The noise presents at the RF and image frequency will be mixed down to the IF.

(3) Noise at multiples of the LO frequencies: Any noise that is near a multiple of the LO frequency can also be mixed down to the IF, just like the noise at the RF.

Besides, the flicker noise will become more important in the homodyne receiver. In the design of the direct down-conversion mixer, how to reduce the flicker noise of upper quad transistors is the important thing. This noise can be reduced by increasing the device size for a given g_m.

2.5.4 Port-to-Port Isolation

The isolation between each two ports of a mixer is critical. The LO-RF feed-through results in LO leakage to the LNA and eventually the antenna, whereas the RF-LO feed-through allows strong interferers in the RF path to interact with the local oscillator driving the mixer. The LO-IF feed-through is important because if substantial LO signal exists at the IF output even after low-pass filtering, then the following stage may be desensitized. Fortunately, this feed-through can be reduced largely be used the double-balanced architecture. Finally, the RF-IF isolation determines what fraction of the signal in the RF path directly appears in the IF, a critical issue with respect to the even-order distortion problem in homodyne receivers.

The required isolation levels greatly depend on the environment in which the mixer is employed. If the isolation provided by the mixer is inadequate, the preceding or following circuits may be modified to remedy the problem.

Chapter 3

Low Power Ultra-Wideband Active Balun

3.1 Introduction

New low-power CMOS active baluns are designed for ultra-wideband applications, using a pair of common-source NMOS and common-gate PMOS transistors.

This chapter will be divided into two sections. Section 3.2 addresses the new architecture of 8 GHz low power ultra-wideband active balun. Section 3.3 delineates the improved low power ultra-wideband active balun with tunable ability for process variation.

3.2 Low Power Ultra-Wideband Active Balun

3.2.1 8 GHz Low Power Ultra-Wideband Active Balun

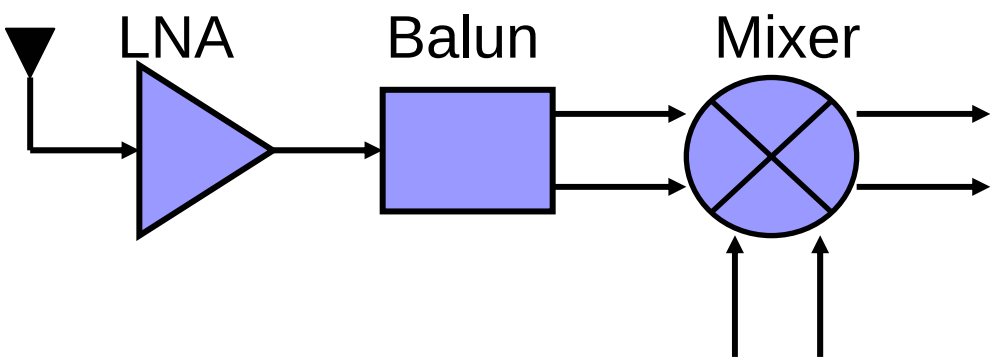


Fig. 3.1 Front-End

Balun circuits are the critical block required in RF and microwave circuits whereas signal in a balanced format is necessary. An ideal differential balun generate a

pair of differential output signals of balanced amplitudes and phases (0 dB gain difference and 180° phase difference) from a single input. The proposed balun is designed for the front-end application in Fig. 3.1. For ultra wideband, low power and small area, active balun with limited power consumption is a better choice.

Like mentioned, it is very popular to apply the configuration of a differential amplifier as active balun at high frequency. But infinite impedance at the current source limits the bandwidth. And two DC branches need twice DC power consumption. Higher power consumption limits the value of this kind of active balun, too. I use a PMOS to replace a NMOS (M2) in Fig. 3.2., and apply the folded topology . The NMOS Mn and PMOS Mp both connect at the source ports.

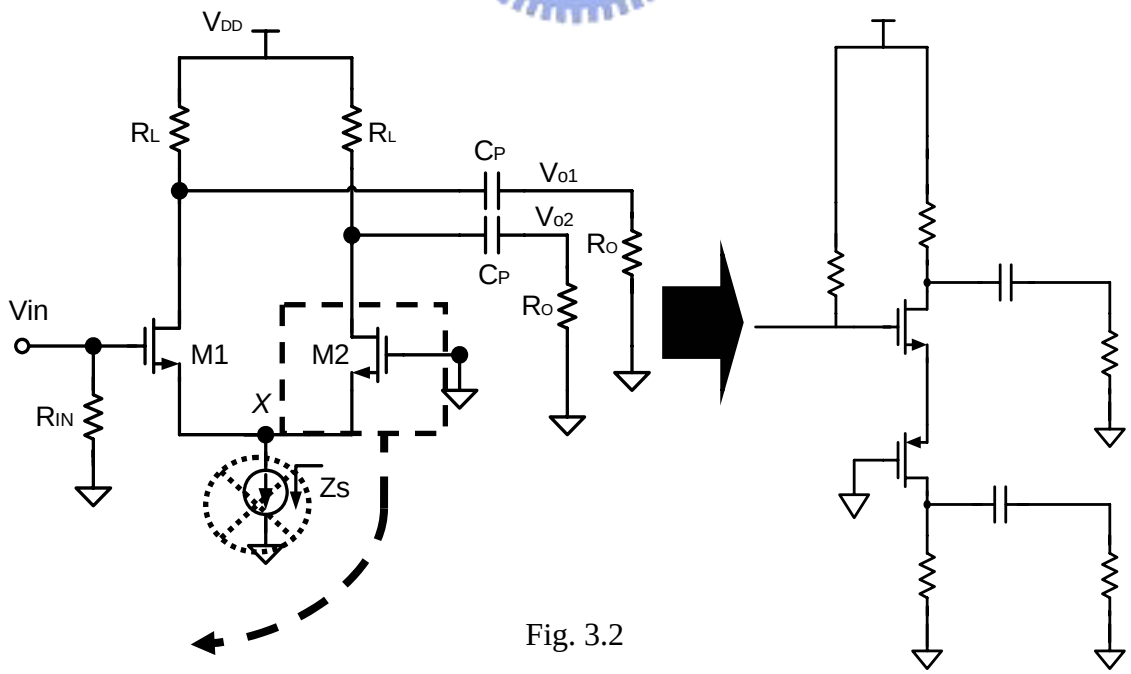


Fig. 3.2

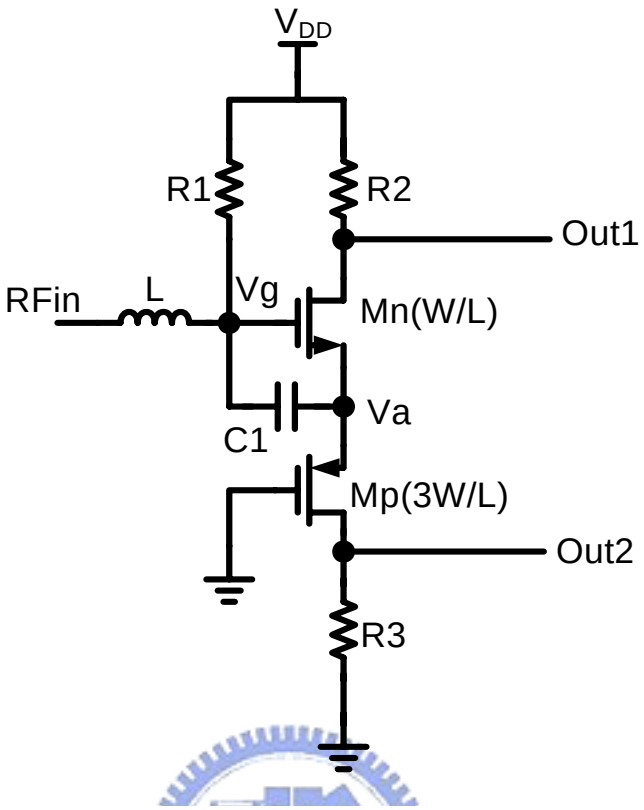


Fig. 3.3. Schematic of the proposed balun circuit.

Fig. 3.3. shows the schematic of the proposed balun circuit, which consists of an NMOS and a PMOS pair. The two transistors, connected both at the source ports, are configured in a manner that the NMOS is as common-source, while the PMOS as common-gate. Reused DC biasing current greatly reduces power consumption. Another viewpoint of this circuit reveals that the differential amplifier can be considered as a folded topology of this new balun. The common-source node at V_a corresponds to the current-source node in a differential amplifier. Without using a current source, this proposed balun needs no feedback compensation for gain and phase imbalance. The gate ports are directly DC-connected to V_{DD} and the ground, respectively. The resistors

R_2 and R_3 provide DC biasing and output loading. The values must be carefully chosen to sustain proper biasing of the transistor pair in the saturation condition. Actually the biasing current shall be small. As such, the V_a is biased at the DC voltage around $V_{DD}/2$. The impedance matching components, R_1 and L, are for measurement purpose. In a fully integrated system they might be unused when combined with a previous stage. This proposed balun circuit is advantageous in less circuit complexity, die area, and dc current.

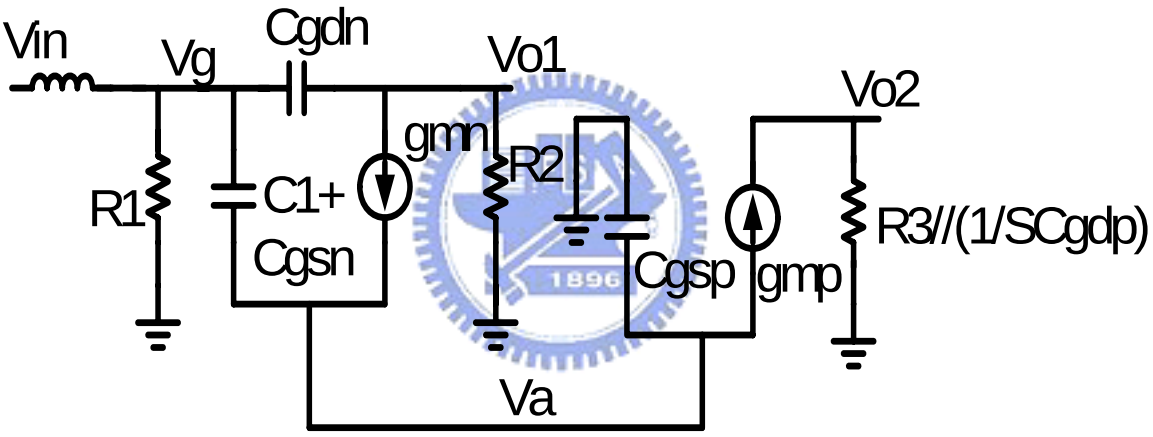


Fig. 3.4. Small-signal equivalent circuit model of the proposed balun circuit.

The small-signal equivalent circuit is as shown in Fig. 3.4. Critical to affect output imbalance, the gate-drain parasitic capacitance, C_{gd}, shall be included in the analysis. Derived from the core circuit, the common-source voltage, v_a, is related to the gate voltage, v_g, as

$$v_a = v_g \frac{g_{mn} + sC_{gsn}}{g_{mn} + s(C_1 + C_{gsn}) + g_{mp} + sC_{gsp}} \qquad (3\text{-}1)$$

If the voltage v_a is one half of the gate voltage v_g, two outputs can reach a well-balanced condition. This leads to the requirement of $g_{mn} = g_{mp}$ and $C_1+C_{gsn} = C_{gsp}$. To do so, the PMOS size is chosen as three times of the NMOS size. An external capacitor, C_1, is also added for the latter requirement. Under these conditions, the voltage ratio of the two outputs is given by

$$\frac{v_{o1}}{v_{o2}} = -\frac{R_2(0.5g_m - sC_{gdn})}{1 + sC_{gdn}R_2} \cdot \frac{1 + sC_{gdp}R_3}{0.5g_m R_3} . \qquad (3\text{-}2)$$

As can be seen, the impedance matching components affect no gain and phase imbalance. A balanced output demands $v_{o1} = -v_{o2}$. If biasing current is large, then $g_m >> \omega C_{gdn}$ and the condition is fulfilled. In low-power cases, the condition can be fulfilled if the values of R_2 and R_3 follow these equations,

$$R_3 = \frac{2C_{gdn}}{g_m(C_{gdp} - C_{gdn})} \text{, and } \frac{1}{R_2} = \frac{1}{R_3} + \frac{2\omega^2 C_{gdn} C_{gdp}}{g_m} . \qquad (3\text{-}3)$$

As $g_m >> 2\omega^2 C_{gdn} C_{gdp}$ in the frequency range of interest, the choice of R_2 an R_3 holds over a broad frequency range. It concludes that the effect on imbalance from the transistor parasitic is less than that from the compensation feedback and the current source parasitic.

3.2.2 Microphotograph of Chip

A balun circuit was designed in a standard 0.18um CMOS technology. Fig. 3.5. shows the micrograph of the fabricated circuit. The total chip area is 0.57mm by 0.68mm including bonding pads for on-wafer probing measurements. The area of the core circuit could be much reduced in a fully integrated circuit. The RF input and output ports are placed on the opposite sides of the chip to improve the isolation.

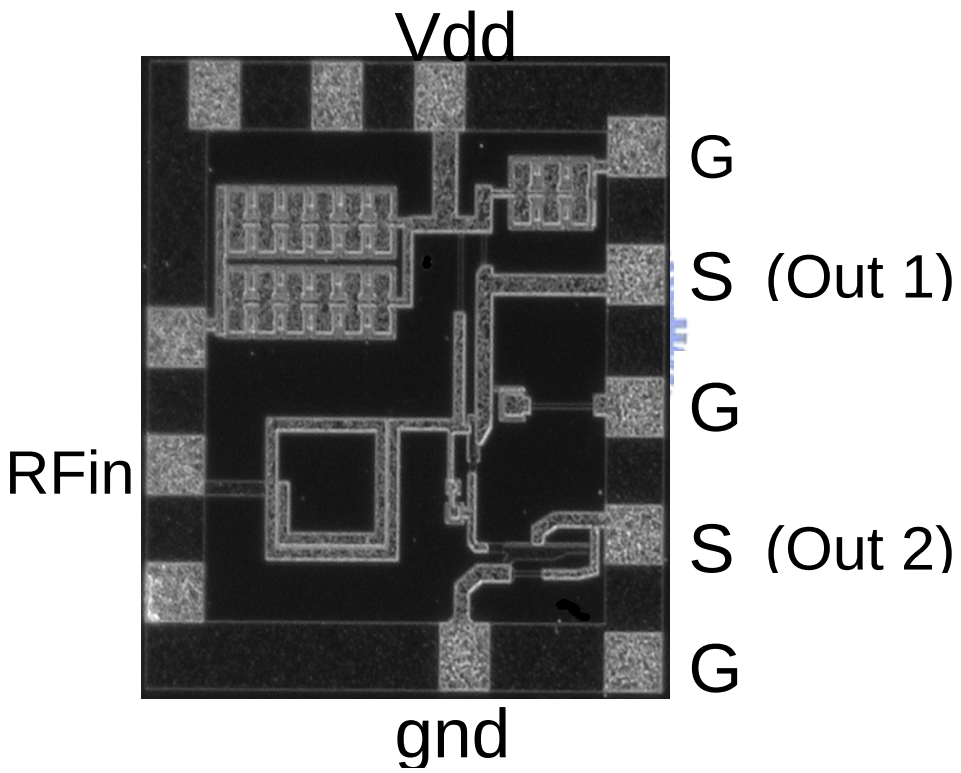


Fig. 3.5. Micrograph of the fabricated active balun.

3.2.3 Simulation and Measurement results and Discussion

The load impedance at each output port is the same as the source of 50-Ω. As such, the circuit presents an impedance transformation ratio of 1:2. Specified for ultra-wideband application, the design is optimized at the frequency of 8-GHz for minimum phase error and gain imbalance based on Eq. (3-3). The ideal design gives gain and phase imbalance of ±1dB and ±1.5°, respectively, up to 11-GHz. Post-layout simulation shows that the circuit achieves imbalance of 2dB and 3° up to 8-GHz. This circuit could operate under supply voltage variation from 1.2V to 1.5V with reasonable balanced outputs. It consumes a power level of only 1.44mW, much less than those of previous work.

The measurement results of the gain difference and the phase difference are shown in Fig. 3.6. and Fig. 3.7. It shows good agreement with post-layout simulations, except at frequencies higher than 6-GHz. The discrepancy of phase difference arises from measurements conducted by two-port on-wafer probing tests. Although probe parasitic are well calibrated for the two ports under test, the third port is terminated into an un-calibrated probe. The unexpected parasitic greatly affects measurements accuracy, especially for phase imbalance. It is found that by adding a parasitic inductance of 50fH at the third port output, simulation data approaches to measurement data. The issue could be resolved by four-port measurements.

As to the discrepancy of gain difference, it is due to the unaccounted parasitic at the gate-port of the PMOS. It turns out the gain balance is quite sensitive to an inductive parasitic at this location.

The measured IIP3 and noise figure at the OUT1 port are shown in Fig. 3.8 and Fig. 3.9, respectively. The OUT2 port is terminated with a 50Ω resister. The circuit does give good linearity performance over the entire frequency range. Note that the noise performance is degraded by the matching resistor R1. This could be improved in a fully integrated environment without R1. Later Fig 3.13 will show the difference of NF between having R1 and without R1.

The measured S11 and measured S22 are shown in Fig. 3.10. S12 is better than -20dB from 0 to 8GHz. Fig.3.11 shows the measured differential gain. According to the simulated differential gain, the differential gain should have a pretty flat gain property. The mean of the simulated differential gain is about -2dB. The variation of the simulated differential gain is below ±0.5dB. We can observe the slop of the measured differential gain increases. The variation of the measured differential gain increases to ±1.5dB. The parasitic inductance of 50fH at the third port output and the process variation cause this result.

For input impedance matching, using small resister R1 about 100Ω to let S11 to be below -10dB from 0 to 10 GHz. But some part of the signal power flow through

this path to ground. Small resister R1 will causes lower differential gain and higher noise figure. The simulated differential gain without R1 and the simulated noise figure without R1 are shown in Fig. 3.12 and in Fig. 3.13, respectively. We can notice the differential gain improve greatly and so does NF. The performance of this active balun is summarized in Table 3.1. We can observe the advantages of the proposed active balun are more wide bandwidth and less power consumption.

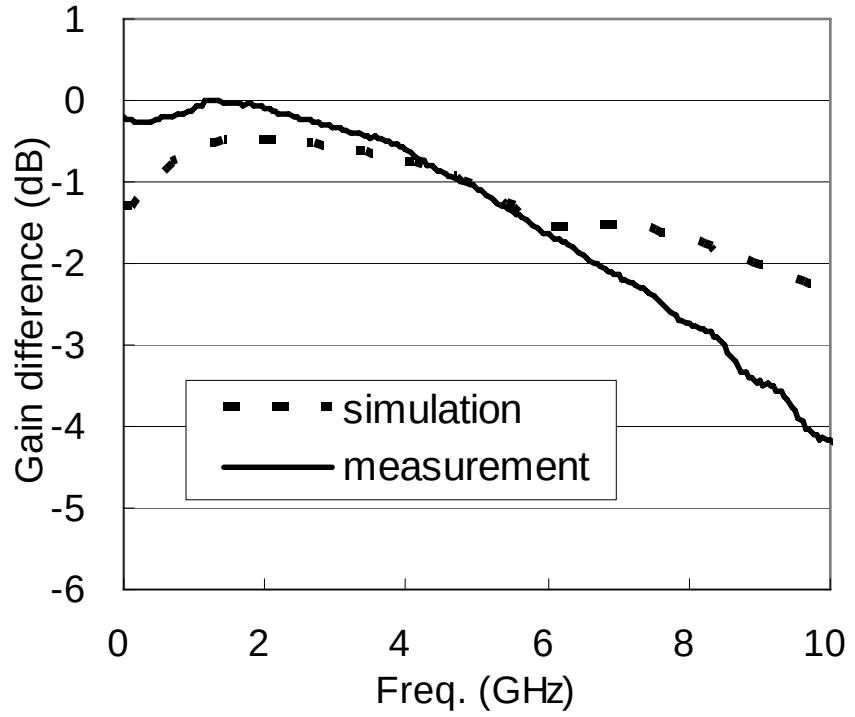


Fig. 3.6. Measured data and simulation of gain difference.

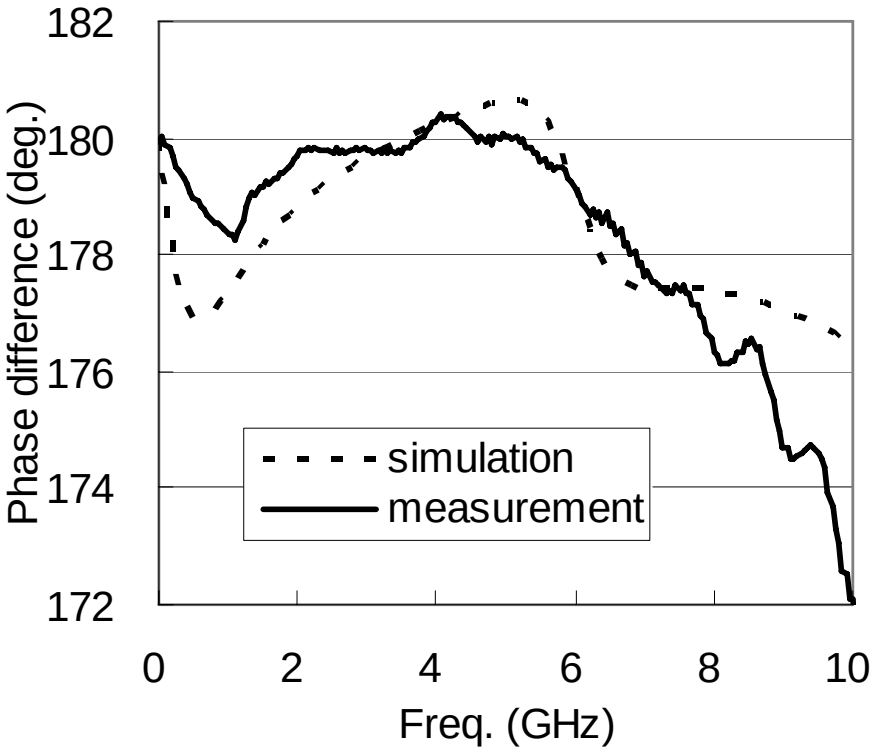


Fig. 3.7. Measured data and simulation of phase difference.

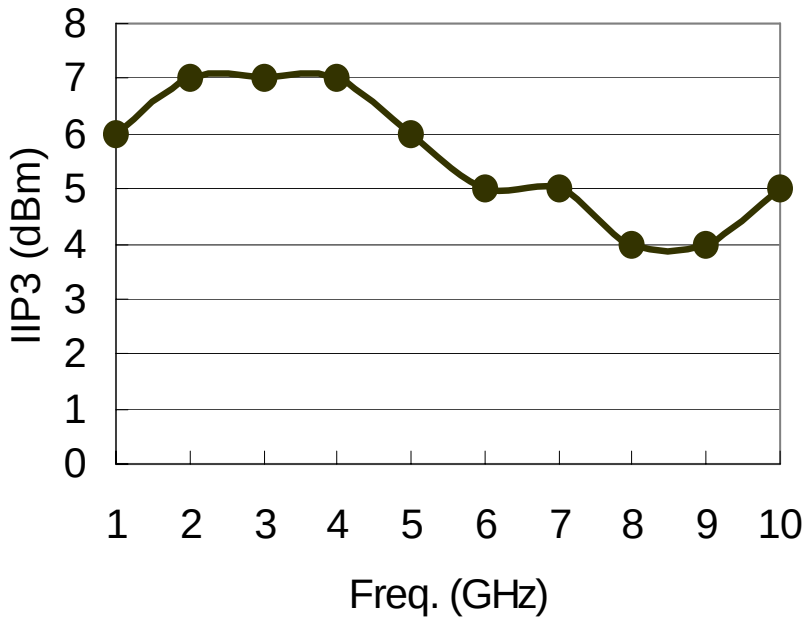


Fig. 3.8. Measured IIP3 of the active balun.

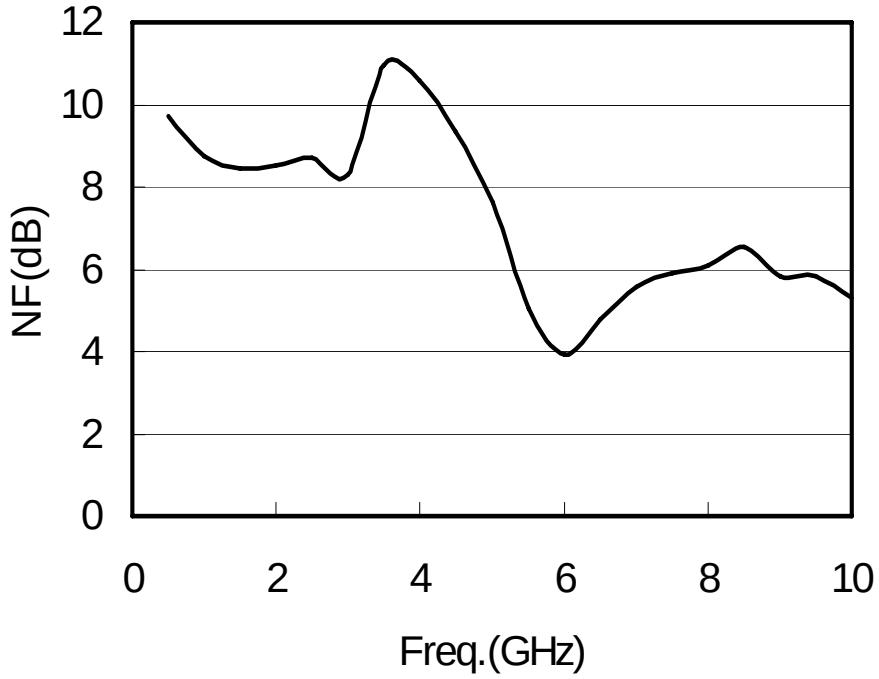


Fig. 3.9. Measured NF

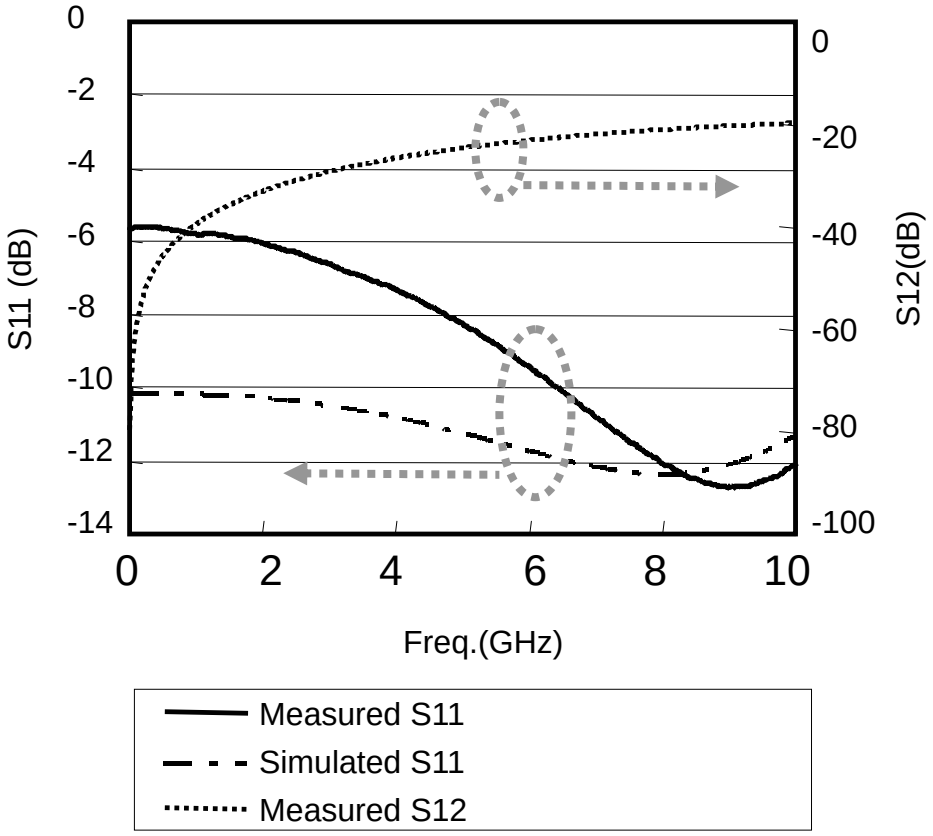


Fig. 3.10. Measured S11 and Measured S12.

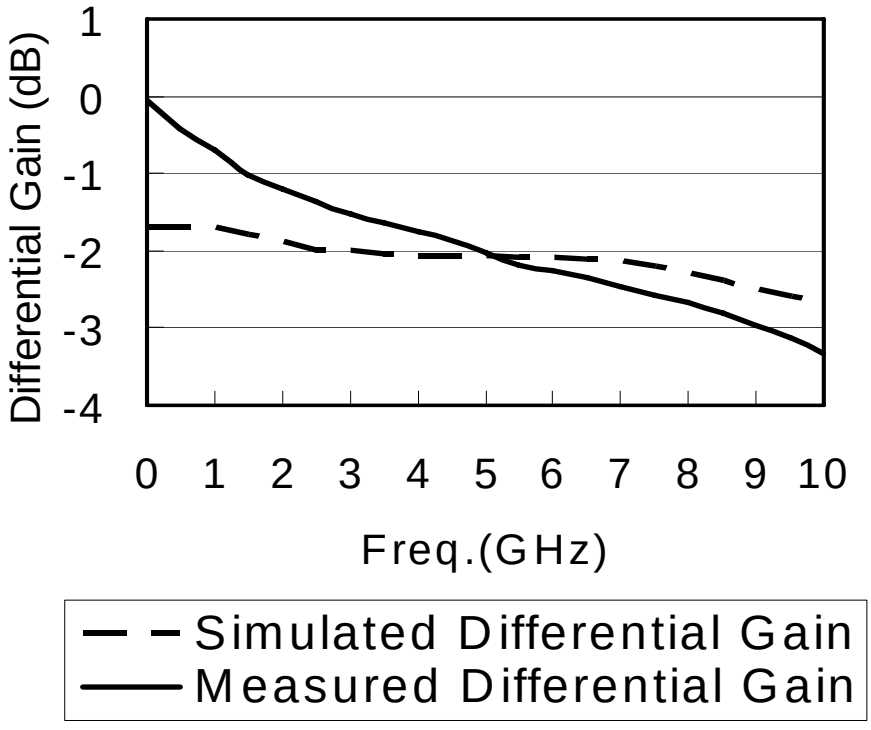


Fig. 3.11. Measured Difference Gain.

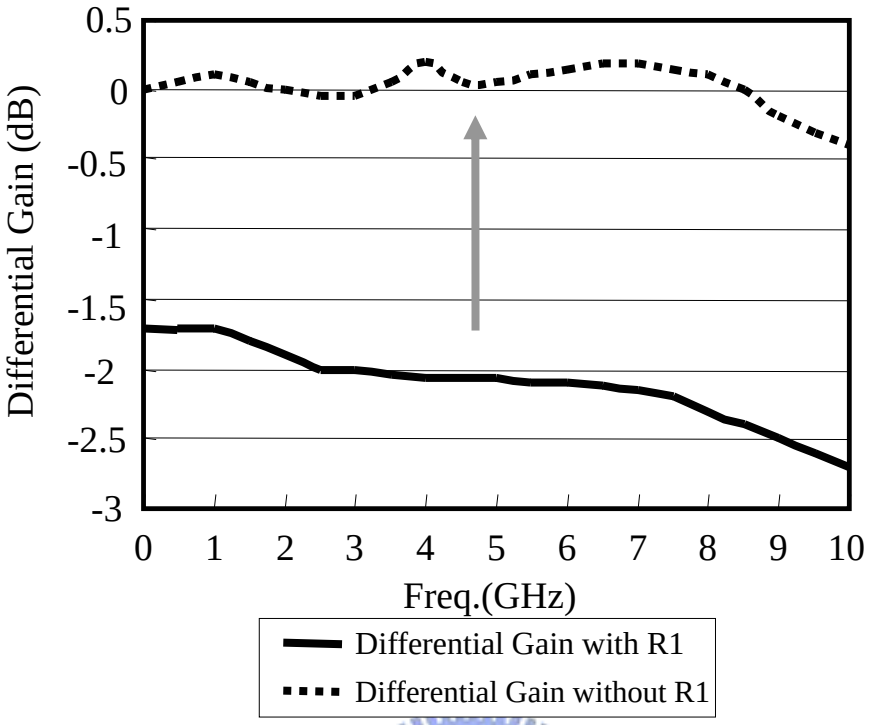


Fig. 3.12. Simulated Differential Gain without R1.

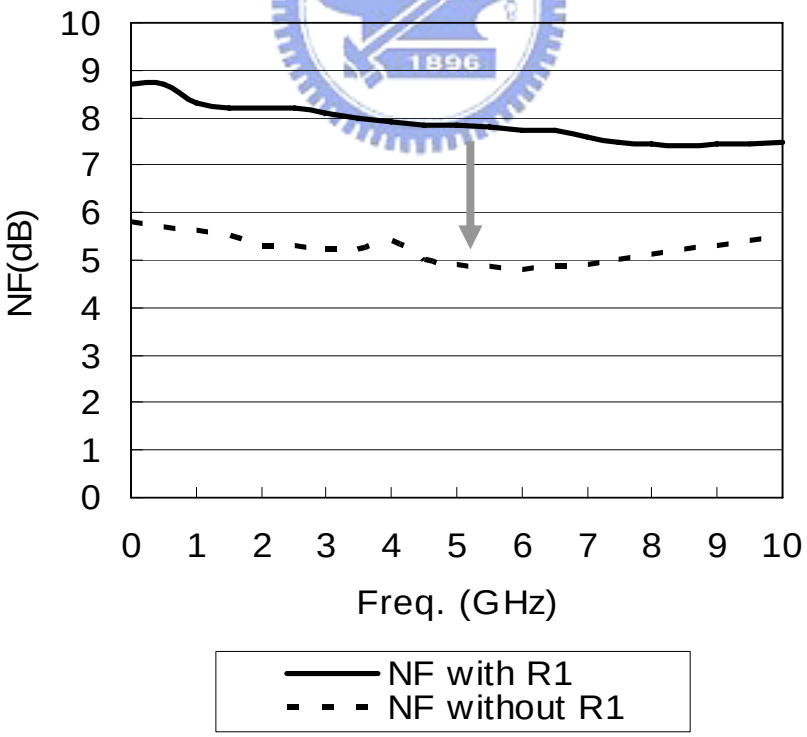
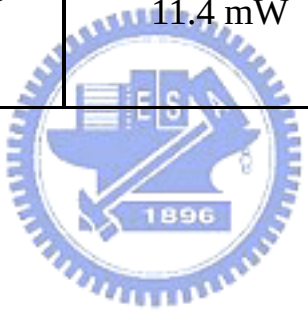


Fig. 3.13. Simulated NF without R1.

TABLE 3.1 Summary of measured performance and comparison to other active balun

	This work	**[7]** ***MTT '98***	**[8]** ***ISCAS '03***
Vdd	1.2V	3V	3V
Gain error	2dB	±1 dB	0.02 dB
Phase error	3 °	-1°	0.58 °
Freq.	~8 GHz	1.7 ~ 5.8 GHz	5.1 ~ 5.9 GHz
Power consumption	1.44 mW	11.4 mW	9.17 mW



3.3 Improved Low Power Ultra-Wideband Active Balun

Discussed in section 3.2, the gain error and phase error rise when frequency increase. According to the measurement result, we can find out two critical effects cause this result. First is the measurement environment. As mentioned, the probe parasitic are well calibrated for the two ports under test, the third port is terminated into an un-calibrated probe. The unexpected parasitic greatly affects measurements accuracy, especially for phase imbalance. It is found that by adding a parasitic inductance of 50fH at the third port output, simulation data approaches to measurement data. But this issue could be resolved by four-port measurements.

Second, unpredictable effects like process variation will affect the measurement result, too. Process variation will affect the circuit itself and change the output loading (the input impedance of the next stage). It is difficult to prevent this issue. So the active balun with a tunable function to calibrate the mismatch from the process variation is necessary.

And when active baluns combine with the next stage, the input impedance of the next stage (the output loading of the active balun) may changes. So it is necessary to see the variation of the gain difference and the phase difference when the RL in Fig. 3.14 changes. GD(200) and PD(200) mean the gain difference and the phase difference when RL in Fig. 3.14 equals 200Ω, respectively. We can observe the gain difference and the

phase difference both increase when RL increases in Fig. 3.15. So we need to design a tunable active balun for the output loading variation.

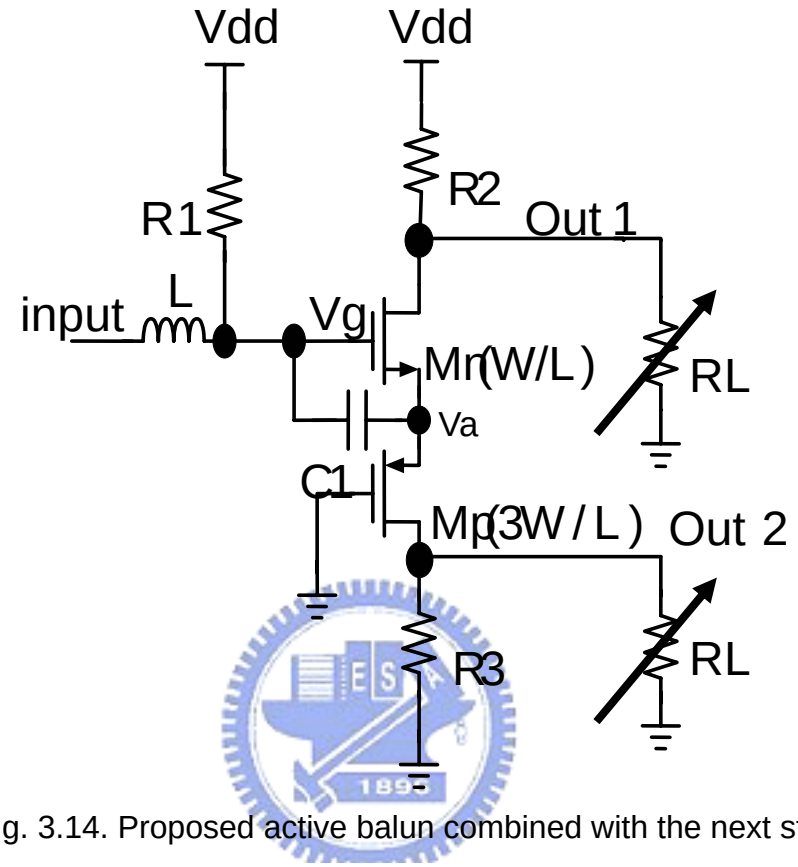


Fig. 3.14. Proposed active balun combined with the next stage.

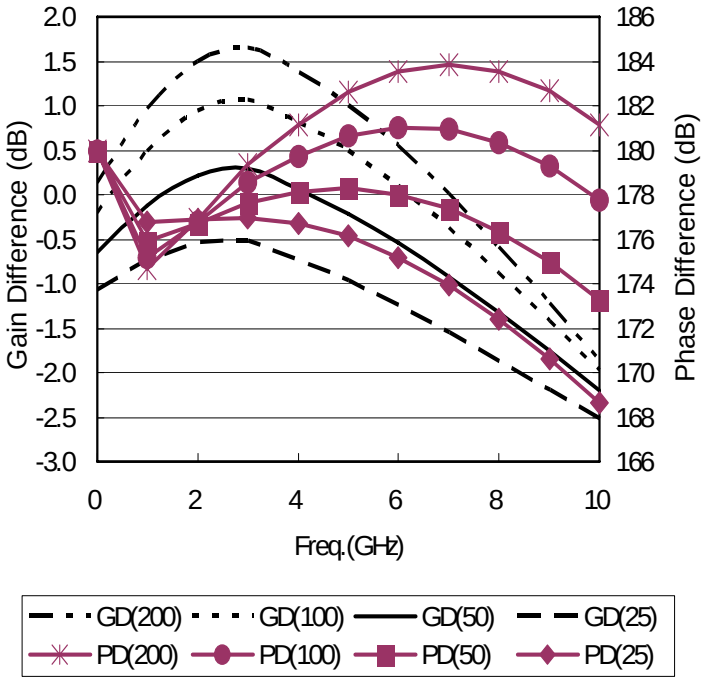


Fig. 3.15. The simulated gain difference and phase difference with difference RL.

3.3.1 Design on 0~10 GHz Ultra Wide-Band Low Power Tunable Active Balun for Loading Variation and Process Variation Compensation

The tunable ultra wide-band active balun is shown in Fig. 3.16. According to Eq. (3-3), as $g_m >> 2\omega^2 C_{gdn} C_{gdp}$ in the frequency range of interest, the choice of R_2 an R_3 in Fig. 3.3 holds over a broad frequency range. Appropriate *R2* and *R3* can make minimum gain and phase error over the desirable bandwidth. So, use an active tunable resister M1 to replace R2 in Fig. 3.3 for tuning if it is necessary.

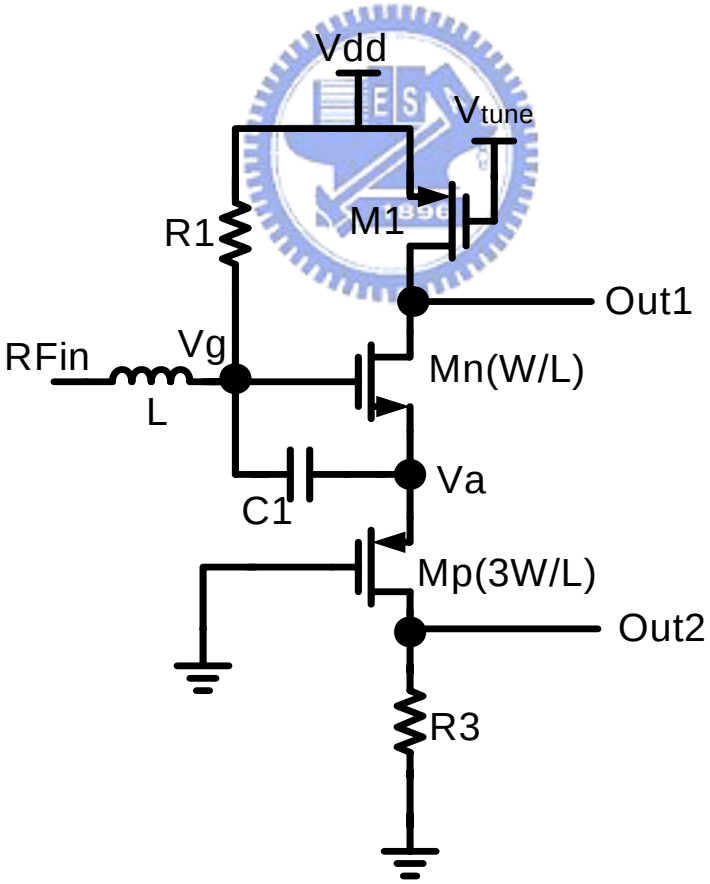


Fig. 3.16. The proposed tunable active balun.

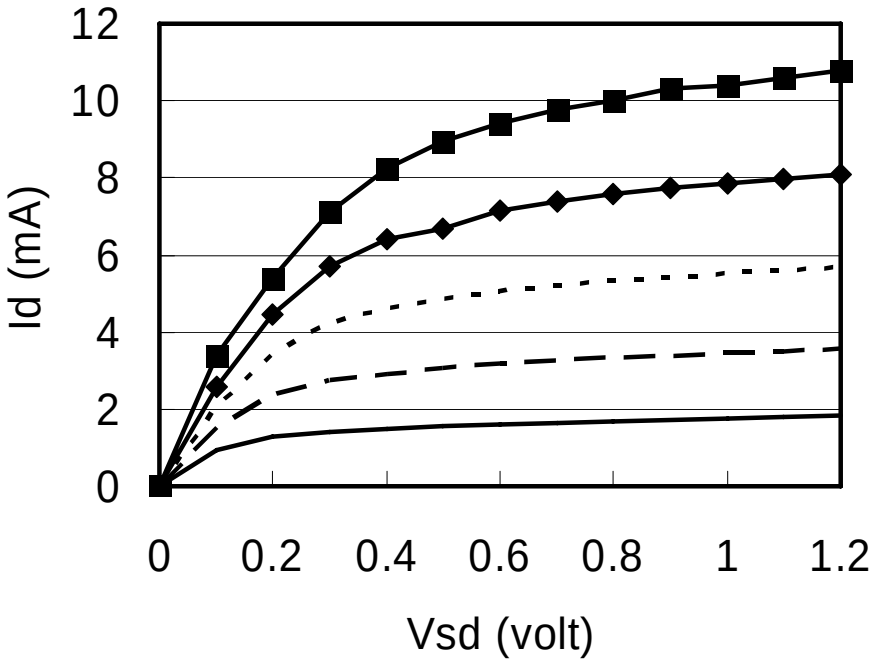


Fig. 3.17. PMOS I_V curve.

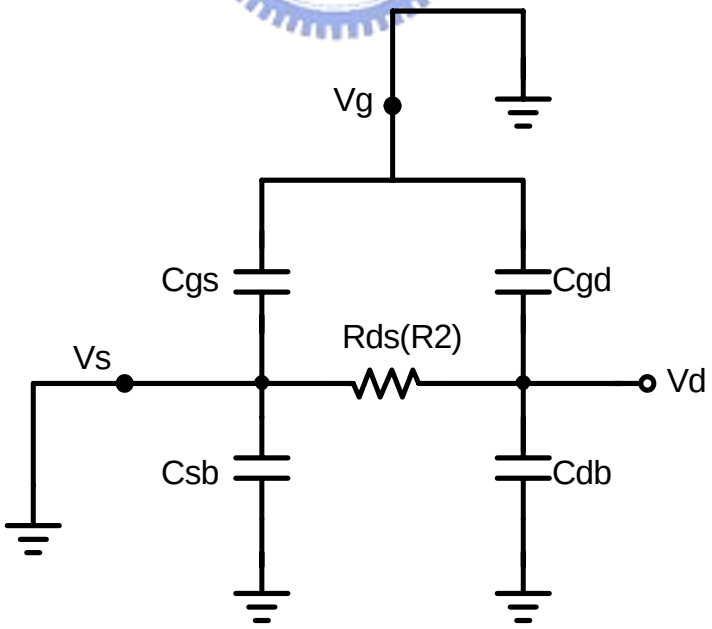


Fig. 3.18. The equivalent model of the PMOS M1on the triode region.

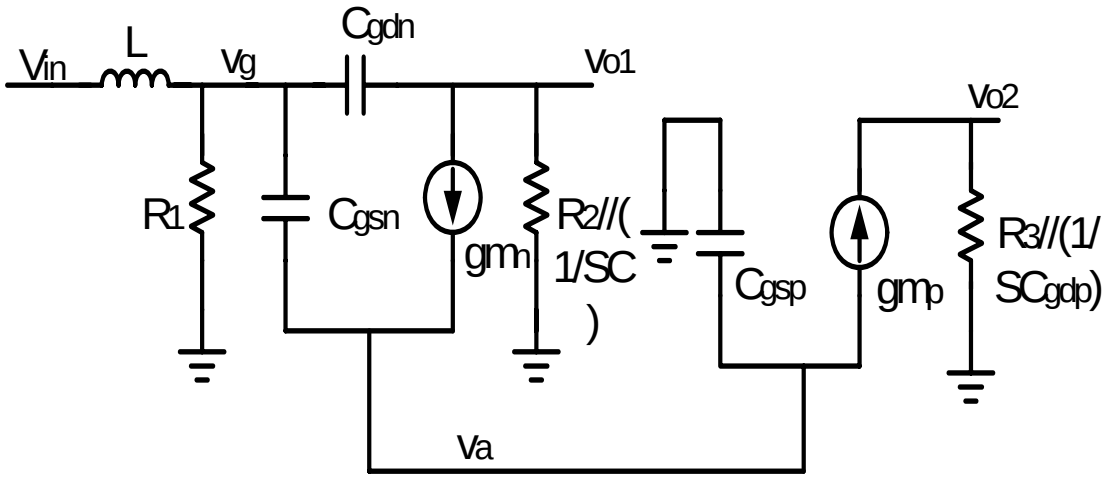


Fig. 3.19. Small-signal equivalent circuit model of the proposed tunable balun circuit.

The PMOS M1 works in the triode region. The I_V curve of the PMOS is shown in Fig. 3.17. On the triode region, MOS can be an active resister. When tuning V_{SG} of the PMOS, the value of the active resister Rds ($\frac{dVsd}{dId}$) changes. The equivalent model of the PMOS in the triode region shows in Fig. 3.18. Cgs and Csb of PMOS M1 can be ignored because Vg and Vs in Fig. 3.17 connect to ground directly. Let Rds as R2 and $Cgd // Cdb = C$.

The small-signal equivalent circuit is as shown in Fig. 3.19. Critical to affect output imbalance, the gate-drain parasitic capacitance, C_{gd}, shall be included in the analysis. Derived from the core circuit, the common-source voltage, v_a, is related to the gate voltage, v_g, as

$$v_a = v_g \frac{g_{mn} + sC_{gsn}}{g_{mn} + s(C_1 + C_{gsn}) + g_{mp} + sC_{gsp}} \qquad (3\text{-}4)$$

If the voltage v_a is one half of the gate voltage v_g, two outputs can reach a well-balanced

condition. This leads to the requirement of $g_{mn} = g_{mp}$ and $C_1+C_{gsn} = C_{gsp}$. To do so, the PMOS size is chosen as three times of the NMOS size. An external capacitor, C_1, is also added for the latter requirement. Under these conditions, the voltage ratio of the two outputs is given by

$$\frac{v_{o1}}{v_{o2}} = -\frac{(R_2 // \frac{1}{sC})(\frac{1}{2}g_m - sC_{gdn})}{1+sC_{gdn}(R_2 // \frac{1}{sC})} \bullet \frac{1+sC_{gdp}R_3}{\frac{1}{2}g_m R_3} \qquad (3\text{-}5)$$

As can be seen, the impedance matching components affect no gain and phase imbalance. A balanced output demands $v_{o1} = -v_{o2}$. If biasing current is large, then $g_m >> \omega C_{gdn}$ and the condition is fulfilled. In low-power cases, the condition can be fulfilled if the values of R_2 and R_3 follow these equations,

$$R_3 = \frac{2C_{gdn}}{g_m(C_{gdp}-C_{gdn})}, \text{ and } \frac{1}{R_2} \cong \frac{1}{R_3} + \frac{2\omega^2 C_{gdn}C_{gdp}}{g_m}. \qquad (3\text{-}6)$$

As $g_m >> 2\omega^2 C_{gdn}C_{gdp}$ in the frequency range of interest, the choice of R_2 an R_3 holds over a broad frequency range. It concludes that the effect on imbalance from the transistor parasitic is less than that from the compensation feedback and the current source parasitic.

When process variation occurs, gain error and phase error will rise. Tuning the gate voltage of the PMOS M1 to changes the value of R2 to minimize the mismatch. Fig. 3.20 and Fig. 3.21 show phase difference and gain difference shift when the gate

voltage of the PMOS M1 changes. As the gate voltage of the PMOS M1 rise 0.1V, gain difference and phase difference shift 1dB and 1.5°, respectively. According to the simulated result, when the output loading changes from 25 to 200Ω, the improved active balun still can achieves the desired performance. For constant DC power consumption, the bottleneck of the DC current is on the PMOS Mp not PMOS M1. So, when tuning the value of R2, DC power consumption almost will not increase.

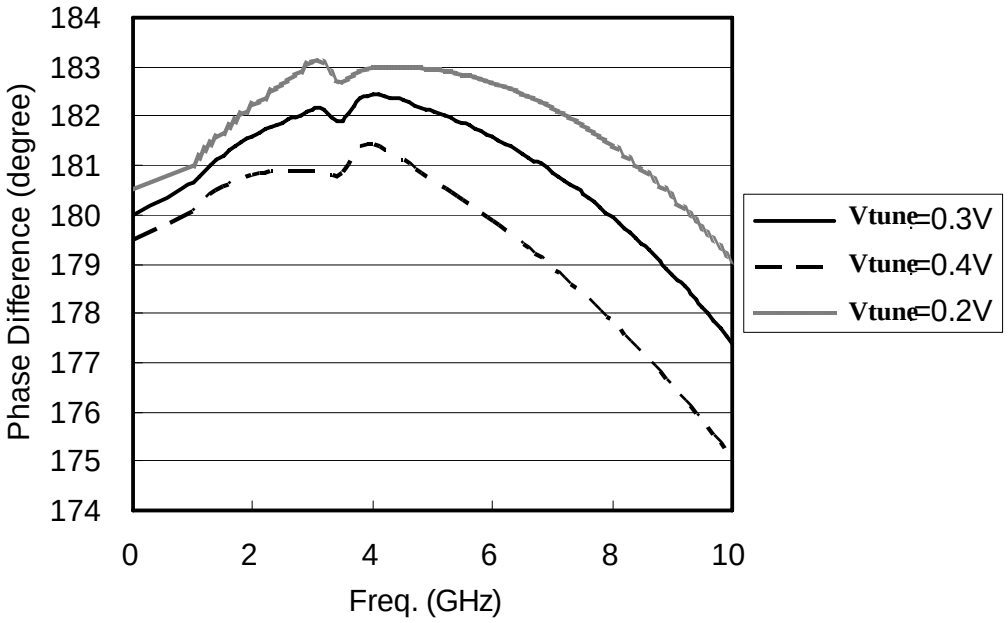


Fig. 3.20. Phase difference vs. Vtune.

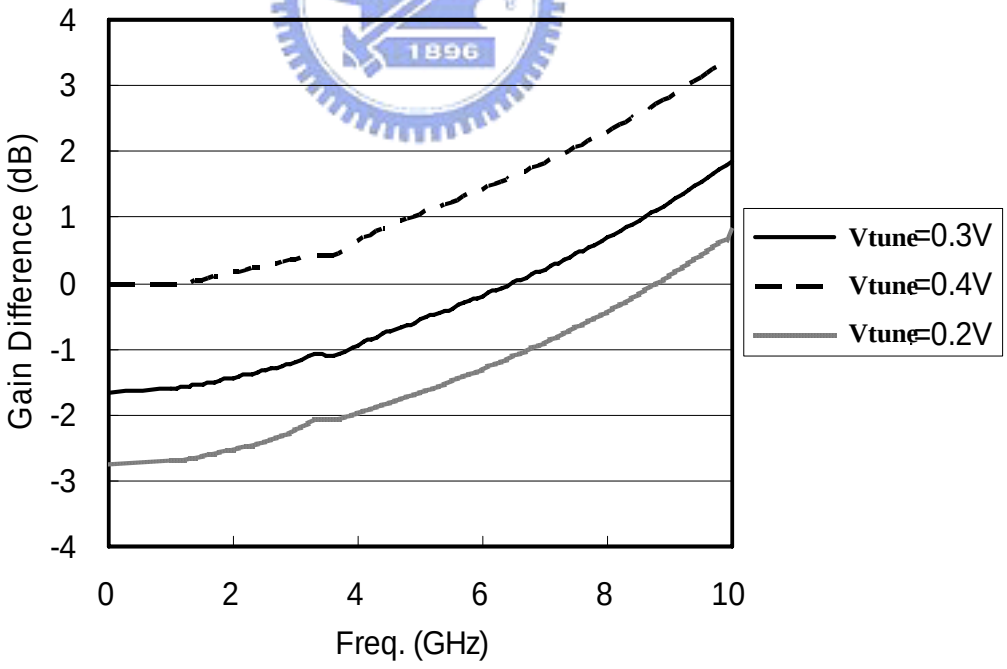


Fig. 3.21. Gain difference vs. Vtune.

3.3.2 Microphotograph of Chip

A tunable balun circuit was designed in a standard 0.18um CMOS technology. Fig. 3.22 shows the micrograph of the fabricated circuit. The total chip area is 0.5mm by 0.68mm including bonding pads for on-wafer probing measurements. The area of the core circuit could be much reduced in a fully integrated circuit. The RF input and output ports are placed on the opposite sides of the chip to improve the isolation. According to the last measurement result of the 8GHz ultra wideband active balun, we find out there is the unaccounted parasitic at the gate-port of the PMOS resulting in higher gain error. So adding bypass capacitors to prevent this issue.

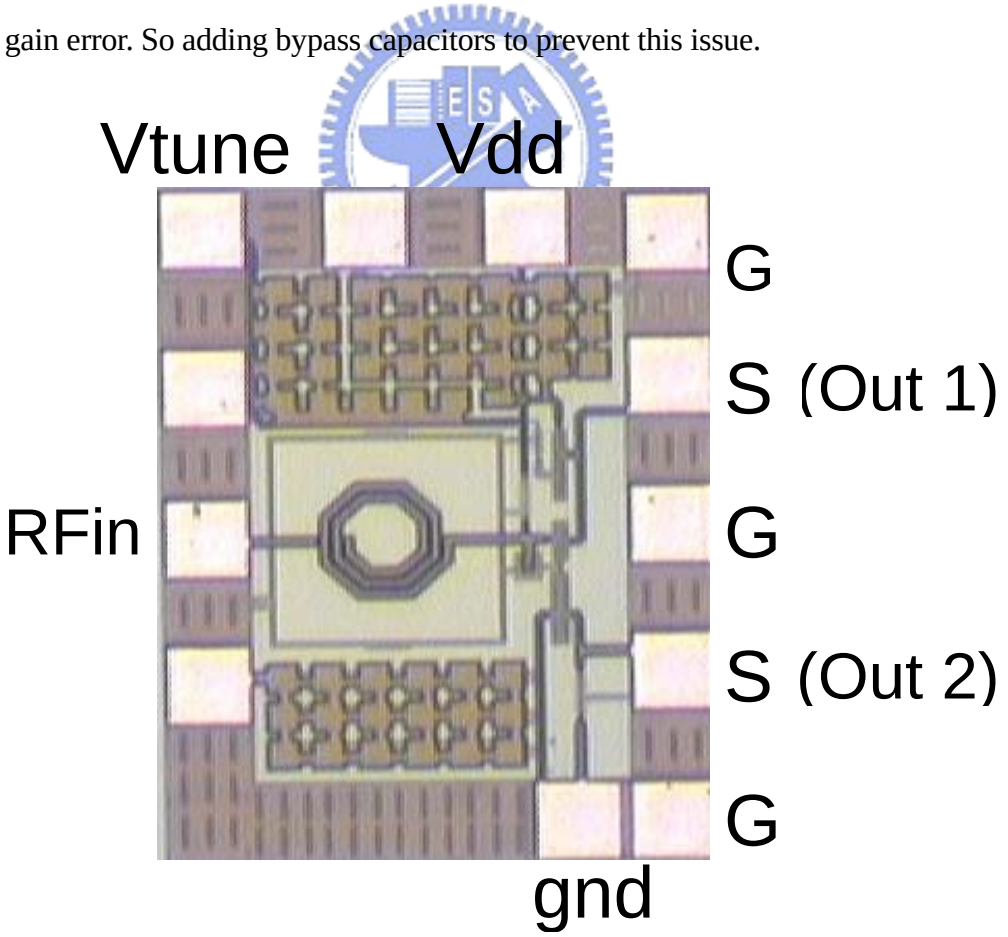


Fig. 3.22. Micrograph of the fabricated tunable active balun.

3.3.3 Simulation and Measurement results and Discussion

The load impedance at each output port is the same as the source of 50-Ω. As such, the circuit presents an impedance transformation ratio of 1:2. Specified for ultra-wideband application, the design is optimized at the frequency of 8-GHz for minimum phase error and gain imbalance based on Eq. (3-6). The ideal design gives gain and phase imbalance of ±1dB and ±2°, respectively, up to 10-GHz. Post-layout simulation shows that the circuit achieves imbalance of 2dB and 3° up to 10-GHz. The optimized frequency shifts from 8-GHz to 6-GHz when Vtune rise from 0.3V to 0.4V. Based on process variation, choosing the appropriate value of Vtune to minimize gain error and phase error. This circuit operates under supply voltage 1.2V with reasonable balanced outputs.

According to the DC measured result, the DC current of this proposed tunable active balun chip reduces greatly to only 0.75mA. 0.75mA is much less than post-layout simulation about 1.2mA. The DC current under Slow/Slow corner test is 0.65mA much close to the DC measured result. Fig. 3.23 shows the method to measure I_V curve of the active resister M1 to hope to find out the reason of the DC mismatch. Add a bias tee at the output 1 and measure the DC current flow through from Vdd.

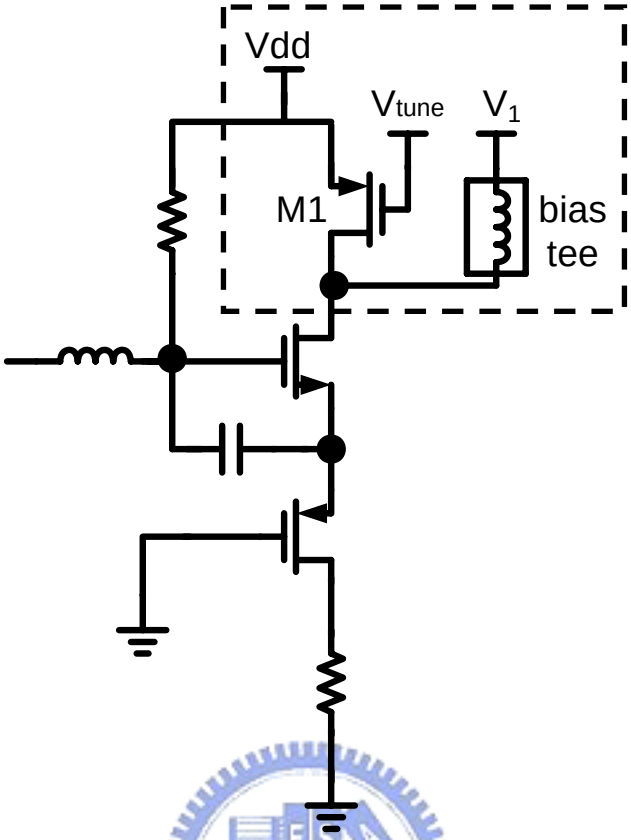


Fig. 3.23. Measure I_V curve of the active resister.

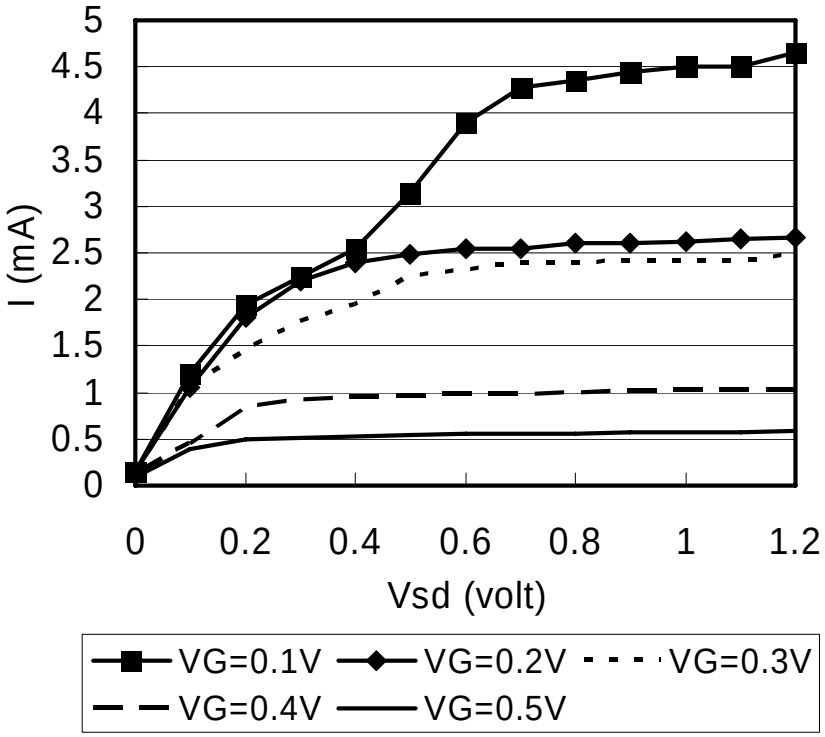


Fig. 3.24. Measured I_V curve of the active resister M1.

Fig. 3.24 shows the measured I_V curve of the active resister. The measured I_V curve of the active resister compares with the simulated I_V curve under the typical/typical and slow/slow corner test is shown in Fig. 3.25 (Vdd = 1.2V, Vtune = 0.3V). We can observe the measured I_V curve is even less than the simulated I_V curve under the slow/slow corner test. Fig. 3.26 shows the DC voltage at node A and node B. DC voltage gives a good agreement with simulation. The voltage at node B reduces because DC current decreases. DC current mismatch will affects the performance of the proposed tunable active balun greatly.

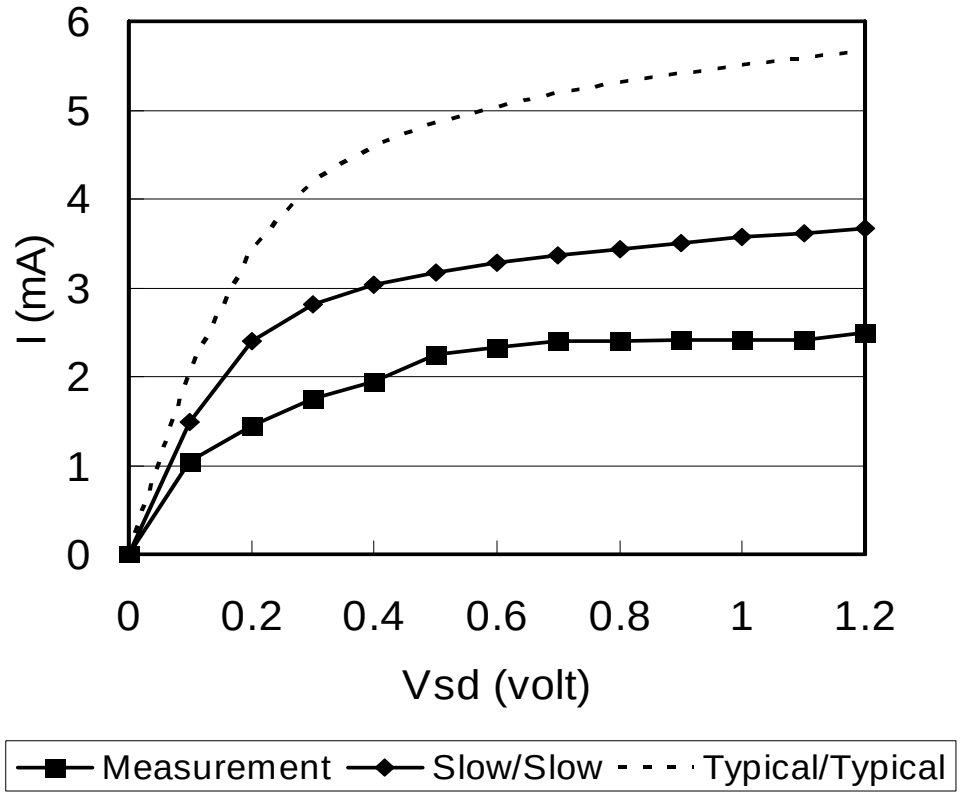
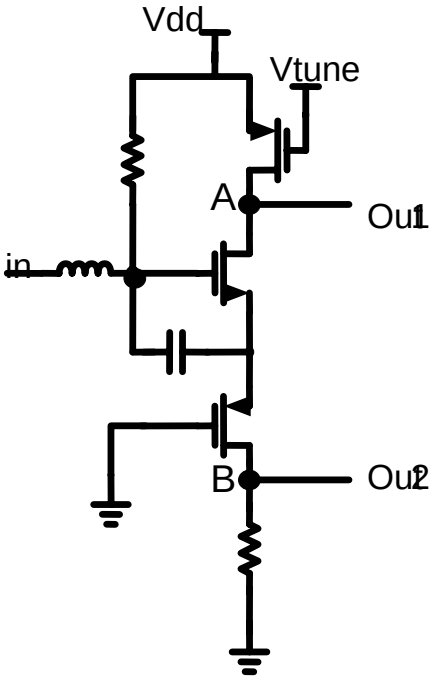


Fig. 3.25. The measured I_V curve of the active resister compared with the simulated IV curve under TT & SS corner test.



	DC current	V_A	V_B
Simulation	1.2mA	1.11V	0.12V
Mea1	0.756mA	1.09V	0.067V
Mea2	0.762mA	1.09V	0.068V
Mea3	0.778mA	1.09V	0.068V

Fig. 3.26. DC voltage at node A and node B.

The measured S11 and measured S12 are shown in Fig. 3.27. S12 is better than -20dB from 0 to 5GHz. Gain difference and phase difference are shown in Fig. 3.28. As the gate voltage of the PMOS M1 rise 0.1V, gain difference and phase difference shift 1dB and 2°, respectively. The performance of this active balun is summarized in Table 3.2.

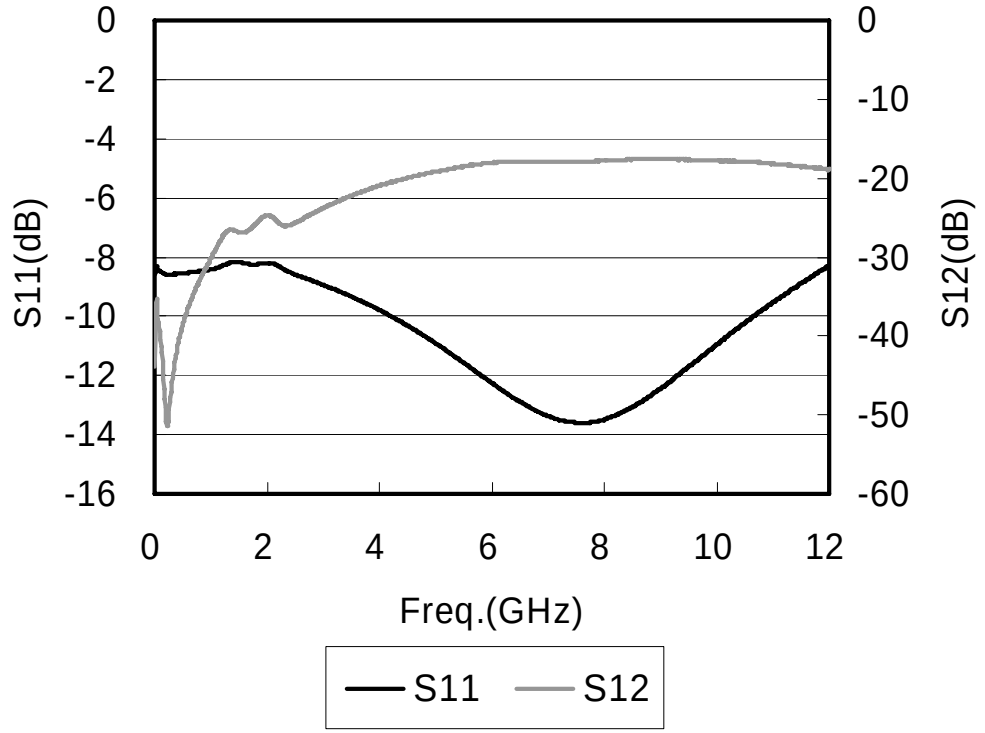


Fig. 3.27. Measured S11 and Measured S12.

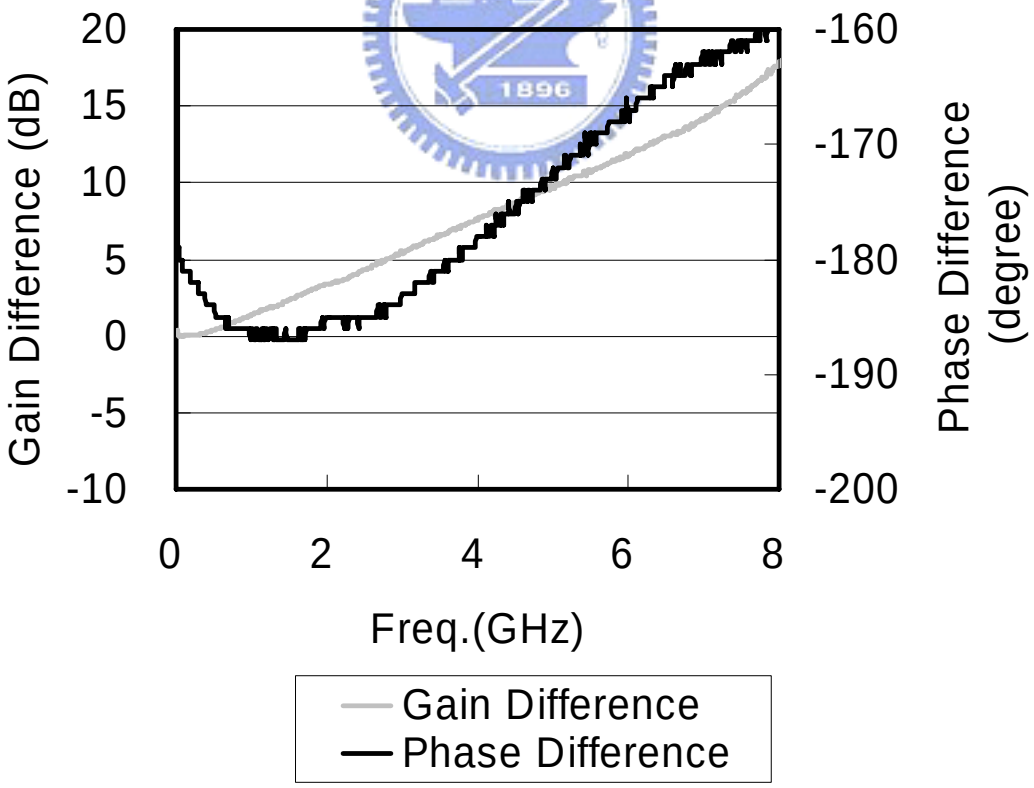


Fig. 3.28. Measured Gain Difference and Measured Phase Difference

TABLE 3.2 Summary of measured performance and comparison to the simulated performance

	Simulation	***Measurement***
Vdd	1.2V	1.2V
Freq.	0 ~10 GHz	0 ~ 5 GHz
Max. Gain error	±2 dB	±8 dB
Max. Phase error	3°	5°
Gain Difference tunable region	±1 dB / ±0.1V	±1 dB / ±0.1V
Phase Difference tunable region	±1.5° / ±0.1V	±1.75° / ±0.1V
Output Loading variation region	25 ~ 200 Ω	
Power consumption	1.44 mW	0.9 mW

Chapter 4

Low Power Ultra-Wideband CMOS Mixer with Active Balun

4.1 Introduction

In this chapter a mixer with an active balun is proposed for low-power and low-voltage operation. The mixer circuit is constructed in a folded configuration, while the balun in a cascoded configuration combining an NMOS and a PMOS. Thus, the total power consumption in the proposed circuit is as low as 1.5mW.

In the following sections 4.2, we first introduce the circuit design of the mixer. We also provide design analysis. In section 4.3, we will explain the circuit of the proposed mixer combined with the proposed active balun which mentioned in chapter 3.

4.2 Low Voltage 0.2-mW CMOS Mixer

Mixers are commonly used for frequency translation in Radio frequency (RF) communication systems. The frequency translation results from multiplication of the RF input signal with a “local oscillator” (LO) signal. In practice, mixers are preferably implemented using “hard switching” via a large LO signal, which mathematically corresponds to multiplication with a square wave, instead of a sine

wave. This renders 2 dB higher conversion gain ($2/\pi$ instead of 1/2) and lower noise figure. And a sufficiency of V_{DS} (> 0.5V) achieves an IIP3 well above 0dBm.

A key problem for the realization of analog circuits in current and future digital CMOS technology is the continuously reducing supply voltage for each technology generation, resulting in nonconducting or poorly conducting switches conveying voltages in the “middle voltage range” between the supply voltages. This is a severe problem in analog and mixed analog—digital circuits exploiting switches, like A/D and D/A converters and switched capacitor circuits, but also in mixers.

Fig. 4.1 shows the schematic of the proposed CMOS mixer circuit. It consists of a modulating stage with differential-pair transistors, *M5~M8*, for frequency mixing, and a CMOS amplifier stage, *M1~M4*, for LO signal buffer. To accommodate low supply voltage, these two stages are constructed in a folded topology, rather than in a cascode configuration of the Gilbert cell. To account for the operation condition in each stage, DC biasing is blocked to each other by capacitors *C3* and *C4* to allow appropriate biasing in each stage.

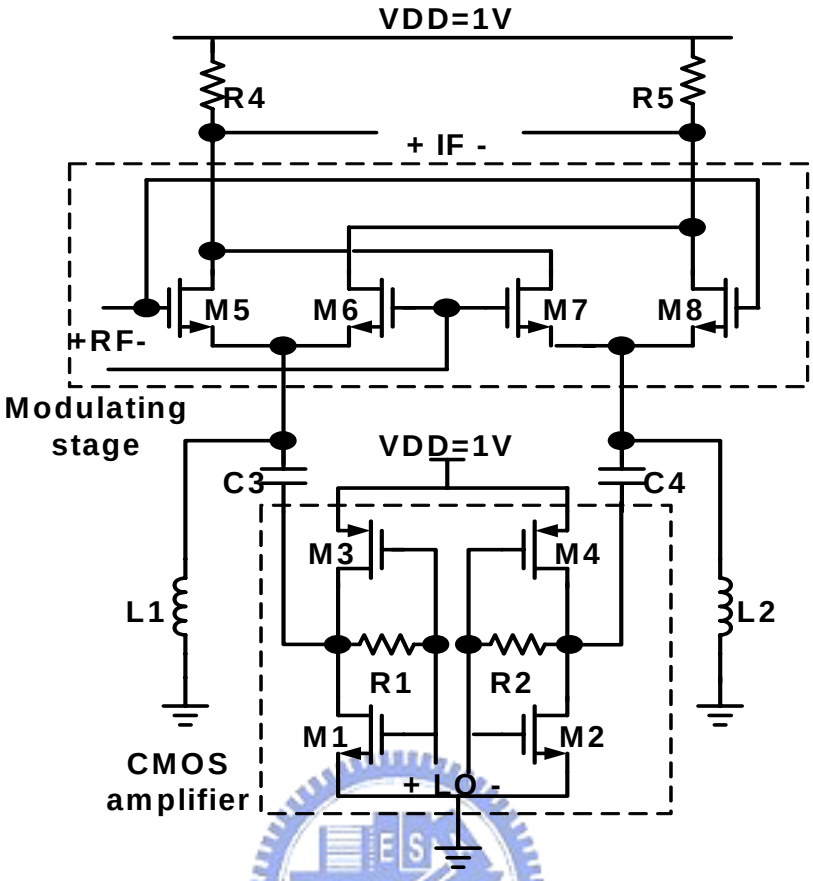


Fig. 4.1 Schematic of the proposed mixer circuit.

Frequency mixing occurs at the modulating stage by utilizing the nonlinear I-V characteristic of MOS transistors, instead of switching current of the transconductance stage as in [3]. Differential RF signal is driven into the transistor gate ports while the LO signal is driven into the source ports. Actually transistors are biased in the subthreshold region, not only providing the necessary nonlinearity but also saving power consumption. It is found that this mixer functions at a supply voltage even lower than 1-V. Note that the voltage swing of LO at the source of M5~M8 must be a little smaller signal. Because if Lo at the source of M5~M8 is large signal, the propose mixer

does not operates in the subthreshold region. Actually the propose mixer operates in the saturation region at the most of time. Fig. 4.2 shows the real current (DC+AC) when the voltage swing of LO signal at the source of M5~M8 is about 0 dBm. We can observe that although the DC power consumption is very low (0.05 mW) but the actual power consumption is much higher than the DC power consumption (about 20 times lager than DC power consumption). This proposed mixer reserves the elasticity of the further mixer design for low voltage and low power. Those inductors *L1* and *L2* provide DC biasing paths to the modulating stage. Combined with *C3* and *C4*, these components give high pass filtering to the LO signal and make the large LO signal to become the small LO signal. When the mixer is combined with the active balun, these components can also be further tuned to obtain flat conversion gain over the broad frequency range of interest.

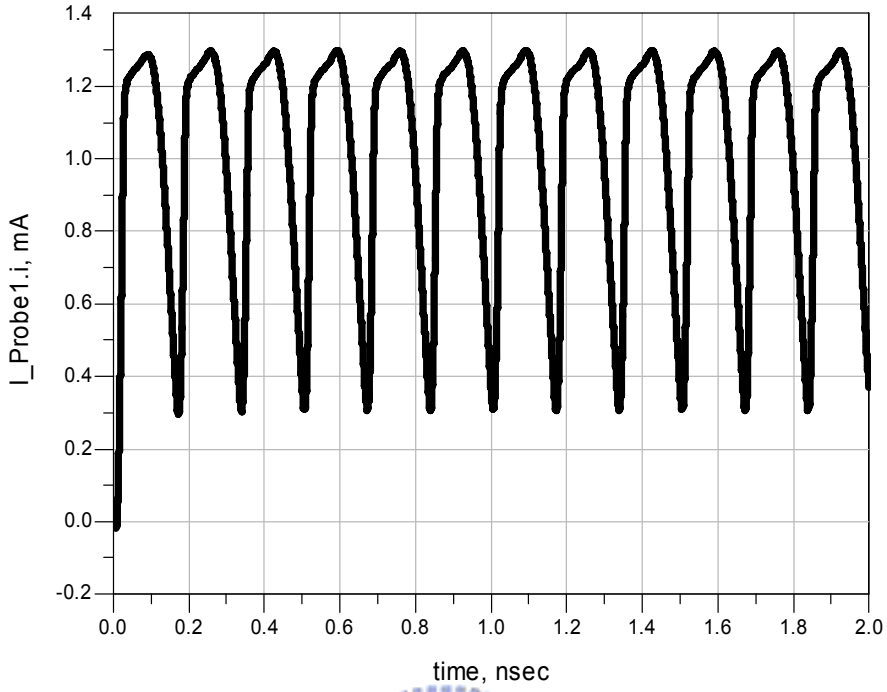


Fig. 4.2 The real current (DC+AC) when the voltage swing of LO at the source of M5~M8 is about 0 dBm.

The LO buffer is essentially a CMOS inverter amplifier. The typical voltage transfer characteristic is as shows in Fig. 4.2.1 Large voltage swing of LO signal makes the operation in regions I and V over the most time period. As is well known, a CMOS amplifier consumes no DC power in those regions. Consequently the time averaged power consumption in the mixer is reduced substantially. The mixer's power consumption is only 0.2 mW.

The down-converted IF signal is taken from the double-balanced outputs of the modulating stage. The conversion gain of the mixer is proportional to load resistance of *R4* and *R5*, and the amplitude of LO. Since the modulating stage is biased in the

subthreshold region, or small biasing current, the DC voltage drop across the load resistor is very small. It is possible to apply a large resistance value to obtain high conversion gain. Further the amplitude of LO signal is swept to determine the optimized level for the suitable conversion gain.

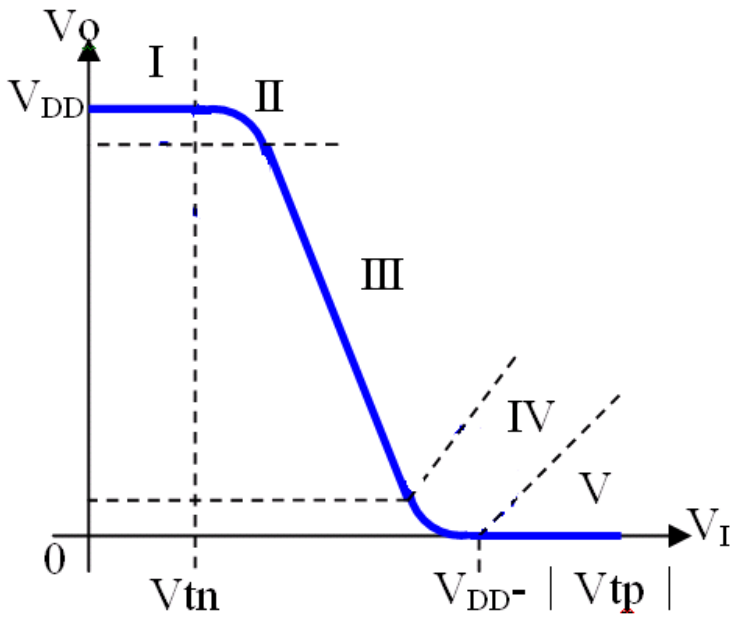


Fig. 4.2.1 The voltage transfer characteristic of a CMOS amplifier.

The double-balanced output benefits noise performance as far as the noise from the CMOS amplifiers and the LO port is concerned. Such configuration generates noise output current in the common-mode form, which is rejected in the differential output. The main noise contribution comes from the modulating stage. Operated in the subthreshold region, those transistors contribute somewhat higher noise.

4.3 Low Voltage 1.5-mW 6~10.6-GHz Ultra-Wideband CMOS Mixer With Active Balun

Fig. 4.3 shows the complete schematic of the proposed mixer with the active balun circuit. Two circuits are DC-blocked by capacitors C5 and C6 such that the gate port of the modulating stage in the mixer is biased properly. To increase the IIP3 of the active balun and decrease the voltage drop across the load resistors in the balun, resistors R2 and R3 are replaced by L4 and L5, which are implemented by on-chip low-Q resisters R7 and R8 for broad frequency response.

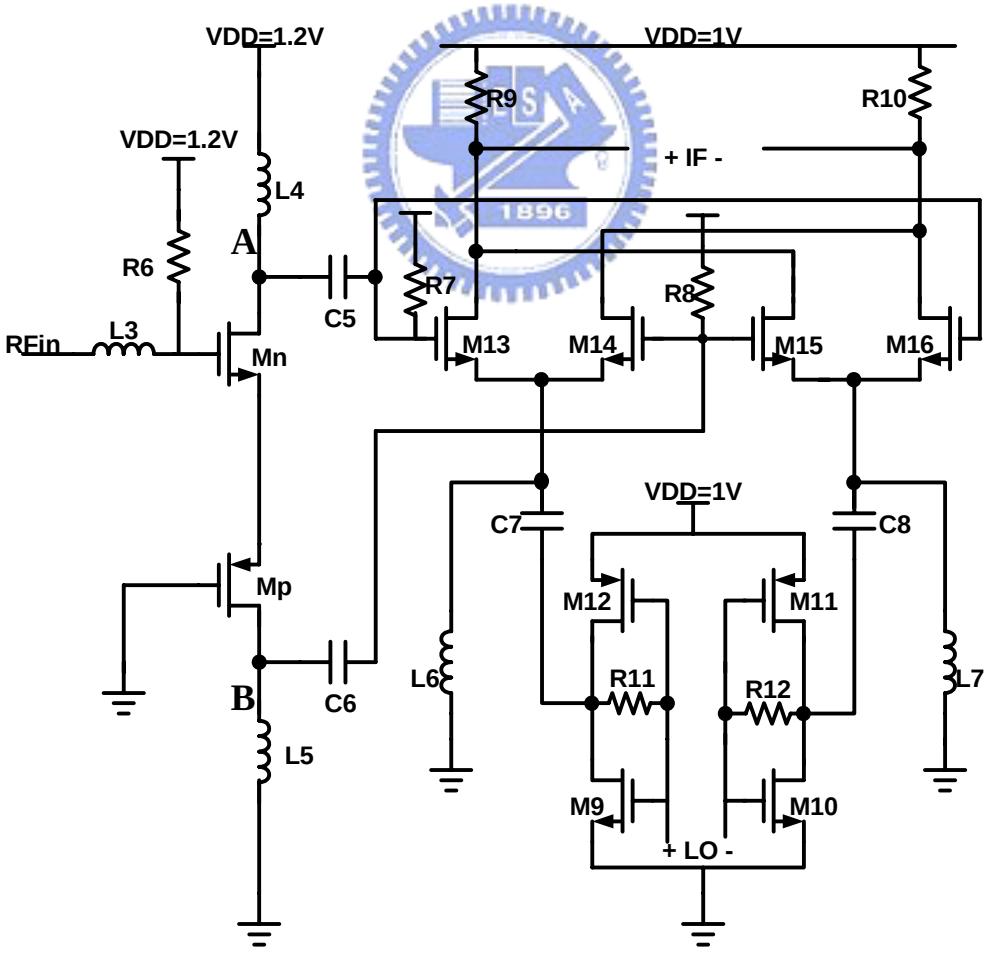


Fig. 4.3 Schematic of the proposed mixer with the proposed active balun circuit.

Gain flatness is realized by superimposing gain of the active balun and the mixer. Although the frequency response of two circuits appears as narrow-band tuned, the composite response achieves broadband gain flatness with appropriate design. As illustrated in Fig. 4.4, the frequency response of the active balun is tuned with peaking around 6-GHz, while that of the mixer around 10-GHz. As a result, the frequency response of the mixer combined with the active balun yields to broadband gain flatness. The load impedance at each balun output port is the same as the source. As such, the balun presents an impedance transformation ratio of 1:2. Specified for ultra-wideband application, the design is optimized at the frequency of 8-GHz for minimum phase error and gain imbalance based on Eq. (4-1).

$$R_3 = \frac{2C_{gdn}}{g_m(C_{gdp} - C_{gdn})}, \text{ and } \frac{1}{R_2} = \frac{1}{R_3} + \frac{2\omega^2 C_{gdn} C_{gdp}}{g_m} \quad (4\text{-}1)$$

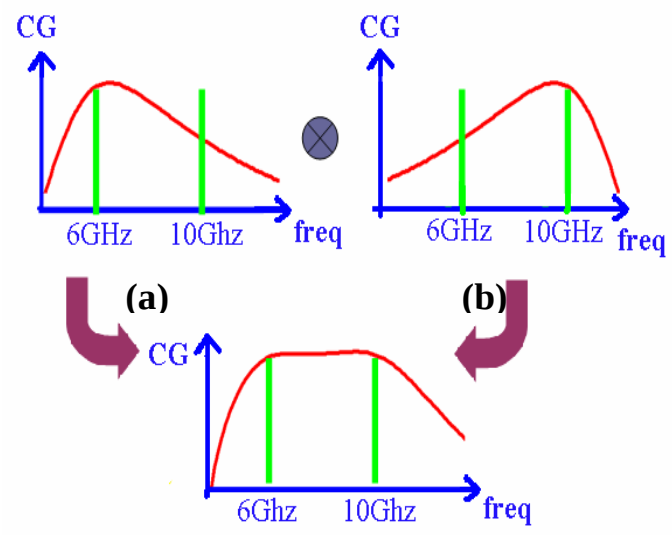


Fig. 4.4 Illustration of broadband gain flatness, (a) conversion gain for the active balun, (b)conversion gain for the mixer, and (c) conversion gain for the mixer combined with the balun.

4.3.1 Microphotograph of Chip

The layout of the mixer with the active balun is shown in Fig. 4.5 The total chip area is 0.698mm by 1.04mm. All long interconnects should be minimized and built on the most top metal to minimize the substrate loss.

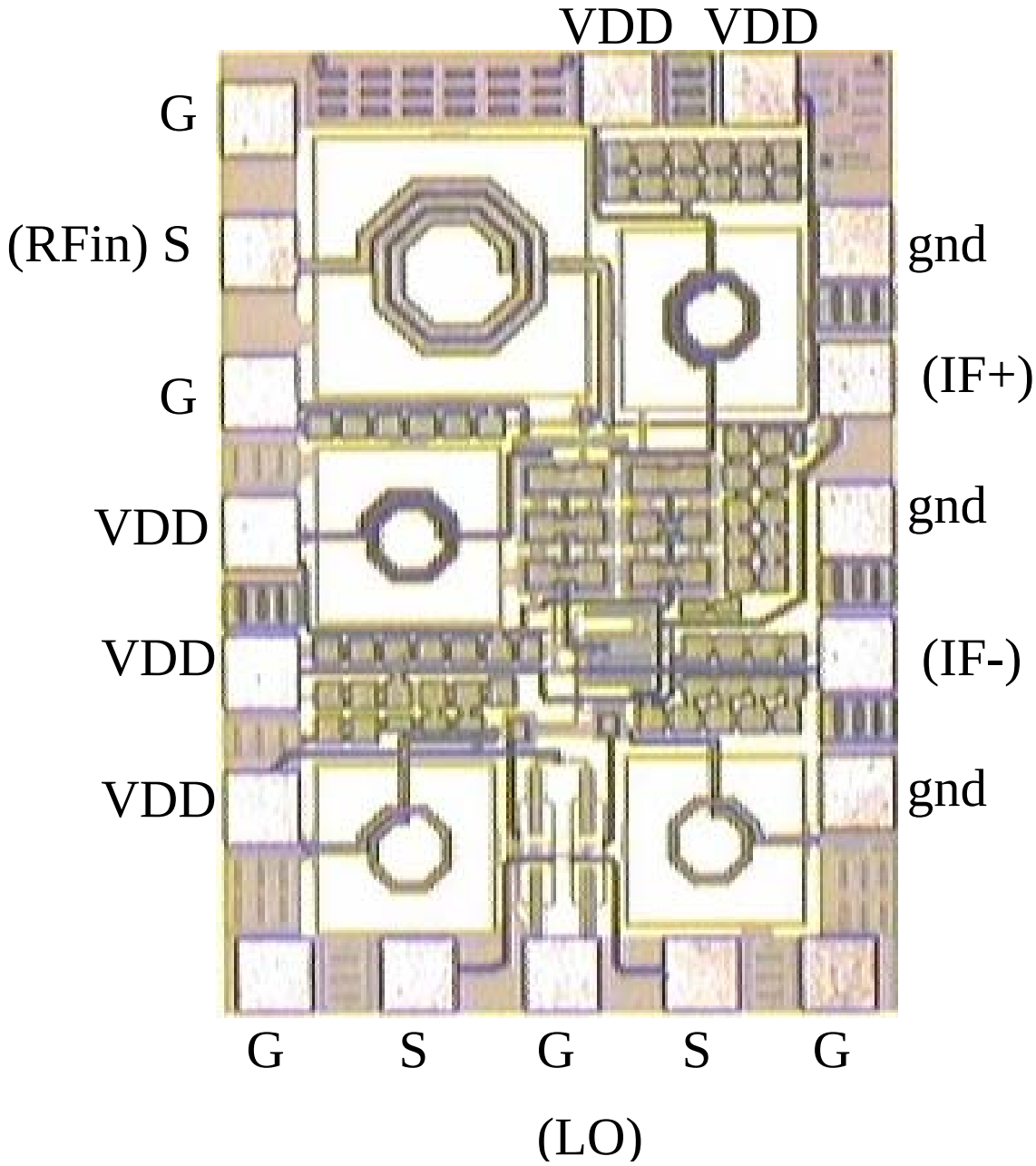


Fig. 4.5 Micrograph of the fabricated mixer with the active balun.

4.3.2 Simulation and Measurement results and Discussion

Fig. 4.6 shows gain difference and phase difference at the balun outputs of node A and B in Fig 4.3. The active balun provides differential signal of the gain and phase imbalance within 0.5 dB and 1.5°, respectively, over the frequency range from 6 to 10.6-GHz. Fig 4.7 shows the measurement diagram. A unit gain output buffer is used to transform the differential signal into the signal-ended form, and provides high input impedance to reduce loading effect. Fig. 4.8 shows the measured S11. Real inductor and capacitor is larger than the TSMC model. That is why the difference between the simulated S11 and measured S11. Fig. 4.9 shows the measured conversion gain. We can observe the measured conversion gain fits the simulated conversion gain under the slow/slow corner test. The circuit achieves conversion gain of 10 dB. Gain flatness is within 1.5 dB variation. The measured IIP3 is between 2.5 to 3 dBm shown in Fig 4.10. The measured NF is between 19 to 24 dB shown in Fig 4.11. The circuit consumes DC power level of 1.5 mW, significantly much less that of previous work. The performance summaries of the mixer and the mixer with the active balun are listed in Table 4.1 and 4.2.

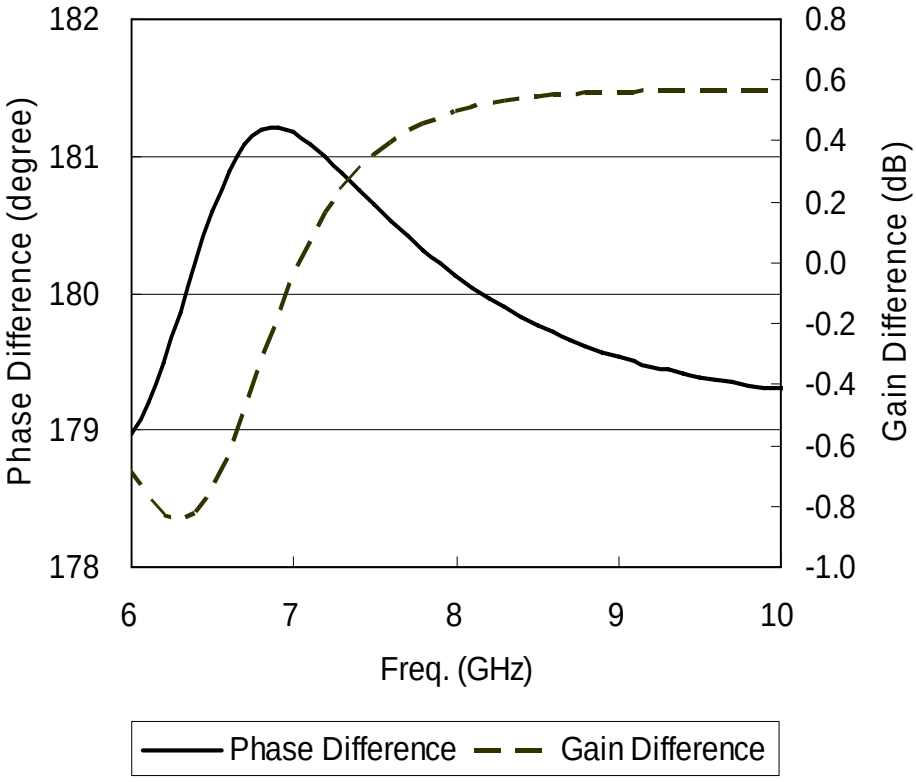


Fig 4.6 Gain Difference & Phase Difference at Node A and B in Fig 4.3.

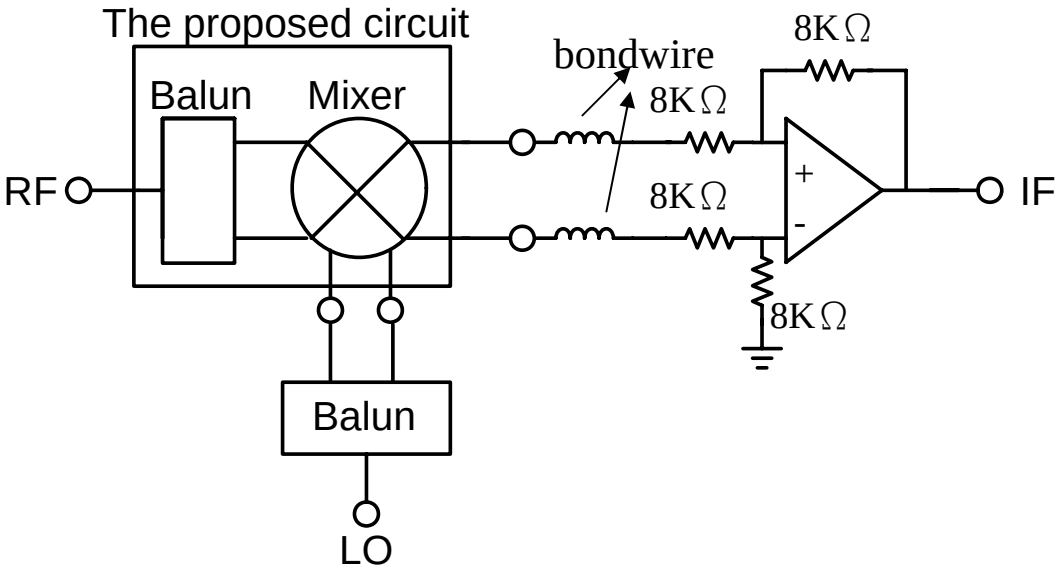


Fig 4.7 Measurement diagram including unit gain output buffer

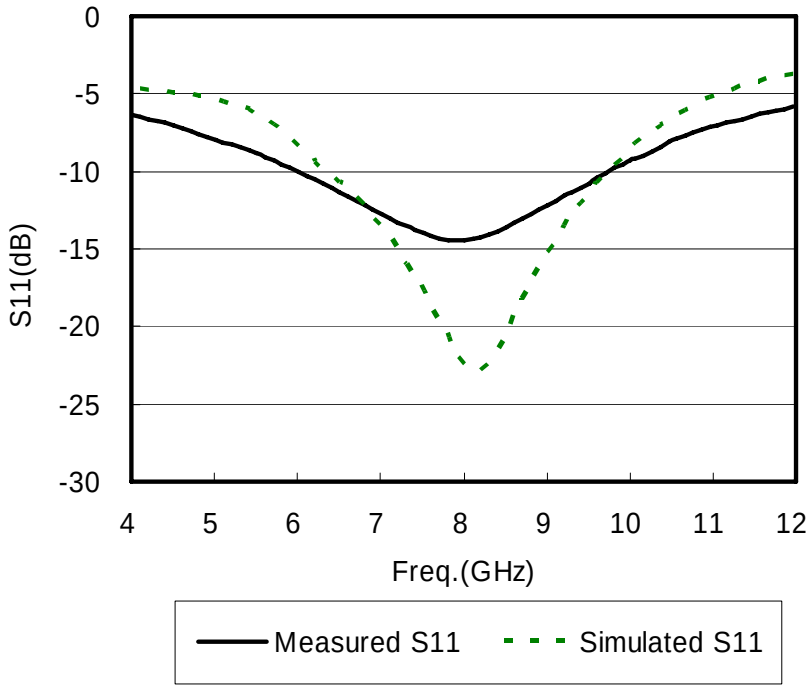


Fig. 4.8 Measured S11

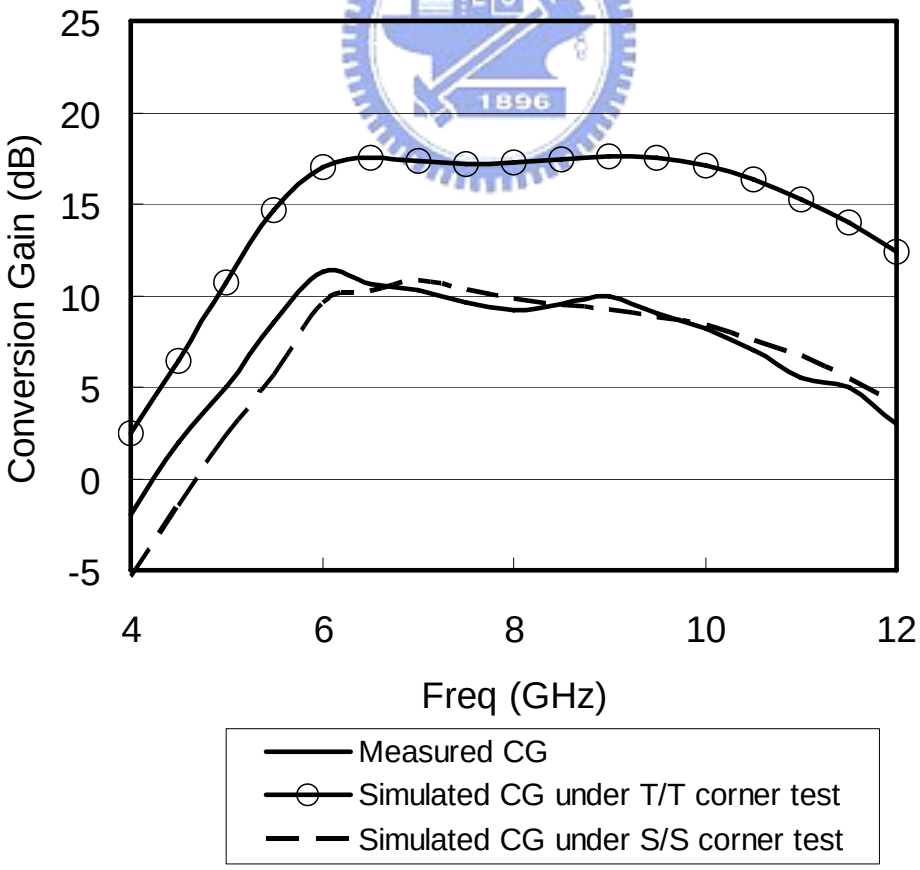


Fig. 4.9 Measured Conversion Gain.

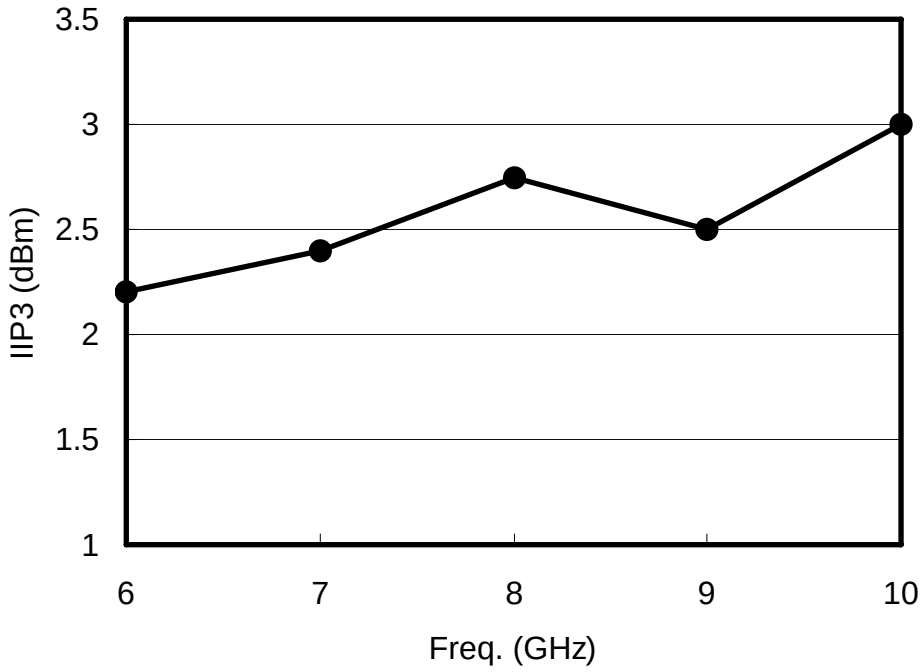


Fig. 4.10 Measured IIP3.

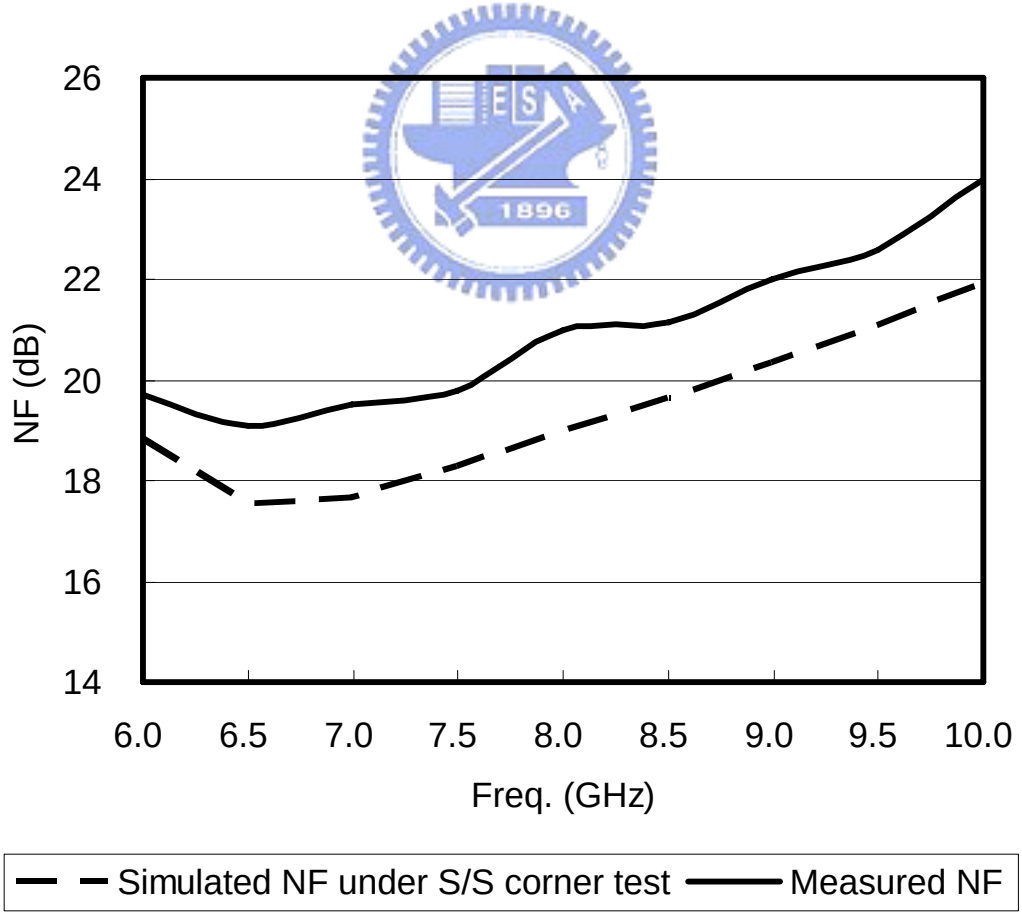


Fig. 4.11 Measured NF

TABLE 4.1 PERFORMANCE SUMMARUY FOR THE MIXER

	This work	[3]	[4]
Frequency	6~10.6GHz	0.5~6GHz	2.5 GHz
Conversion Gain	14~17dB	6~10 dB	9dB
NF	15~18dB	23~27dB	12dB
IIP3	-1~1dBm	2~5dBm	-1dBm
Power	**0.2mW**	1mW	2.8mW

TABLE 4.2 PERFORMANCE SUMMARUY FOR THE MIXER WITH THE ACTIVE BALUN

	Simulation (T/T)	Simulation (S/S)	Measurement
Frequency	6~10.6 GHz	6~10.6 GHz	6~10.6 GHz
Conversion Gain	17 dB ± 0.5 dB	9.5 dB ± 0.5 dB	10 dB ± 1.5 dB
NF	13 ~ 16 dB	17 ~ 22 dB	19 ~ 24 dB
IIP3	0 ~ -1 dBm	2 ~ 3 dBm	2.5 ~ 3 dBm
S11	< -10 dB	< -10 dB	< -10 dB
Supply Voltage	1.2 V	1.2 V	1.2 V
Power	**1.75mW**	**1.2mW**	**1.5mW**

Chapter 5
Low-Power Front-End Circuit

5.1 Introduction

In recent years research on low-power systems is still an emergent topic in order to prolong battery lifetime. Operating at high frequencies, RF integrated circuits are critical circuit blocks to consume a high power level. The front-end circuits, including the low noise amplifier and the mixer, must be on at all times even at the standby mode. Saving power in these circuits shall significantly increase the allowed standby time.

This chapter is aimed at the low-power RF front-end circuit in wireless receivers. For the concern of low power consumption, Direct Conversion Receiver is chosen as the system architecture. It offers great possibility of better from factor, low cost, less power consumption, and the single-chip solution. In this work, a low-voltage, low-power direct down-conversion front-end circuit is implemented. The front-end circuit includes a low noise amplifier and a direct down-conversion mixer, as shown in Fig. 5.1.

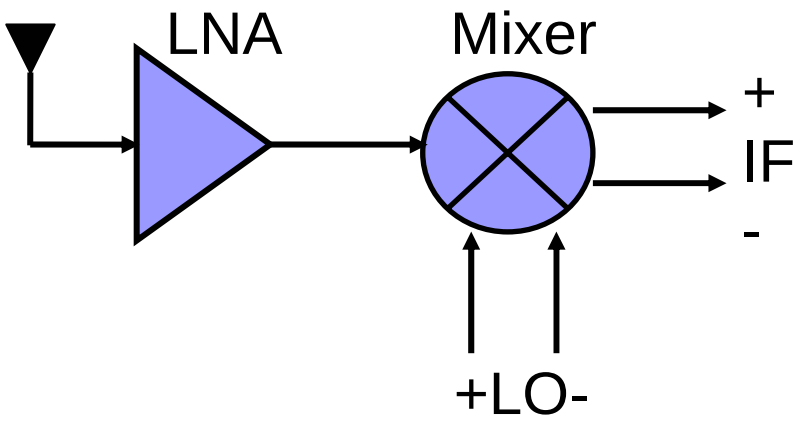


Fig. 5.1 The block diagram of the front-end circuit

5.2 Low Voltage 0.86mW 5 ~ 6 GHz Front-End

In this section, the design principle of the low-power front-end circuit is introduced. Fig. 5.2 shows the schematic of the low-power front-end circuit. R is a large resister for DC bias. The principle emphasizes on the features of each block, which include low noise amplifier and direct down-conversion mixer.

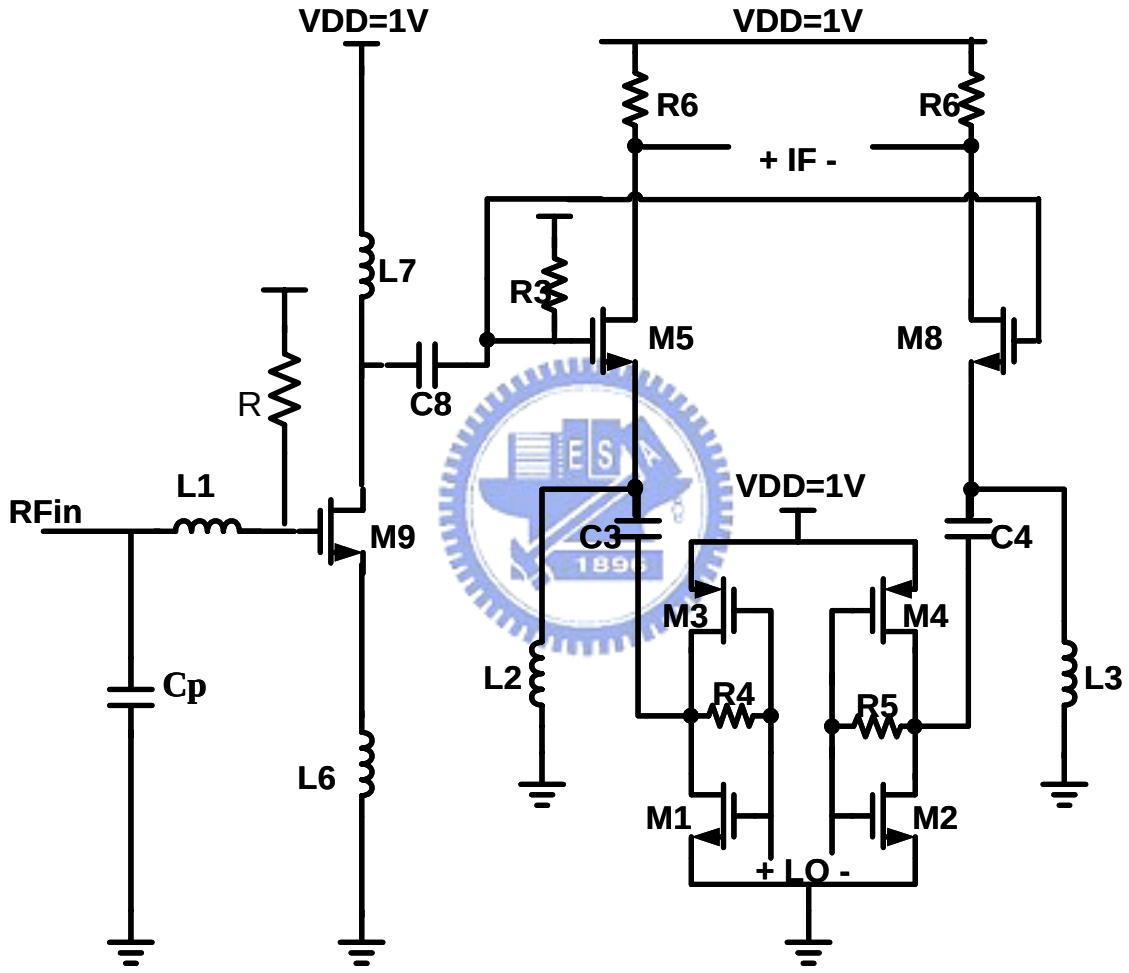


Fig. 5.2 The schematic of the front-end circuit

5.2.1 Low Noise Amplifier

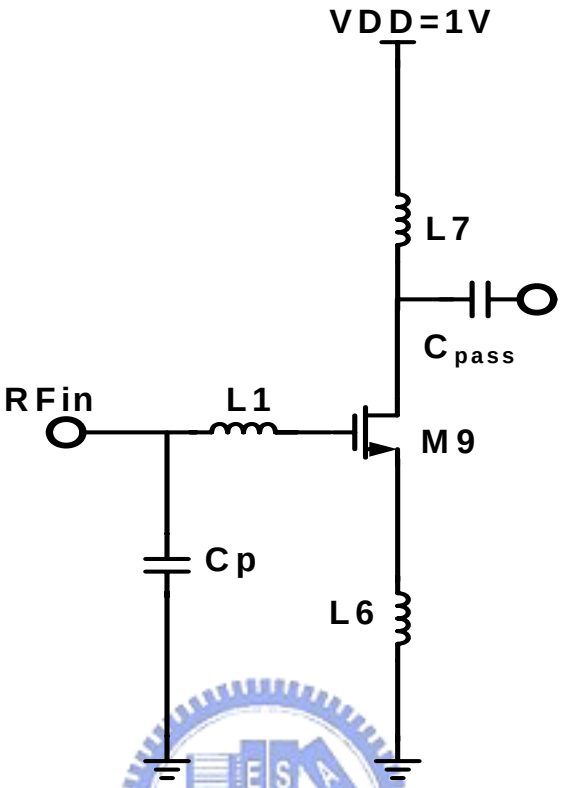


Figure 5.3 The schematic of low noise amplifier

The low noise amplifier is the first stage of the front-end circuit. This stage must provide high gain and low noise to suppress the overall system's noise performance. The inductive source degeneration topology, therefore, is used to achieve noise and power matching simultaneously. Fig. 5.3 shows the schematic of the low noise amplifier, where Cp is the parasitic capacitance of the pad. In order to simplify analysis, we ignore the effect of the C_{gd} and the C_p. The input Impedance, therefore, can be simply expressed as

$$Z_{in} = s(L_1 + L_6) + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s \qquad (5\text{-}1)$$

The imaginary part of the impedance can be set to zero by choosing L_1 appropriately at the resonant frequency, and real part can be made equal to 50Ω by choosing

appropriate value of the L_6 for input matching.

At the condition of the input matching, the equivalent transconductance of this architecture can be expressed as

$$G_m = \frac{\omega_T}{2\omega_0 R_s} \tag{5-2}$$

where ω_T is equal to g_m/C_{gs} approximately.

Besides, the noise performance is the most critical parameter in the design of LNA. From noise analysis of LNA in section 2.1, we can get the optimal noise performance. For fixed power dissipation, we can adjust device size and bias point to minimize the noise figure. When the optimum device size is selected, the equivalent transconductance, G_m, is decided by $V_{gs.opt}$.

5.2.2 Low Voltage 0.1mW CMOS Mixer

As mentioned, mixers are commonly used for frequency translation in Radio frequency (RF) communication systems. The frequency translation results from multiplication of the RF input signal with a “local oscillator” (LO) signal.

For low power, we adopt the single input mixer which is the half of the mixer in section 4.2 for connecting after the single end LNA directly without an active balun. Fig. 5.4 shows the schematic of the proposed CMOS mixer circuit. Like the mixer in section 4.2, it consists of a modulating stage with differential-pair transistors, *M5 and M6*, for frequency mixing, and a CMOS amplifier stage, *M1~M4*, for LO signal buffer, too. To accommodate low supply voltage, these two stages are constructed in a folded

topology, rather than in a cascode configuration of the Gilbert cell. To account for the operation condition in each stage, DC biasing is blocked to each other by capacitors *C3* and *C4* to allow appropriate biasing in each stage. The operating functions all follow the discussion in the section 4.2.

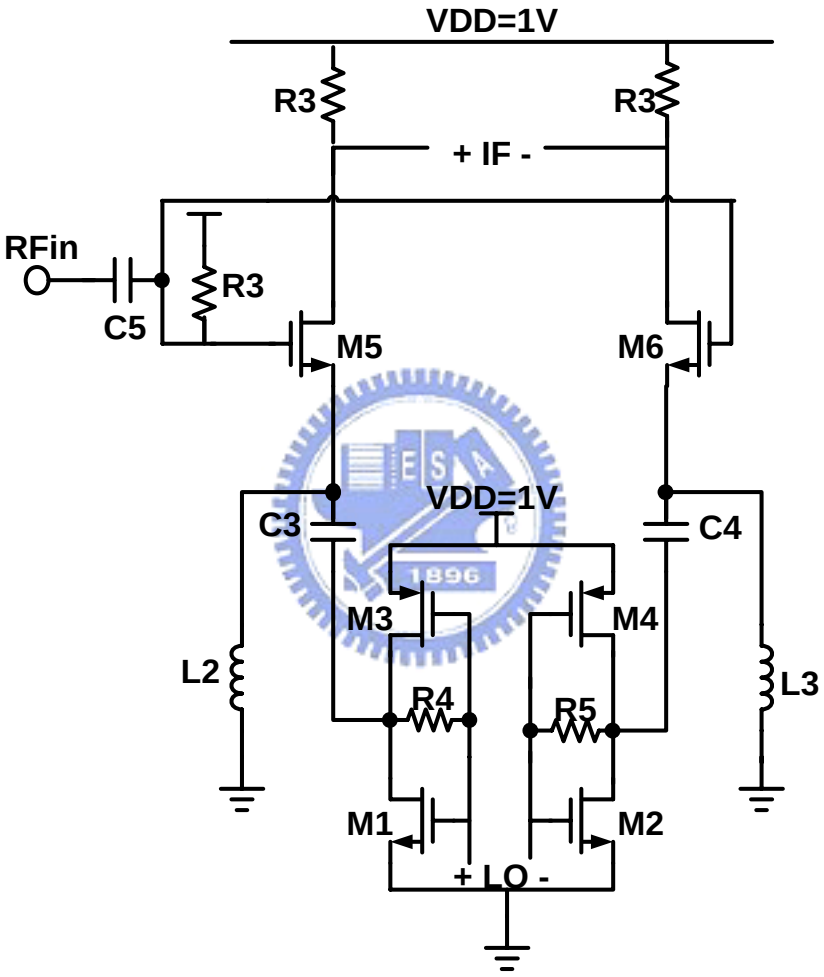


Figure 5.4 The schematic of the proposed mixer

5.2.3 *Microphotograph of Chip*

The layout of the front end is shown in Fig. 5.5 The total chip area is 1.157mm by 0.675mm. All long interconnects should be minimized and built on the most top metal to minimize the substrate loss.

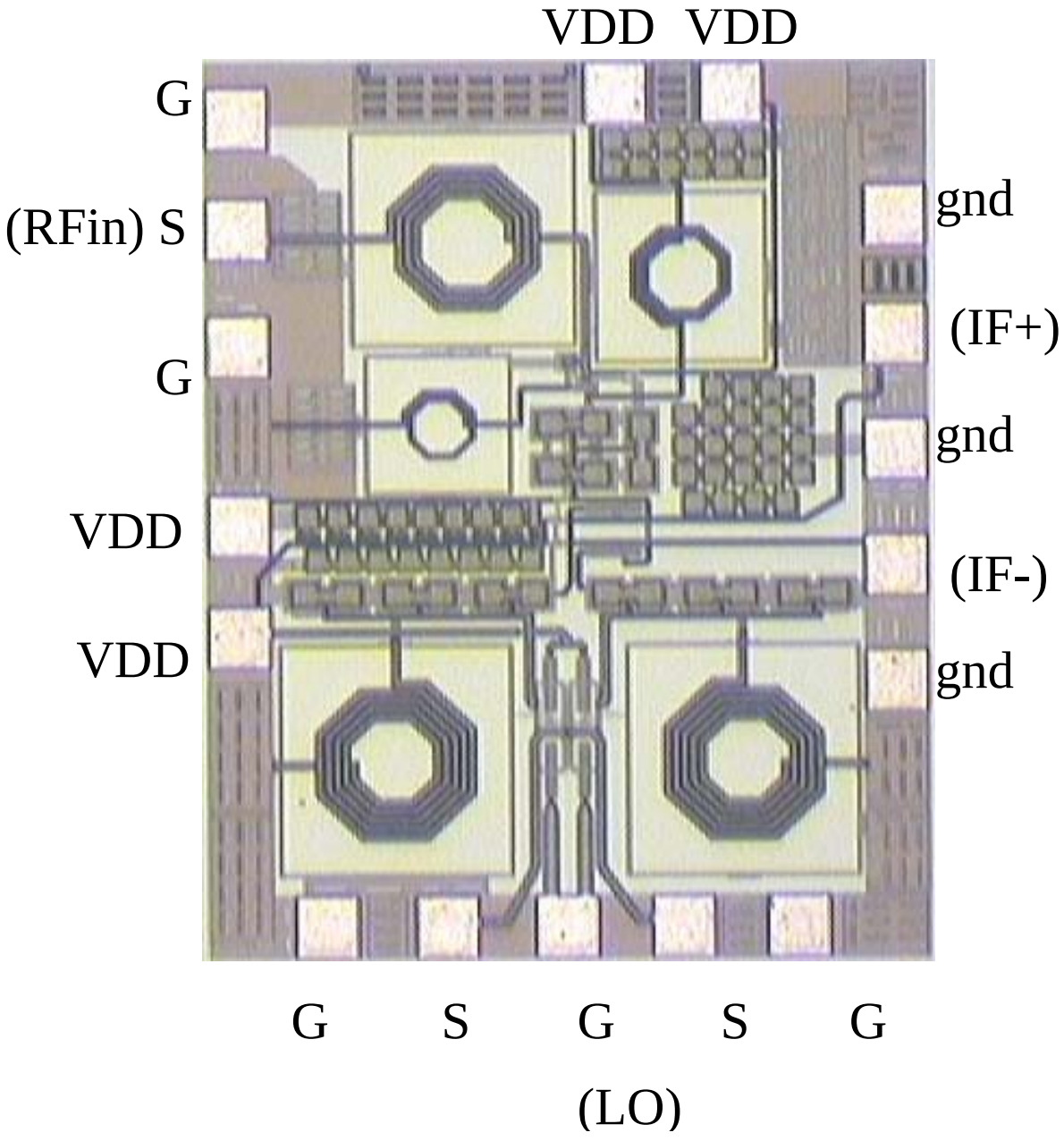


Fig. 5.5 Micrograph of the fabricated front end.

5.2.4 Simulation and Measurement results and Discussion

Fig 5.5 shows the measurement diagram. A unit gain output buffer is used to transform the differential signal into the signal-ended form, and provides high input impedance to reduce loading effect. Fig. 5.6 shows the measured S11. Real inductor and capacitor is larger than the TSMC model. That is why the difference between the simulated S11 and measured S11. Fig. 5.7 shows the measured conversion gain. We can observe the measured conversion gain fits the simulated conversion gain under the slow/slow corner test. The circuit achieves the max conversion gain of 26 dB. And the 3 dB bandwidth is about 1 GHz. The measured IIP3 is between -7 to -5.5 dBm shown in Fig 5.8. The measured NF is between 12 to 13 dB shown in Fig 5.8. The circuit consumes DC power level of 0.86 mW, significantly much less that of previous work. The performance summary of the front end is listed in Table 5.1.

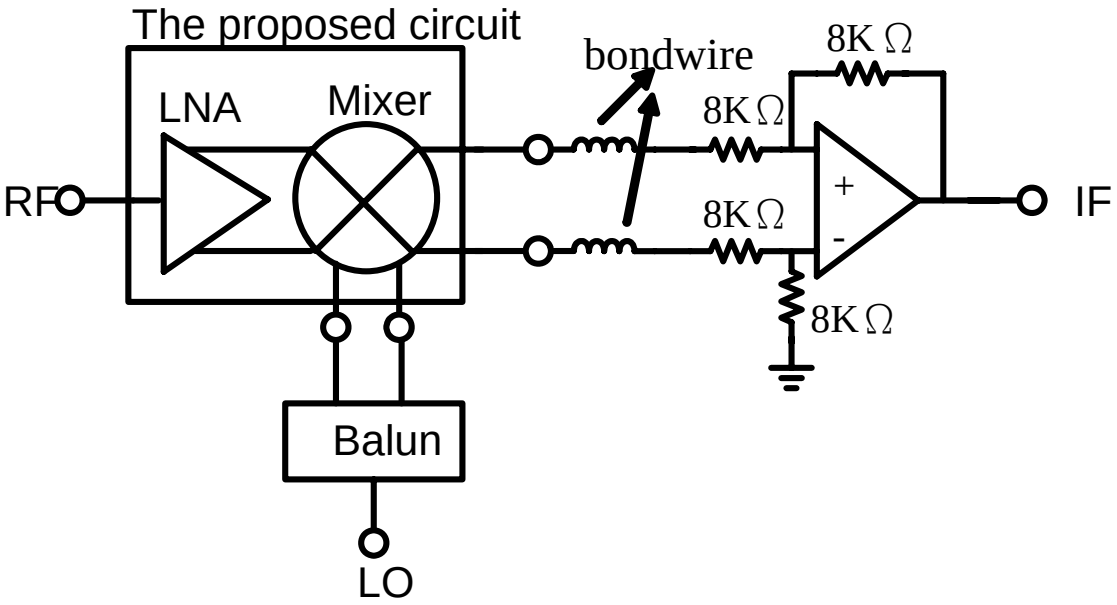


Fig. 5.5 Measurement diagram including unit gain output buffer

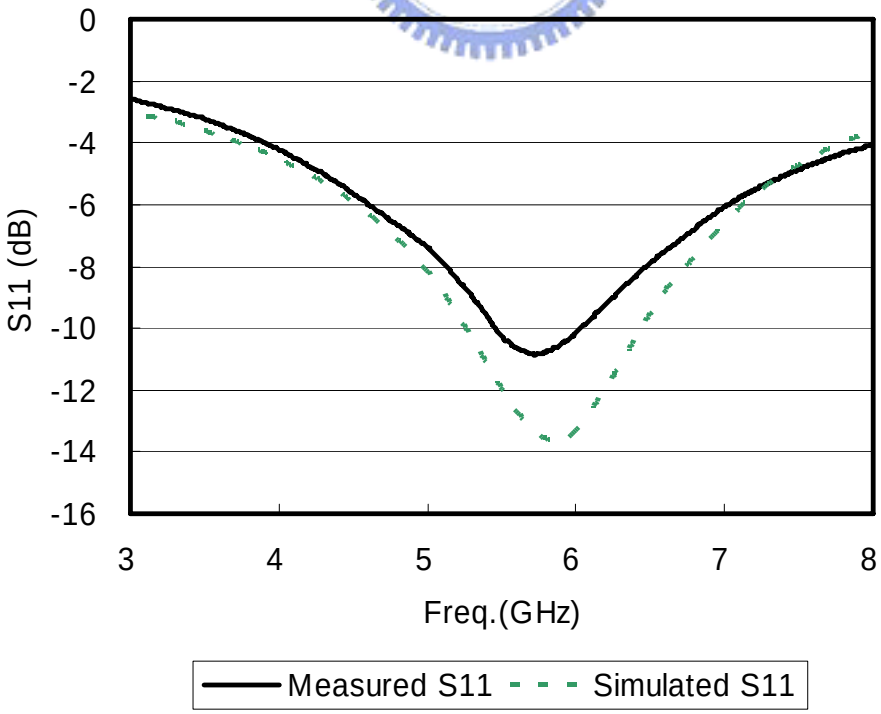


Fig. 5.6 Measured S11

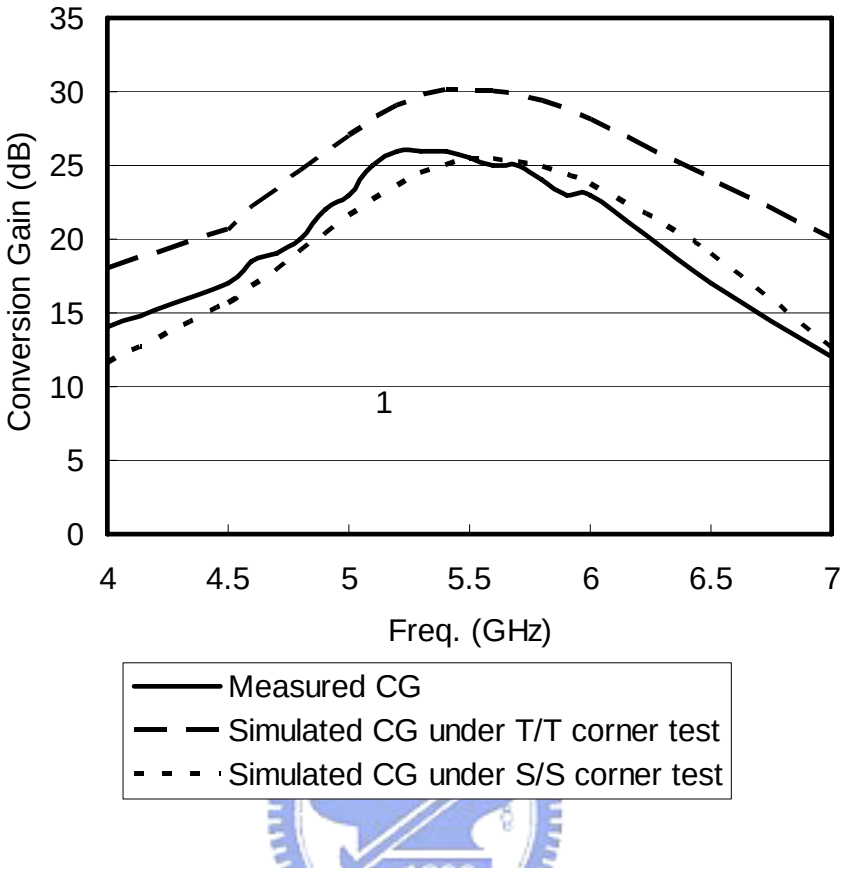


Fig. 5.7 Measured Conversion Gain

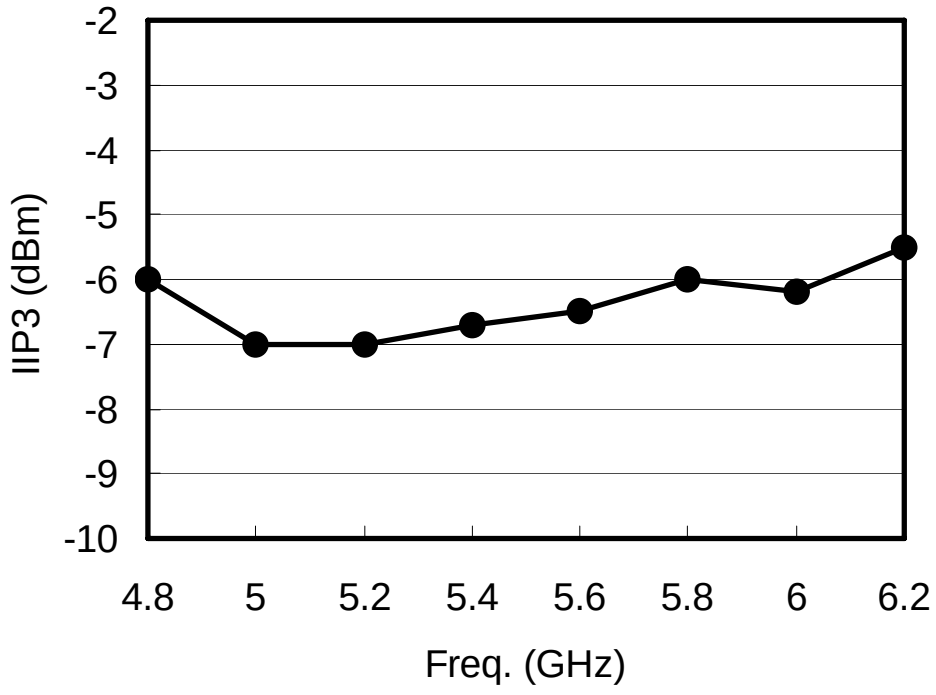


Fig. 5.8 Measured IIP3

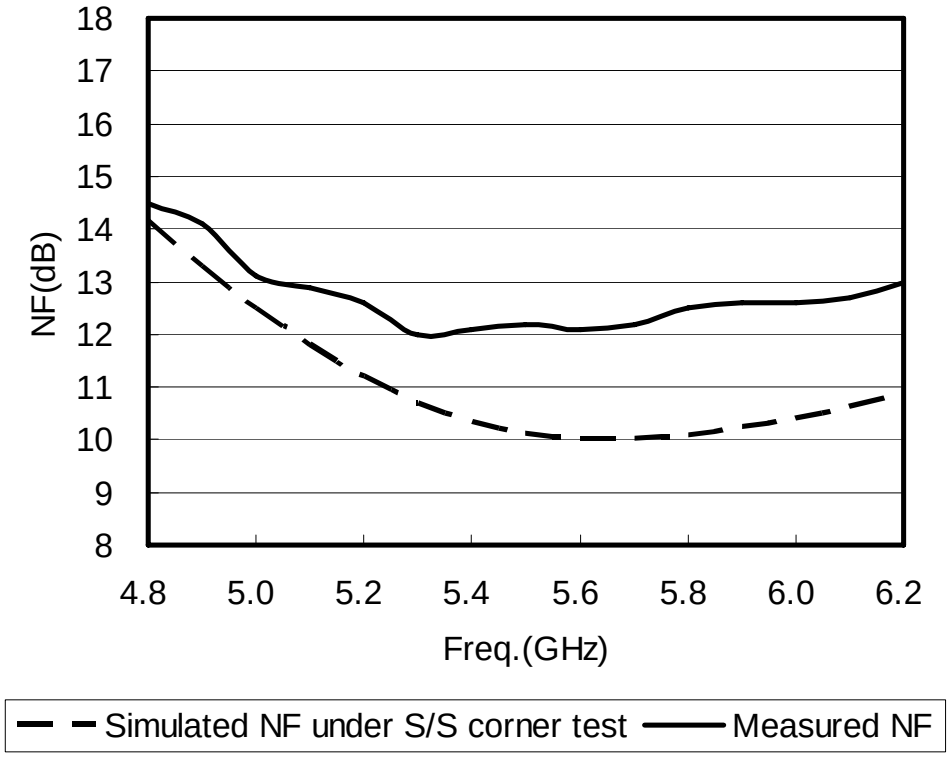


Fig. 5.9 Measured NF

TABLE 5.2 PERFORMANCE SUMMARUY FOR THE FRONT END

	Simulation(T/T)	Simulation(S/S)	Measurement
Frequency	5 ~ 6 GHz	5 ~ 6 GHz	5 ~ 6 GHz
Conversion Gain	27 ~ 30 dB	22 ~ 25 dB	23 ~ 26 dB
NF	8~9 dB	10~12 dB	12~14.5 dB
IIP3	-8.5 ~ -9.5 dBm	-5 ~ -7 dBm	-5.5 ~ -7 dBm
S11	< -10 dB	< -10 dB	< -8 dB
Supply Voltage	1 V	1 V	1 V
Power	**1 mW**	**1 mW**	**0.86 mW**

Chapter 6
Conclusion

In chapter 3, using a pair of common-source NMOS and common-gate PMOS transistors, the proposed active balun is advantageous in low power and broadband performance. With using any current source as the conventional differential-amplifier configuration, the circuit needs no compensation feedback network. The fabricated circuit in a standard 0.18um CMOS process achieves imbalance less than 2dB and 3° up to 8-GHz, applicable to use in ultra-wideband systems. It could save up to 88% of power consumption as compared to previous work. The active balun is intended for complete integration for future wireless applications.

In chapter 4, a low-voltage and low-power CMOS mixer with an active balun is designed for frequency down-conversion in ultra-wideband applications. The mixer contains CMOS amplifiers as the LO buffer and the modulating stage in a folded configuration to allow low-voltage operation. The RF input signal comes from a new low-power active balun that uses a pair of common-source NMOS and common-gate PMOS transistors. This balun gives an impedance transformation ratio of 1:2, and provides a differential signal within 0.5dB and 1.5° of gain and phase imbalance, respectively, from 6 to 10.6-GHz. The mixer and the active balun are designed in 0.18 μm CMOS technology to operate at 1.2-V supply voltage. The circuit performance

of the mixer with the active balun achieves flat conversion gain of 10 dB within 1.5 dB variation, the maximum IIP3 of 3 dBm, and the minimum noise figure of 19 dB. The total circuit only consumes power of 1.5 mW. As compared to typical designs, it saves about 85% and 95% of power consumption in the balun and the mixer circuits, respectively.

In Chapter 5, a low voltage 1 mW 5 ~ 6 GHz front-end is presented. Modify the mixer in chapter 4 from a differential input mixer to a signal input mixer. The modified mixer still follows the same operating function. The LNA and the mixer are designed in 0.18 μ m CMOS technology to operate at 1-V supply voltage. The circuit performance of the front end achieves max conversion gain of 26 dB at 5.3 GHz, the maximum IIP3 of -6 dBm, and the minimum noise figure of 12 dB. The total circuit only consumes power of 0.86 mW.

Chapter 7

Future Work

When a low power UWB 6 ~ 10 GHz LNA is designed. The LNA can be combined with the 1.5 mW 6 ~ 10 GHz CMOS mixer with an active balun to be a wideband front end receiver for UWB system in low power performance.

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