INTEGRATION, the VLSI journal 42 (2009) 83–88

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

A 1-V RF-CMOS LNA design utilizing the technique of capacitive feedback matching network

Fadi Riad Shahroury, Chung-Yu Wu *

Nanoelectronics and Gigascale Systems Laboratory, Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan

ARTICLE INFO

Keywords:
Low-noise amplifier (LNA)
Noise optimization
Low voltage
RF

ABSTRACT

In this paper, a CMOS low-noise amplifier (LNA) with a new input matching topology has been proposed, analyzed and measured. The input matching network is designed through the technique of capacitive feedback matching network. The proposed LNA which is implemented in a 0.18-μm1*P6M CMOS* technology is operated at the frequency of 12.8 GHz. It has a gain S21 of 13.2 dB, a noise figure (*NF*) of 4.57 dB and an NF_{min} of 4.46 dB. The reverse isolation S12 of the LNA can achieve −40 dB and the input and output return losses are better than −11 dB. The input 1-dB compression point is −11 dB m and IIP3 is −0.5 dB m. This LNA drains 10 mA from the supply voltage of 1 V.

1. Introduction

Over the last two decades, the rapid growth of portable wireless communication systems, such as cellular phones, global positioning satellites (GPS), bluetooth, wireless local area network (WLAN), ultra-wideband (UWB), etc., has greatly increased demand for high performance and low cost radio frequency (RF) receivers. This has driven recent effort to implement RF receivers in advanced CMOS technologies in order to increase integration level, reduce power consumption, and reduce chip area. To achieve the above design goals, it is important to design suitable low voltage and low power analog front-end in RF receivers. In the RF receiver front-end design, the low-noise amplifiers (LNAs) play a crucial role since the whole system-sensitivity is mainly determined by the noise figure of the LNA.

In the design of RF-CMOS LNAs, it is known that the key performance parameters are power-gain and noise figure (*NF*) besides the stability, linearity and isolation. The goal of LNA design is to achieve maximum power-gain and minimum *NF* simultaneously at any given amount of power dissipation. To reach this goal, the input impedance Z_{in} of a LNA must be kept close enough to the optimum source noise conjugate impedance $Z^*_{n,opt}$.

Conventionally, the inductive source-degeneration technique is used to achieve this goal [1]. However, this inevitably decreases the equivalent transconductance of the LNA at high frequencies, which reduces the power-gain [2]. To retain the power-gain, the power dissipation has to be increased significantly. For the LNAs operated above 10 GHz, an accurate and small source-degeneration inductor value is required. The variations of the inductance make Z_{in} not close enough to $Z^*_{n,opt}$. To realize the accurate and small source-degeneration inductance, microstrip line can be used at frequencies higher than 20 GHz. But it is chip area consuming if being used at frequencies below 20 GHz.

So far, many high-frequency RF-CMOS LNAs have been proposed [3–7]. Among them, the proposed LNA structure at 17 and 24 GHz [3] uses microstrip line to realize accurate source-degeneration inductor. However, the chip area is still large. The multistage common-source amplifiers are used in the LNAs in [4–6]. Each stage is designed with inductive source degeneration. To reach sufficient gain and good stability at frequencies from 8 GHz to Ku-band, high power dissipation is needed [4–6]. Although power-gain match can be achieved by utilizing the inputmicrostrip line in the LNA design [7], Z_{in} is not equal to $Z^*_{n,opt}$ in this case. Thus the minimum *NF* and maximum power-gain cannot be achieved simultaneously.

The approach described in this work relies on the introduction of a new LNA design technique, which uses the gate-drain capacitance and output capacitance of the input MOSFET to form the capacitive feedback matching network and bring the input impedance Z_{in} close to the optimum source noise conjugate impedance $Z^*_{n,opt}$. The current of the input MOSFET is then amplified by a RF current-mirror amplifier. It is shown that the proposed LNA has a high power-gain of 13.2 dB, a high reverse isolation of −40 dB, and a good linearity with the input 1-dB compression point at −11 dB m and IIP3 is −0.5 dB m. The *NF* and NF_{min} of the proposed LNA are 4.56 dB and 4.46 dB, respectively. Therefore, the LNA has good noise performance because *NF* and NF_{min} are very close to each other. Besides, the proposed LNA has a small power consumption of 10 mW under the low power supply voltage of 1 V.

The proposed input matching method is discussed in Section 2 and its effect on the noise figure (*NF*) is presented in Section 3. The

* Corresponding author.
E-mail addresses: fadi_rs@alab.ee.nctu.edu.tw (F.R. Shahroury), peterwu@mail.nctu.edu.tw (C.-Y. Wu).

0167-9260/$ - see front matter © 2008 Published by Elsevier B.V.
doi:10.1016/j.vlsi.2008.09.007

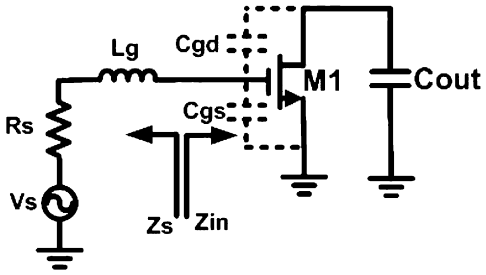


Fig. 1. The common-source amplifier as the input stage.

details of the designed CMOS circuit of the LNA are presented in Section 4. While in Section 5, it describes the experimental results. Finally, the conclusion is given in Section 6.

2. Proposed input matching method

The input impedance of the LNA is designed to match with the antenna, in order to prevent the incoming signal from reflecting back and forth between the LNA and the antenna. Generally, the antenna has 50-Ω load to the LNA. Unfortunately, the input impedance of a MOSFET device is inherently capacitive, so the matching with 50-Ω resistive input impedance is not an easy task. Thus, a capacitive feedback matching technique is proposed to overcome this problem [8].

The common-source amplifier as the input stage is shown in Fig. 1, where Z_s is the impedance seen from the right node of the input matching inductor L_g, Z_{in} is the input impedance of M1, C_{gd} is the gate-drain capacitance, C_{gs} is the gate-source capacitance, C_{out} is the output loading capacitance which is the input capacitance of the next stage, R_s is the signal-source resistance, and V_s is the input signal voltage source. By using Millers theorem on C_{gd}, the input impedance Z_{in} can be derived as

$$Z_{in} = \frac{R_f}{(Q_f^2+1)} + \frac{1}{j\omega_o(C_{gs}+C_{gd})\left(\frac{1}{Q_f^2}+1\right)}, \tag{1}$$

where

$$Q_f = \omega_o(C_{gs}+C_{gd})R_f, \tag{2}$$

$$R_f = \frac{1}{g_m}\frac{C_{out}}{C_{gd}}, \tag{3}$$

g_m is the transconductance of M1, and ω_o is the operating angular frequency. As it can be seen from the above equations, both C_{gd} and C_{out} with g_m together providing a real term R_f which contributes to the real input impedance in Z_{in}. They are called the capacitive feedback matching network.

3. The noise analysis of the proposed input matching method

In the LNA design, input power match is essential but not sufficient. It is also vital for a LNA to satisfy the noise performance requirement, so that the circuit itself does not degrade the output signal-to-noise ratio (SNR) to an unacceptable level. Thus, a careful noise analysis on the capacitive feedback matching technique is developed to establish the principle of operation clearly and find the limits on noise performance. A brief review of the standard CMOS noise sources will facilitate the analysis.

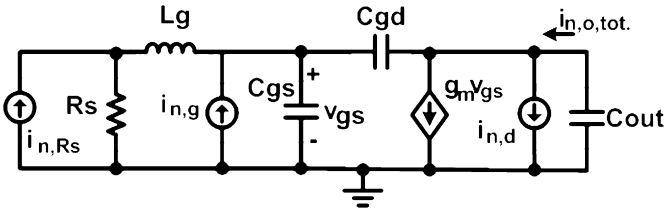


Fig. 2. The small-signal equivalent circuit for noise calculations.

3.1. Noise sources

Fig. 2 shows the small-signal model of the equivalent circuit for the noise analysis. Three noise sources have been considered in Fig. 2. They are the thermal noise of the source resistance i_{n,R_s}, the thermal noise of the channel current $i_{n,d}$, and the gate induced current noise $i_{n,g}$. They can be expressed as [9]

$$\overline{i^2}_{n,R_s} = 4kT\frac{1}{R_s}\Delta f, \tag{4}$$

$$\overline{i^2}_{n,d} = 4kT\gamma g_{d0}\Delta f, \tag{5}$$

$$\overline{i^2}_{n,g} = 4kT\delta\frac{\omega^2 C_{gs}^2}{5g_{d0}}\Delta f, \tag{6}$$

where k is Boltzmann's constant, T is the absolute temperature, R_s is the source resistance, g_{d0} is the zero-bias drain conductance, γ is the thermal noise coefficient, Δf is the noise bandwidth in hertz, and δ is the gate induced current noise factor.

According to [9], there is a correlation between the gate induced current noise $i_{n,g}$ and the thermal noise of the channel current $i_{n,d}$. This correlation can be treated by separating $i_{n,g}$ into two parts. $i_{n,gc}$ is the part that fully correlated with thermal noise of the channel current $i_{n,d}$, whereas $i_{n,gu}$ is the uncorrelated part. Hence, the gate induced current noise can be written as

$$\overline{i^2}_{n,g} = \underbrace{4kT\delta\frac{\omega^2 C_{gs}^2}{5g_{d0}}(1-|c|^2)\Delta f}_{i_{n,gu}} + \underbrace{4kT\delta\frac{\omega^2 C_{gs}^2}{5g_{d0}}|c|^2\Delta f}_{i_{n,gc}}, \tag{7}$$

where the correlation coefficient c is defined as [9]

$$jc = \frac{\overline{i_{n,g}i_{n,d}^*}}{\sqrt{\overline{i_{n,g}^2}\,\overline{i_{n,d}^2}}}. \tag{8}$$

Because of the correlation, special attention must be paid to the reference polarity of the correlated component. The value of c is positive for the polarity shown in Fig. 2.

3.2. Capacitive feedback matching network noise analysis

Noise performance is usually evaluated with noise figure (NF) which indicates the noise suppression ability of the circuit. Noise figure is defined as

$$NF = 10\log(F), \tag{9}$$

where F is the noise factor which is defined as the total output noise power divided by the noise power at the output due to the input source. F can be expressed as

$$F = \frac{\overline{i_{n,o,tot.}^2}}{\overline{i_{n,o,Rs}^2}} = \frac{\overline{i_{n,o,Rs}^2} + \overline{i_{n,o,g+d}^2}}{\overline{i_{n,o,Rs}^2}}, \tag{10}$$

where $\overline{i_{n,o,tot.}^2}$ is the mean-squared of the total output noise current, $\overline{i_{n,o,Rs}^2}$ is the mean-squared output noise current due to

$i_{n,Rs}$, and $\overline{i^2_{n,o,g+d}}$ is the mean-squared output noise current due to $i_{n,d}$ and $i_{n,g}$. Considering correlation, $\overline{i^2_{n,o,g+d}}$ can be re-expressed as

$$\begin{aligned}\overline{i^2_{n,o,g+d}} &= \overline{(i^*_{n,o,d}+i^*_{n,o,g})(i_{n,o,d}+i_{n,o,g})}\\ &= \overline{i^2_{n,o,d}} + 2\mathrm{Re}(\overline{i_{n,o,d}i^*_{n,o,g}}) + \overline{i^2_{n,o,gu}}.\end{aligned} \tag{11}$$

From (8), (10) and (11) noise factor can be expressed as

$$F = \frac{A^2\overline{i^2_{n,d}} + 2\mathrm{Re}(AB^*c\sqrt{\overline{i^2_{n,g}i^2_{n,d}}}) + B^2\overline{i^2_{n,gu}}}{D^2\overline{i^2_{n,Rs}}}, \tag{12}$$

where

$$A = \frac{i_{n,o,d}}{i_{n,d}} = 1, \tag{13}$$

$$B = \frac{i_{n,o,g}}{i_{n,g}} = \frac{R_S + SL_g}{R_s + SL_g + Z_{in}}Z_{in}g_m, \tag{14}$$

$$D = \frac{i_{n,o,Rs}}{i_{n,Rs}} = \frac{R_S}{R_s + SL_g + Z_{in}}Z_{in}g_m. \tag{15}$$

Finally, the noise factor for a capacitive feedback matching network is obtained from Eqs. (12)–(13) as

$$\begin{aligned}F = 1 + \frac{\gamma}{\alpha}\frac{1}{g_m,R_s}\Bigg\{&\left(|c|\alpha\sqrt{\frac{\delta}{5\gamma}}\right)^2\\ &+ (R_s^2 - s^2L_g^2)\left(\frac{1}{R_f^2} - \frac{\alpha^2\delta}{5\gamma}(1-|c|^2)s^2C_t^2\right)\\ &-(sC_tR_s)^2\left[1+|c|\alpha\sqrt{\frac{\delta}{5\gamma}}\right]^2 + \frac{2R_s}{R_f}\Bigg\},\end{aligned} \tag{16}$$

where $C_t = C_{gs} + C_{gd}$ and $\alpha \equiv g_m/g_{d0}$. By taking the derivatives of (16) with respect to R_s and L_g and let the derivatives equal to zero, optimum source noise impedance, $Z_{n,opt} = R_{s_{n,opt}} + j\omega L_{g_n,opt}$, corresponding to minimum noise figure can be written as

$$\begin{aligned}Z_{n,opt} = &\frac{\sqrt{\frac{\alpha^2\delta}{5\gamma}(1-|c|^2)+\frac{1}{Q_f^2}} + j\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\left\{\alpha^2\frac{\delta}{5\gamma}(1-|c|^2)+\frac{1}{Q_f^2}+\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}}\\ &\times\frac{1}{\omega(C_{gs}+C_{gd})}.\end{aligned} \tag{17}$$

Using (1), (17) can be re-expressed in $Z^*_{n,opt}$ as

$$Z^*_{n,opt} = \mathrm{Re}[Z_{n,opt}] + \eta\,\mathrm{Imag}[Z_{in}], \tag{18}$$

$$\eta = \frac{\left(1+\frac{1}{Q_f^2}\right)\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\left\{\alpha^2\frac{\delta}{5\gamma}(1-|c|^2)+\frac{1}{Q_f^2}+\left(1+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}}. \tag{19}$$

From (18), the imaginary part of $Z^*_{n,opt}$ is nearly the same as the imaginary part of Z_{in} and expressed as $\eta Imag[Z_{in}]$.

For the circuit in Fig. 1, the condition for maximum input power transfer (thus power-gain) is $Z_{in} = Z^*_s$ and that for the minimum noise figure is $Z_s = Z_{n,opt}$. Ideally, we have the condition for maximum power-gain and minimum noise figure is $Z_{in} = Z^*_{n,opt}$. From (1), Eqs. (17) and (18), this condition can be satisfied if η is close to 1 and

$$\frac{1}{g_m(Q_f^2+1)}\frac{C_f}{C_{gd}} = R_{s_{n,opt}}. \tag{20}$$

In the proposed technique of capacitive feedback matching network, the value of η is more close to 1 when compared to the inductive source-degeneration technique. Moreover, (20) can be satisfied by designing suitable device parameters g_m, C_{gd}, and C_{gs} of the device M1, which are related to gate-source voltage V_{gs} and transistor size W/L. In other words, the proposed design technique and input stage in Fig. 1 help to maximize the power-gain and to minimize the noise figure simultaneously by bringing Z_{in} close to the optimum source noise conjugate impedance $Z^*_{n,opt}$.

It can be seen from (1) that without the feedback gate-drain capacitance C_{gd}, the input impedance of the common-source amplifier would have no real part. However, the optimum source noise impedance $Z_{n,opt}$ in (17) has a real part. Then it is impossible to satisfy the condition $Z_{in} = Z^*_{n,opt}$. In the proposed technique, C_{gd} and the capacitive feedback matching network are used to satisfy the condition. Thus the technique is called the technique of capacitive feedback matching network.

4. Circuit implementations

The complete circuit of the proposed LNA with the output stage is shown in Fig. 3 where in the LNA stage, M1 with the input amplifier transistor and M2/M3 form the current-mirror amplifier as the second amplifier stage. The effective transconductance of the two stages is given by

$$|G_{eff}| = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_o}\right)\frac{g_{m3}}{\omega_o C_{out}} = \frac{1}{2R_s}\left(\frac{\omega_T}{\omega_o}\right)^2\xi, \tag{21}$$

where ω_T is unit gain angular frequency, g_{m3} is the transconductance of M3, C_{out} is the total capacitance at the drain of M1 which is dominated by C_{gs} of M3, and ξ is a constant approximately equal to 1 under the condition of C_{out} approaching C_{gs} of M3. So using coupling capacitor between M1 and M3 to isolate the bias levels results in serious degradation on the gain due to the parasitic capacitance of the bottom-plate of coupling capacitor. For this reason, M2 is used as the master transistor of the MOSFET current-mirror amplifier along with the slave transistor M3. The size of M2 is chosen to be very small as compared to M1 and M3 to obtain a higher current gain. Moreover, from Hspice noise simulation results, M2 contributes less than 1.5% of over all LNA noise figure. Since the cascode structure is not adopted, the proposed LNA can be operated at a low supply voltage.

In order to make the parallel resonance circuit behave like a capacitive load, a parallel resonance circuit composed of L2 and the parasitic capacitance at the drain of M1 resonates at the

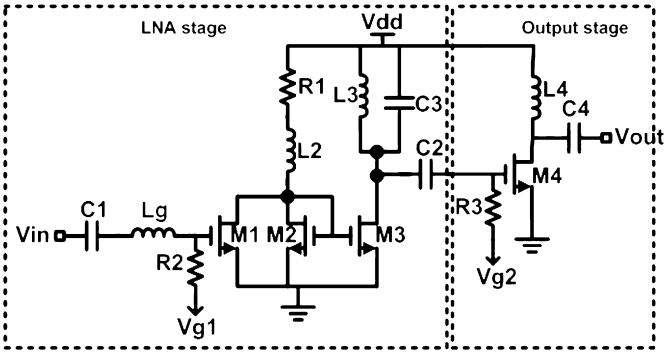


Fig. 3. The complete circuit diagram of proposed LNA.

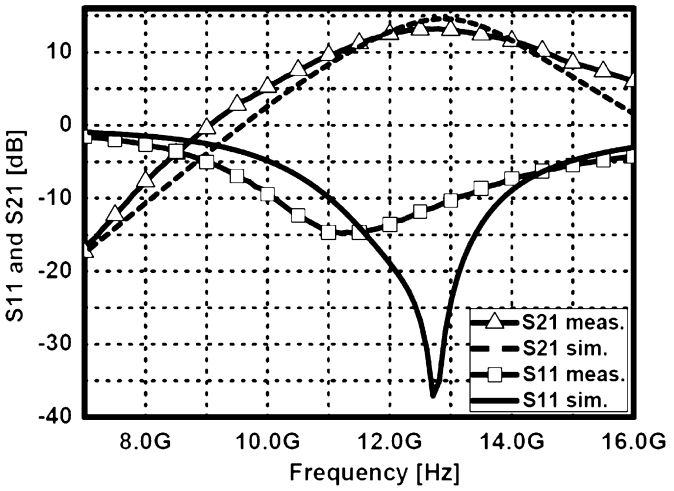


Fig. 4. The measured and simulated S_{11} and S_{21} results of the proposed LNA.

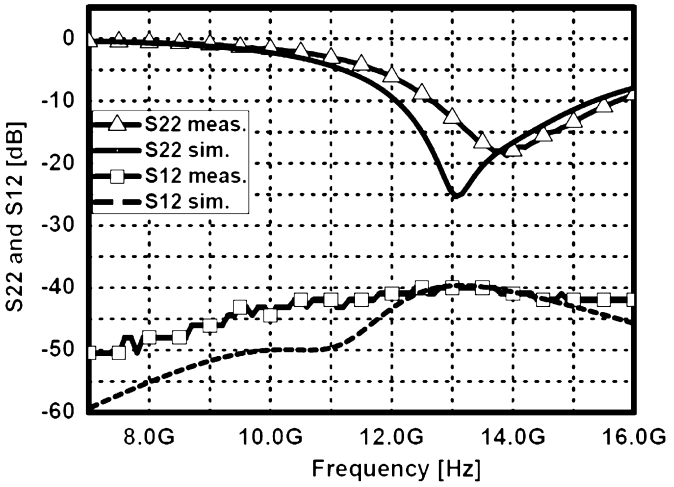


Fig. 5. The measured and simulated S_{22} and S_{12} results of the proposed LNA.

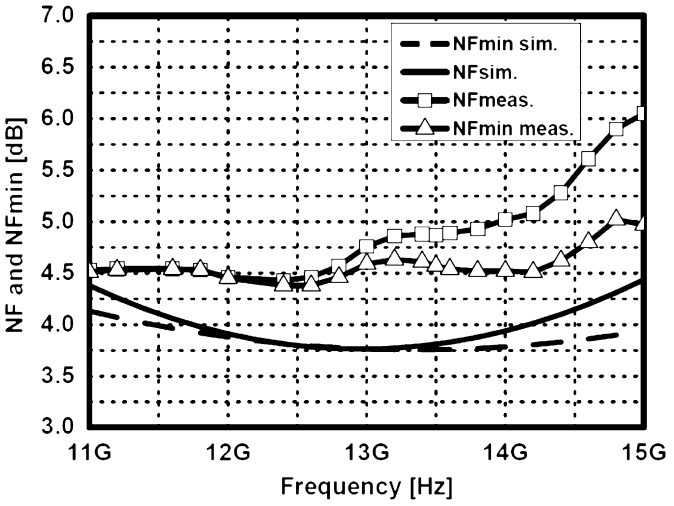


Fig. 6. The measured and simulated noise figure *NF* and minimum noise figure $NF_{\min}$ of the proposed LNA.

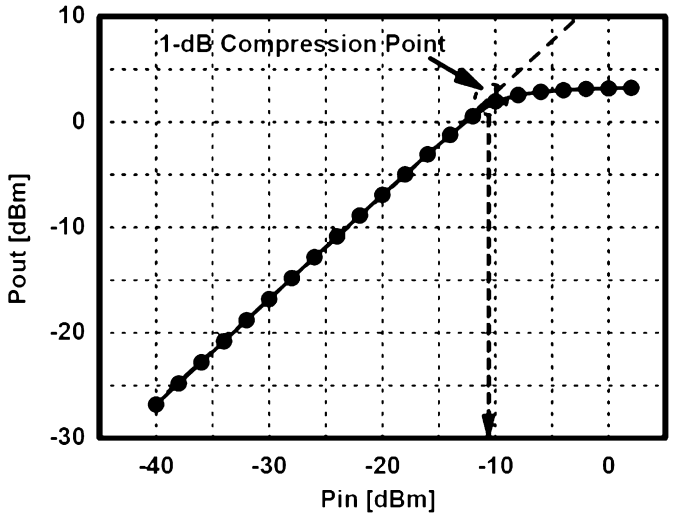


Fig. 7. The LNA measurement results of P_{in} versus P_{out}.

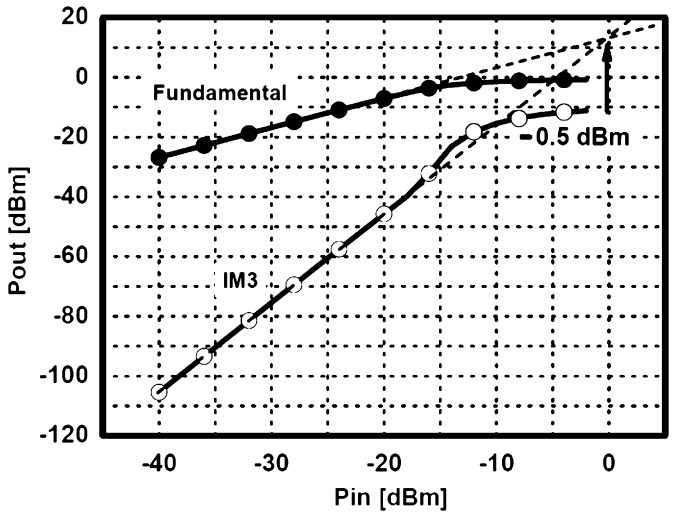


Fig. 8. The LNA measurement results of two-tone test.

frequency below the operating frequency of the LNA. R1 is used to ensure stability. C1 and C2 are dc blocking capacitors. The tank L3 and C3 is used to resonate with the parasitic capacitances of the gate M4. R2 is used to provide the gate dc bias of M1 and chosen large enough that its equivalent noise current is small enough to be ignored.

In the output stage, the output buffer composed of M4, L4, C4, and R3, is designed for the measurement purpose. R3 is used to provide the gate dc bias of M4, C2 and C4 is the dc blocking capacitor. The output inductor L4 is used to resonate with the parasitic capacitances at the drain of M4. The voltage gain of the buffer is unity.

Form (19) and under the condition of the short channel devices, the expected noise parameters of device are $\alpha = 0.6$, $\delta/\gamma = 2$, $|c| = 0.5$ and $Q_f = 2$. In the proposed LNA, the η is 0.87, while the η of the LNA with source degenerative method is equal to 0.82.

It is important to notice that some amount of mismatch in the input matching $Z_{\text{in}} = Z_s^*$ has negligible effect on the LNA performance, while the mismatch in $Z_s = Z_{\text{n,opt}}$ directly affects the *NF* [10]. Thus Re[Z_{in}] is designed to be equal to the calculated $R_{s_{\text{n,opt}}}$.

5. Experimental results

Based upon the proposed technique of capacitive feedback matching network and LNA structure, an experimental chip of a LNA operated at 13 GHz was designed and fabricated in a 0.18-μm 1*P6M CMOS* technology. The chip photograph is shown in Fig. 9 and the total die area is 746.5 μm × 884.6 μm including all testing pads and dummy metals. The performance of the fabricated LNA circuit was tested through on-wafer probing technique. The measured and simulated S21 and input return loss S11 are shown in Fig. 4. In Fig. 4 the measured S21 is 13.2 dB at 12.8 GHz. The measured and simulated output return loss S22 and reverse isolation S12 are shown in Fig. 5. As can be seen from Figs. 4 and 5, the measured reverse isolation S12 of the LNA achieves −40 dB whereas the input and output return losses are better than −11 dB. The frequency shift from 13 to 12.8 GHz is mainly due to the inaccurate modeling of planar inductor at high-frequency. Besides, the parasitic capacitances that results from metal-fill, RF-pads, and interconnection lines have minor contribution to the shift.

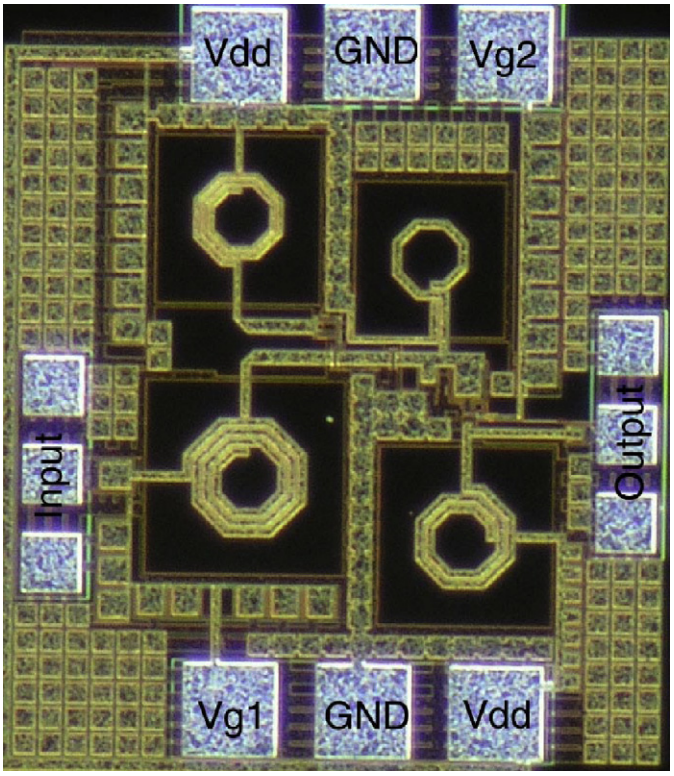


Fig. 9. The chip photograph of the proposed LNA.

The fabricated LNA has a *NF* of 4.57 dB and the minimum noise figure $NF_{\min}$ of 4.46 dB at 12.8 GHz as shown in Fig. 6. As may be seen from Fig. 6, *NF* and $NF_{\min}$ are very close to each other over a large frequency range. Thus the proposed LNA is insensitive for operating frequency variations. The measured output power versus the input power is shown in Fig. 7 where the input referred 1-dB compression gain is −11 dB m. The measured two-tone test results are shown in Fig. 8. In Fig. 8 the measured IIP3 is −0.5 dB m.

The measured performance parameters are summarized in Table 1 where comparisons with other published works are also listed.

In order to compare the performance of our LNA design, three different figures of merit *FOMs* previously presented in literature have been considered herein. In detail, *FOM*1 is defined as the ratio between the power-gain (S_{21}) in dB and the power consumption in Watt. *FOM*2 is defined to include the *NF* of the LNA. *FOM*3 takes into account the IIP3 and the operating frequency f_c as well. They can be written as [11]

$$FOM1 = \frac{S_{21}}{\frac{P_{DC}}{10^{-3}}}, \tag{22}$$

$$FOM2 = \frac{10^{S_{21}/10}}{[10^{NF/10} - 1] \times \frac{P_{DC}}{10^{-3}}}, \tag{23}$$

$$FOM3 = \frac{[10^{(S_{21}+IIP3)/10}] \times \frac{f_c}{10^9}}{[10^{NF/10} - 1] \times \frac{P_{DC}}{10^{-3}}}. \tag{24}$$

Based upon Table 1, it is clear that the proposed LNA outperforms all the other LNAs with a higher value of FOM. As expected, the proposed LNA with the technique of capacitive feedback matching network has high power-gain and low-noise figure under low power dissipation. It can be operated at a low supply voltage of 1 V since the cascode structure is not adopted. However, it still has a high reverse isolation.

Table 1
The measured performance parameters of the fabricated LNA and comparisons with other published LNAs

	This work	[5]	[6]	[6]	[7]
Tech.	0.18 μm *CMOS*	0.18 μm *CMOS*	0.18 μm *CMOS*	0.18 μm *CMOS*	90 nm *CMOS*
Topology of input matching	Capacitive feedback	Source-degeneration inductor			Microstrip line
Freq. (GHz)	12.8	14	8	9	20
Gain (dB)	13.2	10.71	13.5	12.2	5.8
NF (dB)	4.57	3.16	3.2	3.7	6.4
IIP3 (dB m)	−0.5	1.6	−3.2[a]	−1.3[a]	5.2
Power (mW)	10	28.6	22.4	19.6	10
Supply (V)	1	1.3	1	1	1.5
S11 (dB)	−11	−10	−5.8	−5.4	–
Chip size (mm^2)	0.746 × 0.885	0.88 × 0.77	–	1 × 0.9	0.7 × 0.8
FOM1	1.32	0.374	0.6	0.622	0.58
FOM2	1.12	0.383	0.92	0.63	0.11
FOM3	12.8	7.2	3.5	4.2	7.4

[a] The IIP3 is predicted by input P1 dB+10 dB m.

6. Conclusion

A new LNA structure with the technique of capacitive feedback matching network is proposed and analyzed. An experimental chip of 13-GHz LNA has been successfully designed and fabricated. The measurement results have shown that the proposed LNA can achieve minimum noise figure and maximum power-gain simultaneously. In additions, the *NF* is insensitive to the large operating frequency shift.

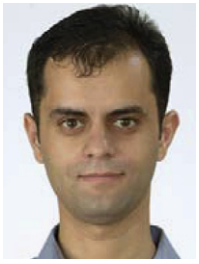
Future research will be conducted on the design of LNAs at frequencies of 24-GHz or below using the technique of capacitive feedback matching network. Besides, the integration of LNA with mixers to form receivers will be performed.

Acknowledgments

This work was supported by the National Science Council (NSC), Taiwan, under the Grant NSC-95-2221-E-009-292. The authors would like to thank the National Chip Implementation Center (CIC), National Applied Research Laboratories, Taiwan, for the fabrication of testing chip. The authors would also like to thank the support of CAD tools HFSS from Ansoft Taiwan.

References

[1] R.E. Lehmann, D.D. Heston, X-band monolithic series feedback LNA, IEEE Trans. 32 (1985) 2729–2735.
[2] F. Ellinger, 26–42 GHz SOI CMOS low noise amplifier, IEEE Solid-State Circuits 39 (2004) 2259–2268.
[3] L.M. Franca-Neto, B.A. Bloechel, K. Soumyanath, 17 GHz and 24 GHz LNA designs based on extended-S-parameter with microstrip-on-die in 0.18/spl mu/m logic CMOS technology, in: Proceedings of the 2003. ESSCIRC '03, September 2003, pp. 149–152.
[4] X. Guan, A. Hajimiri, A 24-GHz CMOS front-end, IEEE Solid-State Circuits (2004) 368–373.
[5] K.L. Deng, et al., A Ku-band CMOS low-noise amplifier, in: Proceedings of the RFIT, November 2005, pp. 183–186.
[6] T.K.K. Tsang, M.N. El-Gamal, Gain controllable very low voltage (1 V) 8–9 GHz integrated CMOS LNAs, in: Proceedings of the RFIC, June 2002, pp. 205–208.
[7] M.A. Masud, et al., 90 nm CMOS MMIC amplifier, in: Proceedings of the RFIC, June 2004, pp. 201–204.
[8] R. Fadi Shahroury, C.Y. Wu, CMOS LNA design using capacitive feedback matching network, in: Proceedings of the IPS, July 2006, pp. 101–103.
[9] A. Van der Ziel, Noise in Solid State Device and Circuits, Wiley, New York, 1990.
[10] T.K. Nguyen, et al., CMOS low-noise amplifier design optimization techniques, IEEE Trans. Microwave Theory Tech. 52 (5) (2004) 1433–1442.
[11] R. Brederlow, et al., A mixed-signal design roadmap, IEEE Des. Test Comput. 18 (6) (2001) 34–36.



Fadi R. Shahroury was born in 1977. He received the B.Eng. (with the highest distinction) degree in Electronics Engineering from Princess Sumaya University for Technology, Jordan, in 2000. He is currently working toward the Ph.D. degree at the National Chiao Tung University, Hsinchu, Taiwan. His current research interests are in low-voltage, low-power, and very high-frequency integrated circuits design and analog integrated circuits design in CMOS technology.

Dr. Chung-Yu Wu was born in 1950. He received the M.S. and Ph.D. degrees from the Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan, ROC, in 1976 and 1980, respectively. In addition, he conducted post-doc research at UC Berkeley in summer of 2002. Since 1980, he has served as a consultant to high-tech industry and research organizations and has built up strong research collaborations with high-tech industries. From 1980 to 1983, he was an Associate Professor at National Chiao Tung University. During 1984 to 1986, he was a Visiting Associate Professor in the Department of Electrical Engineering, Portland State University, Portland, OR. Since 1987, he has been a Professor at National Chiao Tung University. From 1991 to 1995, he was rotated to serve as the Director of the Division of Engineering and Applied Science on the National Science Council, Taiwan. From 1996 to 1998, he was honored as the Centennial Honorary Chair Professor at National Chiao Tung University. Currently, he is the president and chair professor of National Chiao Tung University. He has published more than 250 technical papers in international journals and conferences. He also has 19 patents including nine US patents. His research interests are nanoelectronics, low-power/low-voltage mixed-signal VLSI design, biochips, neural vision sensors, RF circuits, and CAD analysis. Dr. Wu is a member of Eta Kappa Nu and Phi Tau Phi Honorary Scholastic Societies. He was a recipient of IEEE Fellow Award in 1998 and Third Millennium Medal in 2000. In Taiwan, he received numerous research awards from Ministry of Education, National Science Council, and professional foundations.