Chapter 2
The Study on Polycrystalline Pentacene Thin Film Transistors

2.1 Introduction

Recent focus and attention on organic thin film transistors (TFTs) resulted in dramatic performance improvements [69-71]. Earlier literature pointed out that the properties of organic TFTs were highly dependent on the film quality of organic semiconductors, which were determined by pre-layer's morphology, surface energy, process temperature, thickness, and so on [72]. In the early stage, researches interests on the formation of large poly-grains or single crystal of pentacene film due to that the larger poly grains of pentacene usually have higher mobility. However the large poly grains are not the only factor to reach high mobility [72]. The detail mechanisms are still under investigated. In this chapter, we built up a simple process system to study the crystallization and growth mechanisms of pentacene. Pentacene was thermal evaporated at different substrate temperatures with various pretreatment layers. The film quality was characterized by atomic force microscope (AFM), scan electron microscope (SEM) and X-ray diffraction. The different TFT configurations were also studied, here. The inverted staggered type TFT utilizing gold as source/drain electrode and inverted coplanar type TFT utilizing Indium Tin Oxide (ITO) as electrodes were fabricated and characterized. The former so-called the top contact (TC) TFT had been proven with superior properties than the latter so-called bottom contact (BC) TFT. The reason would be briefly discussed latter.

Another topic in this chapter is the analysis of device parameters of organic TFTs.

The device performance is usually measured on basis of the following parameters: the field-effect mobility (μ), modulated on/off current ratio, threshold voltage (V_{th}), and subthreshold swing, etc. Among these, the V_{th} is one of the most important parameters. Most research literature indicates that scientists extract the V_{th} by fitting the charge sheet model equation described in Chapter 1. In large bias regime, the organic TFTs were proved to follow Eqs. (1.1)(1.2) when the gate bias exceeds V_{th}. And the item of field effect mobility was usually with the correction of $\mu = \mu(V_G)$ to compensate the gate bias dependent mobility. However, the definition of V_{th} in Eqs(1.1)(1.2) was deducted from traditional field effect transistors, yet this approach may not work with organic TFTs since most organic semiconductors only function in uni-polar operation and biased in accumulation mode. The physical value of V_{th} in organic TFTs is questionable and difficult to define [51,52].

In this chapter, we study the V_{th} of pentacene based TFTs with the inverted staggered structure featuring gold top contact. A non-linear relation between V_{th} and pentacene thickness was observed during the study. It was interesting to find that the results were different from those observed by R. Schroeder et al.[73] Thus, we opted for a numerical analysis of the current-voltage relation in terms of Fowler-Nordheim (FN) tunneling of gold/pentacene contact, space-charge limited current (SCLC) of bulk region from contact to channel, and field effect channel of pentacene transistors. In the end, we proposed a V_{th} model with the correction of bulk traps. The experimental data shows stable consistency of the model.

2.2 Experiment

The experiments in this chapter could be divided into two parts: the pentacene film morphology control by different process recipes and the fabrications of different

TFT configurations. The thermal evaporator system is schematic plotted in Fig. 2.1. The distance between crucible and substrate is confined to the limits of 15 cm due to the light molecular weight of organic semiconductors. The lamp heater is beneath and at the back of the holder. The substrates are OA-10 glass of thickness 0.7 mm and purchased from Nippon Electric Glass.

The detail process is described as below. For the standard inverted staggered type TFTs configuration (See Fig. 2.2), first, the glass substrate was cleaned with a standard detergent clean process. A 1500 Å layer of Cr was deposited on a glass substrate by sputtering and patterned by photolithography to define the gate electrodes. Then, a silicon dioxide layer of thickness 3000 Å was prepared by plasma-enhanced chemical vapor deposition (PECVD) at 106.6 Pa and 380 ℃. The gases He, O_2 and tetraethylorthosilicate (TEOS) were used with the following respective breakdown of gas quantity: 100, 3500, and 175 sccm. This layer served as the gate dielectric. Then, the samples were baked in oven at 150 ℃ for 15 min. Pentacene was purchased from FLUKA Chemical (97^+ %) and used without any further purification. The pentacene films with various thicknesses were deposited at a rate 0.5 of $Å s^{-1}$ at different substrate temperature. The pentacene active layer was thermally sublimated in a vacuum at a pressure of 10^{-5} torr. The substrate holder rotated slowly during evaporation to enhance the uniformity. Finally, the gold source-drain electrodes were deposited and patterned on the surface of the pentacene film through shadow mask evaporation.

For the inverted coplanar type TFTs configuration (See Fig. 2.3), the gate electrode was replaced by an indium tin oxide (ITO) layer of thickness 1500 Å. The layer was sputtered and patterned by photolithography. And after the same gate oxide procedure with the inverted staggered type TFT, the source/drain electrodes, also associated with a sputtered ITO layer of thickness 1500 Å, was deposited and

patterned. Finally the pentacene was thermal evaporated to form the active region as aforementioned.

The pentacene morphology experiments were fabricated as follows. First, after the same standard detergent clean process, the TEOS oxide of thickness of 3000 Å was deposited with the same recipe described above by PECVD. Then, the samples were baked in oven at 150 ℃ for 15 min. After that, a pretreatment layer of Hexamethyldisilazane (HMDS, $(CH_3)_3SiNHSi(CH_3)_3$) or a polyimide layer of thickness 3000 Å was coated on or not. Then, pentacene was thermal sublimated at different substrate temperature.

The thickness of pentacene was verified by SEM. The crystalline was verified by X-ray diffraction (XRD). The surface morphology was characterized by a Seiko Instruments, Inc. SPA-500 scanning probe microscope with DF20 tip and operated in non contact mode at 1Hz scan rate. The work function of ITO and the ionization potential of pentacene were 4.96 and 5.30 eV, respectively. Which were measured by photoelectron spectrometer (Model AC-2, Riken-Keiki Co.). The inverted staggered type organic TFTs all have the channel width and channel length of 1000 μm and 100 μm, respectively. All current–voltage (*I*–*V*) measurements were made using a Hewlett-Packard 4155B Precision Semiconductor Parameter Analyzer in a dark chamber under conditions of high vacuum. The capacitance-voltage (CV) measurement of the source (gold)/pentacene/oxide/gate(Cr) configuration in each TFT was performed at low frequency of 500 Hz by using Hewlett-Packard HP 4284 Precision LCR-meter in the ambient air.

2.3 Result and Discussion

2.3.1 The Growth of Pentacene

The most of difficulties to analyze the properties of pentacene based TFTs is the uncertain reproducibility. Therefore, the study on the properties of pentacene TFTs sometimes focused on the qualitative analysis rather than quantitative analysis. Fig. 2.4 denotes the surface morphology of pentacene at different substrate temperatures of room temperature, 50 ℃, 70 ℃, and 90 ℃, respectively. These figures depicted the definitely without doubt polycrystalline morphology of pentacene. Obviously, the sizes of ploy grains gradually increase from 0.5 μm to nearly 1.5 μm when process temperature increases. The phenomenon was also observed by C.D. Dimitrakopoulos et al [74]. At very low substrate temperature, the rod-like pentacene molecules do not have sufficient momentum to move during deposition, thus the molecules would immediately stick when they reach the surface of substrate, therefore forming an amorphous type film structure. When the substrate temperature increase, the pentacene molecules have enough momentum to arrange a well-ordered crystalline structure, therefore a poly crystalline morphology would be observed. In our experiments, the room temperature sample formed a poly crystalline morphology with smaller poly grains. When substrate temperature exceeded 50 ℃, the size of poly grains will stop growing and keep its size in the range of 1.5 μm. The process dependent grain size need to be further considered with the nucleation mechanism of pentacene. IBM reported that the pentacene growth mechanism would be divided into three steps [75]. First, the resolution limit step, pentacene molecules form the crystalline seeds in the beginning. The resolution strongly depends on the interaction between pentacene molecules and surface molecules of substrate. This mechanism was not fully understood yet [76]. Second, the diffusion limit aggregation step, where molecules diffuse on a surface and stick to any existing island, without further diffusion. Third, the coarsening step, the pentacene islands coarsen until the grains touch each other. In our experiments, the grain size might be limited by the first step

which depends on the interaction between pentacene and oxide.

Fig. 2.5 shows the pentacene morphologies on different pretreatment layers. The sample of Fig. 2.5(a) was fabricated by following the inverted coplanar TFT process. Fig. 2.5(a) denotes the worse morphology of pentacene on oxide than that of Fig. 2.5(b)(c). On the contrary, Fig. 2.5(c) depicts the largest grain size even to 3 μm. This phenomenon could be explained by the theory mentioned above. HMDS, here processed by vacuum evaporation, used to be a promoter material in silicon integrated circuit process. It contains many carbon-hydrogen bonds (alkyl groups at the terminals of molecule) that have weaker interaction with pentacene than that of the dangling bonds on oxide surface. Therefore, in the first nucleation step, the crystal seeds of pentacene would separate far away from each other, which leave larger room for grain growth than the case on oxide surface. The case of the polyimide pretreatment layer was similar, but the amount of alkyl groups was more than that of HMDS. The spun on polyimide is one of the polycarbonates which have many kinds of derivatives. In this experiment, the used polyimide belongs to a kind of alignment layer for liquid crystal. The surface energy and surface roughness of the polyimide might also enhance the grain growth of pentacene except the rich of alkyl groups. The detail mechanism was still investigated. Fig. 2.6 (a) and (b) demonstrated the XRD result of pentacene growth on oxide and polyimide, respectively. Both them apparently revealed the crystalline phase of so-called “thin film phase” with d(001) value of 15.4 Å, which gave the first order diffraction peak at 5.7˚. But, in the oxide case, another crystalline phase of so-called “single crystal phase” with d(001) values of 14.4 Å at the peak range from 5.9˚ to 6.2˚ appears. Pentacene on the polyimide denotes almost only one crystalline phase, but that grown on the oxide mixes two crystalline phases.

In a short summary, pentacene crystallization as a continuous film was

influenced by substrate temperature, morphology and function groups of previous layer, and so on. Although many approaches were proposed to enhance pentacene grain growth, however larger poly grains do not mean better electrical properties. A good interface between pentacene and gate dielectric layer is another key factor. In TFT applications, a single phase of pentacene crystal is preferred for carrier transport due to the lack of interference between two kinds of orientation of pentacene molecules.

2.3.2 Comparison of Top Contact and Bottom Contact Configurations

In the section, two types of TFT configurations were adopted. The detail process was described in section 2.2 Experiments. The pentacene thickness was 65 nm in all samples. Fig. 2.7 shows the inverted coplanar (BC) TFT utilizing ITO as source/drain contact. The device parameters were extracted by following the charge sheet model (Eqs (1.1)(1.2)). In a specific description, they were described as, the threshold voltage (V_{th}) of -12.5 V, a field effect mobility (μ) of 0.11 cm^2/vs, a sub-threshold slop (SS) of 4 V/decade, and an on/off ratio in the order of 10^6. The measurement was done in vacuum. In ambient air, pentacene TFTs perform inferior electrical properties, and that would be discussed in chapter 3. Fig 2.8 shows the inverted staggered (TC) TFT utilizing Au as electrodes. It has superior properties with a V_{th} of -7.09V, a field mobility of 0.29 cm^2/vs, a sub-threshold slop of 10.2 V/decade, and an on/off ratio in the order of 10^5. The threshold voltage was hard to define in organic TFTs. The calculation approaches and difficulty were discussed in the following sections. As well as the detail considerations of mobility would be done in chapter 3. Comparing the different type pentacene TFTs, the ITO BC TFT demonstrated lower field effect

mobility than that of Au TC TFT. The threshold voltage of both was similar. But the SS and on/off ratio of Au TC TFT was worse than that of ITO BC TFT. In the small drain bias regimes of Fig. 2.7(b) and Fig. 2.8(b), the ITO BC device apparently shows a worse non-linear region than Au TC TFT. This effect was attributed to the contact resistance between source/drain electrodes and pentacene. The junction between pentacene with Au and ITO was supposing to be a schottky or an ohmic contact. To further concern, the work function of ITO in lab was measured as 4.96 eV by ultraviolet photoemission spectroscopy (UPS), although it may range from 4.8 eV to 5.1 eV indeed. The HOMO level of pentacene was measured as 5.3 eV, though its values were reported as 4.8 eV or even higher to 6.2 eV. The work function of Au was supposing as 5.1 eV [77]. From the inference, the barrier height of pentacene/Au would be smaller than that of pentacene/ITO. That could explain the better mobility in Au TC TFT, because the carrier injection from Au electrodes to pentacene was easier than that of ITO BC TFT.

Beside, the surface morphology of pentacene in ITO BC TFT was investigated. In Fig. 2.9 (a)(b)(c) show the result of pentacene on ITO electrodes, on the transition region between ITO to oxide channel, and on the oxide channel region, respectively. The result was very interesting and also observed previously [78]. The pentacene on ITO has a small grain size about 20 nm. At the transition region, pentacene grains were still small. Until far away from ITO electrodes, pentacene grains gradually became large. The photolithography of ITO process was believed to damage the TEOS oxide surface. To improve the conductivity of ITO, an annealing process of 100 ℃ to 150 ℃ was done. This process could improve ITO to crystallize and form a poly crystalline structure. However, at the mean time, this behavior also increases the surface roughness of ITO. That deduced the small poly grains of pentacene on ITO. On the other hand, at the etching process of ITO, the etchant would damage the TEOS

oxide surface and change the surface energy that also decrease the grain growth of pentacene on it. Therefore, the small poly grains of pentacene in ITO BC TFT should be responsible for the smaller mobility than that of Au TC TFT.

Although the Au TC TFT configuration has a better carrier transport behavior than ITO BC TFT, this configuration still surfer from some issues. Such as the bulk region between source/drain electrode to effective channel would limit the threshold characteristics due to the conduction mechanism of organic semiconductor. That would be discussed in the following section. On the other way, the top contact through shadow mask process is not suitable for mass production. However the photolithography process usually damages the organic semiconductor, the top contact need specially process skills, like printing process. That is why in chapter 4, the ITO BC TFT configuration was chosen, it match the niche for mass production.

2.3.3 V_{th} Model Proposed by R. Schroeder

The following section, we try to study the threshold voltage behavior in the gold top-contact pentacene TFTs. The device configuration and the corresponding cross section view at source terminal by SEM are shown in Fig. 2.10(a)(b). Fig. 2.11 shows the top view of channel region for different pentacene thickness samples. In Fig 2.11 (a) the very thin case, pentacene molecules have not form a continuous film, yet. Fig 2.11(b)~(d) show the grain growth behaviors. An interesting polymorphism seems been observed. As long as the thickness increased, the grain size increased and the surface roughness also increased. Till the case of Fig. 2.11(e), the grains shrank. An possible inference was made. The rod-like pentacene molecules crystallized layer by layer, and it depended on the previous layer conditions. At the grain growth cycle, the size and roughness increased at the same time until a saturation condition. The grains

no longer grew, and the following pentacene molecules only saw the high roughness pre-layer. Therefore the stacking of the following pentacene formed smaller grains. The situations are still under study and verified.

Figure 2.12 shows the transfer characteristics of four gold top-contact organic TFTs with different pentacene thickness on (a) a log scale and (b) a double-logarithmic scale. Obviously, the organic TFTs show larger on-current and more positive V_{th} for the device with thinner pentacene film. Gold is expected to form an ohmic contact with pentacene, since its performance measure of 5.1 eV is close to the ionization potential of 5.3 eV typical for pentacene. However, recent study [79,80] pointed out that gold/Pentacene conjunction in real world applications may form a barrier height larger than 0.8~1.0 eV depending on the sample and varying with each lab fabrication. At the same time, the barrier height fell into the range of FN tunneling. Accordingly, R. Schroeder [73] proposed a model to analyze the V_{th} shift in bottom gate, gold top contact pentacene TFT. The researchers assumed that the thicker the pentacene layer was, the more gate bias (V_G) needed to be applied to reach a critical electrical field allowing the carriers to conquer the barrier height of gold/pentacene junction. Such behavior is presented and corrected by the following equation:

$$V_{th}(t) = V_{th}(\Omega) + V_{th,inj}(t) = V_{th}(\Omega) + E_{crit}t \qquad (2.1)$$

where $V_{th}(t)$ is the overall threshold voltage, $V_{th}(\Omega)$ is the intrinsic threshold voltage if gold/pentacene junction is ohmic, $V_{th,inj}(t)$ is thickness-dependent injection barrier contribution, $t = t_i + t_S$ is the combined thickness of insulator and semiconductor, and E_{crit} is the critical field. Two potential problems may arise in the proposed model. First, the carrier injection from gold source to pentacene may be dominated by FN tunneling as indicated the researchers' assumptions. Based on the assumptions, we expected to see obvious non-linear current-voltage behavior in small

drain bias (V_D) region in output characteristics since the V_D should conquer the FN barrier to induce carrier injection. However, the phenomenon does not have a predictable behavior pattern and may not always follow the FN tunneling equation. The details of the study are discussed later. Second, the electrical field between source gold and gate electrode was assumed to be uniformly distributed. Nevertheless, in real world cases, different mediums and interfaces have different electrical field distribution. The biggest drop of gate bias voltage was noted in the gate oxide not the pentacene, and also a part of V_D dropped in the gold/pentacene junction when contact behaviors were governing the carrier transport. Therefore, electrical field distribution had to be considered further and our research indicates that it would not distribute uniformly.

2.3.4 Space-Charge Limited Current in Linear Region

Here, we assumed that the carrier transport between source/pentacene and channel surface could be considered as a combination of two factors. These are the contact and pentacene bulk region. At small bias regime, the contact of gold/pentacene would govern the injection current of organic TFTs. With the increasing bias, the bulk characteristics would limit the carrier transport. For organic semiconductors, even pure non-doped organic film containing no net charges, large amounts of holes or electrons that are determined by the space-charge limited current, (SCLC) are transported crossing thin films, when efficient charge injection occurs at electrode/organic interfaces. The SCLC theory equation is presented below:

$$j_{SCLC} = \frac{8\varepsilon\mu V^2}{9d^3} \tag{2.2}$$

where j_{SCLC} is the SCLC current density, V is the applied voltage between two electrodes, and d is the distance between two electrodes. The contact and bulk limit

carrier transport behaviors could easily be distinguished in organic light emitting device field due to its two terminal electrodes. However, in the top contact organic TFT, the direct evidence of the SCLC was a little difficult to distinguish because the field effect governs the current-voltage relation in most bias regime cases.

In Fig. 2.12, the pentacene TFTs was cut-off at small gate bias. With the increase of gate bias, the charges started to accumulate and form the conduction channel. Under such conditions, the drain current (I_{DS}) would be restricted by the FN tunneling of gold/pentacene contact, SCLC current of bulk region from contact to channel, and field effect channel. Here, the FN tunneling current exhibited exponential growth, and the last two items were proportional to V^2. The figure denotes that the log(I_{DS}) and log (V_G) relation is almost linear in four studied samples. Such behavior explains the relation of $I_{DS} \propto V_G^{\,n}$. The shift of the lines was attributed to the shift of V_{th}. The result seems a little unclear and undefined. Furthermore, the Fig. 2.13 depicts that the dependence of log(I_{DS}) on log(V_D) was linear at small V_D of large V_G. That presents $I_{DS} \propto V_D^{\,n}$ at small V_D. When V_G of -100 V was applied, the field effect channel was formed, the conductivity of channel was assumed to be very high and the current flowing through channel was nearly proportional to V_D at small V_D regardless of the non-ideal effect. Based on the inferences, at small V_D and high V_G, the V_D must sustain the voltage drop of gold/pentacene FN tunneling contact, the pentacene bulk region from contact to channel, and the channel equivalent resistance. Thus the current flows would be limited by three items. The first is the exponential growth function, the second is $I_{DS} \propto V_D^{\,n}$ function, and the last is linear to V_D.

Fig. 2.14 shows the linear scale plot of I_{DS} against V_D. At small V_D, the I_{DS} were not linear with the V_D. The non-ideal effect was extensively discussed before.[81,82] In general, it was attributed to the non-ohmic contact of source/drain with pentacene;

it may be Schottky or FN tunneling contact. Since both of them represented exponential growth function the Fig. 2.13 shows the linear relation of log (I_{DS}) with log (V_D) at small V_D suggesting the $I_{DS} \propto V_D^{\,n}$ relationship. The relationship corresponds to SCLC current-voltage requirement. Thus, we believe that the SCLC of contact to channel region would be the dominating and limiting factor at small V_D. When the V_D is increased, it becomes apparent that the field effect channel governs the whole current-voltage relation.

2.3.5 Pentacene Bulk Traps dependent V_{th} Model

Figure 2.15 shows the extracted V_{th} of four different pentacene thicknesses TFTs. The V_{th} was extracted carefully utilizing different methods in order to verify that the V_{th} due to its physical origin remained unclear. The square root method was normally used and yielded a similar result to that of the constant current (CC) method. The maximum transconductance (Gm) method had a larger variation when compared with the square root method and CC method. Obviously, the V_{th} was strongly affected by extraction methods. This influence may be explained by the gradual accumulated channel formation, gate bias dependent mobility and other factors. It is hard to distinguish the subthreshold and turn-on region. Hence, the different numerical methods would provide different V_{th} data. Detailed study will be further performed in the future. In addition, the data from CV measurement strongly depended on the charge accumulation condition of the channel; the resulted V_{th} was closer to a real world measurements.

In Fig. 2.15, we observed the non-linear relations between V_{th} and the pentacene film thickness. The results are quite different from the linear relation recorded by R. Schroeder et al. On the other hand, we also found that some reported data indicated

the pentacene thickness independent V_{th}.[83] In ideal case, actually, the V_{th} should be independent from the semiconductor thickness. However, the pentacene film demonstrated a defect and trap rich quality that would be charged during conduction. The defects or the traps may be presented as an acceptor-like dopant concentration or treated as trap density states [84-86]. We assumed that the charges in pentacene layer were uniformly distributed featuring the same density in different thickness samples. The gate voltage must add another excess item to conquer the influence of the trapped charges. Here, we assumed the charges were fixed and corresponded to different gate bias values through the relative capacitance. Thus the delta V_{th} could be presented as the integration of total amount of trap charges over the relative capacitance from insulator to semiconductor. The equation could therefore be expressed as:

$$V_{th} = q\int_{t_i}^{t_i+t_s} \frac{n_{bt}}{C(x)}dx + V_{t0} \approx \frac{qn_{bt}}{2\varepsilon}\left[(t_i+t_s)^2 - {t_i}^2\right] + V_{t0} \qquad (2.3)$$

where $C(x)$ is the equivalent capacitance that varied along with the distance x of charges and gate electrode, t_i is the insulator thickness, t_s is the semiconductor thickness, n_{bt} is the constant bulk trap density, ε is the dielectric constant of silicon oxide and pentacene (ε of silicon oxide is 3.9 and pentacene is about 4 [87]. For simplicity value of ε is assumed as 4 in this article.), V_{t0} is the ideal case V_{th} if no impurities or traps exist. The line in Fig. 4 presents the simulated results by fitting the experimental V_{th} data extracted from by different methods. The solid and dashed lines correspond to the square root method and CV method, respectively. The fit is good, with the value of V_{t0} of 0V~-5V being reasonable and normally observed in other TFT technology. The n_{bt} was also estimated to be the order of 10^{17} cm^{-3} based on our model. The value of trap density was similar to the calculated results measured by Horowitz and Schon [84,88] and smaller than result obtained by Rashmi[85]. Trap density value was also smaller than the unintentional doping of Verlaak [86].

Nevertheless, the measurements are still very consistent with the theory.

2.4 Conclusion

Summing up the findings of our research, the basics of pentacene growth mechanism was studied. A suitable pretreatment layer or an adequate growth conditions would improve the crystallization of pentacene. In the electrical analysis of the inverted staggered TFT using Au as electrodes, we should note that recorded data shows a non-linear relation between threshold voltage and pentacene thickness in organic TFTs. The relation follows a square law in our proposed model based on uniformly distributed traps in pentacene film. The trap density can also be extracted by Eq. (2.3) and the magnitude of the value matches the results of other researchers. The good fitting suggest that the V_{th} could be suppressed by enhancing the pentacene film quality or reducing the unintentional dopant. The aforementioned quality enhancement and dopant reduction can be achieved by purification of pentacene. In the research, we also examined the FN tunneling of gold source to pentacene, SCLC from source/pentacene junction to field effect channel and the field effect conduction relationship in pentacene TFT. The SCLC was found to dominate the current-voltage behaviors in small V_D bias regime. The quantity of SCLS current was difficult to measure in pentacene TFT because of its three terminal device and complex behavior. The further investigation will be required in the future.

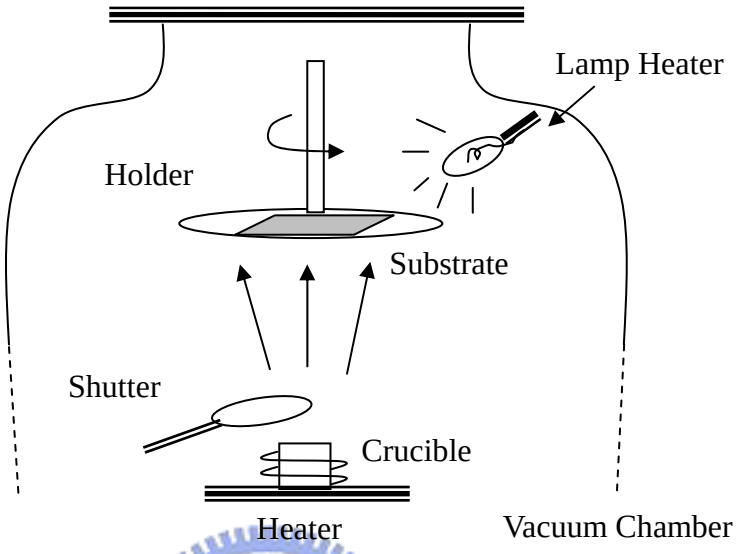


Fig. 2.1 The vacuum thermal evaporation system for pentacene.

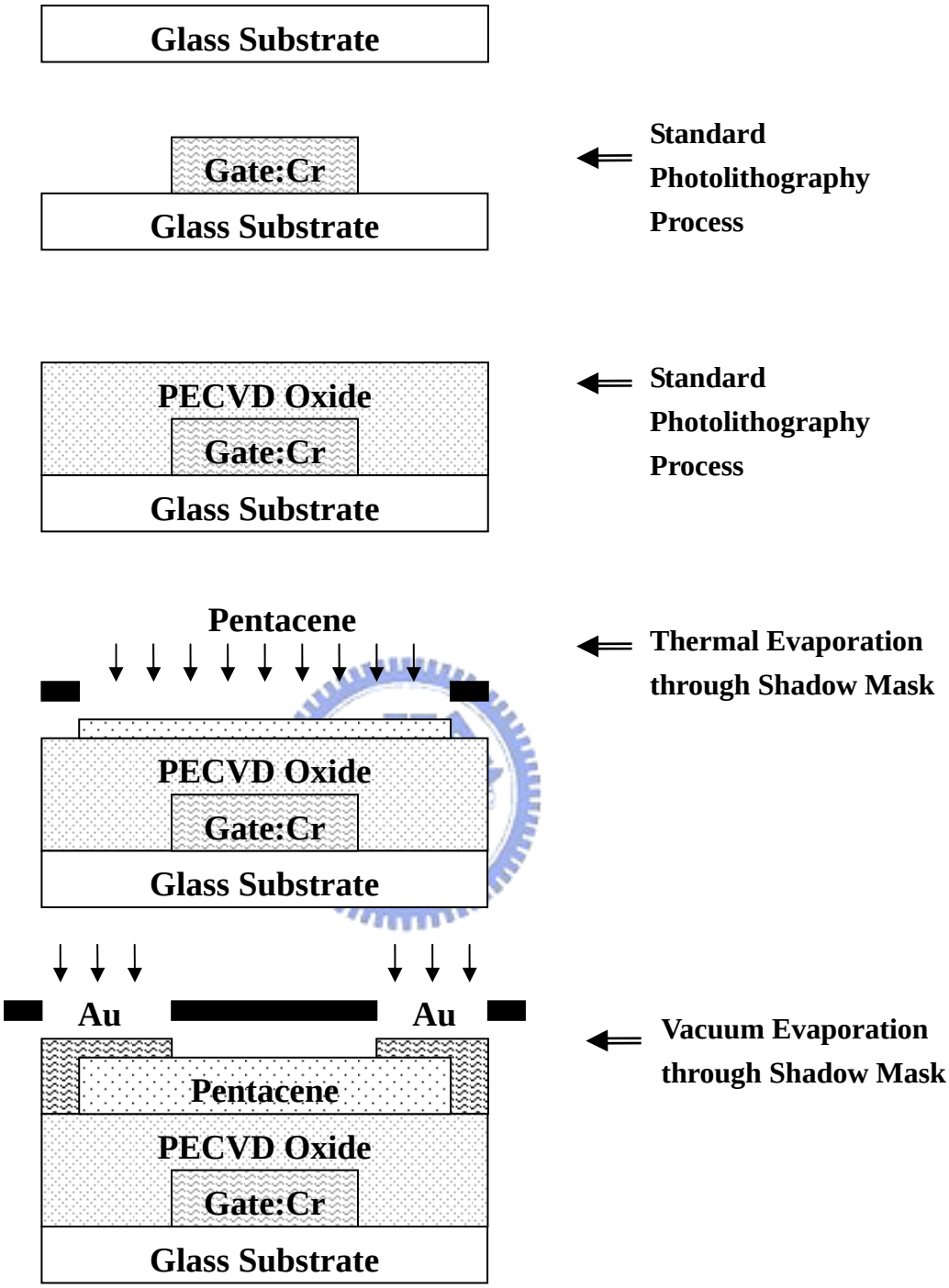


Fig. 2.2 The fabrication process flow of inverted staggered type pentacene TFTs with Au as contact electrodes.

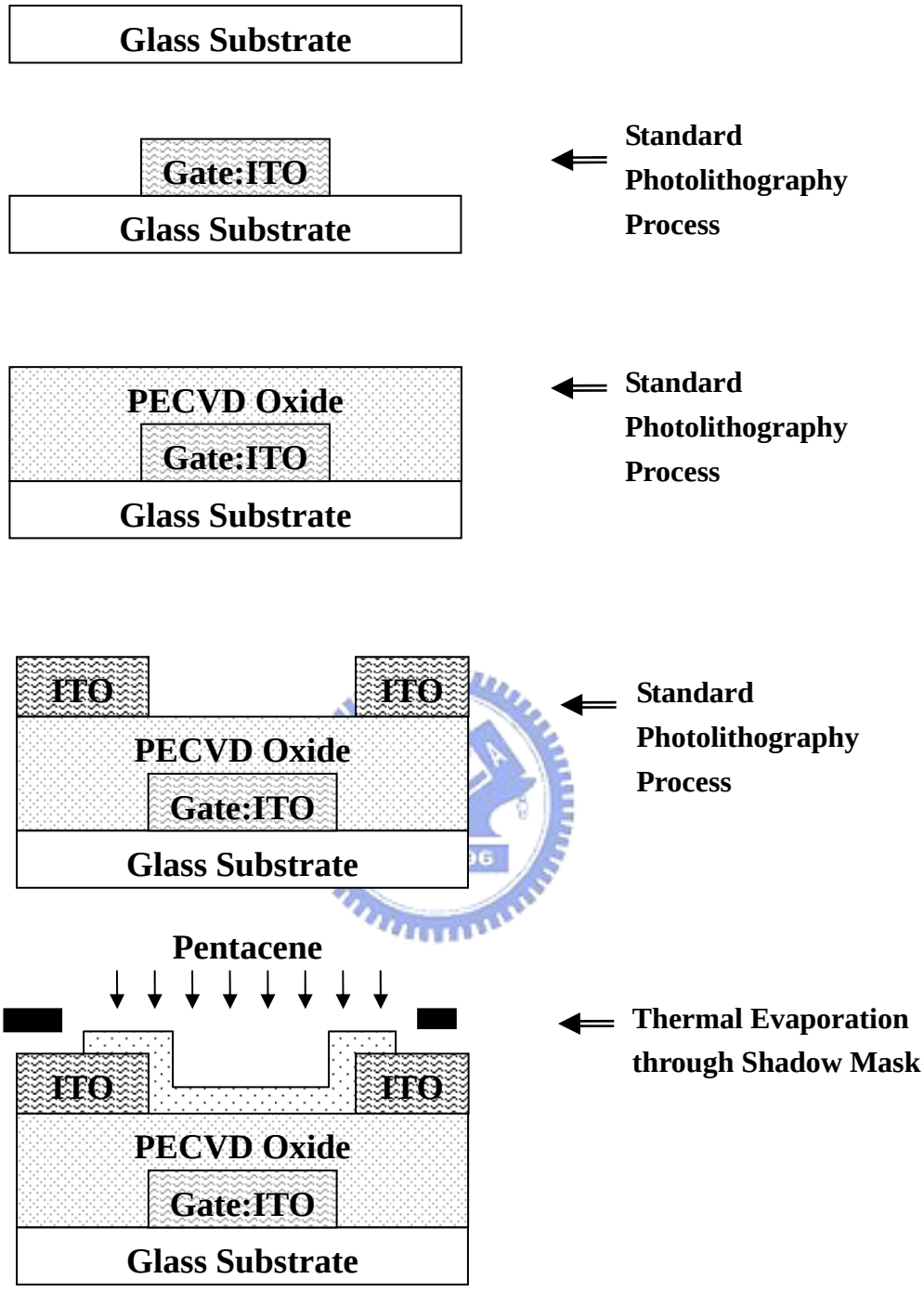


Fig. 2.3 The fabrication process flow of inverted coplanar type pentacene TFTs with ITO as contact electrodes.

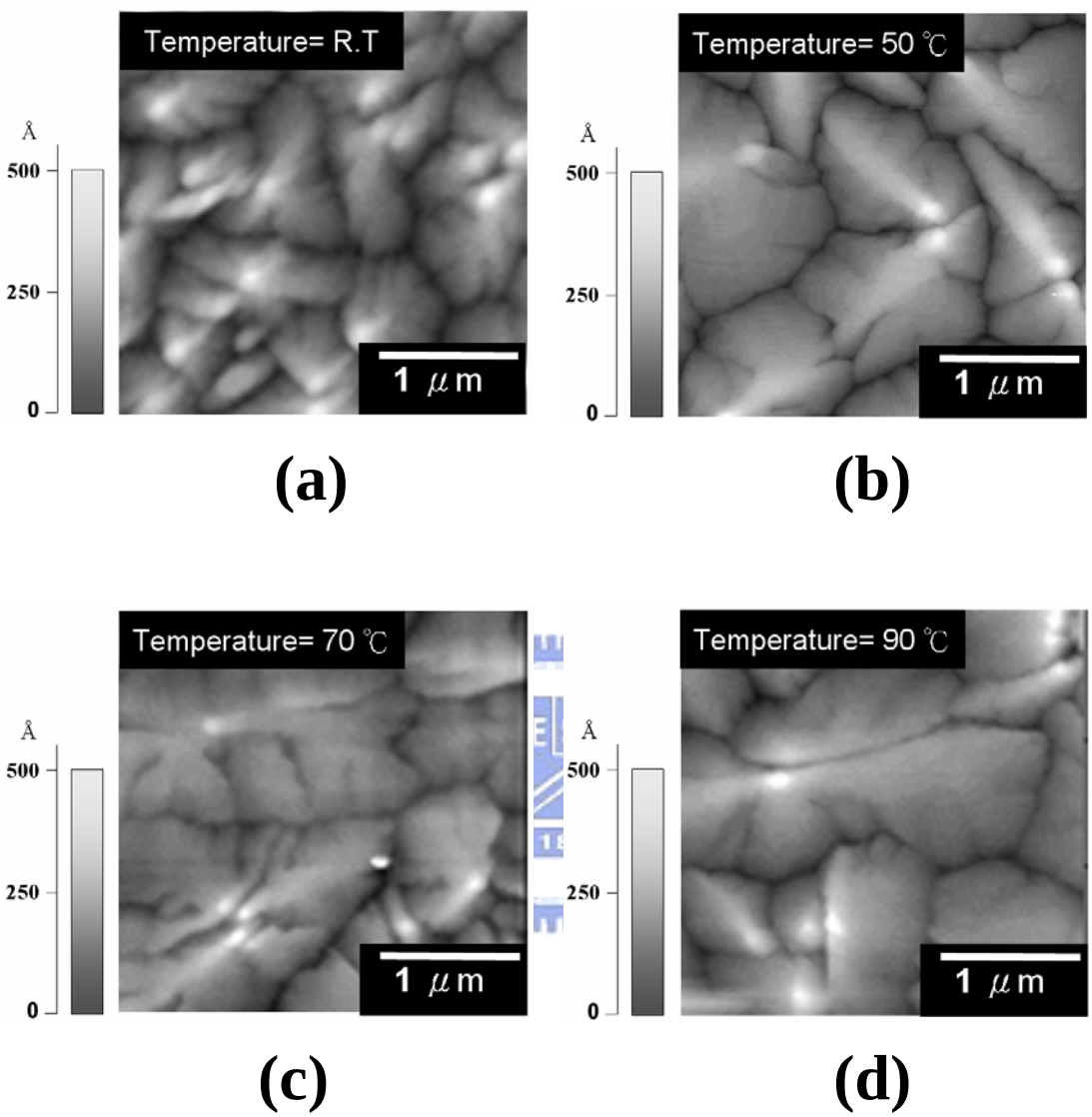


Fig. 2.4 The pentacene growth on silicon dioxide with different substrate temperatures of (a) room temperature, (b) 50 ℃, (c) 70 ℃, and (d) 90 ℃, respectively.

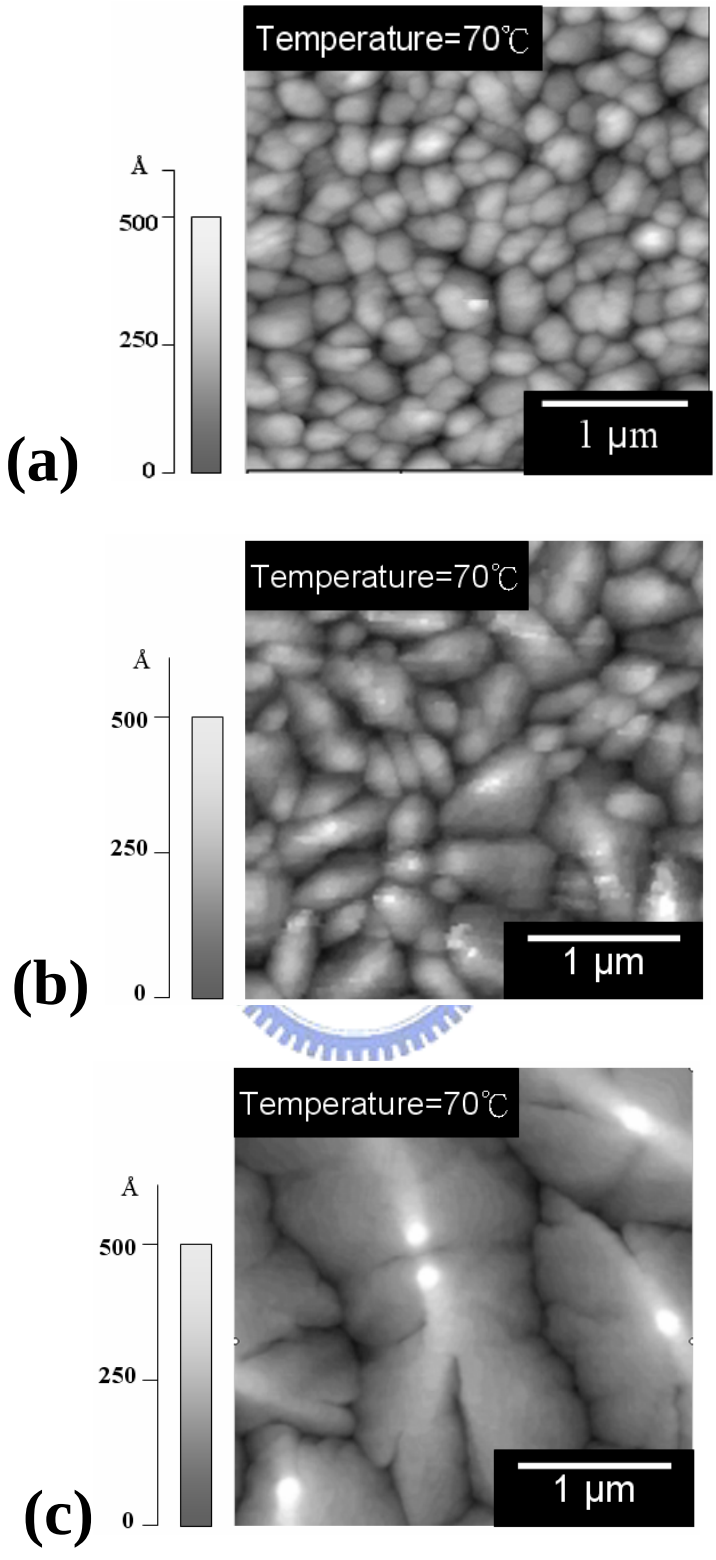


Fig. 2.5 The pentacene growth on oxide with different surface treatment layer (a) without any pretreatment, just only oxide, (b) with HMDS treatment, (c) with a layer of polyimide, all with substrate temperature 70 ℃, respectively.

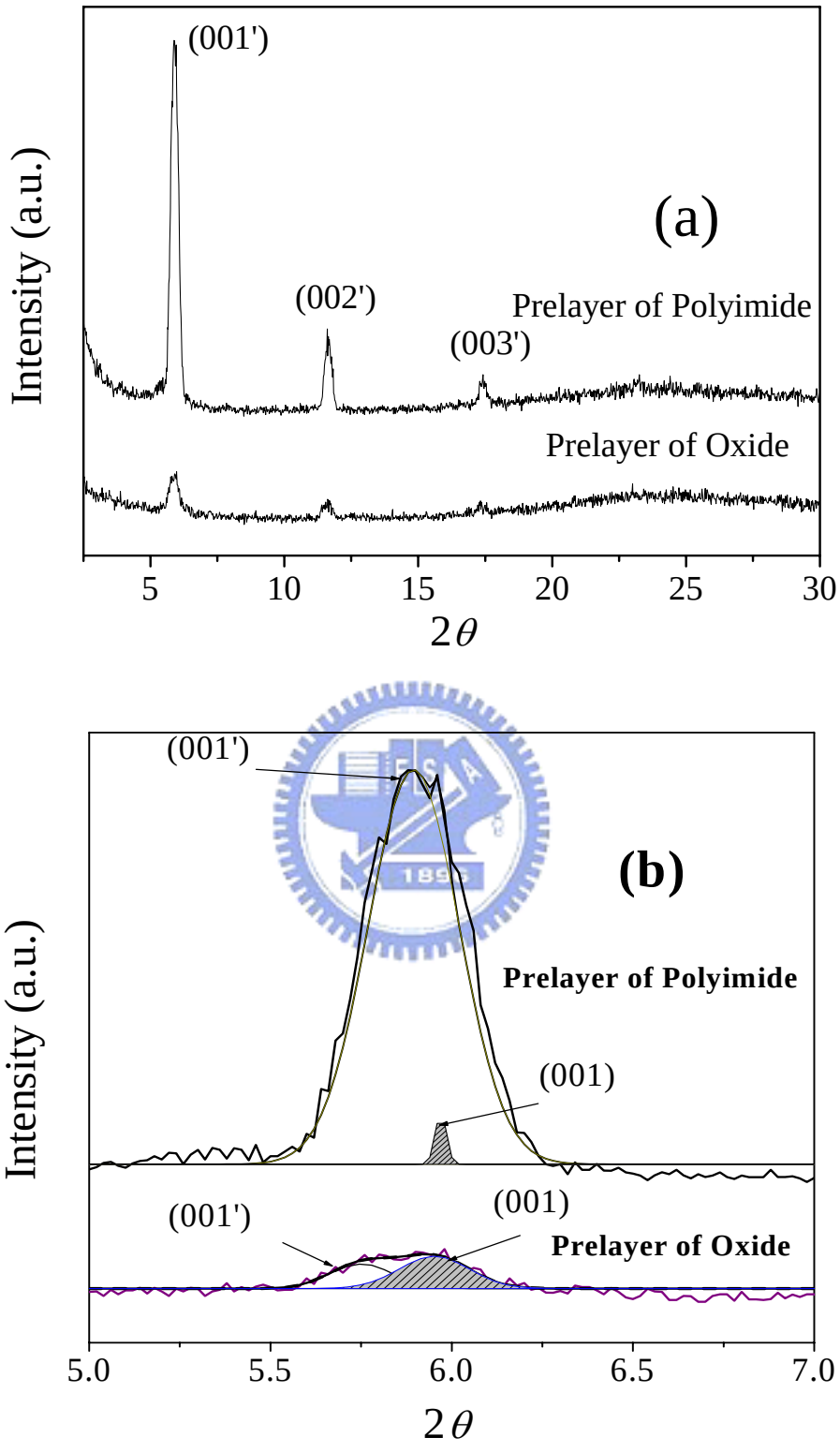


Fig. 2.6 (a) The X-ray diffraction plot of Fig. 2.5(a)(c) samples, pentacene was grown on oxide or polyimide layer, respectively. (b) The enlargement and analysis of (a).

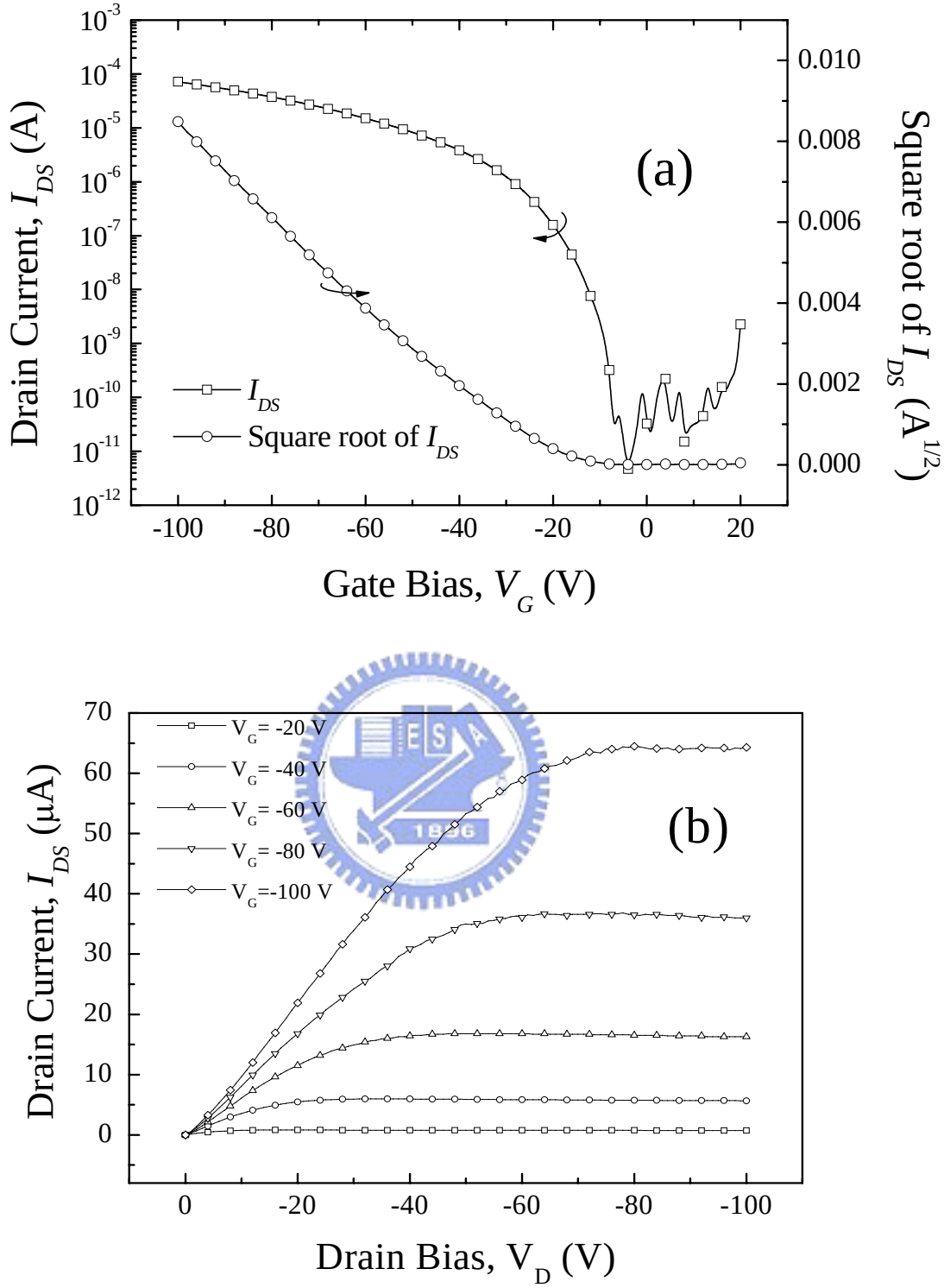


Fig. 2.7 The properties of an inverted coplanar pentacene TFT utilizing ITO as electrodes with channel width 500 μm and channel length 37 μm. (a) The transfer curve of V_D= -80 V. (b) The output curves.

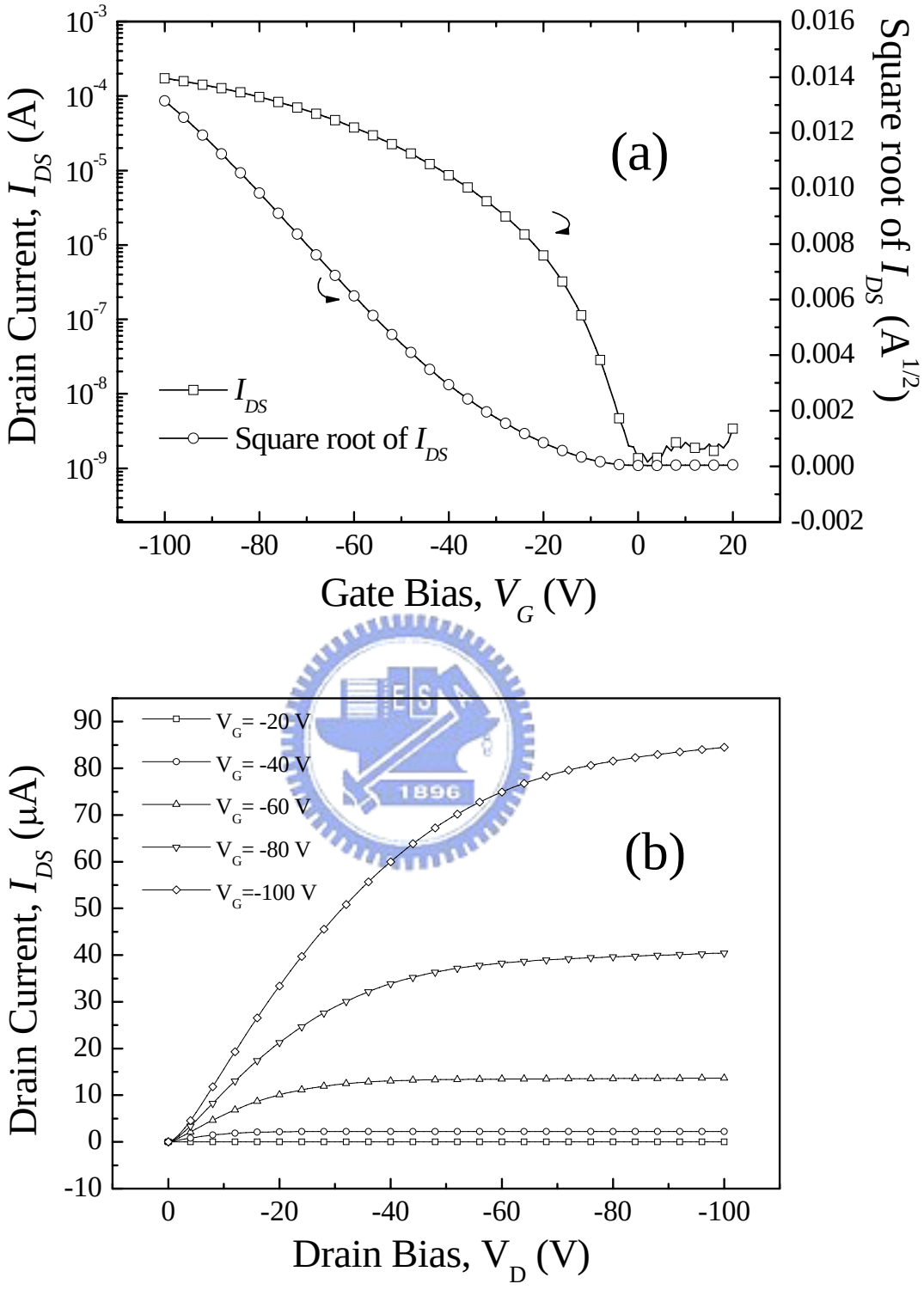
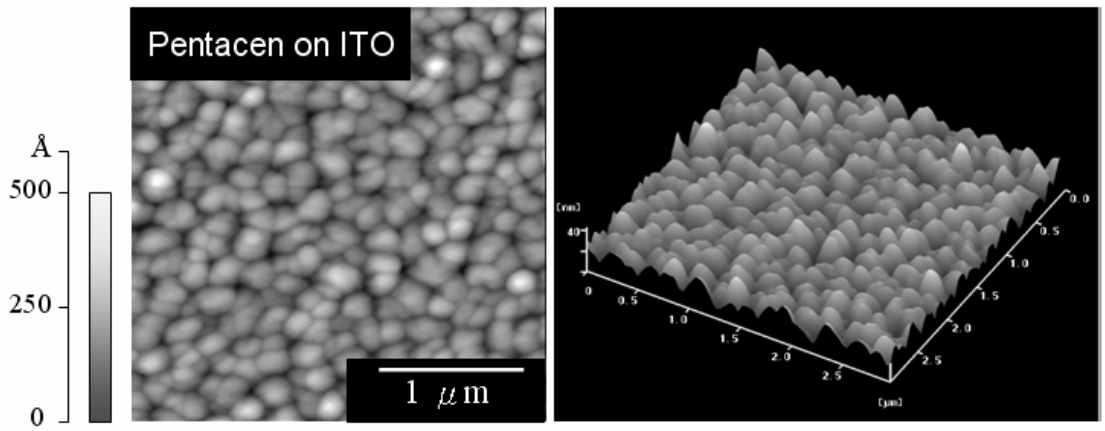
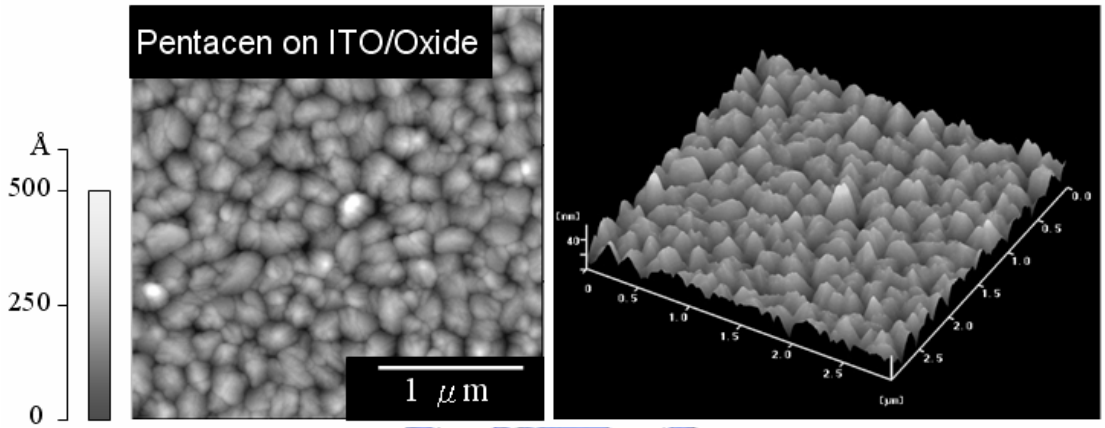


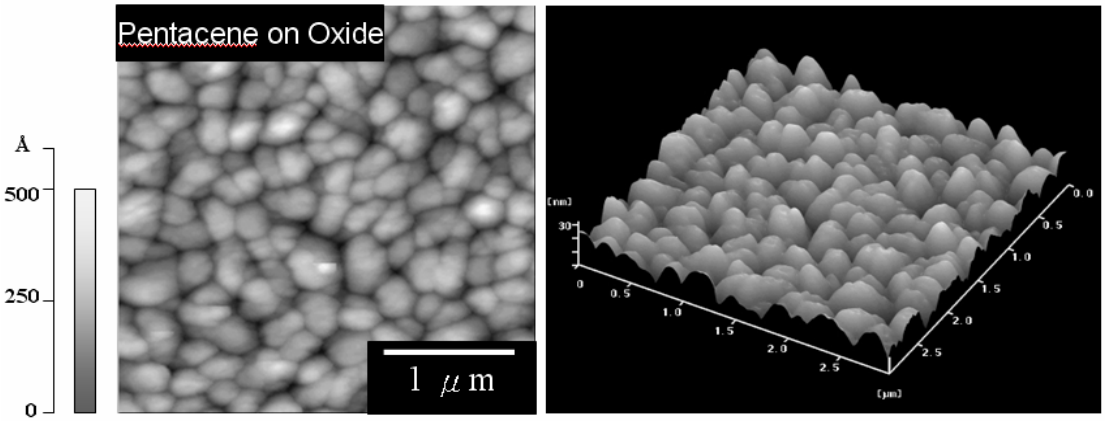
Fig. 2.8 The properties of an inverted staggered pentacene TFT utilizing Au as electrodes with channel width 1000 μm and channel length 100 μm. (a) The transfer curve of V_D= -100 V. (b) The output curves.



(a)

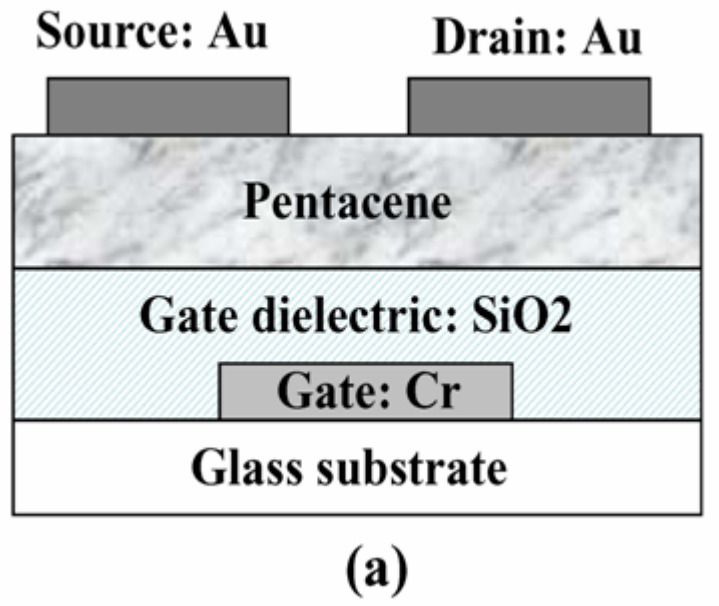


(b)



(c)

Fig. 2.9 The surface morphology of pentacene on an inverted coplanar type TFT utilizing ITO as electrodes, (a) pentacene on ITO electrode, (b) pentacene on the junction of ITO electrode and channel oxide region, and (c) pentacene on the oxide channel region.



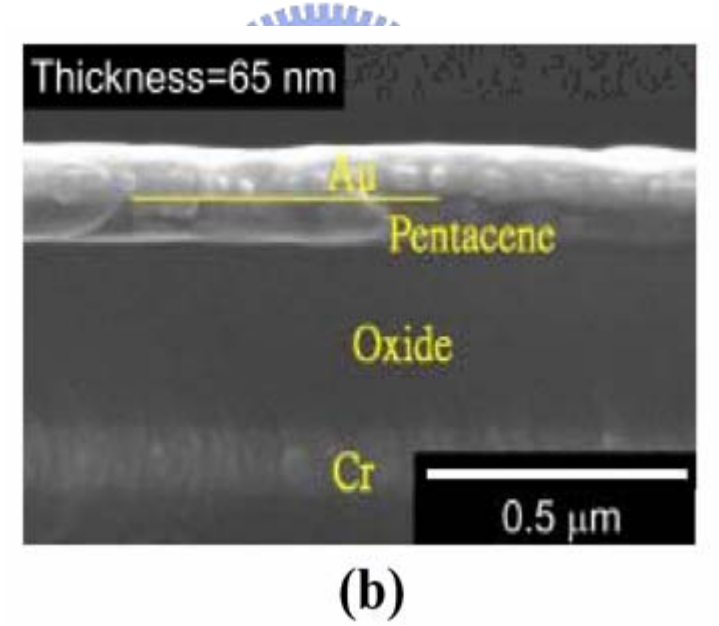
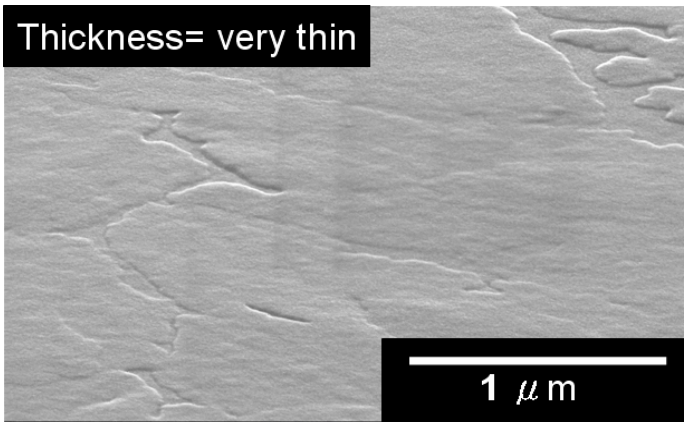
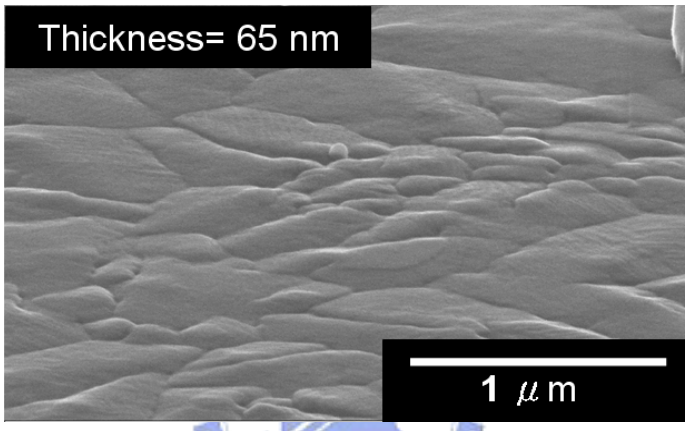


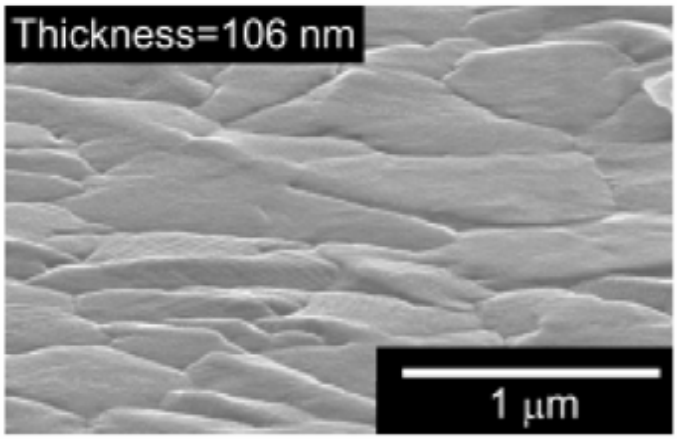
Fig. 2.10 (a) Schematic plot of cross section of inverted-staggered (top contact) device geometry (b) The corresponding cross section SEM image.



(a)



(b)



(c)

Fig. 2.11 The top view SEM images of pentacene film with thickness of (a) very thin, (b) 65 nm, and (c) 106 nm, respectively, in the channel region.

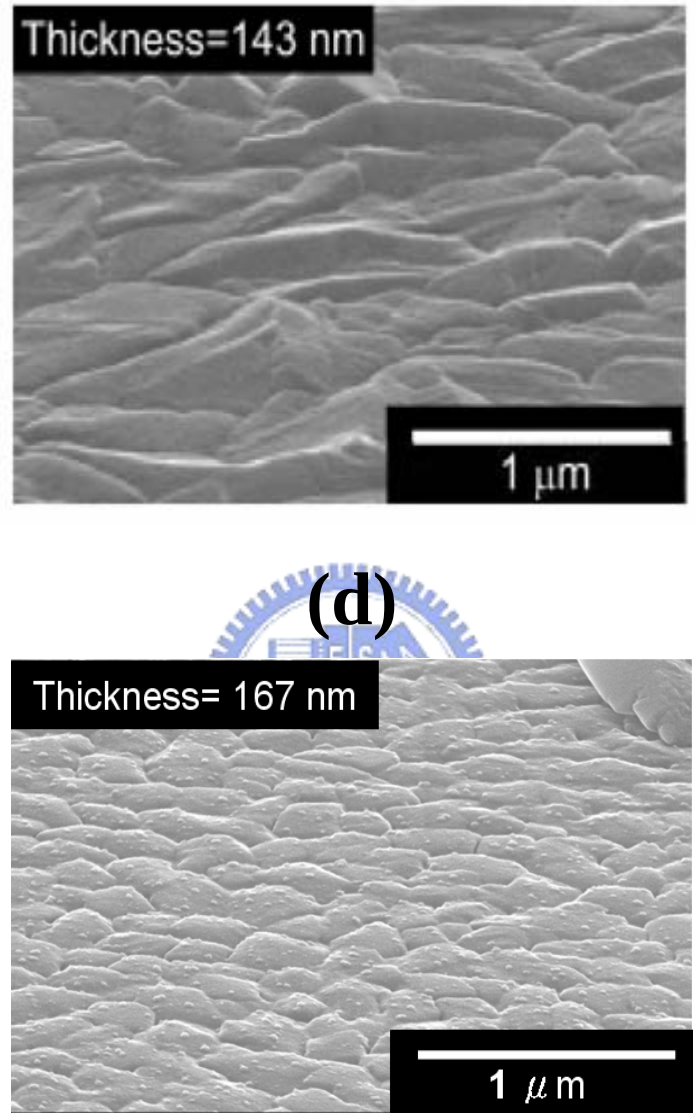


Fig. 2.11 The top view SEM images of pentacene film with thickness of (d)143 nm and (e)167 nm, respectively, in the channel region.

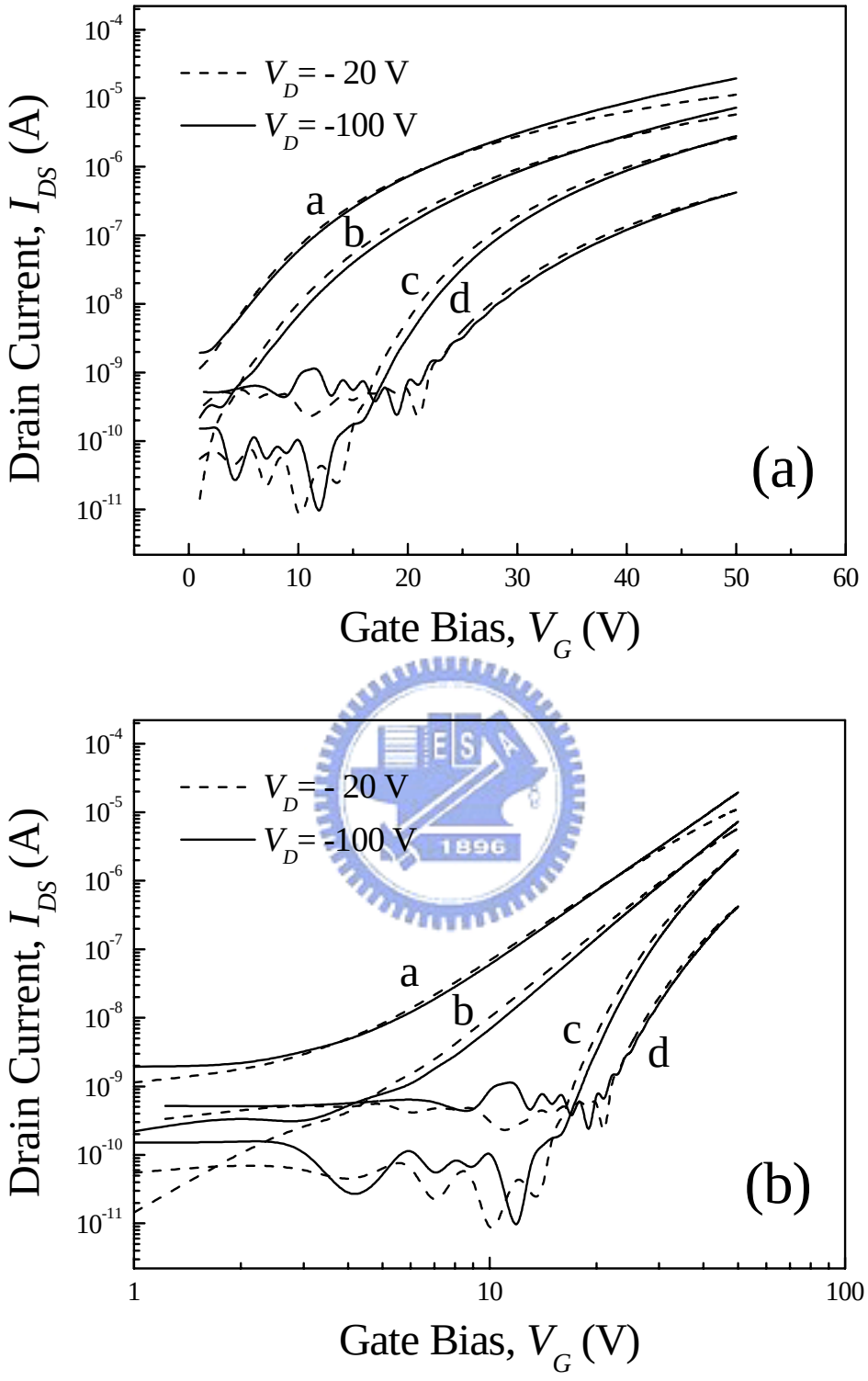


Fig. 2.12 Transfer characteristics in (a) log scale and (b) double-log scale of four pentacene TFTs with different thickness: a-65 nm; b-106 nm; c-143 nm; d-167 nm.

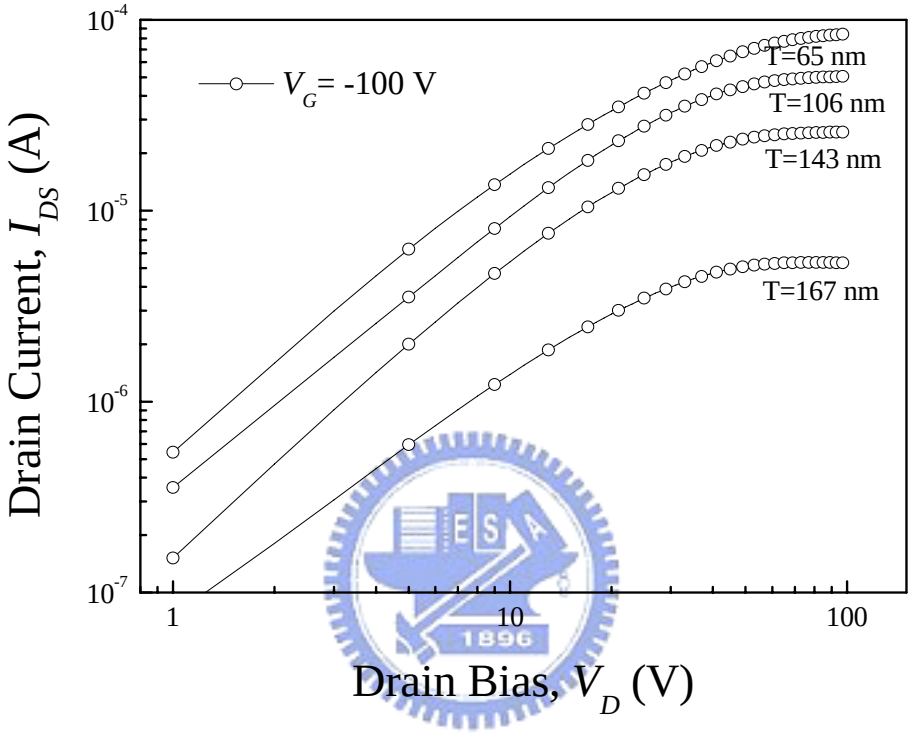


Fig. 2.13 Output characteristics in double-log scale at V_G = -100V for the four pentacene TFTs with different thickness.

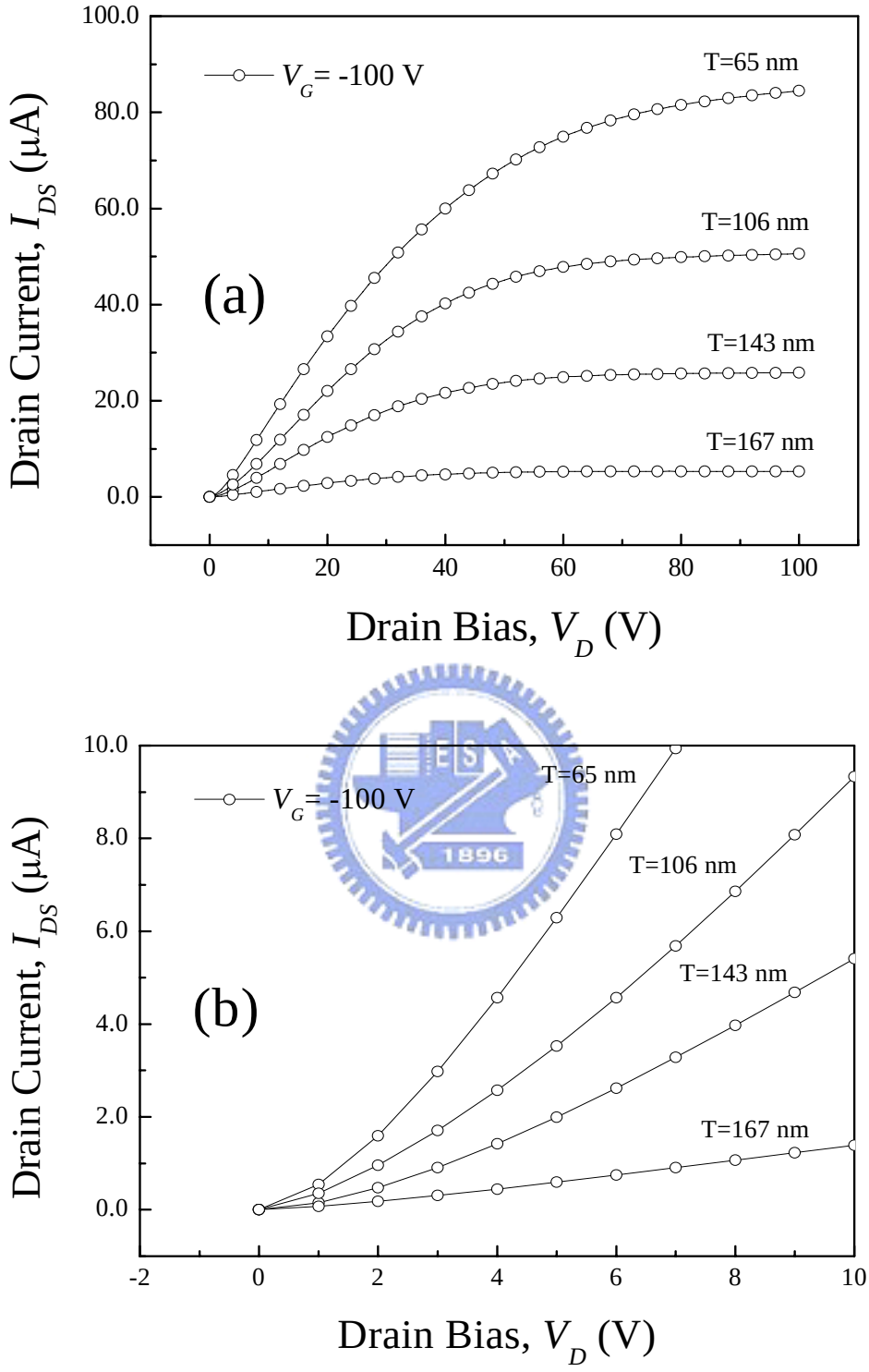


Fig. 2.14 (a) Output characteristics in linear scale at V_G = -100V for the four pentacene TFTs with different thickness. (b) Enlargement of (a) at small drain bias.

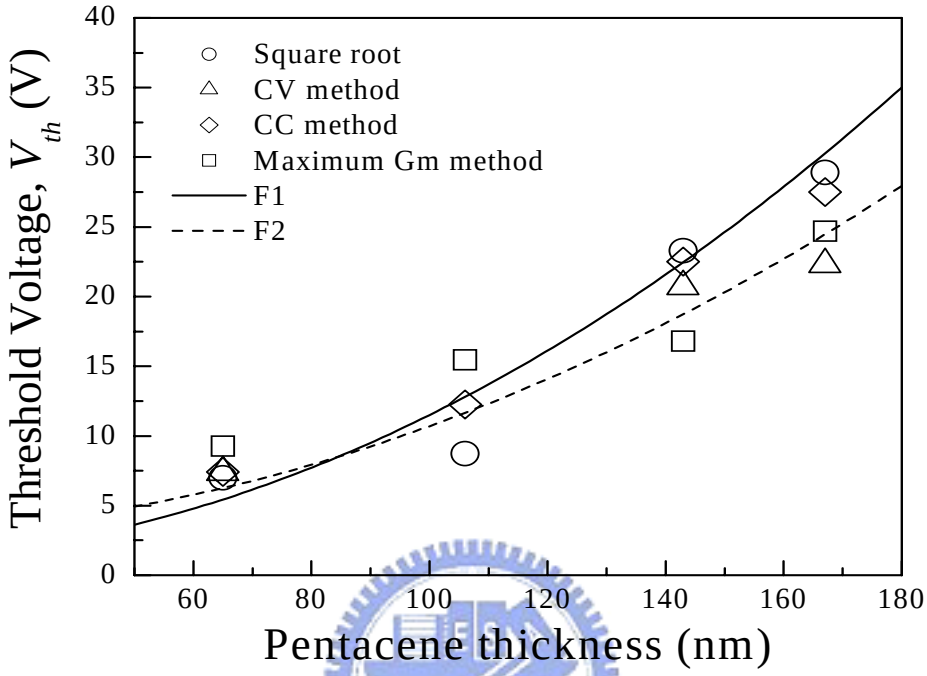


Fig. 2.15 The threshold voltage as a function of thickness of pentacene layer. The threshold voltage was extracted by various methods. Lines are the numerical fits based on Eq. (2.3). Solid line and dashed line are fits for threshold voltage measured by square root method and CV method, respectively.