Chapter 3
Atmosphere Effect on Pentacene Thin Film Transistors

3.1 Introduction

Recently, organic semiconductor materials have been shown to include some of the most popular candidate materials for fabricating of thin film transistors (TFTs) and several electronic and optoelectronic devices. Pentacene, a fused-ring polycyclic aromatic hydrocarbon, is a very promising material for making organic TFTs. Its field-effect mobility of above 1.0 cm^2/Vs and its on/off ratio of above 10^8 have been reported [89,90]. These values are similar to those obtained for amorphous silicon TFTs. However, the intrinsic transport mechanism of organic TFTs is not clear yet. Moreover, organic films are very sensitive to the environment and are unstable in air [24,53,54,55]. Necliudov et al. [56,57] examined the instabilities of the electrical characteristics and the 1/f noise behaviors of pentacene transistors. They reported that atmospheric moisture causes pentacene TFT degradation. Brown et al. [24] found that the organic transistors in air exhibit stronger hysteresis than those in a vacuum. Organic transistors in air have higher off currents because the oxygen dopant [24,58] and/or moisture interact with organic films [59,60]. Recently, Zhu et al. [53] presented humidity sensors that use pentacene transistors. Clearly, contact with compounds in air affects the transport characteristics of organic films.

In this chapter, we consider the electric properties of polycrystalline pentacene TFTs with gold top contacts and Indium Tin Oxide (ITO) bottom contacts. The devices were measured in air and in a high vacuum, respectively. In section 3.4.1~3.4.3, the study focused on the inverted staggered type TFT. The field-effect mobilities at various gate

voltages and drain voltages were examined. The grain boundary potential barrier model was applied to investigate carrier transport in pentacene TFTs. In section 3.4.4, the same method of analysis was applied to the inverted coplanar type TFT. Finally, a short conclusion was given.

3.2 Experiment

Both of the inverted staggered pentacene TFT utilizing gold as source/drain electrodes (TC, top contact) and inverted coplanar pentacene TFT using ITO as electrodes (BC, bottom contact) were used in this chapter. The schematic plots were shown in Fig. 3.1(a)(b). The detail process description was described in Chapter 2. The pentacene film morphology was characterized using a Seiko Instruments, Inc. SPA-500 scanning probe microscope with DF20 tip and operated in non contact mode at 1Hz scan rate. The pentacene thickness of each device was about 65 nm. The width and length of the defined channel were 1000 μm and 100 μm in the TC TFT, respectively. In the BC TFT, the channel width and channel length were 500 μm and 40 μm, respectively.

An HP 4155A Precision Semiconductor Parameter Analyzer was used to measure the electrical characteristics of the organic TFTs. The organic TFTs were first characterized in air and then in a vacuum chamber. The measurement equipment was schematic plotted in Fig. 3.2. The pentacene active layer was patterned using a shadow mask around the measured organic TFTs to minimize the drain current leakage. Fig. 3.1(c)(d) shows atomic force microscope of the topology of the pentacene film. The deposited film consisted of homogeneous grains with a mean diameter of around 0.5~1.5 μm in TC TFT and 0.2~0.4 μm in BC TFT, respectively.

3.3 Grain Boundary Potential Barrier Model

The grain boundary potential barrier model is proposed to explain the carrier transport in polycrystalline semiconductor. The theory divides the material into high (the crystal grains) and low (the grain boundaries) conductivities regions. The two regions are connected in series, therefore the effective mobility, μ, is given by the harmonic mean of the mobility in each region as,

$$\frac{1}{\mu} = \frac{1}{\mu_g} + \frac{1}{\mu_b} \tag{3.1}$$

Here, μ_g and μ_b are the mobility in grains and grain boundaries, respectively. If all the defects are located in the grain boundaries and $\mu_g >> \mu_b$, thus the overall mobility nearly equals to that in the grain boundaries. Assuming, a back-to-back Schottky barrier forms at the intergrain region due to the presence of monoenergetic defect states in grain boundaries and the carrier transport is limited by thermionic emission of the barrier. The energy scheme may present two limiting cases, as in Fig. 3.3. One is the partial depleted case that grain size, L, is larger than the depletion region, W_d, and another is the fully depleted case, $L < W_d$. The energy barrier therefore could be estimated by solving the Poisson's equation and given as

$$E_b = \frac{qN_t^{\,2}}{8\varepsilon_s N} \qquad \text{if} \quad N_t < LN \tag{3.2}$$

for the partial depleted case and

$$E_b = \frac{qL^2 N}{8\varepsilon_s} \qquad \text{if} \quad N_t > LN \tag{3.3}$$

for the fully depleted case. Here N_t is the trap density in the grain boundaries. In the fully depleted case, the conductivity is low due to the lack of carriers which are all trapped and it behaves as if the localized states are uniformly distributed over the film. Whereas increasing the doping concentration, N, for the partial depleted case the conductivity increases rapidly due to both the increase of free carriers and decrease of barrier height. The conductivity by thermioinc emission above the barrier height can be described as

$$\sigma = qN\mu_0 \exp(\frac{-E_b}{kT}) \tag{3.4}$$

Where $\mu_0=qLv_c/kT$. The k is Boltzmann constant, T is temperature and v_c is a thermal collection velocity. In generally case, the total resistivity, ρ, is a sum of the grains ρ_g and the grain boundaries ρ_b.

$$\rho = \rho_g + \rho_b = \frac{1}{q\mu_g N} + \frac{1}{qN\mu_b \exp(-E_b/kT)} \tag{3.5}$$

Hence the overall effective mobility is defined.

$$\frac{1}{\mu} = \frac{1}{\mu_g} + \frac{1}{\mu_b \exp(-E_b/kT)} \tag{3.6}$$

Usually if the $\mu_g >> \mu_b$, the effective mobility would be close to μ_b. For a thin film transistor with the consideration of gate bias effect on the channel carrier density and energy barrier E_b, the current at low drain bias can be written as

$$I_{DS} = W\mu_b C_i V_G \frac{V_D}{L} \exp(-\frac{qE_b}{kT}) = W\mu_b C_i V_G \frac{V_D}{L} \exp(\frac{-q^3 N_t^2 h}{8\varepsilon_s kTC_i V_G}) \tag{3.7}$$

The effective mobility hence can be presented as

$$\mu = \mu_b \exp(\frac{-q^3 N_t^2 h}{8\varepsilon_s kTC_i V_G}) \tag{3.8}$$

This means the field effect mobility is gate bias dependent and the grain boundary trap density can be extracted. The model was proposed by Levincen et al. [91] and modified by many other researches. Such as Horowitz [92] and Verlakk [55] used and modified this model to describe the carrier transport in organic thin film transistors.

3.4 Result and Discussion

3.4.1 Atmosphere Effect on Top Contact Configuration

The effects of the measuring conditions on the performance of the device in air and in a vacuum are investigated. Fig. 3.4 indicates that the output characteristics of a TC

pentacene transistor at various values of gate voltage (V_G). Measurements were made firstly in air and then in a vacuum at 10^{-6} torr. The output current of a TC pentacene transistor in a high vacuum is clearly larger than that in air. The magnitude of the maximum saturation in a vacuum is nearly four times that in air.

At low drain voltage (V_D), the drain current (I_{DS}) increases linearly with V_D (linear regime) and is approximately given by using the following equation:

$$I_{DS} = \frac{W\mu C_i}{L}(V_G - V_{th} - \frac{1}{2}V_D)V_D \quad (3.9)$$

where W and L represent the width and length of the channel, respectively; C_i is the capacitance per unit area of the insulating layer; V_{th} is the threshold voltage, and μ is the field-effect mobility, which can be calculated in the linear regime from the transconductance, using,

$$g_m = \frac{\partial I_{DS}}{\partial I_V}\Big|_{V_D=const} = \frac{WC_i}{L}\mu V_D \quad (3.10)$$

For $-V_D > -(V_G - V_{th})$, I_{DS} tends to saturate (in the saturation regime) because of the pinch-off of the accumulation layer, and is given by the equation,

$$I_{D,sat} = \frac{W\mu_{sat}C_i}{2L}(V_G - V_{th})^2 \quad (3.11)$$

In the saturation regime, μ_{sat} can be calculated from the slope of the plot of $I_{DS}^{1/2}$ against V_G.

Fig. 3.5 plots the I_{DS}-V_G and $I_{DS}^{1/2}$-V_G characteristics of a TC pentacene transistor at a V_D of -100 V. In a high vacuum, the off-current of the TC pentacene transistor is lower and the on-current is higher than those in air. Eq. (3.11) yielded a field-effect mobility of the pentacene transistor as high as 0.43 cm^2/Vs in a high vacuum. The modulated on/off ratio is 10^6; the threshold voltage is -7.26 V and subthreshold slope is 1.7 V/decade. However, the device in air performed poorly, exhibited a field-effect mobility of around 0.11 cm^2/Vs, an on/off ratio of near 10^5, a threshold voltage of -20 V and a subthreshold slope of 5

V/decade. The high vacuum environment markedly improves the performance of the pentacene transistor. Clearly, the charge transport characteristics of pentacene depend strongly on sensitive to the environmental conditions. The obtained results agree with those presented elsewhere [24,53-56].

In ambient air, the polar molecules H_2O, O_2, and CO_2 could easily diffuse into the organic film [53]. The channel conductivity of the film will be affected by dopants [91], as was verified in the off state. Subsidiary experiments were conducted in which the device was exposed to dry air to demonstrate that the H_2O molecules of air were responsible for the large leakage current. The leakage current in dry air was found to be close to that in a vacuum, indicating that moisture is the main cause of the leakage current. This finding may be explained by the fact that H_2O molecules interact with pentacene film to generate some dissociated species, resulting in ionic conductivity characteristics [59,60]. Apparently, the process is reversible and can be removed in a vacuum or dry air. However, the polar molecules may form extra traps at the grain boundaries, as well be considered below.

3.4.2 Atmosphere Effect on Field Effect Mobility

The dependence of mobility on gate voltage in various environments is also studied. The dependence of mobility on gate voltage has been reported for most organic TFTs [24,48,93,94]. Eqs. (3.9) and (3.11), applicable to the linear ($V_G - V_{th} < V_D$) and saturation ($V_G - V_{th} > V_D$) regimes, respectively, yield the field-effect mobility as a function of -($V_G - V_{th}$), which is plotted in Fig. 3.6. At a low drain voltage (-2 V), the mobility of the device in a vacuum is slightly better than that in air. The fall in the mobility with increasing gate voltage is attributable the presence of a contact barrier of pentacene transistors with gold contacts [95-97]. Such a fall in the mobility with increasing V_G has also been observed in the oligothiophene transistor [93]. However, the mobility measured in air gradually

approaches that measured in a vacuum as the negative gate voltage increases. At low gate voltage, most accumulated holes are probably trapped at the grain boundaries and the polar molecules, such as H_2O molecules in air interact with the trapped carriers [53], limiting the charge transport. At a high gate voltage, however, the concentration of accumulated holes is very high throughout the channel region and the traps at the grain boundaries are probably filled. Thus, the mobility of the transistor in air differs only slightly from that in a vacuum.

At large V_D (-20 V and -100 V), the mobility of the devices increases with V_G in a vacuum and in air. Such a quasilinear increase in the mobility with gate bias has also been observed for pentacene transistors [48,95], oligothiophene transistors [90], and, slightly differently, for α-Si transistors [98]. At a V_D of -20 V, the mobility of the transistor measured in a vacuum is highly than that measured in air. One possible explanation is that the traps limit charge transport when the pentacene film is exposed to ambient air. However, at a V_D of -100 V, the mobility of device in air exhibits a marked increase at $-(V_G - V_{th}) < 40$ V , to a value near that of device in vacuo at $-(V_G - V_{th}) > 40$ V. At a higher drain voltage (-100 V) and a higher gate voltage, the charge density in the channel is relatively uniform and the current increases linearly until it saturates. This phenomenon may explain the fact that the mobility of transistor in air is almost the same as that in a vacuum at high $-(V_G - V_{th})$.

As the drain electric field is increased, the carriers are accelerated and their drift velocity increases. This work addresses the dependence of the mobility on the drain electric field in the pentacene transistor in air and in a vacuum. Eq. (3.9) yields the mobility as a function of V_D. Fig. 3.7 plots field-effect mobility versus V_D for various V_G in a vacuum. The mobility at low drain bias increases linearly with the drain bias and eventually saturates at large drain biases. In air, the device exhibits similar behavior but lower mobility at a given drain electric field. Fig. 3.8 plots the drift velocity, $v = \mu(E)E$, of the

holes, as a function of the drain electric field at a V_G of -100 V. In a vacuum, the drift velocity increases linearly with the strength of the electrical field, similar to the carriers in silicon in a low electric field [99]. No high-field saturation of drift velocity was observed over the measurements range considered herein. The drift velocity of the transistor in air was less than that in a vacuum; the drift velocity-electric field characteristics deviate from linearity in a high drain electric field, as shown in Fig. 3.8. Clearly, the device in air exhibits charge trapping that reduces the drift velocity of the holes.

3.4.3 Trap Density Extracted by Levinson Model

Thermally evaporated organic materials of interest herein - pentacene and oligothiophene - are polycrystalline and have large grains. Increasing the grain size has been demonstrated to improve the mobility of polycrystalline pentacene [100] and other polycrystalline organic materials [92]. The grain-boundary potential barrier model is extensively applied to understand carrier transport in such materials. The model assumes that carriers are transported at inter-polygrains by thermionic emission. The concept of grain-boundary potential barriers can be applied to polycrystalline silicon and polycrystalline CdSe [91]. The trap density, N_t, can be determined from a Levinson plot of $\ln[I_{DS}/V_D]$ against $1/V_G$. The Levinson model is based on the predicted transistor drain current in the linear regime, given by

$$I_D = \mu_0 V_{DS} C_i \left(\frac{W}{L}\right) V_G \exp\left(-\frac{E_B}{kT}\right) \tag{3.12}$$

$$\equiv \mu_0 V_{DS} C_i \left(\frac{W}{L}\right) V_G \exp\left(-\frac{s}{V_G}\right) \tag{3.13}$$

where E_B is the potential barrier height; μ_0 is the trap-free mobility, and the thermally activated mobility is given by

$$\mu = \mu_0 \exp\left(-\frac{E_B}{kT}\right) \equiv \mu_0 \exp\left(-\frac{s}{V_G}\right) \tag{3.14}$$

Screening causes E_B to fall as V_G increases [91]. Hence, N_t can be estimated from the slope, s, of the Levinson plot using the formula,

$$S = \frac{-q^3 N_t^{\,2} h}{8\varepsilon_s kTC_i} \tag{3.15}$$

where h represents the thickness of the semiconductor layer, and ε_s is the dielectric constant of the semiconductor. Additionally, E_B and μ_0 at constant V_G can be calculated using Eq. (3.14). Here, we take the ε_s of pentacene as 4 [87]. Fig. 3.9 presents a typical Levinson plot of $\ln[I_{DS}/V_D]$ against $1/V_G$ at V_D of -20 V. From the slope of this plot $N_t \sim 6.11\times10^{11}$ cm^{-2} and 4.89×10^{11} cm^{-2} are estimated for a pentacene transistor in air and in a vacuum, respectively. Then, Eq. (3.14) yields E_B = 29.3 meV and μ_0= 0.56 cm^2/Vs for a device in air at V_G = -100 V. In a vacuum, the lower E_B = 18.8 meV and higher μ_0=0.65 cm^2/Vs were obtained at V_G = -100 V. The values of N_t and E_B are in good agreement with the values in the literature [50,55]. The value of μ_0 is proportional to the mean velocity of the holes [93]. The holes in a high vacuum have a higher drift velocity than in air. The results are consistent with those in Fig. 3.8. Clearly, the pentacene film in air has a higher trap density and higher potential barrier height than in a vacuum. The lower saturation current and higher threshold voltage of the device measured in air ambient showed that the extent of charge trapping is high [101], as this fact was supported by the trap concentration and barrier height obtained from the Levinson plot. The fall in the saturation current [53] and the strong hysteresis [60] of transistors based on pentacene semiconductors when exposed to the moisture in air have already been reported. Zhu et al. also stated that H_2O molecules can easily diffuse into these gaps at the grain boundaries and interact with trapped carriers [53]. In this chapter, devices were first exposed to air and then placed in a vacuum. They performed better when in a vacuum.

Additionally, the saturation current quickly fell under gate bias stress when a device was in air ambient. Interestingly, the original saturation current was fully recovered when

the device was pumped in a vacuum chamber for many hours, showing clearly that the air-induced degradation in device performance is reversible.

3.4.1 Atmosphere Effect on Bottom Contact Configuration

In this section, we applied the same analysis method to inverted coplanar type TFT, BC ITO TFT. Fig. 3.10 demonstrated the output and transfer characteristics of a BC pentacene transistor measured in air and in a vacuum, respectively. In generally, the atmosphere effect on the BC pentacene transistor configuration reveals similar behaviors with that of a TC pentacene transistor configuration. The measurement result in a vacuum still performed better electrical properties than that in ambient air. Clearly, in Fig. 3.10(a)(b), the result measured in vacuum has larger on current than that in air. In specific descriptions, the field effect mobility of the value of 0.02 cm^2/vs in air has been improved to 0.11 cm^2/vs in vacuum. The threshold voltage value of -10.5 V in air shifted to -12.5 V in vacuum. The on/off ratio of the order of 10^5 in air has been improved to the order of 10^6 in vacuum. And the sub-threshold slope varied from 5.5 V/decade in air to 4 V/decade in vacuum. From above, we believed that the carrier transport in vacuum for a BC pentacene transistor has also been enhanced due to the lack of humidity. The detail mechanism was discussed aforementioned, the same as the TC pentacene transistor device.

In Fig. 3.11, we applied the grain boundary potential barrier model to the BC pentacene transistor. However, the result denoted an opposite phenomenon to the TC device. In the air, the $N_t \sim 2.9\times10^{11}$ cm^{-2} in air and $N_t \sim 4.8\times10^{11}$ cm^{-2} in vacuum were estimated. So as, the equivalent barrier heights of -4.07 meV in air and -11.25 meV in vacuum were calculated, respectively. The trap density in vacuum was larger than that in air, as well as the barrier height had the same result. The possible explanation was attributed the different configurations of TC device and BC device. They would be

discussed as following. The BC device using the ITO as source/drain electrodes has a larger injection barrier between ITO with pentacene than Au with pentacene of a TC device, since the work function of ITO, Au, and pentacene were 4.9 eV, 5.1 eV and 5.3 eV, respectively. The gold was supposed to form an ohmic contact with pentacene, thus in the TC device calculation, the junction barrier between source/drain with pentacene could be neglected. However, in BC device, the ITO was supposed to form a higher barrier junction between ITO with pentacene. That junction barrier may fall into the range between ohmic contact and schottky contact due to the large variation of ITO's work function, 4.9 eV~5.1 eV. In this case, it was near the schottky contact because the observation of the large non-linear regime in Fig. 3.10(a). The carrier injection of the schottky barrier junction was proven to vary with the applied gate bias. Nevertheless, the grain boundary potential barrier model only considered the mechanism of carrier transport in poly semiconductors, not the carrier injection of contact. Therefore, Eqs. (3.12) and (3.13) did not exclude the carrier injection behaviors. The exponential function may include the junction barrier height between ITO and pentacene. In Fig. 3.10(a), clearly, we noted the larger on current in air than that in vacuum at very small V_D regime. That means that the junction between ITO with pentacene has a smaller barrier height in air than that in vacuum. That may be explained in sec 3.4.1. The humidity induced the increase of conductivity of pentacene, and generated some trap states that may reduce the barrier between ITO with pentacene in some ways. Form the inference, the combination effect of ITO/junction and grain boundary barrier, the estimated trap density and the barrier height in air may smaller than those in vacuum.

To further consider, the AFM result showed that the size of poly grain in BC device was smaller than that in TC device. The carrier transport in this case may be much closer to the case of amorphous type semiconductor or the fully depleted case of grain boundary potential barrier model. No matter the former or the latter, the behaviors of the mobility

dependence on gate bias was restricted and reduced. In Fig. 3.10(b), the square root of drain current in air showed that no gate dependent mobility was observed, even more the mobility degraded in high gate bias regime. Therefore, the humidity not only increased the trap density in grain boundaries but also affected the carrier transport in poly grains. In small poly grain case, the humidity even suppressed the carrier transport at high bias regime and deduced the violation of grain boundary potential barrier model. But, in another case [102], the BC pentacene transistor demonstrated almost the same behavior with TC pentacene transistor when the grain boundary potential barrier model was applied. In that case, the ITO formed a better ohmic contact with pentacene than this sample. And the extracted trap density in air was higher than that in vacuum.

To sum up briefly, the atmosphere effect on BC ITO TFT was investigated. The humidity also degraded the device properties. However, the grain boundary potential barrier model needs more carefully modification when it is applied to the BC pentacene transistor. The contact effect between ITO with pentacene should be included.

3.5 Conclusion

The electrical properties of the polycrystalline pentacene transistor in air and in a vacuum were studied. The pentacene transistor measured in a high vacuum had greater field-effect mobility, a higher modulated on/off current ratio, a lower threshold voltage, and a better sub-threshold slope than that in air. The poor performance of the device in air follows from the more extensive trapping of carriers in air ambient and the consequent limiting of the charge transport of pentacene transistor. The grain-boundary potential barrier model estimates the potential barrier height and the trap density at the grain boundaries. The model is used to elucidate charge transport in a pentacene transistor under various atmospheric conditions. Moreover, the proposed model offers a satisfactory

explanation of the improved performance of pentacene transistors in a high vacuum and facilitates an understanding of the difference between air and vacuum environments in this regard. However, to further consider the grain boundary potential barrier model in different TFT configurations, this model needs more carefully modification because the different injection barriers between ITO, gold with pentacene, respectively.

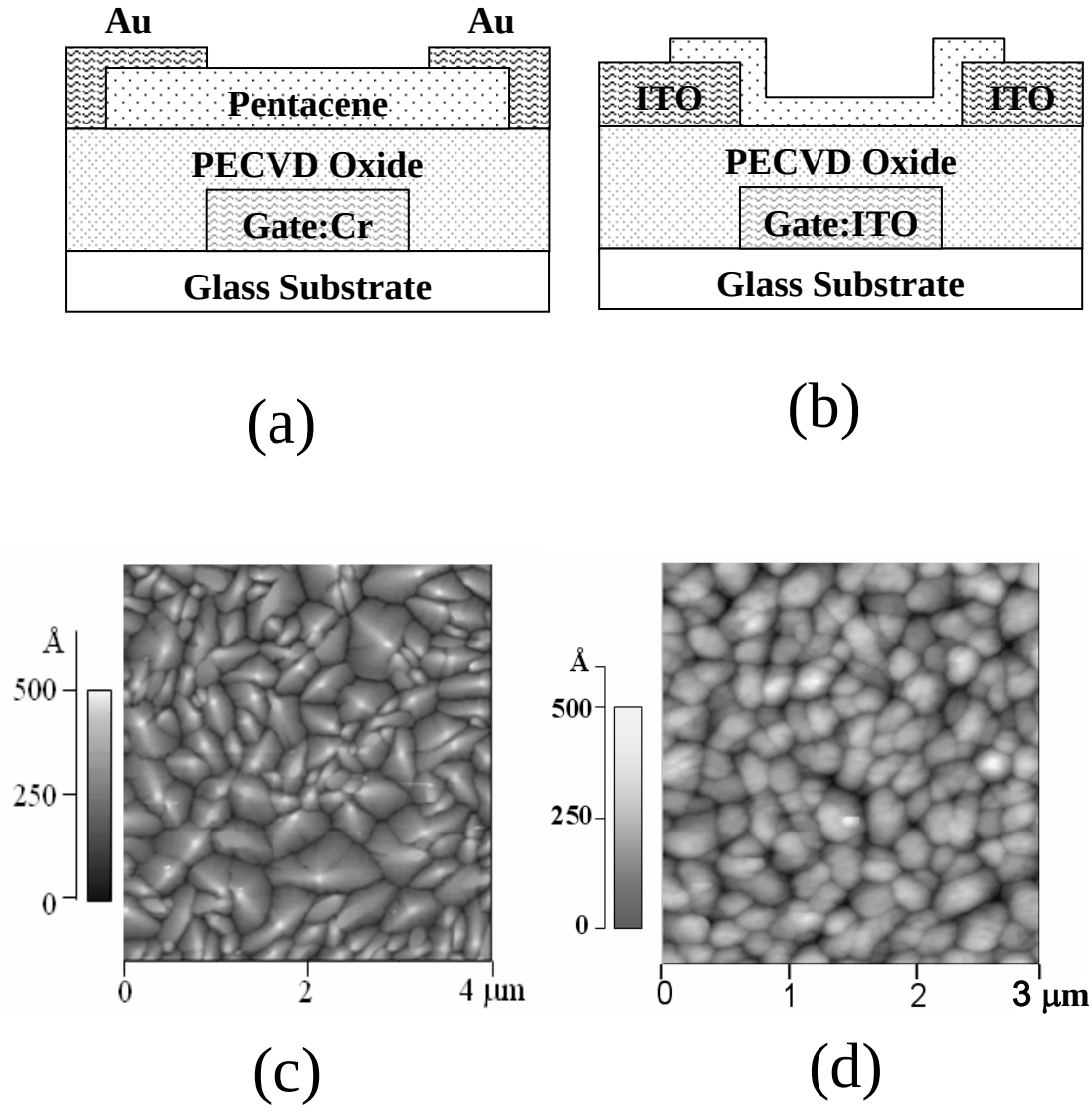

Fig. 3.1. Schematic diagram of (a) an inverted staggered pentacene transistor with gold top contact (TC TFT), (b) an inverted coplanar pentacene transistor with ITO bottom contact (BC TFT), (c) atomic force microscope image of thermally deposited pentacene film on SiO_2 surface in TC TFT, (d) pentacene film in BC TFT..

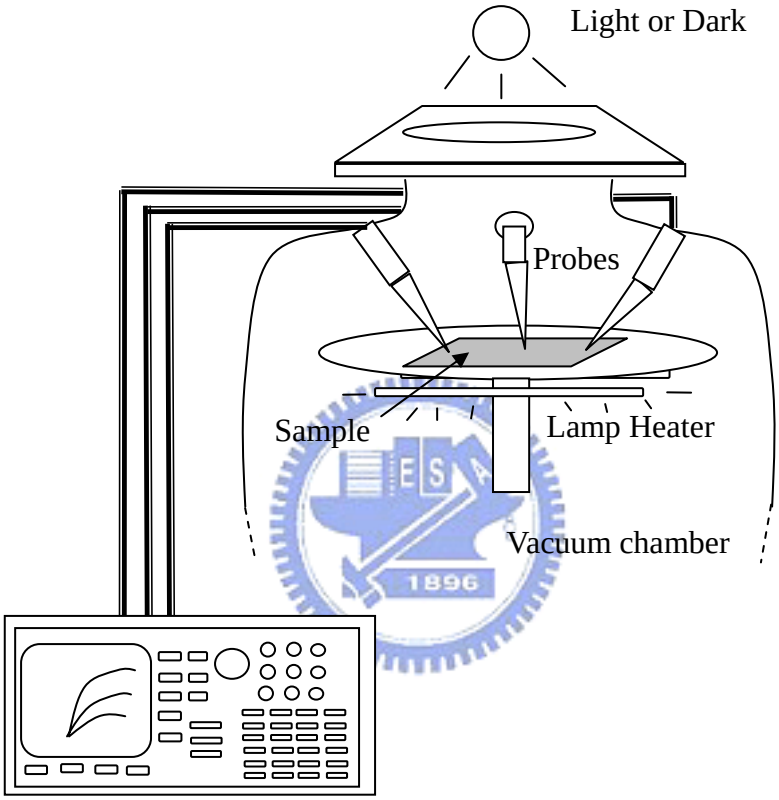

Fig. 3.2 The Vacuum Measurement System.

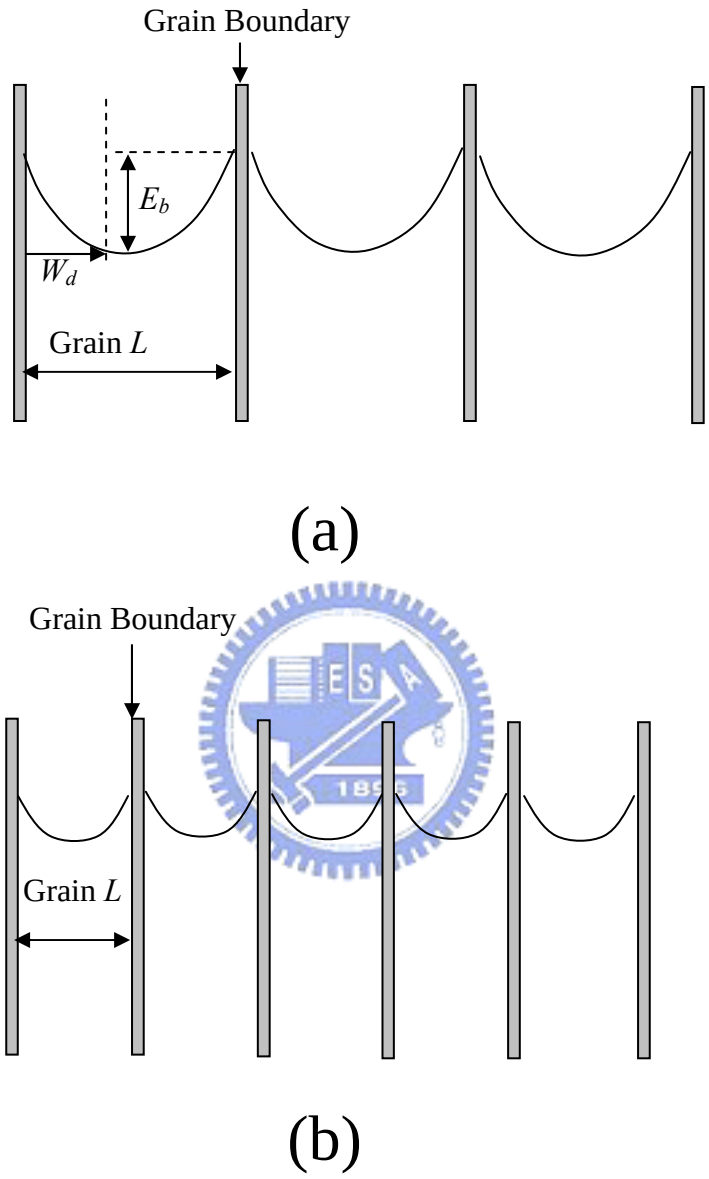

Fig 3.3 Energy scheme of two cases of polycrystalline semiconductors, (a) The grain length, L, larger than twice depleted length, W_d, as $L>2\ W_d$. (b) $L< W_d$. E_b is the energy barrier height.

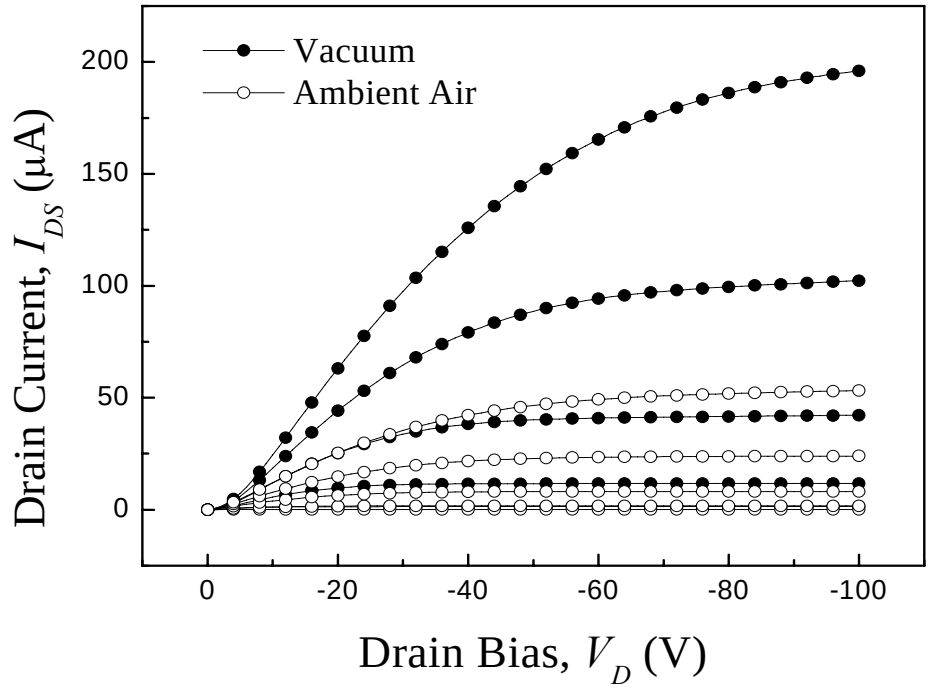

Fig. 3.4. I_{DS}-V_D characteristics of a TC pentacene transistor measured in air and in a vacuum. The V_G was varied from -20 V to -100 V with -20 V step.

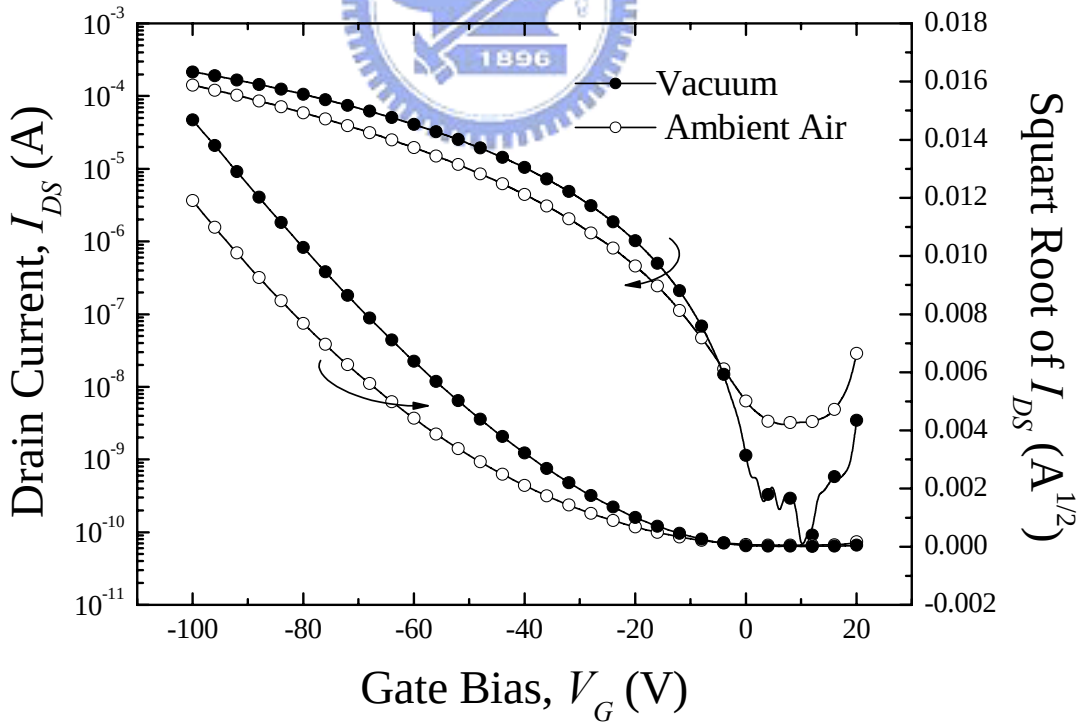

Fig. 3.5 Log(I_{DS})-V_G(left-axis) and $(I_{DS})^{1/2}$-V_G(right axis) characteristics of a TC pentacene transistors measured in air and in a vacuum with a V_D of -100 V.

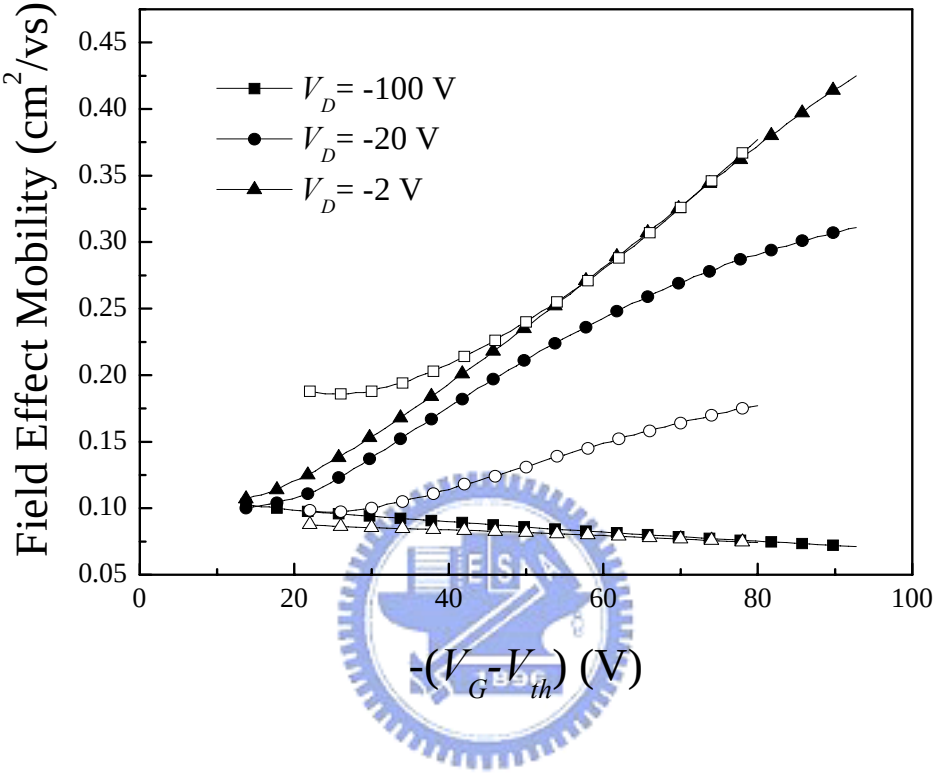

Fig. 3.6 Variation of the field-effect motilities of a TC pentacene transistor as a function of $-(V_G-V_{th})$. Opened and closed symbols correspond to the data measured in air and in a vacuum, respectively.

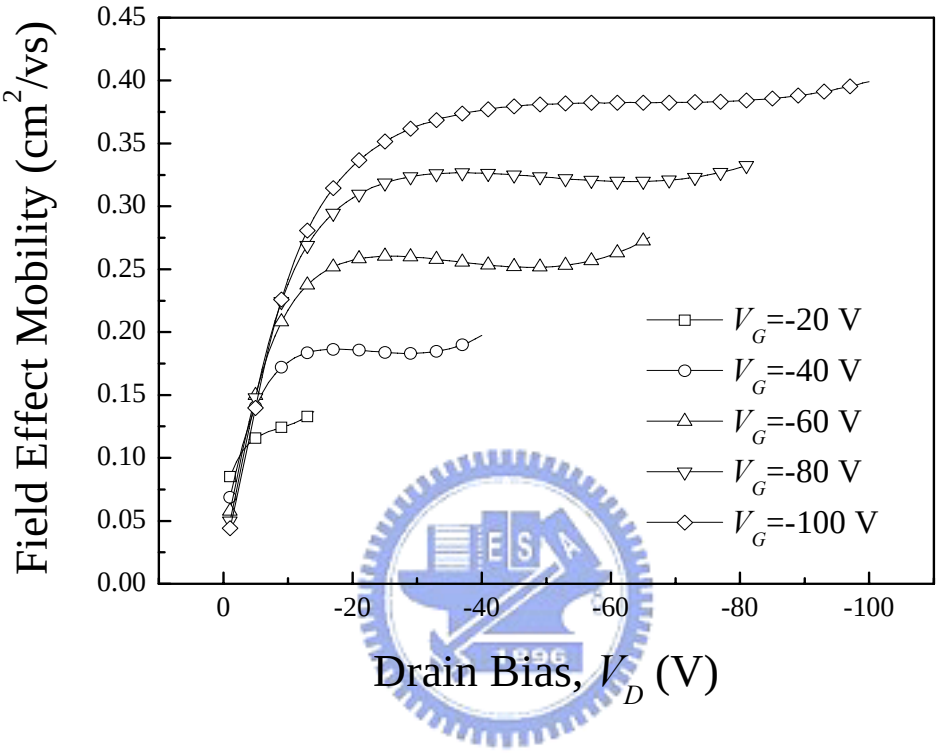

Fig. 3.7 Variation of the field-effect motilities of a TC pentacene transistor measured in a vacuum as a function of V_D for V_G = -100 V, -80 V, -60 V, -40 V and -20 V.

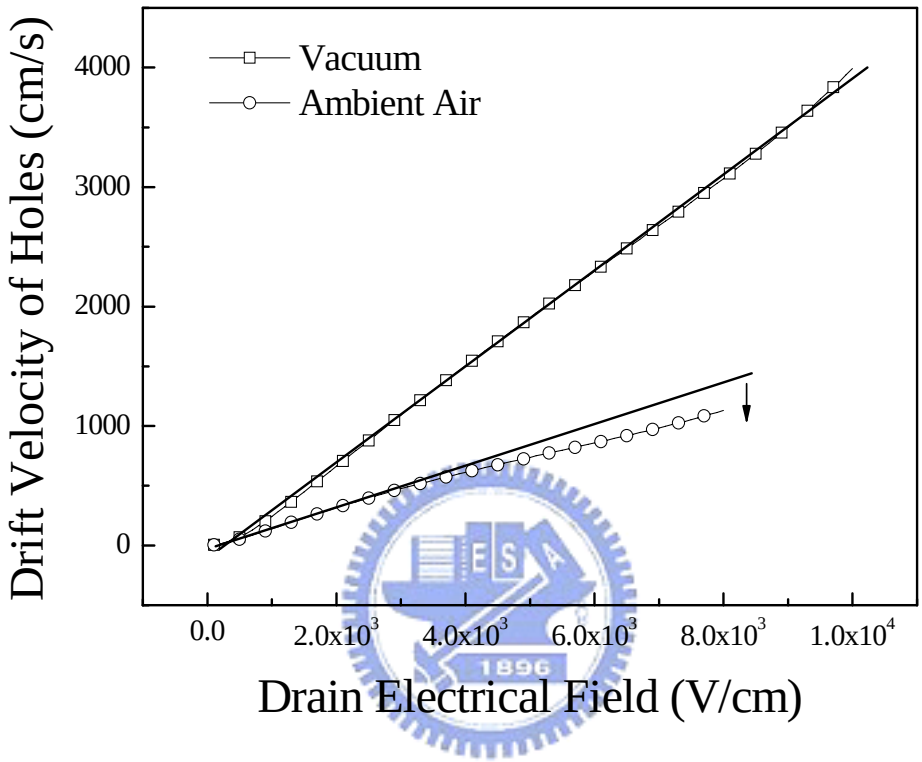

Fig. 3.8 The drain electric field dependence of the drift velocity of holes in TC pentacene transistor with a V_G of -100 V. The transistor was measured in air and then in a vacuum. The straight lines act as the reference.

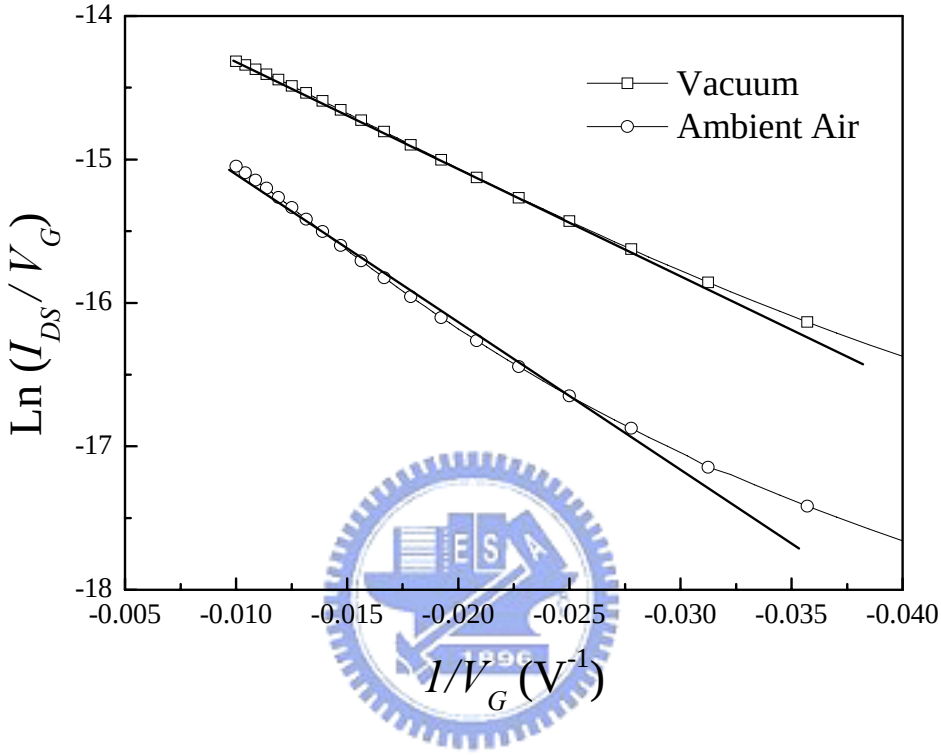

Fig. 3.9 Plot of ln(I_{DS}/V_G) versus (1/V_G) for a TC pentacene transistor measured in air and in a vacuum with a V_D of -20 V.

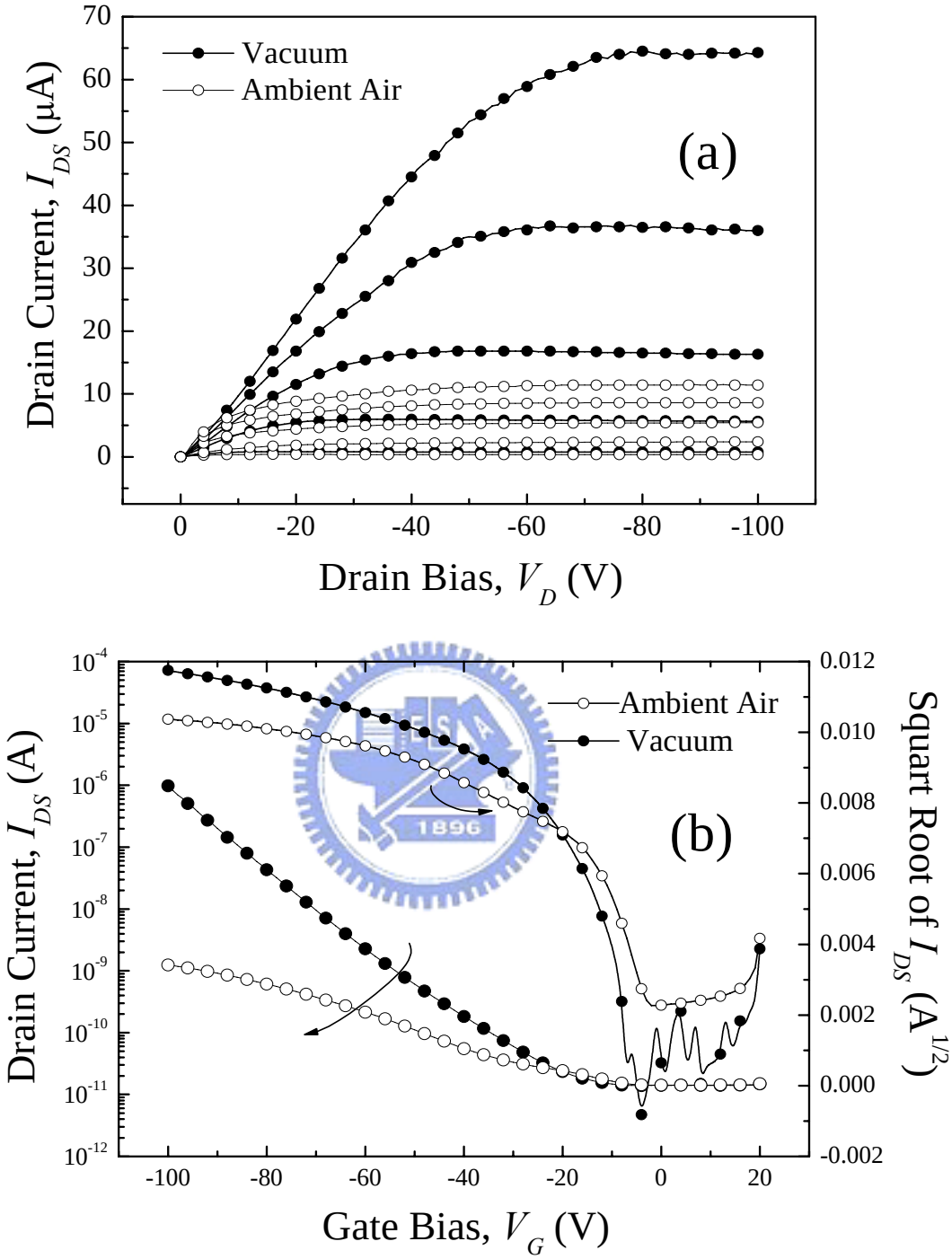

Fig. 3.10 (a) I_{DS}-V_D characteristics of a BC pentacene transistor measured in air and in a vacuum. The V_G was varied from -20 V to -100 V with -20 V step. (b) Log(I_{DS})-V_G(left-axis) and $(I_{DS})^{1/2}$-V_G(right axis) characteristics of a BC pentacene transistors measured in air and in a vacuum with a V_D of -80 V.

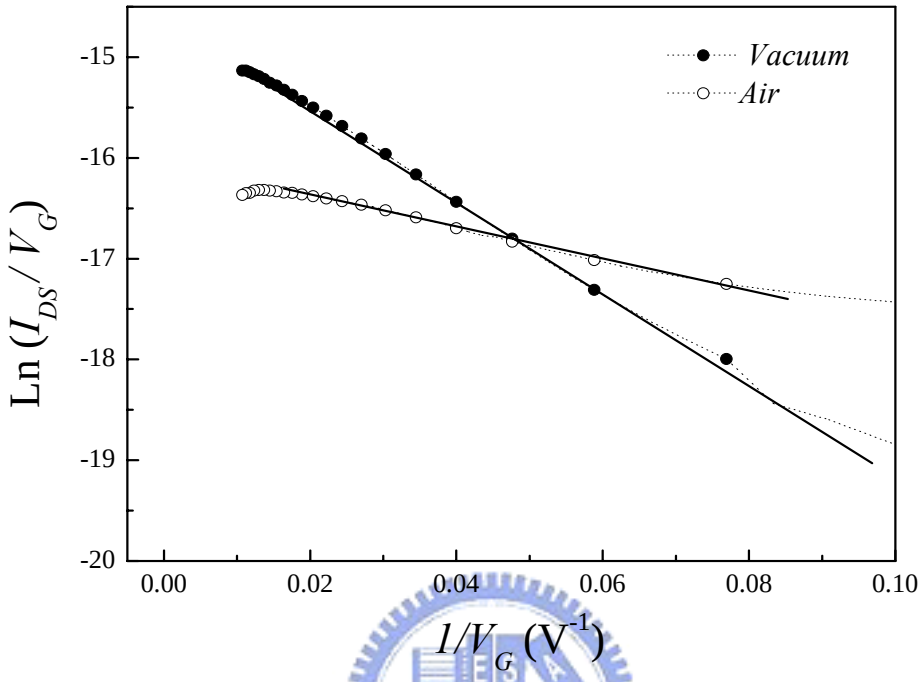

Fig. 3.11 Plot of ln(I_{DS}/V_G) versus (1/V_G) for a BC pentacene transistor measured in air and in a vacuum with a V_D of -20 V.