Chapter 4
The Driving of Liquid Crystal Display by Pentacene Thin Film Transistors

4.1 Introduction

Organic thin film transistors (TFTs) have attracted much attention over the last decade. They can be used in large scale electronic displays, radio frequency identification tags [5], smart cards, microelectronics [6-10] or sensors [11]. Among various organic semiconductors, pentacene, a fused ring polycyclic aromatic hydrocarbon, has exhibited a high field-effect mobility of above 1.0 cm^2/Vs and is considered to be the preferred candidate for replacing amorphous silicon thin film transistors [26,103]. Pentacene, a small-molecule organic compound, can be processed by thermal evaporation or vapor deposition. Other organic semiconductors, the long chain polymers, such as regioregular poly(3-hexylthiophene) [12-14] and poly(9,9'-dioctyfluorene-*co*-2,2'-bi-thiophene) [15,16], have less favorable characteristics than pentacene. However, they can be fabricated in solution processes, such as by spin coating, ink-jet printing [104] or contact printing. Hence, they can be fabricated at low cost by using a roll-to-roll process – even less than 10 % of the cost of fabricating traditional TFTs. Organic TFTs can be fabricated at low temperature and are highly compatible with a flexible/plastic substrate. These facts make it a promising candidate for the next generation of TFT technology.

In active matrix liquid crystal displays (AM-LCDs), for instance, organic TFTs allow the use of inexpensive, light-weight and mechanically rugged plastic substrates as alternatives to glass. Prototype AM-LCDs, each pixel of which is driven by pentacene transistors [61] have been recently demonstrated. A polymer pixel engine has also been

developed [62,63], indicating the potential of organic transistor technology for use in display applications. However, the high operation voltage and photosensitivity of organic TFTs restrict the display type. Thus, most investigations on the use of organic TFTs to drive AM-LCDs, focus on reflective displays, such as the polymer dispersed liquid crystal or electronic-ink displays [64]. These types of displays are suitable for operation at high voltage.

This chapter addresses the factors that affect the driving of a twist nematic liquid crystal (TNLC) display by pentacene transistors with a backlight system. The electronic stability of pentacene transistors is an important factor, regardless of the application. Environmental factors, including the sensitivity to moisture and to illumination of pentacene transistors were studied. An extra protective layer was added on to the pentacene transistors to isolate them from the atmosphere and prevent damage from the subsequent TNLC process. The gate bias stress and device uniformity were also studied. A 3 inch transparent TNLC display with 64 × 128 pixels was fabricated. It can show a black and white image with a contrast ratio similar to that of paper. Moreover, it can easily be fabricated as a color display using color filters.

4.2 Experiment

This study employs the standard inverted-coplanar TFT structure with a bottom-contact (BC) configuration: the organic semiconductor is deposited onto the gate insulator, the prefabricated source and the drain electrodes. The detail process was described in chapter 2. In this chapter, a finger-shaped source/drain electrode structure was adapted for testing devices. This kind of design could be treated as many transistors in parallel connection. That would suppress the variation of each single device. Fig. 4.1(a) depicts the device process flow.

Throughout the TNLC display process, the organic TFTs array (backplane) was processed as above. Then, a water-based encapsulation poly(vinyl alcohol) (PVA) layer of thickness 6000 Å was spin coated on it. A spin-coated and rubbed polyimide (PI) layer of thickness 1000 Å was formed to align the TNLC. The two layers also serve as the protection layer. The bottom plate was thus completed. Subsequently, the top plate was formed by fabricating a sputtered ITO layer of thickness 1500 Å as the common electrodes and then a spin-coated, rubbed polyimide TNLC alignment layer of thickness 1000 Å on a glass substrate. Finally, the two plates were assembled by a full sealing of the TNLC at 150 ℃. The process was shown in Fig. 4.1(b).

All the electrical characteristics were measured using a Hewlett-Packard 4155A Semiconductor Parameters Analyzer and a Keithley Model 237 High-Voltage Source-Measure Unit. The basic electrical characteristics and direct current (dc) stress were measured in normal air, in dry air and in a vacuum (10^{-6} torr).

4.3 Result and Discussion

4.3.1 Sensitivity to Humidity

Fig. 4.2 plots the influence of the measuring environment on the device performance of pentacene transistors with the bottom-contact configuration. In this bottom-contact device, the pentacene was deposited onto the gate insulator, the prefabricated ITO source/drain electrodes. In ambient air, the device performed poorly with a field-effect mobility (μ) of only 0.0181 cm^2/Vs, a threshold voltage (V_{th}) of -3.3 V, an on/off ratio of order 10^4 and a subthreshold slope (SS) of 5.4 V/decade. The electrical parameters were extracted by applying standard metal-oxide-semiconductor field-effect transistor (MOSFET) equations, which are described in an earlier work [105]. Then, the characteristics of the device were measured in dry air after it had been stored in dry air for 25 hours. The device exhibits better

performance with a μ of 0.0263 cm^2/Vs, a V_{th} of -3.3 V, an on/off ratio of 10^6 and an SS of 3.9 V/decade. The performance was near that of the device measured under vacuum conditions, the results for which were a μ of 0.0301 cm^2/Vs, a V_{th} of -6.4 V, an on/off ratio of 10^6 and an SS of 3.2 V/decade. Clearly, the pentacene transistors suffered from humidity/H_2O and so exhibited inferior performance, because the moisture that diffuses into the pentacene grain boundaries acts like a trap center and limits carrier transport. Similar phenomena were observed in another investigation by using a top-contact configuration with Au source/drain electrodes. [105,106]

4.3.2 Effect of Passivation Layer

In the normal AM-LCD, the LCD is built on top of the TFTs. The pentacene transistors failed when the LC solution was deposited onto it, although the pentacene molecule could not dissolve in common organic solvent. However, the solvent may change the pentacene grain states and grain boundaries states, modifying the device characteristics. Accordingly, when pentacene transistors were integrated into an LCD panel, an appropriate protection layer was required to prevent damage caused by the subsequent LC process and the humidity of the ambient air.

A protection layer was deposited onto the device to ensure that the pentacene transistors work correctly under TNLC; the “Experimental” section details this process. Fig. 4.3 plots the output curves of the pentacene transistors with and without a protective layer, as measured in ambient air. Adding the protective layer clearly enhanced the organic TFT characteristics. After the LC process, the organic TFT still outperformed the bare device. The results clearly revealed that the protective layer partially prevented the diffusion of moisture/H_2O, and fully isolated the TNLC from damage by organic solvent.

4.3.3 The Illumination Effect

Most organic semiconductor molecules are very photosensitive, resulting in marked leakage current in AM-LCD application due to the high backlight intensity. Therefore, the electrical characteristics of pentacene transistors were measured in the dark and under illumination in a vacuum chamber, as plotted in Fig. 4.4. The device was operated in the linear region and in the saturation region with drain-to-source voltages (V_D) of -10 V and -50 V, respectively. Under illumination, the extracted field-effect mobility and the modulated on/off ratio were very close to the values obtained in the dark. However, the threshold voltage of -3 V obtained in the dark shifted to a positive 14 V under illumination. Such a shift in the threshold voltage under illumination was also observed in other organic TFTs [107,108]. An almost unchanged on/off ratio of TFT was very important to the operation of AM-TN-LCDs with backlight illumination, since this guaranteed that the turn on/off states of each single pixel was clearly defined without disturbance or error. However, the shift of threshold voltage due to illumination must be compensated for by modulating the gate scan signal voltage, increasing the complex of the driving system.

4.3.4 The Uniformity in Local Substrate

The uniformity of organic TFTs is important to display applications. Fig. 4.5 depicts the pentacene transistors uniformly distributed in a 3 inch organic TFT array substrate. The on-current of the pentacene transistors was in the order of 10^{-6} A at a V_G and a V_D of -25 V and -20 V, respectively. The leakage current was in the order of 10^{-11} A at a V_G and a V_D of -5 V and -20 V, respectively. Hence, the modulated on/off ratio of each device was approximately of the order of 10^5. The threshold voltage was around -4 V, with a variation of ±1 V. This variation of threshold voltage and the modulated on/off ratio arises primarily from the distribution of non-uniform pentacene grains and unintentional doping [109]. The

organic TFT acts just as a switch to ensure that the external signal passes directly to the LC terminal to drive the TNLC. Accordingly, the variation in the threshold voltage very slightly influences the operation of the display and could be easily compensated for by modulating the driving signal.

4.3.5 Gate Bias Stress

Fig. 4.6 plots the drain current (I_{DS}) as a function of time under gate bias stress in ambient air and in a vacuum. The gate voltage and drain voltage were set to the same value of -50 V. The dependence of the drain current in ambient air on time is similar to that in a vacuum but with more rapid decay. Other studies [110,111] revealed that the decay of the on-current could be attributed to the trapping of charges in the channel near the oxide/pentacene interface. The trapped charges generate a built-in voltage that would make the threshold voltage of organic TFT more negative. Hence, for a given dc stress, the actual voltage bias, (V_G - V_{th}), that forms the conducting channel gradually becomes smaller with time, leading to on-current decay. This procedure was found to be reversible. By supporting a suitable positive gate voltage for a short period or by supporting an unbiased state for a long period, trapped carriers can be neutralized or self-recombined. Therefore, the pentacene transistors recovered its initial state. The on-current decay is strongly correlated with the number of initial possible traps and defect states in the pentacene layer. The trap density in vacuo was less evident than that in ambient air [105]. Thus, the longer lifetime in the vacuum was reasonable. In some cases, after a dc stress, the pentacene transistors never recovered. The dc stress bias may be too large to cause the gate insulator to undergo hard break down. The breakdown voltage of the TEOS oxide was near 2~3 MV/cm. Another well-known cause of the drop in lifetime, the hot carrier effect, which is evident in most MOSFETs, did not occur in organic TFTs, because of their low field effect mobility and

small electron momentum.

To further investigate the recovery of dc stress, the device was measured after stress and after supporting an unbiased state for a period. Fig. 4.7(a) shows the transfer curves of the origin state, after dc stress for 25 hrs, after an unbiased state for 1, 2, 3, 4, 5, 8, 20, and 45 hrs. Fig. 4.7(b) denotes the cases in Fig. 4.7(a) with a square root presentation of drain current. This result was interesting due to the recovery or even better performance after a long period unbiased state. A.R. Brown et al. had reported the mechanism of dc stress for organic semiconductors. It was more like a release behavior than a degradation one, the same as aforementioned. In Fig. 4.8, we found that the mobility during recovering procedure was nearly the same but larger than the initial value (the origin state). The threshold voltage varied from initial value of -14 V to -42 V after dc stress, and then gradually recovered to -12 V. This phenomenon corresponded to that the dc stress was not a damage process, but a charge capturing and releasing process in organic semiconductor. The even better mobility than that of origin state was possibly attributed to the reconstruction of pentacene/oxide interface and pentacene molecule's rearrangement (not shown). Those made the pentacene film denser and enhance the carrier transport in pentacene.

4.3.6 The Driving of Display

Fig. 4.9(a) presents an equivalent pixel structure, including an organic TFT with an equivalent capacitance of C_{Pixel} (which combines an additional assistance storage capacitance C_S and a liquid crystal parasitic capacitance C_{LC}). Fig. 4.9(b) presents a microscopic image of the layout of a single pixel and Fig. 4.9(c) presents a cross-section view of the AMLCD. Each pixel was addressed once and its written state is retained for the interval of a frame. The driving scheme is described briefly below. The rows were triggered consecutively by applying a high negative pulse voltage that maintained a scan line selection period (screen

refresh time (T_{frame})/ number of horizontal scan lines (N_{row})). The given scan signal turned on the switch organic TFTs in the pixels of the same row, at the same time the data signals were simultaneously written into individual pixels. The data signal was stored in the storage capacitor to modulate the TNLC state for one frame interval until the next writing.

The most important organic TFT criterion for the operation of this display was to ensure that the proposed on-current (I_{on}) could charge up the pixel capacitor in a limited selection row time. Another condition was that the data signal stored in the storage capacitor would not decay via the organic TFT leakage path in the remaining frame interval. The criteria are specified in terms of the display resolution, the frame rate, the operating voltage and the storage capacitance, according to the following equation.

$$I_{on} \geq \frac{6C_{pixel}V_{on}N_{row}}{T_{frame}} \tag{4.1}$$

$$I_{off} \leq \frac{C_{pixel}V_{on}}{N_{gray}MT_{frame}} \tag{4.2}$$

$$\frac{I_{on}}{I_{off}} \geq 6MN_{row}N_{gray} \tag{4.3}$$

where I_{on} is the required minimum on-current; I_{off} is the required maximum leakage current; N_{gray} is the number of gray levels; M is the empirical safety margin coefficient, and V_{on} is the maximum data signal voltage [112]. Eqs. (4.1) and (4.2) yield the required minimum on-current and the maximum off-current of organic TFTs, respectively. Accordingly, Eq. (4.3) specifies the required modulated on/off ratio of organic TFTs.

A 3 inch active-matrix TNLC display with a 64 × 128 resolution, and a pixel size of 500 μm × 500 μm was fabricated. In the display, the total pixel capacitance was set to 1.4 pF; T_{frame} was 16 ms (frame rate 60 Hz); the scan signal pulse swing was between 0 V to -40 V; the data signal was from 5 V to -20 V, the safety margin coefficient M was 3; N_{gray} was 16 steps; the required minimum on-current should exceed 0.68 μA, and the required maximum

leakage current should be less than 36.7 pA. If N_{gray} was increased to 256 steps, then the leakage current of each pentacene transistor should be less than 2.29 pA for a given pixel structure. Based on the above calculation, the process design rule and the obtained device mobility of 0.014 cm^2/Vs, the driving pentacene transistors in this display were designed with a channel length and a channel width of 70 μm and 320 μm, respectively. The storage capacitance was designed to be 1.4 pF, and the parasitic C_{LC} was calculated to be less than 0.01 pF, to meet the requirements. The final aperture ratio of this display was 38.4 %.

Fig. 4.10 plots the voltage-transmittance curve of a single TNLC cell. The transmittance varied from 35 % at 1.5 V to almost 0 % at 3 V. Out of this range, the TNLC was in the transparent state (< 1.5 V) or in the dark state (> 3 V). The two states determined the contrast ratio of the display. In fact, the pentacene transistors in the pixels were over-designed with a high width/length ratio. The given data signal (5 V to -20 V) was also magnified out of the range of modulation of the TNLC display. The two preventive measurements were made to suppress the signal loss caused by the parasitic effect and to ensure that the on-current sufficed to charge up the storage capacitor. The display could demonstrate a black and white video image with a refresh rate of 20 Hz. It performed a contrast ratio of the order of normal paper and a brightness of 30 nits. Fig. 4.11 shows the display with image pattern, Fig 4.11(a) for the monochrome type display, and Fig. 4.11(b)(c) for the multi-color type display fabricated by integration of color filter. Of course, the performance of this display still has much room for improvement. The yield of pixels and the uniformity need further improvement.

Numerous factors influenced the final display performance. For example, the TNLC display cell gap strongly affected the display uniformity. The contrast ratio of display was determined by the pixel aperture ratio, the black matrix area, the TNLC transmittance, the polarizer absorption and other factors. The organic TFTs variation seems not to affect the display too strongly herein. However, the organic TFTs variation should be further

suppressed to improve the display performance. For instance, the organic TFTs threshold voltage variation of ±1 V yields an almost 5 % difference in the charging on-current, perhaps in response to the charging up of the storage capacitor, in a manner related to the TNLC display transmittance if the display has a high resolution and small gray level step. In conclusion, although the display performance still has much room for improvement, the organic TFTs driving TNLC display was realized.

4.4 Conclusion

A 3 inch 64 × 128 active-matrix TNLC display with pentacene transistors was fabricated and demonstrated. The electronic stability of pentacene transistors was studied in various environments. The pentacene transistors were sensitive to humidity/H_2O and easily failed in organic solvent during the subsequent LC process. A passivation bilayer consists of PVA and PI deposited on the top of the device to overcome issues related to the integration of a pentacene device into an active-matrix TNLC display. The photosensitivity characteristics of pentacene transistors were also investigated. The findings reveal that the pentacene transistors can drive a normal active-matrix TNLC display with a backlight system. However, an additional light shield layer is recommended. The gate bias stress accelerates the on-current decay of the pentacene transistors; fortunately, the decay is reversible. The findings suggest that the reliability of the organic TFT could be extremely raised in real applications by specially operation, since the stress for organic TFT was a release behavior rather than a degradation one. The reliability and uniformity of pentacene transistors were investigated in relation to display applications. In this chapter, the monochrome and multi-color display by integration of color filters were demonstrated. Although this display required adjustment, a high-resolution transparent AMLCD application was realized. In this work, a rigid 0.7 mm glass substrate was adopted. It will

soon be easily transferred to flexible plastic substrates. Therefore the organic TFT has the potential play an important role in future display technology.

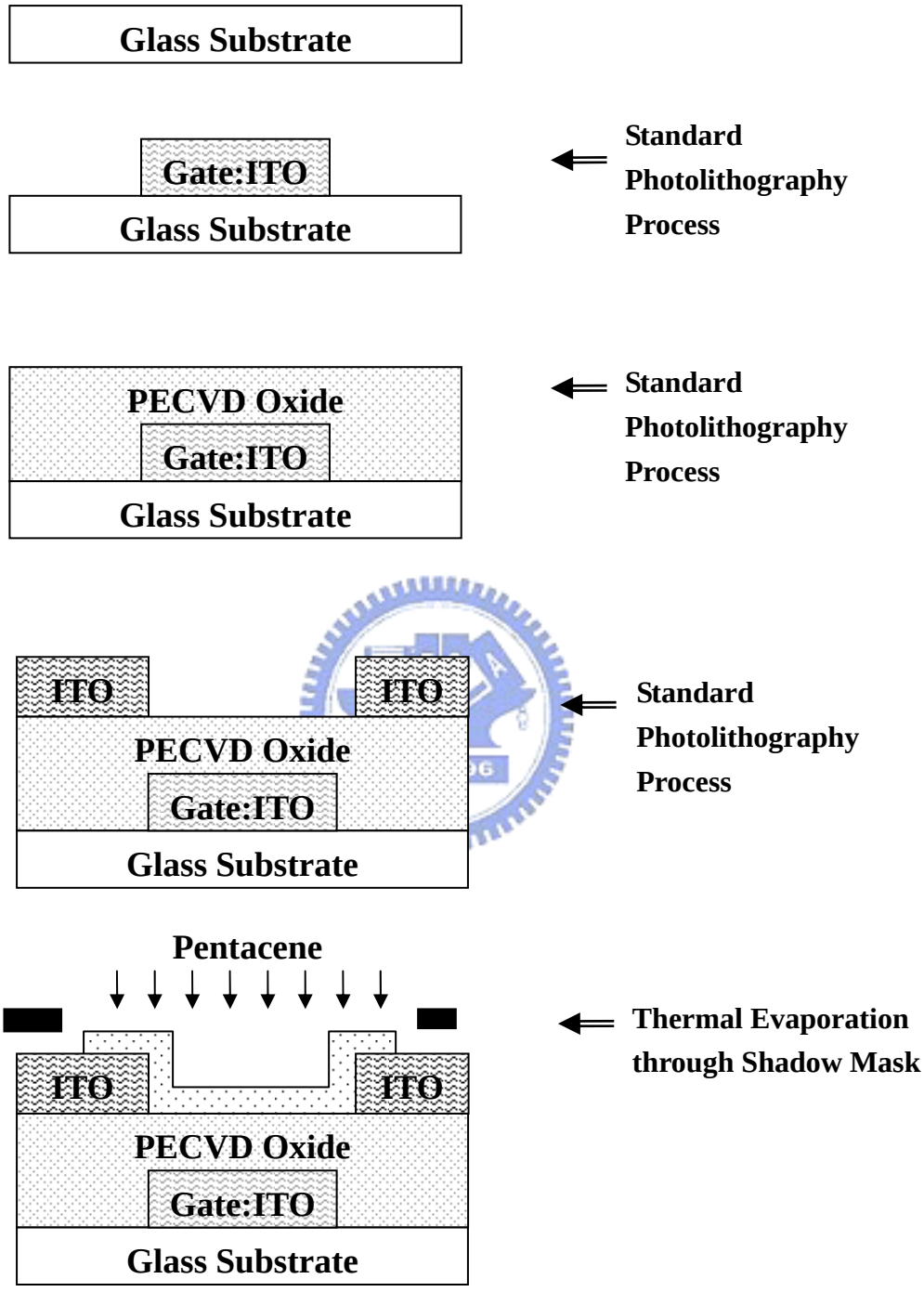

Fig. 4.1 (a) The process flow of the inverted coplanar type pentacene TFTs.

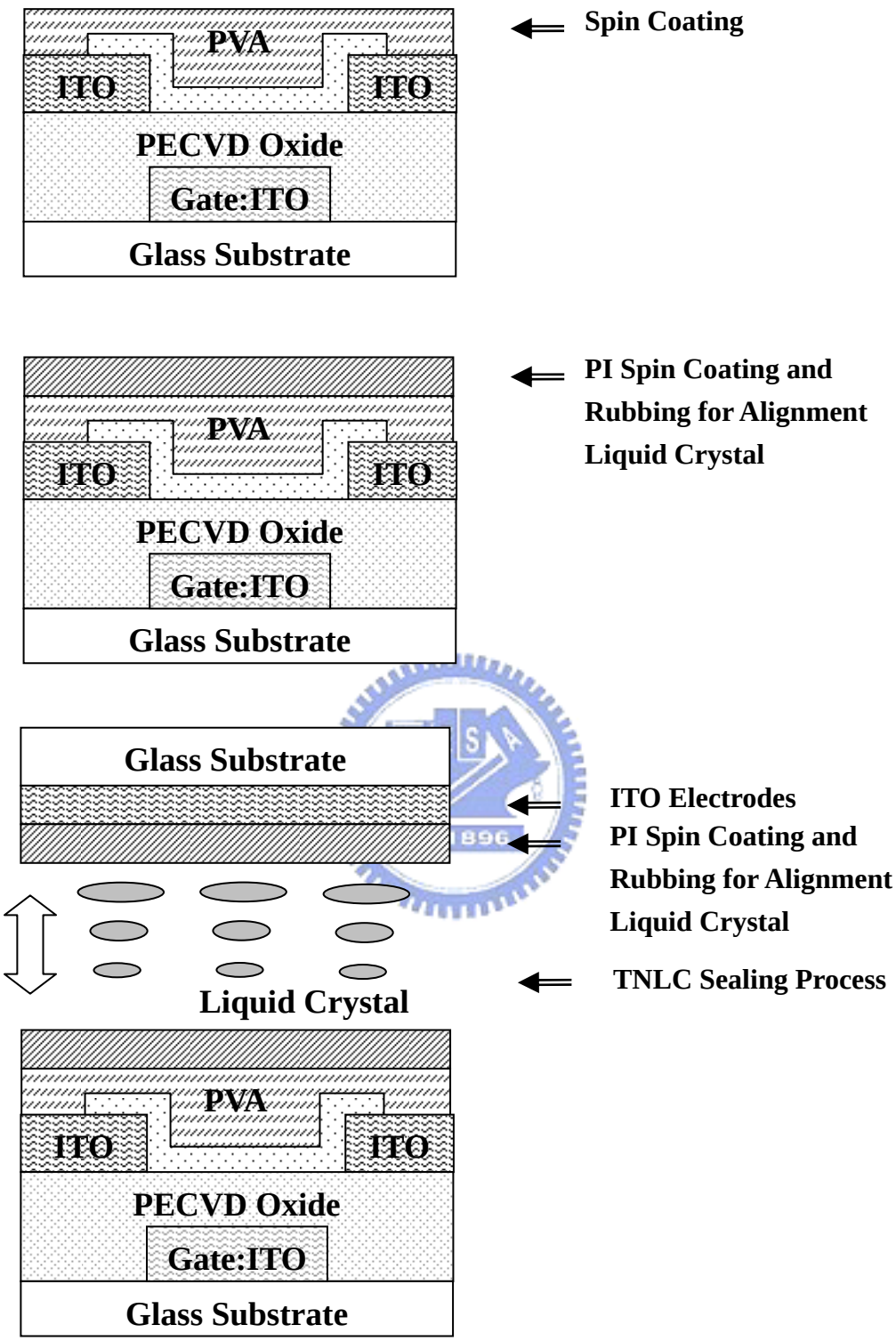

Fig. 4.1 (b) The process flow for an active matrix TNLC display driven by inverted coplanar type pentacene TFTs.

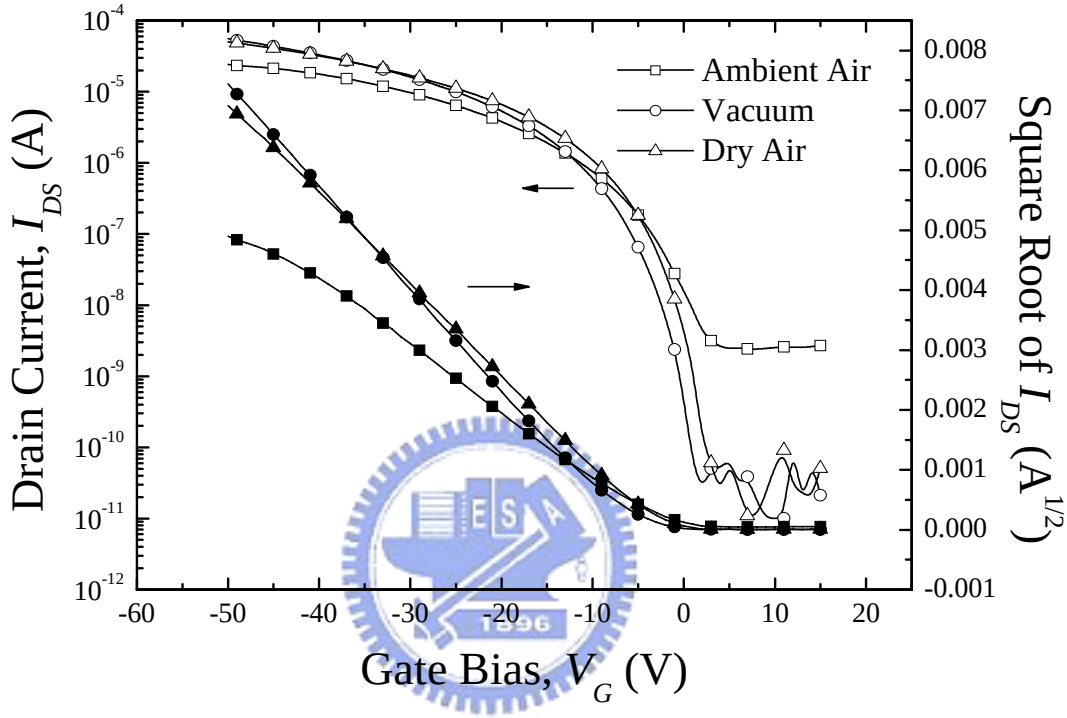

Fig. 4.2 Log (I_{DS})-V_G (left axis, open symbols) and (I_{DS})$^{1/2}$-V_G (right axis, closed symbols) characteristics of a pentacene transistor measured in air (squares), in vacuum (circles), and in dry air after 25 hours of pre-test storage (triangles) with a V_D of -50 V. The channel width and length are 20000 and 57 μm, respectively.

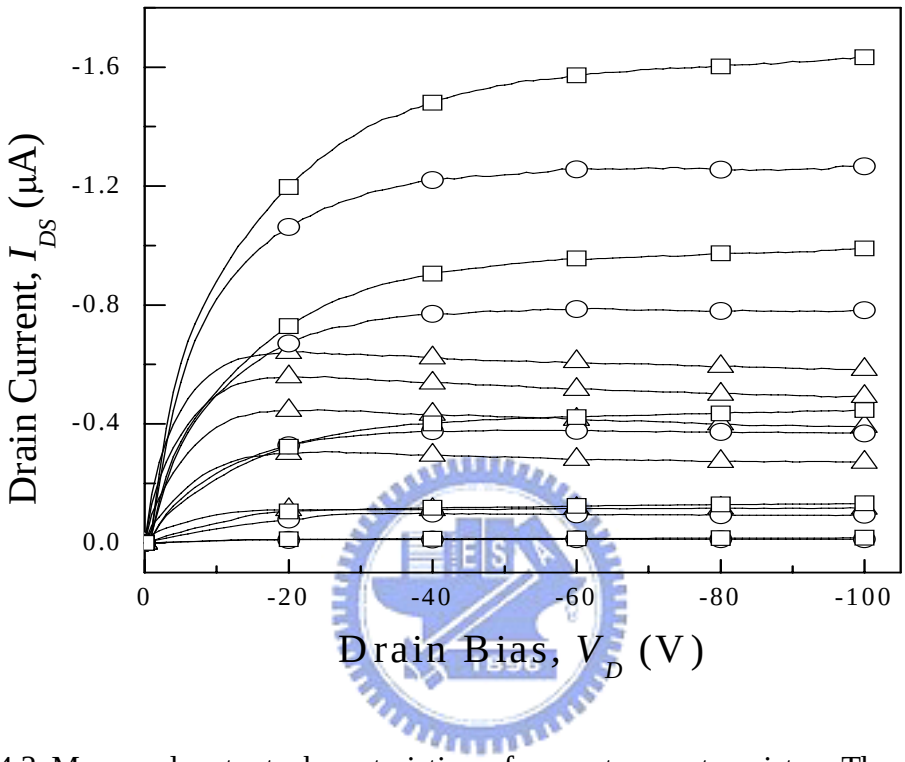

Fig. 4.3 Measured output characteristics of a pentacene transistor. The triangle symbols indicate the bare device without any passivation layer. The circles indicate the same device with the PVA/PI passivation layer upon it. The square symbols show the same device with the PVA/PI passivation layer after the full cycle of liquid crystal processing. The curves correspond to five different gate–source biases, from -20 to -100 V, in increments of -20 V. The measurements were performed in ambient air condition. The featured device had a channel width and length of 500 and 50 μm, respectively.

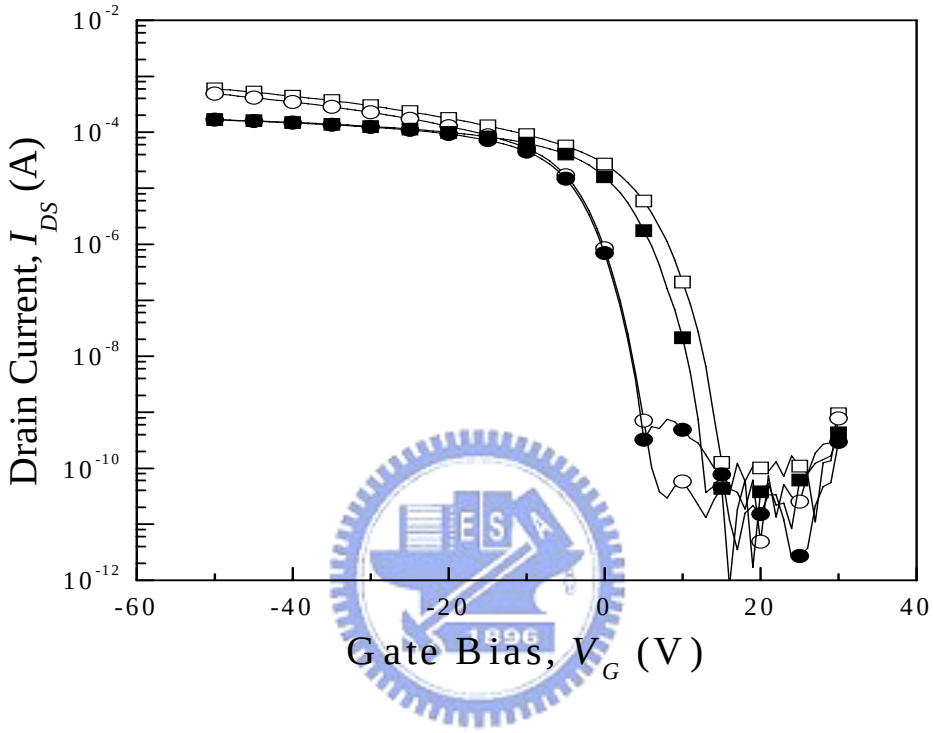

Fig. 4.4 Transfer characteristics of a pentacene transistor under illumination (squares) and without illumination (circles). The curves correspond to two different V_D of -10 V (closed symbols) and -50 V (open symbols), respectively. The measurements were performed in vacuum. The featured device had a channel width and length of 20000 and 57 μm, respectively.

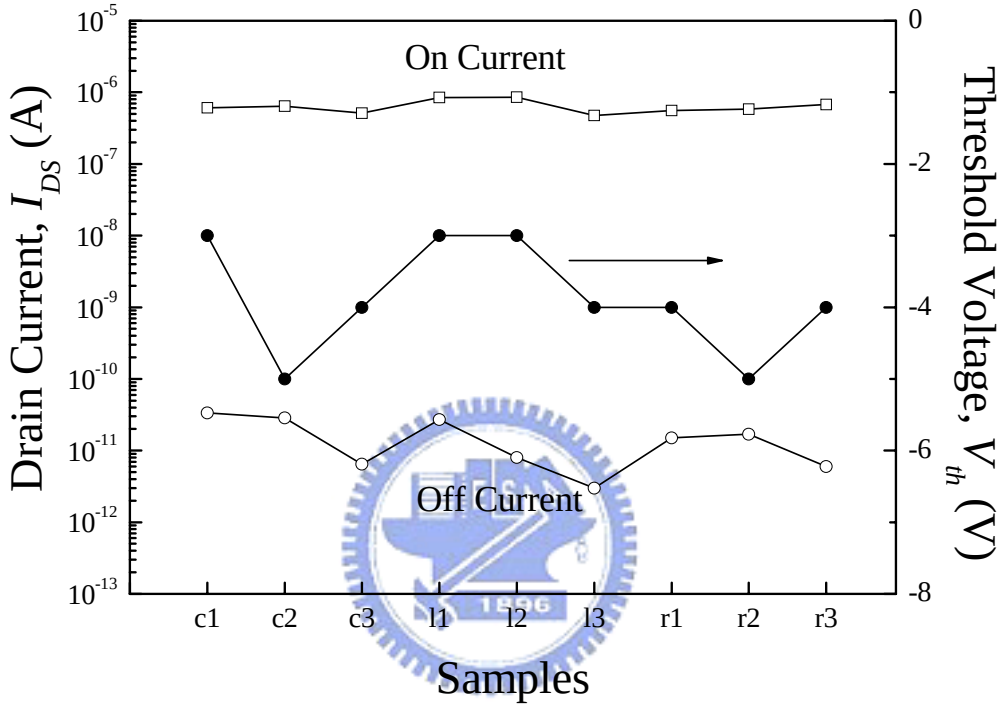

Fig. 4.5 On current, off current, and threshold voltage of nine pentacene transistors distributed in a 3 inch organic TFTs array. The lines were drawn to guide to the eyes.

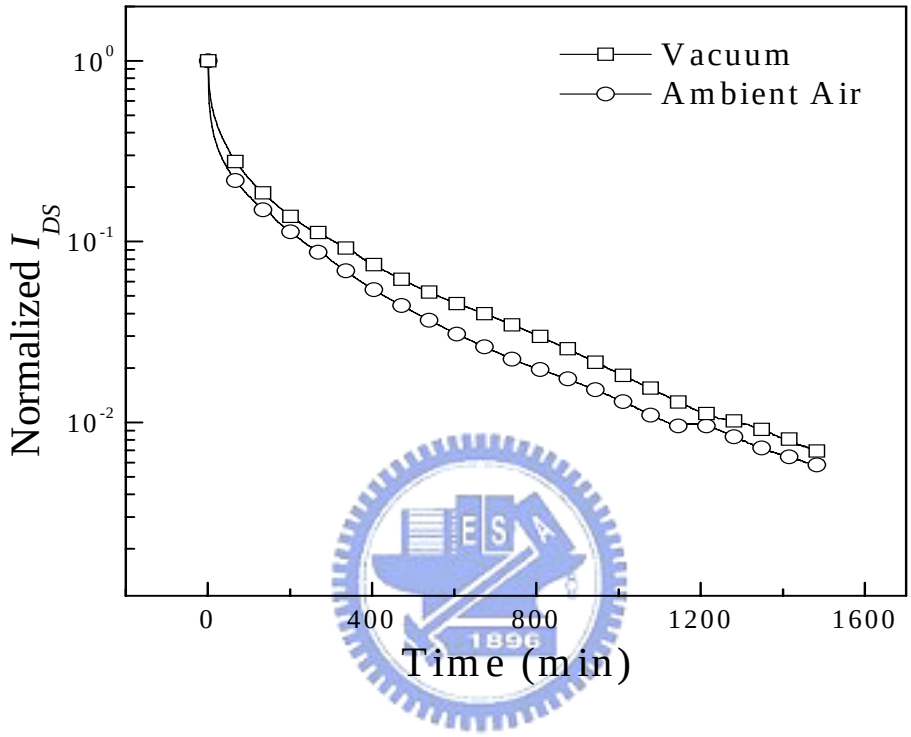

Fig. 4.6 The normalized drain current as a function of time of pentacene transistors stressed at V_G of -50 V and V_D of -50 V in vacuum (squares) and in ambient air (circles).

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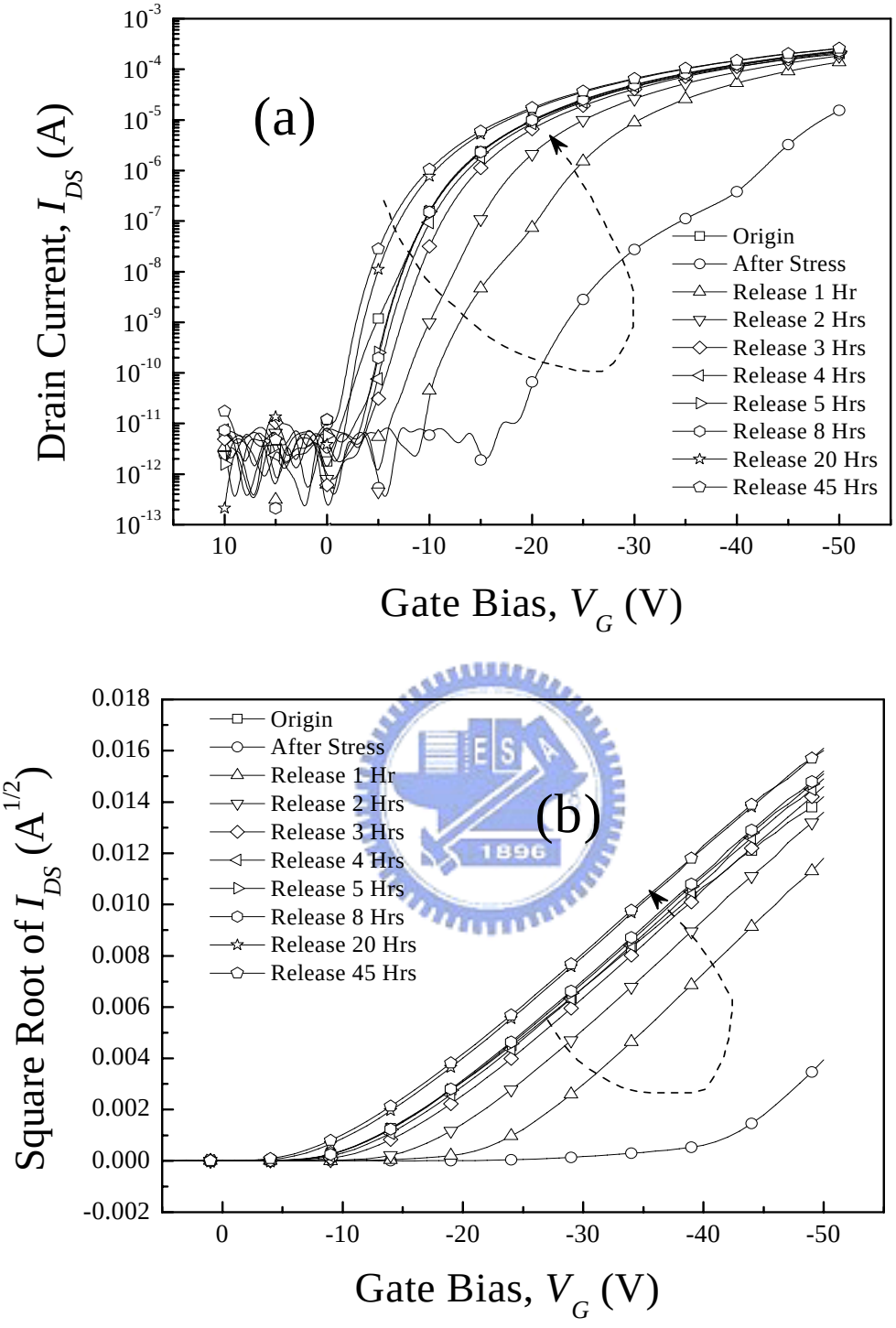


Fig. 4.7 (a) The transfer curves, at V_D of -50 V, in the conditions of the origin state, after dc stress at V_D=V_G=-50 V for 25 hrs, after stress release for 1, 2, 3, 4, 5, 8, 20, 45 hrs. The BC TFT has a device feature of channel width and length of 20000 and 17 μm, respectively. (b) The square root of I_{DS} versus V_G at the same condition with (a).

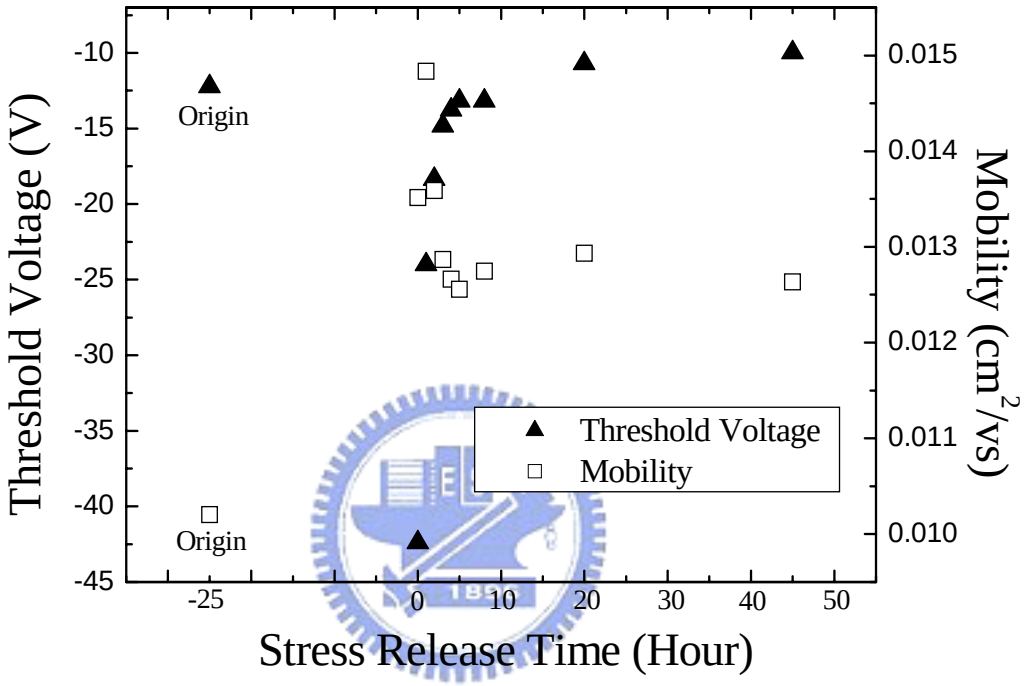


Fig. 4.8 The extracted threshold voltage and mobility of the results in Fig. 4.7.

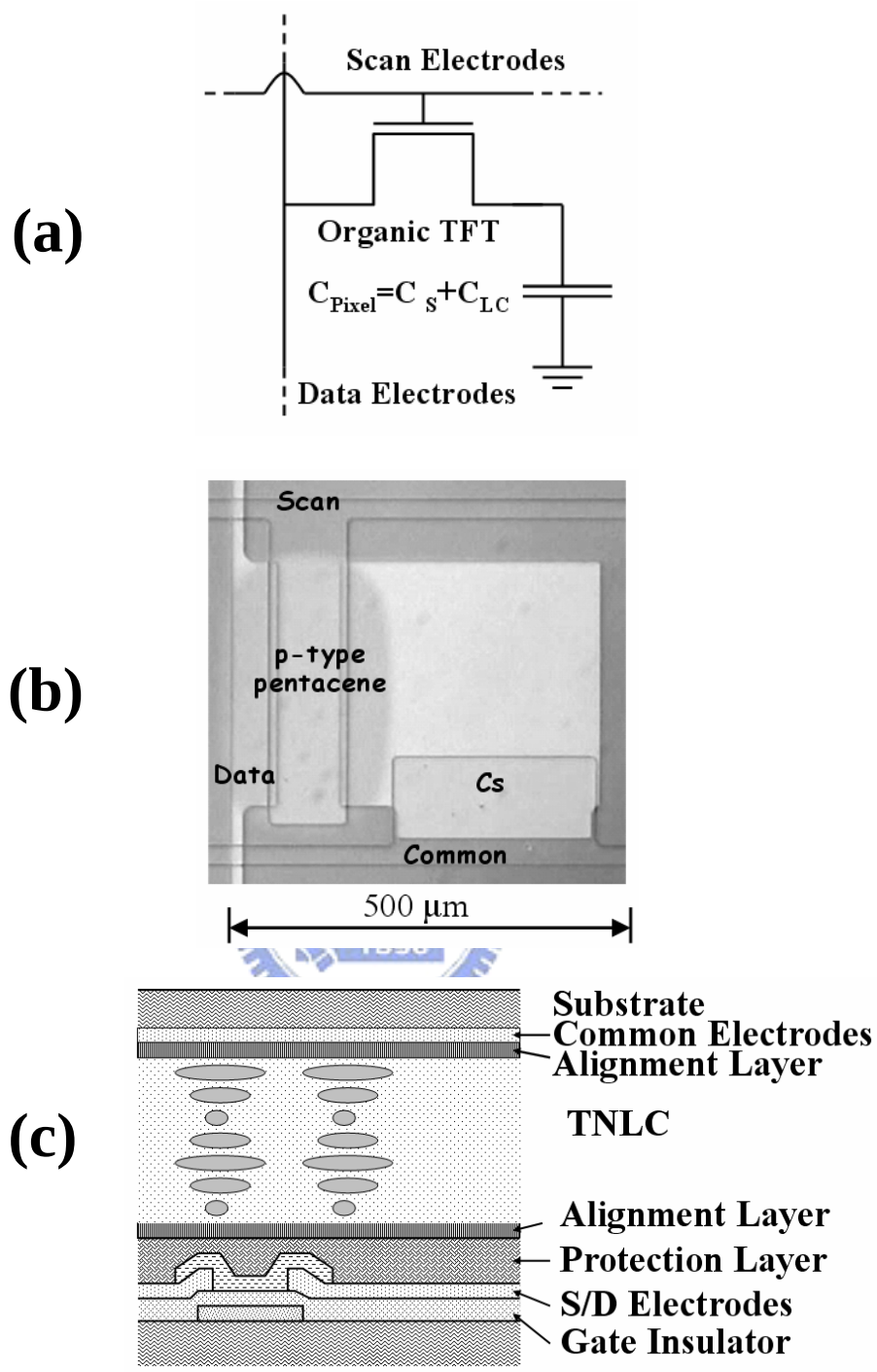


Fig. 4.9 (a) Equivalent pixel structure, including one transistor, one storage capacitor C_S and an additional assisting liquid crystal parasitic capacitor C_{LC}. The reference is made to the Cs on common pixel structure. (b) Microscopic view. (c) Cross section of active-matrix pixel structure.

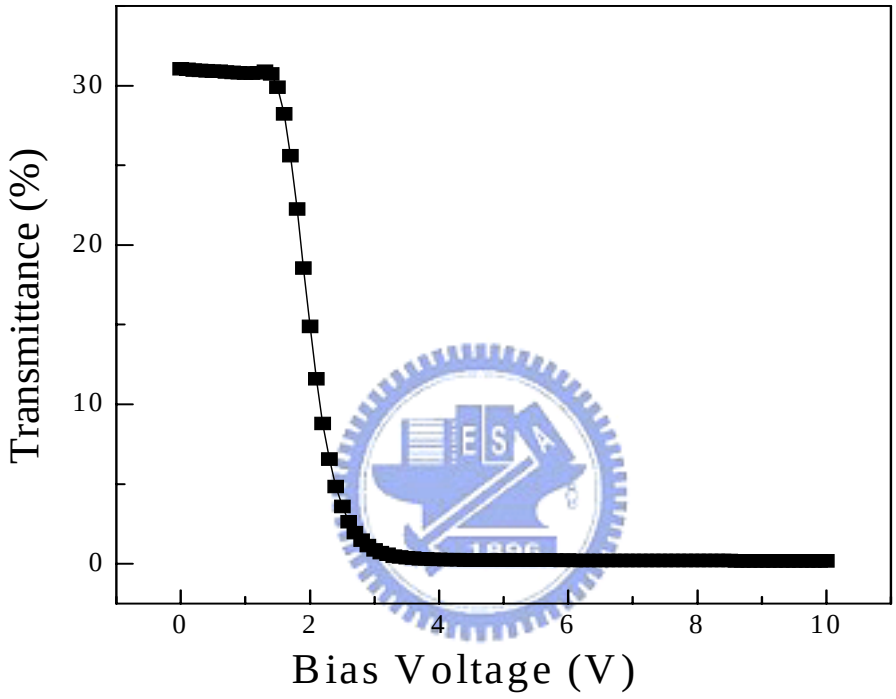
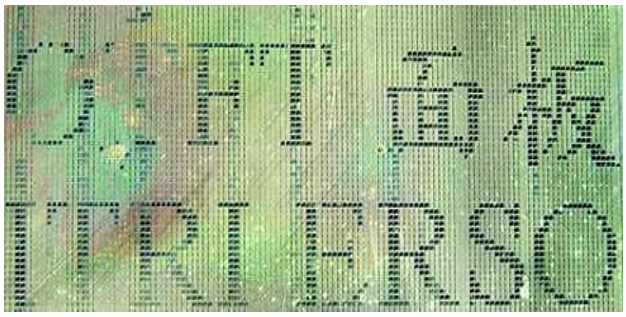
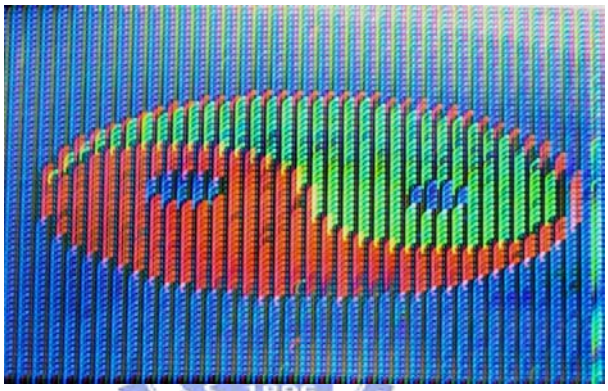


Fig. 4.10 Voltage-transmittance curve of TNLC.



(a)



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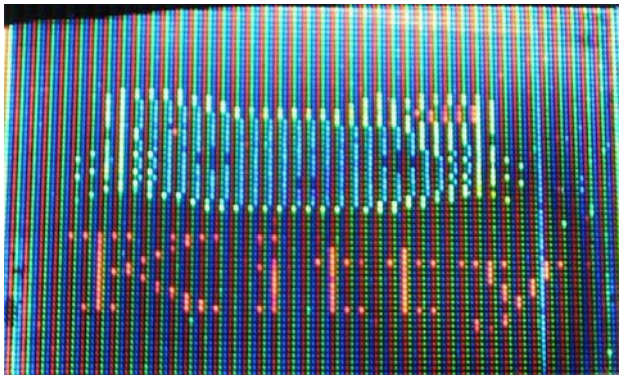

(c)

Fig. 4.11 A 3 inch 64 × 128 active-matrix TNLC display, (a) the monochrome type, (b)(c) the multi-color type with integration of color filter.