國 立 交 通 大 學

電子工程學系　　電子研究所碩士班

碩 士 論 文

用於 UWB 之 CORDIC based 等化器設計

CORDIC based Equalizer for Ultra-Wide band system

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摘要

本論文提出以 CORDIC 為核心的 IEEE802.15.3a 接收器為設計目標的等化器設計與實現。並利用平行化及管線化(pipeline)結構，設計出具有高速以及低複雜度的等化器，其輸出量最快可達到 655 百萬取樣。為了能完成完整的 UWB 模擬及研究。我們根據 S-V 通道模型，以及 Intel 提出的室內通道模型，建構出 UWB 所需的通道模型。在演算法方面，以 CORDIC 為核心的通道估測演算法，以及通道估測誤差修補演算法被推導出，並驗證其複雜度低於一般的演算法。同時,在 CMOS.18 製程下以 SYNOSYS ASTRO 完成 macro 設計。

CORDIC based Equalizer for Ultra-Wide band system

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Abstract

In this thesis, we proposed a high speed Equalizer for CORDIC based inner receiver, including modulation, FFT/IFFT, synchronization and equalization. By the parallel and pipeline design, the proposed design, based on the specification of IEEE 802.15.3a Ultra Wideband system, has good speed performance and low complexity. The throughput can achieves 655M samples per second. In order to fully simulation the UWB system, a channel model base on S-V model and Intel proposed channel model are built and verification. We proposed a CORDIC based channel estimation and channel estimation error tracking algorithm with low computation complexity. Also, the macro design in CMOS.18 μm with core size 1470 x 1470 um^2 is applied with SYNOPSYS ASTRO

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Introduction

1.1. Introduction to Ultra Wide band.

The Ultra Wide Band (UWB) system is a wireless personal area networks (WPAN) which is built for in-home use. It allows consumer to connect their electronic products without cables anymore. Because it offers high-rates in short distance, so consumer can share multimedia in WPAN, including large screen displays, speakers, televisions, digital video recorders, digital cameras, smart phones and more.

1.2. Ultra wide band physical layer.

The UWB system utilize the unlicensed 3.1 ~ 10.6 GHz band. UWB system provides data payload communication capabilities of 53.3, 55, 80, 106.67, 110, 160, 200, 320, and 480 Mb/sec, and UWB system employs orthogonal frequency division multiplexing (OFDM). The system uses a total of 122 sub-carriers that are modulated using quadrature phase shift keying (QPSK). Forward error correction coding (convolutional coding) is used with a coding rate of 1/3, 11/32, ½, 5/8, and ¾. The rate-dependent parameters in each data rate are listed in Table 1.1.

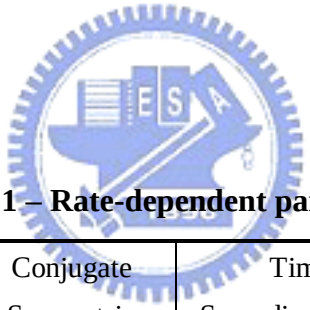


Table 1.1 – Rate-dependent parameters

Data Rate (Mb/s)	Modulation	Coding rate (R)	Conjugate Symmetric Input to IFFT	Time Spreading Factor	Overall Spreading Gain	Coded bits per OFDM symbol (N_{CBPS})
53.3	QPSK	1/3	Yes	2	4	100
55	QPSK	11/32	Yes	2	4	100
80	QPSK	½	Yes	2	4	100
106.7	QPSK	1/3	No	2	2	200
110	QPSK	11/32	No	2	2	200
160	QPSK	½	No	2	2	200
200	QPSK	5/8	No	2	2	200
320	QPSK	½	No	1 (No spreading)	1	200
400	QPSK	5/8	No	1 (No spreading)	1	200
480	QPSK	¾	No	1 (No spreading)	1	200

In Table 1.2, it lists timing-related parameters. An OFDM symbol period is T_{SYM} = T_{CP} + T_{FFT} + T_{GI} = 312.5ns. T_{CP} is the circular prefix which is used in OFDM to mitigate the effects of multi-path. The parameter T_{GI} is the guard interval duration. T_{FFT} is the 123-point FFT period which is 242.42ns

Table 1.2 – Timing-related parameters

Parameter	Value
N_{SD}: Number of data subcarriers	100
N_{SDP}: Number of defined pilot carriers	12
N_{SG}: Number of guard carriers	10
N_{ST}: Number of total subcarriers used	122 (= N_{SD} + N_{SDP} + N_{SG})
Δ_F: Subcarrier frequency spacing	4.125 MHz (= 528 MHz/128)
T_{FFT}: IFFT/FFT period	242.42 ns ($1/\Delta_F$)
T_{CP}: Cyclic prefix duration	60.61 ns (= 32/528 MHz)
T_{GI}: Guard interval duration	9.47 ns (= 5/528 MHz)
T_{SYM}: Symbol interval	312.5 ns (T_{CP} + T_{FFT} + T_{GI})

In table 1.3, the RX-to-TX turnaround time shall be pSIFSTime which is equal to 32 OFDM symbol. The pSIFSTime include the latency of the RF, PHY and MAC. The RX-to-TX turnaround time is related to the throughput of the system. If we can reduce the latency of PHY, we can increase the throughput of the system.

Table 1.3 – PHY layer timing parameters.

PHY Parameter	Value
pMIFSTime	6*T_{SYM} = 1.875 μs
pSIFSTime	32*T_{SYM} = 10 μs
pCCADetectTime	15*T_{SYM} = 4.6875 μs
pChannelSwitchTime	9.0 ns

The proposed UWB system also utilizes a time-frequency code (TFC) to interleave coded data over 3 frequency bands (called a band group), unique logical channels corresponding to different piconets are defined by using upto four different time-frequency codes for each band group. Different preamble patterns are used in conjunction with the different time frequency codes, the time-frequency codes and associated preamble patterns for Mode 1 devices (which operate in band group 1) are defined in Table 1.4.

Table 1.4 – Time Frequency Codes and Preamble Patterns for Different Piconets

Channel Number	Preamble Pattern	Mode 1: Length 6 Time Frequency Code					
1	1	1	2	3	1	2	3
2	2	1	3	2	1	3	2
3	3	1	1	2	2	3	3
4	4	1	1	3	3	2	2

1.3. OFDM overview.

Orthogonal Frequency Division Multiplexing (OFDM) is a multi carrier transmission technique, which divides the available spectrum into many carriers, each carrier had been modulated by a low rate data stream. OFDM is similar to Frequency Division Multiple Access (FDMA) in that the multiple user access is achieved by subdividing the available bandwidth into multiple channels, that are then allocated to users. However, the spectrum usage is much more efficiently because it spaces the

channels much closer. This is achieved by making all the carriers orthogonal to one another, “Orthogonal” means each carriers can avoid interference from others. In FDMA system, guard band are introduced between different carriers, so it can avoid interference too, but it will downgrade the spectrum efficiency. OFDM system simply use Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) to make the carriers “orthogonal”. In eq.(1.1) is a OFDM signal described by mathematical equation, where with N subcarriers and symbol duration is T, and notice that s(n) is the inverse Fourier Transform of the $x_i(n)$. In figure 1.1, it illustrates spectra of eq.(1.1); orthogonal between carriers at any carrier’s sampling point, and the interference of adjacent is all zero.

$$s(n) = \frac{A}{N}\sum x_i(n)\exp(2pf_i n), \quad \text{for } 0 \le n \le N; 0 \le i \le N$$
$$f_i = f_c + \frac{i}{T}, \quad i = 0,1,...,N-1 \tag{1.1}$$

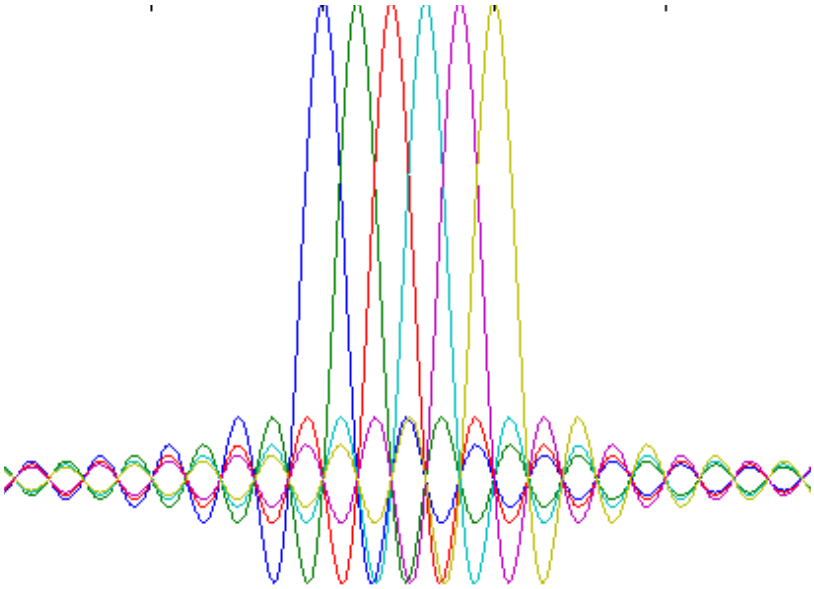


Figure 1.1 Overlapping orthogonal carriers

The OFDM technology has the following advantages:

- OFDM can deal with multi-path,
- Reduce the implementation complexity of equalizer.
- OFDM makes single frequency networks possible, which is especially attractive for broadcasting applications.
- Efficient bandwidth usage by overlapping carriers

But OFDM technology also has some drawbacks:

- OFDM system is sensitive to phase offset and frequency offset.

- OFDM system has larger peak than usual, which means it will reduce the power efficiency of the RF amplifier.

1.4. Channel Equalizer Design spec.

In OFDM system, the multi-path fading, Carrier frequency Offset (CFO) between transmitter and receiver, and Sample Frequency Offset (SCO) between Digital-Analog Converter(DAC) and Analog-Digital Converter(ADC), are the three main issues to distort data. In order to solve the multi-path problem, preambles is used to estimate the channel, but white noise will downgrade the performance of channel estimation, and the system performance will downgrade too. The way to correct the channel estimation will be discuss in chapter 4.

CFO and SCO cause the phase rotation, and will distort our data, by the definition of the UWB specification, the transmitted center frequency tolerance shall be +/- 20 ppm maximum, and the symbol clock frequency tolerance shall be +/- 20 ppm maximum. In UWB, twelve of the subcarriers are dedicated to pilot signals in order to against frequency offsets and phase noise. The detail algorithm will be listed in follow chapters.

1.5. Design requirements of Equalizer for UWB

The frame format of IEEE 802.15.3a standard has preamble, header, payload and inserted data. The header is always sent at an information data rate of 53.3 Mb/s, and the remainder of the frame is sent at the desired information data rate of 53.3, 55, 80, 106.7, 110, 160, 200, 320, 400, or 480 Mb/s. The information is sent in different spreading gains.

1.5.1. Frame Format

Figure 1.2 shows the format for the PLCP frame. The PLCP frame includes PLCP preamble, PLCP header, frame payload, and inserted data. In PLCP preamble, 29 OFDM symbols are included. The packet synchronization sequences are used for packet detection and acquisition, coarse carrier frequency estimation, and coarse symbol timing. The frame synchronization sequences are used for synchronize the receiver algorithm. Finally, the channel estimation sequences {CE_0, CE_1, CE_2, CE_3, CE_4, CE_5} are used to estimate the channel frequency response, fine carrier frequency estimation, and fine symbol timing. In ultra wide-band specification, OFDM symbols are transmitted over three different sub-bands, so each sub-band can only use two channel estimation sequences.

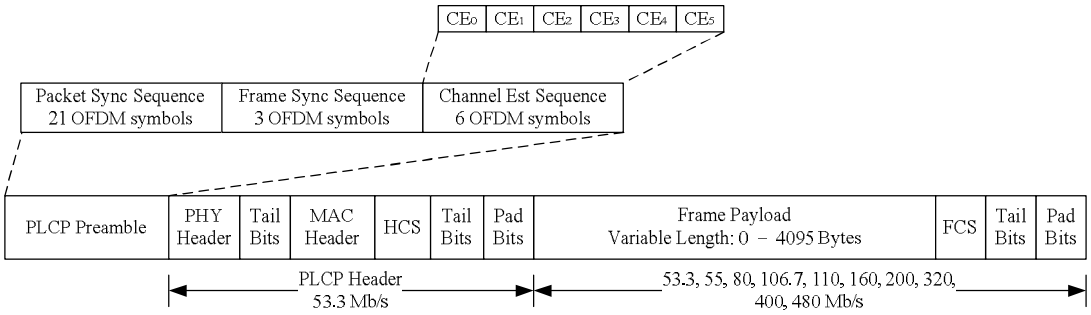


Figure 1.2 – PLCP frame format

1.5.2. Data Subcarriers

An OFDM symbol $r_{data,k}(t)$ is defined as

$$r_{data,k}(t) = \sum_{n=0}^{N_{SD}} c_{n,k} \exp(j2pM(n)\Delta_F(t - T_{CP})) \qquad n = 0,1,...,99, \tag{1,2}$$

where N_{SD} is the number of data subcarriers, and the function ***M(n)*** defines a mapping from the indices 0 to 99 to the logical frequency offset indices –56 to 56, the function M(n) is described as below:

$$M(n) = \begin{cases} -56 & n = 0 \\ n-55 & 1 \le n \le 9 \\ n-54 & 10 \le n \le 18 \\ n-53 & 19 \le n \le 27 \\ n-52 & 28 \le n \le 36 \\ n-51 & 37 \le n \le 45 \\ n-50 & 46 \le n \le 49 \\ n-49 & 50 \le n \le 53 \\ n-48 & 54 \le n \le 62 \\ n-47 & 63 \le n \le 71 \\ n-46 & 72 \le n \le 80 \\ n-45 & 81 \le n \le 89 \\ n-44 & 90 \le n \le 98 \\ 56 & n = 99 \end{cases} \tag{1.3}$$

Notice that the logical frequency offset indices -55, -45, -35, -25, -15, -5, 5, 15, 25, 35, 45, and 55, are not defined in the function of M(n), those subcarriers will insert pilot subcarriers. Subcarrier frequency allocation is shown in fig 3.2. To avoid difficulties in DAC and ADC offsets and carrier feed-through in the RF system, the subcarrier falling at DC (0^{th} subcarrier) is not used. The frequency allocation of subcarrier shows in Fig. 1.3.

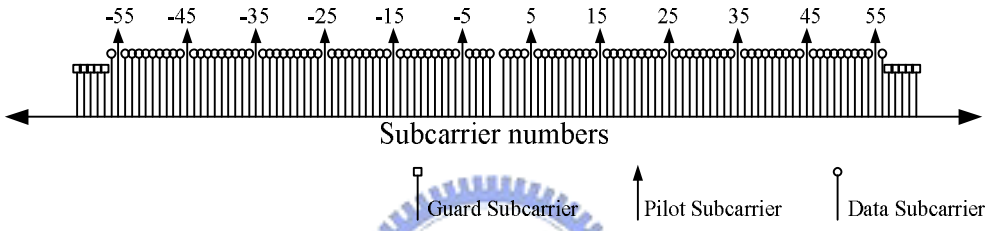


Figure 1.3 – Subcarrier frequency allocation

For lower information data rates, such as 53.3, 55, and 80 Mb/s, conjugate symmetric input to IFFT is needed, so the stream of complex numbers is divided into groups of 50 complex numbers. The complex numbers $c_{n,k}$ is corresponds to subcarrier n of OFDM symbol k, as follows:

$$\begin{aligned} c_{n,k} &= d_{n+50\times k} \\ c_{(n+50),k} &= d^{*}_{(49-n)+50\times k} \end{aligned} \qquad n = 0,1,\mathbf{K},49, k = 0,1,\mathbf{K},\mathrm{N}_{\mathrm{SYM}}-1 \tag{1,4}$$

For information data rates that higher than 106.7, such as 110, 160, 200, 320 and 480 Mb/s, the stream of complex numbers is divided into groups of 100 complex

numbers. Again, the complex numbers $c_{n,k}$, which corresponds to subcarrier n of OFDM symbol k, as follows:

$$c_{n,k} = d_{n+100\times k} \qquad n = 0,1,\mathbf{K},99, k = 0,1,\mathbf{K},\mathrm{N_{SYM}} - 1 \qquad (1,5)$$

Where NSYM denotes the number of OFDM symbols in the MAC frame body, tail bits, and pad bits.

1.5.3. Pilot subcarriers

In each OFDM symbol, twelve of the subcarriers are dedicated to pilot signals in order to make coherent detection robust against frequency offsets and phase noise. These pilot signals shall be put in subcarriers numbered –55, –45, –35, –25, –15 –5, 5, 15, 25, 35, 45, and 55. The contribution due to the pilot subcarriers for the k^{th} OFDM symbol is given by the inverse Fourier Transform of the sequence P_n below, which is further BPSK modulated by a pseudo-random binary sequence, p_l (defined further below), to prevent the generation of spectral lines.

$$P_n = \begin{cases} \dfrac{1+j}{\sqrt{2}} & n = 15,45 \\ \dfrac{-1-j}{\sqrt{2}} & n = 5,25,35,55 \end{cases} \qquad (1,6)$$

For modes with data rates less than 106.67 Mbps:

$$P_{n,k} = P^{*}_{-n,k}, \qquad n = -5,-15,-25,-35,-45,-55 \qquad (1,7)$$

For 106.67 Mbps and all higher rate modes:

$$P_{n,k} = P_{-n,k}, \qquad n = -5,-15,-25,-35,-45,-55 \qquad (1,8)$$

The polarity of the pilot subcarriers is controlled by the following pseudo-random LFSR sequence, p_l:

$p_{0\ldots126}$ = {1, 1, 1, 1, -1, -1, -1, 1, -1, -1, -1, -1, 1, 1, -1, 1, -1, -1, 1, 1, -1, 1, 1, -1, 1, 1, 1, 1, 1, 1, -1, 1, 1, 1, -1, 1, 1, -1, -1, 1, 1, 1, -1, 1, -1, -1, -1, 1, -1, 1, -1, -1, 1, -1, -1, 1, 1, 1, 1, -1, -1, 1, 1, -1, -1, 1, -1, 1, 1, -1, -1, -1, 1, 1, -1, -1, -1, -1, 1, -1, -1, 1, -1, 1, 1, 1, 1, -1, 1, -1, 1, -1, 1, -1, -1, -1, -1, -1, 1, -1, 1, 1, -1, 1, -1, 1, 1, 1, -1, -1, 1, -1, -1, -1, 1, 1, 1, -1, -1, -1, -1, -1, -1, -1}.

Only one element of this sequence is used for an OFDM symbol. Based on the definition, the generator polynomials of p_l is illustrated in Fig 3.3

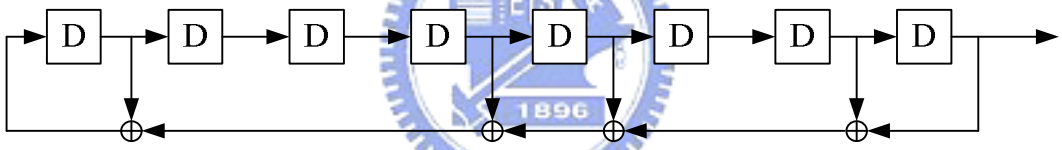


Figure 1.4 – The generator polynomials of p_l

The initial values from left to right are 1, -1, -1, -1, 1, 1, 1, 1.

1.5.4. Guard subcarriers

In each OFDM symbol, ten subcarriers are dedicated to guard subcarriers or guard tones. The guard subcarriers can be used for various purposes, including relaxing the specs on transmit and receive filters. The magnitude level of the guard tones is not specified other than the definition below, and implementations can use reduced power for these subcarriers if desired. The guard subcarriers shall be

located in subcarriers –61, –60,…, –57, and 57, 58, …, 61. The same linear-feedback shift register (LFSR) sequence, pl, that is used to scramble the pilot subcarriers shall be used to generate the modulating data for the guard subcarriers. The guard subcarrier symbol definition for the nth subcarrier of the kth symbol is given as follows:

$$P_{n,k} = p_{\mathrm{mod}(k+l,127)}\left(\frac{1+j}{\sqrt{2}}\right),\ l = 0,1,2,3,4;\ n = 57+l \tag{1,9}$$

For modes with data rates less than 106.67 Mbps:

$$P_{n,k} = P^{*}_{-n,k}, \qquad n = -57,\ldots,-61 \tag{1,10}$$

For 106.67 Mbps and all higher rate modes:

$$P_{n,k} = P_{-n,k}, \qquad n = -57,\ldots,-61 \tag{1,11}$$

In this numbering, k=0 shall correspond to the first OFDM symbol following the PLCP preamble (i.e., the first OFDM symbol following the channel estimation symbols CE0-CE5).

1.5.5. Channelization

In IEEE 802.15.3a specification, the PHY operating frequency (3.1 – 10.6 GHz) is split into 14 bands. Five band groups are also defined, consisting of four groups of three bands each and one group of two bands. Only band group 1 is used for Mode 1

devices (mandatory mode). Based on this, there are 128*3 = 384 sub-channels to estimate. The band allocation is summarized in Table 1.5

Table 1.5 – OFDM PHY band allocation

Band Group	BAND_ID	Lower frequency	Center frequency	Upper frequency
1	1	3168(MHz)	3432(MHz)	3696(MHz)
	2	3696(MHz)	3960(MHz)	4224(MHz)
	3	4224(MHz)	4488(MHz)	4752(MHz)
2	4	4752(MHz)	5016(MHz)	5280(MHz)
	5	5280(MHz)	5544(MHz)	5808(MHz)
	6	5808(MHz)	6072(MHz)	6336(MHz)
3	7	6336(MHz)	6600(MHz)	6864(MHz)
	8	6864(MHz)	7128(MHz)	7392(MHz)
	9	7392(MHz)	7656(MHz)	7920(MHz)
4	10	7920(MHz)	8184(MHz)	8448(MHz)
	11	8448(MHz)	8712(MHz)	8976(MHz)
	12	8976(MHz)	9240(MHz)	9504(MHz)
5	13	9504(MHz)	9768(MHz)	10032(MHz)
	14	10032(MHz)	10296(MHz)	10560(MHz)

1.5.6. Time-domain Spreading

For data rates of 55, 80, 110, 160 and 200 Mbps a time-domain spreading operation is performed with a spreading factor of 2. The time-domain spreading operation consists of transmitting the same information over two OFDM symbols. These two OFDM symbols are transmitted over different sub-bands to obtain frequency diversity. For example, if the device uses a time-frequency code [1 2 3 1 2

3], as specified in table 1.4, the information in the first OFDM symbol is repeated on bands 1 and 2, the information in the second OFDM symbol is repeated on bands 3 and 1, and the information in the third OFDM symbol is repeated on bands 2 and 3 [1].

1.6. Organization of this thesis.

This thesis is organized as follows: The first chapter describes a briefly introduction of UWB. In order to do the ultra wide-band equalization fully simulation, the chapter 2 introduce two UWB channel models, one is S-V channel model, the other is Intel proposed channel model, and also channel verification for both of channel models. In chapter 3, the algorithm of channel estimation, phase error tracking, and also channel estimation error tracking will be described. The chapter 4 shows the hardware implementation and verification for proposed channel equalizer. The chapter 5 shows the simulation result and the performance of the proposed design. Finally, a brief conclusion and future work are presented in chapter 6.

Chapter 2.
Channel Model

2.1. Introduction to Channel Model for Ultra Wide Band.

For doing the ultra wide-band equalization fully simulation, channel is needed to be generated and simulated in the platform. The goal of the channel model is to capture both the path loss and multi-path characteristics of 'typical' environments where IEEE 802.15.3a devices are expected to operate. In the follow, the Saleh-Valenzuela (S-V) model and Intel proposed channel model will be introduced. Then I will show that the channel we generated match several primary characteristics of multi-path channel.

2.2. The Saleh-Valenzuela (S-V) multi-path model

The Saleh-Valenzuela (S-V) model is the Ultra-wideband indoor path loss model which is presented by S. Ghassemzadeh and V.Tarokh [2]. The authors presented a simple statistical multi-path model that is easily integrates with the path loss model.

The model is based on over 3000,000 UWB frequency responses at 712 locations in 23 homes. The model regenerates the statistical properties of the indoor channel with high accuracy. This model can be used for simulation and performance evaluation of any UWB system with nominal bandwidth less than or equal 1.25 GHz, and it can be upgraded with further measurements. The main algorithm will shows below.

The channel impulse response of the IEEE model can be expressed as follows:

$$h(t) = X\sum_{n=1}^{N}\sum_{k=1}^{K(n)} a_{nk}d(t - T_n - t_{nk}) \qquad (2\text{-}1)$$

where X is a log-normal random variable representing the amplitude gain of the channel, N is the number of observed clusters, K(n) is the number of multi-path contributions received within the n-th cluster, α_{nk} is the coefficient of the k-th multi-path contribution of the n-th cluster, T_n is the time of arrival of the n-th cluster, and τ_{nk} is the delay of the k-th multi-path contribution within the n-th cluster.

The S-V model is based on the observation that usually multi-path contributions generated by the same pulse arrive at the receiver grouped into clusters. The time of arrival of clusters is modeled as a Poisson arrival process with rate Λ:

$$p(T_n \mid T_{(n-1)k}) = \Lambda e^{-\Lambda(T_n - T_{n-1})} \qquad (2.2)$$

Where T_n and T_{n-1} are the times of arrival of the n-th and the (n-1)-th clusters.

Within each cluster, subsequent multi-path contributions also arrive according to a Poisson process with rate λ:

$$p(t_n \mid t_{(n-1)k}) = l e^{-l(t_n - t_{n-1})} \tag{2.3}$$

Where τ_{nk} and $\tau_{(n-1)k}$ are the time of arrival of the n-th and the (n-1)-th contributions within cluster k.

In the S-V model, the gain of the n-th ray of the k-th cluster is a complex random variable α_n with modulus β_{nk} and phase θ_{nk}. The β_{nk} values are assumed to be statistically independent and Rayleigh distributed positive random variables, while the θ_{nk} values are assumed to be statistically independent uniform random variables over $[0,2\pi]$ or:

$$p(b_{nk}) = \frac{2b_{nk}}{\left\langle |b_{nk}|^2 \right\rangle} e^{\frac{b_{nk}^2}{\left\langle |b_{nk}|^2 \right\rangle}}$$
$$p(q_{nk}) = \frac{1}{2p} \tag{2.4}$$

where <x> is the expected value of x and where:

$$\left\langle |b_{nk}|^2 \right\rangle = \left\langle |b_{00}|^2 \right\rangle e^{\frac{-T_n}{\Gamma}} e^{\frac{-t_{nk}}{g}} \tag{2.5}$$

Notice that the total energy contained in the β_{nk} terms must be normalized to unity for each realizations:

$$\sum_{n=1}^{N} \sum_{k=1}^{K(n)} |b_{nk}|^2 = 1 \tag{2.6}$$

Base on the equation throw (2.1) to (2.6), the Power Delay Profile (PDP) of an impulse response (with $\theta_{nk} = 1$) will look like figure 2.1 below

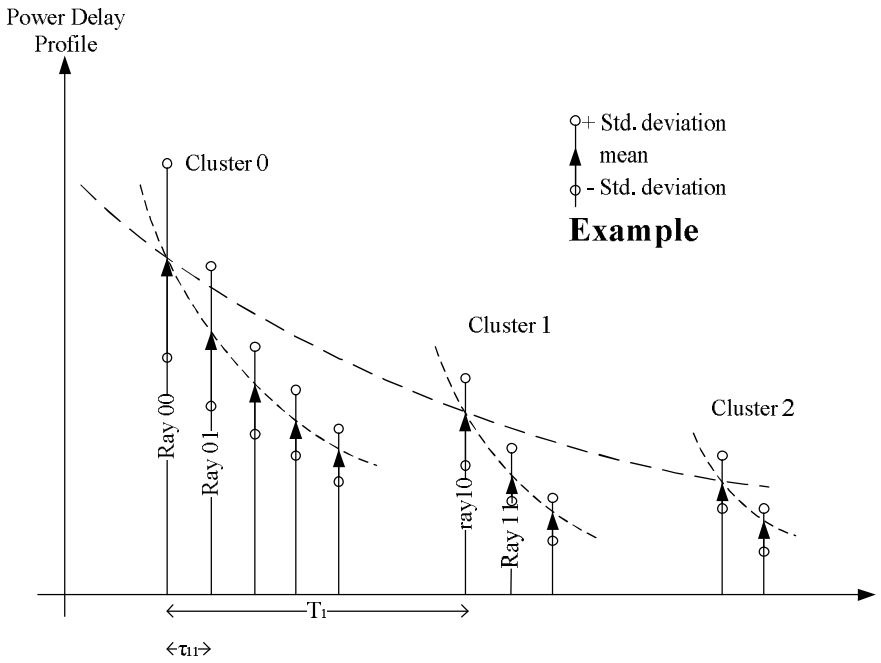


Figure 2.1 - Typical PDP for S-V model

2.3. The Intel proposed UWB multi-path channel model

In fact, ultra wide band multi-path channel model that the intel proposed is similar to S-V model. Both of them have same time arrival model [3], which means in the intel proposed multi-path channel model, the time of arrival of clusters and rays is also modeled as a Poisson arrival process. But in the intel proposed model [3], the β_{nk} values are assumed to be log-normal distributed positive random variables, that is:

$$
\begin{aligned}
& b_{nk} = 10^{\frac{x_{nk}}{20}} \\
& x_{nk} \sim Normal(u_{nk}, s_x^2 + s_V^2) \\
& u_{nk} = \frac{10\ln(\langle |b_{00}|^2 \rangle) - 10\frac{T_n}{\Gamma} - 10\frac{t_k}{g}}{\ln(10)} - \frac{(s_x^2 + s_V^2)\ln(10)}{20}
\end{aligned}
\tag{2.5}
$$

2.4. The path-loss model

The amplitude gain X in Eq. (2.1) is assumed to be a log-normal random variable:

$$X = 10^{\frac{g}{20}}$$
$$g \sim Normal(g_0, s_g^2) \tag{2.6}$$

The g_0 depends on the average total multi-path gain G:

$$g_0 = \frac{10\ln(G)}{\ln(10)} - \frac{s_g^2 \ln(10)}{20} \tag{2.7}$$

The value G can be determined as indicated below:

$$G = \frac{G_0}{D^g}$$
$$G_0 = 10^{-A_0/10} \tag{2.8}$$

In Eq. (2.8), A_0 (in dB) = $10\log(E_{TX}/E_{RX0})$. Values for both A0 and γ are suggested in (Ghassemzadeh and Tarokh, 2003) for different propagation environments: A_0=47dB and γ =1.7 for a LOS environment, and A_0= 51dB and γ =3.5 for a NLOS environment.

According to the above definitions, the channel model represented by the impulse response is fully characterized when the following parameters are defined:

- Λ : The cluster average arrival rate
- λ : The ray average arrival rate
- Γ : The power decay factor for clusters
- Γ : The power decay factor for rays in a cluster
- s_x : The standard deviation of the fluctuations of the channel coefficients

for clusters

- s_z : The standard deviation of the fluctuations of the channel coefficients for rays in each cluster
- s_g : The standard deviation of the channel amplitude gain

The IEEE suggested an initial set of values for the above parameters. These values will shows in table 2.1 [2].

Table 2.1 – Parameter Settings for the IEEE UWB Channel Model

Scenario	Λ	λ	Γ	γ	s_x	s_z	s_g
Case A LOS (0-4 m)	0.0233	2.5	7.1	4.3	3.3941	3.3941	3
Case B NLOS (0-4 m)	0.4	0.5	5.5	6.7	3.3941	3.3941	3
Case C NLOS (4-10 m)	0.0667	2.1	14	7.9	3.3941	3.3941	3
Case D Extreme NLOS Multi-path Channel	0.0667	2.1	24	12	3.3941	3.3941	3

2.5. Channel Verifications

In fact, the channel model should be reflective of actual channel measurements. Since it may de difficult for a single model to reflect all of the possible channel environments and characteristics, the group chose to try and match the following primary characteristics of the multi-path channel [4]:

- RMS delay spread
- Power decay profile
- Number of multi-path components (defined as the number of multi-path arrivals that are within 10 dB of the peak multi-path arrival)

The following Table (table 2.2) shows the target channel characteristics and the model characteristics which are generated by our group, and channel realizations from CM1 to CM4 will showed in figure 2.2 to figure 2.5

Table 2.2 – Multi-path channel characteristics and corresponding model parameters

Target Channel Characteristics[5]	**CM 1**[1]	**CM 2**[2]	**CM 3**[3]	**CM 4**[4]
Mean excess delay (nsec) (t_m)	5.05	10.38	14.18	
RMS delay (nsec) (t_{rms})	5.28	8.03	14.28	25
NP_{10dB}			35	
NP (85%)	24	36.1	61.54	
Model Parameters				
Λ (1/nsec)	0.0233	0.4	0.0667	0.0667
λ (1/nsec)	2.5	0.5	2.1	2.1
Γ	7.1	5.5	14.00	24.00
γ	4.3	6.7	7.9	12
s_1 (dB)	3.3941	3.3941	3.3941	3.3941
s_2 (dB)	3.3941	3.3941	3.3941	3.3941
s_x (dB)	3	3	3	3
Model Characteristics[5]				
Mean excess delay (nsec) (t_m)	5.0943	10.916	16.538	27.406
RMS delay (nsec) (t_{rms})	4.875	9.1993	13.233	21.631
NP_{10dB}	12.95	18.68	30.08	41.23
NP (85%)	17.04	31.42	55.93	96.4
Channel energy mean (dB)	-0.6123	-0.2597	-0.4232	-0.545
Channel energy std (dB)	2.0123	2.1298	2.22	2.1682

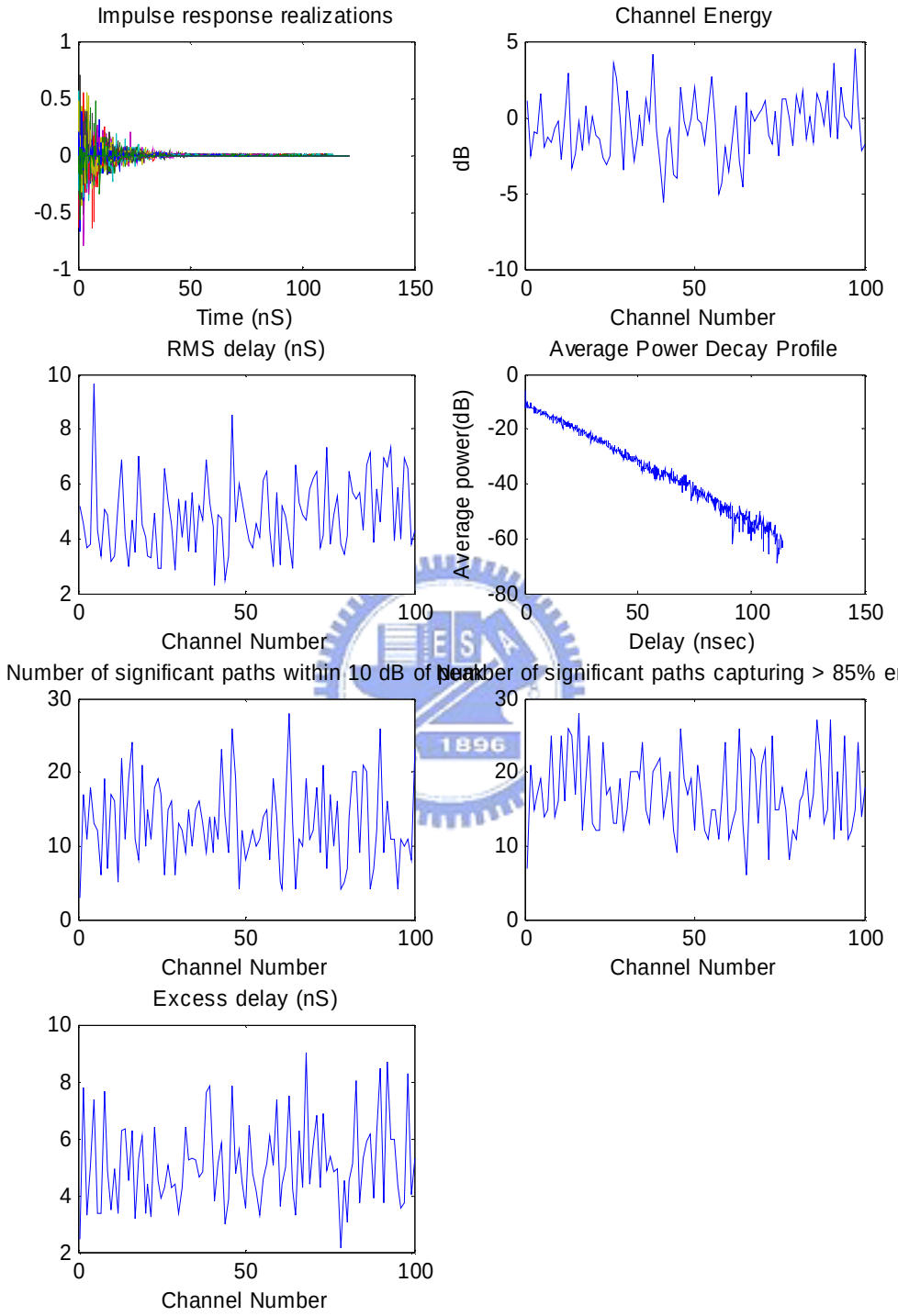


Figure 2.2 CM1 channel realizations

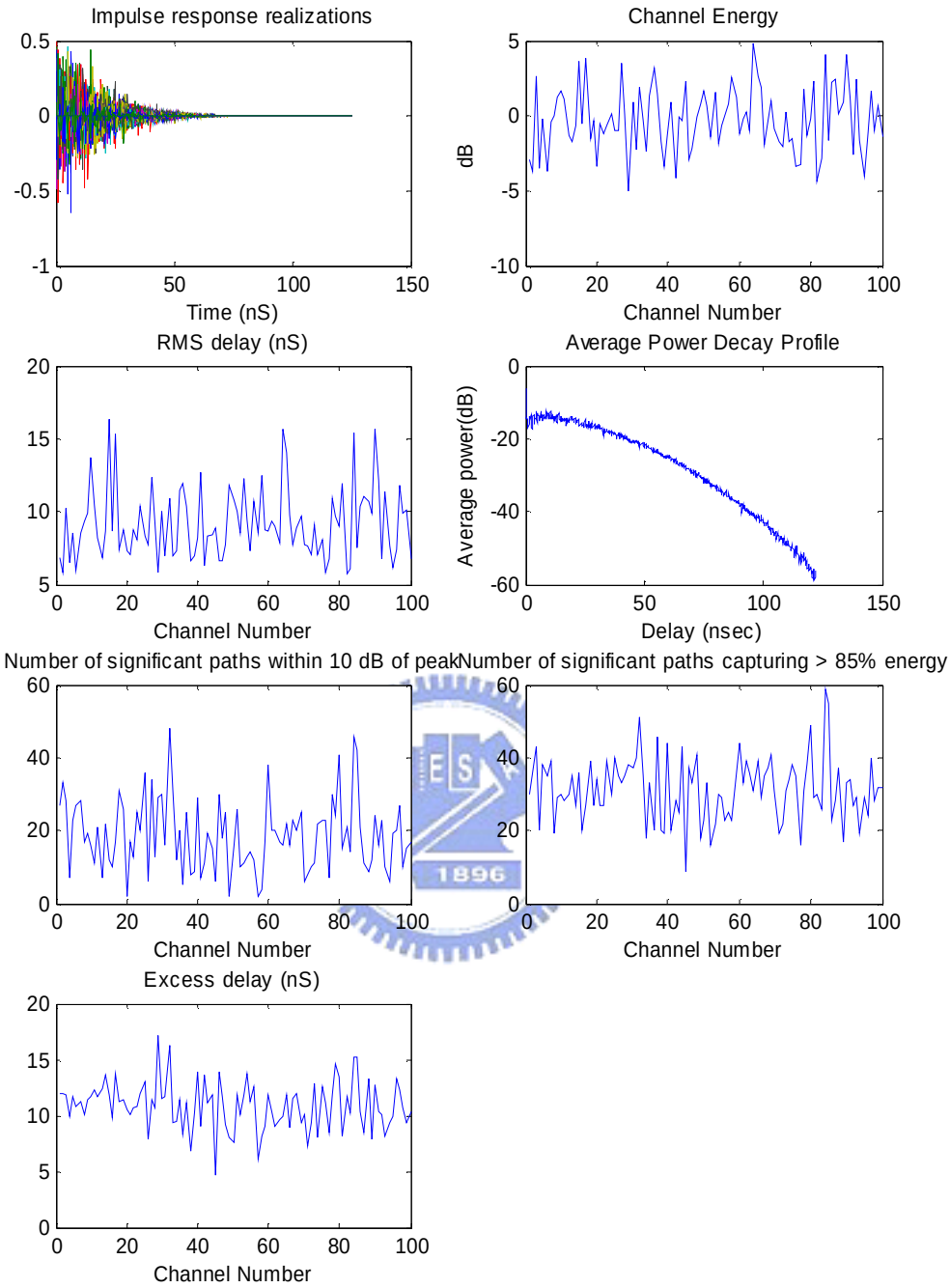


Figure 2.3 CM2 channel realizations

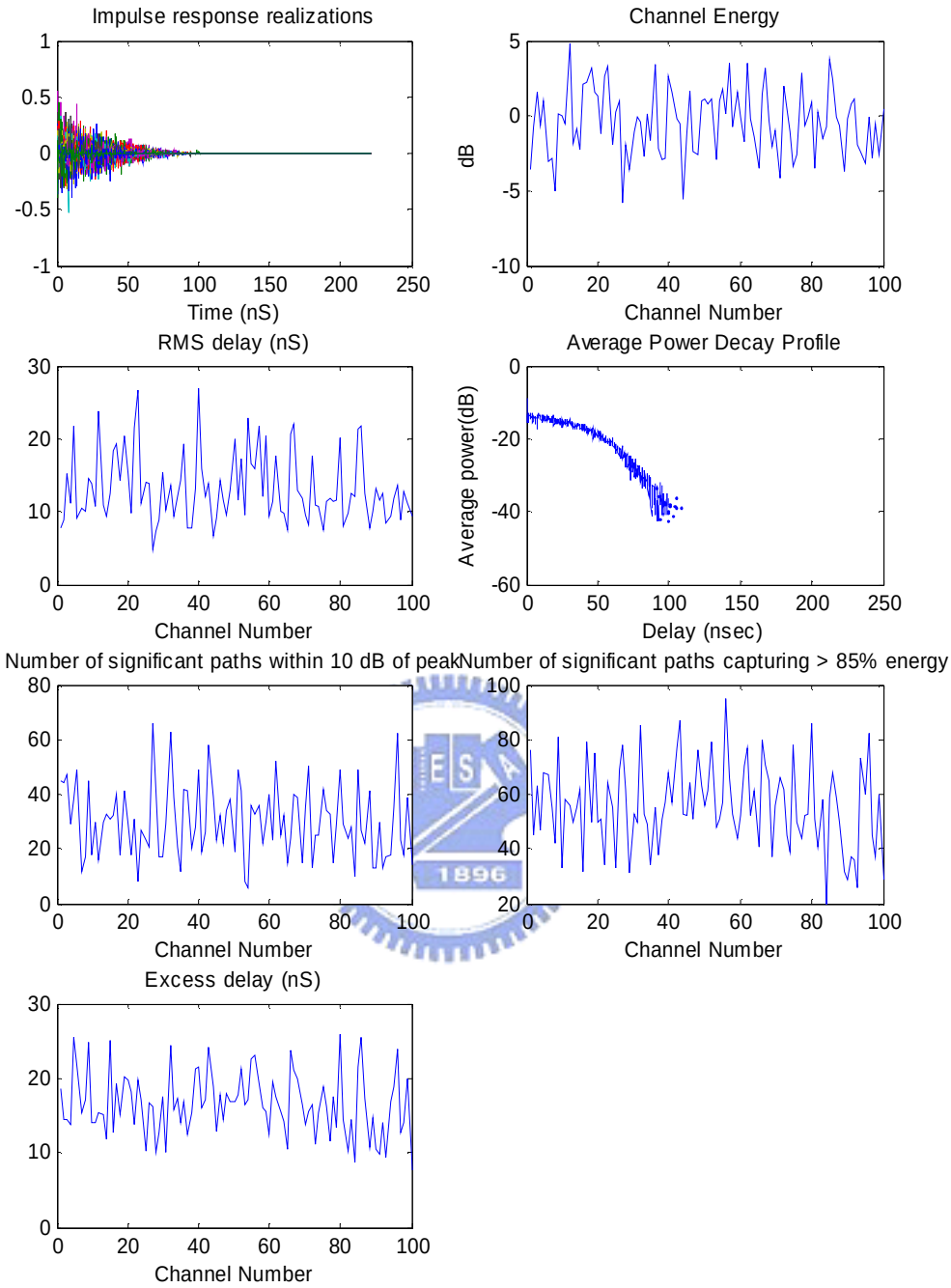


Figure 2.4 CM3 channel realizations

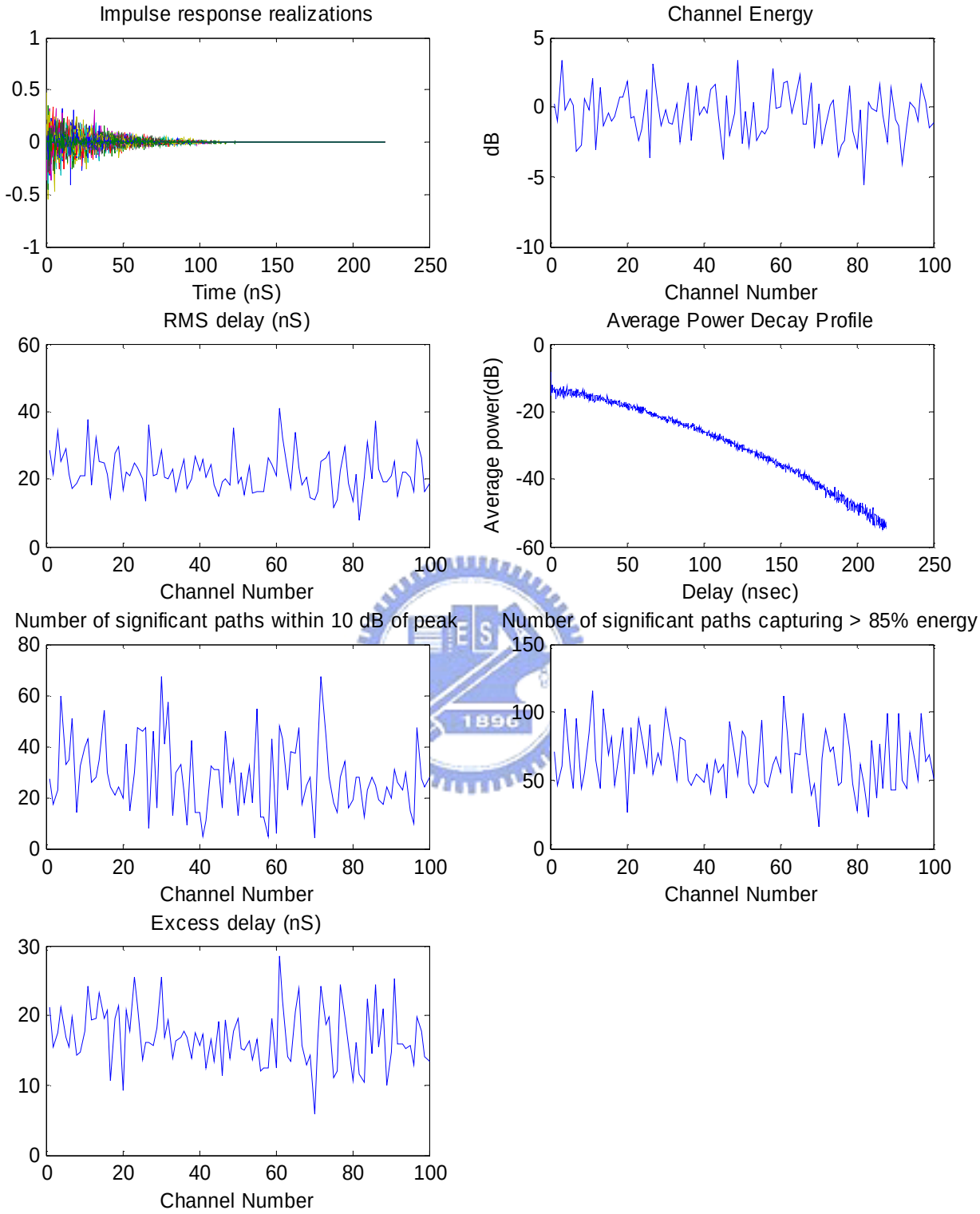


Figure 2.5 CM4 channel realizations

Chapter 3.
A Equalizer design for UWB systems.

In order to propose a low complexity and high speed channel equalizer, CORDIC is used to achieve the target. The CORDIC not only reduce the complexity of phase offset tracking, but also reduce the complexity of channel estimation and CE error tracking. In this chapter, we will discuss about how CORDIC work and how it can reduce the complexity.

3.1. CORDIC algorithm.

A Coordinate Rotation DIgital Computer (CORDIC) algorithm is a well-known iterative method for the computation of vector rotation**.** It simply uses shifters and adders to calculate the length and the angle of the vector in a plane. This algorithm is easy to be improved. Here gives a simple example for CORDIC algorithm used for phase rotation.

Iteration 1 : Let A be a vector in a plane. To rotate A to x-axis, we firstly rotate A by A' vectors. A' is a vector of which the length is the same as A, but orthogonal to A. After the first iteration, the result of vector A_0=A+A' will resident in the opposite part in view of x-axis.

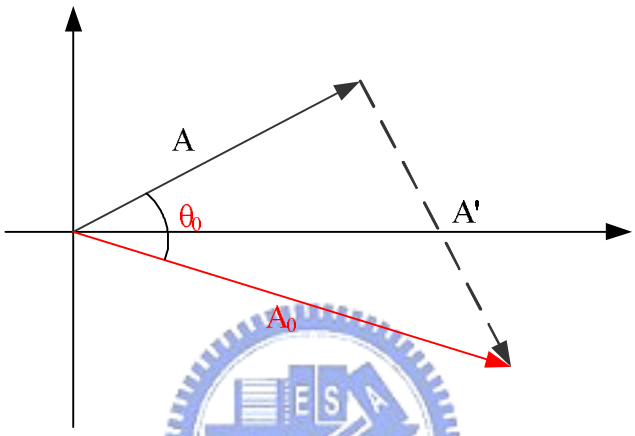


Figure 3.1 - iteration 1

$$
\begin{aligned}
& i = 0 \\
& u_0 = sign[y(0)] = 1 \\
& \begin{bmatrix} x(1) \\ y(1) \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} x(0) \\ y(0) \end{bmatrix} \\
& q_0 = \tan^{-1}(1) \qquad (3.1) \\
& q \cong q_0 \\
& A_0 = A \times \sqrt{1^2 + 1^2} \\
& \Rightarrow A = \frac{A_0}{\sqrt{1^2 + 1^2}}
\end{aligned}
$$

The motion of iteration 1 is shown in Equ. (3.1), where x(0) and y(0) are the x-axis and y-axis of the vector A, and θ is the angle of vector A which is to approximate θ_0 after this iteration.

Iteration 2 : For future approximation, A_0 is shifted to A_0', where A_0' is

orthogonal to A_0,and with length being 1/2 A_0. The rotating angle θ_1 will be $\tan^{-1}(1/2)$ = 22.5°.

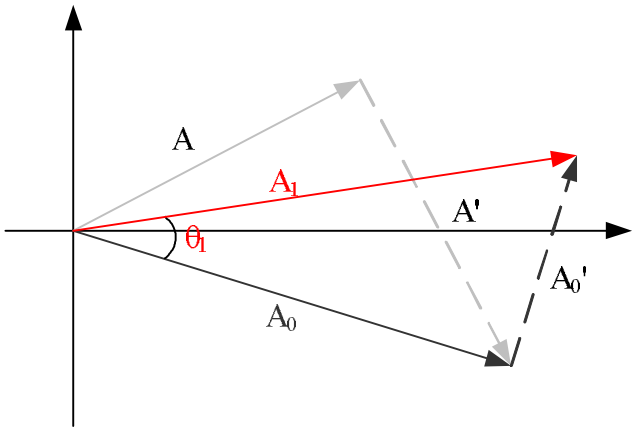


Figure 3.2 - iteration 2

$$i = 1$$

$$u_0 = sign[y(1)] = -1$$

$$\begin{bmatrix} x(2) \\ y(2) \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} x(1) \\ y(1) \end{bmatrix}$$

$$q_1 = \tan^{-1}(1/2) \qquad (3.2)$$

$$q \cong q_0 - q_1$$

$$A_1 = A_0 \times \sqrt{1^2 + (1/2)^2}$$

$$\Rightarrow A = \frac{A_0}{\sqrt{1^2+1^2}} = \frac{A_1}{\sqrt{1^2+1^2} \times \sqrt{1^2 + (1/2)^2}}$$

The motion of iteration 2 is shown in Equ. (3.2), the angle θ now is approximate as θ_0- θ_1 after this iteration.

Iteration 3 : For future approximation, A_1 is shifted to A_1', where A_1' is orthogonal to A_1,and with length being 1/4 A_1. The rotating angle θ_1 will be $\tan^{-1}(1/4)$ = 14.03°.

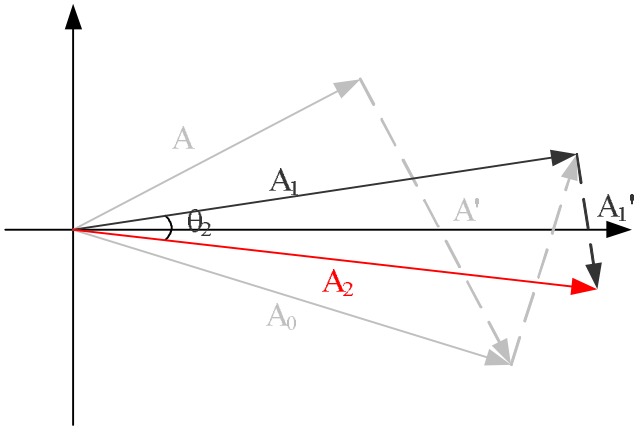


Figure 3.3 - iteration 3

$$i = 2$$

$$u_0 = sign[y(2)] = 1$$

$$\begin{bmatrix} x(3) \\ y(3) \end{bmatrix} = \begin{bmatrix} 1 & 1/4 \\ -1/4 & 1 \end{bmatrix} \begin{bmatrix} x(2) \\ y(2) \end{bmatrix}$$

$$q_2 = \tan^{-1}(1/4)$$

$$q \cong q_0 - q_1 + q_2 \tag{3.3}$$

$$A_2 = A_1 \times \sqrt{1^2 + (1/4)^2}$$

$$\Rightarrow A = \frac{A_0}{\sqrt{1^2+1^2}} = \frac{A_1}{\sqrt{1^2+1^2} \times \sqrt{1^2 + (1/2)^2}}$$

$$= \frac{A_2}{\sqrt{1^2+1^2} \times \sqrt{1^2 + (1/2)^2} \times \sqrt{1^2 + (1/4)^2}}$$

The motion of iteration 3 is shown in Equ. (3.3), the angle θ now is approximate as $\theta_0 - \theta_1 + \theta_2$ after this iteration.

After i iterations, the vector will be closer to x-axis, and the difference vector A in between will be $A-A_i$. The tolerance of the difference can be evaluated by system applications and to facilate the difference evaluation, A can be represented as A_i. The derivative is listed below.

$$u_0 = sign[y(i)]$$

$$\begin{bmatrix} x(i+1) \\ y(i+1) \end{bmatrix} = \begin{bmatrix} 1 & u_i 2^{-i} \\ -u_i 2^{-i} & 1 \end{bmatrix} \begin{bmatrix} x(i) \\ y(i) \end{bmatrix}$$

$$q_2 = \tan^{-1}(2^{-i})$$

$$q = q_0 - q_1 + q_2 + ... = \sum_i u_i q_i \tag{3.4}$$

$$A_{i-1} = A_i \times \sqrt{1^2 + (2^{-i})^2}$$

$$A = \frac{A_0}{\sqrt{1^2+1^2}} = \frac{A_1}{\sqrt{1^2+1^2} \times \sqrt{1^2+(1/2)^2} \times .....}$$

$$= \frac{A_i}{\prod_i k_m(i)} \qquad k_m(i) = \sqrt{1^2 + (2^{-i})^2}$$

From the equation, each iteration of CORDIC can simply be implemented as shifters and adders. The structure is shown in figure 3.4 and figure 3.5

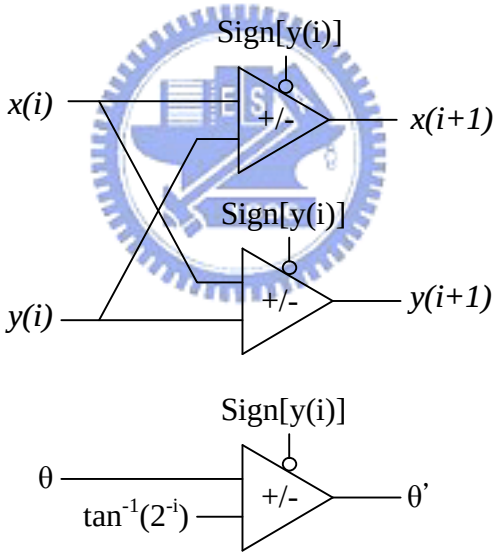


Figure 3.4 - The structure of CORDIC (one iteration)

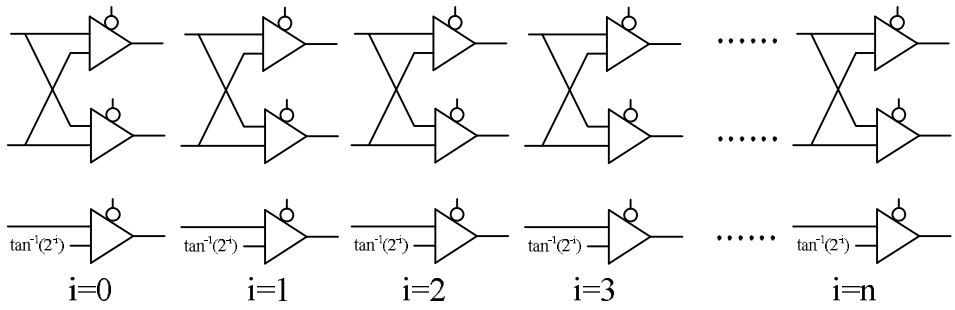


Figure 3.5 - The structure of CORDIC (n iterations)

The advantage of CORDIC is that it can be implemented as pipeline to increase throughput. And it doesn't need any multiplier so it can achieve area efficiency. In order to meet UWB specification, 10 stages are designed and clock latency is 11.

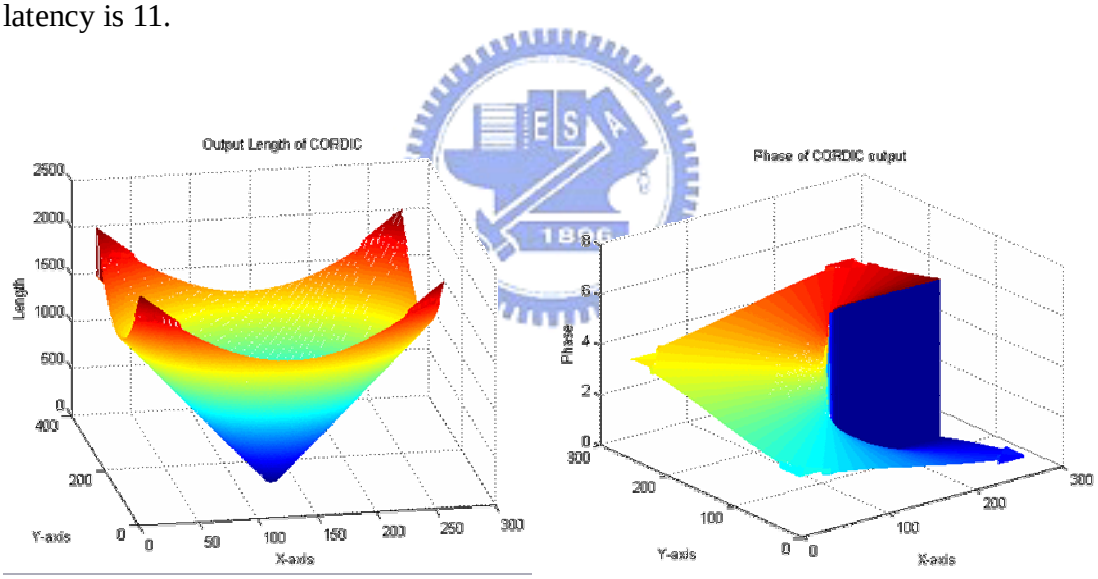


Figure 3.6 - CORDIC output

CORDIC has some drawbacks, that the phase being derived by CORDIC is only approximate. Figure 3.7 shows the phase error of CORDIC output. From the figure we can know, if the length of input vector is too short (less than 2 unit), the phase of CORDIC output will cause large error. The solution is to add some extra bits

in LSB (as fig 3.x shows), which also means to add the resolution.

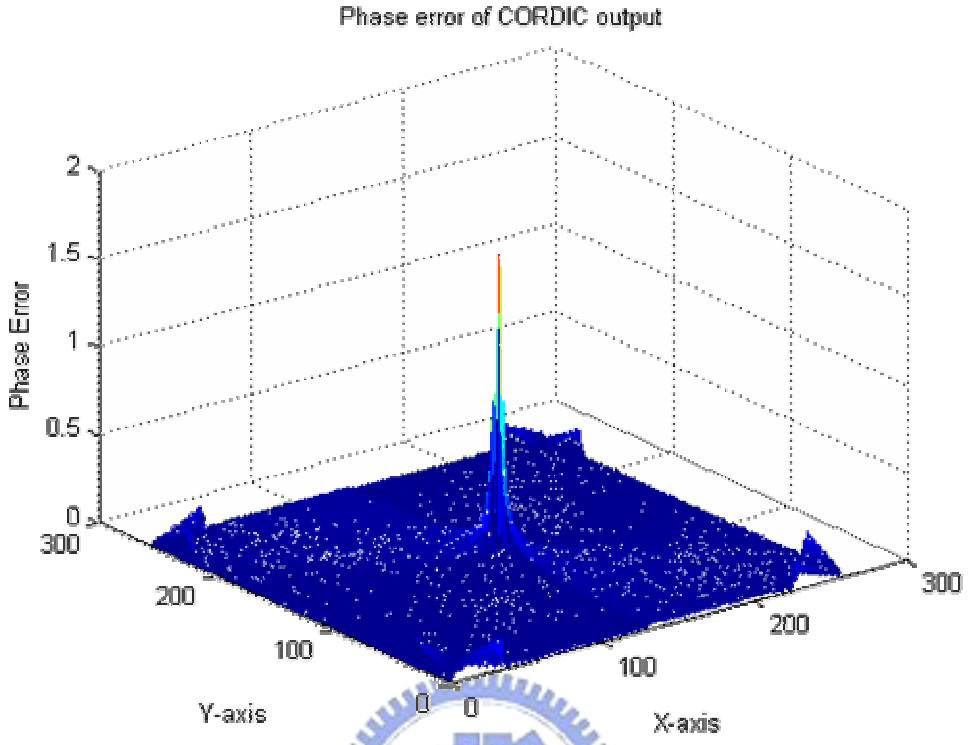


Figure 3.7 - Phase error of CORDIC output

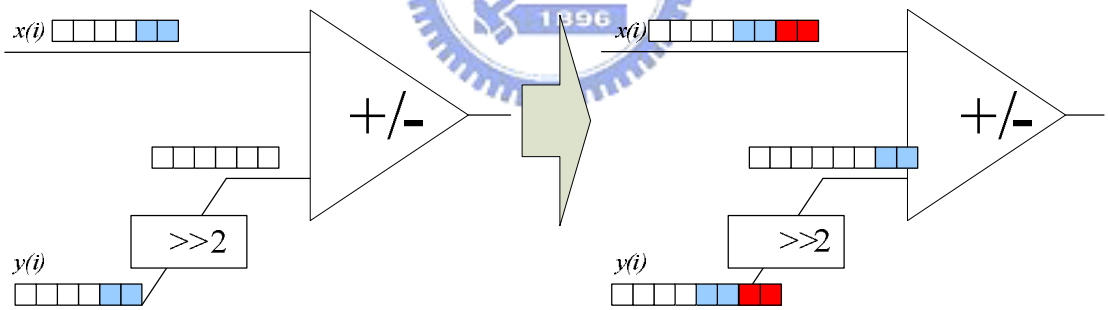


Figure 3.8 – The solution of phase error cause by low magnitude

3.2. Equalization algorithm.

Multi-path fading is one of the data distortion issues in OFDM system. It also generates Inter-symbol interference (ISI) and inter-carrier interference (ICI) to destroy the system performance. In ultra wide-band system, guard interval (GI) is used for

each OFDM symbol to against ISI. However, ICI arises and produces interference between different sub-channels. To eliminate ICI

The channel frequency response (CFR) of multi-path fading environment is also called as a frequency-selective fading. In ultra wide-band, two preambles are used to estimate the fading channel. Here I use zero forcing (ZF) channel estimation algorithm to estimate the channel. The Zero forcing channel estimation and equalization can be derived as follow:

- *channel estimation*:

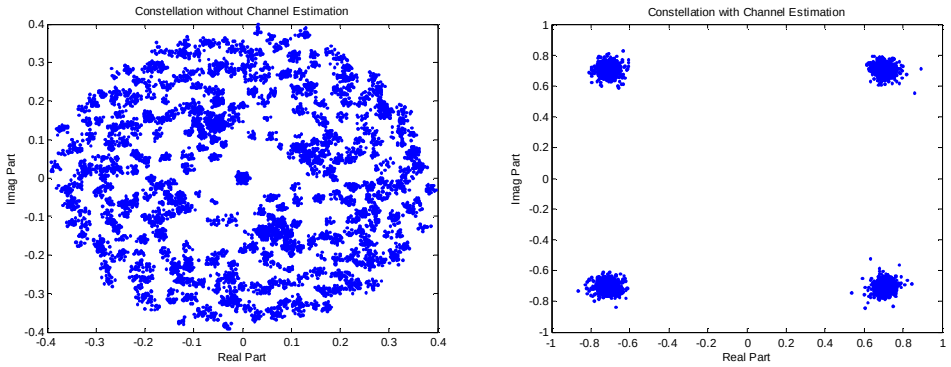
$$\begin{aligned} R_{1,k} &= X_k \cdot H_k + N_{1,k} \\ R_{2,k} &= X_k \cdot H_k + N_{2,k} \\ \tilde{H}_k &= \frac{R_{1,k} + R_{2,k}}{2X_k} = \frac{H_k + H_k}{2} + \frac{N_{1,k} + N_{2,k}}{2X_k} = H_k + N_k \end{aligned} \tag{3.5}$$

- *Equalization*:

$$\hat{y}_{l,k} = \frac{R_{l,k}}{\tilde{H}_k} = \frac{D_{l,k} \cdot H_k + N_{l,k}}{H_k + N_k} = D_{l,k} \cdot \frac{H_k}{H_k + N_k} + N'_{l,k} \tag{3.6}$$

In equation (3.5), $R_{1,k}$ and $R_{2,k}$ means the two received long preamble signals. X_k is the long training symbol which specified in ultra wide-band specification. H_k is the estimated channel response. $N_{1,k}$ and $N_{2,k}$ are noises in the channel. N_k is the channel estimation error which comes from channel noise $N_{1,k}$ and $N_{2,k}$.

Equ. (3.6) is the equalize equation. From the equation we can see the channel estimation error will deeply distort the data, so the channel estimation error tracking is used to fix the channel estimation (CE) error [5].



(a) (b)

Figure 3.9 - QPSK constellation : (a) without CE (b) with CE

Based on IEEE 802.15.3a specification, two preambles are used to estimate channel, but according to equ. 3.5, the noise will distort the estimated channel [11], as the fig. 3.10 shows. The ideal CFR is a smooth curve, so in the propose design, a low pass filter is used to smooth the estimated channel, and make the CE error smaller. The smoothed filter is realized by 3-tap because the channel model CM2, CM3 and CM4 swing acutely.

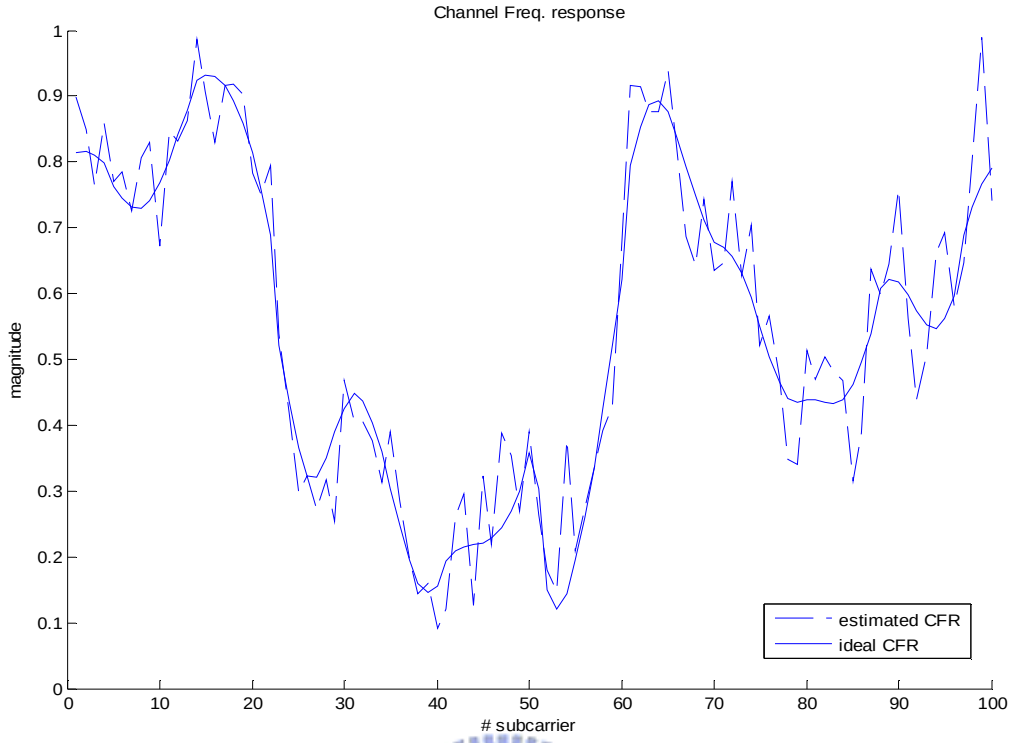


Figure 3.10 – Channel estimation (CE) error

3.2.1 Channel estimation error tracking

The idea of The CE error tracking algorithm comes from the least-mean-square (LMS) algorithm. It works on the basis of the update equation.

$$\tilde{G}_{l+1,k} = \tilde{G}_{l,k} - m\nabla^{C}_{\tilde{H}} \mid e_{l,k} \mid^2 \qquad \tilde{G}_{l,k} = 1/\tilde{H}_{l,k} \tag{3.7}$$

Where $\nabla^{C}_{\tilde{H}}$ denotes complex gradient operator, $e_{l,k}$ is the error vector between estimated vector $\hat{y}_{l,k}$ and predict vector $d_{l,k}$:

$$e_{l,k} = d_{l,k} - \hat{y}_{l,k} \tag{3.8}$$

Replacing $|e_{l,k}|^2$ by $e_{l,k} \cdot e^{*}_{l,k}$, then we can obtain

$$\begin{aligned} \tilde{G}_{l+1,k} &= \tilde{G}_{l,k} - m\nabla^{C}_{\tilde{H}} e_{l,k} \cdot e^{*}_{l,k} = \tilde{G}_{l,k} - m(2e^{*}_{l,k} \cdot R_{l,k}) \\ &= \tilde{G}_{l,k} - 2me^{*}_{l,k} \cdot R_{l,k} \end{aligned} \tag{3.9}$$

Notice that $d_{l,k}$ is just a predict vector. The prediction may be wrong when the signal to noise ratio (SNR) is small. So the trust area is defined to reduce the wrong prediction. When the estimated vector is in the place out of the trust area, the CE error tracking will stop working (μ =0), otherwise, the CE error tracking will work as definition.

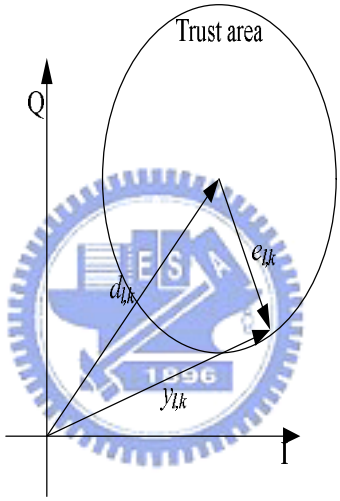


Figure 3.11 – The Trust area definition

The following figure shows the CE error before and after CE error tracking, the channel estimation error is reduced after CE error tracking.

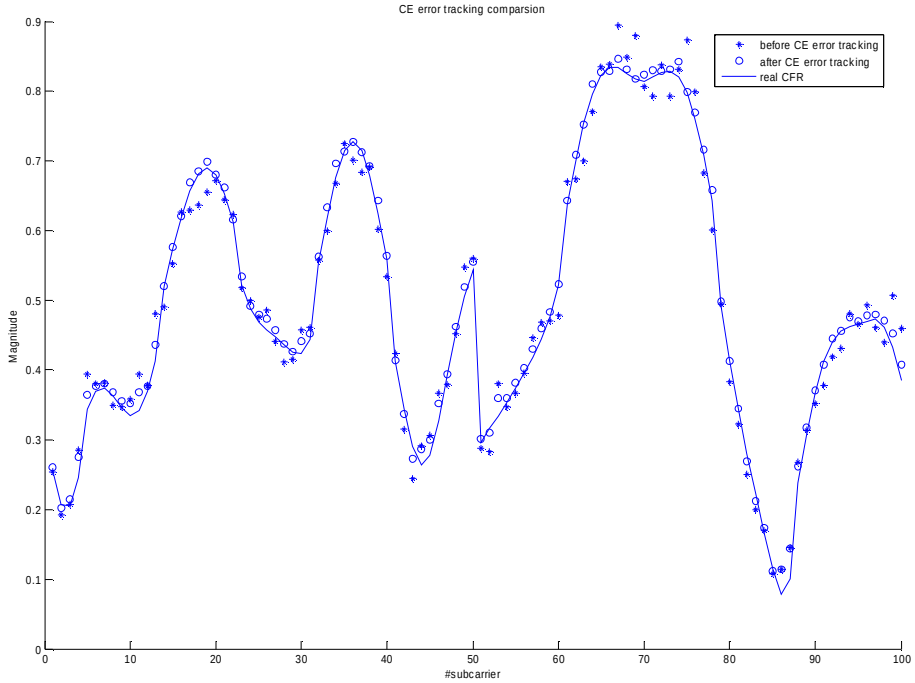


Figure 3.12 - CE error comparison

3.3. The CORDIC based Equalization algorithm

The CORDIC based equalizer works in polar-coordinate system. So the zero forcing algorithm has to do some change to fit the system [6]. The Zero forcing channel estimation and equalization in polar-coordinate can be derived as follow:

- *channel estimation*:

$$R_{1,k} = X_k \cdot H_k + N_{1,k}$$
$$R_{2,k} = X_k \cdot H_k + N_{2,k} \quad (3.10)$$
$$\arg(\tilde{H}_k) = \frac{\arg(R_{1,k}) + \arg(R_{2,k})}{2} - \arg(X_k)$$
$$abs(\tilde{H}_k) = \frac{abs(R_{1,k}) + abs(R_{2,k})}{2}$$

- *equalization*:

$$\arg(\hat{y}_{l,k}) = \arg(R_{l,k}) - \arg(\tilde{H}_k) \quad (3.11)$$
$$abs(\hat{y}_{l,k}) = abs(R_{l,k}) / abs(\tilde{H}_k)$$

Where the function of arg(X) equals the angle of X, the function of abs(X) equals the absolute value of X. Notice that there are difference between the estimated channel in polar-coordinate system and Cartesian coordinate system. As shown in fig. 3.13. the amplitude of $\tilde{H}_k$ is shorter than the practical value.

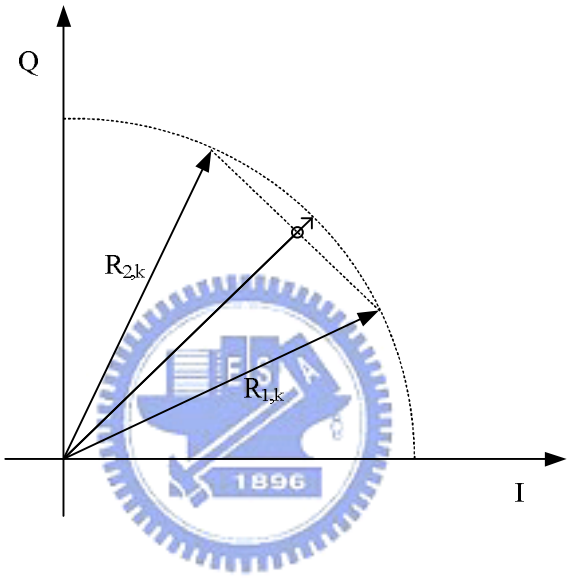


Figure 3.13 – Illustration of channel estimation

The vectors multiplication and division become addition and subtraction of phases, so the computation complexity of channel estimation and equalization in the polar coordinate system (equ. 3.5 and equ 3.6) are less complex than one in Cartesian coordinate system (equ. 3.10 and equ. 3.11).

3.3.1. The CORDIC based Channel Estimation Error Tracking

In the polar coordinate system. Same update equation is used for CE error

tracking.

$$\arg(\tilde{\tilde{H}}_{l+1,k}) = \tilde{\tilde{H}}_{l,k} - m\nabla_{\tilde{\tilde{H}}} \mid e_{l,k} \mid^2 \tag{3.12}$$

Where $\nabla_{\tilde{\tilde{H}}}$ denotes gradient operator, $e_{l,k}$' is the error vector between estimated angle $\arg(\hat{y}_{l,k})$ and predict angle $\arg(d_{l,k})$:

$$e_{l,k}' = \arg(d_{l,k}) - \arg(\hat{y}_{l,k}) \tag{3.13}$$

Finally, equ. (3.12) can become:

$$\begin{aligned} \arg(\tilde{\tilde{H}}_{l+1,k}) &= \tilde{\tilde{H}}_{l,k} - m\nabla_{\tilde{\tilde{H}}} \mid e_{l,k}' \mid^2 \\ &= \tilde{\tilde{H}}_{l,k} + m(2e_{l,k}') \end{aligned} \tag{3.14}$$

The computation complexity of channel estimation error tracking in the polar coordinate system (equ. 3.14) are also less complex than the one in Cartesian coordinate system (equ. 3.9). The definition of trust area is also change (shows in Figure 3.13), when the estimated phase is between π/8 ~3π/8, and the length is between 0.5~1.33, then estimated vector would be trust and the CE tracking will be working.

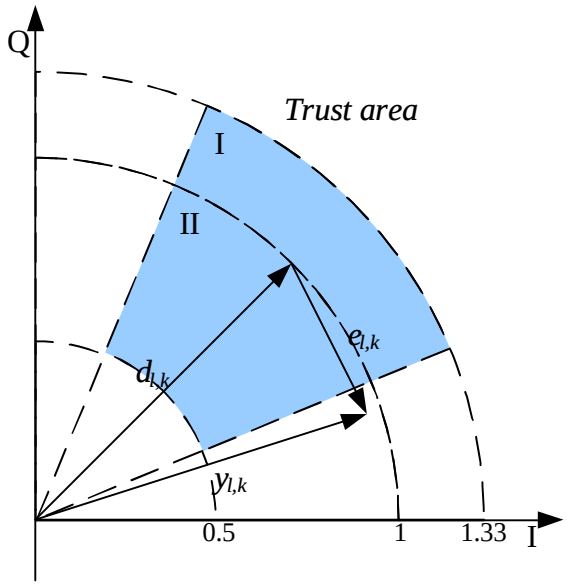
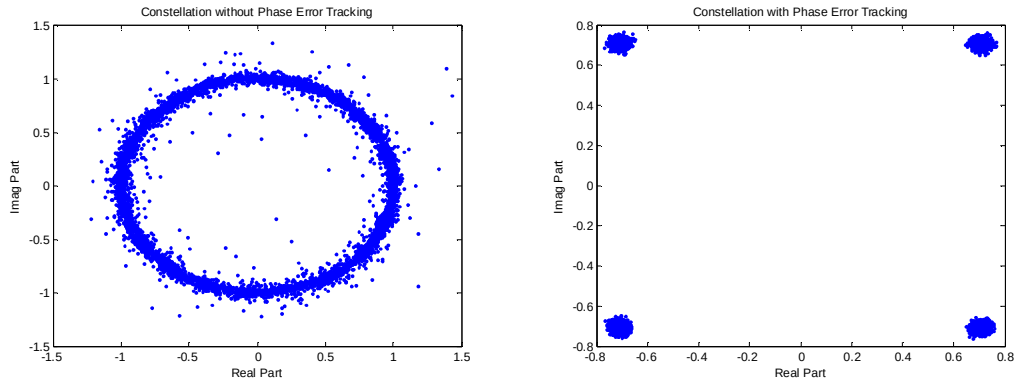


Figure 3.14 – The Trust area definition in polar coordinates CE tracking

3.4. Phase Error Tracking

Carrier Frequency offset (CFO) and sampling clock offset (SCO) are the other two major data distortion issues in OFDM systems which are cause by crystal oscillator frequency mismatch and digital-to-angle converter (DAC) angle-to-digital converter (ADC) mismatch. CFO and SCO cause data rotation in frequency domain and received data incorrect. Phase error tracking (PET) is generally applied to trace the phase rotation; Fig. 3.15 shows the QPSK constellation with and without PET.



(a) **(b)**

Figure 3.15 - QPSK constellation : (a) without PET (b) with PET

3.4.1. Carrier Frequency Offset Tracking

Let S_n be the base band transmitted signal and can be expressed as [7]

$$s_n = 1/N \sum S_k e^{j(2pkn)/N} \tag{3.15}$$

Let h_n be the channel impulse response and $x_n = s_n \otimes h_n$. After receiver down converts the signal with a carrier frequency f_r, the received complex baseband signal C_n can be expressed as

$$\begin{aligned} c_n &= x_n \exp(j2pf_t nT)\exp(-j2pf_r nT) \\ &= x_n \exp(j2p(f_t - f_r)nT) \\ &= x_n \exp(j2pf_\Delta nT) \end{aligned} \tag{3.16}$$

Where f_Δ and T is the difference of transmitter carrier frequency and receiver carrier frequency. The CFO will cause the OFDM symbol rotation, like the fig 3.15 shows, the phase error increase when the symbol index *l* increase:

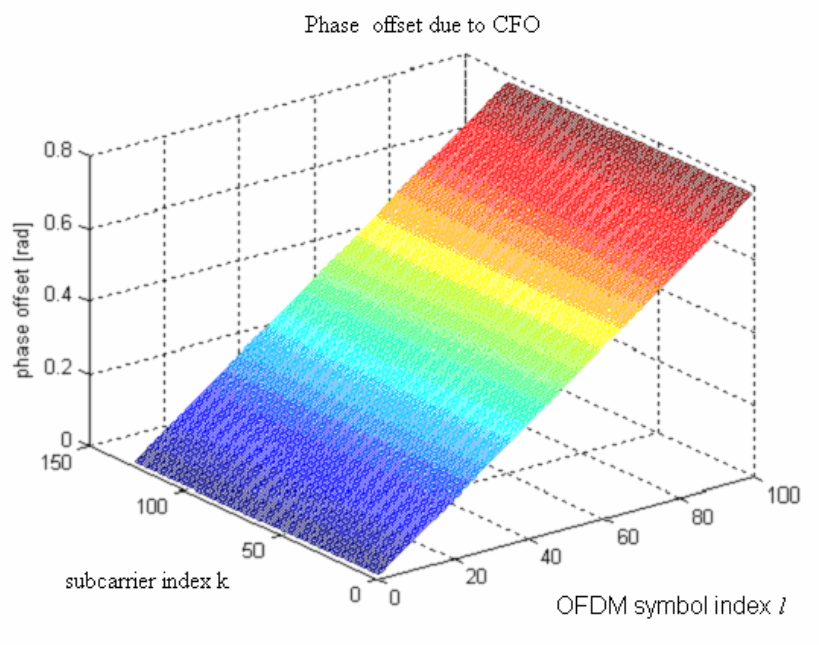


Figure 3.16 – Phase offset due to CFO

The standard specifies the maximum oscillator frequency error is +/- 20 ppm. Thus if the transmitter and the receiver oscillator both have the maximum allowed error, but with opposite sign. The total error will be 40ppm. The carrier frequency specified in ultra wide-band is about 3960 MHz, therefore the maximum frequency error f_{Δ} =3960 * 40 =158.4 KHz. At receiver, short and long preamble signals can be used to perform coarse and fine CFO acquisition.

CFO causes the OFDM symbol rotate, so the phase shift between two preambles $R_{1,k}$ and $R_{2,k}$ are reasonably caused by CFO. Here we use average phase shift of two preambles to be the initial value of CFO.

$$\hat{q}_0 = \frac{1}{N}\sum_{k=1}^{N} \arg(R_{2,k}) - \arg(R_{1,k}) \qquad (3.18)$$

Where $\hat{q}_0$ is estimated CFO, and it should be $2pf_\Delta$. Since the channel estimation takes average of two preamble signals, so the phase shift of the first OFDM symbol will be $1.5\hat{q}_0$. Fig. 3.17 shows phase shift caused by CFO.

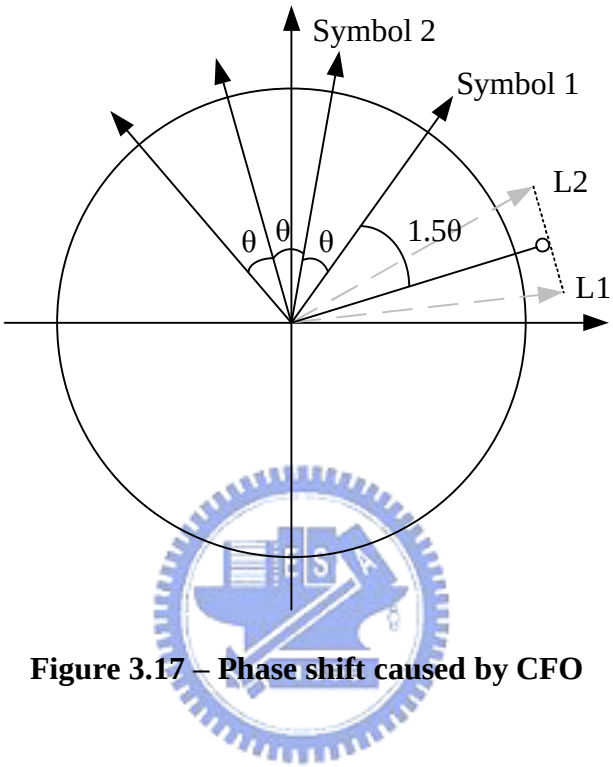


Figure 3.17 – Phase shift caused by CFO

During the signal transmission, 12 pilot signals can be used to adaptive the value θ. The tracking algorithm of $\hat{q}_0$ proposed here can be written as

$$\hat{q}_l = \hat{q}_{l-1} + a\frac{1}{12}\sum_k \arg(\hat{y}_{l,k}) - \arg(P_{l,k}) \qquad (3.19)$$
$$k = -55,-45,-35,-25,-15,-5,5,15,25,35,45,55$$

Where α is adaptive constant for CFO, $P_{l,k}$ are desired signals that specified.

3.4.2. Sampling Clock Offset Tracking

The normalized SCO can be expressed as

$$T_\Delta = \frac{T_r - T_t}{T_t} \tag{3.20}$$

Where T_t and T_r are the sampling period at transmitter and receiver, respectively.

The effect on received signal after DFT can be shown as

$$\begin{aligned} C'_{l,k} &= S_{l,k} H_k e^{j(2\pi klT_\Delta \frac{T_S}{T_u})} \sin c(\pi kT_\Delta) \\ &\overset{kT_\Delta << 1}{\approx} S_{l,k} H_k e^{j(2\pi klT_\Delta \frac{T_S}{T_u})} \\ &\approx S_{l,k} H_k e^{j(2\pi klf)} \end{aligned} \tag{3.21}$$

where T_s and T_u are OFDM period and FFT integration period, respectively. Beside ICI, SCO also rotates sub-channel signal and the amount of phase shift is function of symbol index *l* and sub-channel index *k*, as fig. 3.18 shows.

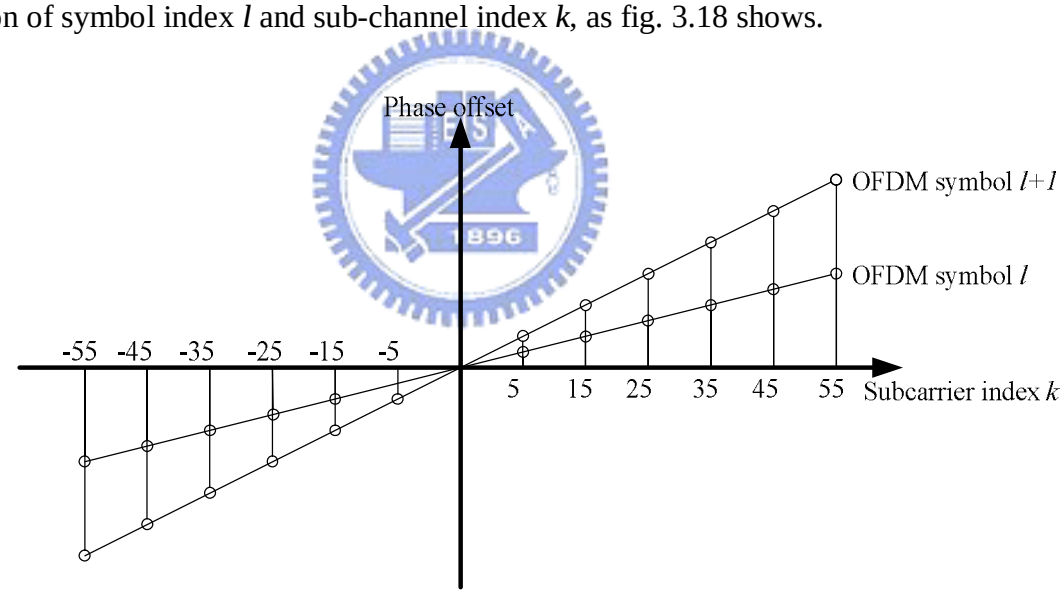


Figure 3.18 – Phase offset due to SCO

Two long preambles can help us to estimation the SCO offset and compensate for it. The estimation of $\tilde{f}_0$ can be expressed as follow

$$\tilde{f}_0 = \frac{1}{57\times 56}\left\{\sum_{k=1}^{56}[\arg(R_{2,k}) - \arg(R_{1,k})] - \sum_{k=-56}^{-1}[\arg(R_{2,k}) - \arg(R_{1,k})]\right\} \quad (3.22)$$

During the signal transmission, 12 pilot signals are also used to adaptive the value. The tracking algorithm of $\tilde{f}_l$ proposed here can be written as

$$e_l = \frac{1}{6\times 60}\left[\sum_{k=55,45,35,25,15,5}\arg(\hat{y}_{l,k}) - \arg(P_{l,k}) - \sum_{k=-55,-45,-35,-25,-15,-5}\arg(\hat{y}_{l,k}) - \arg(P_{l,k})\right] \quad (3.23)$$
$$\tilde{f}_{l+1} = \tilde{f}_l + e \cdot e_l$$

Where ε is adaptive constant for SCO, $P_{l,k}$ are desired signals that specified.

Chapter 4.
Implementation and Verification

4.1. Architecture of the proposed equalizer.

By using the equalizer scheme as described in chapter 3, we will discuss the implementation of equalizer. Fig. 4.1 shows the function block of the proposed equalizer.

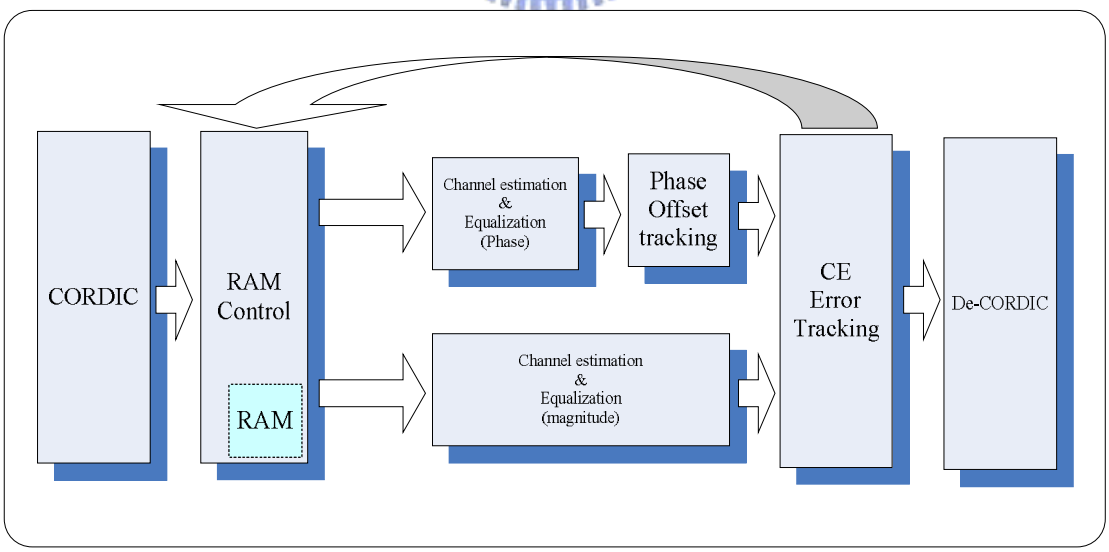


Figure 4.1 – function block of the processed equalizer.

4.1.1. Architecture of the CORDIC based Equalizer.

The architecture of the proposed channel equalizer is illustrated in fig. 4.2. In the proposed design, the architecture spilt into two parts, one is phase, the other one is magnitude. The magnitude part is simply implemented as a divider with 5 clock latency. The phase part is much complexity and will be discuss in the follow section.

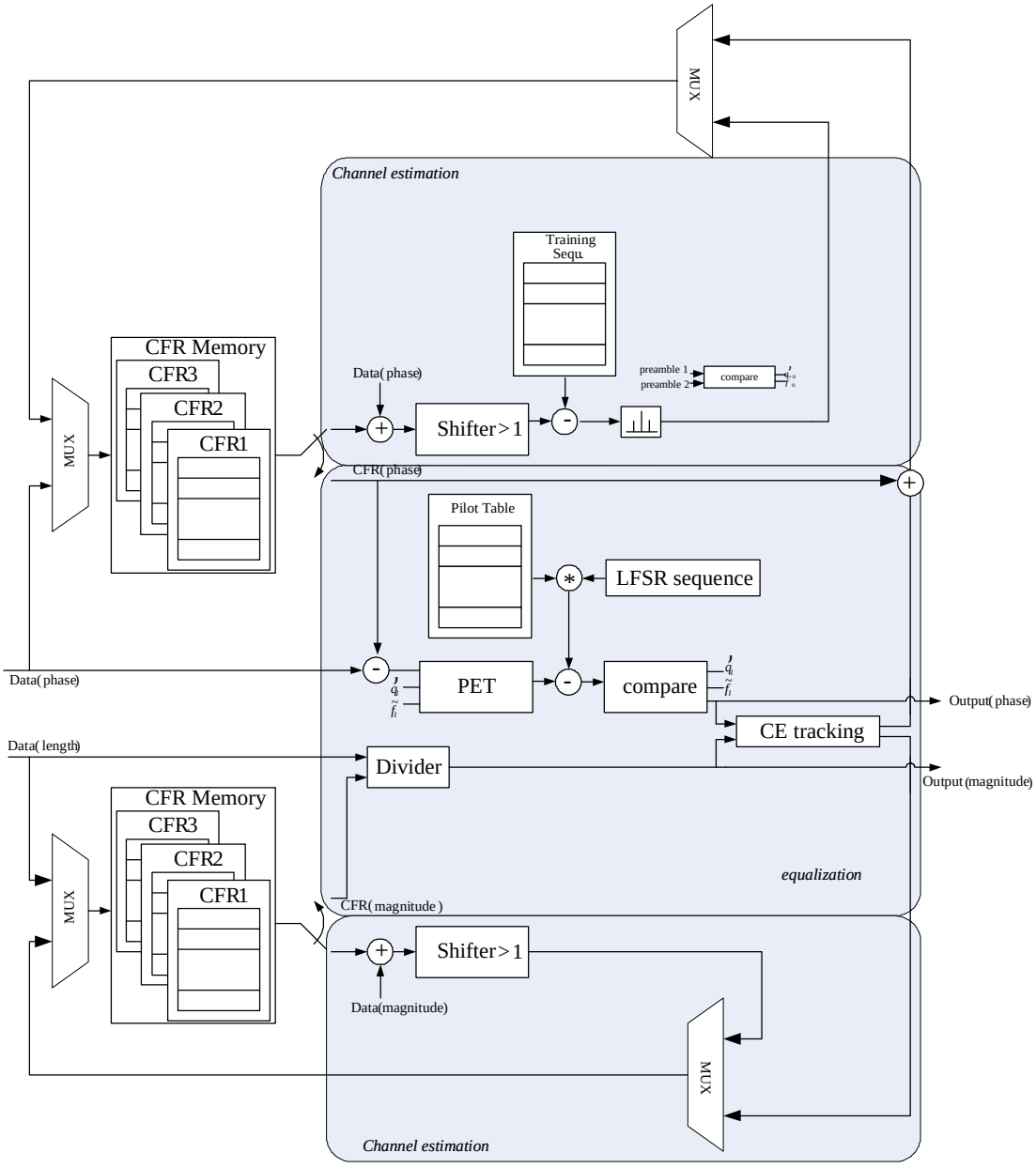


Figure 4.2 - The architecture of the proposed equalizer

4.1.1.1 Architecture of RAM control

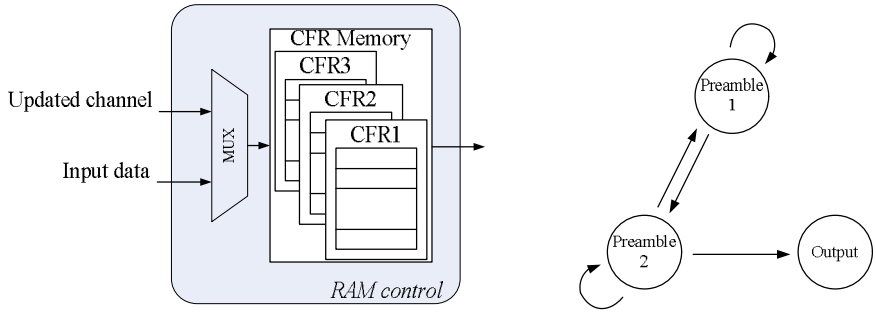
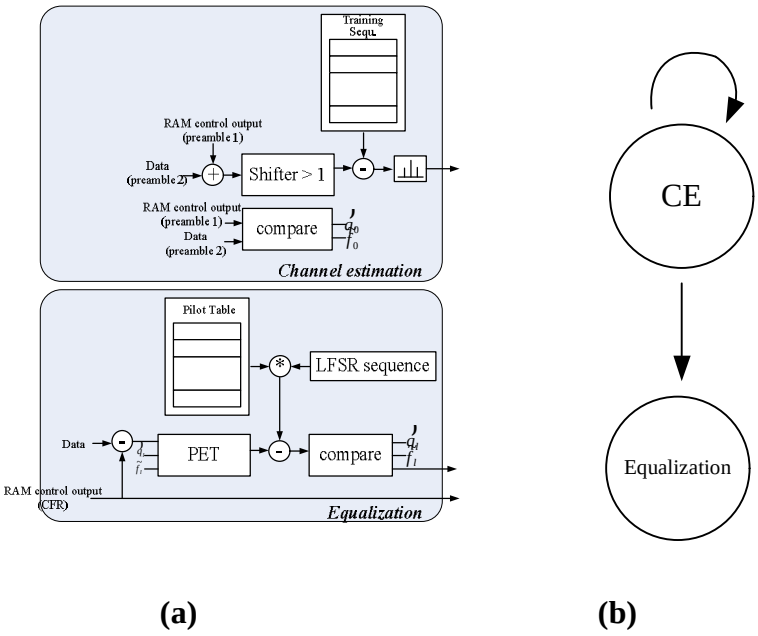


Figure 4.3 – RAM control module (a) Architecture, (b) finite state machine

Fig. 4.3 illustrated the architecture of the proposed RAM control. The function of RAM control module is to store the channel frequency response (CFR) in the memory. When the first preamble arrived, it will be stored in memory. When the second preamble is arrived, both preambles will send to the "channel estimation" block, then the estimated channel will be calculated and store in CFR memory.

4.1.1.2 Architecture of CE & PET (phase)



(a) **(b)**

Figure 4.4 – CE & PET module (a) Architecture, (b) finite state machine

Fig. 4.4 illustrated the architecture of the CE & PET module, the module is a finite state machine with two states. In CE state, channel is estimated and phase offset is also been tracked. In equalization state, the module will do data equalization and adaptive phase error tracking.

4.1.1.3 Architecture of CE error tracking

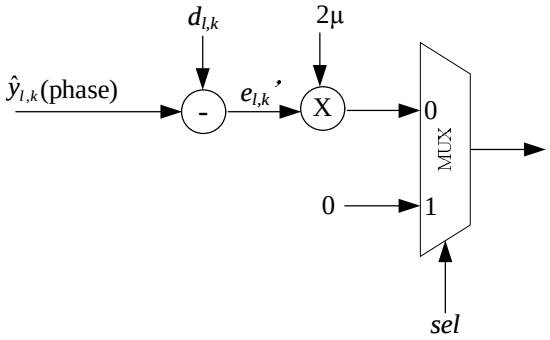


Figure 4.5 – The architecture of the CE error tracking

Fig. 4.5 illustrated the architecture of the CE error tracking. It is simply implemented as a combinational circuit. Sel=0 When $\hat{y}_{l,k}$ is in the trust area, and the output will be 2 μ $e_{l,k}$', otherwise, the output will be 0 in order to stop CE adaptation.

4.1.1.4 Architecture of CE (magnitude)

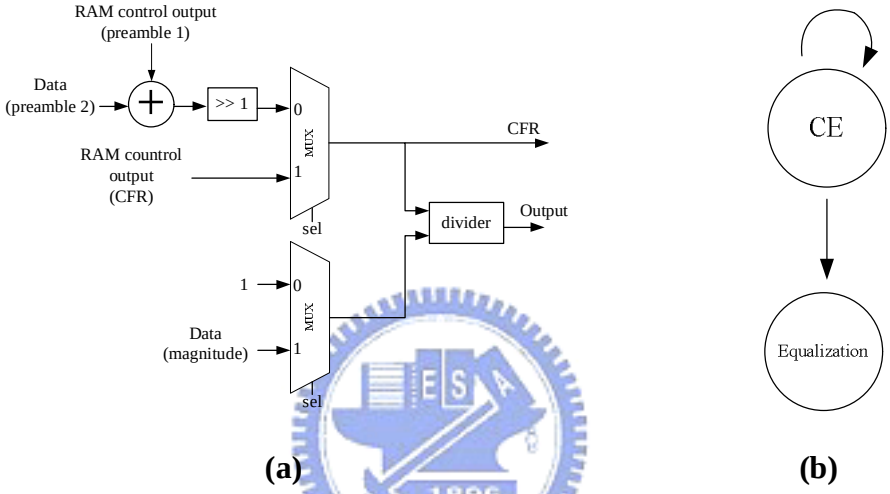


Figure 4.6 – CE module (a) Architecture, (b) finite state machine

The architecture of CE in magnitude is only 2 multiplexers and 1 divider (as the fig 4.6 shown). In state CE, sel is equal to 0, and the output CFR will be the estimated channel, again the estimated channel will be store in RAM control. In state "equalization", sel is equal to 1, the data will go through the divider and output the equalized data.

4.1.2. Architecture of the CORDIC

With the original CORDIC algorithm, the range of the phase to be detected should between -π ~ π, which will be hard to express in 2's complement. Also, the angular adder can not be implemented by conventional adder and should be redesign. In the proposed design, the range of the angle is normalized with the 2/π, therefore, the range of the phase will be normalized from -2 to 2. The normalized phase is as shown in Fig. 4.7. It can be shown that the phases can be easily represented as 2's complement form.

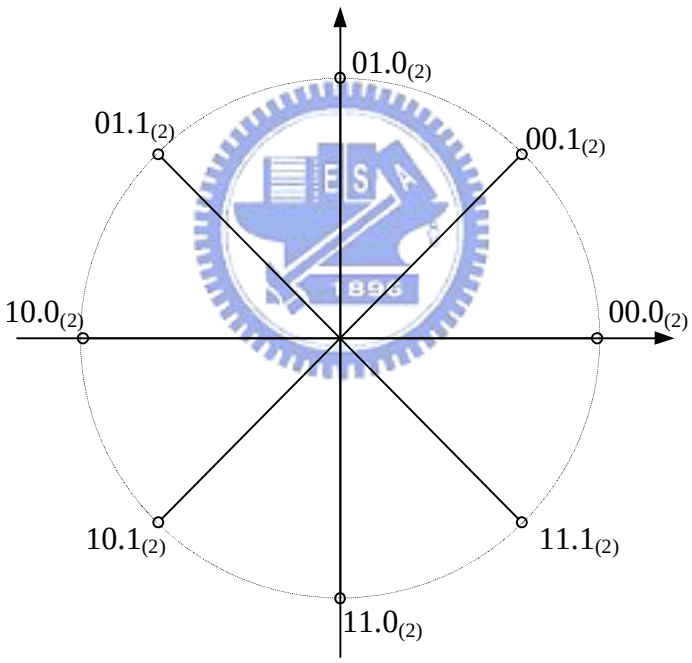


Figure 4.7 – The normalized phase

Besides, with the normalized phases, the adder does not have to be redesigned due to the proposed methodology. Even the overflow will happen, the result still accuracy. For example, the conventional calculation result of π/2 + 3π/4 = 5π/4 (=

-3π/4), corresponsively, the proposed calculation result have same result of $01.0_{(2)}$ + $01.1_{(2)} = 10.1_{(2)}$.

The other advantage is that, the proposed methodology can easily tell which quadrant does vectors belong to. It will reduce the complication of CE error tracking and phase error tracking.

In the de-CORDIC design, only 5-stage is needed because the resolution connecting with Viterbi decoder needs three bits.

4.2. Implementation issues

Hardware cost and system performance are trade-off in hardware implementation, so the fixed-point simulation will be needed before the implementation [8]. the following figure (Fig. 4.8) shows the fixed-point simulation result.

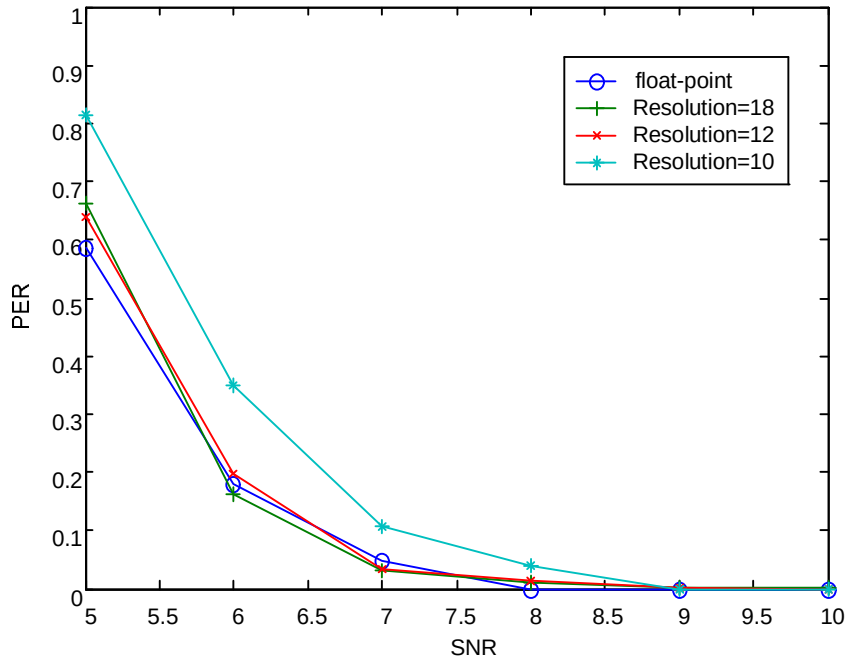


Figure 4.8 – PER analysis with different word-length

According to the figure 4.8, when the resolution is lower than 12, the system performance will be decrease critically, so 12-bit resolution are chosen in the design.

In UWB system, clock rate 528 Mhz will be needed to meet the throughput rate 480Mbits/s, but it is too fast for logical design to approach it, so parallel circuit will be used to make the clock rate lower. The following table is the comparison between 2 parallel circuits and 4 parallel circuits.

Table 4.1 – the comparison between different parallel circuits

	Clock rate	Area	Power
2 parallel circuits	264Mhz	51893 (54% CORDIC; 46% Equalizer)	N/A
4 parallel circuits	132Mhz	88390 (59% CORDIC; 41% Equalizer)	69.3826 mW

As the table shows, 2 parallel circuits only save about 30000 gate counts in hardware implementation. Although 2 parallel circuits design has lower area, 132 MHz is the major clock rate in our system integration. In order to reduce the complexity of system implementation, 4 parallel circuits design are chosen to be implemented.

4.3. Hardware synthesis

In this section, we discuss the implementation of the proposed equalizer design. We use SYNOPSYS design compiler to synthesize the register-level verilog file with UMC 0.18 μm slow library. The gate counters and the critical path delay of each module is shown in table 4.2, respectively.

Table 4.2 – Synthesis reports for each module

Module Name	Gate count	Max. Path Delay (ns)
CORDIC (x4)	39450	5.57
De-CORDIC(x4)	12706	5.25
Ram_control	4648	5.18
Equalizer_phase	16456	5.66
Equalizer_length	16303	5.64

4.4. Soft IP Qualification

IP qualification is the key of SOC. As SOC become popular, the qualification of IP is more important. In this study, we also discuss about the IP qualification (IPQ). IPQ defined the coding style. The verilog codes which follow the IPQ may be easier to understand. Table 4.3 shows the result of IP qualification.

Table 4.3 – The result of IP qualification

	Before Modification	After Modification
Error	858	0
M1 & M2	1303	259

In our design, 251 warnings come from naming convention rule NC.7-1, which defined as use consistent signal names throghout the hierarchy. The rule can not be avoided if the circuit use repeatedly in a design. The fig. 4.9 shows the detail information of IPQ.

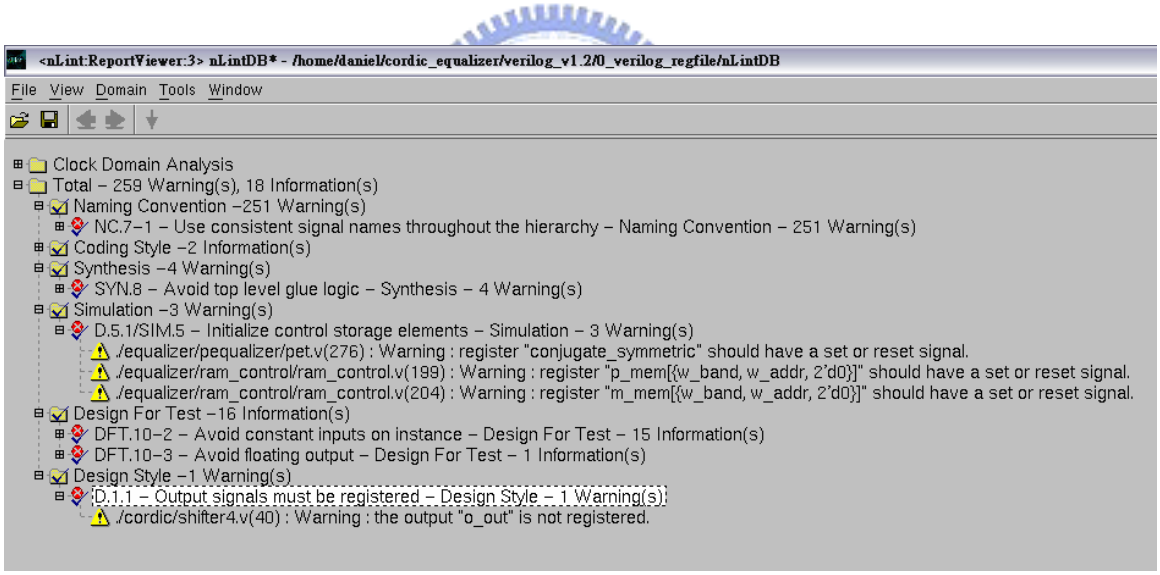


Figure 4.9 – The detail information of IPQ

In IP qualification, reasonable test patterns are needed for verification. The code coverage, which means the percentage of the verified design is checked in different verifying methodology, is used here to show how reasonable the test pattern is. In our

design, the code coverage of statement coverage, branch coverage and toggle coverage are almost 100%. The result is illustrated in fig. 4.10, and the table 4.4 list the met soft IP qualification.

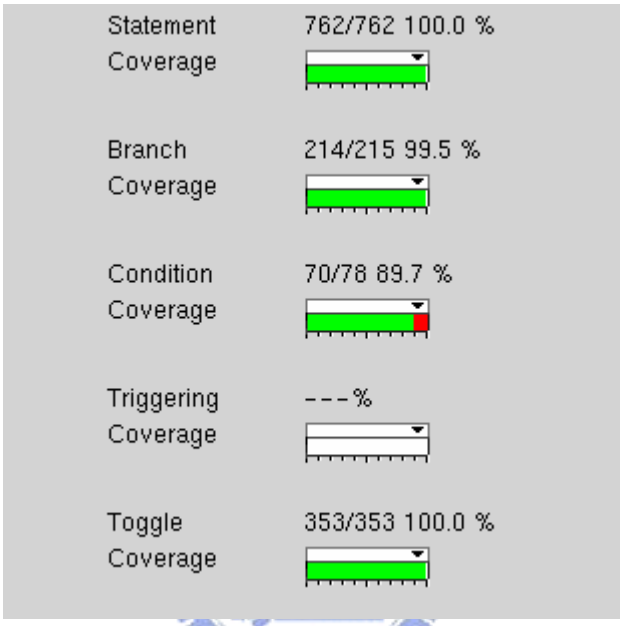


Figure 4.10 – The code coverage of test patterns

Table 4.4 – The met soft IP qualification

	Soft IP	IP Designer Self-assessment
Verification		
[S.VG.1] verification plan	M1	y
[S.VG.1.1] RTL dynamic simulation	M1	y
[S.VG.1.2] All timing exceptions must be identified	M2	y
[S.VG.2] Code coverage must be conducted and the coverage metrics must be documented and delivered.	M2	y
[S.VG.3] All response checking must be done automatically	M2	y
The rules of writing testbench		
[S.TB.1] testbenches must begin with a header	M2	y
[S.TB.2] Testbenches must be written with comments	R	n
[S.TB.3] Keep line length within 72 characters in testbench codes	R	y
[S.TB.4] Testbenches should be partitioned into behavioral ans synthesizable sections	R	n
IP prototyping		
[S.PT.1] Soft IP prototyping	M2	y

4.5. FPGA prototyping.

In FPGA prototyping, the input pattern is saved in Logic Analyzer (LA) and sent to FPGA. Then the result by waveform will sent back to the LA to dump the file for checking. In the proposed design, RAM will be used, but FPGA dose not support it, so in FPGA verification, Register file will be used to take replace RAM. The FPGA verification plan shows in Fig. 4.11, and Fig. 4.12 depicts the verifying situation.

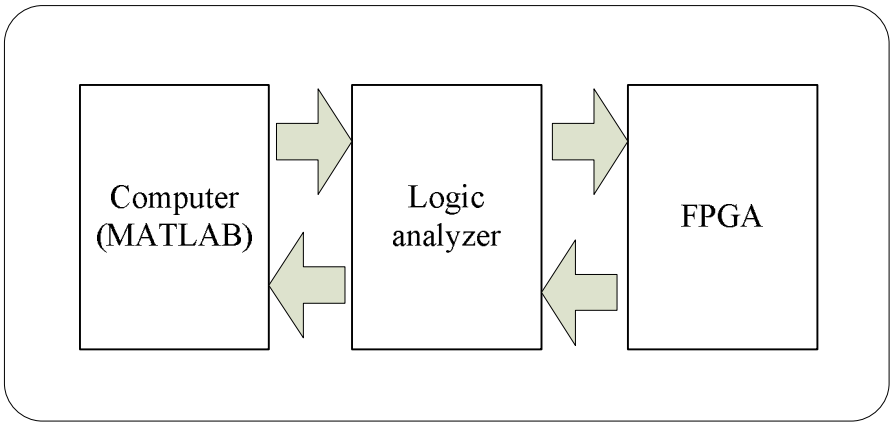


Figure 4.11 – The FPGA verification plan

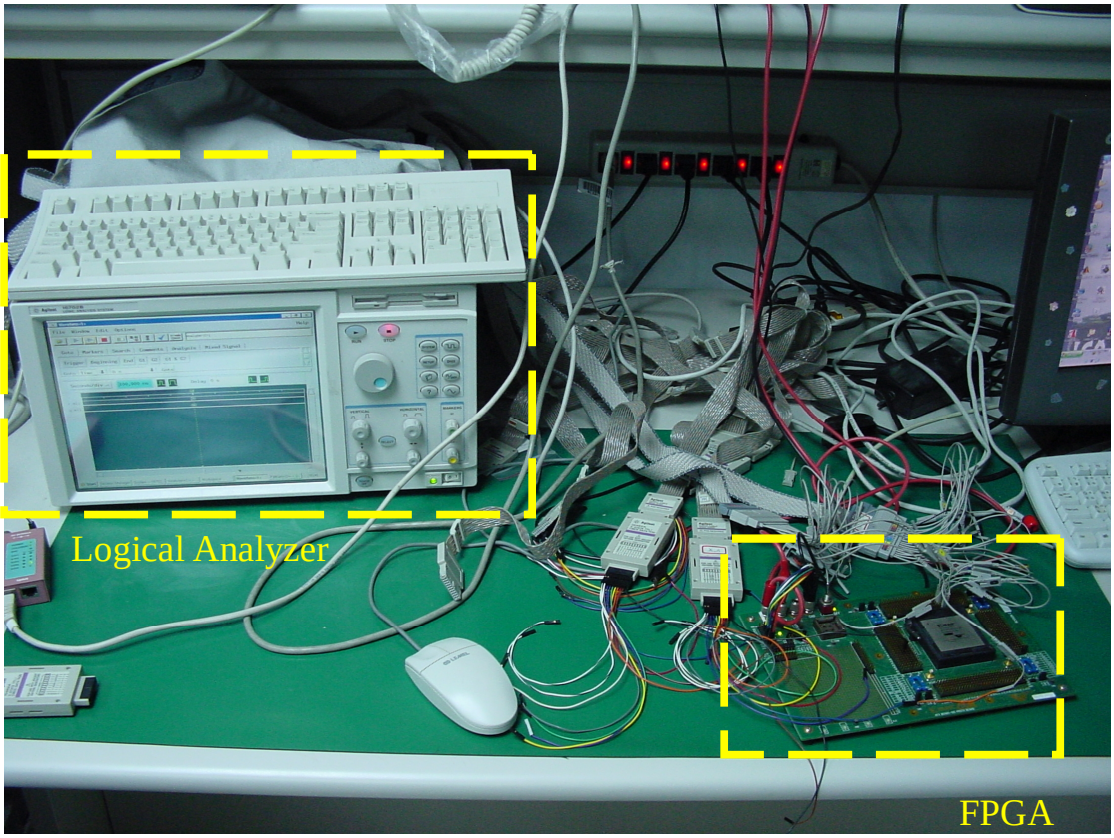


Figure 4.12 – Logic analyzer and FPGA board.

Table 4.5 – Xilinx FPGA synthesis report.

Traget Device	Xcv2000e-bg560
Slices	10449
Slices Flip Flops	9,905
Gate count	157,486
Timing	27.901ns (35.84 MHz)

4.6. Implementation results

The maximum clock rate is 164MHz, which throughput can approach 655MHz at maximum. The PAR process of layout is applied with SYNOPSYS ASTRO by UMC 0.18 μm. The chip feature shows in table 4.6, and fig. 4.13 depicts the macro layout view of equalizer.

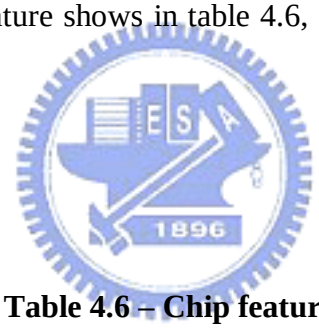


Table 4.6 – Chip feature

Module name	equalizer
Technique	0.18um CMOS, 1P6M
Gate count	88390
Macro Size	1470x1470
Clock rate	528MHz
Throughput	480Mbit/s
Power dissipation	69.3826 mW

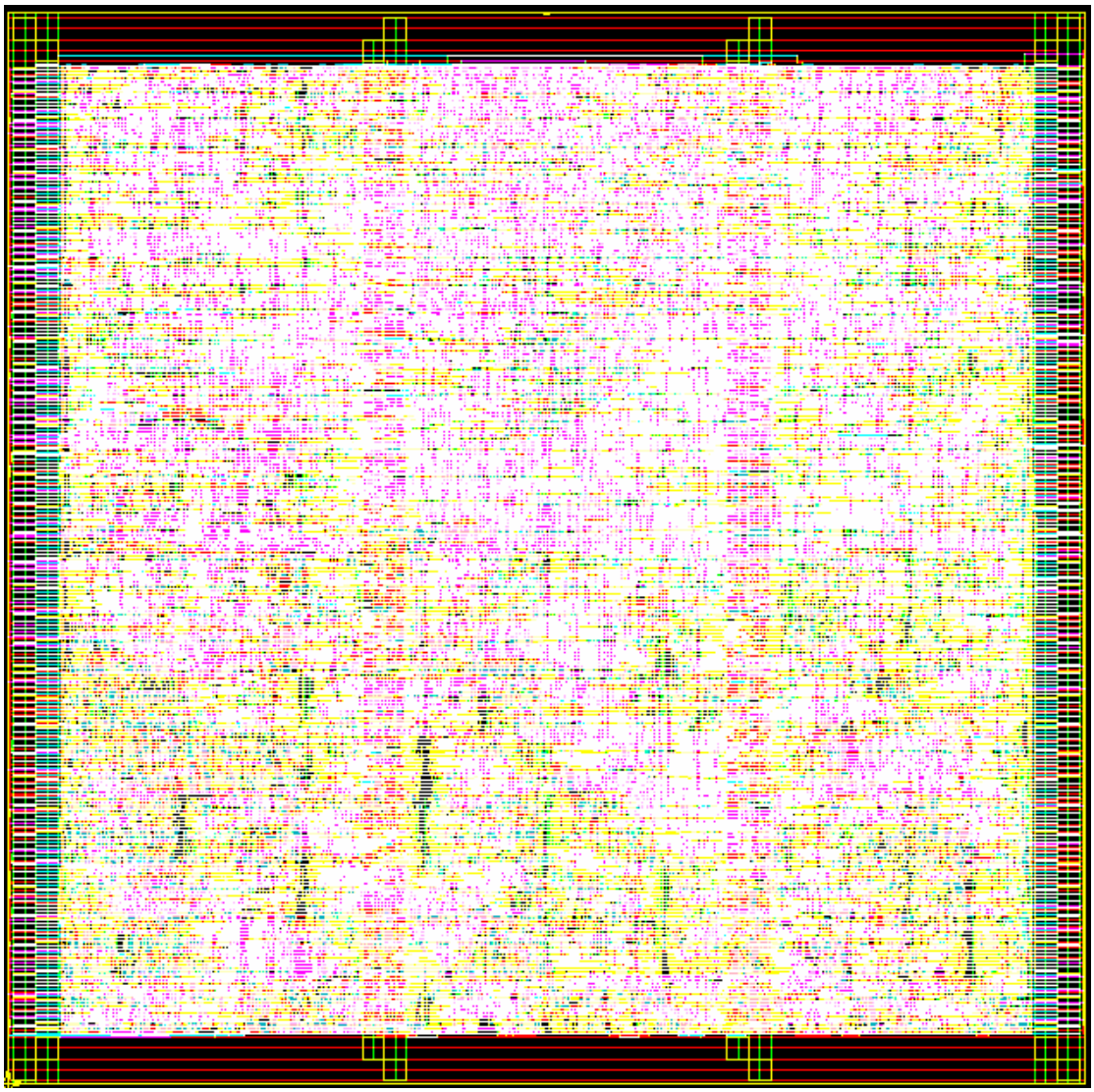


Figure 4.13 – Macro layout view

Chapter 5.
Simulation result and performance analysis

5.1. Introduction

In this chapter we will discuss the design flow, system platform and performance for the proposed design. In this study, behavior model is built by Matlab, and then do system co-simulation with RF in Agilent ADS tool. The design flow is illustrated in Fig. 5.1. this kind of waterfall model can work well up to 100k gate count design.

After RTL code is development and verified, two ways are used for implement the design, one is ASIC, the other is FPGA prototyping. Both of them will be discussed in chapter 5. FPGA prototyping is for verifying hardware design in general, because FPGA can simulate the real world situations which we don't concern before. After that, we synthesis the design to gate-level netlist by reasonable design constrains, and check the timing, area and power, if all of them pass, we will run

Place & Route. After all, we check the timing, area and power again. If all of them conformed, the design is done.

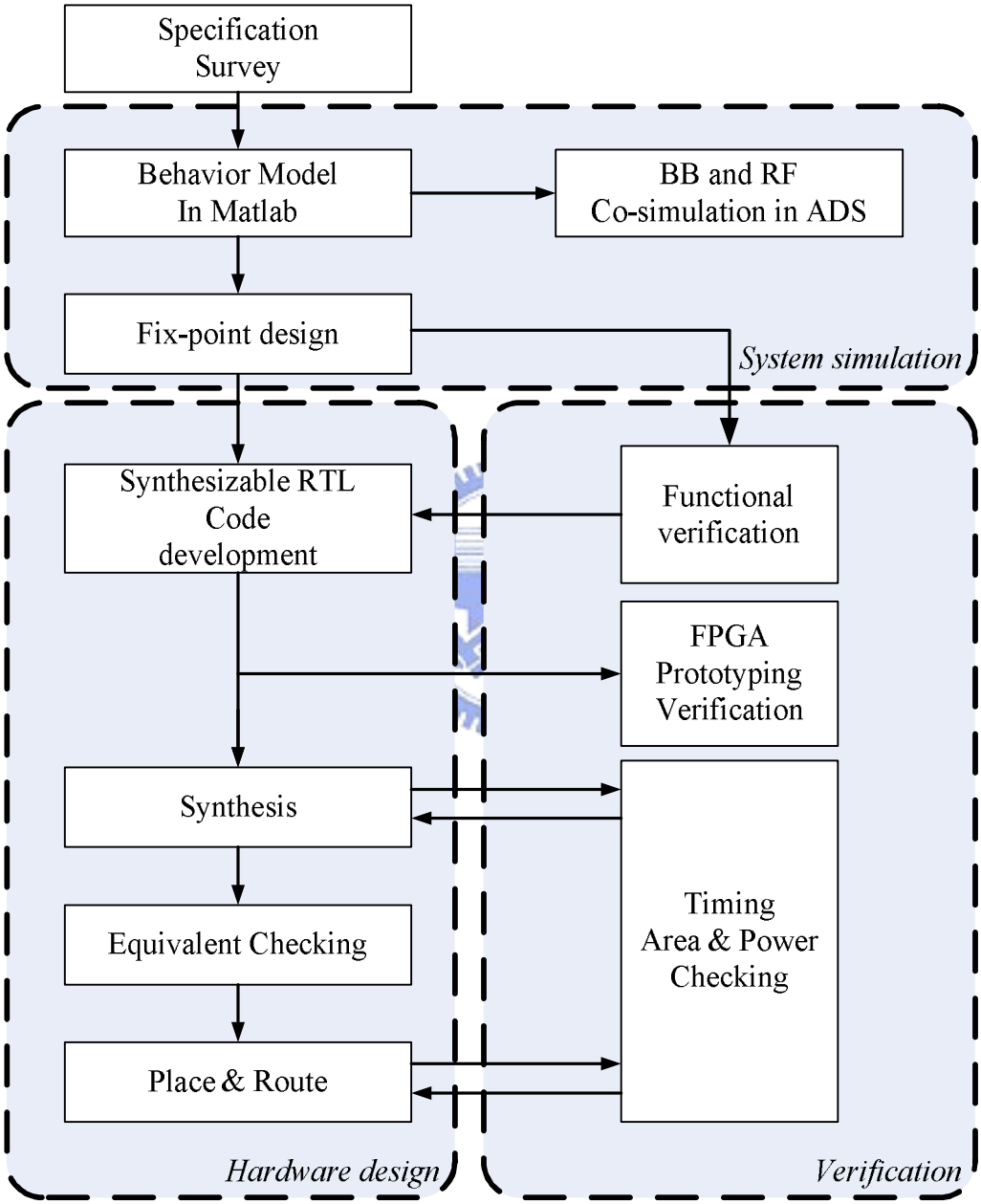


Figure 5.1 – Design & verification flow

5.2. System platform

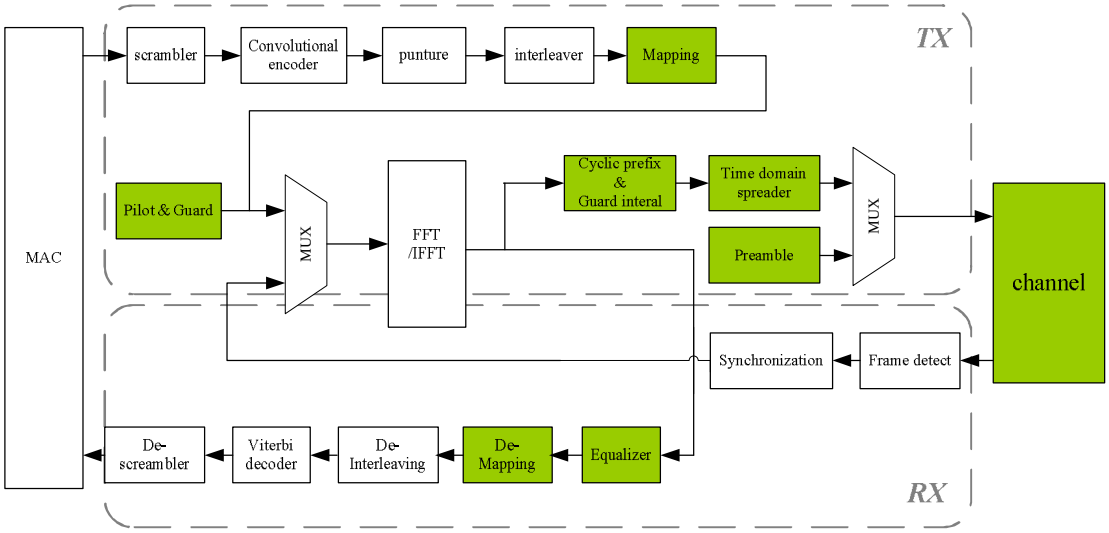


Figure 5.2 – System platform for UWB system

Our system is illustrated in Fig. 5.2 [5]. The platform by MATLAB is based on 802.15.3a standard. The system platform it built for system performance analysis and function verification. Such as error vector magnitude (EVM), bit error rate (BER) and packet error rate (PER).

In system co-simulation, the baseband platform and the RF behavior model are combined together in Agilent ADS tool. It is because the information of RF simulation is viewed as timed sequence, so the sequences calculated by MATLAB should be packed and transformed into timed sequence, then RF team can check their parameter settings and performance, such as Tx EVM, Tx power spectrum, Rx sensitivity and PER etc. Fig. 5.3 shows the co-simulation platform.

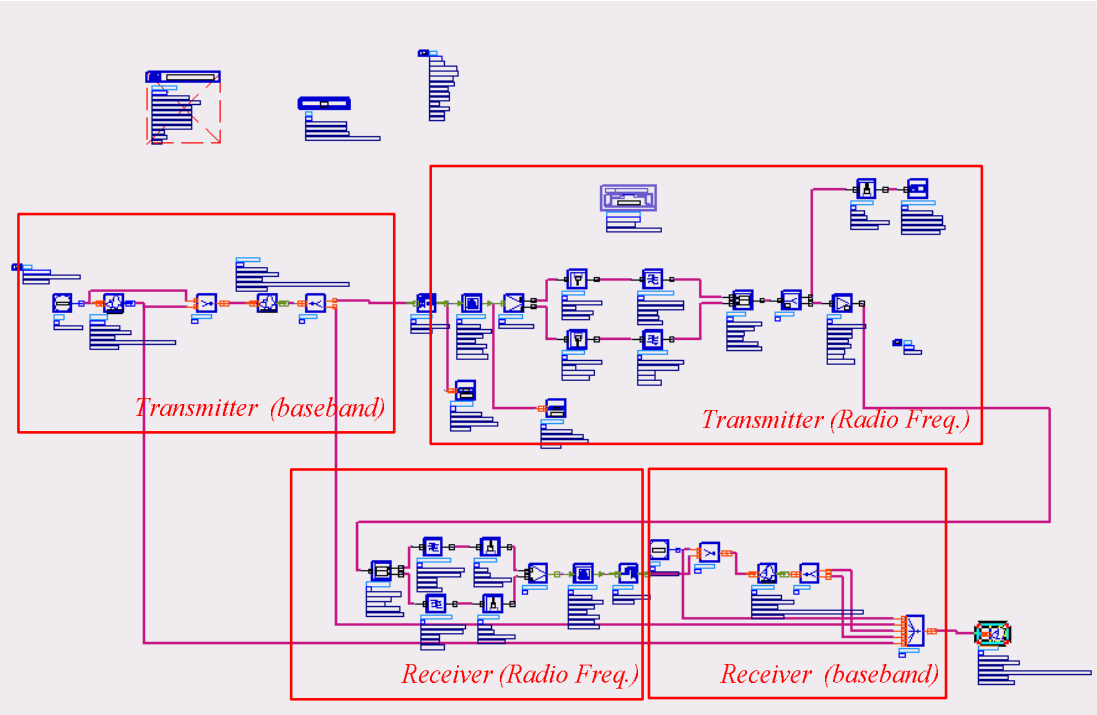


Figure 5.3 – Co-simulation platform

5.3. Performance analysis

The proposed channel is simulated in the IEEE 802.15.3a system platform. The PER analysis will focus on the 8% PER, which is requirement in IEEE 802.15.3a.

5.3.1 CE error tracking Performance

To analyze the CE error tracking performance of the proposed channel equalizer, error vector magnitude (EVM) is measured. The EVM value of CE can be derived as equ. 5.1, where $y_{l,k}$ is the data after equalization, $x_{l,k}$ is the data from transmitter, which means ideal vector.

$$EVM_{dB} = 20\log\left(\sqrt{\frac{\sum_{l}\sum_{k}\left\|x_{l,k}-\hat{y}_{l,k}\right\|^2}{\sum_{l}\sum_{k}\left\|\hat{y}_{l,k}\right\|^2}}\right) \tag{5.1}$$

From the definition, if the EVM_{dB} is lower when system performance is better, the fig. 5.4 shows the EVM with and without CE error tracking in condition of CM2 channel model, 40ppm CFO, 40ppm SCO.

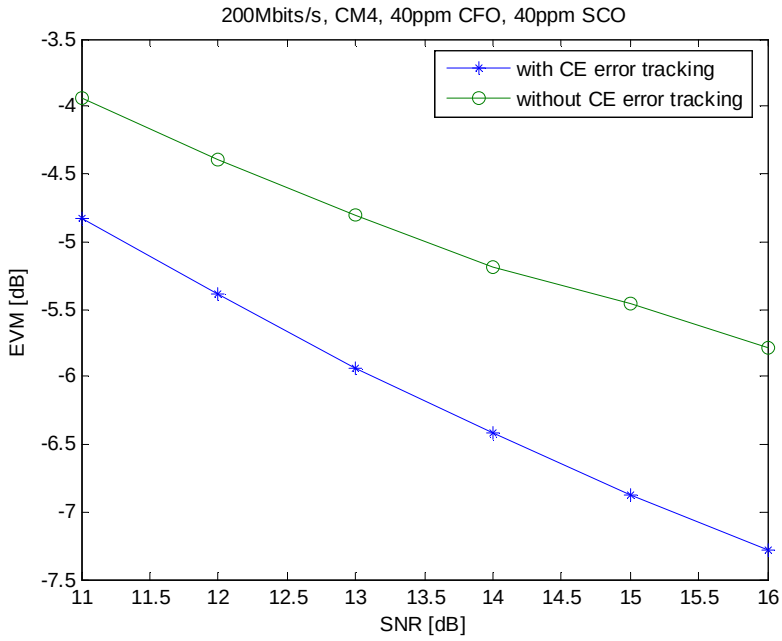


Figure 5.4 – CE error tracking performance analysis

From the figure we can know, the proposed CE error tracking achieves 0.5~1dB gain in EVM compared with the system without CE error tracking.

To analysis the performance, packet error rate (PER) is also a target to achieve. In IEEE 802.15.3a specification, PER is define as the probability of a 1024 byte packet miss, and should be less than 8%. The simulation of PER should be averaged

over a minimum of 50,000 realizations for each multi-path channel environment. The fig 5.5 shows the PER with and without CE error tracking. Notice that it achieves about 0.7 dB gain in PER compared with system without CE error tracking. The condition of the simulation is 200Mbits/s, CM4 channel and AWGN, 40ppm CFO and 40ppm SCO.

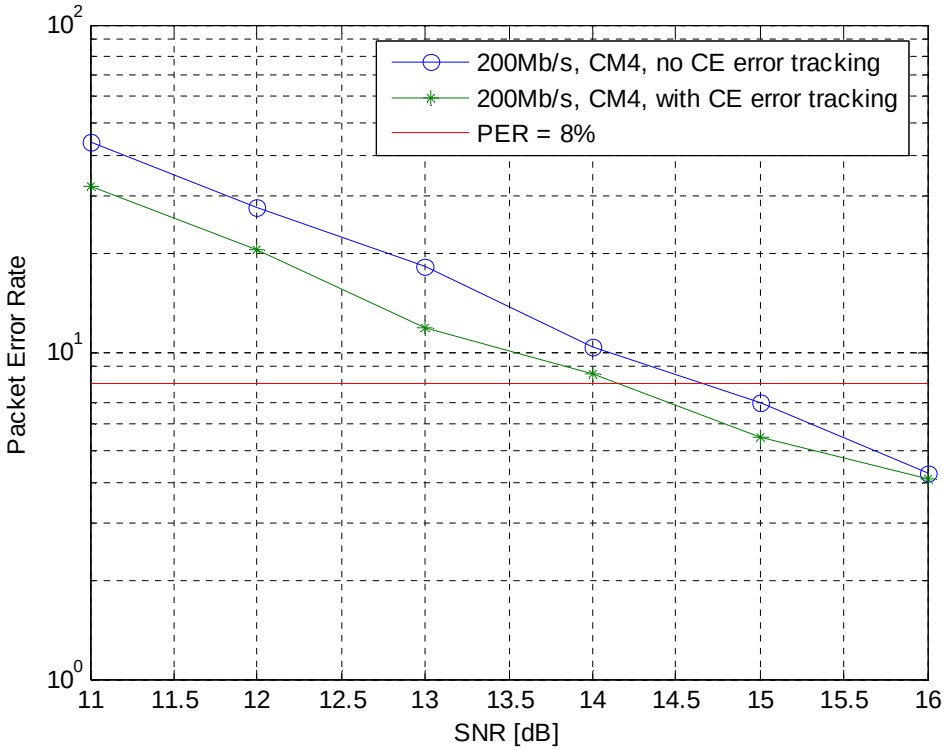


Figure 5.5 – CE error tracking performance analysis

5.3.2 Phase error tracking Performance

To verify the PET performance, the design is simulated under 40ppm CFO and 40ppm SCO, which is standard requirement. In the following simulation and

comparison, the proposed design is compare to a simple PET algorithm, which realize below.

$$\hat{q}_l = \frac{1}{12}\sum_k \arg(\hat{y}_{l,k}) - \arg(P_{l,k}) \qquad (5.2)$$
$$k = -55,-45,-35,-25,-15,-5,5,15,25,35,45,55$$

$$\hat{f}_l = \frac{1}{6\times 60}\left[\sum_{k=55,45,35,25,15,5} \arg(\hat{y}_{l,k}) - \arg(P_{l,k}) - \sum_{k=-55,-45,-35,-25,-15,-5} \arg(\hat{y}_{l,k}) - \arg(P_{l,k})\right] \qquad (5.3)$$

The algorithm only use 12 pilot subcarriers to against the phase offset, so the $\hat{q}_l$ and $\hat{f}_l$ will be oscillate, just like the fig. 5.6 shows. The fig. 5.7 shows the EVM comparison between adaptive PET and without adaptive PET. PET with adaptive filter can against the noise. The fig. 5.7 is another PET performance analysis with EVM. The figure shows that adaptive PET achieves 2.5 dB gains than other one. It increase the system performance a lot.

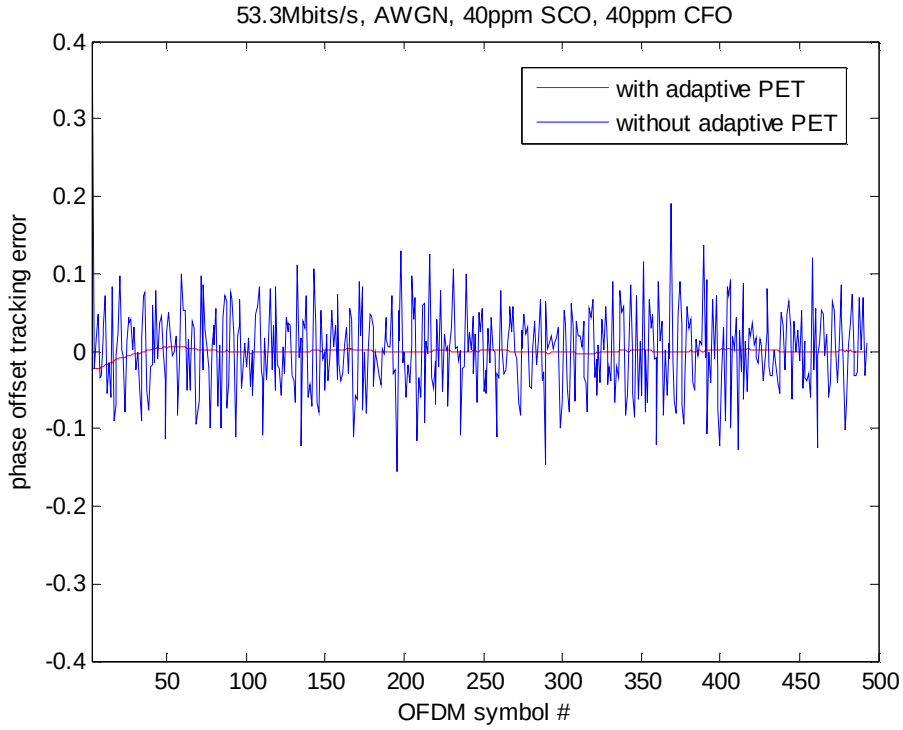


Figure 5.6 – The phase offset deviation analysis

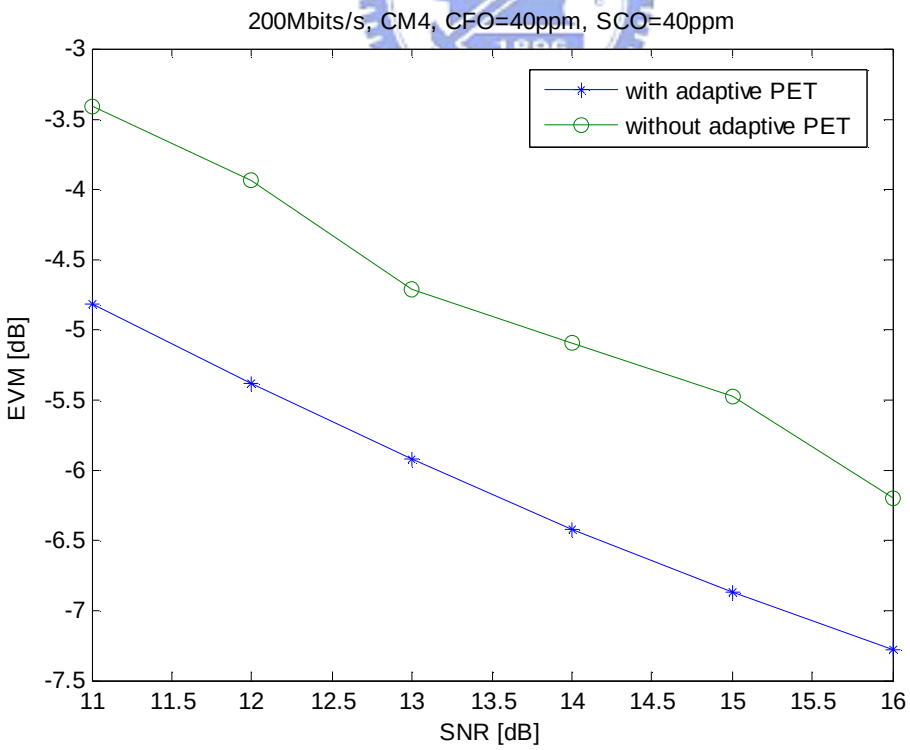


Figure 5.7 – PET performance analysis

5.3.3 System Performance

To verify the complete system performance of the proposed channel equalizer, PER of a complete IEEE802.15.3a basdband processor are measured with the Intel proposed indoor wireless channel model that contains 40ppm CFO and 40ppm SCO. The PER curves of different transmission mode are shown in fig. 5.8.

The design SNR for 8% PER is listed in table 5.1. the table tells the proposed system has better performance in data rate of 480Mbits/s. The proposed baseband system achieves 1.05~6.09 dB gain in SNR compared with standard requirement.

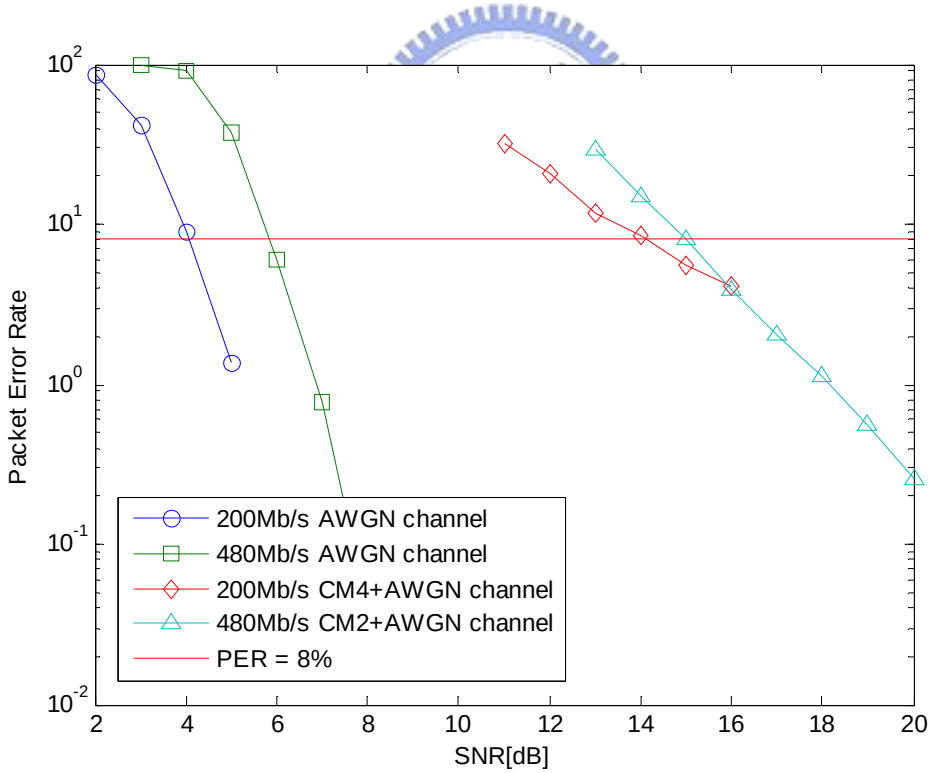


Figure 5.8 – PER performance of the proposed baseband platform

Table 5.1 – Required SNR for 8% PER of the proposed baseband platform

Data Rate	Design SNR (AWGN)	Design SNR (Multi-Path)
200Mbits/sec	4.11 dB	14.18 dB
480Mbits/sec	5.03 dB	15.01 dB
Data Rate	**SNR Constraint (AWGN)**	**SNR Constraint (Multi-Path)**
200Mbits/sec	5.16 dB	15.1 dB
480Mbits/sec	9.66 dB	21.1 dB

Chapter6.
Conclusions and Future Work.

6.1. Conclusions

Ultra Wide-Band uses OFDM system, which makes ultra wide-band system transmit in high data rates, but the system becomes sensitive to phase offset and phase noise. In this thesis, we propose a high speed and low complexity equalizer for WLAN IEEE 802.15.3a. In the proposed equalizer architecture, CORDIC module reduces the computation complexity of channel estimation, equalization, and phase error tracking.

IP qualification is the key of SOC, as SOC become more and more popular, IP qualification become more and more important. In this study, we consider the equalizer with soft IP qualification to achieve IP reuse.

6.2. Future Work

In the proposed equalizer architecture, CORDIC module reduces the computation complexity of channel estimation, equalization, and phase error tracking,

but it cost too much area. In the proposed design, CORDIC and de-CORDIC use about 50% of the total gate count of the equalizer. If there is more than one block need CORDIC module (like CORDIC based FFT [14]), then CORDIC can be share and reuse.

Bibliography

[1] A. Batra, et al., "*MultiBand OFDM Physical Layer Proposal for IEEE 802.15 Task Group 3a*,", http://www.multibandofdm.org, September 2004.

[2] A.Saleh and R.Valenzuela, "*A Statistical Model for Indoor Multipath Propagation*,", IEEE JSAC, Vol. SAC-5, No. 2, pp. 128-137, Feb. 1987

[3] IEEE P802.15-02/279r0-SG3a, "*UWB Channel Modeling Contribution from Intel*", available at http://grouper.ieee.org/groups/802/15/pub/2002/Jul02.

[4] J. Foerster et al., "*Channel modeling sub-committee report final*,", IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs), IEEE P802.15-02/490r1-SG3a, Feb. 2003.

[5] Anuj Batra, Jaiganesh Balakrishnan, G. Roberto Aiello, Jeffrey R. Foerster, and Anand Dabak, , *"Design of a Multiband OFDM System for Realistic UWB Channel Environments"*, IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 52, NO. 9, SEPTEMBER 2004

[6] Chia-Sheng Peng; Yuan-Shin Chuang; Kuei-Ann Wen, "*CORDIC-based architecture with channel state information for OFDM baseband receiver*", IEEE Transactions on Consumer Electronics, Volume 51, Issue 2, pp. 403 – 412, May 2005

[7] Yi-Hsin Yu, "*A channel equalizer for OFDM-based wireless access system*", M.S.

thesis, Dept. Electronics Engineering, National Chiao Tung Univ., Taiwan, 2004.

[8] Yuqiang Zhang; Junhui Zhao, "*Performance simulation of fixed-point for MB-OFDM UWB system*", Wireless Communications, Networking and Mobile Computing, 2005. Proceedings. 2005 International Conference on Volume 1, pp. 292 - 295, Sept. 2005

[9] Anuj Batra, Jaiganesh Balakrishnan, G. Roberto Aiello, Jeffrey R. Foerster, and Anand Dabak, , *"Design of a Multiband OFDM System for Realistic UWB Channel Environments",* IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, VOL. 52, NO. 9, SEPTEMBER 2004

[10] Yuan-Mao Chang; Cheng-Wei Kuang; Chien-Ching Lin; Tzu-Shien Sang; Hsie-Chia Chang; Chen-Yi Lee, "*A new channel equalizer for OFDM-based wireless communications*", IEEE VLSI-TSA International Symposium pp.104 – 107, April 2005

[11] Choi, J.D.; Stark, W.E., "*Performance of UWB communications with imperfect channel estimation*", Military Communications Conference, 2003. MILCOM 2003. IEEE Vol 2, pp. 915 - 920 Vol.2, Oct. 2003.

[12] Hewavithana, T.C.; Brookes, D.A., "*Blind adaptive channel equalization for OFDM using the cyclic prefix data*", Global Telecommunications Conference, 2004. GLOBECOM '04. IEEE Volume 4, pp.2376 - 2380 Vol.4, Dec. 2004

[13] Hsuan-Yu Liu; Chien-Ching Lin; Yu-Wei Lin; Ching-Che Chung; Kai-Li Lin; Wei-Che Chang; Lin-Hung Chen; Hsie-Chia Chang; Chen-Yi Lee, "*A 480Mb/s LDPC-COFDM-based UWB baseband transceiver*", Proceedings on of IEEE International Solid-State Circuits Conference, pp. 444 - 609, Feb. 2005

[14] Jen-Chih Kuo; Ching-Hua Wen; An-Yeu Wu, "I*mplementation of a programmable 64/spl sim/2048-point FFT/IFFT processor for OFDM-based communication systems*", Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium, pp. II-121 - II-124 vol.2, May 2003.

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論文題目 ： CORDIC based Equalizer for Ultra-Wide band system

用於 UWB 之 CORDIC based 等化器設計