國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

採用行為模型設計方法
之超寬頻射頻前端接收器設計

UWB RF Receiver Front-End Design by Using Behavior Model

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中華民國九十五年六月

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摘　　要

為了改善射頻電路設計流程以及系統驗證的效率，本論文提出一個可用於寬頻放大器的行為模型計設方法。此行為模型將一放大器分成輸入介面、增益級與輸出介面三個部份，並且可同時模擬輸入／輸出阻抗匹配、雜訊指數、頻率響應以及非線性失真等射頻電路的特性。為了證明此方法的可行性，本論文設計了一個寬頻放大器的行為模型，並比較電晶體階層與型為模型的系統模擬結果，其 EVM 的均方根值誤差小於 0.79%，模擬時間減少了 87%。此行為模型除了能夠用來模擬一個既有的電路外，也能夠用來幫助設計新的電路。本論文利用此行為模型設計了一個以電容性交錯藕合技術做為輸入阻抗匹配的低雜訊放大器，並將此放大器應用於超寬頻射頻前端接收器。經由 0.18-μm CMOS 製程進行電路實作，此射頻前端接收器的模擬結果，其頻寬範圍為 3.1-10.6GHz，消耗功率為 11.4mW，同時具有 20.9 dB 的最大電壓增益、3.4dB 的最低雜訊指數和-14.3dBm 的最大第三階互調線性度。

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ABSTRACT

In order to improve RFIC design flow and facilitate system performance verification, an innovative behavior model of wideband amplifier is proposed. The proposed behavior model can simultaneously predict the characteristics of RF effect of input/output impedance matching, noise, frequency response and nonlinearity in one single model. To demonstrate the feasibility of the model, a wideband LNA has been designed with this model. The system simulation results show that the behavior model agrees well with the transistor level circuit

with RMS error less than 0.79%, and 87% reduction of simulation time is achieved. The proposed behavior model can not only model an existed circuit, but also can help to design a new circuit. In this thesis, a design example of wideband LNA with capacitive cross-coupling (CCC) technique for input matching is presented. And the LNA is utilized in a receiver front-end design for UWB application. A circuit implementation in 0.18-μm CMOS process shows a 3.1-10.6GHz bandwidth. The UWB receiver front-end provides a maximum voltage conversion gain of 20.9 dB while drawing 11.4 mW from a 1.8-V supply. A double sideband noise figure as low as 3.4 dB and a maximum IIP3 of -14.3 dBm have been simulated.

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誌予　　2006

洪志德

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Chapter 1

Introduction

Recently, the Federal Communications Commission (FCC) in US has approved the use of ultra-wideband (UWB) technology for commercial applications in the 3.1-10.6 GHz frequency band [1]. The newly unlicensed UWB opens doors to wireless high-speed communications and has been exciting tremendous academic research interest. UWB performs excellently for short-range high-speed uses, such as automotive collision-detection systems, through-wall imaging systems and high-speed indoor networking, and plays an increasingly important role in wireless personal area network (WPAN) applications. This technology will be potentially a necessity in our daily life, from wireless USB to wireless connection between DVD player and TV, and the expectable huge market attracts various industries.

The main challenge of IC design nowadays is how to implement circuits with the minimum

chip area, power consumption and time to market. Demands on cost reduction for wireless multimedia applications have driven the integration of both analog/RF and digital/baseband building circuits into a wireless transceiver system on a chip (wireless SoC). By integrating the circuits on a single chip, the pads can be reduced, and the chip area therefore is reduced. For wireless SoC designs involving analog/RF circuit integration, the system performance must be verified by the system simulation which takes a lot of time. In order to reduce the time for verification, the analog behavior models are used in system simulation. The analog behavior models are difficult to implement due to the complex analog characteristics, especially for the wideband applications. The lack of behavior model for analog/RF circuits make the verification for the entire system performance very time consuming. The wideband analog/RF behavior models which have essential RF characteristics, such as frequency response, input/output impedance and NF, are required for UWB system verification.

1.1 **Motivation**

The behavior models of analog circuit blocks are widely used in system co-simulation. Several behavior models were introduced to describe the RF effects: linear transfer functions represent frequency dependence [2], S-parameter data in Touchstone format characterize impedance mismatch and frequency response for linear small-signal amplifiers, and black box

models in Volterra series can model nonlinear distortion [3]. Nevertheless, these models describe RF characteristics individually without considering the impact of each other and are insufficient for system simulation. Besides, the top-down design methodology is preferred to refine the specifications of the building blocks of RF module circuits at the beginning stage for developing sophisticated wireless systems. The table-based or polynomial models can not support top-down design methodology due to the lack of circuit insights in these models.

A behavior model, which can not only be used in system co-simulation, but also assist with circuit design is desired. The research goal of this thesis is to implement a behavior model which can achieve the above requirements. Then, implement a low-power receiver front-end in the low-cost CMOS technology for wireless UWB applications by using the proposed behavior model.

1.2 **Specifications**

1.2.1 MB-OFDM Proposal Brief

In the MB-OFDM proposal, the frequency band of UWB is divided into 14 bands, in where each band has a bandwidth of 528 MHz. As shown in Table 1, the 14 bands are categorized into 5 band groups. There are 3 bands in each band group except band group 5 which has only

2 bands. A time-frequency code (TFC) is utilized to interleave coded data over up to three frequency bands in each band group. There are 122 modulated and pilot subcarriers out of a total of 128 subcarriers of 4.125 MHz. The QPSK modulation signals are used in the OFDM subcarriers. The subcarrier falling at DC (0th subcarrier) is omitted. Devices operating in band group #1 are denoted as Mode 1 devices. It is mandatory for all devices to support Mode 1 operation. Supporting other band groups operation is optional and can be added in the future. The transmission spectrum shall have a 0 dBr (dB relative to the maximum spectral density of the signal) bandwidth not exceeding 260 MHz, -12 dBr at a 285 MHz frequency offset, and -20 dBr at a 330 MHz frequency offset and above. The transmitted spectral density shall fall within the spectral mask, as shown in Figure 1. The average power of the transmitted signal is -9.9 dBm. There are several data rates supported for a UWB system, they are list in Table 2. For a packet error rate (PER) of less than 8% with a PSDU of 1024 bytes, the minimum receiver sensitivity numbers for the various rates are listed in Table 2. The higher data rate must have higher sensitivity since the signal to noise ratio will become small when the data rate is increased.

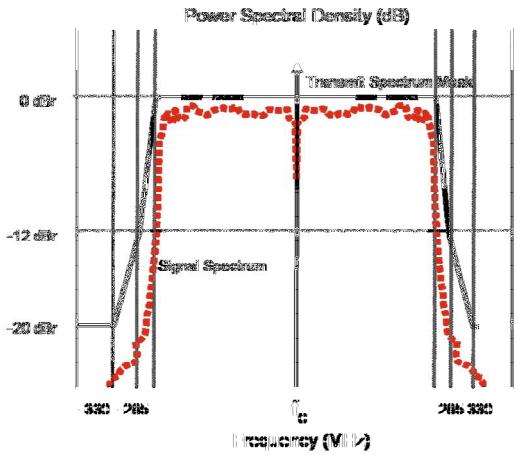


Figure 1 Transmitter power spectral density mask in MB OFDM proposal

Table 1. Band assignment in Multi-Band OFDM proposal.

Band Group	BAND_ID	Lower frequency	Center frequency	Upper frequency
1	1	3168 MHz	3432 MHz	3696 MHz
	2	3696 MHz	3960 MHz	4224 MHz
	3	4224 MHz	4488 MHz	4752 MHz
2	4	4752 MHz	5016 MHz	5280 MHz
	5	5280 MHz	5544 MHz	5808 MHz
	6	5808 MHz	6072 MHz	6336 MHz
3	7	6336 MHz	6600 MHz	6864 MHz
	8	6864 MHz	7128 MHz	7392 MHz
	9	7392 MHz	7656 MHz	7920 MHz
4	10	7920 MHz	8184 MHz	8448 MHz
	11	8448 MHz	8712 MHz	8976 MHz
	12	8976 MHz	9240 MHz	9504 MHz
5	13	9504 MHz	9768 MHz	10032 MHz
	14	10032 MHz	10296 MHz	10560 MHz

Table 2. Receiver performance requirement in MB OFDM proposal.

Data rate (Mb/s)	Minimum sensitivity (dBm) for Mode 1
53.3	-83.6
80	-81.6
110	-80.5
160	-78.6
200	-77.2
320	-75.5
400	-74.2
480	-72.6

1.2.2 Architecture and Link Analysis

Direct-conversion is adopted in the system architecture as shown in Figure 2. The bulky image rejection filters are omitted and SoC integration is more accessible with this architecture. Beside, the power consumption can be reduced.

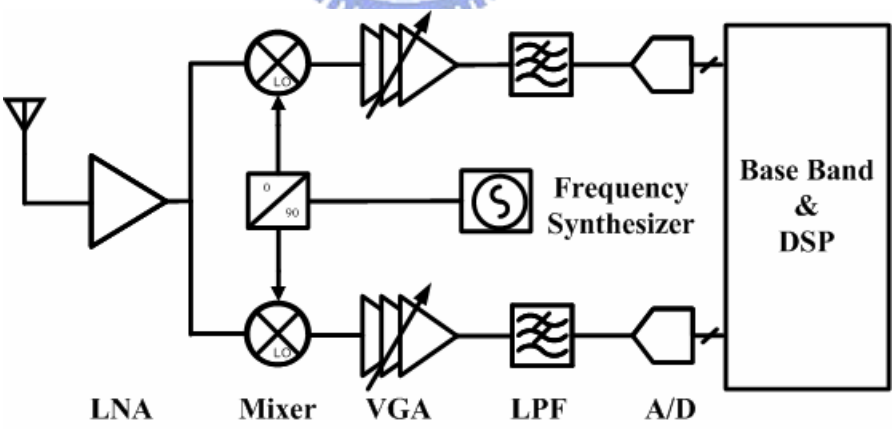


Figure 2 Direct-conversion architecture for UWB receiver.

The first building block in receiver path is LNA. It is a very important component in a receiver. If the gain of LNA is large enough, the noise from circuits behind LNA can be

ignored since the signal becomes very large. The LNA affects the sensitivity of the receiver. For UWB specification, the noise figure of the receiver after antenna must be lower than 6.6 dB. If the loss of switch and RF filter is 1.7 dB, the noise figure after filter must less than 4.9 dB. Since the bandwidth of UWB is from 3.1 GHz to 10.6 GHz, the impedance matching, the flatness of gain, and noise matching are difficult to achieve. The specification of each block in the receiving path is shown in Figure 3, and the NF link budget analysis is shown in Figure 4. The gain and NF specification of the receiver front-end which includes LNA and mixer are 22 dB and 3.82 dB, respectively.

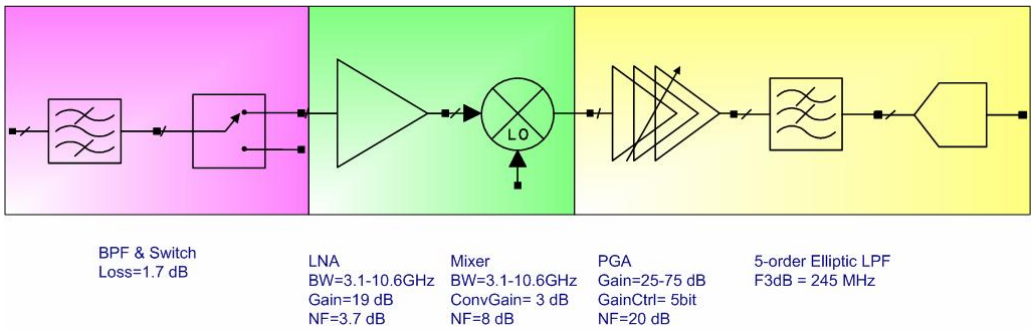


Figure 3 UWB receiver specifications.

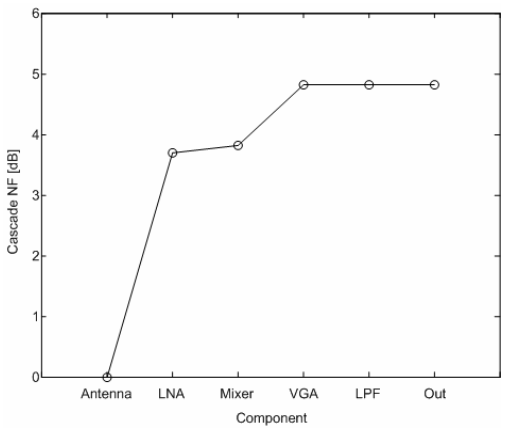


Figure 4 Receiver noise figure degradation.

1.3 **Organization**

The organization of this thesis is overviewed as follows. Chapter 2 describes the design flow for RF circuit design and proposes a unified behavior model. It also demonstrates a design example of UWB LNA. Chapter 3 reveals some examples of UWB LNA in recent researches, and chooses the capacitive cross-coupling (CCC) input matching technique for the UWB LNA design. A wideband LNA with CCC technique is designed by using the proposed behavior model in Chapter 4. The wideband LNA is also used in receiver front-end for ultra-wideband application. Chapter 5 concludes with a summary of contributions and suggestions for future work.

Chapter 2

A Unified Behavior Model Design

In order to improve the efficiency of circuit design, a design flow is presented in this chapter. In order to design the circuit by the proposed design flow, a unified RF behavior model combining the RF effects of input/output impedance, noise, nonlinearity and frequency response simultaneously is proposed. Section 2.1 addresses the design motivation of the design flow and the behavior model. The proposed behavior model consisting of input/output impedance and G_m suitable for the proposed design flow is presented in section 2.2. A Verilog-A behavior model for an ultra-wideband CMOS low noise amplifier is developed for fast and accurate system simulation in section 2.3. The analog performances of transistor level and behavior model are compared in section 2.4. The system co-simulation environment and results are presented in section 2.5.

2.1 Design Motivation

The design efficiency can be improved by the proposed circuit design flow and decreasing

the system simulation time. In order to reduce the time of system verification, behavior models are used in system co-simulation. In this thesis, a proposed behavior model can be used not only in the proposed circuit design flow to assist with the RF circuit design but also reduces the time of system verification.

In order to design a RF circuit efficiently, a valid design flow is required. Figure 5 shows the proposed design flow. To deign a circuit block of a system, it always needs to get the system specification first. The specification can tell us useful information about the system, and we can determine the system architecture by the information from specifications. The specifications of each building block can be calculated, once the system specifications and architecture are determined.

In the traditional design flow, the circuit design starts with the defined specification of each building block for system co-simulation. The design can be treated as an IP (Intellectual Property) if the design can be used in the system.

Actually, the RF circuitry usually consists of several circuit modules. Each circuit module has its assignments to assist the circuit design can meet the specifications. In the proposed design flow, the RF modules can be divided into three parts: input interface, output interface and G_m stage. The proposed design flow determines the specifications of each part. Than, we develop the behavior models of each part, a system simulation will be accomplished by these behavior models. If the performance can meet the system specifications, we can choose the

circuit topology by using the behavior model which has been selected. In an amplifier, the input interface acts like the input matching circuit. The output interface likes the output matching and the load of the amplifier. The G_m stage is the core of the amplifier, such as common source amplifier, common gate amplifier….etc. We can build up a database of all reference designs.

If the database is large enough, the proposed behavior can assist in designing a new circuit. The suitable topologies of a new target circuit which has difference specifications can be searched in the enormous database. After choosing the circuit topology by the database and optimize the circuit, if the specification can't meet the system requirement, we can replace the part which has poor performance in the circuit from the database. This method is more suitable to IP application. Each part of a building block treats as an IP, and the circuit design becomes more flexible.

Analog circuit design for communication system requires different levels of parameter abstraction. There are two ways to implement design flow. A top-down design starts with behavior models using the design flow to determine the most important characteristics and gradually modify each subsystem to increase the accuracy. A bottom-up design starts with a detailed specification and determines a behavior model which can be used in system co-simulation.

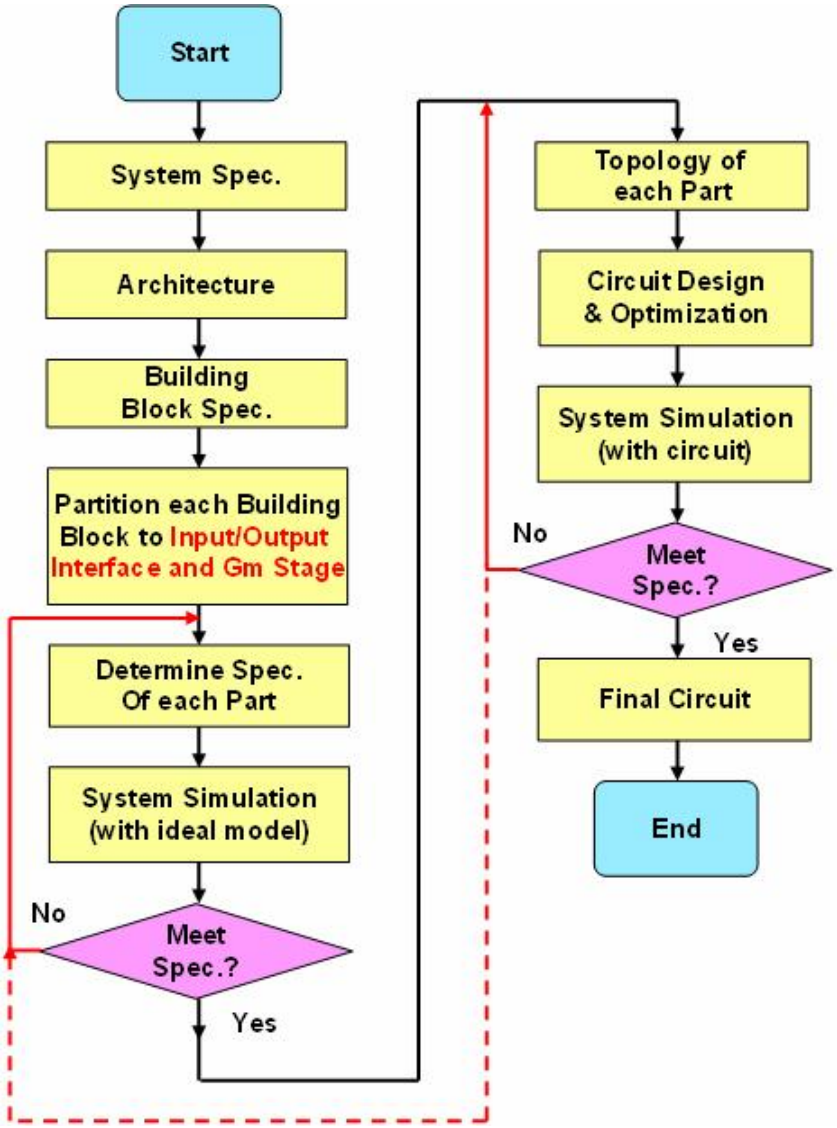


Figure 5 The proposed design flow

In this chapter, we focus on the development of a behavior model and system verification of an existing design, therefore we pays attention to the bottom-up design flow. The entire transceiver is verified with BER (bit-error rate) or EVM (error vector magnitude) simulation. Simulation with full-chip RF transceiver in transistor-level SPICE netlists is time consuming and very inefficient. Performing system simulation with analog/RF circuit elements prior to

chip implementation is crucial and urgent for designers in designing complicated wireless systems nowadays and facing very tight time-to-market schedule. In order to reduce the simulation time, behavior models for analog/RF circuits with accurate prediction are required in system simulation.

Typical characteristics must be considered and accurately modeled in RF designs including linearity, noise, gain, and frequency response. Traditionally, these characteristics are simulated with empirical models based on measurement. For example, n-port network parameter data in Touchstone format are used to characterize frequency response and noise performance. For nonlinear effect, either Taylor series or Volterra series are used instead to describe low-frequency or high-frequency distortion. The noise/frequency response and nonlinearity distortion are modeled separately without considering the impact of each other. Several kinds of behavior model are used in the different simulation environment. In this thesis, we propose a unified RF behavior model which combines the effects of input/output impedance, noise, nonlinearity and frequency response simultaneously and reduces the overall simulation time efficiently.

2.2 **The Unified Behavior Model**

Here, we focus on the RF building blocks of two-port network, such as amplifiers and

filters. Mixers and switches are beyond the scope of this behavior model. As shown in Figure 6, the proposed behavior model consists of three modules: input interface module ($H_{IF,i}$) for the input impedance network, core module (H_{Gm}) for the gain stage, and output interface module ($H_{IF,o}$) for the output load impedance. The architecture is appropriate to the design flow which described in previous chapter. In a LTI system, the transfer function of the two port network is represented by $H_{IF,i} \cdot H_{Gm} \cdot H_{IF,o}$ in the system simulation platform. Detailed modeling approach for each module is described in the following section.

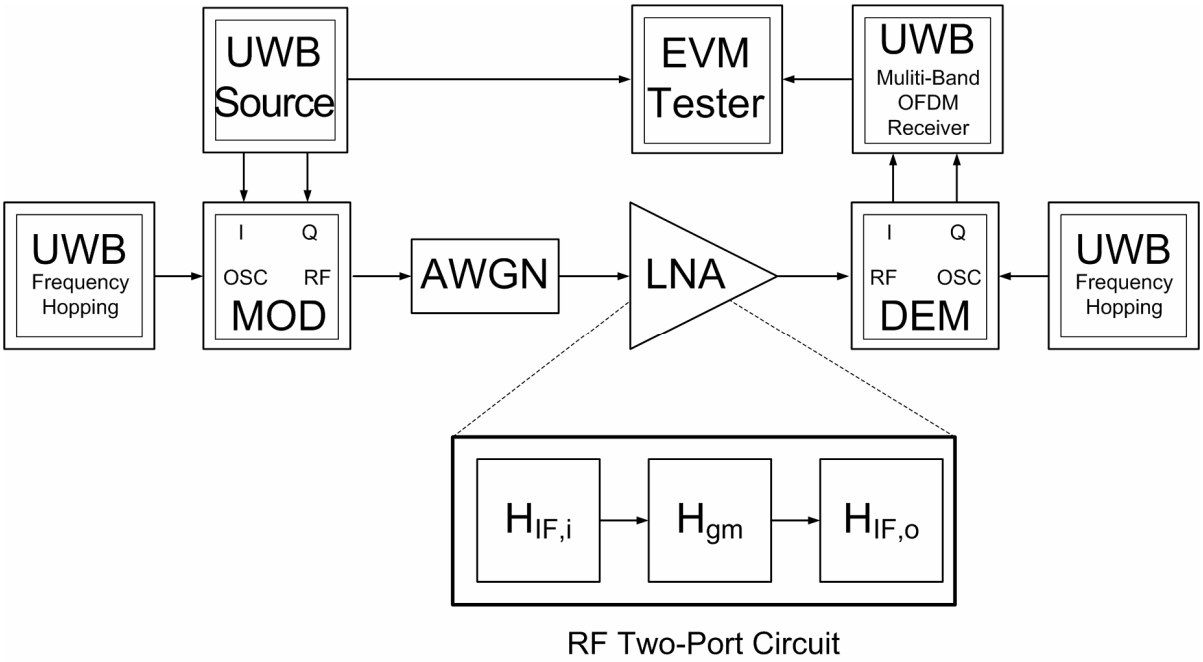


Figure 6 UWB system simulation block diagram.

2.2.1 Modeling of Input and Output Interfaces

The input/output impedance networks of a two-port circuit shape its frequency response

and bandwidth. Though Laplace transfer function can be used to model the frequency response [4], it only defines the voltage/current transfer relation and requires additional impedance networks for the loading effect. The additional impedance networks nevertheless also shape the overall frequency response and introduce iterations in modeling. Instead of using Laplace transfer function, the proposed model employs equivalent impedance networks to portray the frequency response and the impedance matching properties of input/output interfaces at the same time. An equivalent circuit consisting of resistors, inductors, and capacitors is established to model the input matching network and the input impedance of the active device. The capacitors and inductors are used to define the reactance of $H_{IF,i}$, while the resistors to define the loss including the resistor loss as well as the inductor loss and the capacitor loss. Physically, regular resistors contribute not only loss but also thermal noise. However, the equivalent resistors in $H_{IF,i}$ are not the actual thermal noise sources, and are intended to model the loss only. Similarly, the load impedance and the output impedance of the active device are modeled as a network of noiseless resistors, inductors, and capacitors.

2.2.2 Modeling of Gain Stage

The gain stage can be simply modeled by a controlled signal source, depending on the input and output signal types of the active circuit topology. For example, it can be a

voltage-controlled current source (VCCS) for a common source amplifier or a current-controlled current source (CCCS) for a common-emitter amplifier. Since the input impedance of the controlled signal sources have been considered in the input interface module, $H_{IF,i}$, and the output impedance of the controlled signal source can also be absorbed into the output load module, $H_{IF,o}$, the controlled signal source in H_{Gm} is ideal and defines the input and output voltage/current relation either linear or nonlinear.

2.2.3 Modeling of Noise

The noise effects are lumped into an equivalent noise source instead of a noisy resistor as [4]. Hence the RF effects are modeled incrementally with iteration reduced. The noise effects of a two-port network are modeled by three equivalent noise sources $i_{n,IF,i}$, $i_{n,Gm}$ and $i_{n,IF,o}$ for the input interface, core and output interface modules, respectively. For easy extraction of noise and model consistency, $i_{n,IF,i}$, $i_{n,Gm}$ and $i_{n,IF,o}$ are all placed at the output node of each module. The explicit input noise source of the active device, for example, is absorbed to $i_{n,IF,i}$ in the preceding module.

2.2.4 A Simple Example of the proposed Behavior Model

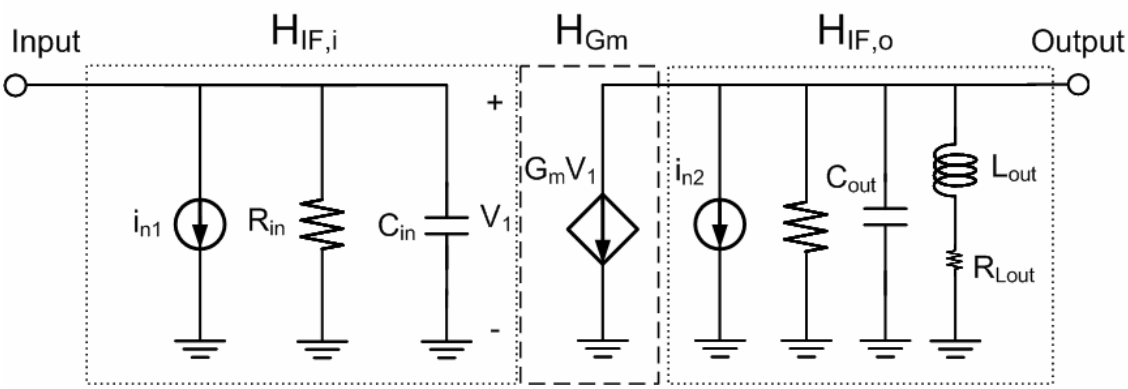


Figure 7 A simple model of common-source amplifier

Figure 7 shows a simple model example of common-source amplifier. The G_m stage of this model which can determine the gain and the nonlinearity is the type of VCCS due to the common-source topology. Input interface is defined by a resistor and a capacitor, and the output interface is defined by a resonance tank for RF application. The noise sources i_{n1} and i_{n2} are placed at the output of the input/output interface to model the noise performance of the circuit.

2.2.5 Modeling Flow

A modeling flow is developed for the proposed unified RF behavior model as depicted in Figure 8. The two-port circuit is mapped into three behavior modules as mentioned above with RF characteristics relation equations in each module derived. This is a process of

abstracting the physical circuit topology into a simplified equivalent circuit and grouping the equivalent circuit elements into each module accordingly, which has a great influence on the iterations in later optimization processes. From the results of the transistor level simulation or measurement, the initial values for the model parameters in $H_{IF,i}$, H_{Gm} and $H_{IF,o}$ are extracted. The parameter extraction is followed by four optimization processes to fit the model parameters for RF characteristics of input and output impedance, frequency response, noise and nonlinear effects in sequence. The optimization is a complex task due to the correlation among the RF characteristics, and therefore proceeded incrementally by considering the noise and nonlinear effects. That is, for small input signal condition, the two-port circuit is regarded as a noiseless linear circuit in the first two optimization procedures and then a noisy linear circuit in the noise optimization. On the other hand, the circuit is considered as a noisy weak nonlinear network in the final optimization procedure. For reverse isolation concern, more iterations are required in the non-unilateral cases. The optimal model parameters are obtained if the root mean square error (RMSE) is smaller than a threshold value. Ultimately, a system simulation is performed to verify the accuracy and feasibility of the RF behavior model.

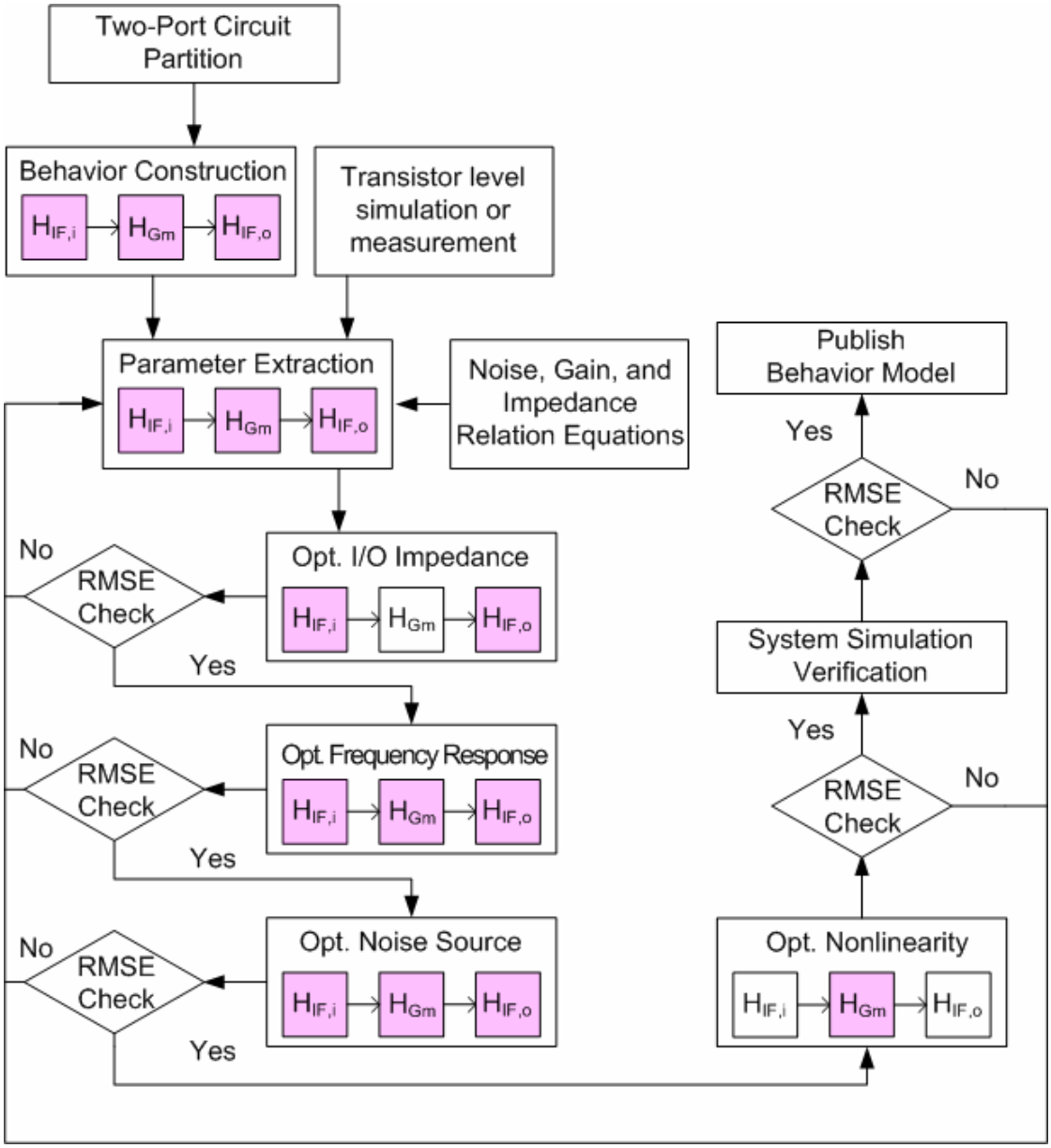


Figure 8 Unified behavioral modeling flow.

2.3 **Design Example of UWB LNA**

In this section, a behavior modeling example of a wideband CMOS low noise amplifier for ultra wideband applications is presented according to the above modeling procedure.

The targeting UWB LNA was fabricated in 0.18-μm CMOS technology and the circuit schematic is illustrated in Figure 9. The LNA employs stagger tuning technique, which consists of two stacked common-source stages with different resonance frequencies [5]. The output buffer in Figure 9 is for measurement purpose only and omitted in the behavior model. The behavior model of the UWB LNA contains three interface modules, $H_{IF,i}$, $H_{IF,c}$ and $H_{IF,o}$, and two G_m-core modules, $H_{Gm,1}$ and $H_{Gm,2}$, mapping the two amplification stages as shown in Figure 10.

2.3.1 I/O Interface

A simple RLC parallel network can be used to model the interface modules for narrow band circuits. To model the input band-pass matching network and the input impedance of transistor M1 of the UWB LNA, ideal lump elements L_1,L_2,L_3,C_1,C_2,C_3 and R_1 are used in $H_{IF,i}$. $H_{IF,c}$ and $H_{IF,o}$ add R_{C4}, R_{L4}, R_{C5}, and R_{L5} in the RLC parallel network due to the low-Q loads of the wide-band amplifier. It should be noted again that all resistors framed in Figure 10 are noiseless.

2.3.2 G_m Core

In an N-stage amplifier, N numbers of G_m-core modules are exploited regardless its

topology. The partition of the RF behavior model is determined by the critical impedance components which contribute the poles or zeros in the frequency response of the RF circuits. Two G_m cores $G_{m,1}$ and $G_{m,2}$, as a consequence, exist in the behavior model and their initial values are extracted from the small-signal transconductance values of transistors M_1 and M_2. Combining $H_{Gm,1}$ and $H_{Gm,2}$ with $H_{IF,i}$, $H_{IF,c}$, and $H_{IF,o}$, the frequency response is optimized to portray the noiseless linear characteristic of the UWB LNA.

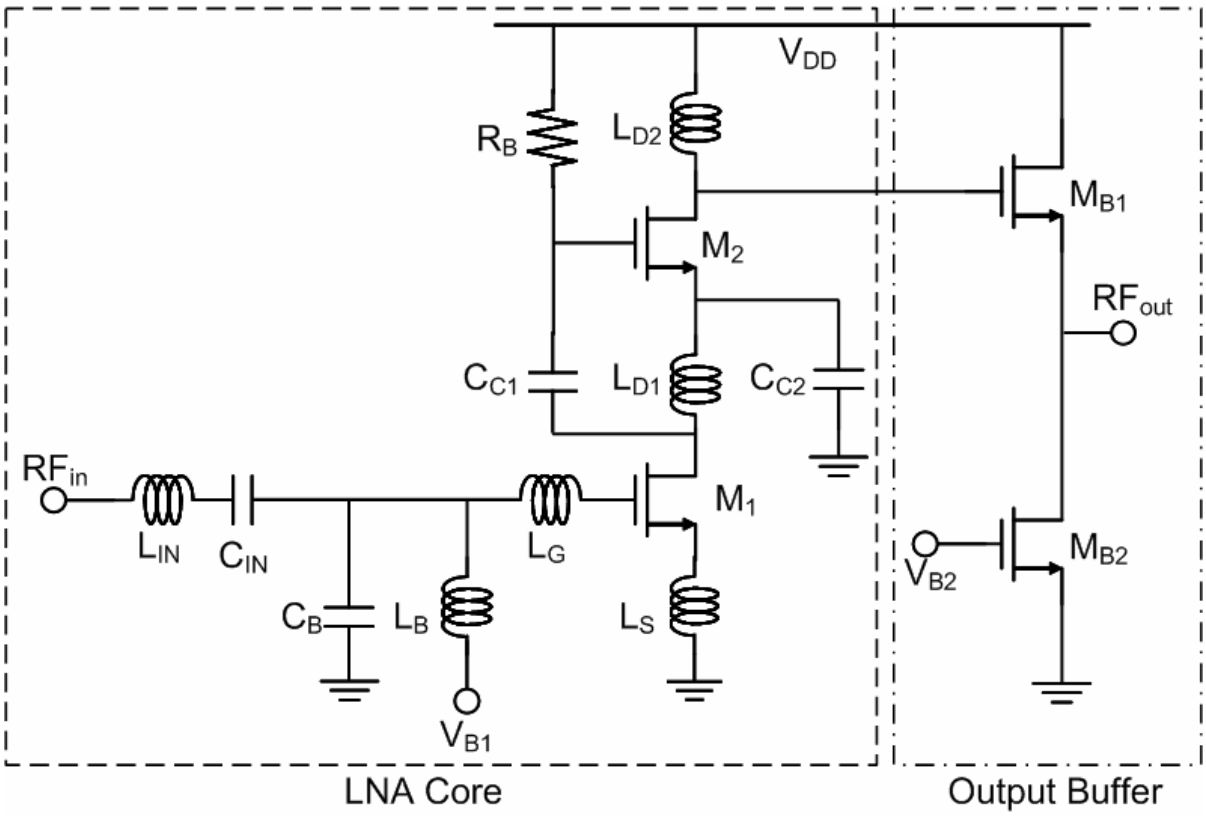


Figure 9 Target UWB LNA circuit.

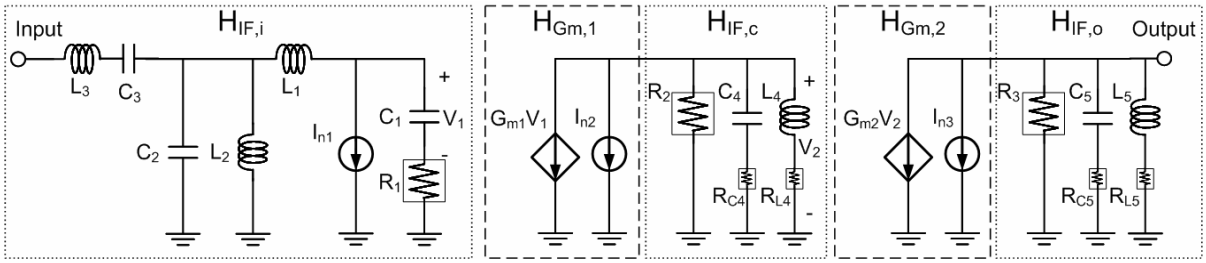


Figure 10 The UWB LNA Model.

2.3.3 Noise Sources

The noise sources considered in the RF behavior model are only thermal noise contributed by the resistors and transistors of the RF amplifier while the flicker noise of MOSFET devices is not critical. The thermal noise of a MOSFET device includes gate noise and drain current noise [6]. For calculation simplicity, the drain current noise source stays in the module of G_m-core and the gate noise source is, on the contrary, placed in the preceding interface module. The noise of $H_{IF,c}$ and $H_{IF,o}$ is also merged into the preceding G_m-core modules. Consequently, three noise sources I_{n1}, I_{n2} and I_{n3} are adopted to describe the noise performance.

2.3.4 Nonlinearity

The UWB LNA is assumed weakly nonlinear and then modeled with Taylor series expansions for its transfer function [7]. Where x(t) and y(t) are the input and output signals.

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \cdots\cdots \quad (3\text{-}1)$$

In addition, the nonlinear effect is dominated in the second stage of the UWB LNA. Therefore, the nonlinearity is simply related to the third order coefficient (α_3) of Taylor series in $H_{Gm,2}$ and its initial value is set to be

$$a_3 = \frac{4}{3}\frac{A_V}{A_{IIP3}^2} \quad (3\text{-}2)$$

2.4 **Performance Results**

In this section, we compare the analog performance between transistor level circuit and behavior model. The Figure 11 and 12 shows the comparison results of input/output impedance (I/O interface) which include the real part and the image part. In order to predict the performance of system simulation, the input/output impedance characteristics of behavior model must be close to transistor level circuit in the pass band of the target amplifier which operates from 2.7 to 8.5 GHz. From Figure 11 and 12, we can observe that the input/output impedance between behavior model and transistor level circuit are consistency in the pass band for both real part and image part. In the pass band, the RMSE (root mean square error) are less than 1.75 Ohm and 1.59 Ohm for real part and image part of input impedance, and 0.86 Ohm and 0.82 Ohm for real part and image part of output impedance.

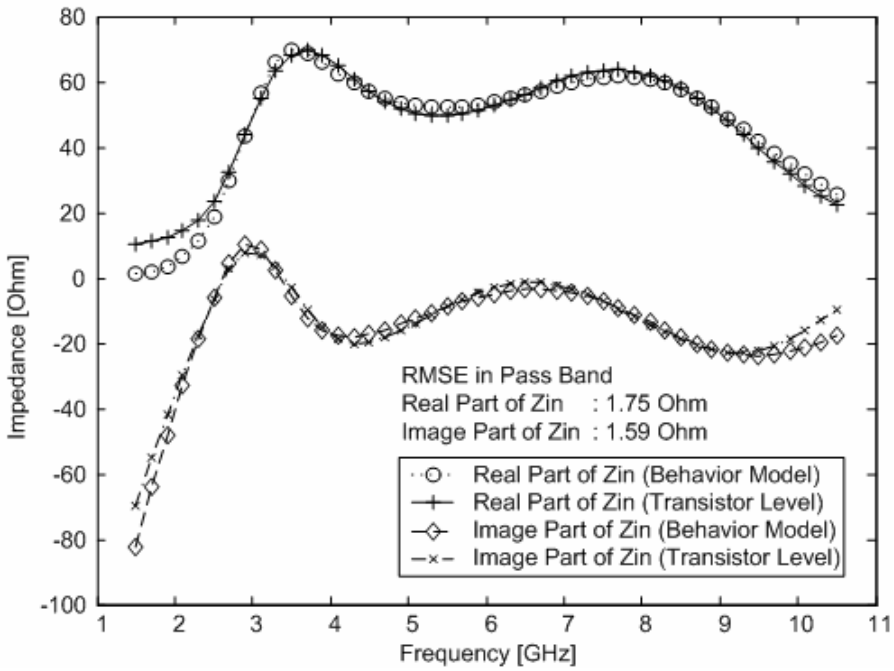


Figure 11 Comparison of input impedance.

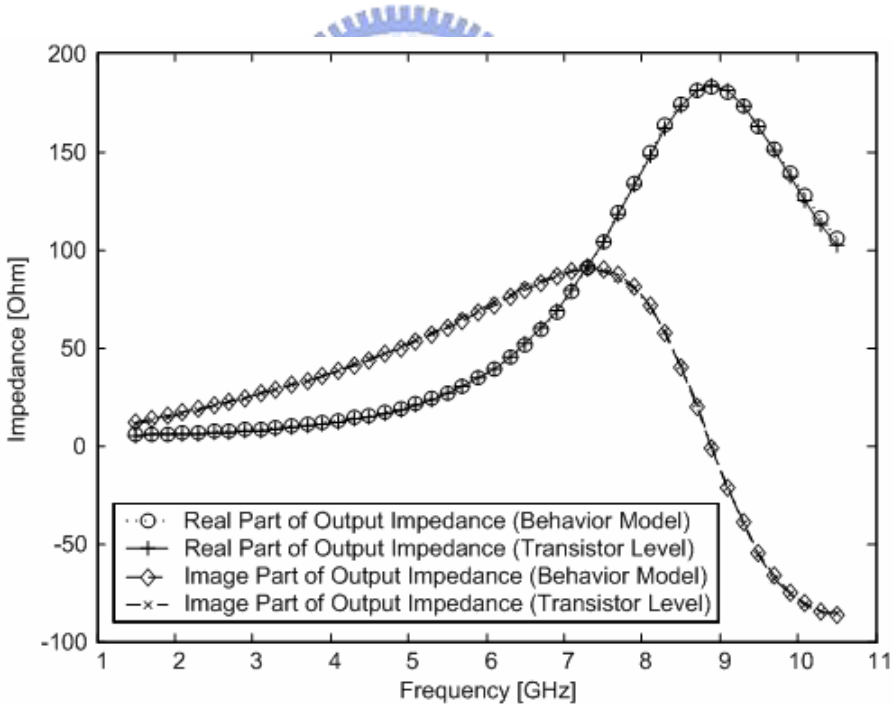


Figure 12 Comparison of output impedance.

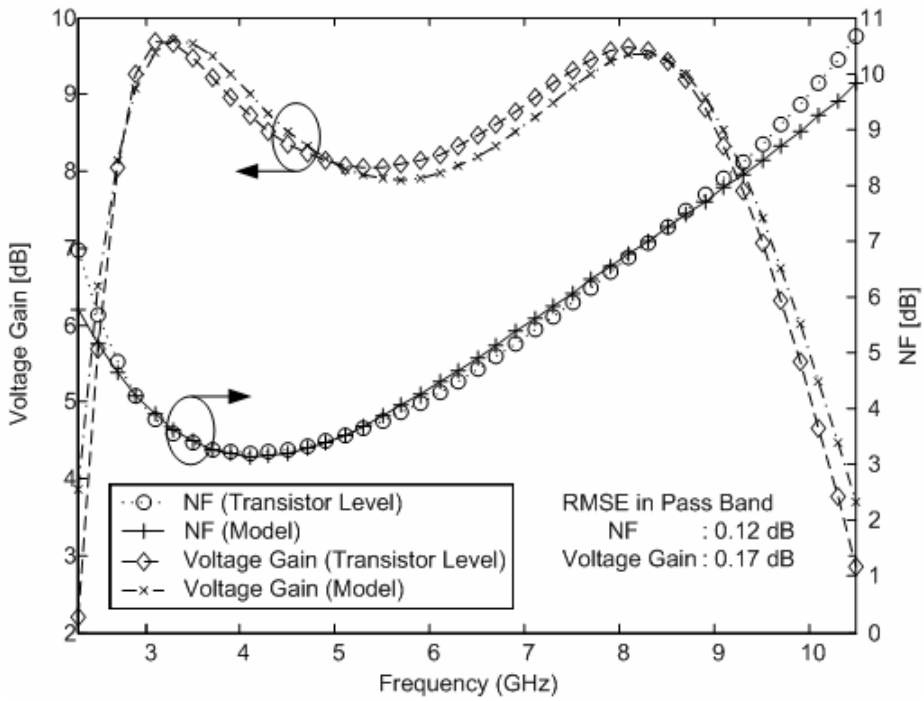


Figure 13 Comparison of voltage gain and NF.

The comparison of voltage gain and NF are shown in Figure 13. The RMSE in pass band is less than 0.12 dB and 0.17 dB for NF and voltage gain, respectively.

The nonlinearity simulation of the UWB LNA is performed by a two-tone test with a 4.125 MHz spacing. The α_3 was selected to be -1.8, so the input IP3 and P_{1dB} agree with the transistor level simulation. The α_3 is optimized in the second amplification stage, and the nonlinearity performance versus frequency has the same trend with the transistor level simulation. From Figure 14, we can find the RMSE variation of the input IP3 and P_{1dB} are less than 1.05 dB and 0.91 dB.

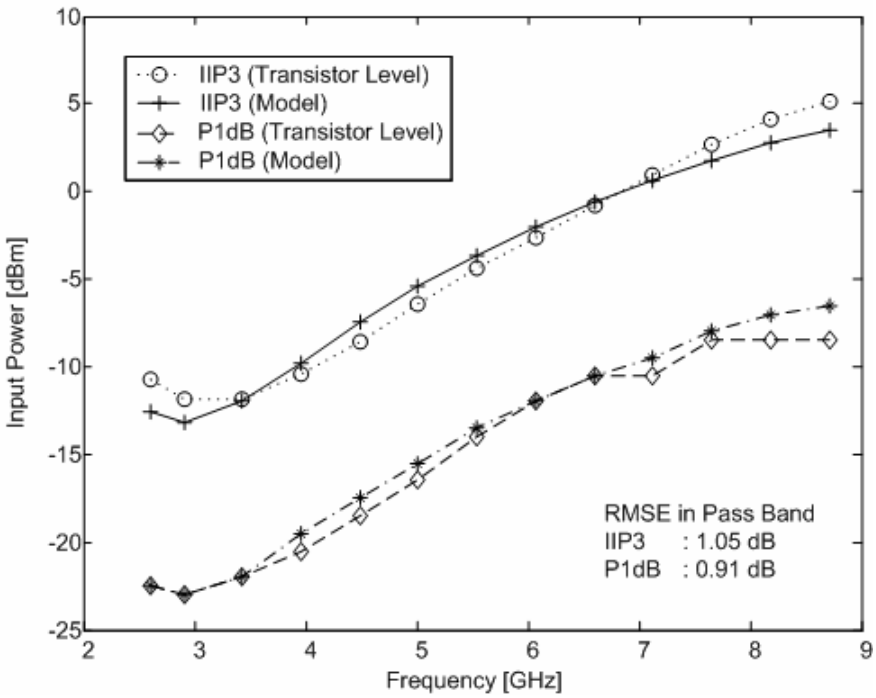


Figure 14 Comparison of input IP3 and P_{1dB} in the frequency band of interest.

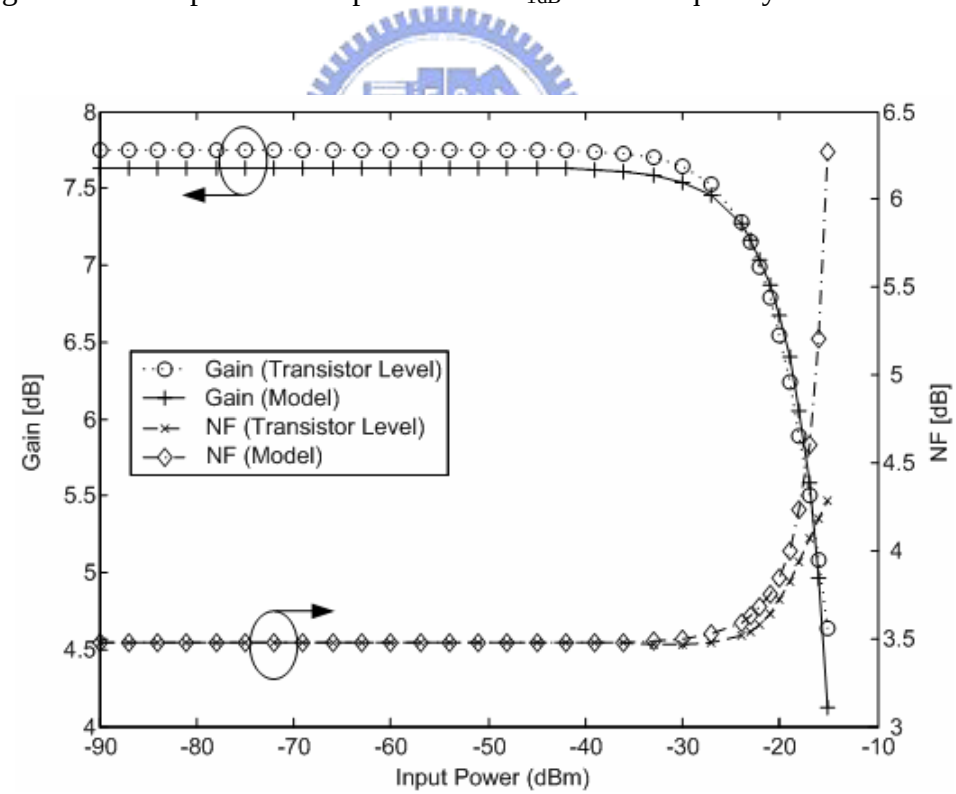


Figure 15 Comparison of NF and gain with sweeping RF power at 5.016 GHz.

We also sweep the input power to observe the gain and NF performance at 5.016 GHz.

Figure 15 shows the gain and NF are consistency if the input power is less than input P_{1dB}. It means that the behavioral model can be used before the large signal starts to degrade the performance. Since the input power of UWB LNA is always chosen to be small, the behavior model is suitable to the system simulation.

2.5 **System Simulation Platform**

2.5.1 RF/Baseband Co-Simulation Environment

Since the analog performance of behavior model agrees well with the transistor level, we replace the transistor level circuit with the behavior model in system co-simulation. Figure 16 shows the RF/Baseband co-simulation environment which is supported by the Multi-Band OFDM UWB design library in Agilent ADS platform. The “Baseband Amplifier” in Figure 16 is an ideal amplifier which can be used in baseband simulation environment. An analog circuit can be used in this environment for RF/Baseband co-simulation when we enable the “Analog Amplifier” and disable the “Baseband Amplifier”. The target UWB LNA can be utilized in the block of “Analog Amplifier”. Figure 17 shows the circuit of “Analog Amplifier”. We can choose either behavior model or transistor level in the block of “Analog Amplifier” to compare the UWB LNA system performance with the transistor level and

behavior model. The gain of the variable gain amplifier (VGA) is regulated to normalize the input power of UWB receiver.

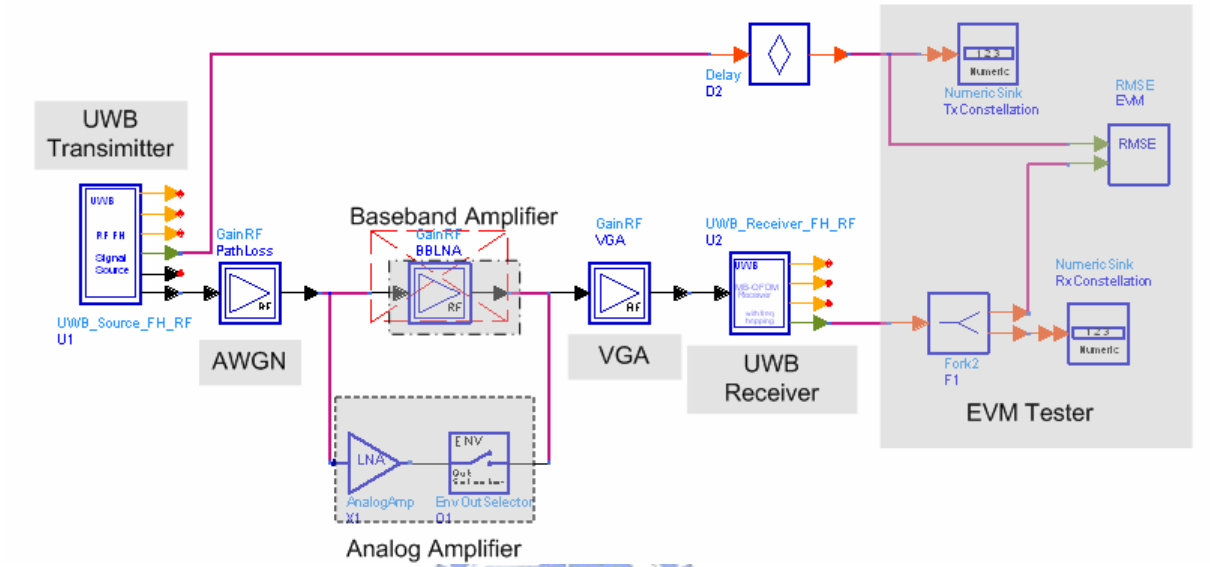


Figure 16　RF/Baseband co-simulation model.

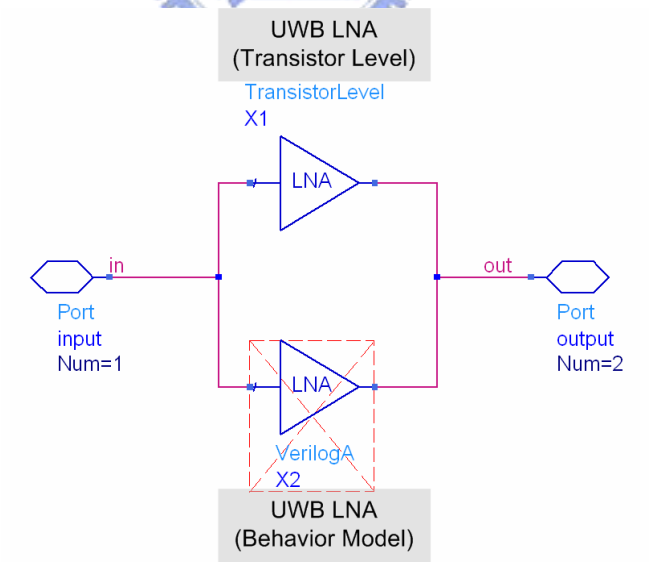


Figure 17　RF and Analog receiver behavior model.

2.5.2 System Level Performance

Error vector magnitude (EVM) simulation is performed based on the platform in figure 16 with the Multi-Band OFDM UWB design library in Agilent ADS and the unified RF behavior model. Using the circuit envelope simulator, the platform allows cosimulating the baseband algorithms and RF Verilog-A models. The input signal is 480-Mbps OFDM modulated at 5.016 GHz with power level sweeping from −72.8 to −27.8 dBm. The simulation results shown in Figure 18 agree well with those of the transistor-level LNA with EVM RMS error less than 0.79% and the simulation time for all power sweeps is reduced 87%. The simulation results verifies the accuracy of the unified RF behavior model and demonstrates great efficiency. The simulation time in transistor level becomes longer for the larger input power due to the nonlinearity in transistor level circuit becomes severe, and increases the iteration of the simulator. The behavior model, on the other hand, doesn't show the same increase of iteration.

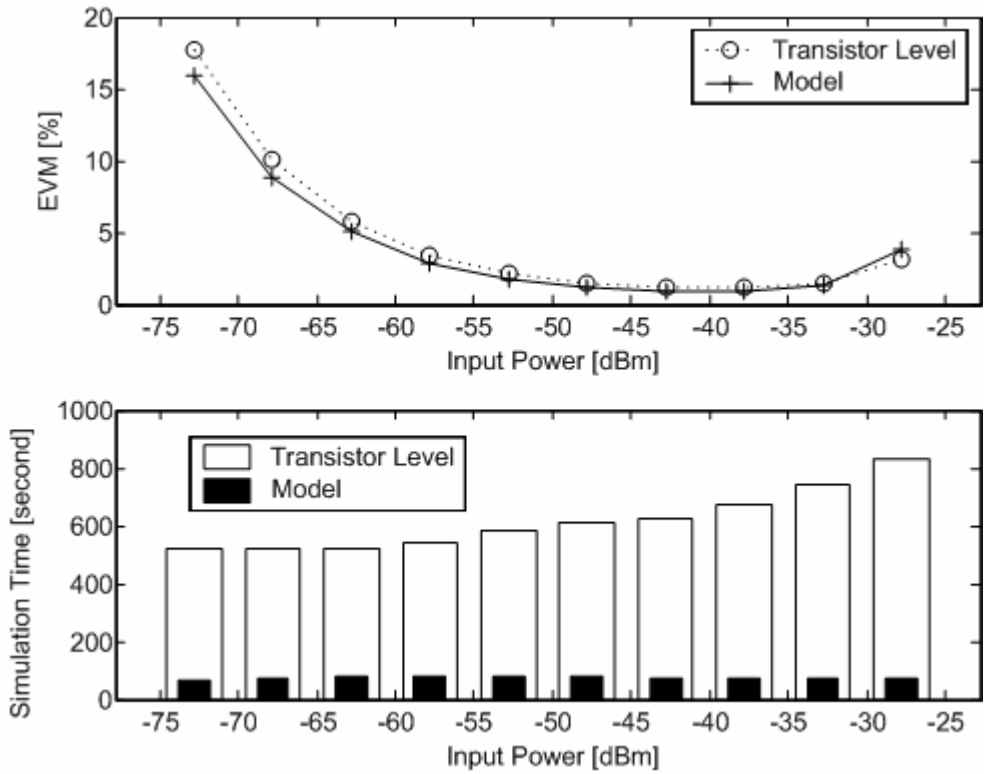


Figure 18 Comparison of UWB system EVM simulation results.

Chapter 3

Capacitive Cross-Coupling UWB LNA

A design example of broad band LNA with input matching using band pass filter is modeled in in previous chapter. The NF of the LNA in chapter 2 increases rapidly in high frequency, therefore the topology presented in chapter 2 is not suitable for UWB application. We propose a LNA topology which can achieve wideband matching, flat NF and gain from 3.1 to 10.6 GHz for UWB application. In this chapter, section 3.1 shows the design considerations and recent researches for wideband LNAs. The capacitive cross-coupling technique is chosen for UWB application, and we discuss this topology in section 3.2. Section 3.3 discusses the UWB LNA with CCC technique in the first gain stage. Section 3.4 shows the second gain stage of the UWB LNA. Section 3.5 discusses the performance of the overall UWB LNA with CCC technique. Section 3.6 summarizes this UWB LNA design.

3.1 Design Consideration of Wideband LNA

The LNA is the first module in the receiver path, which affects the performance of signal

bandwidth and noise figure of the system directly. There are several kinds of wideband LNA design topologies proposed in these years [5], [8]-[11], [14]. A wideband LNA can be partitioned to three parts by our behavior modeling method. The optimal design topologies of the three parts can be chosen by using the proposed behavior modeling method.

3.1.1 Basic Concerns

In designing a LNA, noise optimization and input impedance matching are usually more explored. In LNA circuits, noise sources close to the input have more contribution since they are amplified by the circuits and then appear at the output. That is the reason why the input network and the input devices are the main targets in noise reduction. Resistors are not good for input matching in LNA designs because they produce lots of thermal noise. While on-chip spiral inductors are widely used for impedance matching, they do generate thermal noise due to low quality factor; i.e. noticeable parasitic resistance. However, it is hard to accomplish the noise matching and input matching simultaneously especially, especially for a broadband LNA.

Inductive source degeneration is widely employed for input match in the narrow-band design [7]. It provides a real term $\omega_T L$ for the input impedance while generating little noise and consuming tiny voltage headroom, and the real term is independent of frequency. It is

also found in the broadband design when the input impedance is concluded in a band-pass filter [5], [8]-[9].

Common gate topology can easily achieve broadband matching. The input impedance will be $1/g_m$ and equal to source resistor [7]. The input impedance is in series with source resistor. However, the minimum noise figure will be larger than 3 dB. It's not suitable for UWB system.

3.1.2 Recent Research Reviews on Broadband LNA

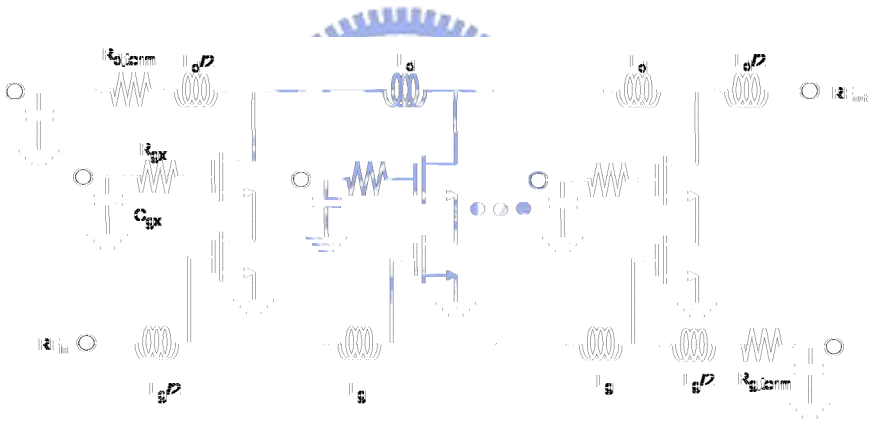


Figure 19 Distributed amplifier

Several LNA design techniques had been reported for broadband communication applications. The well-developed distributed amplifier is known as its wide bandwidth. The wideband performance of the distributed amplifier is dependent on the same signal delay of each stage. However, as shown in Figure 19, it requires many stages to get wider bandwidth. Each stage of the distributed amplifier needs chip inductors and consumes DC power. For

UWB application, many stages consumes large area due to the many chip inductors and much power. [10].

Broadband matching can be achieved by employing common-gate topology. The drawback of common-gate is the poor noise performance. A common-gate LNA was proposed to cancel the noise contribution from the input of common-gate stage as shown in Figure 20 [11]. Shunt-peaking and stagger tuning techniques are used to have flat gain form 3.1~10.6 GHz. The noise canceling bandwidth is, however, limited when the load impedance is relative to frequency.

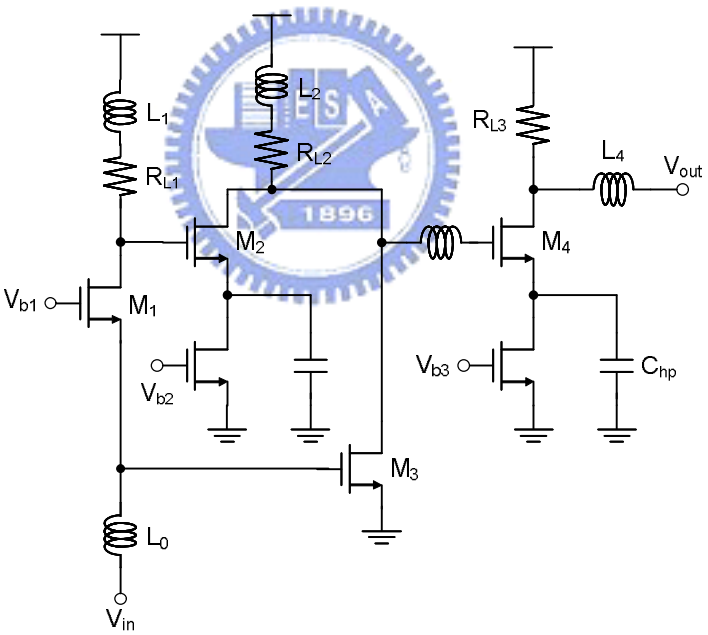


Figure 20 A broadband noise-canceling CMOS LNA

A capacitive cross-coupling technique was proposed to have the noise contribution form input MOSFETs [12]-[13], as shown in Figure 21. Since loads of the differential pair is

equivalent, the noise cancellation ability won't reduce even though the operation frequency is different. In this topology, if the noise parameter of the transistor, γ, is equal to 1, the minimum noise figure is larger than 1.76 dB, and it is not good enough for some systems.

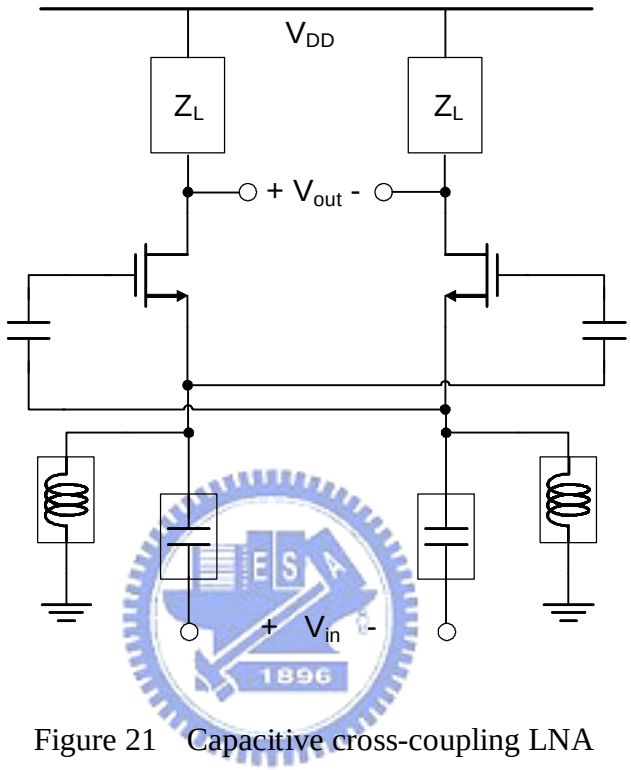


Figure 21 Capacitive cross-coupling LNA

The LNA employing stagger tuning technique consists of two common-source stages with different resonant frequencies to extend the bandwidth. A current reuse topology is used in this LNA to reduce the DC power consumption. The inductive source degeneration is used together with a three-section band-pass Chebychev filter to provide broadband input match [5], as shown in Figure 22. The noise optimization used in narrow-band design is employed and in-band average noise figure is optimized. The design begins with narrow-band-like topology and results in good broadband performance. However, there are many inductors in

input matching circuit, and the chip area becomes large.

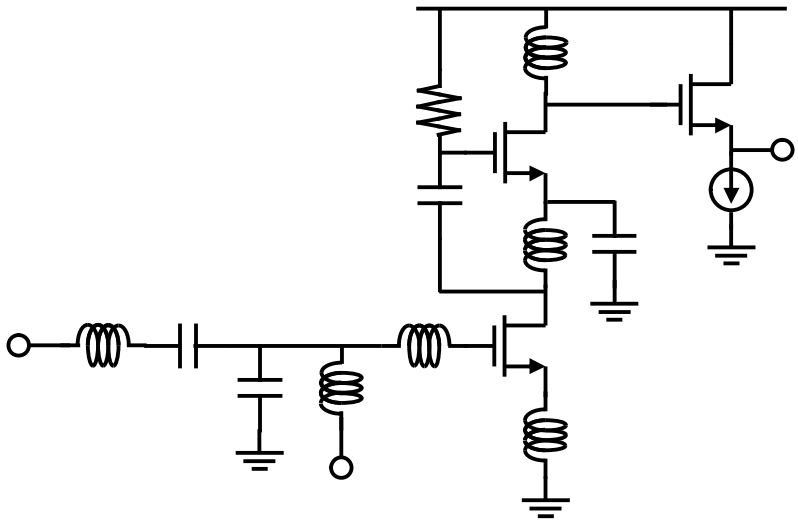


Figure 22　A wideband LNA with band-pass filter for input matching

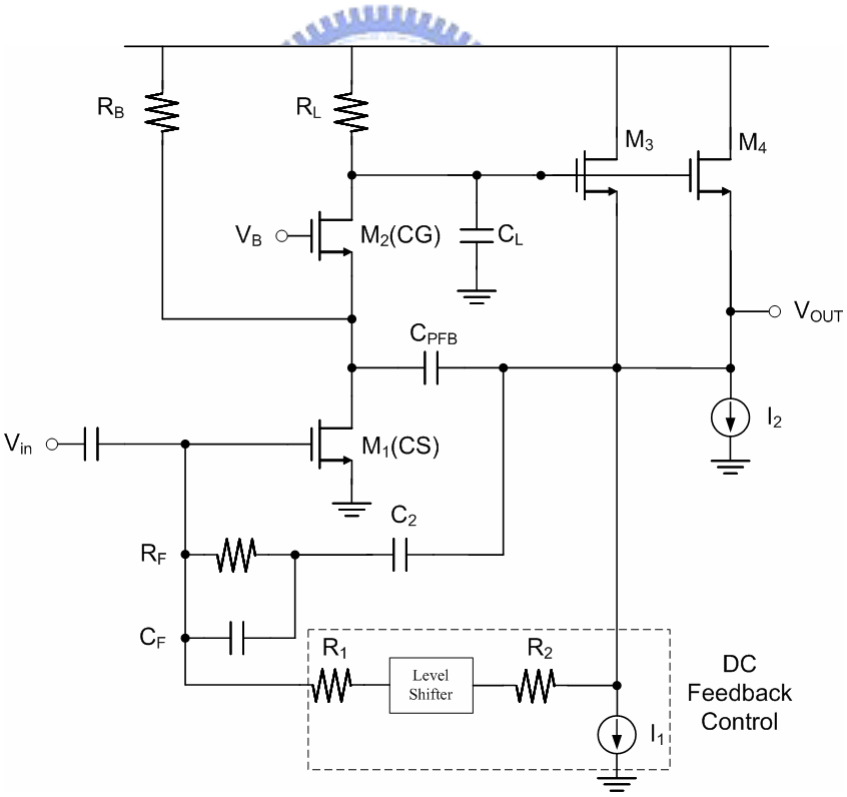


Figure 23　Resistive-Feedback CMOS LNA

A resistive feedback CMOS LNA is proposed to achieve DC to 8GHz bandwidth with large

gain and low noise figure [14], as shown in Figure 23. The chip area of this circuit is respectably small owing to no passive inductors in the circuit. The transistor M_3 is an active inductor, and the capacitor C_{PFB} compensates for parasitic capacitance C_L and increase bandwidth. The resistive feedback can not only provide for matching but also flat gain, but the bandwidth of resistive feedback is hard to achieve 3.1 GHz to 10.6 GHz for specification of UWB system.

3.1.3 Summary of Wideband LNAs

Several LNA design techniques had been reported for broadband communication applications. Several methods to obtain wideband impedance matching, noise matching and flat frequency response described above. We summarize the techniques for wideband operation in Table 3 and wideband matching in Table 4. We can have a flat frequency response by combining more than one method in Table 3, but the matching method in a circuit must be only one. To choose a suitable topology for matching circuit can dominate the performance of the LNA.

Table 3. Flat frequency response methods.

Techniques of Flat Frequency Response	Drawbacks
Shunt-Peaking	**Consumes DC power in resistor**
Feedback	**Consumes large DC power**
Stagger Tuning	**Use more than one inductors**
Distributed Amplifier	**Large area and DC power**

Table 4. Broadband matching methods.

Topology	Broadband Impedance Matching	NF_{min}	NF (3.1~10.6GHz)	Power Consumption	Area
LC-Ladder	**Good**	**Good**	**Bad**	**Good**	**Large**
Feedback	**Bad**	**Good**	**Moderate**	**Bad**	**Small**
Capacitive Cross-Coupling	**Good**	**Bad**	**Good**	**Moderate**	**Small**
Common Gate with Noise Canceling	**Good**	**Good**	**Moderate**	**Moderate**	**Small**
Distributed Amplifier	**Good**	**Bad**	**Moderate**	**Bad**	**Large**

From Table 4, we can find that the capacitive cross-coupling topology can achieve wideband matching easily with moderate DC power and small chip area consumption. Especially, this topology has a flat NF from 3.1 to 10.6 GHz. It is, therefore suitable for UWB

applications. Once the input matching topology is determined, the circuit can use the shunt-peaking and stagger tuning techniques to achieve a flat gain from 3.1 to 10.6 GHz.

3.2 **Capacitive Cross-Coupling Amplifier**

In these years, common source and common gate gain stages are widely used in LNA design. In common-source gain stage, a source degenerate inductor can offer the resistive impedance, and the series gate inductor can cancel the capacitive impedance to achieve narrow band input matching [7]. For wideband input matching, the reactive part of input impedance must be cancelled within a wide frequency range. We can use the band pass filter, such as LC-Ladder filter which we present last section to cancel the reactive impedance over a wide bandwidth. The NF of common-source LNA will be better if the input quality factor, Q, is increased. The NF is constrained by the low Q on-wafer inductors.

The common-gate gain stage can not only achieve the g_m stage of an amplifier but also accomplish the input matching. The main drawback of common-gate amplifiers is the relatively high noise figure. Ignore the noise sources which generate from the passive components, a common gate LNA has the minimum noise factor [7]:

$$Noise\ Factor = 1 + g \tag{3.1}$$

Where γ is the coefficient of channel thermal noise. When the input impedance of

common-gate topology is matched to 50 Ohm, the NF is usually larger than 3dB. This topology is easy to perform wideband matching, but difficult to meet the noise requirement for UWB applications.

The capacitive cross-coupling (CCC) can be used for input matching and gain enhancement [12]-[13]. The noise factor of an amplifier is expressed as:

$$Noise\ Factor = \frac{Total\ noise\ power @ output}{Noise\ power @ output\ due\ to\ source\ only} \tag{3.2}$$

Since the noise sources from the MOSFETs in CCC are the same as common-gate gain stage, the gain enhancement characteristic can reduce the NF due to the output noise which is contributed from source noise becomes larger. The detail will be discussed latter.

In this section, the input matching, gain and noise performances will be demonstrated. A differential common-gate input gain stage with CCC is shown in Figure 24. I_{n1} and I_{n2} are the thermal noise from M_1 and M_2. Assume that C1 and C2 are large enough and we can ignore its impedance, the small signal of Figure 24 can be simply presented as shown in Figure 25.

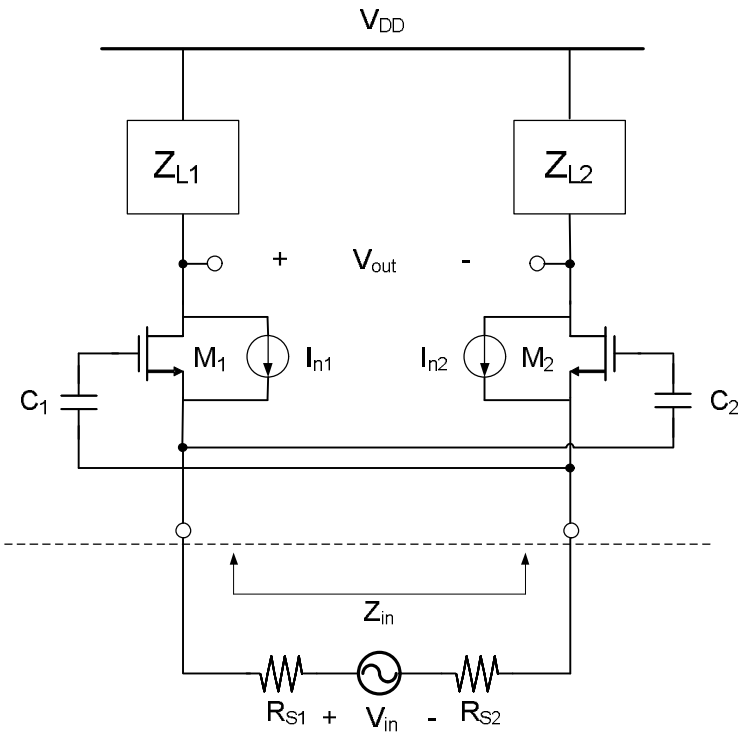


Figure 24 Gain stage of capacitive cross-coupling technique

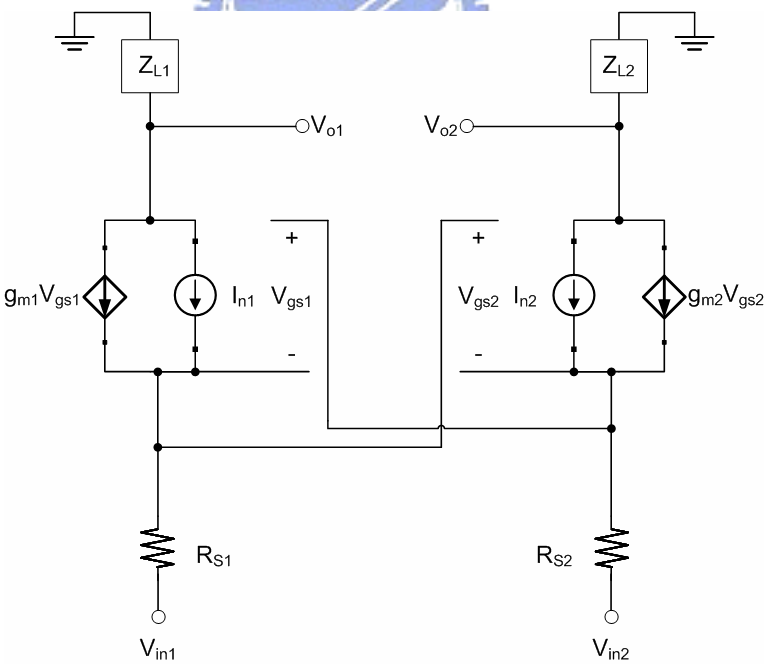


Figure 25 Small signal model of CCC technique

Let $Z_{L1} = Z_{L2} = Z_L$, $g_{m1} = g_{m2} = g_m$, $R_{S1} = R_{S2} = R_S$ and $I_{n1} = I_{n2} = I_n = 4\,kT\,\gamma\,g_m$, where the

Boltzmann constant k = 1.38×10^{-23} J/K, and T is the absolute temperature. We only consider the thermal noise in MOSFETs in Figure 25. The input impedance is equal to (detailed analysis shows in Appendix):

$$Z_{in} = \frac{1}{g_m} \tag{3.3}$$

When $g_m=1/2R_S$, typically is 0.01 A/V, the input matching can be achieved. The voltage gain of the CCC topology is given by (detailed analysis shows in Appendix):

$$A_V = \frac{V_{out}}{V_{in}} = \frac{V_{o1}-V_{o2}}{V_{in1}-V_{in2}} = 2g_m \times Z_L \times \frac{\frac{1}{2g_m}}{R_S + \frac{1}{2g_m}} = \frac{Z_L}{R_S + \frac{1}{2g_m}} \tag{3.4}$$

The noise contribution from source noise and I_n at output can be expressed as (3.5) and (3.6) (detailed analysis shows in Appendix):

$$V_{n,out,RS} = 2\times \left| \frac{2g_m \frac{1}{R_S}}{2g_m + \frac{1}{R_S}} \times Z_L \right|^2 \times 4kT \times R_S \tag{3.5}$$

$$V_{n,out,I_n} = 2\times \left| \frac{\frac{1}{R_S}}{2g_m + \frac{1}{R_S}} \times Z_L \right|^2 \times 4kT \times g \times g_m \tag{3.6}$$

The coefficient “2” in equation (3.5) and (3.6) represents the sum of the two noise sources from I_n and R_S in Figure 25. The noise factor can be calculated by equation (3.2):

$$Noise\ Factor = 1 + \frac{2 \times \left| \frac{\frac{1}{R_S}}{2g_m + \frac{1}{R_S}} \times Z_L \right|^2 \times 4kT \times g \times g_m}{2 \times \left| \frac{2g_m \times \frac{1}{R_S}}{2g_m + \frac{1}{R_S}} \times Z_L \right|^2 \times 4kT \times R_S} = 1 + \frac{g}{4g_m R_S} \tag{3.7}$$

If the input impedance matching is considered, the g_m is equal to $1/2R_S$, so the equation (3.7) can be represented by:

$$Noise\ Factor = 1 + \frac{g}{2} \tag{3.8}$$

From equation (3.8), we can find that the noise contribution from the thermal noise of MOSFETs is reduced to half. The CCC technique can minimize the thermal noise from the input MOSFETs in a common-gate topology.

The common-gate topology with noise canceling architecture can also cancel the thermal noise from the input MOSFETs [11], but the noise canceling ability will become poor due to the load impedance is varied with frequency. In CCC technique, the noise canceling mechanism is independent to frequency.

3.3 **The First Gain Stage with CCC Technique**

The gain stage with CCC topology can achieve wideband matching and low noise. In order to use this topology for UWB application, the gain flatness from 3.1 GHz to 10.6 GHz must

be achieved. When the CCC technique is used in the UWB LNA gain stage, the flat frequency response methods listed in Table 3 can be employed. The proposed CCC LNA uses the shunt-peaking and stagger tuning methods to achieve the flat frequency response from 3.1 GHz to 10.6 GHz.

The first gain stage is very critical for a LNA. The input matching is determined by the first gain stage, and the NF is also dominated by this stage. The CCC technique is used in the first stage owing to its excellent input matching ability and the relative low NF compared with general common-gate topologies. The CCC topology can have flat and wide frequency response if the wideband load is used. In the proposed CCC UWB LNA, we use the shunt-peaking technique to perform the wideband load, and the frequency response will be more flat than a single inductor. The Z_{L1} and Z_{L2} in Figure 24 are replaced by the shunt-peaking load, as shown in Figure 26. The R_{LS} and L_S are used as the shunt-peaking load. C_P and R_P are the parasitic capacitors at drain node of the MOSFETs. The parameter R_P is usually the output resistance of MOSFET, r_o, which doesn't generate any noise. Assume $Z_{L1} = Z_{L2} = Z_L$, it means that all parameters in Z_{L1} and Z_{L2} are the same, the noise factor of the CCC topology can be written by equation (3.9). The noise factor is simplified to equation (3.10) when $g_m = 1/2R_S$. From equation (3.9) and (3.10), we can find that the NF of the CCC topology is independent to R_P and C_P. Only the shunt-peaking components affect the NF. The NF can be minimized, if the R_{LS} and sL_S are infinity. Unfortunately, the R_{LS} and sL_S in the

circuit can't be arbitrary large. The sL_S is limited by the resonance frequency. The impedance of L_S starts to decrease when the operation frequency is higher than the resonance frequency. The R_{LS} is limited by the headroom of the circuit.

$$\begin{aligned} Noise\ Factor &= 1+\frac{g}{4g_m R_S}+\frac{Noise\ power@output\ due\ to\ R_{LS}}{Noise\ power@output\ due\ to\ source} \\ &= 1+\frac{g}{4g_m R_S}+\frac{2\times 4kT\times R_{LS}\times\left|\dfrac{\left(R_P \,//\, \dfrac{1}{sC_P}\right)}{(R_{LS}+sL_S)+\left(R_P \,//\, \dfrac{1}{sC_P}\right)}\right|^2}{2\times 4kT\times R_S\times\left|\dfrac{2g_m}{1+2g_m R_S}\times Z_L\right|^2} \\ &= 1+\frac{g}{4g_m R_S}+\frac{2\times 4kT\times R_{LS}\times\left|\dfrac{Z_L}{(R_{LS}+sL_S)}\right|^2}{2\times 4kT\times R_S\times\left|\dfrac{2g_m}{1+2g_m R_S}\times Z_L\right|^2} \\ &= 1+\frac{g}{4g_m R_S}+\left|\frac{(1+2g_m R_S)}{2g_m\times(R_{LS}+sL_S)}\right|^2\times\frac{R_{LS}}{R_S} \end{aligned} \tag{3.9}$$

$$Noise\ Factor = 1+\frac{g}{2}+\frac{2R_{LS}}{g_m\times(R_{LS}+sL_S)^2} \tag{3.10}$$

Equation (3.9) shows that the NF will be improved as g_m increased. There is a trade-off between NF and input matching. Figure 27 illustrates the NF and input matching of the first stage vs. g_m of the input transistors. The R_{LS} and sL_S are chosen to 400 Ohm and 30 Ohm in this figure. The NF improves with the increase of sL_S. The L_S must be larger than 1.54 nH in 3.1 GHz. This inductance is feasible for chip inductors. For input matching, the best value of g_m is equal to $1/2R_S$, where R_S is 50 Ohm. So the g_m must be equal to 10 mA/V. Besides the g_m, the parasitic capacitance at the input node will affect the input matching, too. Especially at high frequency, the effect of the parasitic capacitance is crucial. A parasitic capacitance is

considered at 10.6 GHz, and the comparison of the variance g_m and input matching is shown in Figure 27. As shown in Figure 27, once we choose the gm value to 14 mA/V, the NF is low and S11 will less than -10 dB.

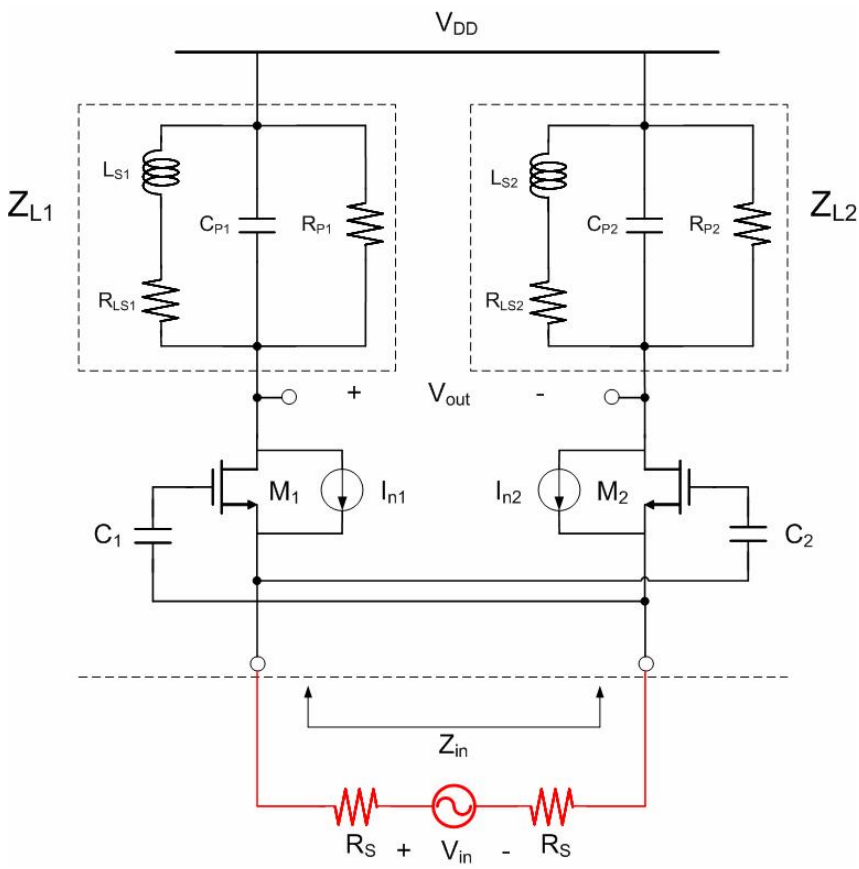


Figure 26 CCC technique with shunt-peaking load

When the g_m is determined, the size of the input transistors can be determined. Since the smaller size of transistors owning smaller parasitic capacitors, we can increase the overdrive voltage to keep g_m equal to the determined value. But the higher overdrive voltage will drive MOSFETs into velocity saturation region and makes its noise performance worse. A optimal width of the input transistor must be chosen.

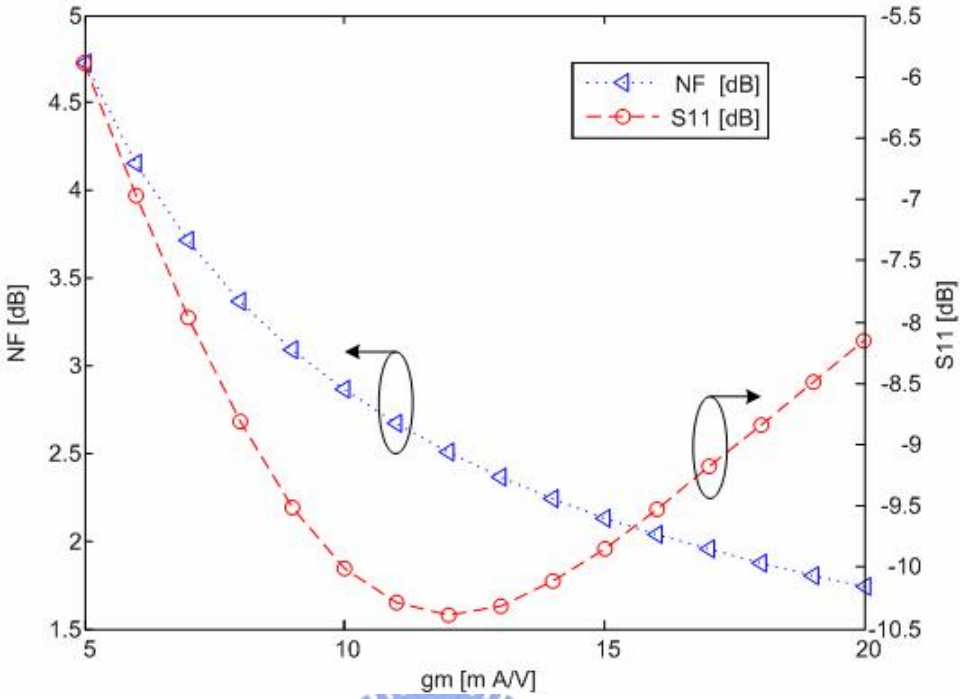


Figure 27 NF and S_{11} v.s. g_m

3.4 **The Second Gain Stage**

Although the first gain stage employs the shunt-peaking technique to extend the bandwidth of the UWB LNA, the bandwidth is still hard to meet the further wideband frequency range for UWB specification. As a consequence, we use the stagger tuning technique to extend the bandwidth. The schematic of the second stage is shown in Figure 28. The load of the second stage is equal to the first stage. The C_{P2} and R_{P2} are the parasitic capacitance and resistance at the output of the second stage. The R_{LS21} and L_{S21} are the shunt-peaking load for extend the bandwidth.

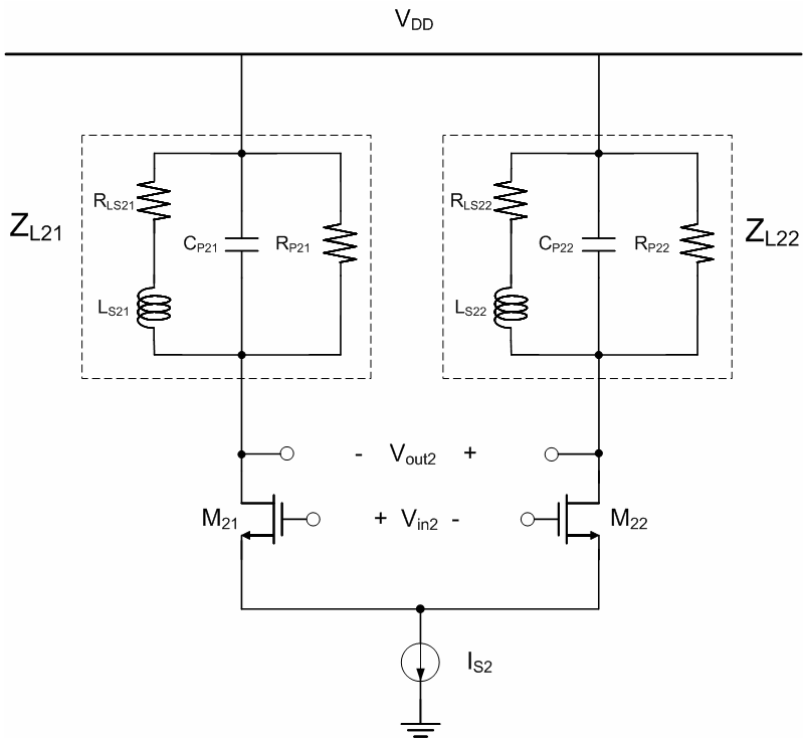


Figure 28 The second stage of the UWB LNA.

The second stage has the differential pair with current source, I_{S2}, which is performed by a NMOS transistor. There are some advantages in this topology.

First, the noise contribution from the MOSFETs in the first stage can be reduced to half if the circuit is perfect matched. If the circuit mismatch occurred in the first stage and the second stage, the gain of the UWB LNA will decrease, and the noise contribution from the MOSFETs in the first stage will be larger than $\frac{g}{2}$. When we cascade gain stages, the mismatch will become more serious. The ideal current source has infinity output impedance. When the current source is connected by the source of the differential pair, the source of the differential pair can be considered as virtual ground. The signal in each output of the second

stage has the component which is relative to $V_{in2}+$ - $V_{in2}-$. The result means that the noise contribution from the MOSFETs in the first stage is determined in the second stage. The noise contribution from the input MOSFETs is only influenced by the mismatch due to the first and the second stages. The mismatch from the latter stages, like mixer, buffer, VGA or filter won't affect the noise canceling advantage by CCC technique.

Second, the current source can bias the differential pair. Without the use of current source, there are two methods to bias the differential pair. One is to use the DC block to isolate the first and the second stage, and to bias the differential pair directly. The DC block must be implemented by the on-chip MIM capacitors. It must have some loss when the non-ideal capacitor is used to the DC block, the impedance of the non-ideal capacitor is not zero. In order to minimize the impedance of the MIM capacitor, the capacitor must be big enough. A problem occurs when the DC block is chosen as a large MIM capacitor, the parasitic capacitance becomes larger. The gain will be reduced at high frequency when the parasitic capacitance increased. There is another method to bias the differential pair. We can use the output voltage of the first stage to bias the differential pair. The drawback of this method is that the gate voltage of a MOS transistor is very sensitivity. Since the shunt-peaking technique is used in the load of the first stage, the problem becomes more serious. Because of the variation in the chip resistor is serious, the output voltage of the first stage has level shift when the load resistor is changed. The current of the differential pair may become much

larger or much smaller due to the variation of the resistor.

The differential pair bias by the current source can overcome above disadvantages. Since the current source fixed the DC current of the differential pair, the source voltage of the differential pair is allowed to variation in a range. The variation of the load resistor in the first stage won't influence the bias of the differential pair. Although the output voltage of the first stage is variable, the V_{gs} of the differential pair is fixed due to the flexible source voltage since the DC current is fixed by the current source. The second stage is not sensitive to the output of the first stage, and the linearity of the second stage becomes better. The DC block does not be used in this bias method. The first stage and the second stage can be connected directly. For the stagger tuning technique, the linearity is determined by the latter stage. It is a good advantage since the linearity is determined by the second stage.

3.5 **The Overall UWB LNA with CCC Technique**

After understanding the characteristics of the first stage and the second stage, we can start to design the UWB LNA. The overall UWB LNA with CCC technique for input matching is shown in Figure 29. The bias tee is used to provide the dc current path and the ac signal path to M_{11} and M_{12}.

After cascading the first stage and the second stage, the noise factor and gain can be

expressed in equation (3.11) and (3.12). The effect of C_1, C_2, L_{in1} and L_{in2} are omitted in (3.11) and (3.12), and we assume that $L_{S11} = L_{S12} = L_{S1}$, $R_{LS11} = R_{LS12} = R_{LS1}$, $L_{S21} = L_{S22} = L_{S2}$, $R_{LS21} = R_{LS22} = R_{LS2}$. The g_{m1} is the transconductor of M_{11} and M_{12}, and g_{m2} is the transconductor of M_{21} and M_{22}.

$$Noise\ Factor = 1 + \frac{g_1}{2} + \frac{2R_{LS1}}{g_{m1} \times (R_{LS1} + sL_{S1})^2} + \frac{2g_2}{g_{m1} g_{m2} Z_{L1}^2} + \frac{2R_{LS2}}{g_{m1} g_{m2}^2 Z_{L1}^2 (R_{LS2} + sL_{S2})^2} \tag{3.11}$$

$$A_V = g_{m1} Z_{L1} g_{m2} Z_{L2} \tag{3.12}$$

Where γ_1 and γ_2 are the coefficient of channel thermal noise of M_{11}, M_{12} and M_{21}, M_{22}.

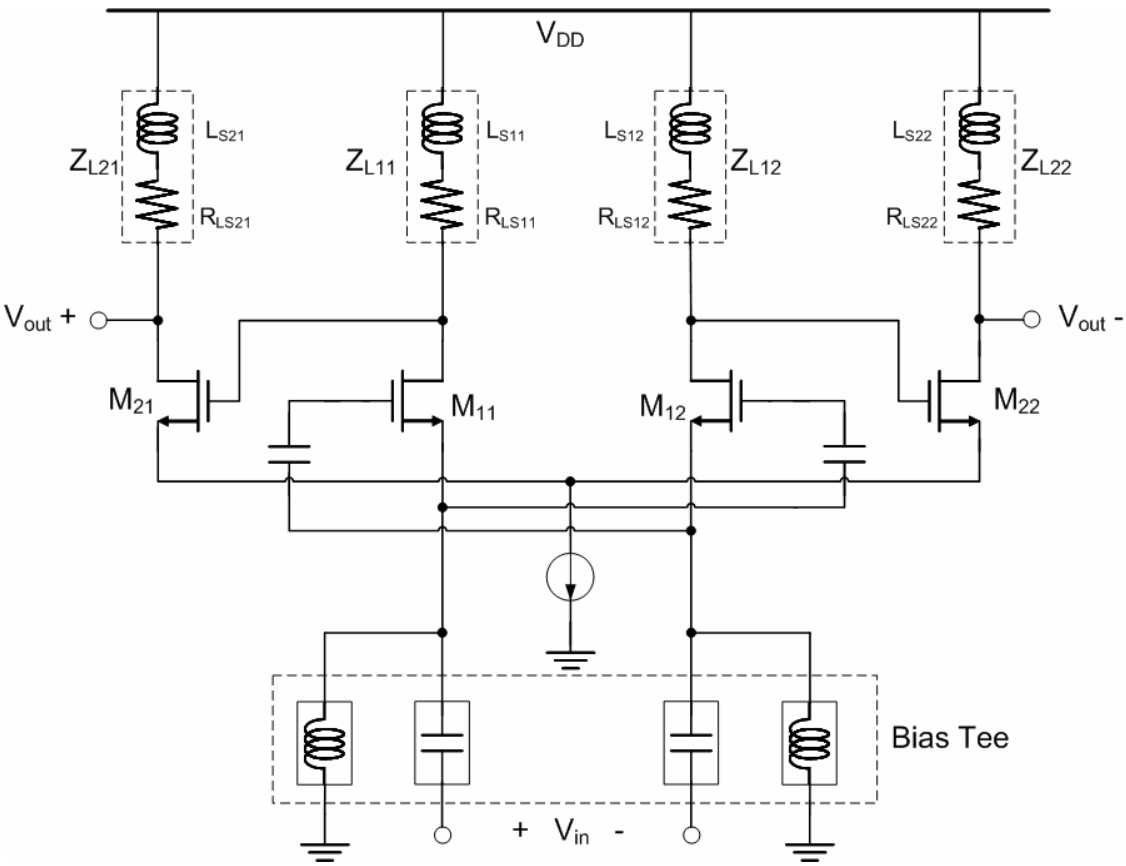


Figure 29 The overall UWB LNA with CCC technique for input matching.

In equation (3.11), the parasitic capacitance won't affect the noise contribution from the

first stage, but it will increase the noise contribution from the second stage. It is because the voltage gain is decreased in high frequency due to the effect of the parasitic capacitances. The noise contribution from the second stage will be relative large if the gain of the first stage becomes smaller, and the NF will become poor.

Equation (3.11) also tells us when sL_{S1} and sL_{S2} increased, the NF will be improved. The impedance of an ideal inductor will increase when the frequency is raised. Unfortunately, a practical inductor has resonance frequency due to the parasitic capacitor. When the operation frequency is higher than the resonance frequency of the inductor, the inductor will become to capacitive. The impedance of the inductor is no longer increased with the raised frequency. Since the NF will become poor in high frequency, we can choose the L_{S1} and L_{S2} which resonate at high frequency. The best resonance frequency is setting to the highest frequency of the UWB specification because the inductor has the largest impedance in the resonance frequency. The inductors can provide the gain of the UWB LNA in high frequency, and the gain in low frequency will be improved by the series resistors.

3.6 **Summary**

In this chapter, the CCC technique is used to perform a LNA for UWB application. It has good noise performance from 3.1 to 10.6 GHz. The performance is suitable for UWB system.

A UWB LNA with CCC technique will design by using behavior model in next chapter. And it will be used in UWB receiver front-end.

Chapter 4

Receiver Design by Using Proposed Behavior Model

The analysis of capacitive cross-coupling (CCC) LNA is described in the previous chapter. In this chapter, a design example for UWB LNA with CCC matching technique starts with behavior model is described. Section 4.1 discusses the structure of a coarse behavior model of CCC LNA. Section 4.2 discusses how to design a CCC LNA by using the behavior model, and modified the behavior model after the transistor level circuit is performed. Section 4.3 discusses the concept of receiver front-end. Section 4.4 explains the design of mixer. The simulation results of the receiver front-end are shown in Section 4.5. Section 4.6 shows the measurement consideration and environment. Section 4.7 summarizes this receiver front-end design work.

4.1 Construct a Coarse Model of CCC LNA

A coarse behavior model can be easily constructed for a UWB LNA with CCC technique in

Figure 30. The structure of the behavior model is discussed as follows.

4.1.1 Input Interface

We simply use the single input structure to simulate the differential pair of CCC topology. Input interface is easily presented by a parasitic capacitor and a resistor. Equation (3.3) presents the real part of input impedance only, the parasitic capacitance must be considered in high frequency and wideband condition. For differential input, the input impedance is equal to $1/g_{m1}$ for 100 Ohm input matching. Since the single input replaces the differential input, the input resistor R_{in} in figure 30 is selected to $1/2g_{m1}$ for 50 Ohm impedance matching, and the value of C_{in} is considered by the pad capacitor and C_{gs1}, where g_{m1} and C_{gs1} are the transconductor and gate-source capacitor of the input transistor.

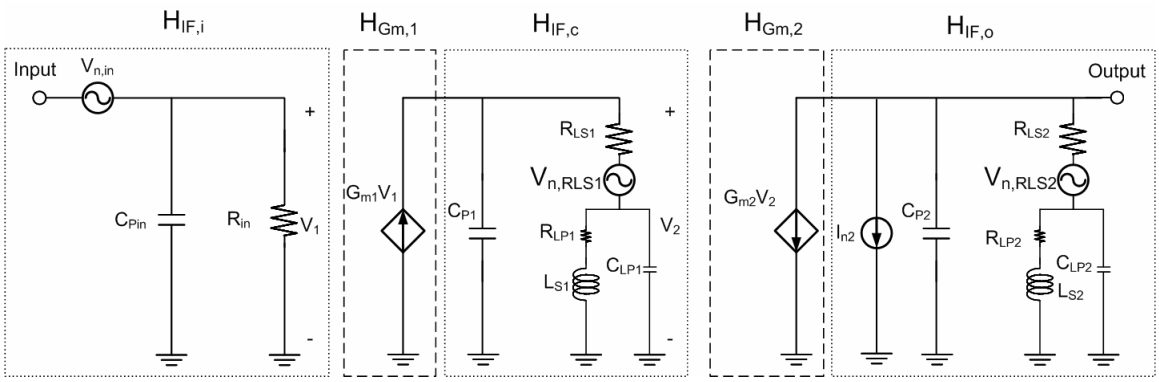
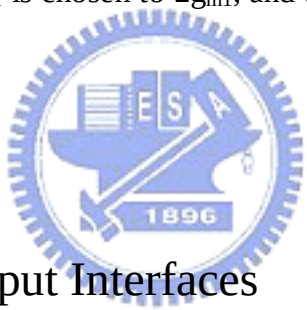


Figure 30　The behavior model of UWB LNA with CCC technique

4.1.2 Gain Stage

In order to obtain the flat frequency response, the stagger tuning technique is used in this circuit. There are two gain stages and three interfaces in this LNA. The first gain stage, $H_{Gm,1}$, is CCC topology, which has common-gate and common-source characteristics simultaneous. In this model, we use the voltage controlled current source (VCCS) with positive gain to exhibit the gain of the first stage. The second stage, $H_{Gm,2}$, is a simple common-source differential pair, a VCCS with negative gain can exhibit it. In order to maintain the gain to equation (3.4), the value of G_{m1} is chosen to $2g_{m1}$, and the value of G_{m2} is chosen to the g_m of the differential pair.



4.1.3 Center and Output Interfaces

The center and output interface are relation to the frequency response, and the output interface is also relation to output impedance. In order to achieve flat frequency response, shunt-peaking technique is used in center and output interfaces. In equation (3.11), the inductors of these two interfaces are chosen to resonant at high frequency due to achieve the flat NF in pass band. The parameters L_{S1}, R_{LS1}, C_{LS1}, and L_{S2}, R_{LS2}, C_{LS2} are the parasitic parameters of inductors in the center and output interfaces. The parameters of R_{S1} and R_{S2} are chosen to extend the bandwidth of the load. We consider the parasitic capacitance, C_{P1} and

C_{P2}, at the center and output interfaces. The best value of C_{P1} and C_{P2} can resonant with L_{S1} and L_{S2} at high frequency. The resistors of R_{S1} and R_{S2} provide the gain in lower frequency, and the L_{S1} and L_{S2} provide the gain in higher frequency. The frequency response can become flat from 3.1 GHz to 10.6 GHz.

4.1.4 Noise Sources

The noise source in this model is different than that of the model in chapter 2. In chapter 2, the passive components in the model provide no noise, and use three noise sources to fit the noise performance. That is the method to model an existed circuit. In this chapter, we construct a behavior model first and using this behavior model to design a circuit. We must place the noise sources by physical viewpoint. The resistors, R_{S1}, R_{LS1}, R_{S2} and R_{LS2} generate noise power with value 4kTR. A noise source is placed at input, which retain to the NF like to equation (3.7). The noise source is chosen to $4kT/g_{m1}$. The noise source from differential pair is chosen to $4kTg_{m2}$.

4.2 **Design a CCC LNA**

After constructing and fine tune the coarse behavior model of CCC LNA in previous section, we can design the transistor level circuit. The coarse behavior model determines the

components parameters of transistor level.

4.2.1 Performance Comparison between the Coarse Behavior Model and Transistor Level

Section 4.2.1 shows the comparison of transistor level/behavior model. To achieve suitable input matching and good NF, the transconductors of the input transistors are chosen to 14.5 mA/V. After choosing the devices size from the coarse behavior model, the results are presented in figure 31. The UWB LNA is simulated with an ideal differential to single output buffer.

In figure 31, we can find that the input matching results between behavior model and transistor level have different trends. There are some critical points which we didn't consider in input matching circuit. The input impedance can't be presented by a resistor and a parallel capacitor only. In the transistor level, input matching become worse at high frequency, we can add the series inductors at input to cancel the capacitive effect, and the S_{11} will be large than -10 dB. Besides the input matching, the estimated parasitic capacitance in the coarse model is smaller than transistor level.

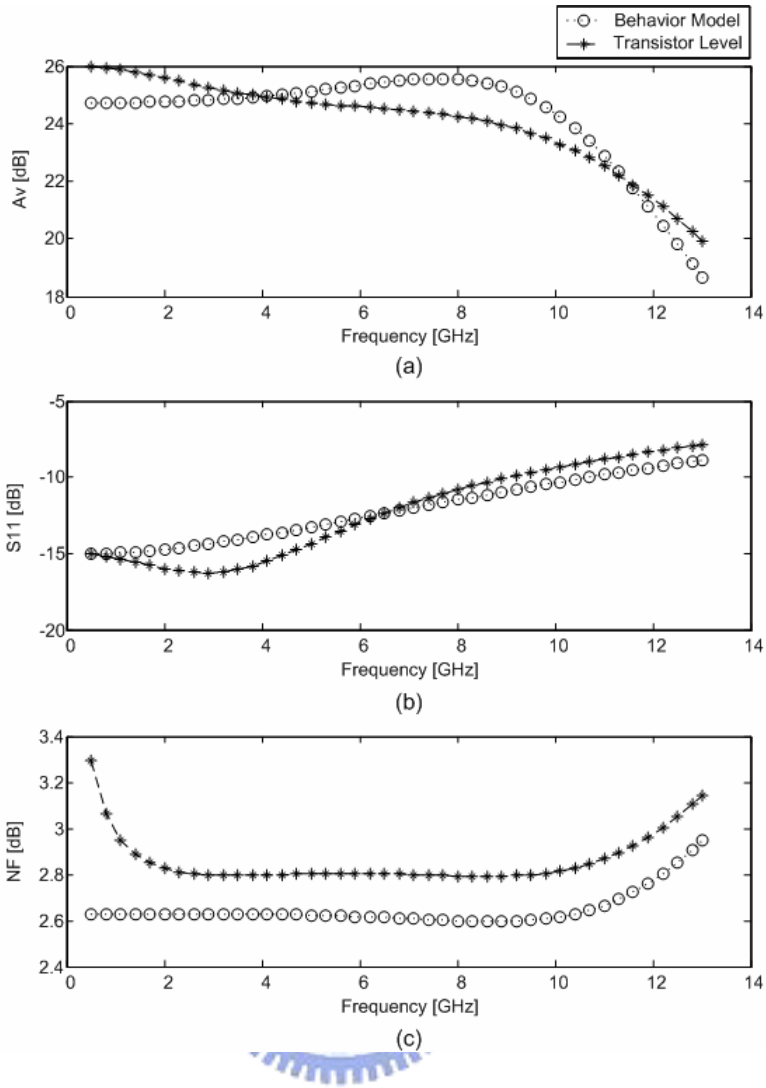


Figure 31 Simulation results of Behavior Model and Transistor Level,

(a) voltage gain, (b) S_{11}, (c) noise figure.

4.2.2 Modify the Behavior Model

From figure 31 (b), we can find that there is a low-Q resonance tank at 3 GHz. The information reveals that the inductance impedance appears in the input matching circuit. The impedance between drain and source of input transistors, C_{ds} and r_O, are not considered in

figure 25. These impedances provide a feedback loop between input and output of the first gain stage. After considering the impedances, the input impedance can be modified by:

$$Z_{in} = 2\times\left[(1/sC_{ds})+(1/2g_m)+r_O\right]+2\times\frac{Z_L}{r_O}\times\frac{sC_{ds}r_O+1}{sC_{ds}+\left(2g_m+\frac{1}{r_O}\right)} \tag{4.1}$$

The first term of (4.1) can be approximated to $1/2g_m$ since this impedance is relative small than others. Besides the term of $1/2g_m$, equation (4.1) shows that an impedance series to $1/2g_m$. From figure 31 (b), we can speculate that this term reveals the inductance impedance.

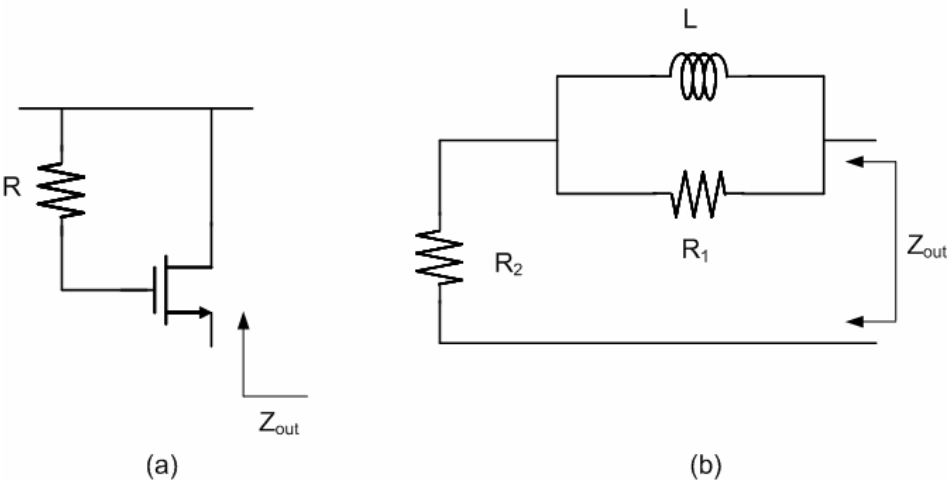


Figure 32 Active inductor, (a) schematic, (b) small signal circuit.

Figure 32 is the active inductor [15]. Assume $R >> 1/g_{mL}$, Z_{out} can be approximate to:

$$Z_{out} \approx \frac{sRC_{gs}+1}{sC_{gs}+g_{mL}} \tag{4.2}$$

where C_{gs} and g_{mL} are the gate-source capacitance and transconductor of the transistor. The values of the small signal circuit can be present to:

$$
\begin{aligned}
R_1 &= R - 1/g_{mL} \\
R_2 &= 1/g_{mL} \\
L &= \frac{C_{gs}}{g_{mL}}\left(R - 1/g_{mL}\right)
\end{aligned}
\tag{4.3}
$$

Compare (4.2) with the second term of (4.1), we can find the second term of (4.1) has the component of inductance impedance. To contrast between (4.2) and the second term of (4.1), the parameters in the second term of (4.1) can be presented to:

$$
\begin{aligned}
&C_{ds} \rightarrow C_{gs} \\
&r_O \rightarrow R \\
&2g_m + 1/r_O \rightarrow g_{mL}
\end{aligned}
\tag{4.4}
$$

Unfortunately, the active inductor in (4.1) has a coefficient Z_L/r_O which is relative to the frequency. And we can't reveal this phenomenon by the simple RLC circuit. In order to express this phenomenon, the $1/2g_m$ is series to a low-Q inductor which value must be optimized to fit the S_{11} of the transistor level.

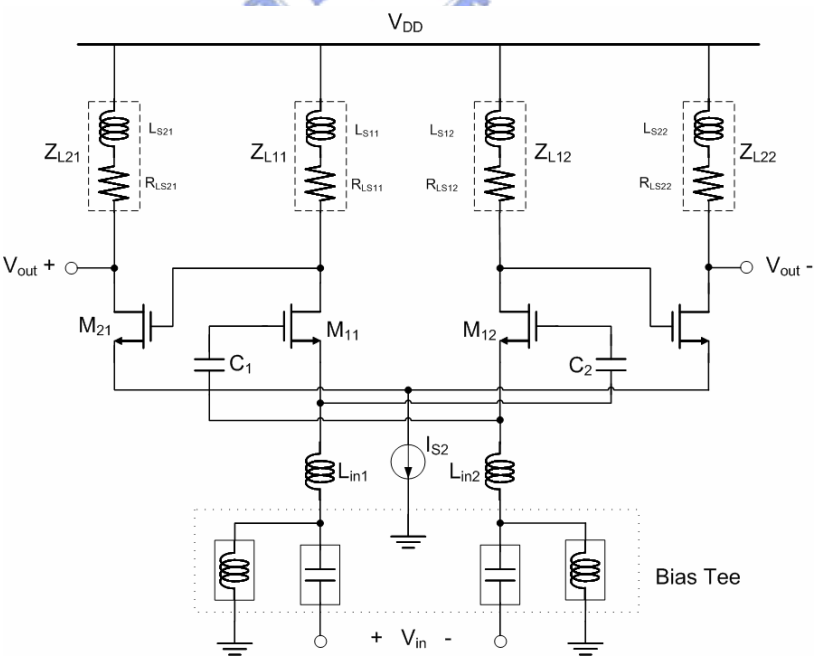


Figure 33 The proposed CCC LNA

Since the S_{11} in figure 32 (b) can't meet specification (< -10 dB) at high frequency, a series inductor can be placed at the input to cancel the capacitance impedance at high frequency and improve the input matching. The final circuit of the CCC LNA is shown in figure 33, and the modified behavior model is shown in figure 34.

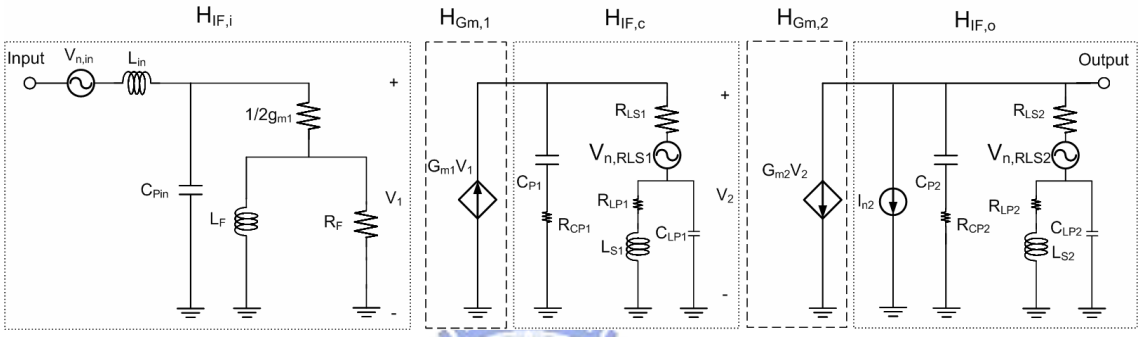


Figure 34 The modified behavior model of UWB LNA with CCC technique

After fine tuning, the results between the modified behavior model and transistor level are shown in figure 35. We can find that the input matching of the behavior model can fit the transistor level when the low-Q inductor is series to $1/2g_{m1}$. The input return loss is improved due to the series inductors, L_{in1} and L_{in2}.

The NF of transistor level is poor than behavior model at low frequency. It is because the behavior model only considers the thermal noise from the transistors and the series resistors. Other noise sources, like the gate noise and flicker noise of the transistors are not considered in behavior model due to design simplicity, and these noise elements are not the critical noise source for the NF performance in UWB system.

The analog characteristics of the transistor level can be fitted by the modified behavior model and can be used for system verification which mentions in chapter 2.

The pre-simulation result of the UWB LNA is shown in Table 5. In Table 5, we can observe that the LNA can meet the specification in Figure 1. We can use this LNA to UWB application.

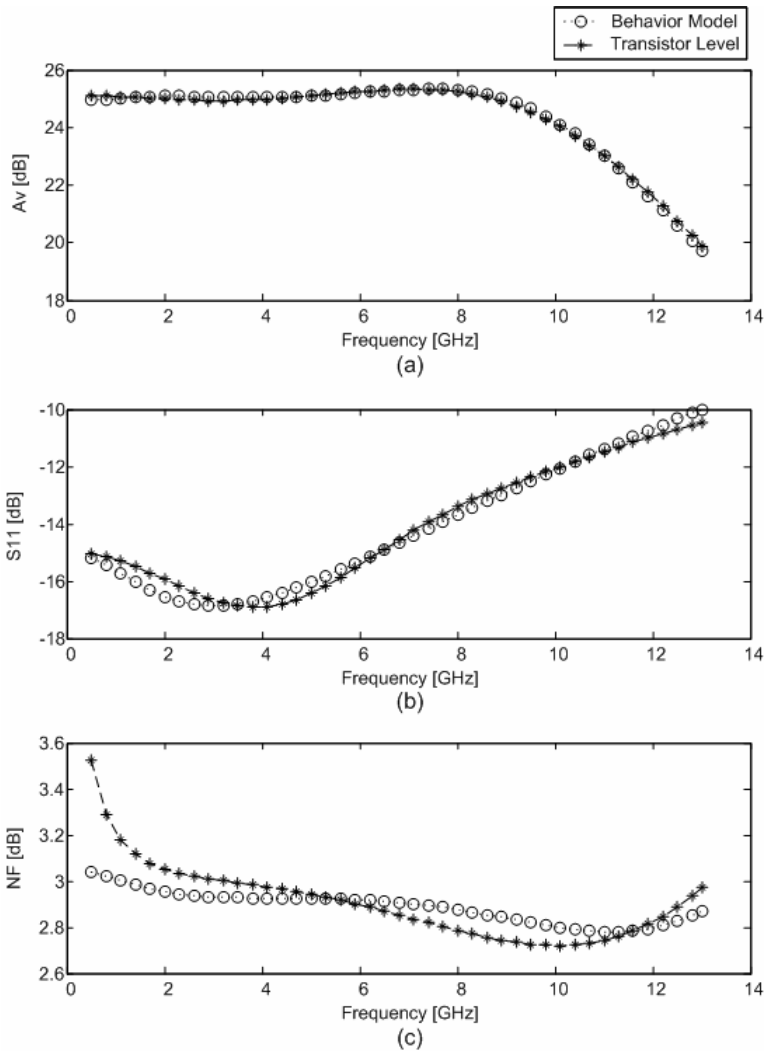


Figure 35 Simulation results of the modified Behavior Model and Transistor Level, (a) voltage gain, (b) S_{11}, (c) noise figure.

Table 5. Pre-simulation results of the UWB LNA with CCC technique.

	Spec.	CCC LNA (Pre-Simulation)
Technology	--	**0.18 μm CMOS**
Power supply	--	**1.8 V**
Bandwidth	**3.1 ~ 10.6 GHz**	**0.5 ~ 10.6 GHz**
Power consumption	--	**11.23 mW without buffer**
Voltage Gain	**19 dB**	**23.5 ~ 25.3 dB**
S_{11}	**< -10**	**< -11 dB**
NF (3.1~10.6 GHz)	**< 3.7 dB**	**2.72 ~ 3.53 dB**

4.3 **UWB Receiver Design with CCC LNA**

A wideband differential LNA needs wideband RF differential to single output buffer for measurement purpose. Because the wideband RF differential to single output buffer is difficult to implement, we add the mixer to down-converter the signal to lower frequency. And a baseband transformer can be used to transfer the differential signal to single-end signal at low frequency. The system architecture is shown in figure 1. Since this circuit is designed for on-wafer measurement, the quadrature modulation can't be measured in this environment. The quadrature modulation is not used in this design.

The direction-conversion architecture is used in this system. The advantages of direction-conversion architecture are presented in chapter 1.2. Here, we discuss the issues of

this architecture, such as DC offsets, even-order distortion, and flicker noise. The I/Q mismatch is also an issue of direction-conversion, since the quadrature modulation is not used in this design, we don't discuss the problem in this thesis.

4.3.1 DC Offset

When the downconverted band extends to zero frequency, extraneous offset voltages can corrupt the signal and saturate the following stages. The main cause of DC offsets is the strong LO signal leaking to RF port through capacitive and substrate coupling and causing the self-mixing leaking as shown in Figure 36. The problem of offset gets worse if self-mixing varies with time. This happens when the LO signal leaks to the antenna and is radiated and subsequently reflected from moving objects back to the receiver.

There are various means of offset cancellation. High pass filtering or capacitive coupling can be a good solution for wideband channels that contain little energy near DC. In the MB OFDM proposal, the subcarrier falling at DC (0th subcarrier) is not used, and the lower corner frequency can be higher than 2 MHz.

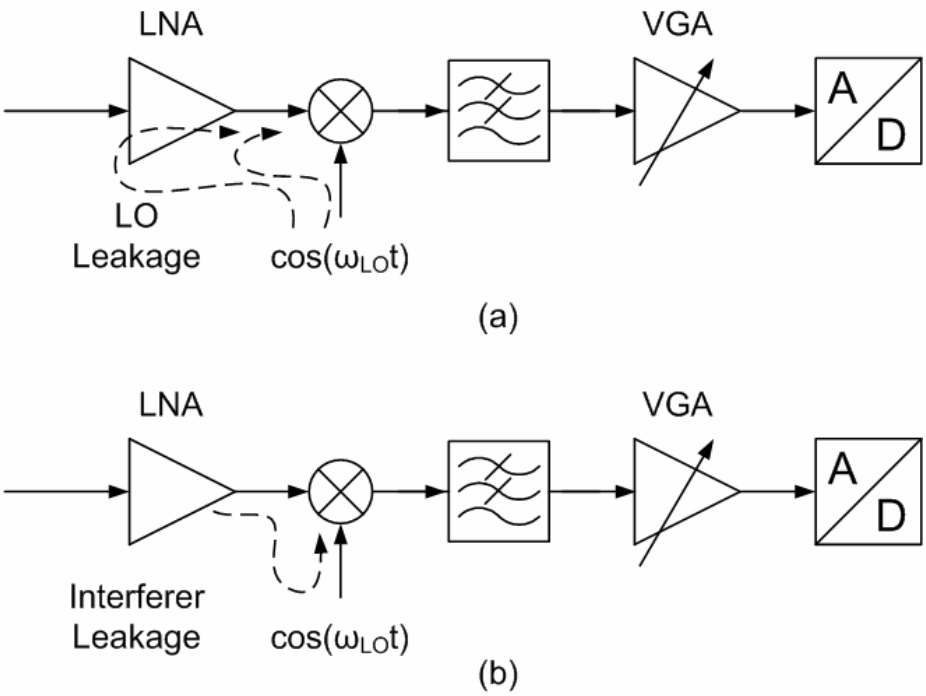


Figure 36 Self-mixing of (a) LO signal, (b) a strong interferer.

4.3.2 Even-Order Distortion

Suppose two strong interferers close to the channel of interest enter the LNA, the second order intermodulation distortion of the LNA will induce a low-frequency beat at the LNA output as shown in Figure 37. The mismatch of differential switching transistor pair results in direct feedthrough from the RF input to the IF output which corrupts the baseband signal. The RF port of the mixer also suffers from the same even order distortion effect. To mitigate the even order distortion, the LNA and mixer should present good second-order nonlinearity performance characterized by the second-order intercept point (IP2). Since the input of our CCC LNA is differential topology, and the second-order nonlinearity performance is,

therefore, good.

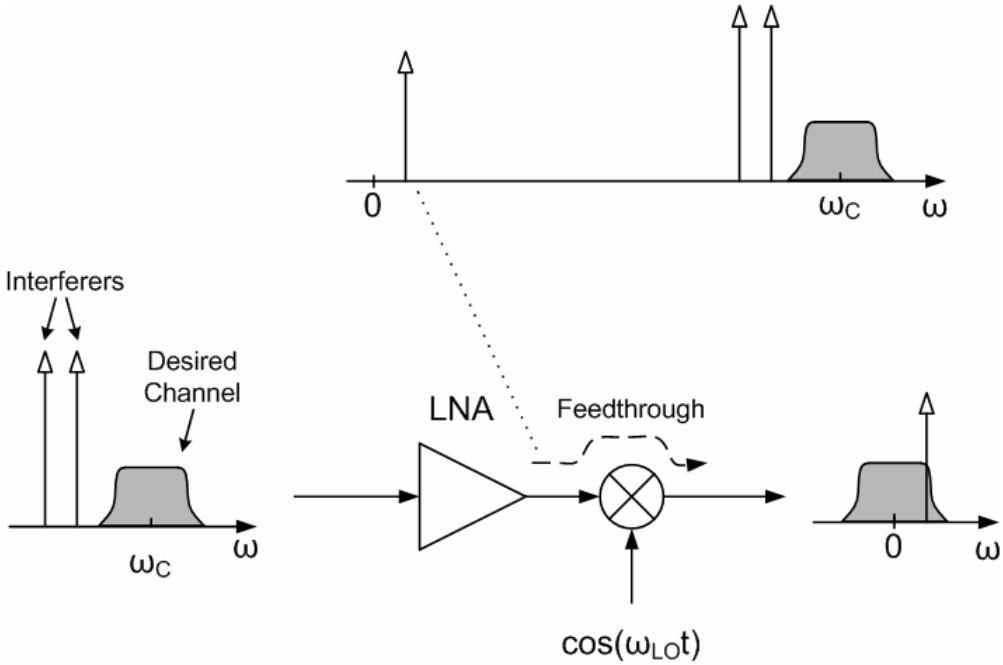


Figure 37 Effect of even-order distortion on interferes.

4.3.3 Flicker Noise

Since the downcoverted spectrum extends to zero frequency, the 1/f noise of devices significantly corrupts the baseband signal. This is a severe problem in the circuits employing MOSFETs. Several means may be applied to reduce the flicker noise in the receiver. In baseband circuits, the PMOS devices can be used to lower 1/f noise. Devices with larger size also help. An on-chip AC coupling capacitor between the LNA and the succeeding mixers can effectively prevent the 1/f noise at the LNA output from entering the mixers.

4.4 **Mixer Design**

A down-conversion mixer is used to convert the RF frequency to IF frequency. In the direct-conversion receiver structure, zero IF is required in the design. A double-balance passive mixer is used in this receiver front-end [16]. The passive mixer can be easily used in wideband application. The conversion gain of this passive mixer is equal to:

$$G_c = \frac{2}{p} \times \sin\left(\frac{p \times \Delta T}{T}\right) \times \frac{T}{\Delta T} \tag{5.3}$$

where ΔT is the equivalent turn-on time of the switch pair of the passive mixer, and T is the LO period. The conversion gain can increase due to the reduced equivalent turn-on time. When ΔT <0.6T, the conversion gain becomes positive. An output buffer is designed for measurement purpose. A source follower topology is utilized in this buffer. The passive mixer and output buffer are shown in Figure 38.

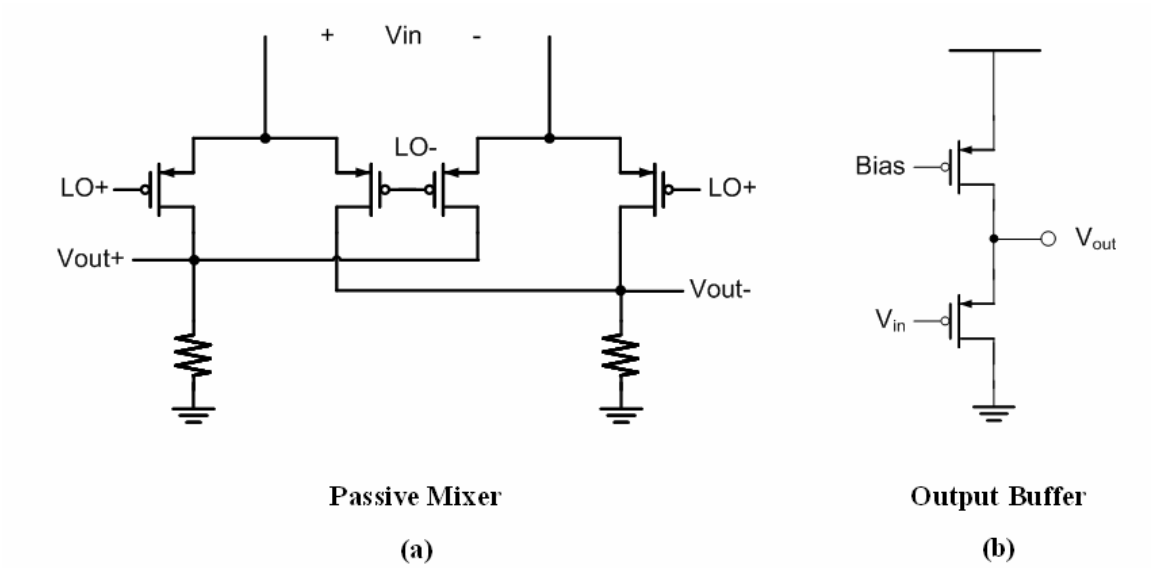


Figure 38 (a) Double-balance mixer, (b) output buffer

4.5 **Simulation Results**

A UWB receiver front-end is performed by previous design consideration. The circuit layout of the UWB receiver front-end is shown in Figure 39. The area of this circuit is 1.1 mm^2, and the core area of this circuit is less than 0.5 mm^2.

The results of post layout simulation are shown in figure 40 to 45. The conversion gain decreases and the NF increases with the increase of signal frequency higher than 8 GHz. The result is due to the parasitic capacitance of the circuit layout. The conversion gain and NF can be more flat with smaller inductors and resistors in the shunt-peaking load. There are some constraints for conversion gain and NF as shown in equations (3.11) and (3.12). The conversion gain and NF degrade with the reduction of the load. In order to meet the UWB system specs. in figure 2, the load values are chosen to meet the requirement of the conversion gain. The output buffer reduces the conversion gain of 7 dB in this design. In SoC design, the output buffer is not used in the system. After compensating the loss of the output buffer, the conversion gain can meet the specification.

In figure 41, when the IF frequency is near low frequency, the NF becomes higher which is due to the flicker noise. Input and output return losses are shown in figure 42 and 43. In pass band, the input return loss is less than -10.1 dB and output return loss is less than -14.9 dB.

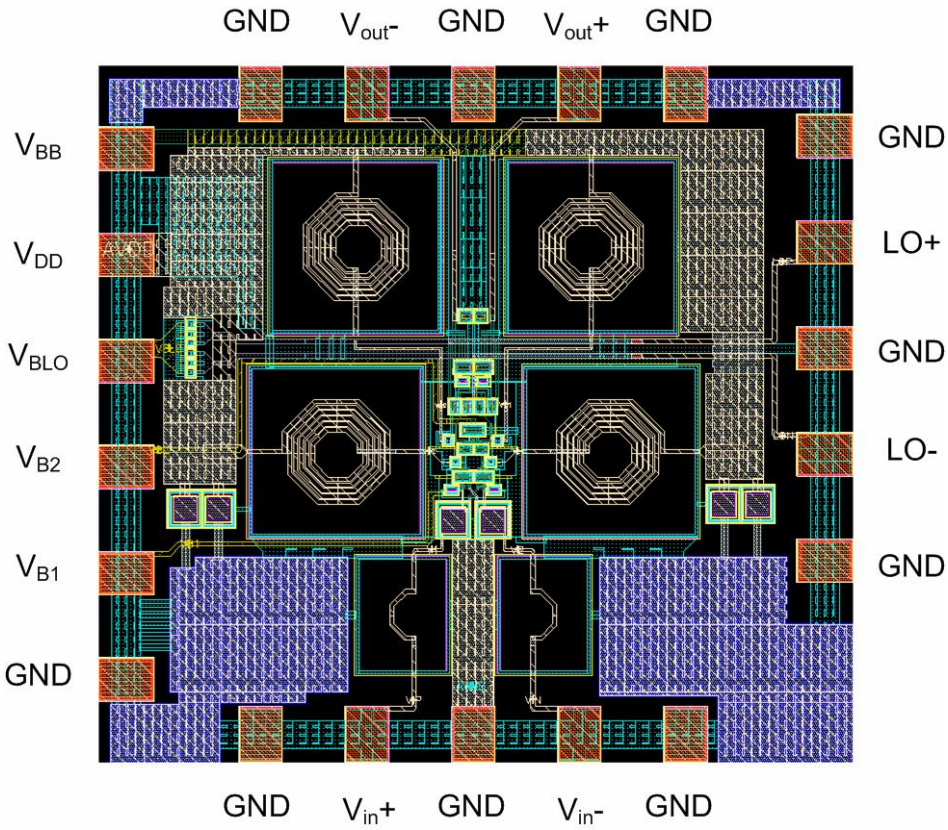


Figure 39 Circuit Layout of the UWB receiver front-end with CCC technique

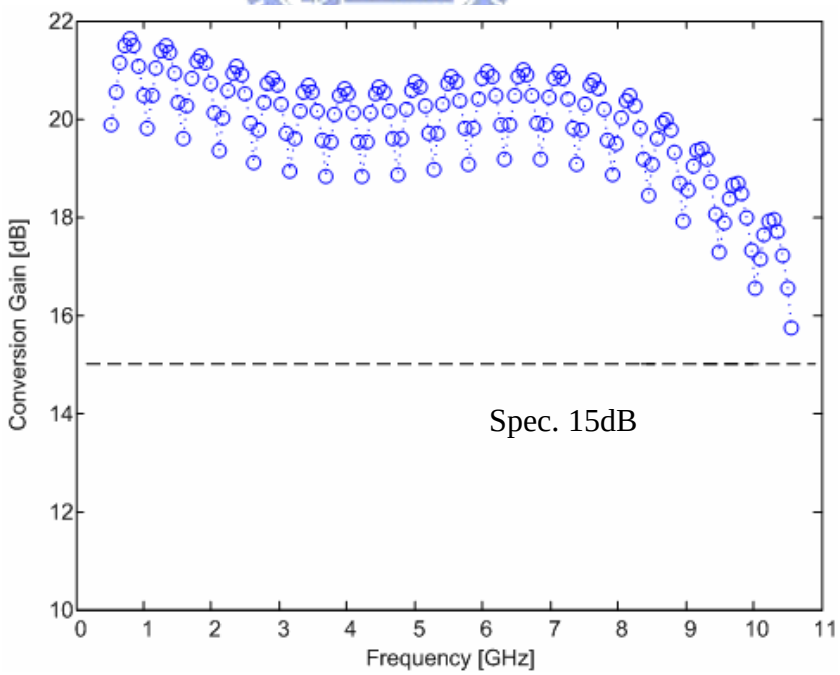


Figure 40 Conversion Gain

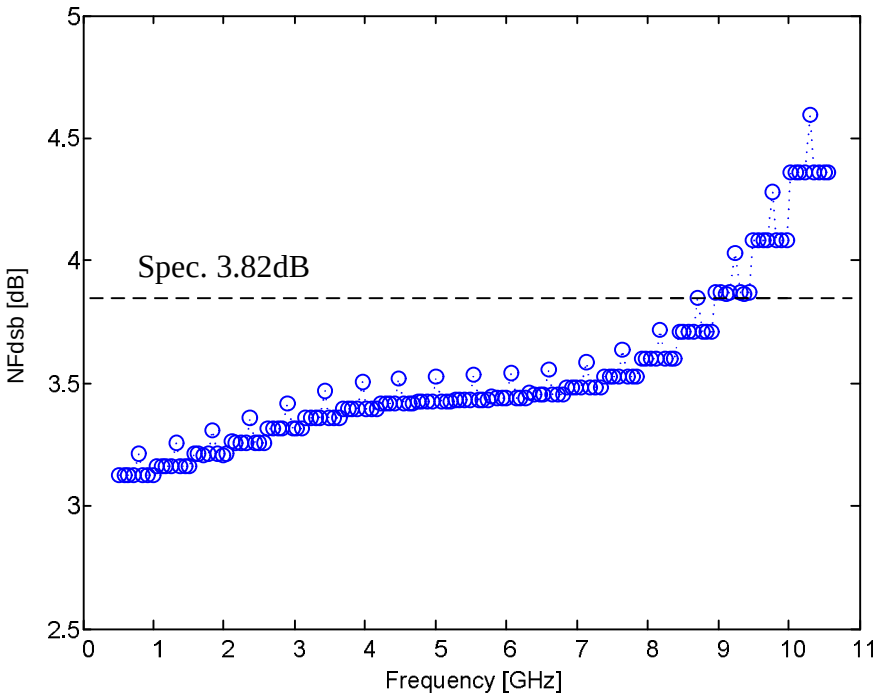


Figure 41　Noise figure

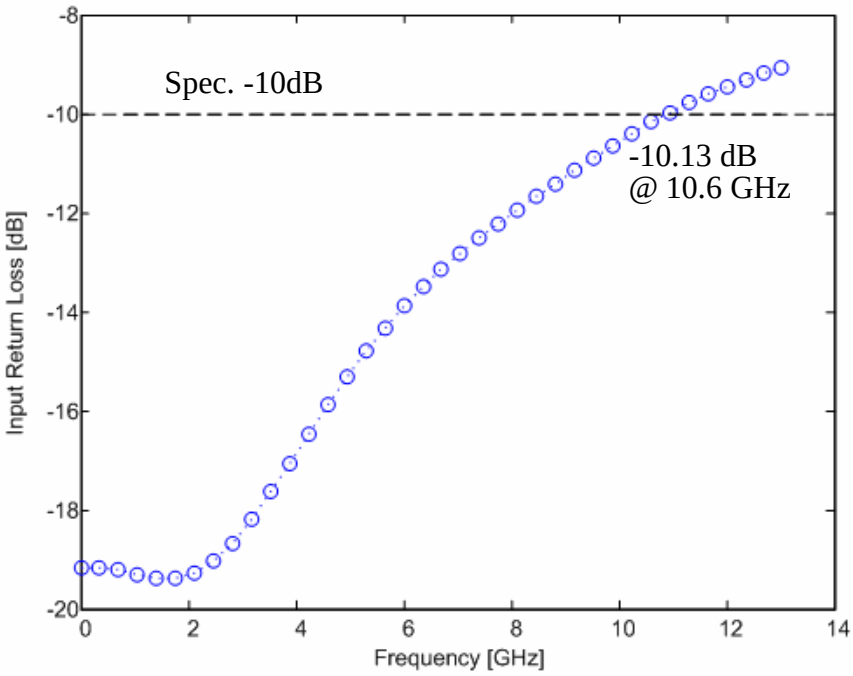


Figure 42　Input return loss

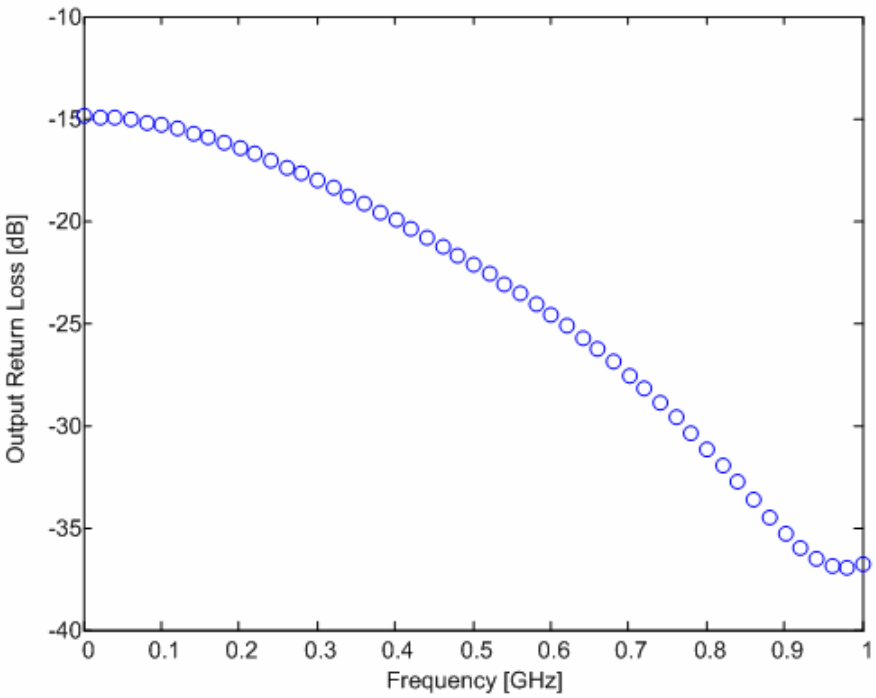


Figure 43　Output return loss

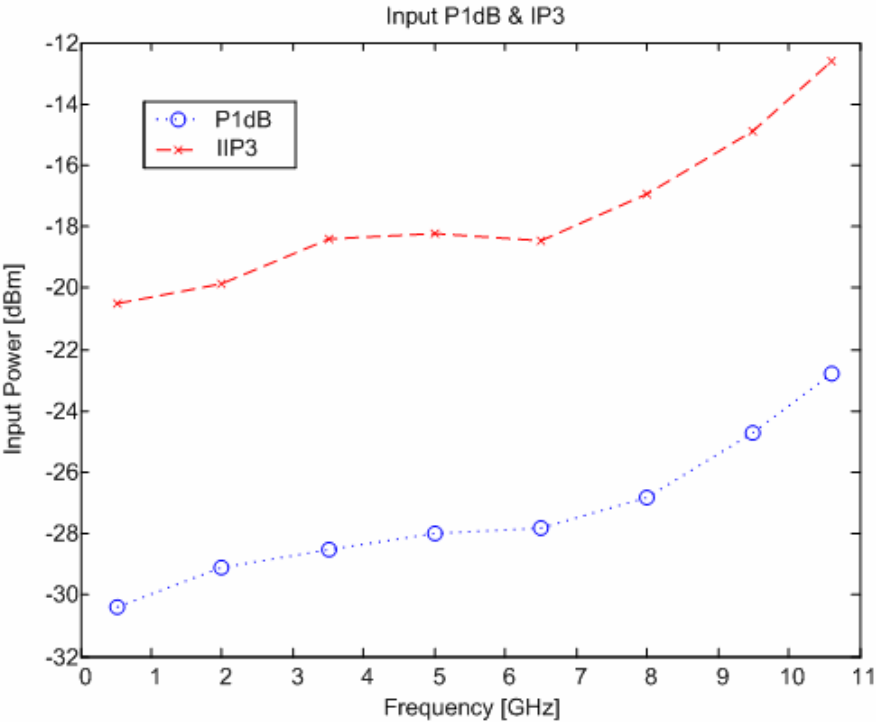


Figure 44　Input IP3 and P1dB

The IIP3 and input P1dB are shown in figure 44. In higher frequency, the circuit has better linearity, because the gain of the first stage of LNA is dropped in high frequency.

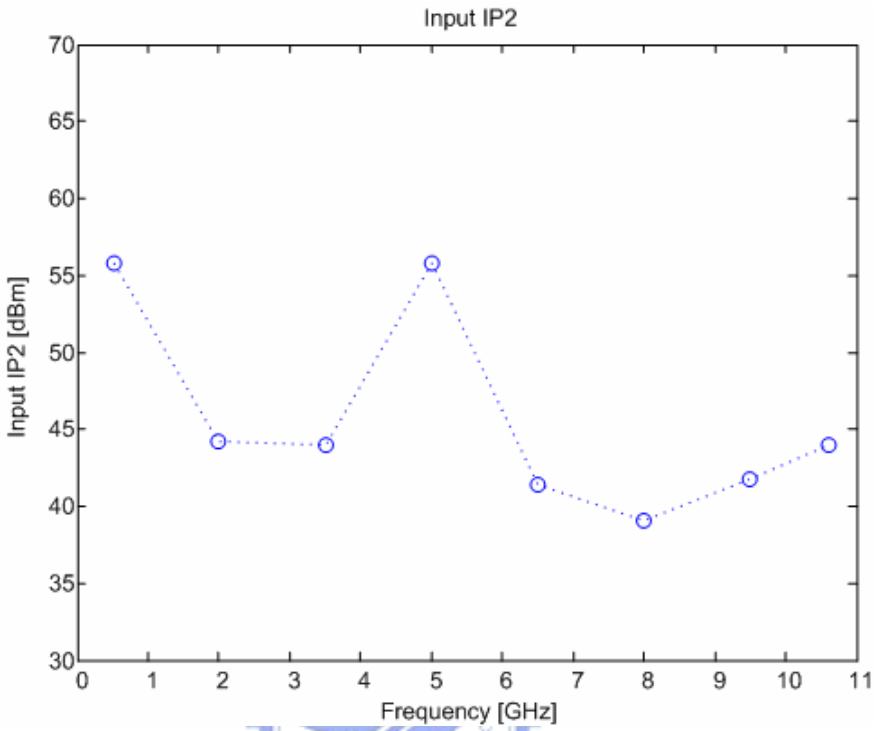


Figure 45 Input IP2

In order to observe the performance of the second order distortion, we assume that there has 1% mismatching in the differential pair of the receiver front-end. And the results is shown in figure 45.

The comparison results are shown in table 6. The proposed receiver front-end with CCC technique has a flat NF from 0.5 GHz to 10.6 GHz while consume power of 11.4 mW in CMOS 0.18 μ m fabrication.

Table 6. Comparison results

Parameters	Spec.	This Work Post-Simulation	RFIC 2005 pp.343 [17]	ISSCC 2006 pp.128 [18]
Technology	--	0.18 um CMOS	0.25 um SiGe BiCMOS	0.18 um CMOS
Power supply	--	1.8 V	2.7 V	2.3 V
Bandwidth	3.1 ~ 10.6 GHz	0.5 ~ 10.6 GHz	3.1 ~ 10.6 GHz	3.1 ~ 8 GHz
Power consumption	--	11.4 mW without buffer	83.7 mW	44.85 mW
Conversion Gain	22	15.8 ~ 21.6 dB	20.6 ~ 21.8 dB	12 ~ 22 dB
IIP3	--	-12.6 ~ -20.5 dBm	IIP3 : -12.7 dBm	@2.6GHz IIP3 : -2.6 dBm
IIP2	--	39.04 ~ 55.82 dBm	29 dBm	33 dBm
S11	< -10	< -10.1 dB	< -10 dB (3.8 ~ 6.6 GHz)	< -5 dB
NF	< 3.9	3.12 ~ 4.6 dB NF_{DSB}	4.1 ~ 6.2 dB NF_{DSB}	5 ~ 6.5 dB
Circuits	LNA + Mixer	LNA + Mixer	LNA + Mixer	LNA + Mixer + Filter
Architecture	--	Homodyne	Homodyne	Heterodyne

4.6 **Measurement Plan**

The receiver front-end is designed for on-wafer measurement. The RF differential input circuit is hard to measure, especially for wideband circuit. A wideband single to differential balun must be used for measurement. Figure 46 shows the measurement environment setting. Except the single to differential balun, the bias tees must be used at input, and the DC blocks are required for the input of LO.

The single to differential balun for RF input and LO input and differential to single transformer for IF output are shown in Figure 47. A broadband balun, Model 5230B, which can operate from 5 kHz to 11 GHz, can be used at the input to provide the differential input signal in this circuit as shown in Figure 47 (a). The rate race coupler is used for single to differential balun of LO input as shown in Figure 47 (b). This technology can be used in narrow band. For UWB receiver front-end, each LO frequency of balun is required. The phase error of this balun can be tuned less than 1°. The ADT4-6WT differential to single transformer can be used in IF output. The receiver front-end can be measured with the proper balun and transformer. The input balun will affect the gain and NF of the receiver front-end. A method can de-embedding the effect of input balun is discussed in [19].

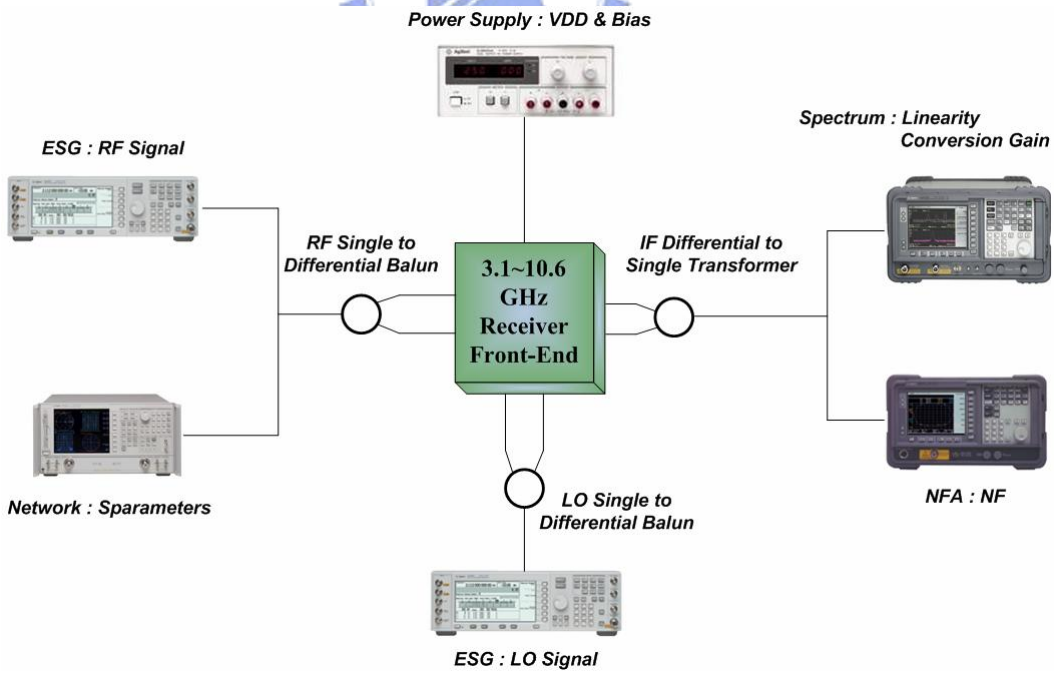


Figure 46 Measurement Environment

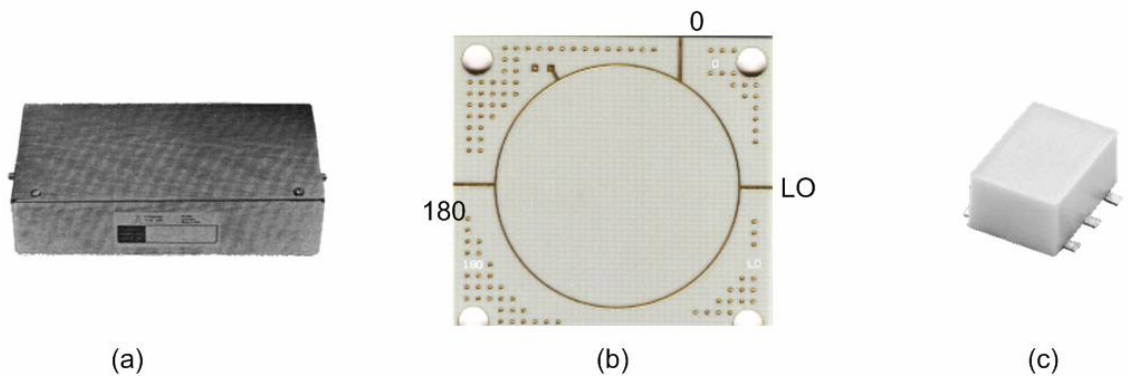


Figure 47 (a) Model 5230B, (b) rate race coupler (c) ADT4-6WT

4.7 **Summary**

The proposed behavior model can be used to assist circuit design. Since the circuit is designed by using the behavior model, the behavior model can be modified by the circuit of transistor level. And it can be used for system verification. A design example of UWB receiver front-end with CCC technology is demonstrated in this chapter by using behavior model.

Chapter 5

Conclusions and Future Work

This thesis presents a design flow with behavior model to design the circuit efficiently. The proposed unified behavior model, which divides a circuit to three parts: input interface, gain stage, and output interface, can be utilized in this design flow. The behavior model can assist the circuit design. A 3.1-10.6 GHz RF front-end for UWB direct conversion receiver with capacitive cross-coupling (CCC) technique is designed by using this behavior model in a 0.18 μm CMOS technology. The receiver front-end performs low power, wide bandwidth and low noise. In conclusion, the key contributions presented in previous chapters are summarized below.

5.1 **Summary**

A unified behavior model combining the RF effects of noise, nonlinearity, frequency response, and input/output impedance is proposed in chapter 2. The system simulation can be performed by this behavior model and reduce the overall simulation time efficiently. In order

to achieve the receiver front-end specification for UWB application, the CCC technique for input matching is utilized in the UWB LNA. The analysis of CCC topology for UWB LNA utilization is discussed in chapter 3. The CCC UWB LNA design by using behavior model is shown in chapter 4. The UWB LNA is used to design the UWB receiver front-end. A wideband passive mixer is designed for the purpose of low power little flicker noise and high linearity after the LNA. The UWB receiver front-end referenced to the overall band groups of the Multi-Band OFDM with operation frequency range 3.1-10.6 GHz provides a maximum voltage conversion gain of 20.9 dB, maximum input IP3 of -14.3 dBm and a minimum NF_{DSB} of 3.4 dB while drawing 11.4 mW from a 1.8-V supply.

5.2 **Recommendations for Future Work**

In this thesis, there are some design considerations which are included. We give some recommendations and improvement in this section. First, the nonlinearity characteristic of the proposed behavior model is performed by Taylor series. This method can express the weak signal condition, only. Other methods of nonlinearity, like volterra series, can be used in this behavior model for strong signal condition. Second, the transfer function can't be used to describe the impedance characteristic in Verilog-A now. If the impedance can be described by equations, the simulation time will reduce greatly. Finally, the characteristics of a mixer are

like to a LNA. A model of wideband mixer can be performed by the proposed behavior model.

Appendix

Analysis of CCC Topology

The voltage gain, input impedance and noise contribution from each component of capacitive cross-coupling are discussed in appendix.

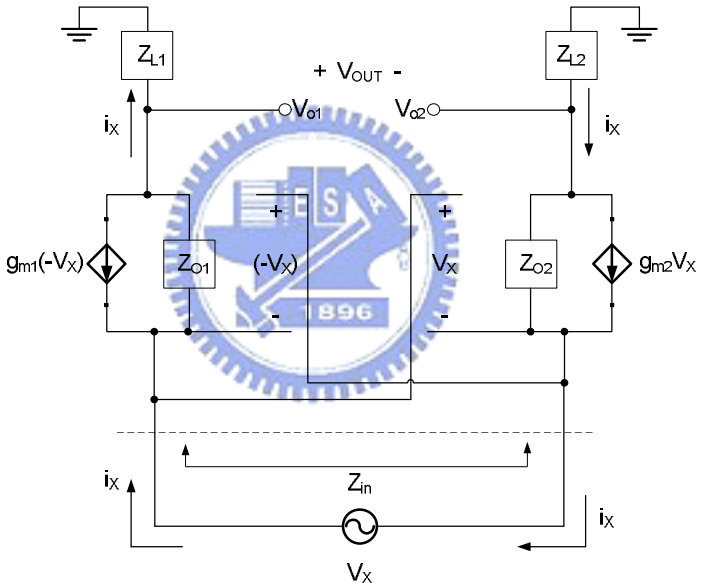


Figure A.1 Small signal circuit for input impedance calculation.

The small signal circuit for input impedance calculation is shown in Figure A.1. Assume $g_{m1} = g_{m2} = g_m$, $Z_{O1} = Z_{O2} = Z_O$, and $Z_{L1} = Z_{L2} = Z_L$:

$$\begin{aligned} V_X &= (i_X - g_m V_X) Z_O + 2 i_X Z_L + (i_X - g_m V_X) Z_O \\ &= 2 i_X Z_O + 2 i_X Z_L - 2 g_m Z_O V_X \end{aligned} \tag{A.1}$$

$$(1 + 2 g_m Z_O) V_X = 2 i_X (Z_O + Z_L) \tag{A.2}$$

$$Z_{in} = \frac{V_X}{i_X} = \frac{2(Z_O + Z_L)}{1 + 2g_m Z_O} \tag{A.3}$$

The input impedance of the CCC topology is shown in (A.3). When we assume Z_O being infinite, the input impedance can be obtained:

$$Z_{in} = \frac{2(Z_O + Z_L)}{1 + 2g_m Z_O} \approx \frac{2Z_O}{2g_m Z_O} = \frac{1}{g_m} \tag{A.4}$$

When we assume Z_O being $Z_O = (1/sC_{ds}) \| r_O = \frac{r_O}{sC_{ds}r_O + 1}$, the input impedance can be obtained:

$$\begin{aligned} Z_{in} &= \frac{2\left(Z_L + \frac{r_O}{sC_{ds}r_O + 1}\right)}{1 + 2g_m \times \frac{r_O}{sC_{ds}r_O + 1}} \\ &= \frac{2 \times \frac{r_O}{sC_{ds}r_O + 1}}{1 + 2g_m \times \frac{r_O}{sC_{ds}r_O + 1}} + \frac{2 \times Z_L}{1 + 2g_m \times \frac{r_O}{sC_{ds}r_O + 1}} \\ &= \frac{2}{sC_{ds} + 2g_m + \frac{1}{r_O}} + \frac{2 \times Z_L \times (sC_{ds}r_O + 1)}{sC_{ds}r_O + 2g_m r_O + 1} \\ &= 2 \times \left[(1/sC_{ds}) + (1/2g_m) + r_O\right] + 2 \times \frac{Z_L}{r_O} \times \frac{sC_{ds}r_O + 1}{sC_{ds} + \left(2g_m + \frac{1}{r_O}\right)} \end{aligned} \tag{A.5}$$

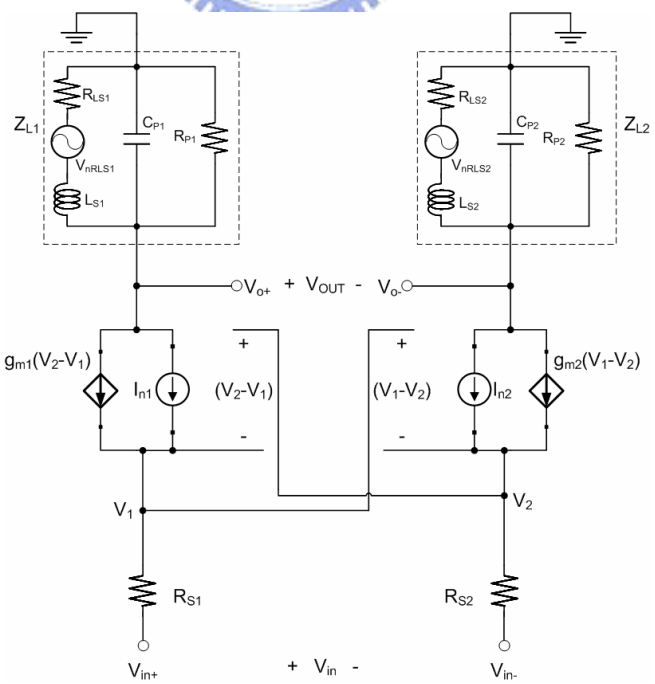


Figure A.2 Small signal circuit for voltage gain and noise calculation.

The voltage gain and noise contribution of each component can be calculated by Figure A.2, Assume $g_{m1} = g_{m2} = g_m$, $R_{S1} = R_{S2} = R_S$, and $Z_{L1} = Z_{L2} = Z_L$:

Voltage gain:

$$\frac{1}{R_S}V_1 = \frac{1}{R_S}V_{in+} + g_m(V_2 - V_1) \tag{A.6}$$

$$\frac{1}{R_S}V_2 = \frac{1}{R_S}V_{in-} + g_m(V_1 - V_2) \tag{A.7}$$

(A.6) - (A.7):

$$\begin{aligned}\frac{1}{R_S}(V_1 - V_2) &= \frac{1}{R_S}(V_{in+} - V_{in-}) + 2g_m(V_2 - V_1)\\ \frac{1}{R_S}V_{in} &= \left(\frac{1}{R_S} + 2g_m\right)(V_1 - V_2)\end{aligned} \tag{A.8}$$

$$\frac{1}{Z_L}V_{O+} + g_m(V_2 - V_1) = 0 \tag{A.9}$$

$$\frac{1}{Z_L}V_{O-} + g_m(V_1 - V_2) = 0 \tag{A.10}$$

(A.9) - (A.10)

$$\begin{aligned}\frac{1}{Z_L}(V_{O+} - V_{O-}) &= 2g_m(V_1 - V_2)\\ (V_1 - V_2) &= \frac{(V_{O+} - V_{O-})}{2g_m Z_L} = \frac{V_{OUT}}{2g_m Z_L}\end{aligned} \tag{A.11}$$

From (A.8) and (A.11):

$$\begin{aligned}\frac{1}{R_S}V_{in} &= \left(\frac{1}{R_S} + 2g_m\right)\frac{1}{2g_m Z_L}V_{OUT}\\ A_V = \frac{V_{OUT}}{V_{in}} &= \frac{2g_m Z_L}{\frac{1}{R_S} + 2g_m} \times \frac{1}{R_S} = \frac{2g_m Z_L}{1 + 2g_m R_S} = \frac{Z_L}{\frac{1}{2g_m} + R_S}\end{aligned} \tag{A.12}$$

The voltage gain of the CCC stage is shown in (A.12). Noise contribution from R_S can be easily expressed by the voltage gain. In order to calculate the noise factor, we calculate the

noise contribution from I_{n1}, I_{n2} and R_{LS1}, R_{LS2}.

Noise contribution from I_{n1}:

$$\frac{1}{R_S}V_1 = g_m(V_2 - V_1) + I_{n1} \tag{A.13}$$

$$\frac{1}{R_S}V_2 = g_m(V_1 - V_2) \tag{A.14}$$

(A.13) - (A.14)

$$\frac{1}{R_S}(V_1 - V_2) = 2g_m(V_2 - V_1) + I_{n1}$$

$$\left(\frac{1}{R_S} + 2g_m\right)(V_1 - V_2) = I_{n1} \tag{A.15}$$

$$(V_1 - V_2) = \frac{I_{n1}}{\frac{1}{R_S} + 2g_m}$$

$$\frac{1}{Z_L}V_{O+} + g_m(V_2 - V_1) + I_{n1} = 0 \tag{A.16}$$

$$\frac{1}{Z_L}V_{O-} + g_m(V_1 - V_2) = 0 \tag{A.17}$$

(A.16) - (A.17)

$$\frac{1}{Z_L}(V_{O+} - V_{O-}) = 2g_m(V_1 - V_2) - I_{n1} \tag{A.18}$$

From (A.15) and (A.18):

$$\frac{1}{Z_L}V_{OUT} = \frac{2g_m}{\frac{1}{R_S} + 2g_m} \times I_{n1} - I_{n1} = \frac{\frac{1}{R_S}}{\frac{1}{R_S} + 2g_m} \times I_{n1}$$

$$V_{OUT} = \frac{\frac{1}{R_S}}{\frac{1}{R_S} + 2g_m} \times Z_L \times I_{n1} = \frac{\frac{1}{2g_m}}{R_S + \frac{1}{2g_m}} \times Z_L \times I_{n1} \tag{A.19}$$

Equation (A.19) shows the noise contribution from In1. If the noise source I_{n2} is equal to I_{n1}, and the circuit is perfect balance, the noise contribution from I_{n1} and I_{n2} are the same.

Noise contribution from R_{LS1} and R_{LS2}:

Assume $R_{LS1}=R_{LS2}=R_{LS}$, $L_{S1}=L_{S2}=L_S$, $C_{P1}=C_{P2}=C_P$, and $R_{P1}=R_{P2}=R_P$:

$$Z_{L1} = Z_{L2} = Z_L = \frac{(R_{LS} + sL_S) \times \left[(1/sC_P) \| R_P \right]}{(R_{LS} + sL_S) + \left[(1/sC_P) \| R_P \right]} \tag{A.20}$$

$$V_{OUT} = V_{n,RLS1} \times \frac{\left[(1/sC_P) \| R_P \right]}{(R_{LS} + sL_S) + \left[(1/sC_P) \| R_P \right]} = V_{n,RLS1} \times \frac{Z_L}{(R_{LS} + sL_S)} \tag{A.21}$$

If $V_{nRLS2}=V_{nRLS1}$, they have the same noise contribution.

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Publication List

1. C. D. Hung, W. S. Wuen, Mei-Fen Chou, and Kuei-Ann Wen, “A Unified Behavior Model of Low Noise Amplifier for System-Level Simulation”, accepted by European Conference on Wireless Technology (ECWT 2006), Manchester, UK, Sep. 2006.

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論文題目 ： UWB RF Receiver Front-End Design by Using Behavior Model

採用行為模型設計方法之超寬頻射頻前端接收器設計