Design and Implementation for high-throughput Turbo Decoder Chip

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Abstract

In this thesis, two high-throughput decoder designs about turbo code are presented. The first one is a high-throughput Max-Log-MAP decoder. The high throughput is achieved with a radix-4x4 ACS design, resulting in a highly parallel and area-efficient decoder. We further apply the retiming technique to reduce the critical path delay. After chip implementation in 0.13um 1P8M technology, the 1.96mm^2 core area can support the maximum 952MS/s data rate.

Since the turbo decoder is composed by two MAP decoders, a following high-throughput turbo decoder design is presented. The inter-block permutation is introduced to overcome the long block interleaver latency. A butterfly network is proposed to interchange the symbols between each block without complex control logic. The radix-2x2 retimed Max-Log-MAP decoder is used as component decoders. Finally, a turbo decoder implementation in 0.13um 1P8M technology can achieve 1.06 Gb/s throughput with 8 decoding iterations in the 17.81 mm^2 silicon area.