使用諧波抑制技術

之串疊組態 **E** 類放大器設計

學生：游振威　　　　　　　　　　　　　指導教授：溫瓌岸 博士

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國立交通大學電子工程學系 電子研究所碩士班

摘　　要

　　為了得到可提供高輸出功率與高功率增加效率(PAE)且不需耗費大面積的功率放大器，非線性的 E 類放大器是個最佳選擇。串疊組態的 E 類放大器架構可提供比差模架構、共閘架構以及傳統的共源架構更高的功率增加效率(PAE)。儘管 E 類放大器擁有高功率增加效率(PAE)的優點，較差的諧波壓抑將可能使得系統因為諧波過高而無法符合所定義之傳輸規格。為了解決非線性放大器此一缺點，我們在此加入諧波抑制技術，並在少量增加負載電路的條件下比傳統的共源架構更有效的降低二階與三階諧波的發生。經由 0.13-μm CMOS 製程進行電路製作後，其模擬結果顯示在頻率範圍 2.39 - 2.69 GHz 此 E 類放大器提供高於 49％的功率增加效率(PAE)，同時最高可提供 24.66dBm 最大輸出功率以及 63.4％最大功率增加效率(PAE)；加入諧波抑制技術後，二階與三階諧波分別為 75.8dBc 與 **59**dBc。此外，此論文提出一個大訊號的射頻電路行為模型。此行為模型能夠有效將耗時的大訊號 **S** 參數的模擬時間減少為 **1/23,640**，並且輸入與輸出阻抗的變異

數分別為（**1.097**$-j$ **1.297**）與（**10.469**$-j$ **22.371**）。

Design of Cascode Class E Power Amplifier

with Harmonic Suppression Technique

Student：Chen-Wei Yu   Advisor：Dr. Kuei-Ann Wen

Co-Advisor：Dr. Wen-Shen Wuen

Department of Electronics Engineering

Institute of Electronics

National Chiao-Tung University

ABSTRACT

In order to obtain moderate chip area, high output power, and high power efficiency simultaneously, nonlinear Class-E power amplifier should be the best choice. Cascode Class-E PA provides better power-added efficiency (PAE) than any other topologies such as differential, common-gate, or common-source. Although Class-E power amplifiers have high power-added efficiency (PAE), poor harmonic suppression would make the whole communication system with nonlinear power amplifier be out of transmission specification.

To conquer the drawback of nonlinear power amplifier, the harmonic suppression technique has been employed. Without greatly increasing the elements of loading network, the 2nd and 3rd order harmonics have been more effectively suppressed than those of conventional loading network. A chip implemented in 0.13-μm shows a 2.39-2.69 GHz bandwidth with PAE higher than 49%. The implemented Class-E PA provides a 24.66 dBm maximum output power and 64% maximum PAE. With harmonic suppression technique, are 75.8dBc and 59dBc of the 2nd and 3rd harmonics suppression are simulated respectively. Moreover, a large signal and power-related behavioral model is presented in this thesis. With this behavioral model, the simulation time of large-signal S-parameter of the implemented circuit can be reduced to about 1/23,640 and variances of input and output impedance are (1.097–j 1.297) and (10.469–j 22.371), respectively.