Contents

摘要	i
Abstract	ii
致謝	v
Contents	vi
List of Figures	ix
List of Tables	xii
Chapter 1 Introduction	1
1.1 Motivation	
1.2 Specifications	4
1.2.1 IEEE 802.16e 2005	4
1.2.2 Architecture	8
1.3 Organization	10
Chapter 2 Circuit Topology	11
2.1 Cascode Class-E PA Topology	11
2.1.1 Voltage Stress of A Common-Source Class-E PA	13
2.1.2 Voltage Stress of A Common-Gource Class-E PA	13
2.1.3 Voltage Stress of A Cascode Class-E PA	15

2.2 Loading Network And Harmonic Suppression Technique	16
2.2.1 Loading Network with Infinite RF-Choke	17
2.2.2 Loading Network with Finite RF-Choke	18
2.2.3 Class-E Power Amplifier with A Finite Number of Harmonics [19]	19
2.2.4 Loading Network with Second Harmonic Suppression Technique [20]	22
2.2.5 Loading Network with Second and Third Order Harmonics Suppre	ession
Technique	23
2.3 Design Considerations	26
2.4 The Analysis of Dissipative Mechanisms	31
2.4.1 Dissipative Mechanism Due To The Implemented Switch	33
2.4.2 Dissipative Mechanism Due To The Resistive Loss of L_b	35
2.4.3 Dissipative Mechanism Due To The Resonant Tank of L_1 and C_1	35
2.4.4 Drain Efficiency	36
Chapter 3 Circuit Simulation And Implementation	38
3.1 Layout Considerations.	38
3.2 Printed Circuit Board (PCB) Design	39
3.3 Simulation Results	41
3.4 Comparison	46
3.5 Measurement Plan	48
Chapter 4 Power-Related Behavior Model	50
4.1 Modeling of Input Matching Network	50
4.2 Modeling of Output Matching Network	57
4.3 Behavioral Model of The Implemented Cascode Class-E PA	62
Chapter 5 Conclusions And Future Work	64

5.1 Summary	
5.2 Future Work	
Bibliography	67
Vita	71



List of Figures

Figure 1	The frequency band of USA application	6
Figure 2	Polar-loop transmitter for WiMAX TX application.	8
Figure 3	(a) Common-source. (b) Common-gate. (c) Combination of common-sour	·ce
	and common-gate into a cascode in order not to provide low impedance los	ad
	to the driving stage.	12
Figure 4	The schematic of conventional loading network with infinite RF-choke.	18
Figure 5	Class-E power amplifier with various number of harmonics [19]	20
Figure 6	Loading network with second harmonic suppression technique	23
Figure 7	A loading network with 2 nd and 3 rd order harmonics suppression technique	24
Figure 8	The Schematic of the implemented cascode Class-E power amplifier	27
Figure 9	Quality factor (Q) of passive component provided by muRata.	30
Figure 10	Input impedance of gate in smith chart.	31
Figure 11	The presented cascode Class-E power amplifier with second and third ord	ler
	harmonics suppression technique.	32

Figure 12 The cascode can be modeled as a shunt capacitor at both gate and drain, a

	turn-on resistance, and an ideal ON/OFF switch	34
Figure 13	The layout of the implemented cascode Class-E power amplifier.	39
Figure 14	Layer stack-up of PCB board.	40
Figure 15	PCB with Chabyshev filter input matching.	41
Figure 16	PCB without passive input matching.	41
Figure 17	Schematic on RFDE.	42
Figure 18	Gate-to-drain voltage of common-gate stage.	43
Figure 19	PAE vs. frequency	43
Figure 20	Output power vs. frequency.	43
Figure 21	Second and third order harmonics suppression.	44
Figure 22	Schematic of common-source Class-E PA.	44
Figure 23	The PAE result of Common-source Class-E PA.	45
Figure 24	The output power result of Common-source Class-E PA.	45
Figure 25	The gate-to-drain voltage stress of Common-source Class-E PA.	46
Figure 26	Measure the S2P files of the input and output probes with the thro	ugh
	calibration kit.	48
Figure 27	Measurement setup.	49
Figure 28	The schematic of the implemented circuit package version.	51
Figure 29	The schematic of input matching network.	52

- Figure 31 The cursory behavioral model of the input matching network. 53
- Figure 32 The comparison of S parameter between the transistor level and proposed behavioral model. (a) S parameter comparison in decibel (dB); (b) S parameter comparison in phase (degree). 54
- Figure 33 The comparison of input impedance between the transistor level and the proposed behavioral model. (a) The input impedance comparison in real part;
 (b) The input impedance comparison in image part. 54
- Figure 34 The real part of impedance comparison with input power ranging from 8dBm to 13dBm. 56
- Figure 35 The image part of impedance comparison with input power ranging from 8dBm to 13dBm. 56
- Figure 36 The schematic of output impedance matching network. 58
- Figure 37 The simplified behavioral model of output impedance matching network. 59
- Figure 38 The comparison of S parameter between the transistor level and proposed behavioral model.(a) S parameter comparison in decibel (dB); (b) S parameter comparison in phase (degree). 60
- Figure 39 The real part of output impedance comparison with input power ranging from 8dBm to 13dBm. 61

Figure 40 The image part of output impedance comparison with input power ranging

61

from 8dBm to 13dBm.



List of Tables

Table 1.	PHY channel spacing.	6
Table 2.	Power classes profiles of OFDM.	7
Table 3.	Power classes profiles of OFDMA.	7
Table 4.	Maximum V_{GS} and V_{GD} stress for each case and assuming the input	t signal V _{in}
	ranging from $-V_{\text{DD}}$ to V_{DD} and gate biased at threshold voltage w	ithout any
	designation.	12
Table 5.	Maximum achievable efficiencies with the use of all harmonics	through a
	highest given order	21
Table 6.	Comparison table of CMOS Class-E PAs	47
Table 7.	Comparison table of harmonics suppression.	47
Table 8.	Variances of input impedance between the simplified model and	transistor
	level.	57
Table 9.	Variances of output impedance between the simplified model and	transistor
	level.	62