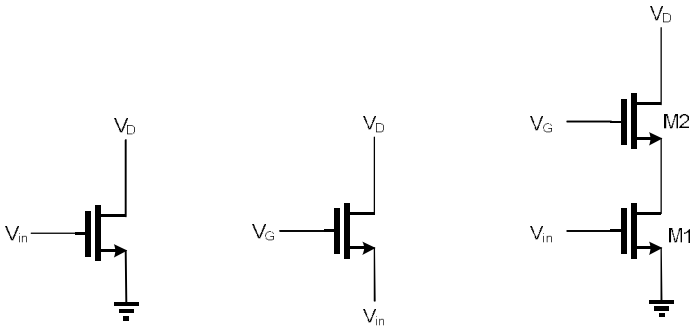
Chapter 2

Circuit Topology

In this chapter, the benefit of cascode Class-E power amplifier is presented in section 2.1. According to [19] of Frederick H. Raab on 2001, the loading network of a Class-E PA has great influence on power efficiency. The published loading networks will be introduced in section 2.2, and the harmonic suppression technique would be also discussed in detail. Section 2.3 discusses the design considerations when implementing a cascode Class-E PA with harmonic suppression. In the last section, the dissipative mechanisms of the proposed Class-E PA are discussed in detail.

2.1 Cascode Class-E PA Topology

Cascode is popularly used in circuit design because of its higher stability and wider bandwidth than single transistor topology. In Class-E PA design, coscode topology allows higher supply voltage to be used and provides higher efficiency due to higher supply voltage being used.



(a) (b) (c)

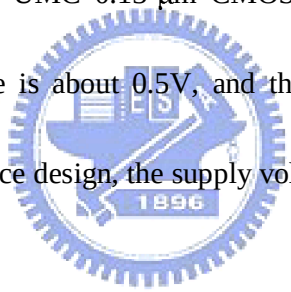
Figure 3 (a) Common-source. (b) Common-gate. (c) Combination of common-source and common-gate into a cascode in order not to provide low impedance load to the driving stage.

		(a)	(b)	(c)
ON	$V_{GS,max}$	$V_{DD} + V_T$	$V_G + V_{DD}$	M2: V_G
				M1: $V_{DD} + V_T$
	$V_{GD,max}$	$V_{DD} + V_T$	$V_G + V_{DD}$	M2: V_G
				M1: $V_{DD} + V_T$
OFF	$V_{GS,max}$	$V_{DD} - V_T$	$V_{DD} - V_G$	M2: $V_G - V_T$
				M1: $-V_{DD} + V_T$
	$V_{GD,max}$	$4.56\ V_{DD} - V_T$	$3.56\ V_{DD} - V_G$	M2: $3.56\ V_{DD} - V_G$
				M1: $V_G + V_{DD} - 2V_T$

Table 4. Maximum V_{GS} and V_{GD} stress for each case and assuming the input signal V_{in} ranging from $-V_{DD}$ to V_{DD} and gate biased at threshold voltage without any designation.

2.1.1 Voltage Stress of A Common-Source Class-E PA

In common-source Class-E PA topology, the transistor is switched from the gate of as shown in Figure 3(a). The maximum achievable voltage of drain on the transistor is $V_{D,max}$, which can be as high as 3.56 times of V_{DD} in an ideal Class-E power amplifier [16]. The gate terminal is biased at threshold voltage V_T for 50% duty cycle. Assuming the input signal swinging from $-V_{DD}$ to V_{DD}, the gate-to-drain stress of common-source is as large as (4.56 V_{DD} - V_T). It results in low supply voltage and in turn low load resistance for the same output power and poor efficiency. In UMC 0.13-μm CMOS process, the width of I/O device is 0.34-μm, the threshold voltage is about 0.5V, and the gate-to-drain breakdown voltage is typical 8.5V. For common-source design, the supply voltage must be less than 1.97V.



2.1.2 Voltage Stress of A Common-Gate Class-E PA

If the power device is switched from the source instead of the gate terminal, which is shown in Figure 3(b), the maximum voltage stress can be reduced to (3.56 V_{DD} - V_G) which is depending on the selection of V_G, so that the supply voltage can be substantially increased for higher power efficiency in common-gate Class-E PA.

As for common-gate design, the supply voltage is related to the value of V_G. In order to sustain higher voltage stress, we can set V_{GD_ON}=V_{GD_OFF} as shown in equation (2.1) and (2.2)

to find out the optimum V_G bias voltage in equation (2.3). In 0.34-μm I/O device technology, the gate-to-drain breakdown voltage is 8.5V so that the supply voltage should be less than 3.73V by equation (2.4) and (2.5).

$$V_{GD\_ON} = V_{GD\_OFF} \tag{2.1}$$

$$3.56V_{DD} - V_G = V_{DD} + V_G \tag{2.2}$$

$$V_G = 1.28V_{DD} \tag{2.3}$$

$$V_{GD\_ON} = V_{GD\_OFF} = 2.28V_{DD} \le 8.5 \tag{2.4}$$

$$V_{DD} \le 3.73V \tag{2.5}$$

Therefore, the supply voltage of common-gate topology is 1.68 times larger than that of common-source. Besides, the voltage headroom reduction due to turn-on resistance of the transistor can be compensated by the amplitude of input signal as shown in equation (2.6).

$$V_{eff} = V_{DD} - V_{R_{on}} + V_{signal} \tag{2.6}$$

In order not to present low impedance node to the driving stage, another common-source stage is needed to combine with common-gate switch into a cascode topology. The comparison of the stress of V_{GS} and V_{GD} is shown in Table 4.

2.1.3 Voltage Stress of A Cascode Class-E PA

During the ON state, the maximum voltage occurred at the gate of M1 in Figure is V_{DD} + V_T because the highest input signal is V_{DD} and the gate is biased at V_T for 50% duty cycle. Assuming the turn-on resistance of transistor is zero, the both drain terminals of M1 and M2 are dropped to zero so that the V_{GS} and V_{GD} of M1 are both V_{DD} + V_T; while the gate-to-source and gate-to-drain voltages of M2 are equal to V_G. During the OFF state, the voltage of M2's drain is as high as 3.56 V_{DD} and the gate-to-drain stress is increased to 3.56 V_{DD} – V_G. Besides, M1 should not draw current during OFF state, but M2 is still on, so that the gate-to-source voltage of M2 is biased at the threshold V_T. After a simple calculation, we can get that the gate-to drain voltage and gate-to-source voltages of M1 are V_G + V_{DD} - 2V_T and V_{DD} + V_T, respectively with the initial assumption that the input signal swings from –V_{DD} to V_{DD}.

Optimizing the cascode Class-E power amplifier, from the point of view of reliability, proper gate bias of common-gate M2 is required to minimize both the gate-to-drain voltages of M1 and M2. In order to share the stress between M1 and M2 for the best performance, we set the gate-to-drain voltage of M1 equal to that of M2, and the optimum is achieved with $V_G = 1.28V_{DD} + V_T$, leading to a maximum gate-to-drain stress $2.28V_{DD} - V_T$ for both M1 and M2 [17]. For the 0.34-μm I/O device in UMC 0.13-μm CMOS process, the

gate-to-drain breakdown voltage is typical 8.5-V and the threshold voltage is 0.5-V, so that the supply voltage can be chosen as high as 3.95-V. Comparing with the 1.97-V supply voltage of common-source, the supply voltage can be increased almost 2 times with cascode topology.

2.2 Loading Network And Harmonic Suppression Technique

The loading network is used to provide proper termination for Class-E power amplifier. The infinite inductor for RF choke was hypothesized in the first publication of Sokal. In practice, infinite inductor is hard to achieve and area consuming, so that finite inductor for RF choke has been widely discussed. After lots of theoretical analysis, it was found that with proper inductance of RF choke, the capacitance of drain can be about 60% higher then that with infinite one, and the peak drain voltage can be 2.5 times of supply voltage comparing to 3.56 times with infinite one.

According to [19] of Frederick H. Raab on 2001, the maximum achievable power efficiency depends on the number of harmonic occurred on the drain. The maximum achievable efficiencies for incremental inclusive harmonics, from the first order through the fifth order, are 50%, 70.71%, 81.65%, 86.56%, and 90.45%, respectively [19]. Loading

network with proper harmonic termination began to be highlighted. These values show that the proper second harmonic termination has the most influence on the enhancement of power efficiency, so that loading network with second harmonic termination has been published [20]. With correct harmonic termination, it results not only higher maximum achievable power efficiency, but harmonic suppression is the additional benefit. In communication system, the second and third order harmonic suppression would be a critical issue. In [21], a loading network with proper second and third order termination has been discussed, which provides benefits of harmonic suppression of second and third order at the same time.

2.2.1 Loading Network with Infinite RF-Choke

The conventional loading network with theoretical assumption of infinite RF-choke is shown in Figure 4 and has been first published by N. O. Sokal in 1975. Infinite RF-choke is used to ensure that the RF signal would not leak to power supply and then cause power loss. In optimum Class-E amplifier operation, C_{shunt}, L, and R are in critical dumping condition which makes the voltage of drain drop to zero immediately when the switch is turned on. The peak voltage would be occurred on drain during the OFF state. As a theoretical analysis in [4], the peak voltage of drain can be 3.56 times of V_{DD}. A device with high gate-to-drain breakdown voltage is necessary to sustain such high voltage for a Class-E power amplifier

design.

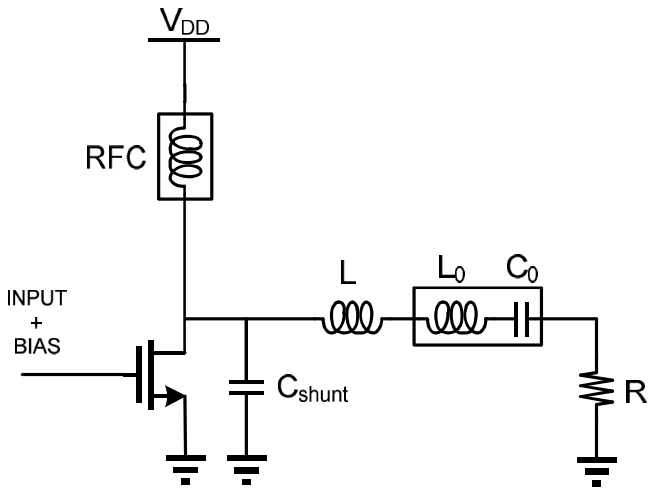


Figure 4 The schematic of conventional loading network with infinite RF-choke.

2.2.2 Loading Network with Finite RF-Choke

In practice, infinite inductance is hard to achieve and less integration for communication system. There were many publications discussing about the influence of finite inductor for RF choke. As demonstrated in [15], with proper value of inductance, the capacitance of drain can be 60% larger than that with infinite inductance for RF choke. If all the shunt capacitance is determined by the parasitic of the active device, it allows larger size and lower turn-on resistance. Therefore, the power efficiency of this amplifier should be improved. The peak voltage stress can be a low as 2.5 times of VDD and the stress of active device can be alleviated.

2.2.3 Class-E Power Amplifier with A Finite Number of Harmonics [19]

According to [19] of F. H. Raab in 2001, providing proper harmonic termination at drain makes the maximum achievable power efficiency higher. The voltage shape of drain can be fixed toward that of ideal Class-E power amplifier. The voltage and current waveforms of a Class-E power amplifier included the number of harmonics are shown in Figure 5. A number of *n* means that all harmonics through *n* are used to fixed the voltage and current waveforms at drain. For $n = 1$, there is no harmonic but fundamental term and the amplifier acts as a Class-A power amplifier. For $n = 3$, both the voltage and current are much similar to those of ideal Class-E PA. With additional harmonics, the waveforms of voltage and current are still shaped toward those of an ideal Class-E amplifier. Switch PA has high power efficiency because the waveforms of voltage and current overlap in a short period. As we can see in Figure 15, with more harmonics used in drain, the achievable power efficiency would be higher without doubt. The table of maximum achievable efficiency versus the number of harmonics is shown in Table 5. In order to design a high efficiency Class-E PA, proper second and third harmonics termination would have the greatest impact on the enhancement of efficiency.

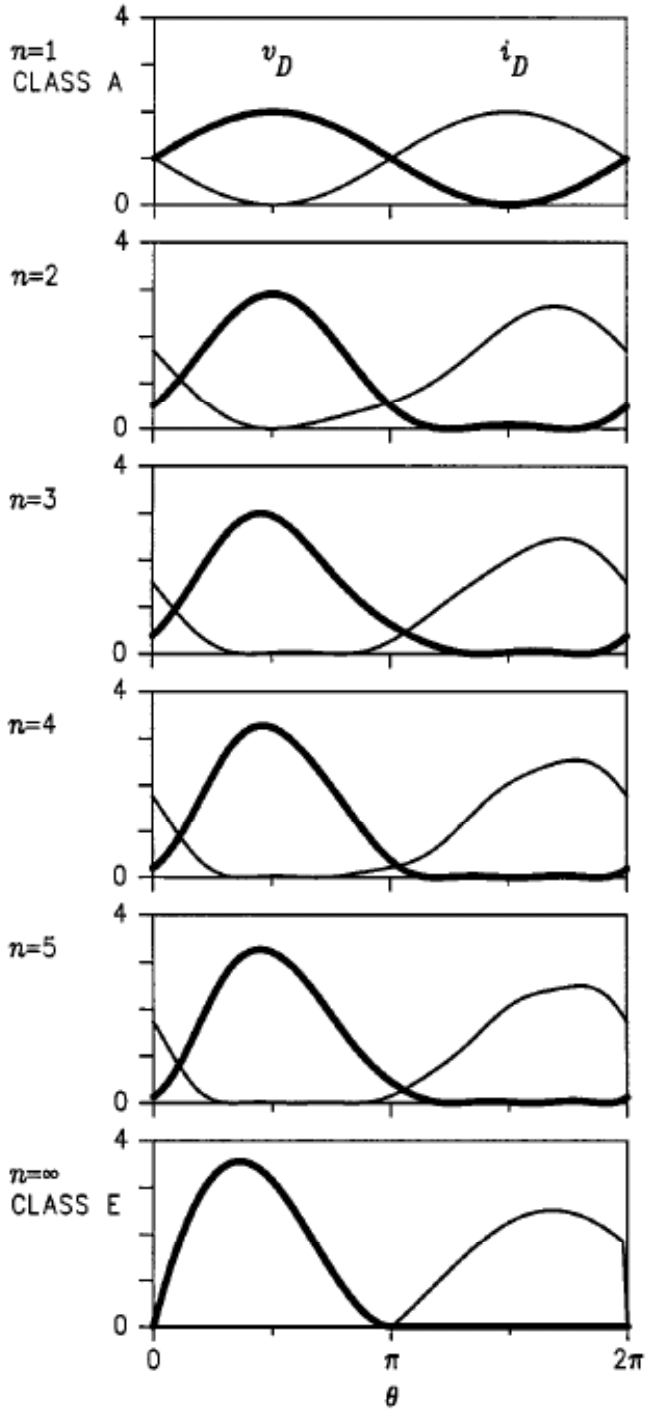


Figure 5 Class-E power amplifier with various number of harmonics [19]

N (number of harmonics)	η (maximum achievable efficiency)
1	50%
2	70.71%
3	81.65%
4	86.56%
5	90.45%
∞	100%

Table 5. Maximum achievable efficiencies with the use of all harmonics through a highest given order

In the optimum Class-E operation, lower order of harmonic term should be terminated with higher harmonic reactance. However, in conventional loading network, the serial resonant tank provides the lowest reactance to the second harmonic term, which is the most significant harmonic term in efficiency enhancement, and allows unwanted second harmonic leaking to the load. It means, with proper resonating tank design, the efficiency should result in a joyful increment.

2.2.4 Loading Network with Second Harmonic Suppression Technique [20]

In order to alleviate the drawback of serial resonating tank providing lowest second harmonic reactance, parallel resonating tank is applied. With setting the resonant frequency at two times of operation frequency as shown in Figure 6, the second harmonic is definitely terminated with the highest reactance. Moreover, the behavior of a parallel resonant tank at the frequency lower than resonant frequency is acted as an inductor which is larger than that of the parallel resonant tank. In other words, parallel resonant tank allows smaller inductance than that actual required. In practice, larger inductors have larger resistive loss and lower self-resonant frequency. The capability of allowing smaller inductors permits the power efficiency higher and higher operation frequency. Besides, it is much expensive for an off-chip inductor with higher self-resonant frequency and lower resistive loss and less area-consuming for an on-chip inductor. The employment of parallel tank makes the whole design cheaper.

According to the theory of [19], the maximum achievable efficiency should be as high as 70.71%. This proposed Class-E PA was implemented in conventional BiCMOS process for operation at 5-6 GHz. This PA shows an output power 19.7 dBm and power-added efficiency greater than 43.6% with 3-V supply voltage.

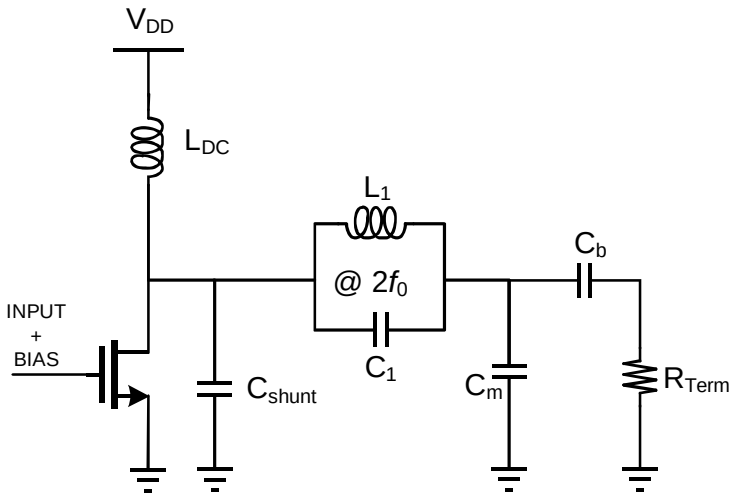


Figure 6 Loading network with second harmonic suppression technique

2.2.5 Loading Network with Second and Third Order Harmonics Suppression Technique

In [21], a loading network with second and third order harmonics suppression technique is shown in Figure 7. Instead of an inductor for RF choke, quarter-wavelength transmission line is applied. At the operation frequency, the quarter-wavelength transmission line behaves as an open circuit and the fundamental signal would not leak to power supply through the quarter-wavelength transmission line. While at the two times of operation frequency, the transmission line acts as a short circuit and passes the current of the second harmonic term to power supply and remains the voltage of second harmonic on drain to shape the voltage waveform of drain. Moreover, because the current of the second harmonic is shorted to ac

ground by the characteristic of quarter-wavelength transmission line, the unwanted second harmonic at the load is suppressed. After simulation, the second harmonic suppression has excellent performance by employing the quarter-wavelength transmission line as an RF choke.

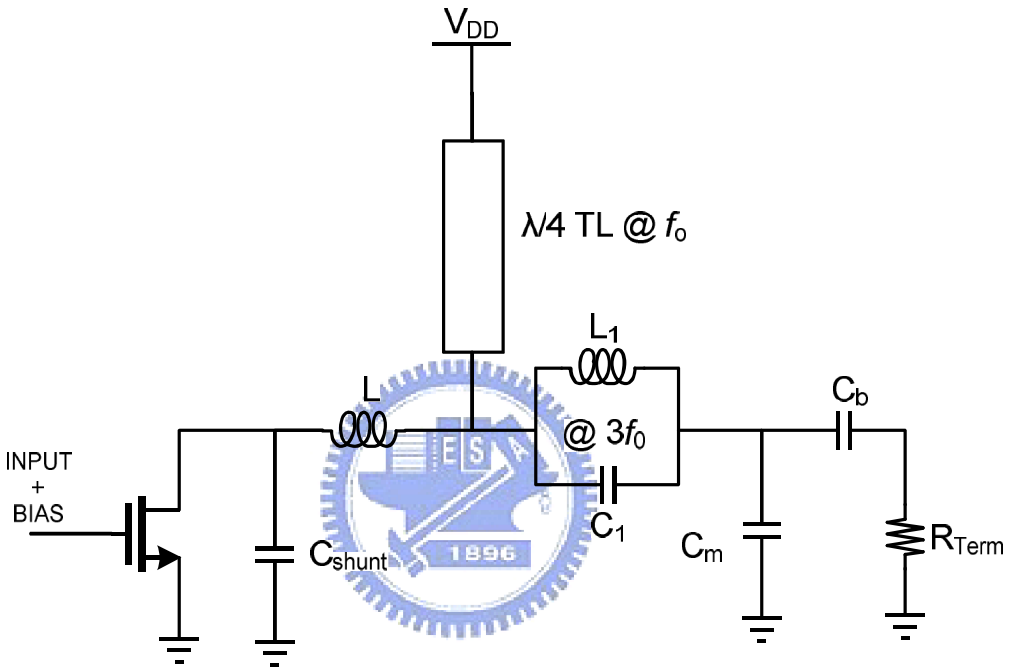


Figure 7 A loading network with 2nd and 3rd order harmonics suppression technique

There are some differences between the harmonic suppression loading network and the conventional one. First, the inductor between switch and quarter-wavelength transmission line is required, and the C_b before the load can't be ignored. If L is eliminated, the second harmonic term will be shorted to ground at drain. It disobeys the original concept that a shunt capacitor could be seen at drain for all harmonics. However, it can be implemented by a

bondwire of package because the Class-E power amplifiers are always implemented on board to improve its power efficiency. And, with the employment of L, the capacitance seen by second harmonic can be compensated for higher efficiency.

While, C_b is used as a DC block which prevents large DC current from power supply to the load. As for the employment of a serial resonant tank, the capacitor of serial resonant tank blocks the DC current to the load.

The resonant tank composing L_1 and C_1, which is design to resonating at three times of operation frequency, is used to provide proper third harmonic termination. It is the same ideal as before that parallel resonant tank allows smaller inductor with higher self-resonant frequency and lower resistive loss to be used and blocks the unwanted third harmonic, which could make the whole communication system fail to specification, to the load.

In an optimized Class-E power amplifier design, sufficient phase shift of output signal is necessary. In practice, if L in Figure 7 provides insufficient inductance for optimal Class-E operation, the parallel resonant tank can provide the rest part of required phase shift and also forming an impedance transformation with C_m.

2.3 Design Considerations

The schematic of the implemented cascode Class-E power amplifier with second and third order harmonics suppression technique is shown in Figure 8. No matter what kind of topology that the active devices are stacking, active devices are used to be an ON/OFF switch. According to the publication of F. H. Raab in 1977, the actual loading resistance R, required shunt capacitance C_{shunt}, and the required output phase shift for optimum Class-E operation L_b can be calculated by equation (2.7), (2.8), and (2.9) respectively.

$$R = 0.577 \frac{V_{DD}^{\ 2}}{P_{out}} \tag{2.7}$$

$$C_{shunt} = 0.183 \frac{1}{\omega_0 R} \tag{2.8}$$

$$L_b = \left(\frac{\pi^2}{16} - \frac{\pi}{4} \right) \frac{R}{\omega_0} \tag{2.9}$$

For the sake of simplicity, these equations are calculated under an initial assumption that L_b provides sufficiency inductance for the optimized Class-E operation. In practice, L_b is implemented with a bondwire of package and provides a small amount of inductance. The insufficient inductance can be provided by the parallel resonant tank composing of L_1 and C_1.

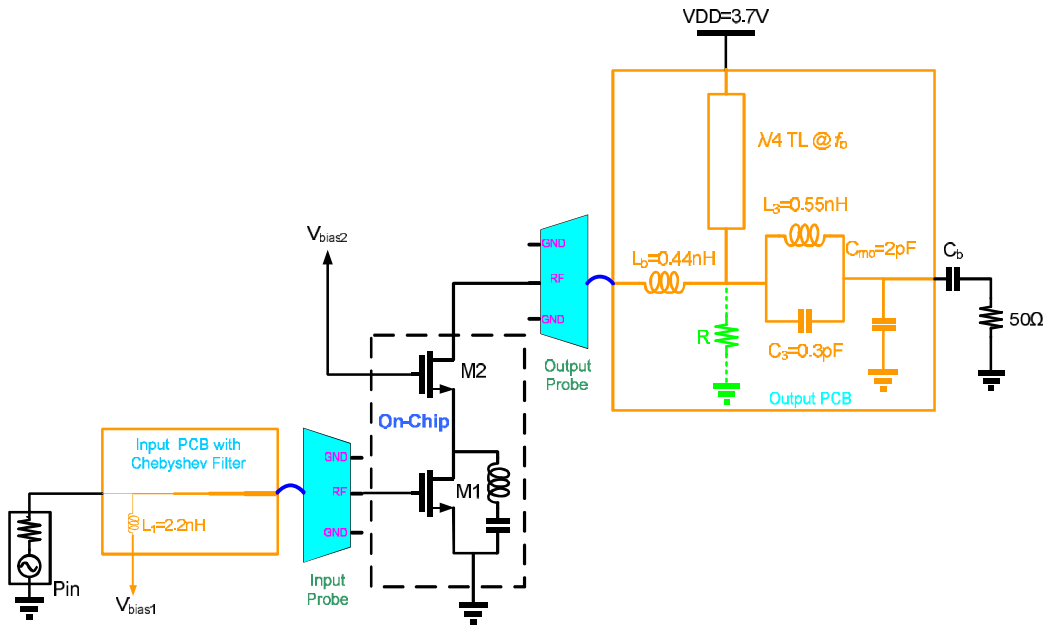


Figure 8 The Schematic of the implemented cascode Class-E power amplifier

The required C_{shunt} can be determined either partially by the parasitic capacitance of the active device and then employing a passive capacitor to lower the nonlinearity of the drain-to-bulk parasitic capacitance, or totally by the parasitic capacitance of the switch. In next section, the composition of the shunt capacitance will be discussed in the view of power efficiency.

As for the loading network, the transmission line is used to be an RF choke and blocks the fundamental signal leaking to the power supply, so that it is implemented with a quarter wavelength of the operation signal. The parallel resonant tank, L_1 and C_1, self resonating at the three times of operation frequency provides larger inductance that that provided by a single L_1. The reactance provided by the parallel resonant tank is calculated in equation (2.10),

(2.11), and (2.12).

$$3\cdot\omega_0 = \frac{1}{\sqrt{L_1 C_1}} \tag{2.10}$$

$$\begin{aligned} Y &= \frac{1}{j\omega L_1} + j\omega C_1 \\ &= j\left(\omega C_1 - \frac{1}{\omega L_1}\right) \\ &= j\left(\frac{\omega^2 L_1 C_1 - 1}{\omega L_1}\right) \end{aligned} \tag{2.11}$$

$$Z = j\left(\frac{\omega L_1}{1-\omega^2 L_1 C_1}\right) = j\left(\frac{\omega L_1}{1-\omega^2 / (3\cdot\omega_0)^2}\right) \tag{2.12}$$

If $\omega < 3\omega_0$, the resonant tank provides inductance; $\omega > 3\omega_0$, capacitance is provided. The inductance that the resonant tank provides at fundamental frequency is shown in equation (2.13).

$$3\cdot\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$$

$$\begin{aligned} Z &= j\left(\frac{\omega_0 L_1}{1-\omega_0^2 / (3\cdot\omega_0)^2}\right) \\ &= j\frac{\omega_0 L_1}{1-1/9} \\ &= j\frac{9}{8}\omega_0 L_1 \end{aligned} \tag{2.13}$$

This mechanism allows the use of a smaller inductance than that required, because smaller inductor has higher self-resonant frequency and lower resistive loss. It further improves the overall power efficiency.

Besides, the parallel resonant tank forms an impedance transformer with C_m from the actual loading R to the terminated loading R_{Term}. Due to the limitation of the supply voltage, in order to provide high output power, it is a trick that a small actual loading resistance is used. But, in the communication system, it is a usual case that the termination resistance of 50 ohm is used.

First of all, if we want to choose the proper values of the impedance transformer, composing of C_m, L_1, and C_1, the Q_{match} of the impedance transformer should be chose at first which is calculated as below:

$$Q_{match} = \sqrt{\frac{R_{Term}}{R} - 1} \tag{2.14}$$

and then the components of C_m, L_1, and C_1 can be expressed as [23]:

$$C_m = \frac{Q_{match}}{\omega_0 R_{Term}}, \quad L_1 = \frac{8}{9}\frac{Q_{match} R}{\omega_0}, \quad C_1 = \frac{1}{9\omega_0^2 L_1} \tag{2.15}$$

where the resonant tank L_1 and C_1 provides 9/8 L_1 at the operation frequency.

The device size of the common-gate stage M2 can be selected as large as the required C_{shunt} for optimized Class-E operation that can be totally provided by the parasitic capacitance on drain. Although the parasitic capacitance of drain is nonlinear, the impact of its nonlinearity on PA performance is weak [33], [34]. Larger device size lower the turn-on resistance and reduce the power loss during the switch is turning on. However, the device size of M2 has a limitation. In optimized Class-E operation, C_{shunt}, L_b, and R should be in the critical dumpling

condition. As long as C_{shunt} is increasing and R is specified, L_b should be smaller according to the critical dumpling condition. The minimum inductance of L_b can be implemented by paralleling five 2.2nH passive components provided by muRata, whose quality factor is higher than 320 from 2 - 3 GHz.

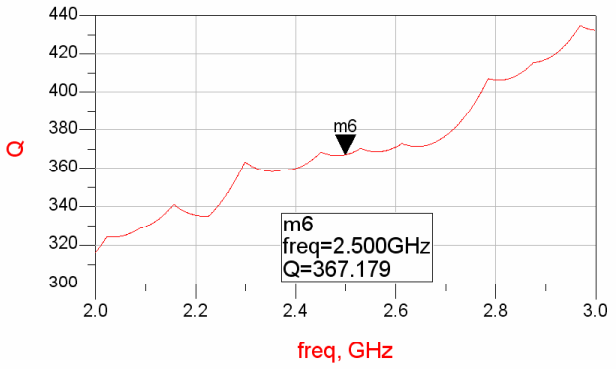


Figure 9 Quality factor (Q) of passive component provided by muRata.

In the point of view of efficiency, the device size of M1 is also as large as possible. But, larger device size results in larger loading effect to the driving stage. As long as larger transistor size is used, the input resistance seen from gate is smaller. Including the parasitic capacitance of gate, the smith chart is shown in Figure 24. Therefore, a parallel inductor is usually required to tune out the parasitic capacitance or to make the impedance line cross the center of the smith chart. In this implemented cascode Class-E PA, a fifth order Chebyshev filter is employed for input matching network and 2.2nH passive component also provided by muRata is used for RF-choke.

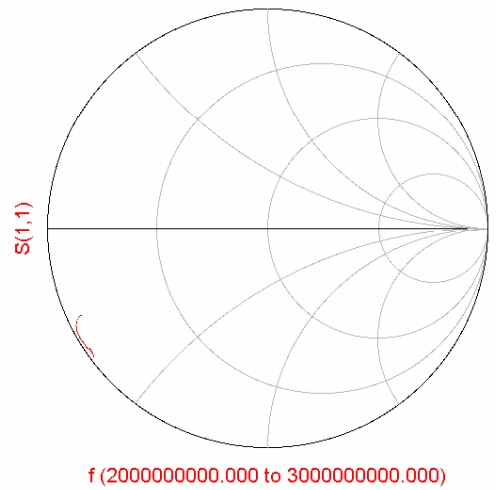


Figure 10 Input impedance of gate in smith chart.

If the size of M1 and M2 are chose as the maximum allowable width, the parasitic capacitance of the interconnection between M1 and M2 is about 2 or 3 times than C_{shunt}. The unwanted parasitic capacitance may cause unwanted charging and discharging. In [24], it has been proposed that the unwanted parasitic capacitance can be tuned out by a parallel inductor, L_r, and the power efficiency can be further improved. Without providing a straight DC path through L_r, a DC-block capacitor is needed.

2.4 The Analysis of Dissipative Mechanisms

The schematic of presented cascode Class-E power amplifier with second and third order harmonics suppression technique is shown in Figure 9. As mentioned before, the L_b is necessary and negligible to keep the Class-E PA operates correctly. In practice, the L_b can be

implemented by a bondwire and the inductance of L_b must be very small. The parallel tank provides extra inductance to ensure optimized Class-E condition, and then forming a matching network from actual load R to termination load R_{term}.

The dissipative mechanisms due to turn-on resistance, parasitic resistance of package bondwire, and resistive loss of parallel resonant tank would be further discussed as follows. And then, the overall efficiency will be calculated.

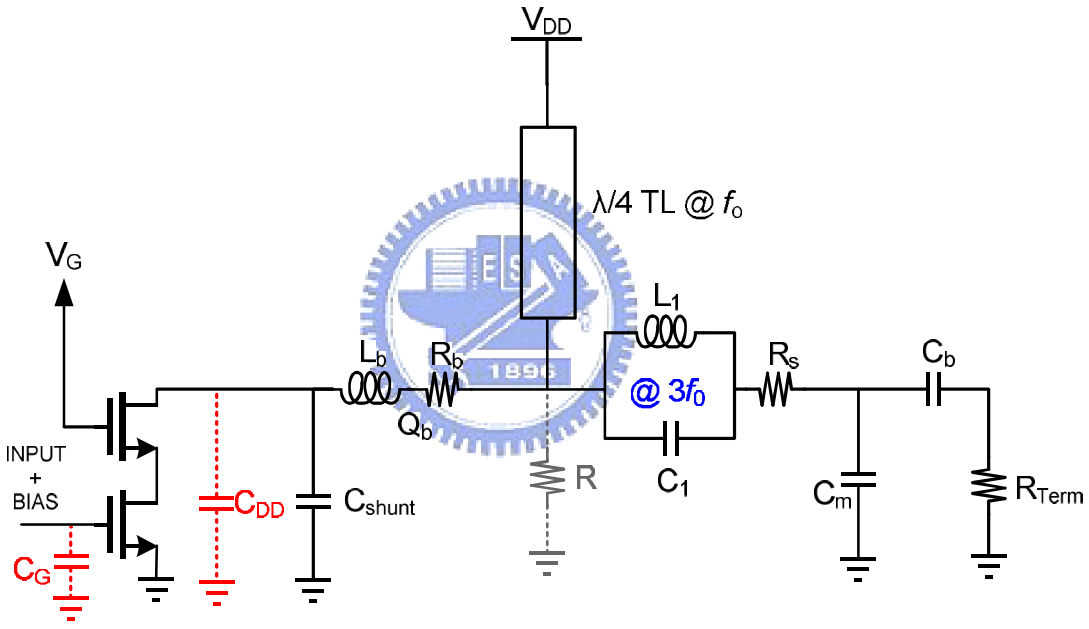


Figure 11 The presented cascode Class-E power amplifier with second and third order harmonics suppression technique.

2.4.1 Dissipative Mechanism Due To The Implemented Switch

The power transistors in Figure 9, behaving as an ON/OFF switch, can be simply modeled as a shunt capacitor to ground at gate and drain, a turn-on resistance, and an ideal ON/OFF switch which are shown in Figure 10. The drain shunt capacitor C_{DD} and turn-on resistance are depended on the size of the transistor, which can be expressed as:

$$\begin{aligned} C_{DD} &= C_{DD\_n} \cdot W \\ R_{on} &= \frac{R_{on\_n}}{W} \end{aligned} \tag{2.16}$$

where C_{DD_n} and R_{on_n} are the drain capacitance and turn-on resistance normalized to the width of the transistor.

The drain capacitance C_{DD}, which is mainly constructed by the reverse bias drain-to-substrate capacitance, varies with the drain voltage. However, the capacitance of C_{shunt} can be implemented by either partially C_{DD} and partially passive capacitor or totally C_{DD}. Let α represent the ratio of C_{DD} to C_{shunt}, and the C_{shunt} and C_{DD} can be represented as:

$$\begin{aligned} C_{shunt} &= \frac{0.183}{\omega_0 R} \\ C_{DD} &= C_{DD\_n} \cdot W = \alpha \cdot \frac{0.183}{\omega_0 R} \end{aligned} \tag{2.17}$$

with $\alpha \leq 1$.

When the switch is turn-on, the power would be dissipated by the turn-on resistance. The

power loss normalized to the output power can be described as [22]

$$\left.\frac{P_{loss}}{P_{out}}\right|_{R_{on}} = 1.365\frac{R_{on}}{R} \tag{2.18}$$

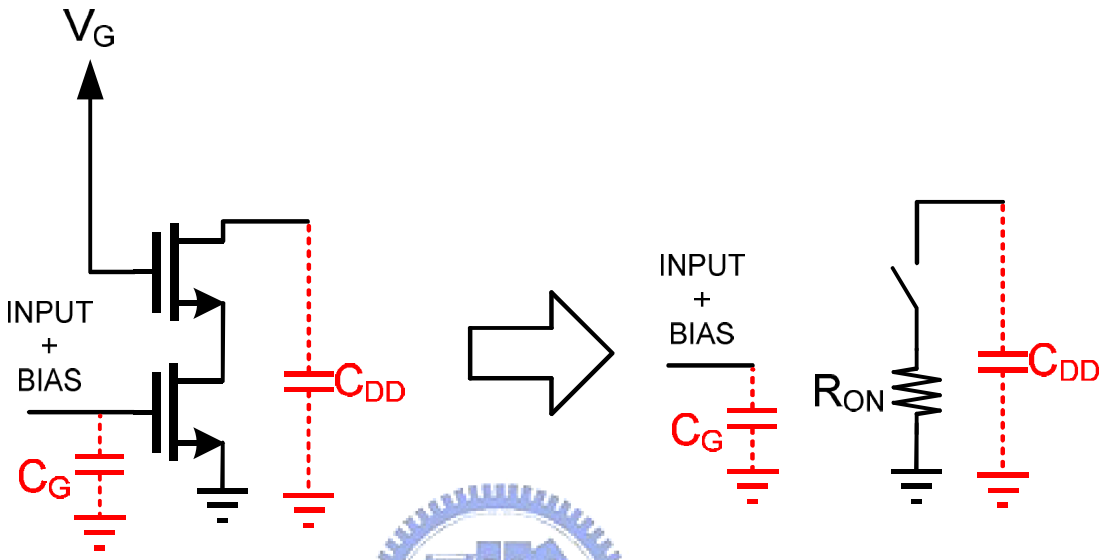


Figure 12 The cascode can be modeled as a shunt capacitor at both gate and drain, a turn-on resistance, and an ideal ON/OFF switch

With employing equation (2.16) and (2.17), equation (2.18) can be arranged to

$$\left.\frac{P_{loss}}{P_{out}}\right|_{R_{on}} = 1.365\frac{R_{on\_n}}{W_g R} = 7.46\frac{\omega_0 R_{on\_n} C_{DD\_n}}{\alpha} \tag{2.19}$$

The maximum allowable device width is achieved with the C_{shunt} is totally composing of the drain capacitance C_{DD}, i.e. α=1. Besides, larger device size makes the gate capacitance increase which causes the loading effect to the driving stage. Its effect can be diminished by

employing a shunt inductor at gate terminal. When the shunt inductor resonates with the gate capacitance, the loading effect can be alleviated.

2.4.2 Dissipative Mechanism Due To The Resistive Loss of L_b

In practice, the inductance L_b can be implemented by a bondwire of package. The quality factor of L_b is assumed to be Q_b so that the parasitic serial resistance can be expressed as $R_b = \omega_0 L_b / Q_b$.

Regarding resistor R_b and R as a voltage divider, the power loss due to R_b which is normalized to output power can be expressed as:

$$\left.\frac{P_{loss}}{P_{out}}\right|_{R_b} = \frac{R_b}{R} = \frac{\omega_0 L_b}{Q_b R} = \frac{Q_{load}}{Q_b} \tag{2.20}$$

$$Q_{load} = \frac{\omega_0 L_b}{R} \tag{2.21}$$

2.4.3 Dissipative Mechanism Due To The Resonant Tank of L_1 and C_1

The parallel resonant tank is assumed to form the impedance transformer with C_m only due to the sake of simplicity. All the required inductance for optimized Class-E operation is

provided by L_b.

This tank can be modeled as an inductor which provides 9/8 times inductance of L_1 and exhibits a quality factor Q_t. The power loss due to the tank can be expressed as equation (2.22).

$$\left.\frac{P_{loss}}{P_{out}}\right|_{R_s} = \frac{R_s}{R_L} = \frac{\omega_0 \, 9/8 \, L_1}{Q_t R} = \frac{Q_{match}}{Q_t} \tag{2.22}$$

where Q_{match} is expressed as equation (2.14).

2.4.4 Drain Efficiency

According to the calculations shown above, the overall power efficiency can be derived. The definition of drain efficiency is defined as equation (2.23).

$$DE = \frac{P_{out}}{P_{DC}} = \frac{P_{DC} - P_{loss}}{P_{DC}} \tag{2.23}$$

In the calculations shown above, it is assumed that the power efficiency is 100%, that is $P_{out} = P_{DC}$. So that, the drain efficiency based upon the calculations above can be expressed as:

$$DE = \frac{P_{out}}{P_{DC}} = \frac{P_{DC} - P_{loss}}{P_{DC}} = 1 - \left.\frac{P_{loss}}{P_{out}}\right|_{ALL} = 1 - \left(\left.\frac{P_{loss}}{P_{out}}\right|_{R_{on}} \times \left.\frac{P_{loss}}{P_{out}}\right|_{R_b} \times \left.\frac{P_{loss}}{P_{out}}\right|_{R_s} \right) \tag{2.24}$$

by replacing with (2.19), (2.20), and (2.22), it can be arranged as:

$$DE = 1 - \left(7.46 \frac{\omega_0 R_{on\_n} C_{DD\_n}}{\alpha} \times \frac{Q_{load}}{Q_b} \times \frac{Q_{match}}{Q_t} \right) \tag{2.25}$$

It is apparently that the loss of a Class-E power amplifier is depended on the characteristic of the selected active devices and passive components while ω_0, α, Q_{load}, and Q_{match} are the design parameters which can be selected by a designer. CMOS process provides the worst parasitic effects but the best integration. In the age of system-on-chip (SoC), it is a great benefit although it provides the worst parasitic effects.

After the implementation on CMOS process is determined, the only thing we can control is the actual resistance. With larger actual loading resistance R, Q_{load} and Q_{match} can be lower and the drain efficiency is also improved. But, the actual resistance can be extremely high because the low supply voltage. For instance, if a Class-E power amplifier provides 25 dBm high output power with 2.5-V supply voltage in 0.25-μm CMOS process, the actual load resistance calculated by equation (2.7) can be as high as 11.4Ω. As for 1.2-V supply voltage, the actual resistance is as small as 2.63Ω. It seems that as the channel length shrinking, CMOS process does not suitable for the implementation of Class-E power amplifiers.

In order to provide high efficiency and high output power, high supply voltage is necessary. The cascode topology allows about two times higher supply voltage than that of a common-source by stacking two active devices. With employing the second and third order harmonics suppression technique, not only the second and third order harmonics would be suppressed at the output terminal but the maximum achievable efficiency is improved to 81.65% in theoretical.