Chapter 3

Circuit Simulation And Implementation

The analysis of a cascode Class-E power amplifier and the second and third order harmonics suppression technique is discussed in the previous chapter. An implemented cascode Class-E power amplifier with second and third order harmonics suppression technique is described in this chapter.

Section 3.1 describes the layout considerations for higher power efficiency. The printed circuit board (PCB) design for testing is mentioned in section 3.2. The simulation results of the implemented cascode Class-E power amplifier and the comparison of CMOS Class-E PAs are shown in section 3.3. Section 3.4 shows the comparison between the proposed work and others. Section 3.5 states the way to measure the implemented cascode Class-E power amplifier.

3.1 Layout Considerations

The layout of the implemented cascode Class-E power amplifier is shown in Figure 25.

Due to the requirement of higher PAE, the passive components are all implemented on board. In the simulation results, the maximum peak current is up to around 0.5A. According to the documents provided by UMC, the maximum allowable AC current of top metal is 16.9mA for 1-μm width. In order to sustain such high current, we use 60-μm metal width for the interconnection of M1 to M2 and M2 to I/O pad to ensure the safety. The total area is 484*1140 um^2.

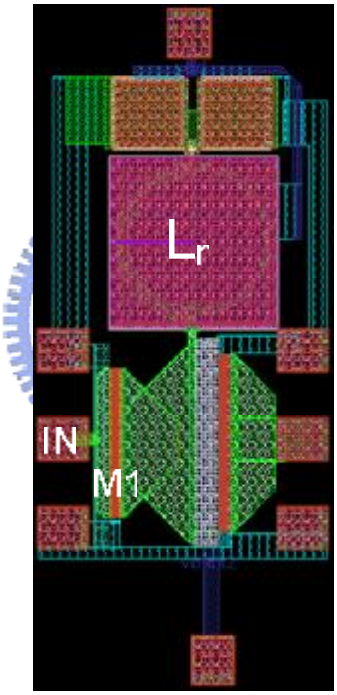

Figure 13 The layout of the implemented cascode Class-E power amplifier.

3.2 Printed Circuit Board (PCB) Design

In order to achieve higher power efficiency, higher quality value of passive components are

required. It is no doubt that the input and output networks should be implemented on PCB board for higher power efficiency. The layer stack-up is illustrated in Figure 14. The loss tangent (δ= 0.0021) and dielectric constant stability for RO4003 material is superior to FR-4, so that RO4003 severs as the dielectric material (ε_r= 3.38) between layer 1 and layer 2. Layer 2 and layer 3 provide large and low impedance power planes. The area of the power planes near the chip look like a good, high frequency capacitor and help with decoupling.

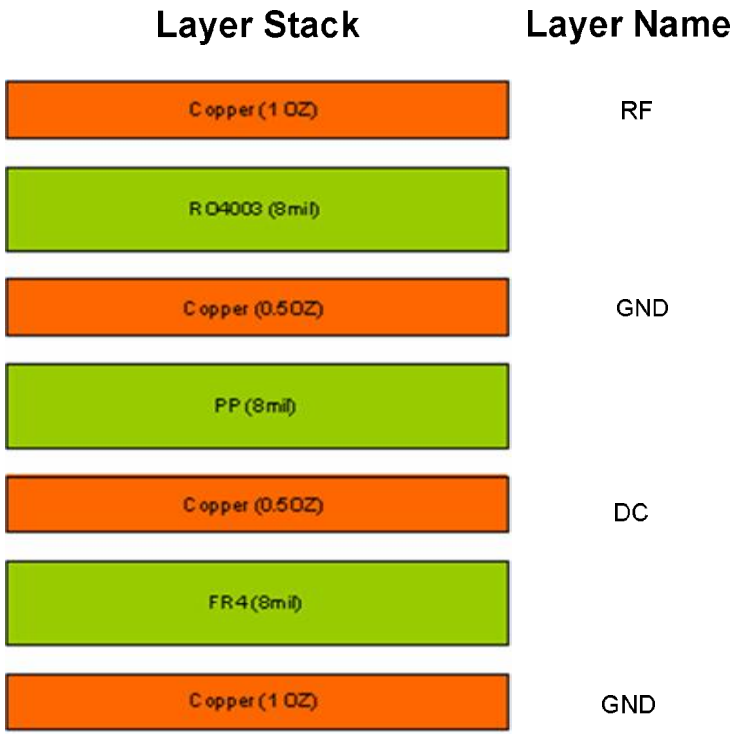

Figure 14 Layer stack-up of PCB board.

There are two PCBs required in this design are shown in Figure 15 and Figure 16 correspondingly. Fifth order Chebyshev filter is used for input matching network, and the adjustability is added to the output network to compensate the process variation.

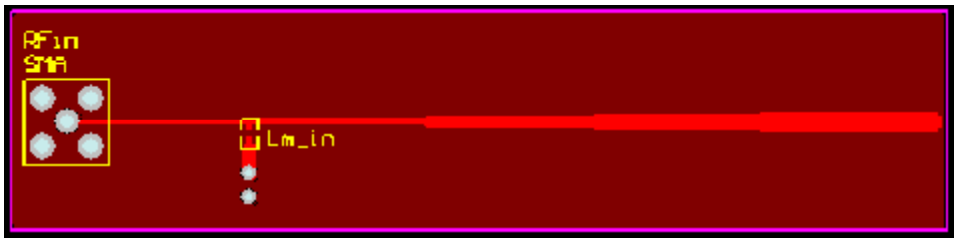

Figure 15 PCB with Chabyshev filter input matching.

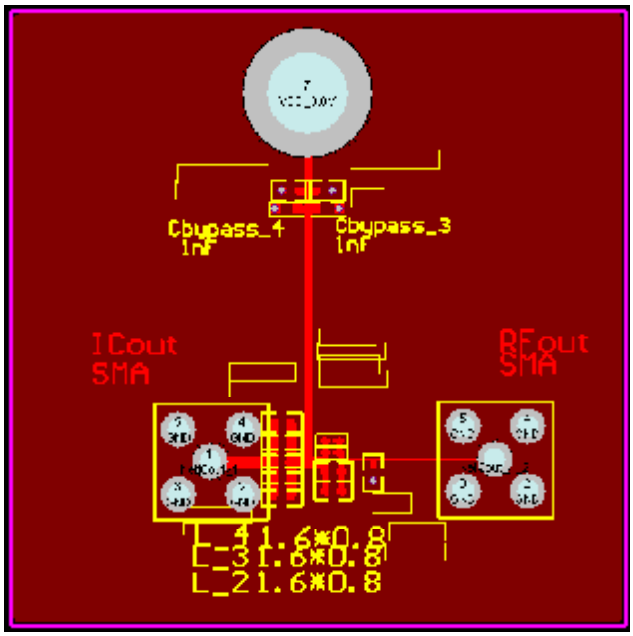

Figure 16 PCB without passive input matching.

3.3 Simulation Results

The post-layout simulation results including all the considerations that mentioned above will be shown in this section. The schematic on RFDE is illustrated in Figure 17. The gate-to-drain voltage must be first checked for the stability of the circuit and the simulation result is shown in Figure 18. According to the documentation of UMC 0.13-μm CMOS

process, the breakdown voltage of gate-to-drain is nominal 8.5-V. As we can see in Figure 18, the both MOSs of cascode Class-E PA operate in the safety region and the maximum gate-to drain bias of M2 is 7.21V.

The overall power-added efficiency (PAE) is shown In Figure 19. Maximum PAE is achieved about 63.4%. Ranging from 2.39GHz to 2.69GHz, the power-added efficiency (PAE) is higher than 49%. As illustrated in Figure 20, this cascode Class-E power amplifier provides maximum 24.7dBm output power.

Due to the harmonic suppression loading network, the harmonic suppression exhibits great performance in Figure 21. It is apparently that the quarter wavelength transmission line provides great and smooth performance of second order harmonic suppression. The maximum second order harmonic suppression is 75.8dBc at 2.56GHz and the maximum third order harmonic suppression exhibits 59dBc at 2.42GHz.

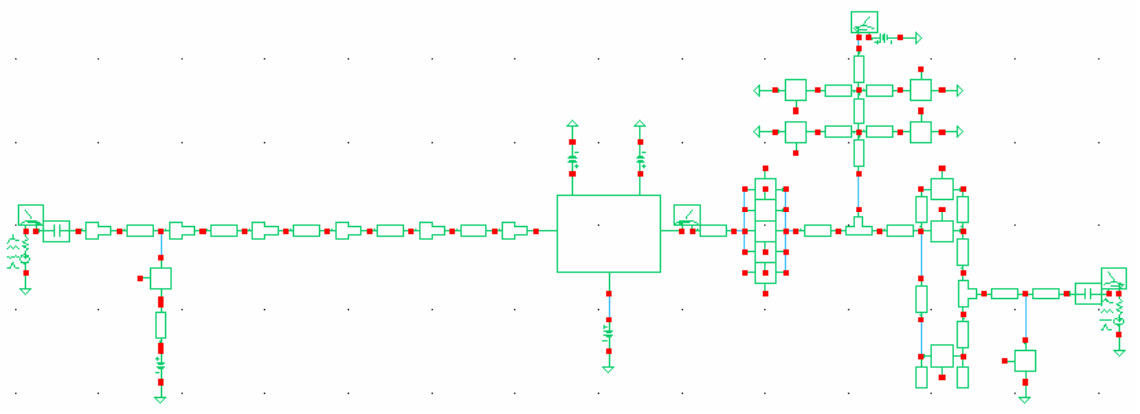

Figure 17 Schematic on RFDE.

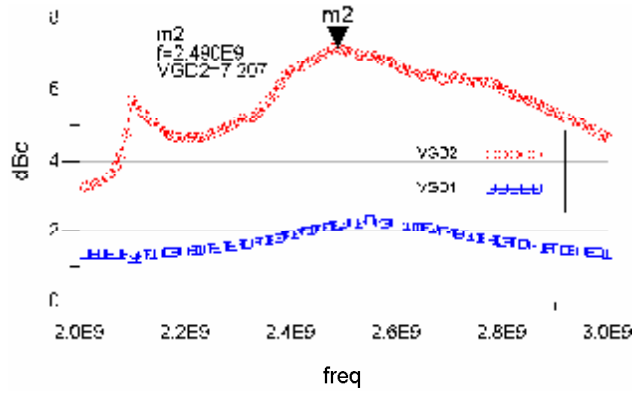

Figure 18 Gate-to-drain voltage of common-gate stage.

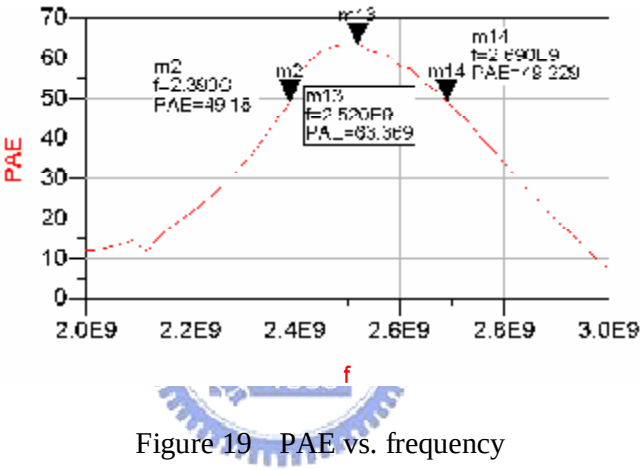

Figure 19 PAE vs. frequency

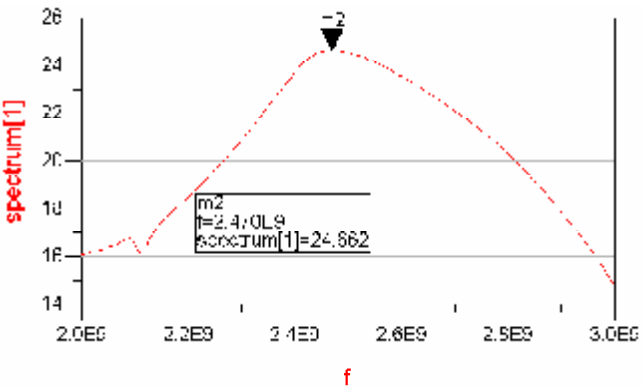

Figure 20 Output power vs. frequency.

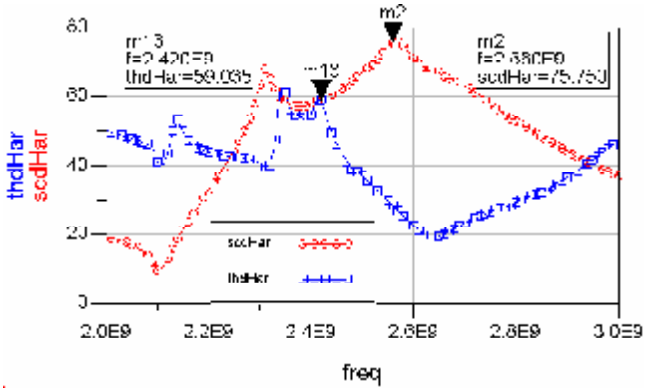

Figure 21 Second and third order harmonics suppression.

Under the same gate-to-drain voltage stress and the same loading network, the common-source can provides maximum 22.85dBm output power and maximum 63.8% PAE with 3.1-V supply voltage. The schematic and simulation results are illustrated in Figure 22, 23, 24, and 25. cascode Class-E PA can provides about 2 dB higher output power

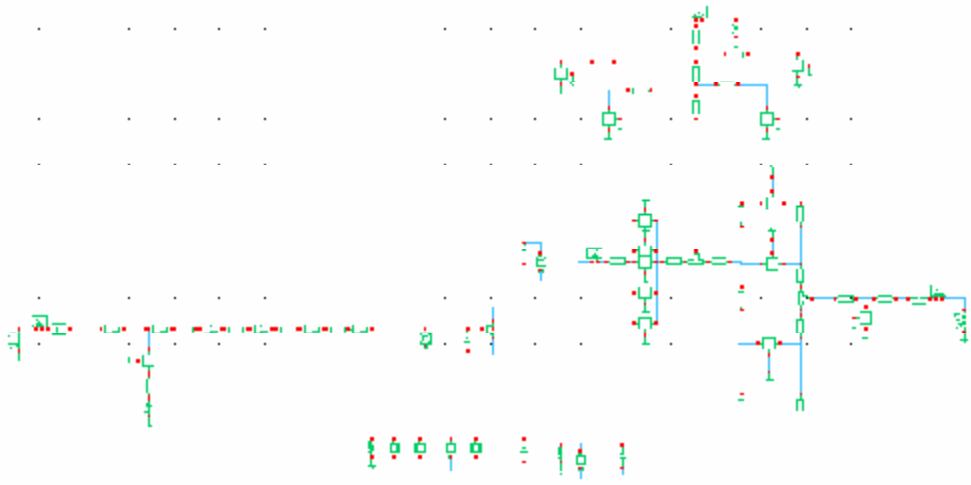

Figure 22 Schematic of common-source Class-E PA.

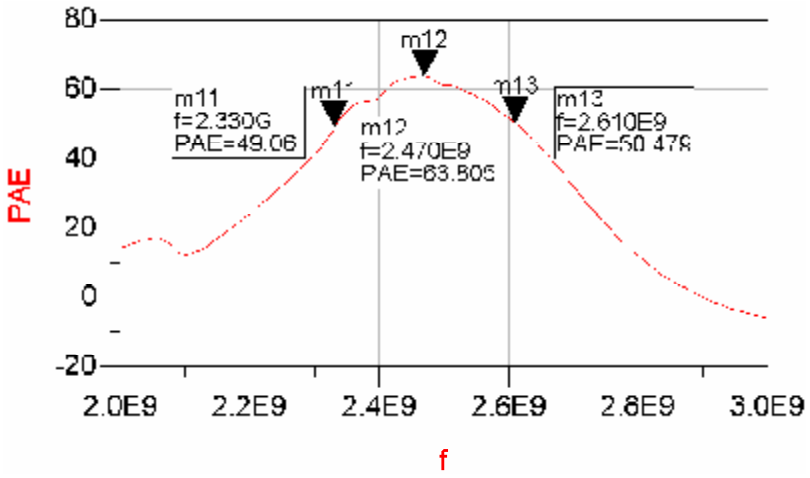

Figure 23 The PAE result of Common-source Class-E PA.

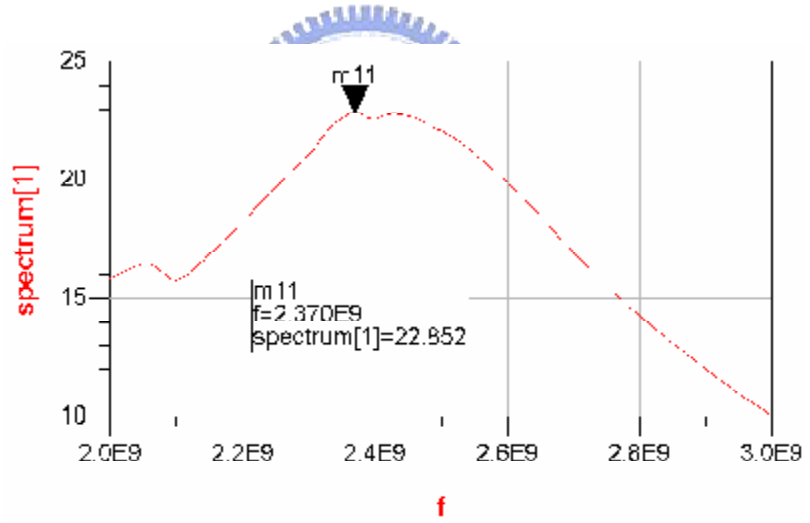

Figure 24 The output power result of Common-source Class-E PA.

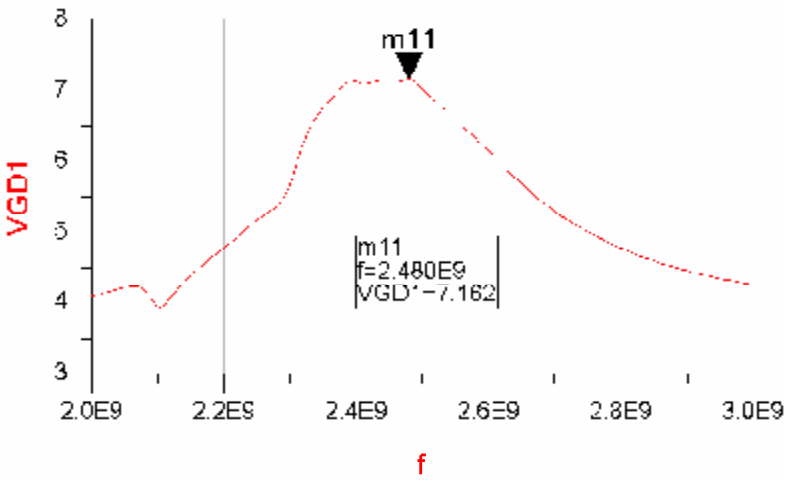

Figure 25 The gate-to-drain voltage stress of Common-source Class-E PA.

3.4 Comparison

The comparison table of FoM is listed in Table 6. In theory, the differential topology benefits double output voltage, i.e. 3-dB higher output power, compared with single-ended topology. In FoM comparison, the differential topology has great benefit among others. It is apparently in the comparison table that cascode topology has higher PAE than others. We can see that this design has second high power-added efficiency (PAE) and the highest FoM despite of the differential topology.

Table 7 shows the comparison of harmonics suppression. We can see that the transmission line and parallel resonant tank have good performance at harmonic suppression.

Title	Fc (GHz)	VDD	Tech.	Topology	Pout (dBm)	PAE (%)	FoM
1999_[14]	1.98	2	0.35	Differential	30	48%	**1881.79**
2002_[31]	0.7	2.2	0.35	Differential	30	62%	303.80
2003_[29]	5.7	2.1	0.18	Differential	25	42.60%	**4376.83**
2003_[28]	2.65	1.7	0.25	Mode-Locking	25.5	35%	872.09
2005_[25]	2.4	3.3	0.18	CS	21.3	40%	310.80
2005_[27]	0.9	4.5	0.5	CS	25	61%	156.25
2001_[15]	0.9	1.8	0.25	common-gate	29.5	41%	295.98
2003_[18]	2.5	1.2	0.35	Common-Gate	20	33%	206.25
2003_[30]	2.4	2.5	0.35	Cascode	20	59%	339.84
2006_[24]	1.7	2.5	0.28/0.13	Cascode	23	67%	386.34
My work (post-sim)	2.54	4	0.34/0.13	Cascode	24.66	**63.4%**	1196.07

Table 6. Comparison table of CMOS Class-E PAs

	2^{nd} Harmonic Suppression	3^{rd} Harmonic Suppression
2006_[24] (cascode)	26 dBc	47 dBc
2002_[31] (differential)	Higher than 60 dBc	Higher than 60 dBc
My design (w/ PCB layout)	Max 75.8 dBc	Max 59 dBc

Table 7. Comparison table of harmonics suppression.

3.5 Measurement Plan

During the measurement of the implemented cascode Class-E PA, the input and output probes would be a part of the device under test. Before the measurement is beginning, the parasitic effects of the input and output probes should be extracted at first. We can get the S2P file of these two probes when these two probes are connected as a device under test as illustrated in Figure 26. Assuming the two probes are identical and neglecting the effect of through, the parasitic effect of each probe can be extracted by behavior modeling technique and then divided by two.

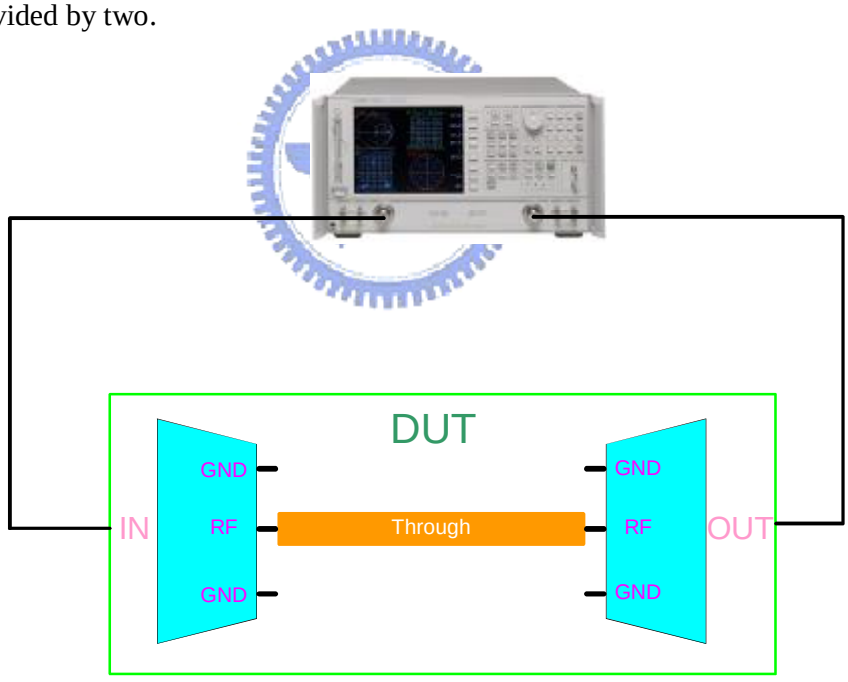

Figure 26 Measure the S2P files of the input and output probes with the through calibration kit.

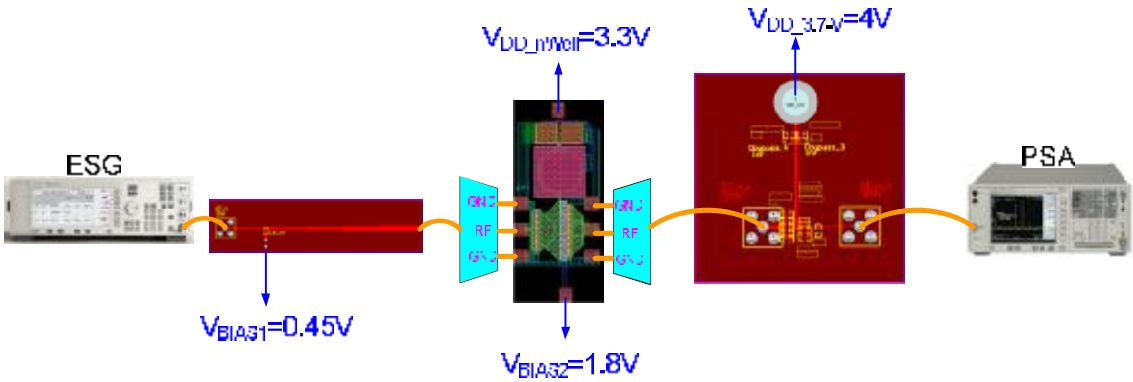

Figure 27 Measurement setup.

The equipment setup is illustrated in Figure 27. After equipments and testing boards are connected as Figure 27 with proper input power and bias voltage, the output power and power efficiency can be obtained by ESG and PSA. An optimized input power is fed in by ESG, and the output tone can be obtained by the PSA.