Chapter 4

Power-Related Behavior Model

The design considerations and circuit implementation of cascode Class-E power amplifier with harmonics suppression technique are presented as before. In this chapter, a power-related behavior model is proposed to save the simulation time. The simulation time of large-signal S parameters can be reduced to about 1/23,640 which is compared with the implemented cascode Class-E PA on package.

The input matching network behavioral modeling will be presented in section 4.1. The behavior model of output matching network will be discussed in section 4.2. In section 4.3, the performance and achievement will be summarized.

4.1 Modeling of Input Matching Network

The presented behavior model is based on the package version of the implemented cascode Class-E PA with harmonics suppression technique. The schematic of the implemented circuit package version is shown in Figure 28.

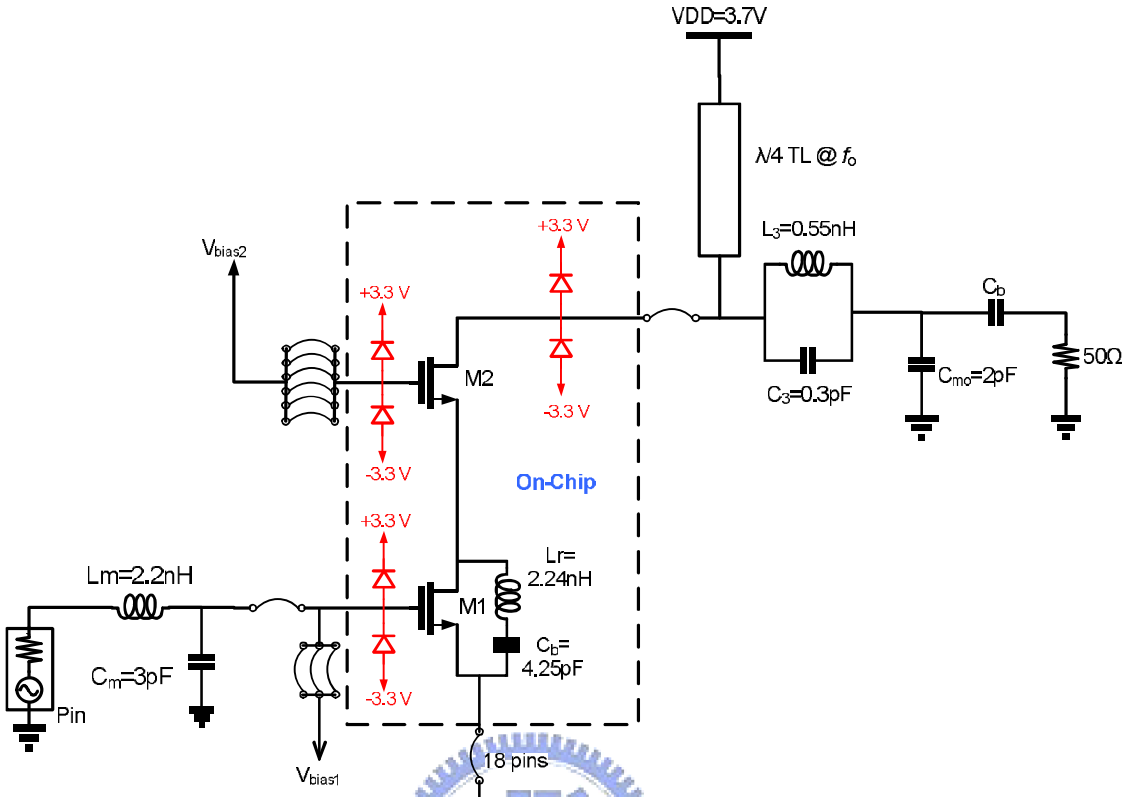


Figure 28 The schematic of the implemented circuit package version.

The schematic of input matching network after parasitic extraction is shown in Figure 29, where the C_p is the extracted parasitic capacitance at gate of the common-source stage. In the input matching network, it is divided into five parts for easier modeling which are shown in Figure 29. Part one consists of a passive inductor with 1.3nH, and part two consists of a passive capacitor with 2.7pF. Part 3 consists of one serial bondwire and three parallel bondwires connecting to the gate bias of common-source stage. Part 4 consists of four sets of pad and ESD diodes including the extracted parasitic capacitance C_p. Part 5 consists of the input impedance of the common-source stage and eighteen grounded pins.

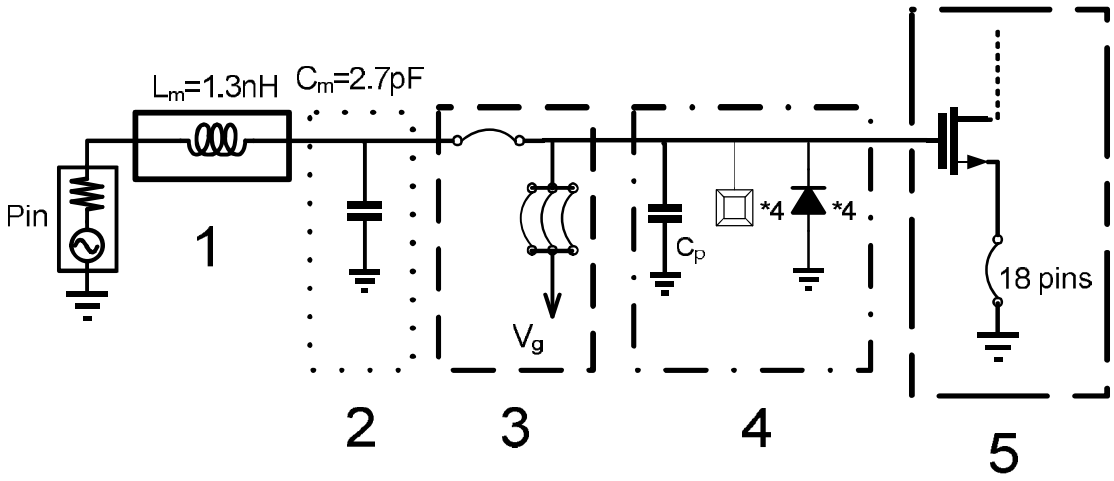


Figure 29 The schematic of input matching network.

According to the simulation results shown before, the optimized input power is 12dBm, and therefore, 12dBm input power is chose to be the initial parameter. The five parts can be modeled individually and then put them together to form the entire behavioral model input matching network. The cursory behavioral model is shown in Figure 30.

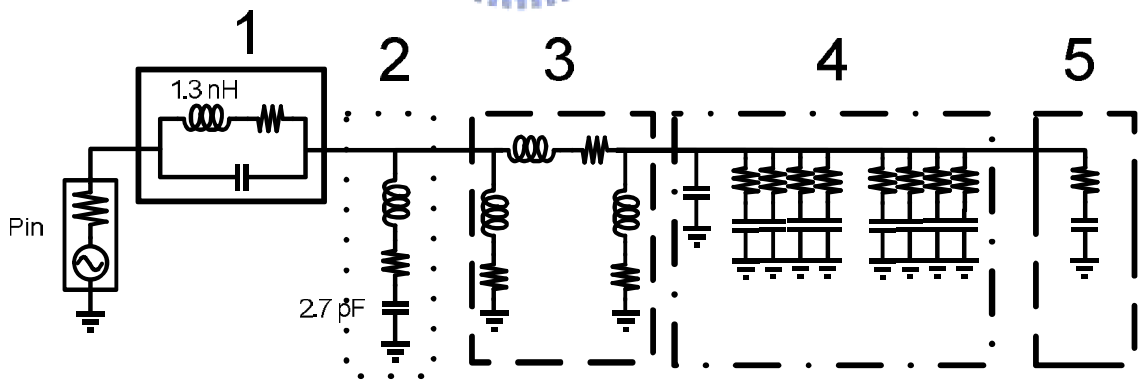


Figure 30 The cursory behavioral model of the input matching network.

As shown in Figure 30, the part 4 consisting of extracted capacitance, pads, and ESD

diodes can be simplified as a serial pair, consisting of a capacitor and a resistor, and it is shown in Figure 31. The comparisons of S parameter and input impedance between the transistor level and the proposed behavioral model based on 12dBm optimized input power are shown in Figure 32 and 33, respectively. In Figure 32, it is apparently that the tendency of the proposed behavioral model is very similar to the simulation result of transistor level in decibel of S parameter, while the phase of the proposed model is almost the same as that of the transistor level. As to the input impedance, there are large variances at both the peak and the trough.

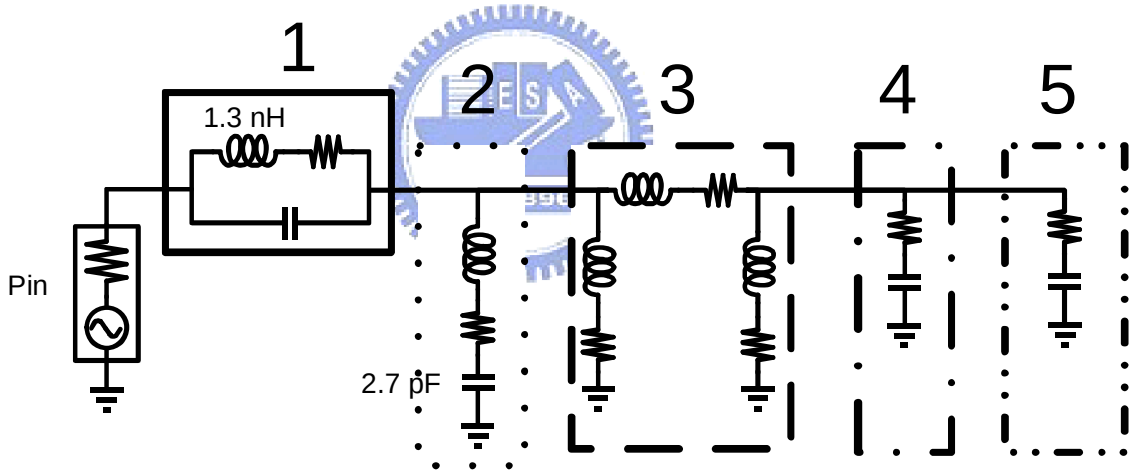


Figure 31 The cursory behavioral model of the input matching network.

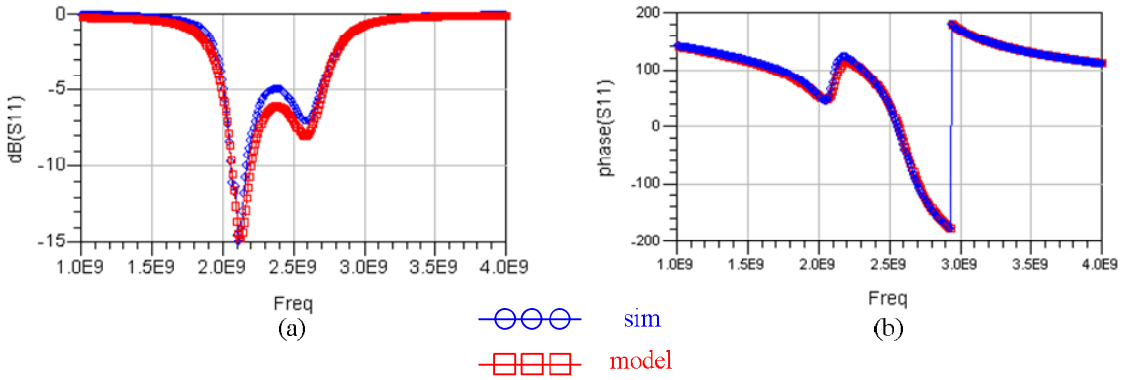


Figure 32 The comparison of S parameter between the transistor level and proposed behavioral model.

(a) S parameter comparison in decibel (dB); (b) S parameter comparison in phase (degree).

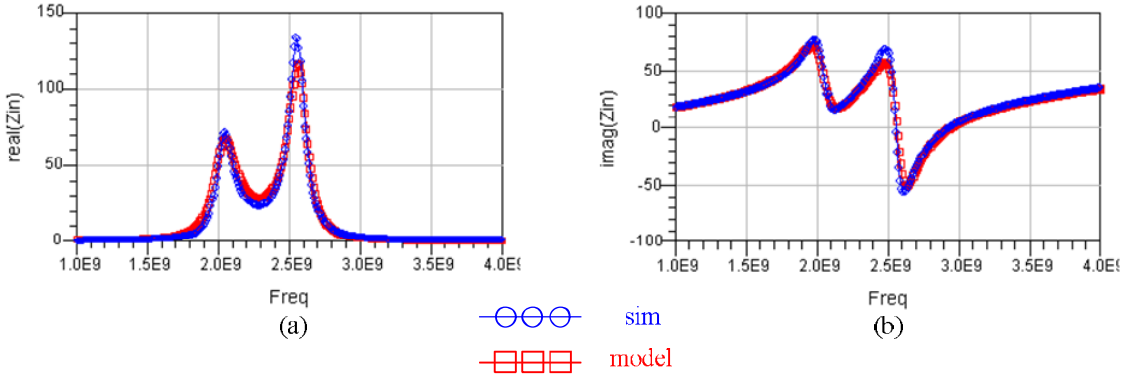


Figure 33 The comparison of input impedance between the transistor level and the proposed behavioral model.

(a) The input impedance comparison in real part; (b) The input impedance comparison in image part.

Because the input impedance would be varied with different input power, the coefficient of

input power should be added in the proposed behavioral model. Fortunately, the passive components, such as inductors, capacitors, bondwires, pads, and ESD diodes, are not varied with different input power but the input impedance of the transistor, i.e. the part 5. In order to get the correct values of R and C in part 5, varied input power ranging from 8dBm to 13dBm is fed into the transistor level circuit. By using equations to subtract the effects of passive components, the correct impedance of part 5 can be found easily and the R and C value of part 5 can be expressed as:

$$R = 3.1128\times10^{-4}\times Pin^3 + 7.8482\times10^{-3}\times Pin^2 - 0.019408\times Pin + 1.3243 \quad (4.1)$$

$$C = 4.1392\times10^{-14}\times Pin + 3.9473\times10^{-12} \quad (4.2)$$

where the input power is ranging from 8dBm to 13dBm.

The real part and image part of impedance comparisons between the transistor level and proposed model with input power ranging from 8dBm to 13dBm are shown in Figure 34 and 35, respectively. No matter real part or image part, the results of the simplified model and those of transistor level are almost overlapped. The variances between the simplified model and transistor level with different input power are listed in Table 8. The average variance is $1.097 - j\ 1.297$ohm.

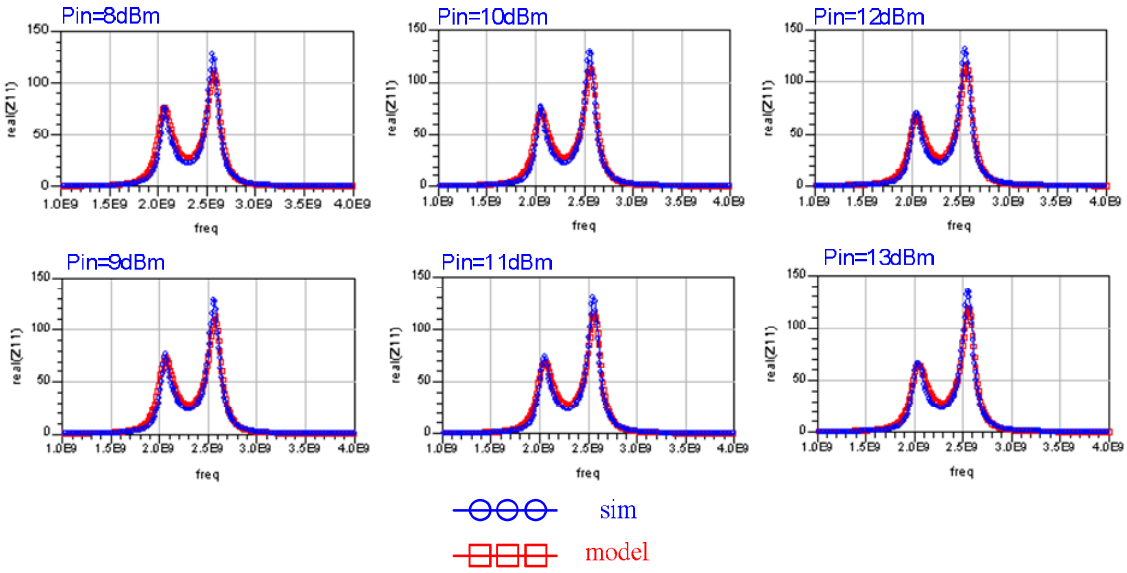


Figure 34　The real part of impedance comparison with input power ranging from 8dBm to 13dBm.

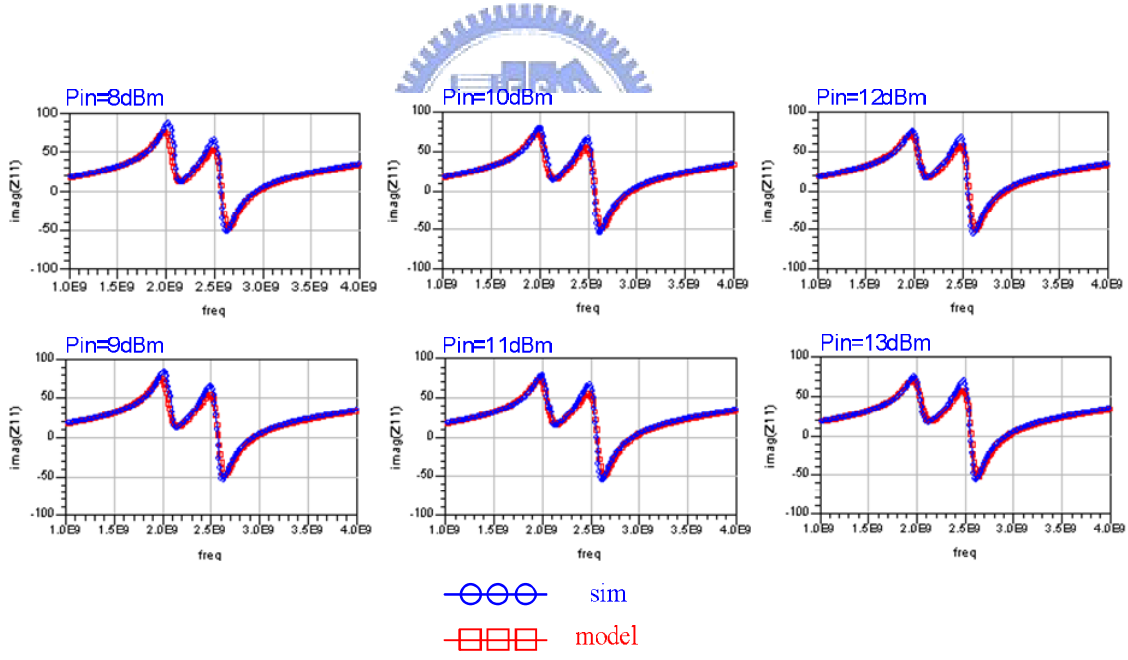
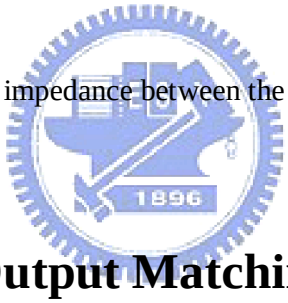


Figure 35　The image part of impedance comparison with input power ranging from 8dBm to 13dBm.

Input Power (dBm)	Variance
8	$1.551 - j\,3.553$
9	$1.024 - j\,2.459$
10	$0.673 - j\,1.367$
11	$0.713 - j\,0.451$
12	$1.259 + j\,0.008$
13	$1.361 + j\,0.041$
Mean	$1.097 - j\,1.297$

Table 8. Variances of input impedance between the simplified model and transistor level.



4.2 Modeling of Output Matching Network

The schematic of output impedance is shown in Figure 36. As the same method that mentioned before, the output matching network can be divided into six parts which are shown in Figure 36 without the DC-block, C_b. No matter in simulation or measurement, the DC-block C_b is just used to block the short path from VDD to the 50Ω termination, and its effect should be neglected in behavioral model. According to the statement of model document provided by UMC, the negative resistance will be occurred at drain due to the self heating effect at high gate and drain bias caused by too large gate width of RF transistor. In

the proposed modeling method, it is difficult to model the negative resistance at drain. Therefore, the output impedance of the transistor is modeled together with the pad, ESD diodes, and bondwire to reduce the effect of negative resistance. The quarter-wavelength transmission line is used as a resonator and it can be modeled as a parallel RLC equivalent circuit calculated in [32]. The simplified model of the output impedance network is shown in Figure 33.

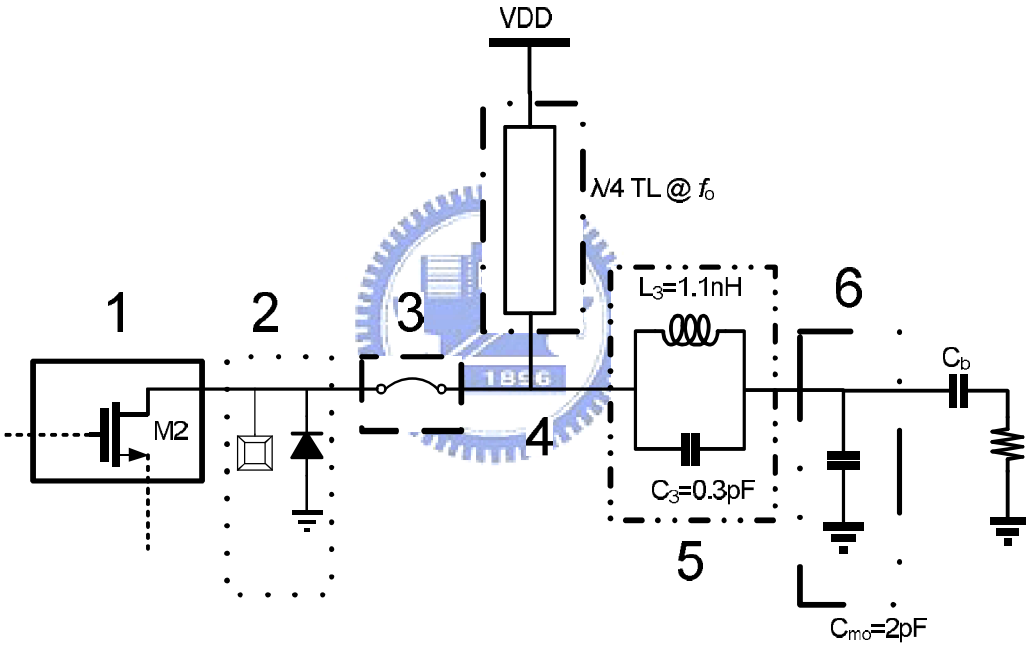


Figure 36 The schematic of output impedance matching network.

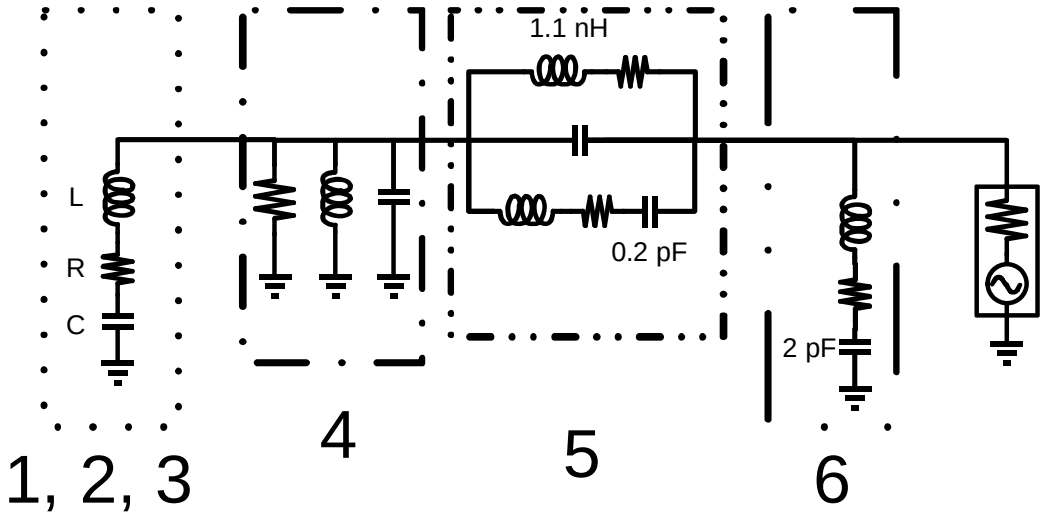


Figure 37 The simplified behavioral model of output impedance matching network.

Because large size of transistors may lead to instability, as stated in UMC documents, negative resistance would be occurred on the drain of M2. There is still no suitable modeling technique to model the negative resistance. For the simplicity, part 2 and part 3 illustrated in Figure 36 are included in the parasitic model of M2.

The comparison of S parameters between the transistor level circuit and the proposed behavior model are illustrated in Figure 38. Because the proposed method of modeling may not be suitable for the negative resistance, the variance of S parameters between the result of transistor level circuit and that of the proposed behavioral model is larger than that of the input matching network, but the tendency is much alike to the results of transistor level.

As similar to the input matching network, the values of RLC shown in Figure 37 can be expressed as equations below:

$$R = -3.3864\times10^{-5}\times Pin^{7} + 1.8179\times10^{-3}\times Pin^{6} - 3.8743\times10^{-2}\times Pin^{5} + 0.40958\times Pin^{4} - 2.1484\times Pin^{3} + 4.4912\times Pin^{2} \quad (4.3)$$

$$C = -1.0998\times10^{-17}\times Pin^{8} + 5.8348\times10^{-16}\times Pin^{7} - 1.2318\times10^{-14}\times Pin^{6} + 1.2945\times10^{-13}\times Pin^{5} - 6.7827\times10^{-13}\times Pin^{4} + 1.4232\times10^{-12}\times Pin^{3} \quad (4.4)$$

$$L = 1.0417\times10^{-12}\times Pin^{4} + 4.0509\times10^{-11}\times Pin^{3} + 5.7188\times10^{-10}\times Pin^{2} + 3.455\times10^{-9}\times Pin + 8.9153\times10^{-9} \quad (4.5)$$

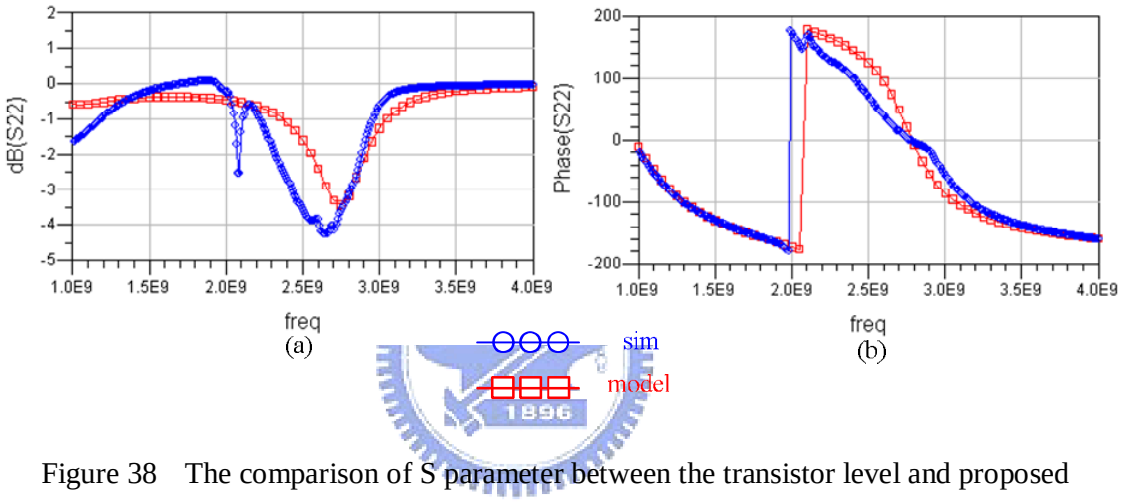


Figure 38 The comparison of S parameter between the transistor level and proposed behavioral model.(a) S parameter comparison in decibel (dB); (b) S parameter comparison in phase (degree).

The real part and image part of output impedance comparisons with different input power are illustrated in Figure 39 and Figure 40, respectively. Although the output model is not as precise as the input model, the tendency of output impedance versus frequency has been sketched. The variances of the simplified model and transistor level are listed in Table 9, and the average variance is $10.469 - j\ 22.371$ohm.

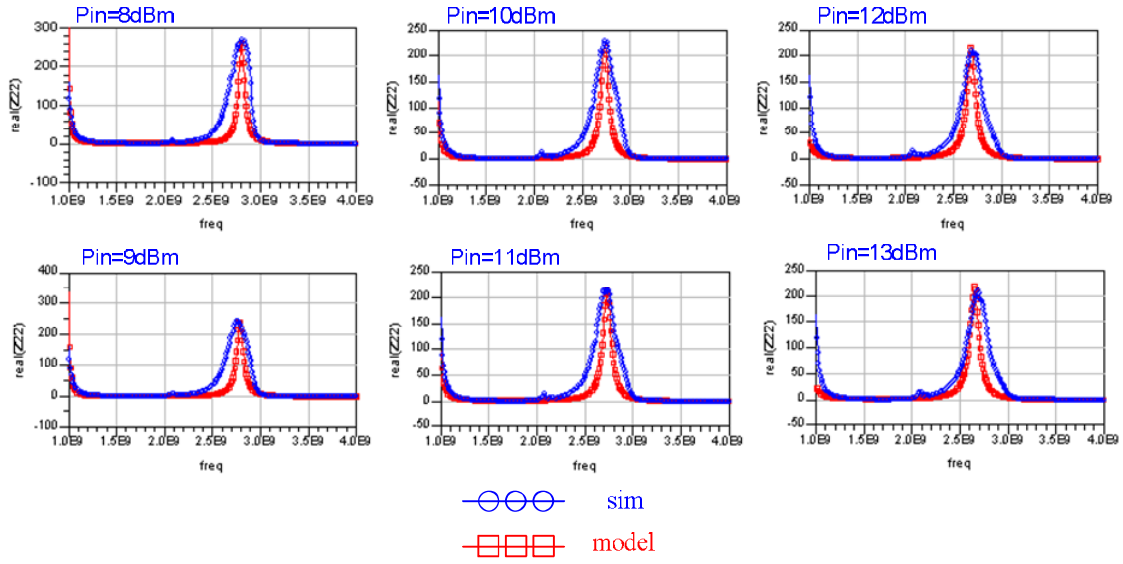


Figure 39　The real part of output impedance comparison with input power ranging from 8dBm to 13dBm.

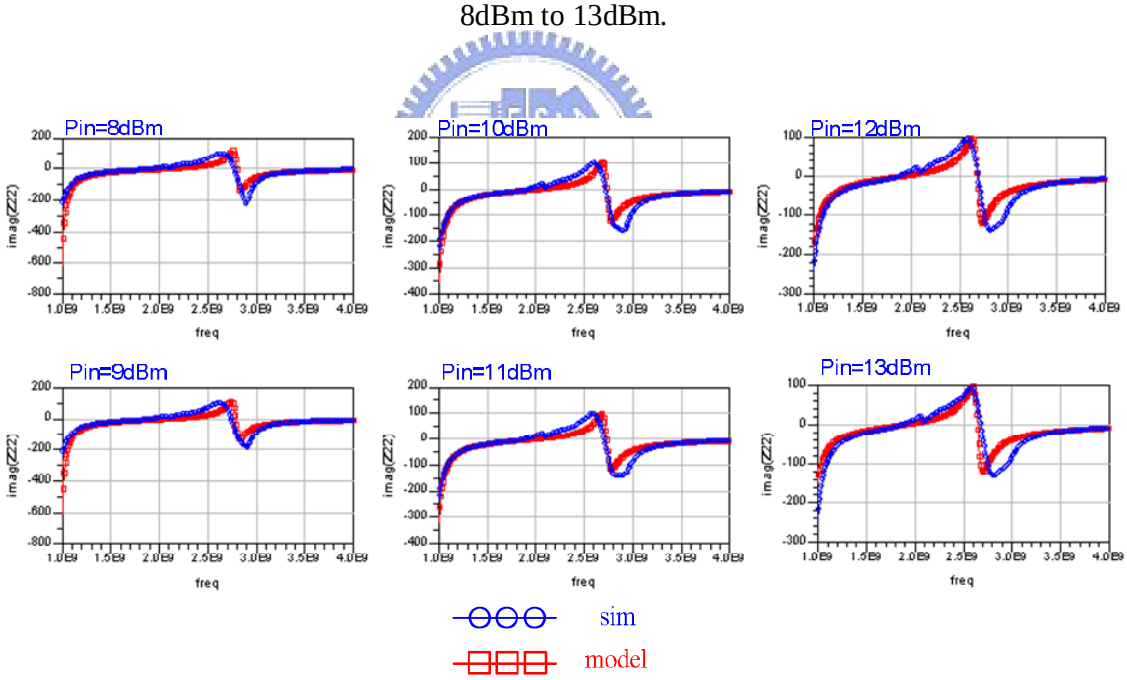


Figure 40　The image part of output impedance comparison with input power ranging from 8dBm to 13dBm.

Input Power (dBm)	Variance
8	$17.672 - j\ 18.398$
9	$13.256 - j\ 22.816$
10	$10.229 - j\ 23.797$
11	$8.25 - j\ 23.697$
12	$7.011 + j\ 23.136$
13	$6.394 + j\ 22.385$
Mean	$10.469 - j\ 22.371$

Table 9. Variances of output impedance between the simplified model and transistor level.

4.3 Behavioral Model of The Implemented Cascode Class-E PA

In the comparison of simulation time, the simulation time of large signal S parameters of the transistor level circuit from 2GHz to 3GHz with 10MHz step is 6,746 seconds; while the simulation time of the proposed behavioral model including input and output matching model is 0.2 seconds. With varying input power from 8dBm to 13dBm, the transistor level circuit consumes 31,916 seconds, and the behavior model consumes just 1.35 seconds. The simulation time is reduced to about 1/23,640. The variances of input and output impedance

are $1.097 - j\,1.297$ and $10.469 - j\,22.371$, respectively.