On Reducing Clock Network Power Consumption by Low-Swing DME Buffering Technique

Student: Yun-Ta Lin Advisor: Prof. Hung-Ming Chen

Department of Electronics Engineering
Institute of Electronics
National Chiao Tung University

ABSTRACT

In modern VLSI design, clocking has consumed significant power in total chip power dissipation. Chips running at higher frequency consume much more power. Without carefully planning clock network, the chips will suffer from high power dissipation. In this thesis, we present a methodology which can be applied in buffered clock tree synthesis to achieve low power demands and zero-skew constraint. It is based on the low-swing interconnections for the clock signal translation and the low-swing double-edge triggered flip-flop for synchronizing elements. Furthermore, we reduce the number of buffers inserted as well as wire length in order to lower power consumption. The experimental results are encouraging. We obtain average 49% power saving, compared with previous work based on low-swing interconnection.