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電子工程學系　　電子研究所碩士班

碩 士 論 文

超寬頻無線網路應用之
單一鎖相迴路頻率合成器設計

Single Phase-Locked Loop Frequency Synthesizer Design for Ultra-wideband Wireless Applications

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中華民國九十五年六月

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摘要。

本論文完成一個可以合成 UWB 全部頻帶的頻率合成器設計，其中，為了防止因使用多組鎖相迴路而造成有多組電壓控制震盪器產生雜訊的互相干擾，本架構只使用了一組鎖相迴路，鎖相迴路中使用了連續的除二電路來產生合成 UWB 頻帶所需的中間頻率，這可減少混波器使用的數量並達到快速切換時間的要求，此外為了濾除不必要的突波雜訊，一組除二電路放置在混波器的下一級來減輕這個問題，且在輸出級有電感電容共振腔當作帶通濾波器來去除雜訊，其中電感電容共振腔還有負電阻和使用電感開關來提高操作的頻率範圍和更有效的去除雜訊，最後，突波雜訊在所有的頻帶都可被壓制在比-24dbc 以下.

Single Phase-Locked Loop Frequency Synthesizer Design for Ultra-wideband Wireless Applications

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Abstract

A CMOS frequency synthesizer which synthesizes all band groups of the ultra-wideband (UWB) system is presented. Only one phase-locked loop is used in this synthesizer to reduce interference of VCOs in multi-PLL frequency synthesizers. Divide-by-two circuit chains are used in the PLL to generate intermediate frequencies and reduce the numbers of required single-sideband (SSB) mixers for all-band frequency synthesis and thus achieve fast switching time. To suppress spurious emissions, the frequency synthesizer employs dividers and SSB mixers in the signal generation path. LC resonant loads at the output buffer together with negative resistances and switching inductors help to suppress more spurious signals and operate in wider frequency range. The spurious suppression is better than -24dBc in all band groups.

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Chapter 1
Introduction

1.1 Background

Recently, the Federal Communications Commission (FCC) in US approved the use of ultra-wideband (UWB) technology for commercial applications in the 3.1-10.6 GHz. UWB performs excellently for short-range high-speed uses, such as automotive collision-detection systems, through-wall imaging systems, and high-speed indoor networking. It plays an increasingly important role in wireless personal area network (WPAN) applications. This technology will be potentially a necessity in our daily life, from wireless USB to wireless connection between DVD player and TV, and the expectable huge market attracts various industries. European Computer Manufacturers Association (ECMA) has released a UWB standard (ECMA-368) based on the proposal of Multi-Band OFDM Alliance for a distributed medium access control (MAC) sublayer and a physical layer (PHY) for wireless networks and a standard (ECMA-369) for the interface between implementations of the PHY and MAC [1].

The newly unlicensed UWB technology opens doors to high-speed wireless communications and has been exciting tremendous academic research interest.

1.2 Motivation

ECMA-368 standard specifies the data rate can be up to 480 Mb/s by utilizing multi-band OFDM technology with frequency bands covering from 3.1-10.6 GHz and each channel bandwidth occupying 264MHz as shown in Figure 1.1. Such ultra-wide frequency bands and channel bandwidth introduce challenges for transceivers implemented in CMOS technology.

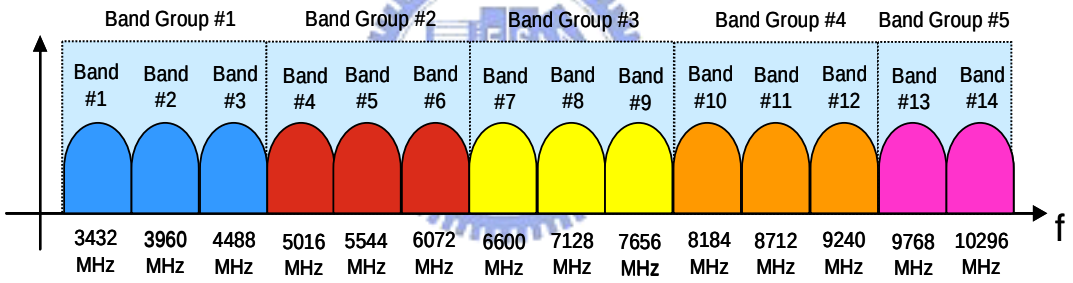


Figure 1.1 The Multi-Band OFDM frequency band plan

Figure1.2. illustrates a UWB transceiver architecture consisting a direct-conversion transmitter and receiver.

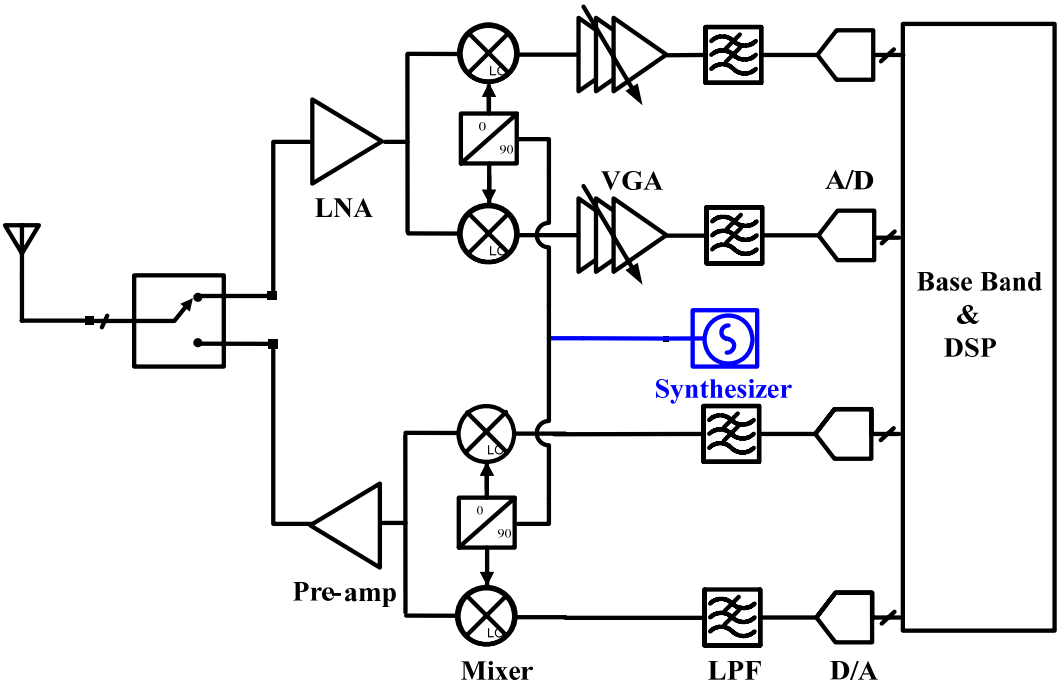


Figure 1.2 The direct-conversion architecture for UWB transceiver

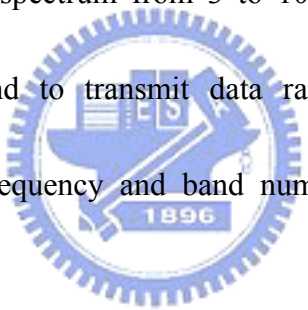
One of the advantages of direct-conversion architecture for receivers (in Figure1.2) is that there is no image problem, and it does not require an image-reject filter. This is because the frequency of the RF signal is exactly equal to the frequency of the LO signal. However direct-conversion receivers have some issues which should be mitigated carefully, such as DC offsets, I/Q mismatch, even-order distortion, and flicker noise. In order to achieve the goal of the RF-SOC, we choose the direct-conversion architecture to design the system.

The frequency synthesizer must provide a clean and stable LO tone. The frequency band is from 3.1GHz to 10.6GHz and the frequency switching time is 9.5ns which is very difficult to achieve with traditional synthesizers with only one phased-lock loop (PLL). Therefore, UWB frequency synthesizers may require more PLLs, selectors,

mixers, LC filters to achieve such short hopping time. In addition, UWB technology occupies such wide frequency range and any spurious emission will be a serious interferer for other wireless systems nearby. Therefore to suppress the spurious signals generated from the frequency synthesizer is very important. The goal of the thesis is to design a frequency synthesizer with fast switching time, wide synthesis frequency bands and low spurious emission for UWB transceivers.

1.3 UWB WPAN Specifications

ECMA368 partitions the spectrum from 3 to 10 GHz into 528MHz bands and employs OFDM in each band to transmit data rates as high as 480Mb/s. The relationship between center frequency and band number is given by the following equation:



Band center frequency=2904+528*Nb, Nb=1…14(MHz) (1.1)

The band allocation is summarized in Table 2.1.

Each band consists of 128 sub-carriers of 4.125MHz bandwidth. In contrast to IEEE 802.11a/g, MB-OFDM UWB employs only QPSK modulation in each sub-carrier. The system hops at the end of each OFDM symbol (every 312.5ns). The band switching must be in less than 9.47ns. It is difficult to synthesize frequency to different bands by changing the division of the divider in short time. In order to make hopping frequency in 9.47ns, mixers can be used to synthesize the frequency. When switching to a different

band is needed, change the input signal of the mixer allows fast switching to another band. In this way, a short switching time can be achieved.

Band Group	BAND_ID	Lower frequency	Center frequency	Upper frequency
1	1	3168 MHz	3432 MHz	3696 MHz
	2	3696 MHz	3960 MHz	4224 MHz
	3	4224 MHz	4488 MHz	4752 MHz
2	4	4752 MHz	5016 MHz	5280 MHz
	5	5280 MHz	5544 MHz	5808 MHz
	6	5808 MHz	6072 MHz	6336 MHz
3	7	6336 MHz	6600 MHz	6864 MHz
	8	6864 MHz	7128 MHz	7392 MHz
	9	7392 MHz	7656 MHz	7920 MHz
4	10	7920 MHz	8184 MHz	8448 MHz
	11	8448 MHz	8712 MHz	8976 MHz
	12	8976 MHz	9240 MHz	9504 MHz
5	13	9504 MHz	9768 MHz	10032 MHz
	14	10032 MHz	10296 MHz	10560 MHz

Table 1.1 OFDM PHY band allocation

1.3.1 Phase Noise

To derive the phase noise specification of the frequency synthesizer, consider the following equation [2]:

$$\text{rms noise} = \frac{180}{\pi} \cdot 10^{k/20} \cdot \sqrt{f_{loop}(1+10^{p/10}) + 10^{p/10} \cdot 2} \tag{1.2}$$

$$k = 20\log \frac{(\text{rms noise}) \cdot \frac{\pi}{180}}{\sqrt{f_{loop} \cdot (1+10^{p/10}) + 10^{p/10} \cdot 2}} \tag{1.3}$$

k is the in-band phase noise density (dBc/Hz), p is the peaking of k, f_{loop} is the loop bandwidth of the phase lock loop. The rms phase noise from 0 Hz up to infinity in the UWB proposal should be below 3.5 degrees rms. Assuming that p is zero and the

loop bandwidth is 300 kHz, in order to achieve the integrated phase noise below 3.5 degrees rms, the phase noise should below -82dBc/Hz. The result can be calculated via the following equation.

$$k = 20\log\frac{(3.5)\cdot\frac{\pi}{180}}{\sqrt{300k\cdot(1+10^{\%10})+10^{\%10}\cdot 2}} = -82.06(dBc/Hz) \qquad (1.4)$$

We can see the phase noise specification is not hard to do in the UWB system, but the spurious specification is difficult to achieve in the UWB system.

1.3.2 Spurious Tones

To derive the spurious tones specification of the frequency synthesizer, consider the Table 1.2 from [1], we can use maximum tolerable interferer at the antenna to calculate.

	Microwave Oven	Bluetooth & 802.15.1 Interferer	802.11b & 802.15.3 Interferer	802.11a Interferer	802.15.4 Interferer
Front-end pre-select filter attenuation (dB)	35	35	35	30	35
Max. tolerable interfere power at the antenna(dBm)	-7.3	-5.8	-5.8	-17	-7.1

Table 1.2 Interference and Susceptible Analysis

In the receive path, the SNR of the wanted signal is calculated by the following equation:

$$SNR = P_{wnated} - P_{noise} \tag{1.5}$$

$$SNR = P_{wnated} - (P_{\text{int}erfer} - P_{spurs}) \tag{1.6}$$

$$P_{spurs}(\Delta\omega) = P_{wanted} - P_{\text{int}erfer} - SNR \tag{1.7}$$

If we have front-end pre-select filter attenuation, the changes are as the following equations:

$$P_{spurs}(\Delta w) = P_{wanted} - P_{\text{int}erfer} - SNR + P_{filter} \tag{1.8}$$

For example, if the transceiver operates at band 1, and the data rate is 110Mb/s, the spurs specification at 1.032GHz can be calculated by the microwave. The minimum sensitivity of the receiver is -74.1dBm.The required SNR is 3.6dB.

$$P_{spurs}(1.032GHz) = -74.1 + 7.3 - 3.6 + 35 = -35.4(dBc) \tag{1.9}$$

The interferers may be mixed with the spurs of the LO signal and down-converted to baseband, corrupting the desired signal. In the UWB system, it is more difficult to meet the LO spurs specification than phase noise specification.

1.3.3 Switching Time

The switching time is different from the settling time. In the UWB system, the time between two hopping frequency is 9.47ns. It is difficult to change the division of the divider to meet the requirement. Selectors and mixers can be used to change the synthesized frequency to different bands, and therefore the switching time can be less than 9.47ns.

The overall design specification of the frequency synthesizer for UWB standard is shown in Table 1.3. The power consumption is designed as small as possible.

Parameters	Specification
Frequency range	3432Mhz~10296Mhz
Phase Noise	<-82.06dBc/Hz@100-kHz
Switching Time	<9.47ns
In-band spurs	<-12.6dBc
Out-band spurs(at2.5G)	<-36.9dBc
Out-band spurs(at5.2G)	<-30.7dBc
Supply Voltage	1.8 V
Process	UMC 0.18-μm CMOS

Table 1.3 Overall design Specification of the frequency synthesizer.

1.4 Organization

This thesis describes the design of CMOS frequency synthesizer for ultra wideband wireless PAN applications. Chapter 1 introduces the motivation and the specifications of frequency synthesizer for the UWB WPAN applications. Chapter 2 discusses the state of the art and the frequency planning in this work. Chapter 3 presents the spurious suppressing techniques in the proposed UWB frequency synthesizer. Chapter 4 presents the linear model of the phase-locked loop in order to decide the loop bandwidth, the phase margin, the phase noise, and the settling time in short time. The design and implementations of the frequency synthesizer are described in Chapter 5, including the

voltage-controlled oscillator, the frequency dividers, the phase frequency detector, the charge pump, the loop filter, and the single-sideband mixer. The layout, the testing setup, and measurement results of the voltage-controlled oscillator are also presented. The phase frequency detectors are also presented and the phase frequency detector with charge pumps in the package version. Chapter 6 gives the conclusions and the future works.

Chapter 2
Frequency Planning

There are many kinds of methods to synthesize frequencies. Such as direct synthesizers, indirect synthesizers (phase-locked loop frequency synthesizers), and direct digital frequency synthesizers. Because the phase-locked loop frequency synthesizer is easy to synthesize high frequencies and consumes low power, it is the most popular method used in high frequency synthesizers. In order to easily integrate in low-cost CMOS process and operate at high frequencies, we choose phase-locked loop synthesizer. There are many kinds of PLL frequency synthesizers changing division to synthesize various frequencies, such as integer-N, and fractional-N frequency synthesizers. However the time to switch between different band frequencies within a band group should be less than 9.47ns. The fast switching time precludes the use of a standard phase-locked loop (PLL)-based frequency synthesizer. Some possible ways of the performing the frequency generation in a UWB device are discussed in this section.

2.1 Architecture of UWB Frequency Synthesizer

In the UWB system, the frequency range is from 3.1-GHz to 10.6-GHz, and the carrier switching time must below 9.47ns. The specifications of the switching time and the spurs are difficult to meet. The frequency hopping time can not be satisfied with conventional PLL-based frequency synthesizers because the locking time of the phase-locked loop is several hundreds ns or several μs. In order to fast switch between bands, one approach incorporates some phase-locked loops and some single sideband mixers to synthesize different frequencies that present all time. The other approach incorporates multiple PLLs to generate different frequencies presented all times. The frequency range of the UWB system is very large, and the range covers the wireless LAN standard such as 802.11a. The reciprocal mixing effect can occur easily and degrade the wanted signal. In order to coexistent with other bands in 3-GHz~8-GHz, the suppression of the spurious must be concentrated. There are several kinds of UWB frequency synthesizer architectures and will be introduced in the following section.

2.1.1 State of the art 1 [3]

In [3], the UWB synthesizer shown in Figure 2.1 is designed to operate in “mode 1” bands. The frequency bands of mode 1 are 3432 MHz, 3960 MHz, and 4488 MHz. The three frequencies are produced by three fixed-modulus phase-locked loops,

therefore avoiding SSB mixers. The SSB mixer must have a low harmonic distortion, and the phase and gain mismatch can introduce spurious at the output of the SSB mixer. The output is changed between three voltage-controlled oscillators by the selector; therefore it may be sensitive to inductor coupling and carrier leakage. The architecture needs a good layout to provide good isolation. When the numbers of bands increases, the architecture will require more phase-locked loops, and it will increase the production cost and consume more power.

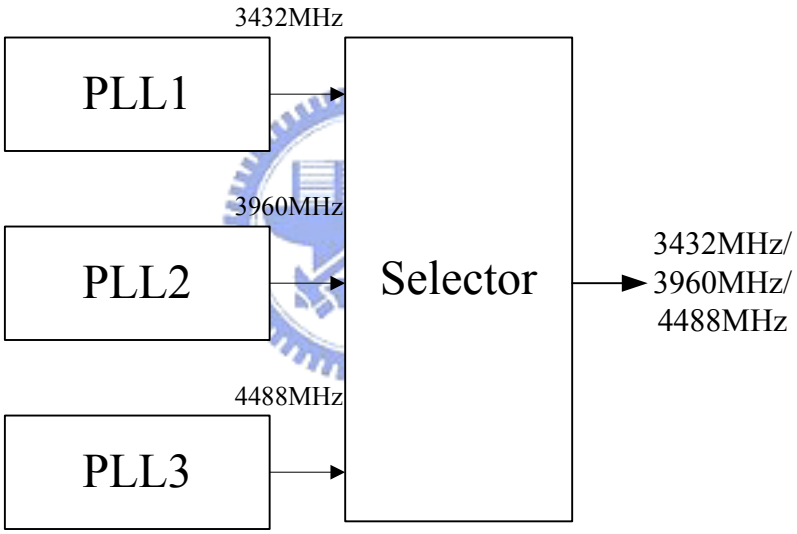


Figure 2.1 One band with one PLL frequency synthesizer

2.1.2 State of the art 2 [2]

In [2], there are two phase-locked loops in the architecture as shown in Figure 2.3. In the UWB center frequencies, some high band frequencies are twice as larger as the low band frequencies. The 6864-MHz, 7392-MHz, and 7920-MHz frequencies are generated by a VCO in the PLL, and the 3432-MHz, 3960-MHz, and 4488-MHz

frequencies can be generated by divde-by-2 circuits. Therefore they can share the same phase-locked loop. For example, In Figure 2.2, when the frequency synthesizer is turned on, PLL1 provides the frequency to the present band (3960-MHz), and PLL2 is switched to the next band (3432-MHz). They operate by turns. Because the symbol period is 312.5ns, the settling time of the PLL standby must be less than 312.5ns. This means the architecture needs a wide loop bandwidth to achieve fast settling time, and the reference spurious problem will be critical. The charge pump circuit must be designed carefully because it is critical to minimize the reference spurious.

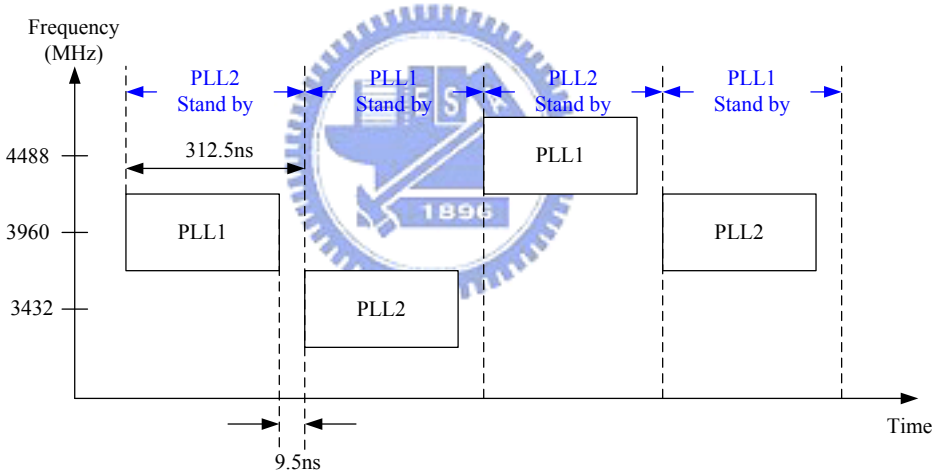


Figure 2.2 Frequency switching for each symbol of a MB-OFDM UWB burst

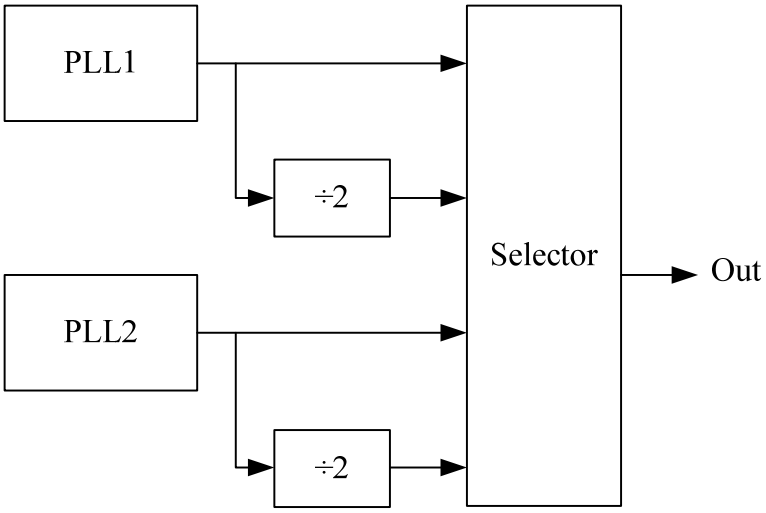


Figure 2.3 Two phase-locked loops frequency synthesizer

2.1.3 State of the art 3 [4]

An approach to synthesize all bands needed by single-sideband mixers and phase-locked loops is introduced in the following sections.

In [4], the architecture in Figure 2.4 uses two phase-locked loops to generate 3960-MHz and 528-MHz frequencies, then the single-sideband mixer spans the frequencies in band group one. Because the SSB mixer needs quadrature inputs, the quadrature signals are provided by the frequency divider circuit in the PLL. For example, in PLL1, it needs to provide quadrature signals at 3960MHz. Therefore the voltage-controlled oscillator needs to oscillate at 7920MHz, and the following divide-by-2 circuit (current mode logic architecture) can provide quadrature outputs at 3960MHz easily. The disadvantage is the spurs problem at the SSB mixer output.

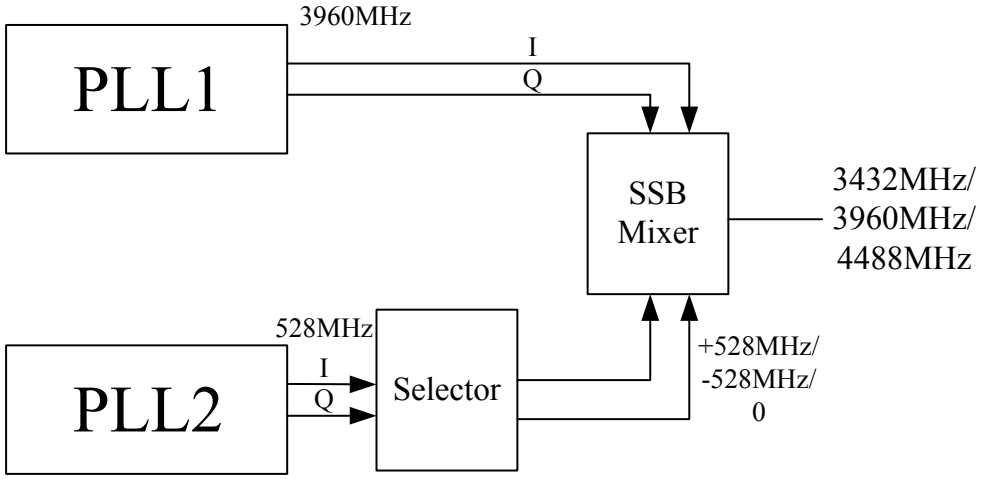


Figure 2.4 Two phase-locked loops and one SSB mixer frequency synthesizer

2.1.4 State of the art 4 [5]

In [5], two PLLs are used again, but in a different way to generate seven bands from 3-GHz to 8-GHz. In Figure 2.5, one phase-locked loop provides two frequencies for input signals of the output SSB mixer. And the programmable tri-mode divider placed in front of the SSB mixer has a DC, and quadrature signals with opposite I/Q sequences, therefore can provide more input signals for the SSB mixer. The SSB mixer has more selections of the input path. Therefore the frequences which the SSB mixer can synthesize will be more than the architecture in Figure 2.5. In order to suppress the spurious, the SSB mixer incorporates LC loads. The LC load acts as a band pass filter, and band switching is accomplished by using capacitor arrays to change the resonance frequency of the LC tank.

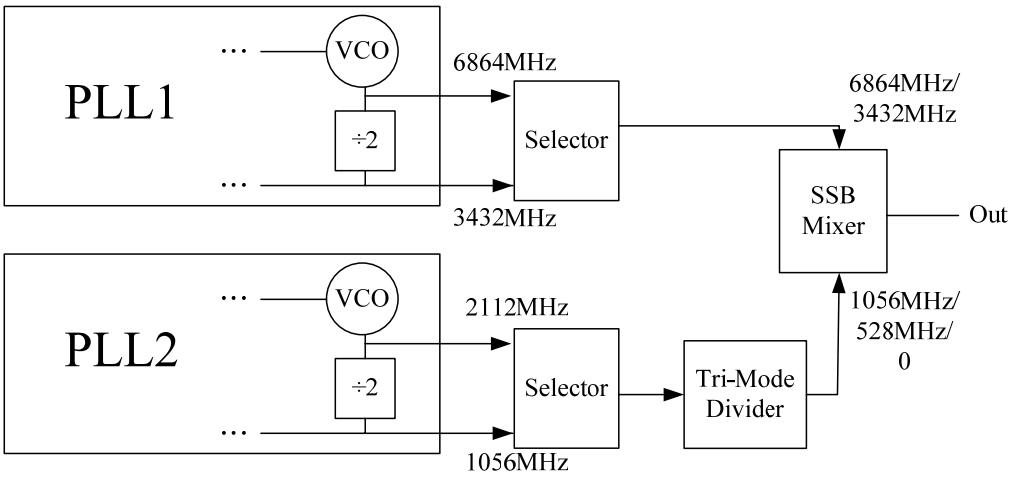


Figure 2.5 New two phase-locked loops and one SSB mixer frequency synthesizer

2.1.5 State of the art 5 [6]

In this year, a frequency synthesizer that generates twelve bands form 3.1-GHz to 9.5-GHz was presented. The frequency synthesizer consist SSB mixers and only one PLL. All the LO frequencies required for 3.1-GHz to 9.5-GHz operation are generated from the 8.448-GHz QVCO which consumes low power. A harmonic suppressing filter is inserted at the SSB1 mixer output terminal. The cut-off frequency of the filter is programmed according to the changing bands.

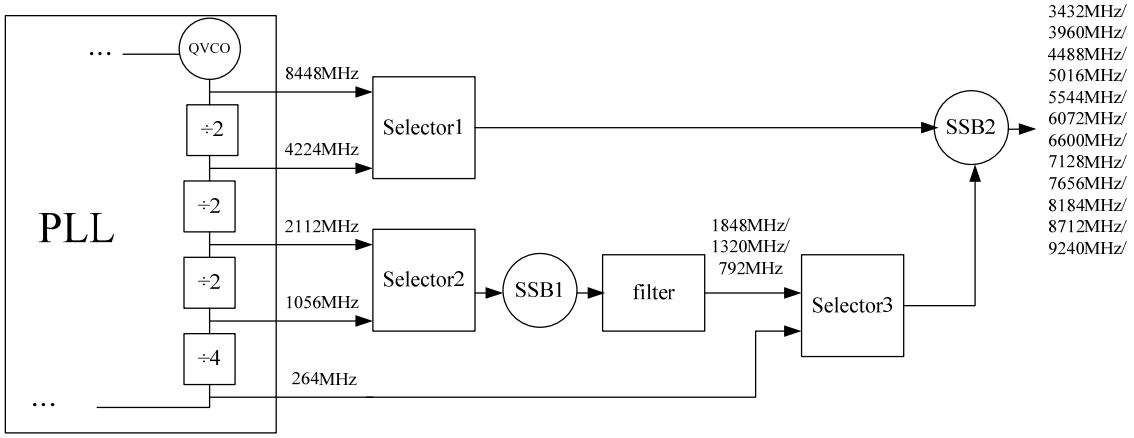


Figure 2.6 A 3.1-GHz to 9.5-GHz UWB frequency synthesizer

There are many kinds of architectures to implement the UWB frequency synthesizer. If the synthesizer architecture does not employ mixers, it required multiple PLLs, and therefore area and power consumption will be increased. The spurious problem is not serious because there is no mixer in the architecture. When the architecture applied to more bands, the carrier leakage problem will be more serious. If the synthesizer architecture consists of mixers, it required less PLLs, the area and power consumption are saved but more spurious will be introduced. The trade off must be made carefully to achieve fast switching time while not to increase area or power and to keep spurious minimized. In Table 2.1, the architecture consisting of mixers can synthesize more band frequencies and consume less power, but the spurious is higher than architecture without using mixers.

	Process (μm)	power (mW)	Spurious (dBc)	Phase noise (dBc/Hz)	@Offset (Hz)	Supply voltage (V)	Frequency range (GHz)	No. of bands	Architecture	Year
[3]	0.13 CMOS	45	-60(only one on)	-105	1M	1.5	3.4~4.5	3	PLL*3	2005 JSSC
[2]	0.18 CMOS	116.28	-52	-109.6	1M	1.8	3.4~7.9	7	PLL*2	2005 JSSC
[4]	0.25 SiGe	27	-35	-104	1M	2.7	3.4~4.5	3	PLL*2+SSB	2005 ISSCC
[5]	0.18 CMOS	48	-37	-103	1M	2.2	3.4~7.9	7	PLL*2+SSB	2005 ISSCC
[6]	0.09 CMOS	47	-20	-98	1M	1.1	3.4~9.2	12	PLL+SSB*2	2006 ISSCC

Table 2.1 The comparison of state of the art

2.2 Frequency Planning

In order to synthesize all band group of the UWB system, there are more intermediate frequency components generated, and more SSB mixers are required. Therefore, the unwanted sidebands are accumulated through multi-stage mixing. The output signal will be degraded because of the multi-stage mixing. So the synthesizer must have approaches to suppress spurious signal. For example, the SSB mixer incorporates band-pass loads to suppress sidebands and spurious sinals.

Because the switching time is 9.47ns, and in order to design a UWB frequency synthesizer which can synthesize all band group frequencies, SSB mixers should be used or it will be difficult to synthesize all band group frequencies with less PLLs. Using multiple PLLs will consume much power and die area. And the LO leakage problem will be worse. So the architecture consisting of SSB mixers is used. In order to reduce the number of phase-locked loops and have a lot of auxiliary frequencies provided for SSB mixers, the frequency of the voltage-controlled oscillator must be chosen carefully. Some possible approaches of the frequency generation in a UWB are discussed in [7]. To generate all band groups, there will be a lot of intermediate frequencies provided for SSB mixers. The intermediate frequencies can be provided by the dividers in the phase-locked loop or the mixers. Using the divider is better because quadrature outputs are easily obtained and no need for power and area wasting mixer

components. In order to have maximum possible intermediate frequencies from a fixed VCO frequency, the division ratio should be with small size such as 2 and 3.

528-MHz is the baseband clock signal in MB-OFDM UWB system. In Figure 2.7, the frequency tree shows the different possible VCO frequencies that can generate a 528-MHz tone by successive division by 2, 3, or both. The SSB mixer requires quadrature signal inputs, and the quadrature signals can be generated by the passive RC polyphase filters or current mode logics. It is not practical by using polyphase filters, because multiple ploypha se filters are required to cover all band groups and cost a lot of area. Aside from the problem, at high frequencies, the parasitic capacitances of the resistor are likely to make unacceptable errors in quadrature. In order to generate quadrature frequencies, the reliable way is by restricting all frequency division in the frequency synthesizer to current mode logic which can produce balanced quadrature outputs.

To sum up, in order to have more balanced quadrature intermediate frequencies by the phase-locked loop, choosing the VCO frequency as 8448-MHz and following the path enclosed by the dotted line (in Figure 2.7) is used in the proposed synthesizer design.

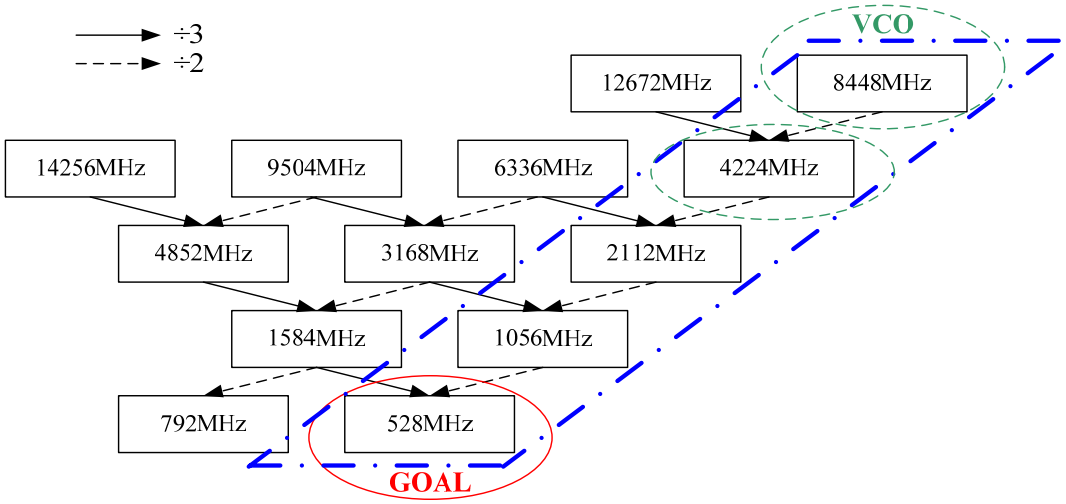


Figure 2.7 A frequency tree

The integer-N architecture is chosen in our phase-locked loop. Since the output signals of the frequency dividers are provided for SSB mixers, so they must be a fixed frequency values. The PLL can generate 8448-MHz and 4224-MHz frequencies. From [1], 8448-MHz and 4224-MHz are upper frequencies of the 3960-MHz and 8184-MHz channels. Now regard these two as the major frequencies and separate the UWB center frequencies into two parts as shown in Figure.2.8. One part is close to 4224-MHz and the other is close to 8448-MHz. In order to synthesize all band group frequencies, the offset frequencies such as 264, 792, 1320, and 1848-MHz are required.

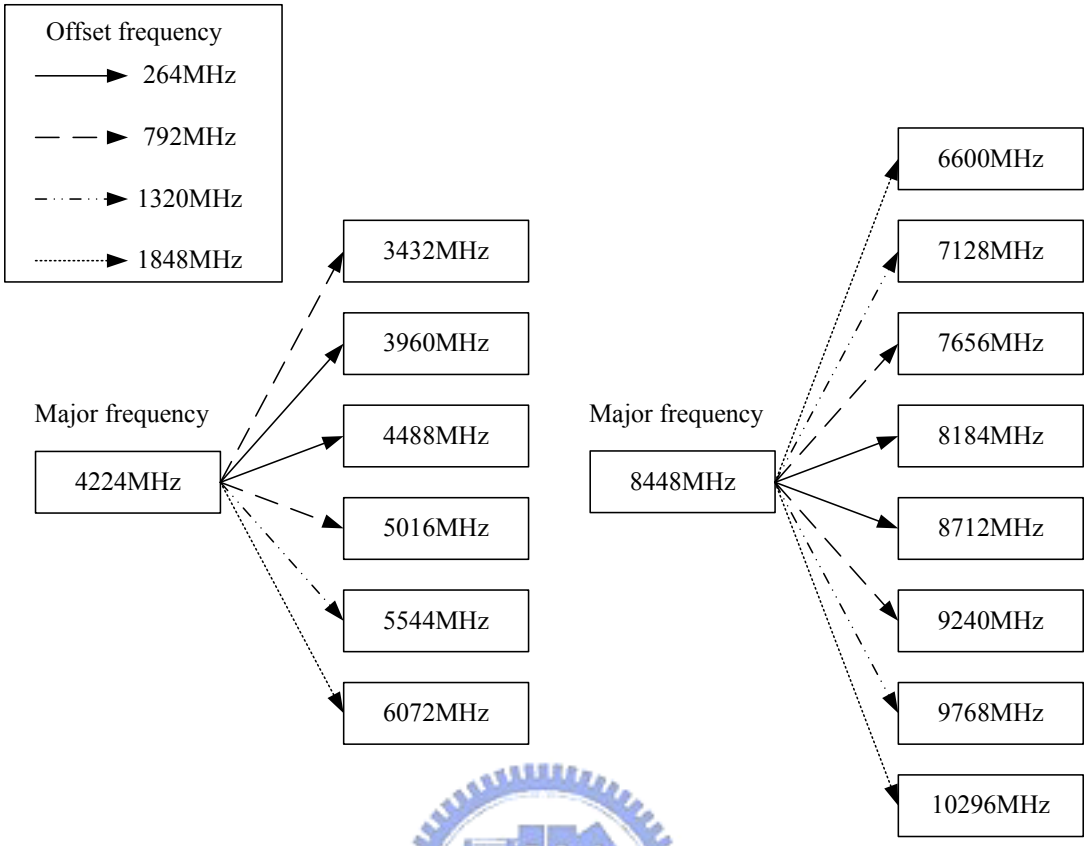


Figure 2.8 Two parts of the UWB frequency bands

Instead of direct mixing these frequencies, a divide-by-two circuit is inserted after the mixer because the division helps to suppress spurious signals [9]. In order to insert a divide-by-two circuit after the mixer, the offset frequencies must be doubled. Therefore 528, 1584, 2640, and 3696 MHz at the mixer output are required and 528 MHz is already generated in the PLL. Now the intermediate frequencies in the PLL are used to generate the doubled offset frequencies. The mixer output frequency 1584 MHz is generated by down-converting 2112 MHz with 528 MHz. (Note: both 2112 MHz and 528 MHz are generated in the PLL). In the similar way, 2640 and 3696 MHz can be acquired by up-converting 2112 MHz with 528 MHz and by down-converting 4224

MHz with 528 MHz respectively. In Fig. 3, the PLL can generate frequencies of 8448, 4224, 2112, 528, and 264 MHz. The SSB1 mixer output frequency is 1584, 2640, or 3696 MHz, and the offset frequencies can be acquired after the divider following the SSB1 mixer. Hence, the SSB2 mixer and the SSB3 mixer can generate all band group frequencies for UWB systems by the major frequencies (8448 and 4224 MHz) and the offset frequencies (264, 792, 1320, and 1848 MHz).

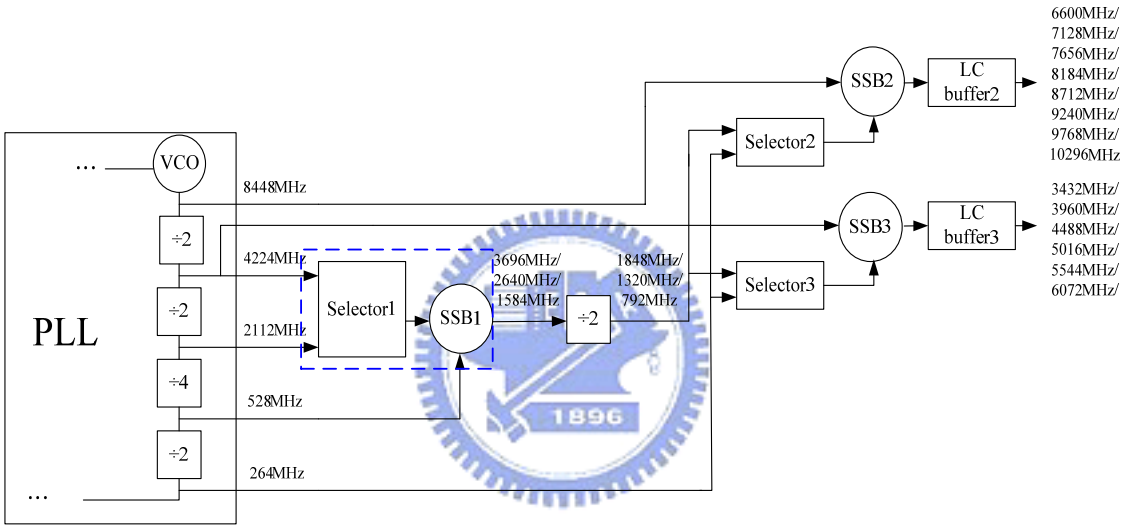


Figure 2.9 Architecture of this work

Chapter 3
Spurious Suppressing Techniques

Frequency spurious of the LO signal can down-convert in-band signals to the same frequency as the wanted band. To meet the specification on low LO spurs is much more difficult than the specification on low phase noise in the UWB system. Therefore to decrease the spurious in the UWB system is very important. This chapter will introduce some spurious suppressing techniques in this work.

3.1 Using Divide-By-2 Circuit After the Mixer

Literature [9], presented that the spurs after division-by-2 is lower than spurs before division-by-2. In Figure 3.1, consider two tones at ω1 and ω2 applied to the divide-by-2 circuit. ω1 is the wanted signal and ω2 is the unwanted spurious whose amplitude is A. The spurious tone $\omega2 = \omega1+\Delta\omega$ can be decomposed into equal amplitude modulation (AM) and phase modulated (PM) sidebands by linear superposition. Each of them is the same amplitude A/2, and they locate symmetrically $\Delta\omega$ away from ω1.

The flip-flop (the divide-by-2 circuit) is sensitive only to the threshold crossing of the input signals. (Note: Assume the differential threshold is zero) Therefore, the flip

flop only reacts to the input PM signals.

In Figure 3.2, the input PM signal is applied to the flip-flop. Whenever the differential clock input across zero, the flip-flop output toggles. The appearance is clear in the time-domain input and output waveforms. The output waveform tracks the input waveform whenever the input signal is at positive-slop trigger. The deviation is also tracked by the flip flop. However, the output frequency is half of the input frequency; the deviation in phase at output is half corresponding to the input signal. Therefore, the PM sidebands at output are half of the input PM sidebands at input. So the amplitude of the output PM sidebands are 0.25A. However, the rate or relative frequency of PM is still the same as before. Therefore, the sidebands are located at $\frac{\omega_1}{2} \pm \Delta\omega$.

To sum up, when large interesting input tones and small unwanted input spurs are applied to the to the divede-by-2 circuit, the large interesting input tones are divided by two, and each of the small unwanted input spurs is surrounded by two output spurs that are symmetrically disposed around the large tone at the same frequency offset as the single input spur but at 1/4 (-12 dB) the input spur's relation amplitude. (In Figure 3.3) More frequency division-by-2 conserves the spur separation but lowers the relative levels by 6 dB.

In an SSB mixer followed by frequency division, gain mismatch and phase errors in the I and Q mixers will generate a small unwanted spurs. This is the input of the

divider From above discussing, the divide-by-two circuit can help to suppress spurious.

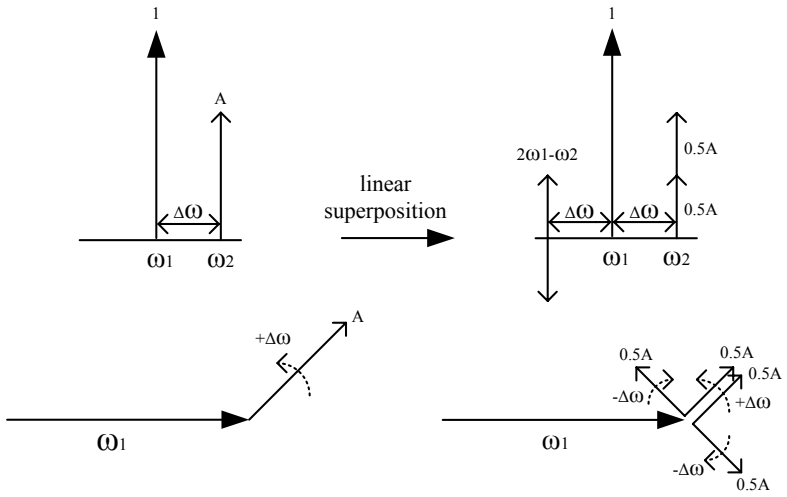


Figure 3.1 Decomposing a spur into equivalent AM and PM sidebands

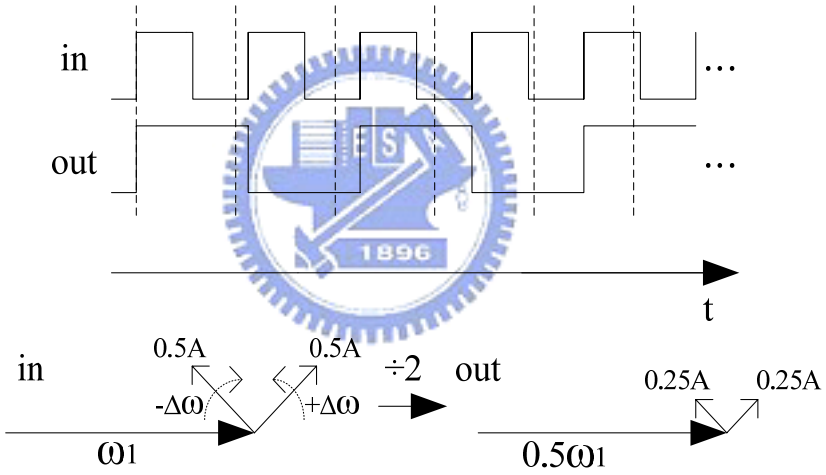


Figure 3.2 Output waveforms of a divide-by-2 circuit when PM signal is input

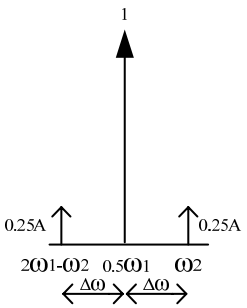


Figure 3.3 Output spectrum of divide-by-2 circuit

Figure 3.4, 3.5, and 3.6 respectively show the output spectrums of the 792-MHz, 1320-MHz, and 1848-MHz generated with and without the divide-by-two circuit. The dot line presents the output without divide-by-two circuit, and the solid line is for that with dive-by-two circuit.

Since the input frequencies of the mixer with and without divide-by-2 are different, the spurs at output are not at the same offset frequency away from carrier frequencies. But the spurious near the synthesized frequency with divide-by-two circuit is lower than that without divide-by-two circuit.

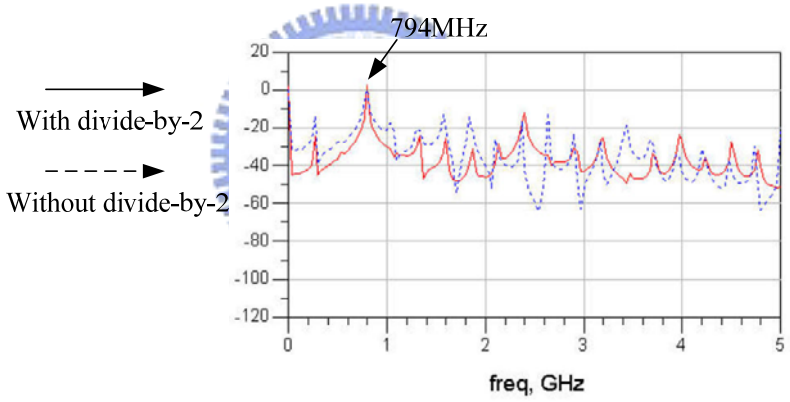


Figure 3.4 Frequency spectrums of 794-MHz

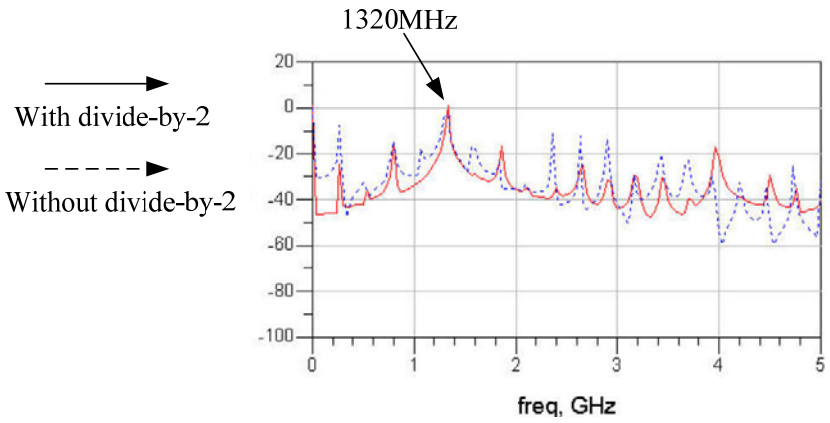


Figure 3.5 Frequency spectrums of 1320-MHz

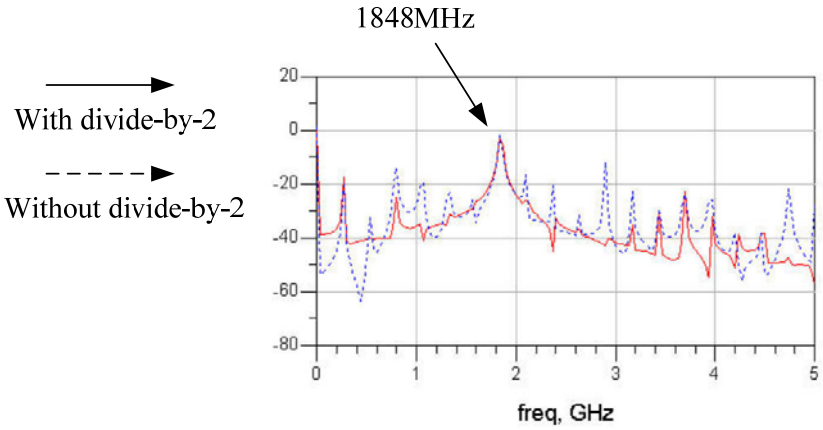


Figure 3.6 Frequency spectrums of 1848-MHz

3.2 Single-Sideband Mixer

Single-sideband mixers are employed in the proposed synthesizer. As shown in Figure 3.7, the relation between the output and the input of the mixer is in the following equation.

$$Out = \cos(\omega_1 t)\cos(\omega_2 t) \pm \sin(\omega_1 t)\sin(\omega_2 t) = \cos(\omega_1 \mp \omega_2)t \qquad (3.1)$$

Therefore, the architecture can make the unwanted sideband lower. But SSB mixers require quadrature inputs and arise two issues which are the mismatches between the quadrature inputs and the nonlinearities. A general way to quantifying the I/Q mismatch in a SSB mixer is to concern two signals $V_0 \sin\omega_I t$ and $V_0 \cos\omega_I t$ to the I and Q inputs and check the spectrum produced by the adder. In the ideal case, the SSB mixer output is shown as equation 3.2. In equation 3.3, ε is a gain mismatch, and θ is phase imbalance.

$$Out = V_0 \cos(\omega_1 t)\cos(\omega_2 t) + V_0 \sin(\omega_1 t)\sin(\omega_2 t) = V_0 \cos(\omega_2 - \omega_1)t \qquad (3.2)$$

$$Out = V_0(1+\varepsilon)\cos(\omega_1 t)\cos(\omega_2 t+\theta) + V_0\sin(\omega_1 t)\sin(\omega_2 t) \tag{3.3}$$

$$Out \approx \frac{V_0}{2}[1+(1+\varepsilon)\cos\theta]\cos(\omega_1-\omega_2)t - \frac{V_0}{2}(1+\varepsilon)\sin\theta\sin(\omega_2-\omega_1)t \tag{3.4}$$
$$+\frac{V_0}{2}[-1+(1+\varepsilon)\cos\theta]\cos(\omega_1+\omega_2)t - \frac{V_0}{2}(1+\varepsilon)\sin\theta\sin(\omega_2+\omega_1)t$$

The power of the sideband at $\omega_2+\omega_1$ divided by that of the sideband at $\omega_2-\omega_1$ is in the following equation.

$$\frac{P_{add}}{P_{sub}} \approx \frac{1-(1+\varepsilon)\cos\theta+\varepsilon}{1+(1+\varepsilon)\cos\theta+\varepsilon} \tag{3.5}$$

In practice, the cross-talk between the two data streams becomes negligible if the above test yields an unwanted sideband about 30dB below the wanted signal.

The mixers are usually designed such that the switching port experiences rapid switching. The switching port is so nonlinear that the RF signal is multiplied by a rectangular waveform. Therefore, in Figure 3.7, harmonics of ω_1 and ω_2 are generated in each port of the mixers, leading to various cross-products after multiplication. The problem will be mitigated by using LC tank. We will introduce in the next section.

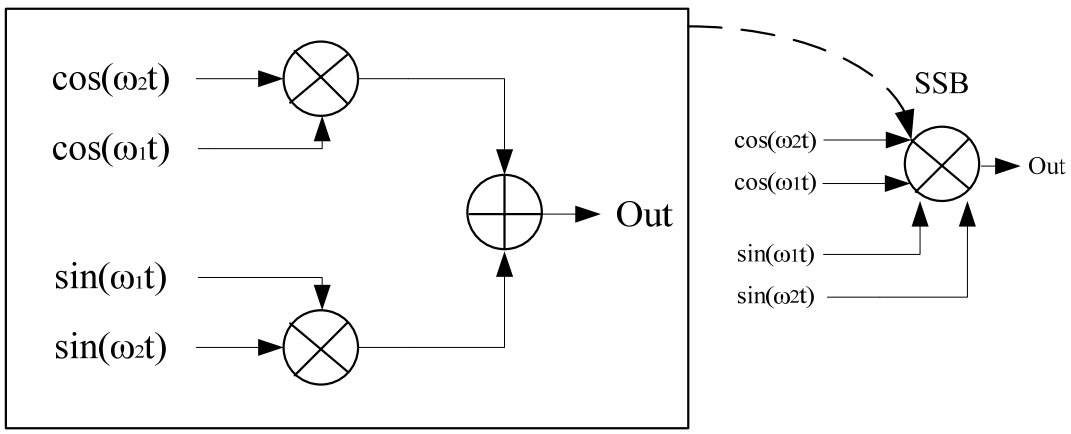


Figure 3.7 Ideal SSB mixing

3.3 LC Tank with Switching Inductor

The SSB mixer in Figure3.8 incorporates band pass loads to suppress spurious [5]. The SSB mixer with inductor loads are used to achieve broadband operation. Band selection is accomplished by adding capacitor arrays to adjust the resonances frequency of the tanks. The wide range operation (3-8GHz) of [5] uses multiple LC tanks. In order to extend the frequency range of the SSB mixer, more LC tanks are required leading more area expansion. However, with some modification on the LC tank, the area can be kept while the operation bandwidth can be improved.

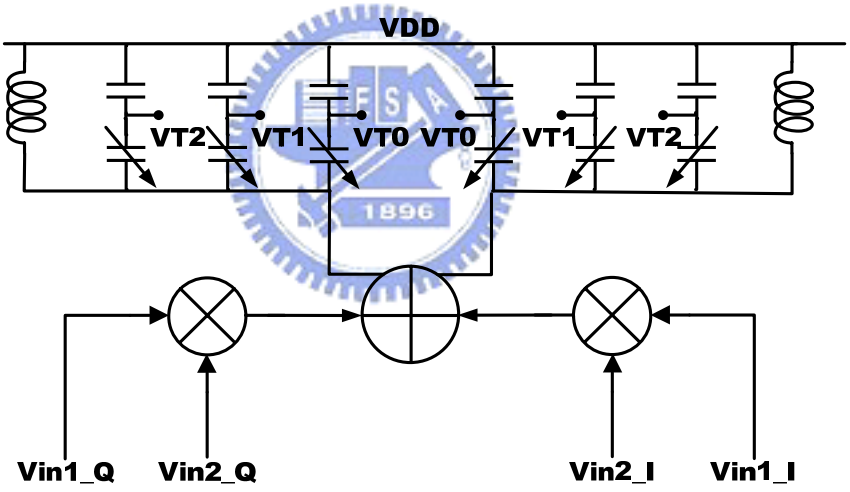


Figure 3.8 A SSB mixer with band pass loads

Changing the resonant frequency of the LC tanks is discussed in [10]. The maximum Q attainable is dominated by the on-chip inductor Q in low-cost CMOS process. Therefore, a restricted bandwidth is obtained at high frequency, and that is not enough for wideband applications. An easy way to raise the bandwidth is to decrease the Q of the tank, but this is unattractive in terms of the gain and the power consumption.

For LC tanks, the center frequency can be tuned either by inductors or capacitors. The most commonly used approach is to vary the parallel capacitors either by varactors or switched-capacitor arrays. However, since the tank impedance would be degraded with the increased capacitance, the tank impedance is lower at lower frequencies as compared to that at higher frequencies. As a result, either the output swing or the power consumption would need to be compromised.

As a better choice to varying the parallel capacitors, the tank inductance can be varied by employing MOS with the center taped inductors. As shown in Figure 3.9, there is a PMOS switch on the center of the inductor. When the voltage Vc is VDD, the PMOS switch is open, and the effective inductance is L. On the other side, when the voltage Vc is GND, the PMOS switch is turned on, and the effective inductance is about L/2.

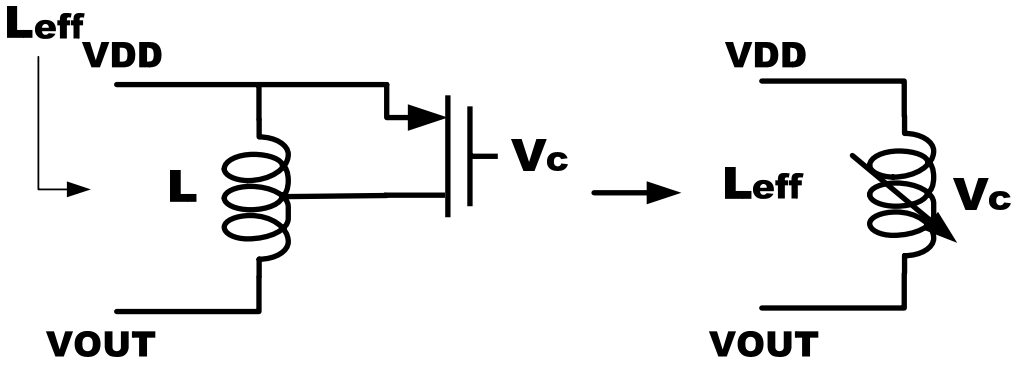


Figure 3.9 A switching inductor

We can use switching inductors to change the resonance frequencies of the LC tanks. In this way, we can avoid using large capacitance, and acquire higher impedance

and wider operation bandwidth.

Figure 3.10 shows the impedance of the LC tank with 5-bit capacitor arrays, while Figure 3.11 is the impedance of the LC tank with 3-bit capacitor arrays and 1-bit switching inductor. It is apparent that using switching inductor can operate wider frequency range and have higher and flat impedance.

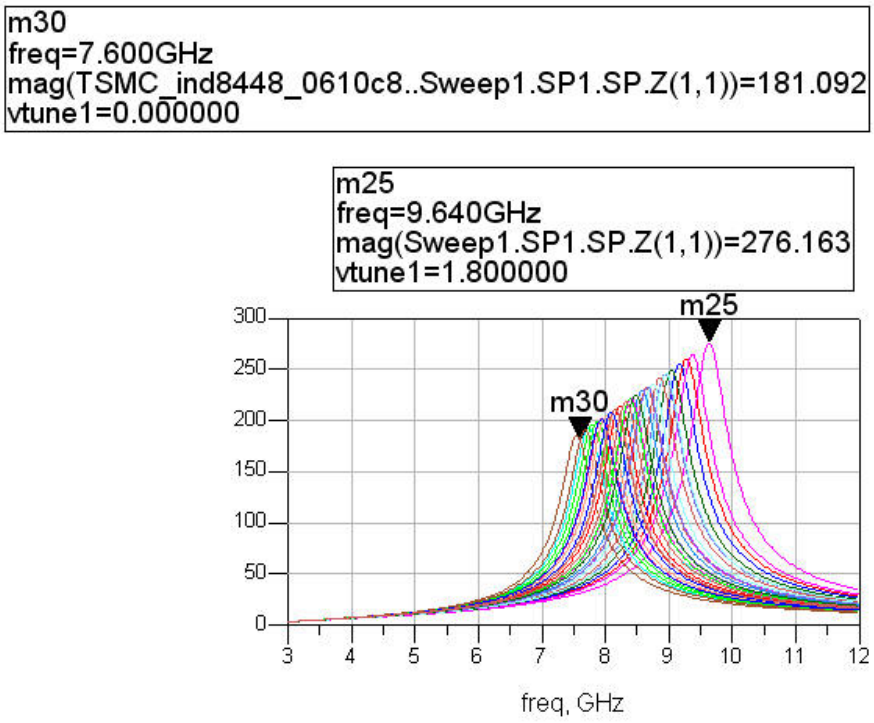


Figure 3.10 LC tanks with 5-bit capacitor arrays

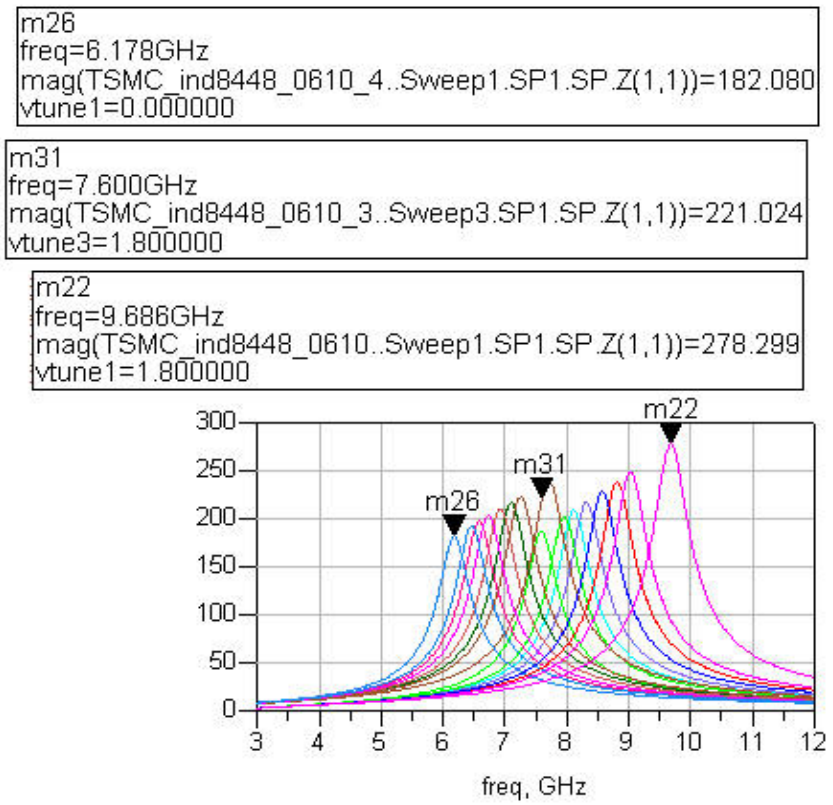


Figure 3.11 LC tanks with 3-bit capacitor arrays and 1-bit switching inductor

3.4 LC Tank with Negative resistance

To have a band-pass load which can operate all band groups in the UWB system requires a lot of capacitance arrays to change the resonance frequency More capacitance also means more parasitic resistances which degrade the quality factor of the LC tank. In order to have a high quality factor, a negative resistance is put in parallel in the LC tank. The architecture is shown in Figure 3.12. The negative resistance can compensate the parasitic resistance and increase the quality factor.

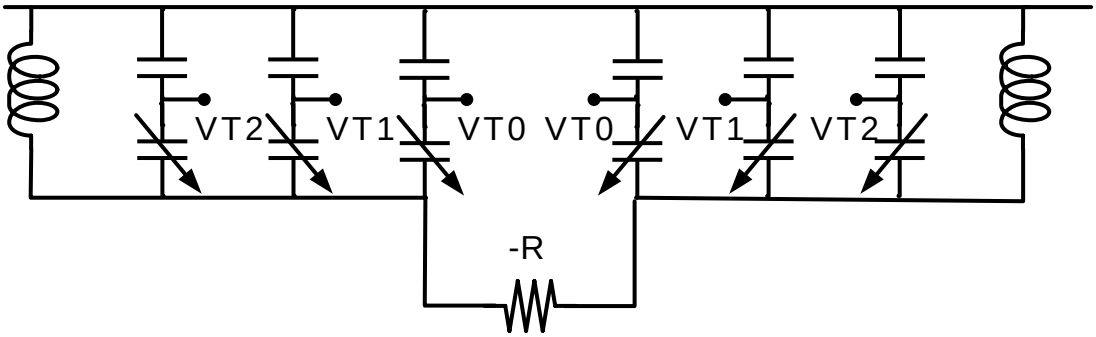


Figure 3.12 LC tanks with a negative resistance

Figure 3.13 and 3.14 show the impedance of the LC tank without and with negative resistance respectively. With the negative resistance, the resonant impedance is much higher.

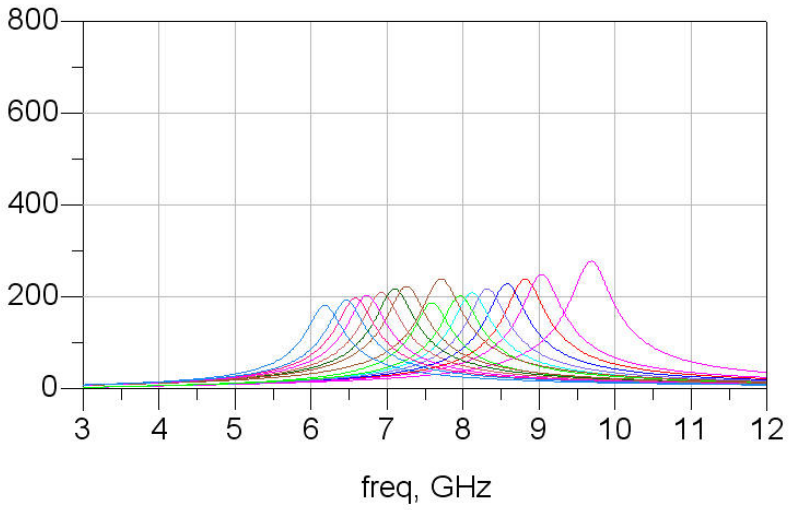


Figure 3.13 LC tanks without negative resistance

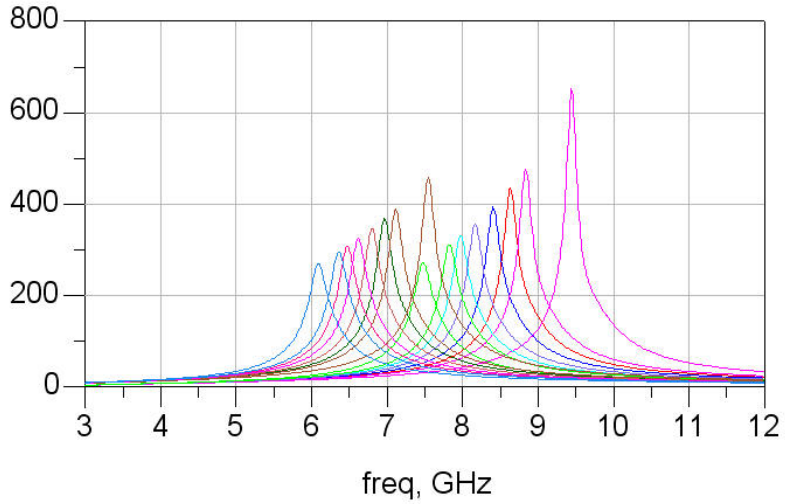


Figure 3.14 LC tanks with negative resistance

Figure 3.15, 3.16 show the output spectrums respectively when the frequency band is at 4488-MHz, 8712-MHz.

The circle solid line is the output spectrum of the last stage mixer. (SSB1 or SSB2 mixer in Figure 2.9) The star solid line and the solid line are the output spectrums of the LC buffer without and with negative resistance respectively. In Figure 3.15, spurious is suppressed 6.697dB more with using negative resistance than without using negative resistance, when the frequency band is at 4488-MHz. Similarly, when the frequency band is at 8712-MHz, it improves 7.152dB.

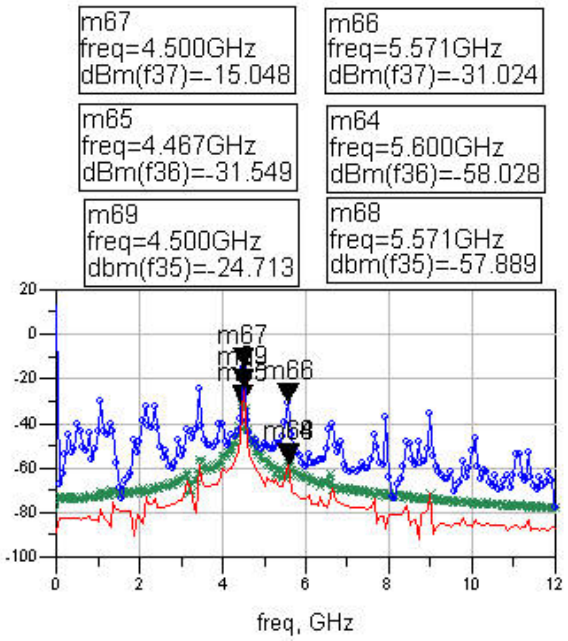


Figure 3.15 Output spectrums at 4488-MHz

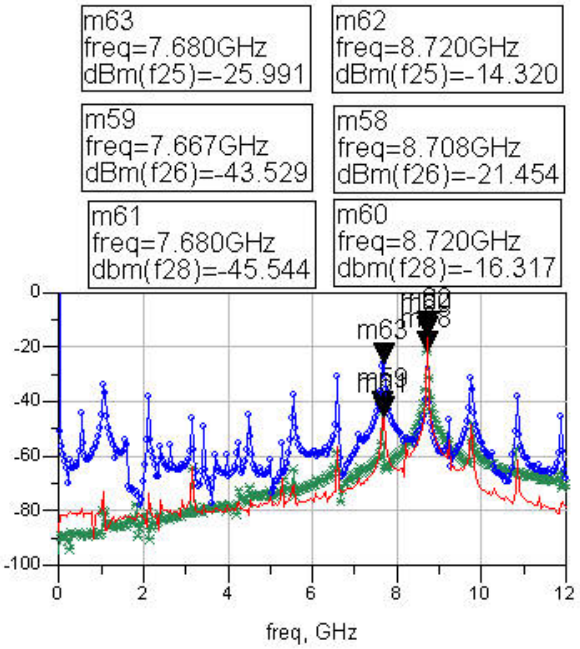


Figure 3.16 Output spectrums at 8712-MHz

Chapter 4
Frequency Synthesizer Design

4.1 Modeling of the PLL

Figure 4.1 is a linear model of a phase-locked loop. The model can help to evaluate the performance of the PLL, such as phase noise, loop stability, and settling time.

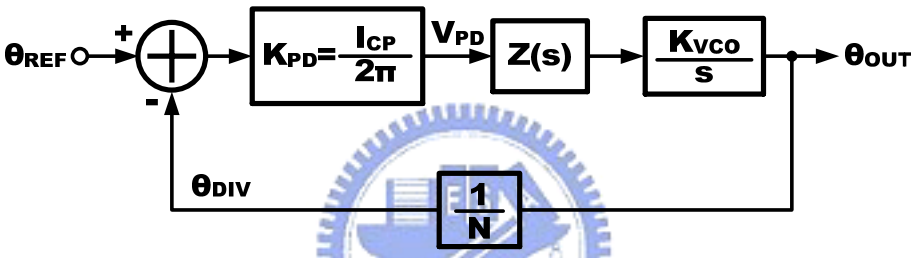


Figure 4.1 Linear model of a generic PLL.

The phase detector can generate a dc value proportional to the phase difference between the input reference signal θ_{REF} and the divided signal $\theta_{DIV.}$ K_{PD} is the phase detector gain in V/rad. The phase detector can be modeled as a substrator. Therefore, the output signal of the phase detector can be expressed by the following equation.

$$V_{PD} = K_{PD}(\theta_{REF} - \theta_{DIV}) \tag{4.1}$$

Although the phase detector gain K_{PD} is nonlinear, the transfer characteristic of the phase detector can be regarded as linear in its operating region. The phase error signal V_{PD} is filtered by the low pass loop filter. which is expressed by Z(s). For example, a second order passive loop filter has the transfer function:

$$Z(s) = \frac{(1 + s\tau_z)}{sC_i \cdot (1 + s\tau_p)} \tag{4.2}$$

The capacitance C_i contributes a pole at origin, τ_Z is a zero for stability concern, and τ_P is a pole for high-frequency spurs filtering.

The output frequency of the VCO is controlled by the voltage V_{CONT}. The relation between the changing frequency of the VCO and the control voltage is $\Delta\omega = K_{VCO} \cdot V_{CONT}$. K_{VCO} is the VCO gain (specified in rad/s/V) and it is nonlinear. Since frequency is derivative of phase, the VCO can be modeled by the following equation.

$$\theta_{OUT}(s) = \frac{K_{VCO} \cdot V_{CONT}(s)}{s} \tag{4.3}$$

Because frequency and phase are related by a linear operator, the division of frequency by a factor N is the same to the division of phase by the same factor. Hence, the frequency divider can be modeled by the following equation.

$$\theta_{DIV} = \frac{\theta_{OUT}}{N} \tag{4.4}$$

Based on the linear model of the PLL, the open loop transfer function can be expressed as follows:

$$G(s)H(s) = \frac{K_{PD} \cdot Z(s) \cdot K_{VCO}}{N} \cdot \frac{1}{s} \tag{4.5}$$

This transfer function can estimate the performance of the PLL.

4.1.1 Loop Stability

In Figure 4.1, because the phased-locked loop in this work employs the charge-pump circuit, the phase detector gain is determined by the charge pump output

current ($K_{PD}=I_{CP}/2\pi$).

The second order passive loop filter shown in Figure 4.2 consists of a capacitor C_Z for zero phase error, a resistor R_Z for stability consideration, and a capacitor C_P for high-frequency spurs filtering.

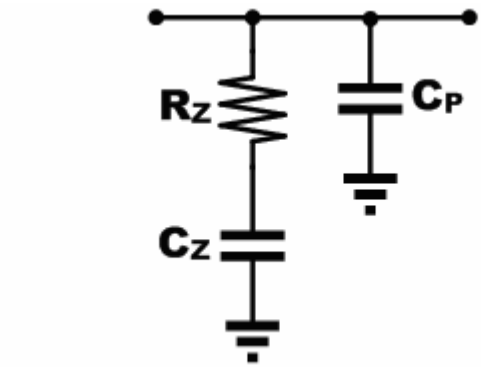


Figure 4.2 A second order passive loop filter.

The impedance of the second order passive loop filter is expressed as

$$Z(s)=\frac{1}{sC_P}//[R_z+\frac{1}{sC_z}]=\frac{\tau_p(1+s\tau_z)}{C_P\tau_z s(1+s\tau_p)} \tag{4.6}$$

The time constants τ_Z and τ_P are given by equation (4.7) and (4.8)

$$\tau_z = R_z \cdot C_z \tag{4.7}$$

$$\tau_p = R_z \cdot \frac{C_zC_p}{C_z+C_p} \tag{4.8}$$

The time constants determine the pole and zero frequencies of the loop filter. The open loop transfer function of the system can be expressed as the following equation.

$$G(s)\cdot H(s)=\frac{K_{PD}\cdot K_{VCO}\cdot \tau_p\cdot(1+s\tau_z)}{s^2\cdot C_p\cdot N\cdot \tau_z\cdot(1+s\tau_p)} \tag{4.9}$$

$$G(j\omega)\cdot H(j\omega)=-\frac{K_{PD}\cdot K_{VCO}\cdot \tau_p\cdot(1+j\omega\tau_z)}{\omega^2\cdot C_p\cdot N\cdot \tau_z\cdot(1+j\omega\tau_p)} \tag{4.10}$$

The phase margin is then given by the following equation.

$$\varphi(\omega) = -180 + \tan^{-1}(\omega \cdot \tau_z) - \tan^{-1}(\omega \cdot \tau_p) \tag{4.11}$$

$$PM = \varphi(\omega) - (-180) = \tan^{-1}(\omega \cdot \tau_z) - \tan^{-1}(\omega \cdot \tau_p) \tag{4.12}$$

The Bode plot of the open loop response is shown in Figure 4.3 where the loop bandwidth, ω_u, is defined as the corresponding frequency when the magnitude of the open loop gain equals one (i.e., unity-gain frequency). The phase margin is chosen between 50^o and 70^o.

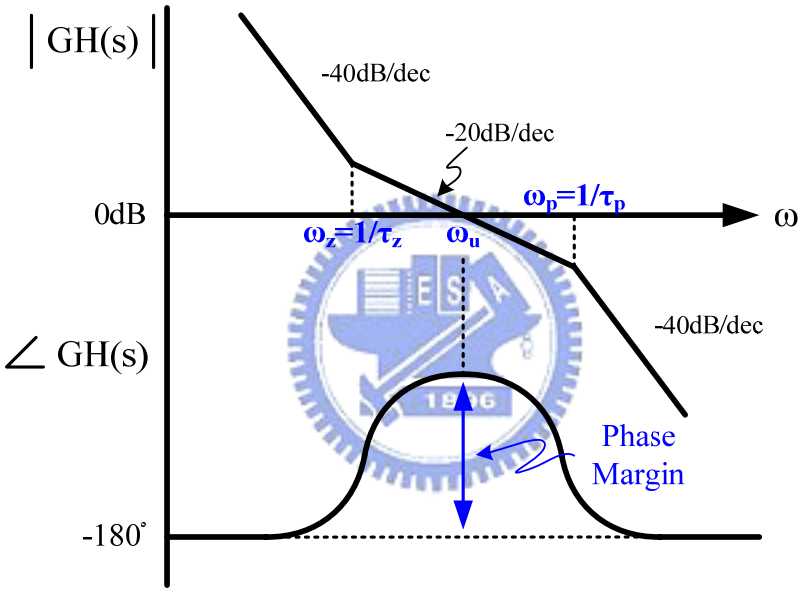


Figure 4.3 Open loop response bode plot.

By setting the derivative of the phase margin equal to zero, the frequency with the maximum phase margin is found, and it is expressed in terms of zero and pole as equation (4.14)

$$\frac{d\varphi(\omega)}{d\omega} = \frac{\tau_z}{1 + (\omega \cdot \tau_z)^2} - \frac{\tau_p}{1 + (\omega \cdot \tau_p)^2} = 0 \tag{4.13}$$

$$\omega_u = \frac{1}{\sqrt{\tau_z \cdot \tau_p}} = \sqrt{\omega_z \cdot \omega_p} \tag{4.14}$$

Consider that the maximum phase margin occurs at the unity-gain frequency,

$$|G(s)\cdot H(s)| = \frac{K_{PD}\cdot K_{VCO}\cdot \tau_p}{\omega_u{}^2\cdot C_p\cdot N\cdot \tau_z}\cdot\left|\frac{1+j\omega_u\tau_z}{1+j\omega_u\tau_p}\right| = 1 \tag{4.15}$$

$$C_p = \frac{K_{PD}\cdot K_{VCO}\cdot \tau_p}{\omega_u{}^2\cdot C_p\cdot N\cdot \tau_z}\cdot\sqrt{\frac{1+(\omega_u\tau_z)^2}{1+(\omega_u\tau_p)^2}} \tag{4.16}$$

The time constants, τ_Z and τ_P are expressed in terms of phase margin and loop bandwidth as follows

$$\tau_p = \frac{secPM - tanPM}{\omega_u} \tag{4.17}$$

$$\tau_z = \frac{1}{\omega_u{}^2\cdot\tau_p} \tag{4.18}$$

The component values of the second order filter are

$$C_P = \frac{K_{PD}\cdot K_{VCO}\cdot \tau_p}{\omega_u^2\cdot N\cdot \tau_z}\sqrt{\frac{1+(\omega_u\tau_z)^2}{1+(\omega_u\tau_p)^2}} \tag{4.19}$$

$$C_z = C_p\cdot\left(\frac{\tau_z}{\tau_p} - 1\right) \tag{4.20}$$

$$R_z = \frac{\tau_z}{C_z} \tag{4.21}$$

Table 4.1 summarizes the loop parameters of the phase-locked loop The VCO gain is 280 MHz/V. The charge pump current is about 210 μA. In this work, the loop bandwidth and the phase margin are chosen to be 300-kHz and 60° respectively. The values of the loop filter components are R_Z= 8.84 kΩ, C_Z= 224 pF, and C_P= 17.32 pF. The K_{VCO} of the VCO is from 180MHz/V to 450MHz/V. When *Kvco* is 180MHz/V, 300MHz/V, and 450MHz/V, the phase margins are 50 degrees, 60 degrees, 40 degrees. All of the phase margins are lower than 40 degrees.

Parameters	Value
Loop Bandwidth ω_u	300-kHz
Phase Margin φ_P	60^o
VCO Gain K_{VCO}	280 MHz/V
Charge Pump Current I_{CP}	210 μA
R_Z	8.84 kΩ
C_Z	224 pF
C_P	17.32 pF

Table 4.1 Summary of loop parameters.

4.1.2 Noise Characteristic of the PLL

In the PLL, there are two main noise sources which are from VCO and reference signals. The transfer function of the noise source from the VCO output is a high-pass characteristic. In the same way, the transfer function of the noise source from the reference clock input is a low-pass characteristic. That one or both noise sources are significant depends on the application of the phase-locked loop. Therefore, the optimum choice of the loop bandwidth in the PLL is important. In the wireless frequency synthesizer, due to the high quality of the crystal-based reference signal, the VCO phase noise dominates the noise. Therefore, it is desirable to make the loop bandwidth wider to suppress the VCO close-in phase noise.

Since the input reference of the phase-locked loop is crystal-based, phase noise contributions from the reference and frequency dividers are very low and negligible. Consider the phase noise contribution from the VCO, charge pump, and loop filter. The transfer function from noise sources to the output can be obtained by the linear PLL model. To derive the transfer function, the linear model of the PLL is shown in Figure 4.4.

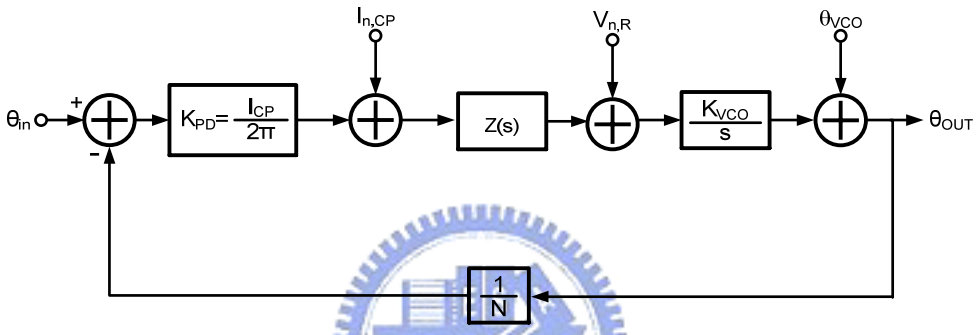


Figure 4.4 Linear model of the PLL with noise source

The transfer function from the input phase θ_{in} to the output phase θ_{out} can be expressed as the following equation, and is a low-pass function.

$$\frac{\theta_{out}}{\theta_{in}} = \frac{K_{PD} \cdot Z(s) \cdot \frac{K_{VCO}}{s}}{1 + \frac{K_{PD} \cdot Z(s) \cdot K_{VCO}}{N \cdot s}} \tag{4.22}$$

Therefore, the phase noise of the reference is attenuated at large frequency offset. (Note: The close-in phase noise of the reference signals is also amplified by the division ratio N of the divider)

The transfer function from the VCO noise $\theta_{n,VCO}$ to the output phase θ_{out} can be expressed as the following equation, and is a high-pass function.

$$\frac{\theta_{out}}{\theta_{vco}} = \frac{1}{1+\frac{K_{PD}\cdot Z(s)\cdot K_{VCO}}{N\cdot s}} \tag{4.23}$$

Hence, the far-offset phase noise of the PLL is dominated by the VCO phase noise.

The transfer function from the charge pump noise current $I_{n,CP}$ to the output phase θ_{out} can be expressed as the following equation, and is a low-pass function.

$$\frac{\theta_{out}}{I_{n,CP}} = \frac{Z(s)\cdot\frac{K_{VCO}}{s}}{1+\frac{K_{PD}\cdot Z(s)\cdot K_{VCO}}{N\cdot s}} \tag{4.24}$$

In the design of the loop filter, phase noise contribution due to the thermal noise of R_z is also an important issue. The transfer function can also be derived as the following equation, and is a band-pass function.

$$\frac{\theta_{out}}{V_{n,R}} = \frac{\frac{K_{VCO}}{s}}{1+\frac{K_{PD}\cdot Z(s)\cdot K_{VCO}}{N\cdot s}} \tag{4.25}$$

It is desirable to reduce the value of R_z and increase the value of C_z at the cost of large chip area for on-chip components.

4.1.3 Behavior Simulation of the PLL

The behavior and circuit (transistor level) simulations are performed in Advanced Design System (ADS). To verify the design of the loop filter in the previous section, the magnitude and phase response of both the open and closed loop are shown in Figure 4.5 where the loop bandwidth and phase margin of the phase-locked loop are 300-kHz and

60°, respectively.

Figure 4.5 Magnitude and phase response of the open and closed loop.

In the UWB system, the switching time is 9.47ns, and it is difficult to meet with traditional PLL-based synthesizer. In order to achieve fast switching time, mixers are employed in the synthesizers. Therefore, the settling time of the PLL does not need to be very fast. The behavior simulation of the PLL can help to check whether the PLL is locked or not. Figure 4.6 is the PLL simulation in time domain.

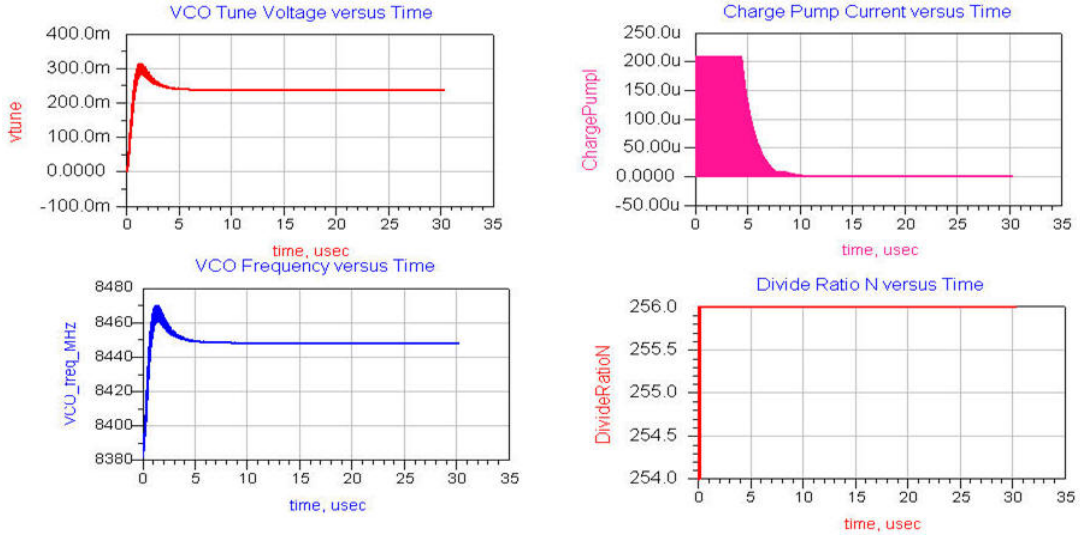


Figure 4.6 Settling time of the phase-locked loop

The simulated loop reductions of the VCO phase noise is shown in Figure 4.7. Since the transfer function from the VCO phase noise to the output phase noise

indicated in Equation (4.22) is a high-pass characteristic. The VCO phase noise is suppressed with the bandwidth of the loop. And the far-offset phase noise of the PLL is dominated by the VCO phase noise. On the other side, the short-offset phase noise of the PLL is dominated by the reference phase noise.

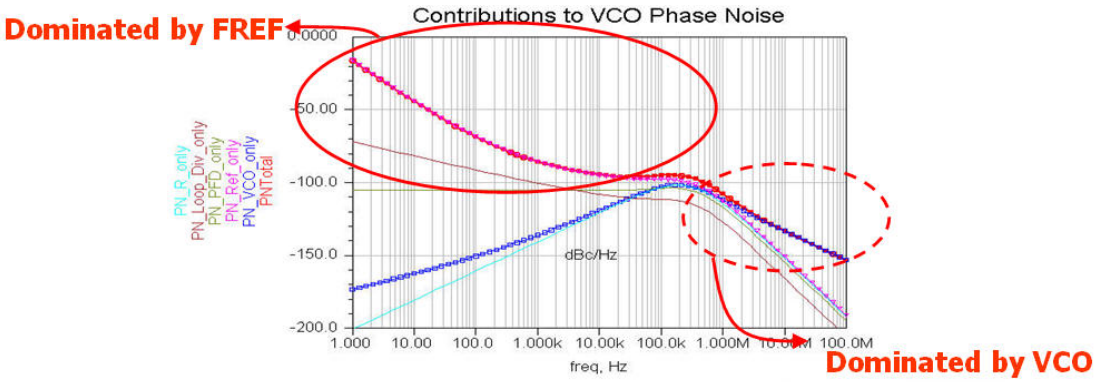


Figure 4.7 Simulated loop reductions of the VCO phase noise.

4.2 Circuit Design

4.2.1 Voltage-Controlled Oscillator

The voltage-controlled oscillator (VCO) is the most important building block of the frequency synthesizer. The design considerations are phase noise, tuning range, frequency pushing, frequency pulling, output power, and power consumption.

There are many kinds of oscillators, such as ring oscillators and LC oscillators. LC oscillators are the best choice for the wireless applications, because ring oscillators suffer from worse phase noise performance.

4.2.1.1 Phase Noise Theory

Figure 4.8 shows the Leeson's phase noise model [11] which is linear and time-invariant. (LTI)

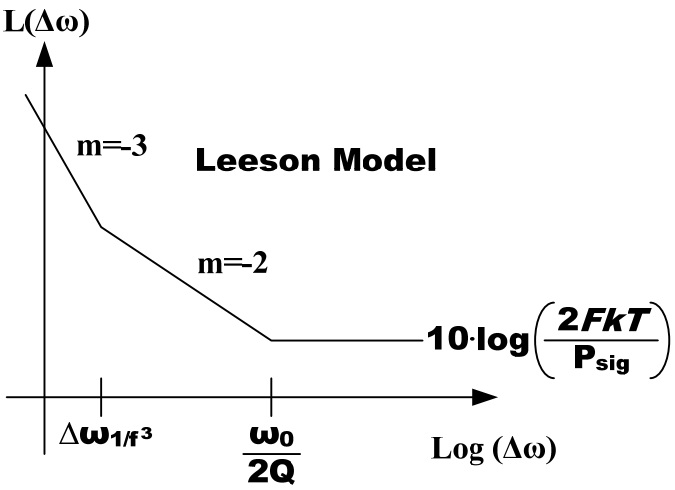


Figure 4.8 Leeson's phase noise model.

The model can be expressed in the following equation. (Note: P_{sig} is the signal power. Q is the quality factor of LC tank. F is an empirical factor to predict the increased noise in the $1/(\Delta\omega)^2$ region. $\Delta\omega_{1/f^3}$ is the corner frequency between $1/(\Delta\omega)^2$ region and $1/(\Delta\omega)^3$ region)

$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_{sig}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{4.26}$$

The Leeson's phase noise model shows that increasing the signal amplitude and quality factor of resonator can reduce phase noise.

The basic model [12] is shown in Figure 4.9 which can help to predict the phase noise. (R_p is the parasitic resistance. $\overline{I_{R_p}^2}$ is the current noise source of R_p Gm is an active to compensate the loss of the tank for steady oscillation.)

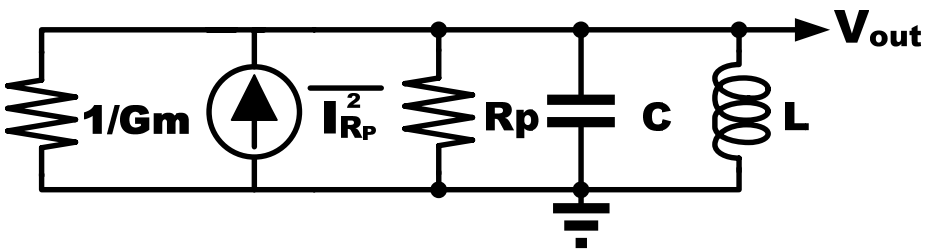


Figure 4.9 Basic model of oscillator circuit.

The transfer function from the current noise source $\overline{I_{R_p}^2}$ to the output voltage V_{out} can be derived and expressed as the following equation.

$$T_{noise}^2(s) = \frac{\overline{V_{out}^2}}{I_{Rp}^2}(s) = \left(\frac{sL}{1 - s(G_M - G_P) + s^2 LC}\right)^2 \tag{4.27}$$

G_p is the inverse of R_p. $H_{noise}(\omega)$ is the inverse of the noise transfer function. Consider the noise transfer function at a frequency offset $\omega_0+\Delta\omega$, $H_{noise}(\omega)$ can be expressed by Taylor series expansion around the center frequency.

$$H_{noise}(\omega_o + \Delta\omega) = \frac{1}{T_{noise}(\omega_o + \Delta\omega)} \approx H_{noise}(\omega_o) + \frac{dH_{noise}(\omega_o)}{d\omega}\Delta\omega \tag{4.28}$$

The first term $H_{noise,R_p}(\omega_o)$ is equal to zero and the second term is equal to

$$\frac{dH_{noise,R_p}(\omega_o)}{d\omega} \cdot \Delta\omega = \omega_o \cdot \frac{dH_{noise,R_p}(\omega_o)}{d\omega} \cdot \left(\frac{\Delta\omega}{\omega_o}\right) = 2j \cdot \sqrt{\frac{C}{L}} \cdot \left(\frac{\Delta\omega}{\omega_o}\right) \tag{4.29}$$

Then, the noise transfer function is given by

$$T_{noise,R_p}^2(s) \approx \left|\frac{1}{2j} \cdot \sqrt{\frac{L}{C}}\right|^2 \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 = \frac{1}{4 \cdot (\omega_o C)^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{4.30}$$

The noise density at a frequency offset $\omega_0+\Delta\omega$ is given by

$$\overline{V_{out,Rp}^2}(\omega_0 + \Delta\omega) = T_{noise}^2(\omega_0 + \Delta\omega) \cdot \overline{I_{Rp}^2} \approx kT \frac{1}{Rp(\omega_o C)^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot \Delta f \tag{4.31}$$

Note that the power needed to maintain the oscillation in the existence of R_p is

given by

$$G_{M,R_p} = \frac{1}{R_p} \tag{4.32}$$

The noise can be split up into a amplitude modulation (AM) and a phase modulation (PM). Therefore, the phase noise is typically half the value given by Equation (4.31).

The noise generated by inductor series resistance R_l and capacitor series resistance R_c can also be calculated. (Note: Series resistances must transfer to parallel resistances by the quality factor) The noise contribution of R_l and R_c can be expressed as follows

$$\overline{V_{out,Rl}^2}(\omega_0 + \Delta\omega) = kT \cdot Rl \cdot (\frac{\omega_o}{\Delta\omega})^2 \cdot \Delta f \tag{4.33}$$

$$\overline{V_{out,Rc}^2}(\omega_0 + \Delta\omega) = kT \cdot R_c \cdot (\frac{\omega_o}{\Delta\omega})^2 \cdot \Delta f \tag{4.34}$$

The power needed to maintain the oscillation in the existence of R_l or R_c are given by

$$G_{M,R_l} = R_l (\omega_o C)^2 \tag{4.35}$$

$$G_{M,R_c} = R_c (\omega_o C)^2 \tag{4.36}$$

The effective resistance is then defined for the evaluation of the LC oscillators. And the phase noise due to the parasitic resistances can be summarized as follows

$$R_{eff} = R_c + R_l + \frac{1}{R_p (\omega_o C)^2} \tag{4.37}$$

$$G_M = R_{eff} (\omega_o C)^2 \tag{4.38}$$

$$\overline{V_{vout,R}^2}(\omega_0 + \Delta\omega) = kT \cdot (Rl + Rc + \frac{1}{Rp(\omega_o C)}) \cdot (\frac{\omega_o}{\Delta\omega})^2 \cdot \Delta f = kT \cdot R_{eff} \cdot (\frac{\omega_o}{\Delta\omega})^2 \cdot \Delta f \tag{4.39}$$

The quality factor of the LC tank can also be expressed in terms of the effective resistance as follows

$$Q = \frac{1}{\frac{1}{Q_{R_p}} + \frac{1}{Q_{R_l}} + \frac{1}{Q_{R_c}}} = \frac{1}{\frac{1}{R_p(\omega_0 C)} + R_l(\omega_0 C) + R_c(\omega_0 C)} = \frac{1}{\mathrm{R}_{eff}(\omega_0 C)} \tag{4.40}$$

Similarly, the phase noise due to the active element can also be calculated. The current noise source of the active element is given by

$$\overline{I_n^2} = 4kT \cdot F \cdot G_M \cdot \Delta f \tag{4.41}$$

where G_M is given by Equation (4.38) and F is the noise factor of the amplifier. Since the noise source of the active element is the same as the noise source of the parallel resistance R_p. The noise transfer function is also given by Equation (4.30). Therefore, the phase noise due to the active element is expressed as follows

$$\overline{V_{out,G_M}^2}(\omega + \Delta\omega) = T_{noise,R_p}^2(\omega + \Delta\omega) \times \overline{I_n^2} \approx kT \cdot \frac{1}{(\omega_o C)^2} \cdot F \cdot G_M \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot \Delta f \tag{4.42}$$

$$\overline{V_{out,G_M}^2}(\omega + \Delta\omega) = kT \cdot R_{eff} \cdot F \cdot (\frac{\omega_o}{\Delta\omega})^2 \cdot \Delta f \tag{4.43}$$

In the design of an actual oscillator, the transconductance used in the circuit will be higher than theoretically needed. The transconductance must be higher than R_{eff} to provide enough negative resistance. By multiplying the noise with a factor α in the equations, the amount of noise which the actual amplifier generates in excess of the ideal amplifier is included. Define a factor A equal to $\alpha \cdot F$, Equation (4.43) becomes as follows

$$\overline{V_{out,G_M}^2}(\omega + \Delta\omega) = kT \cdot R_{eff} \cdot A \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot \Delta f \tag{4.44}$$

The total phase noise at the output can be expressed as

$$\overline{V_{out,G_M}^2}(\omega + \Delta\omega) = kT \cdot R_{eff} \cdot (1 + A) \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \cdot \Delta f \tag{4.45}$$

Hence, the single sideband noise spectral density is given by

$$L(\omega_0 + \Delta\omega) = \frac{1/2 \cdot kT \cdot R_{eff} \cdot [1 + A] \cdot (\frac{\omega_o}{\Delta\omega})^2}{V_{amplitude}^2 / 2} \tag{4.46}$$

Similar to the Leeson's model, increasing the signal amplitude (power) and decreasing the effective resistance can help to lower phase noise. Decreasing the effective resistance means to increase the quality factor of the LC tank. This model only predicts the phase noise of the oscillator in the $1/(\Delta\omega)^2$ region. The phase noise in the $1/(\Delta\omega)^3$ region can not be predicted in the model. A is an empirical factor. The phase noise of the oscillator in the $1/(\Delta\omega)^3$ region is mainly due to the upconversion of low-frequency $1/f$ noise. A time-varing model [13] is more accurate to calculate the phase noise in the $1/(\Delta\omega)^2$ and $1/(\Delta\omega)^3$ regions. The model discussed above is used to evaluate the phase noise.

4.2.1.2 Oscillator Topology

Figure 4.10 shows the circuit schematic of the voltage-controlled oscillator consisting of PMOS cross-coupled pairs, MOS varactors, fixed capacitance, a PMOS transistor providing a current source, and spiral inductors. The PMOS common-source amplifiers are used as output buffers for the measurement.

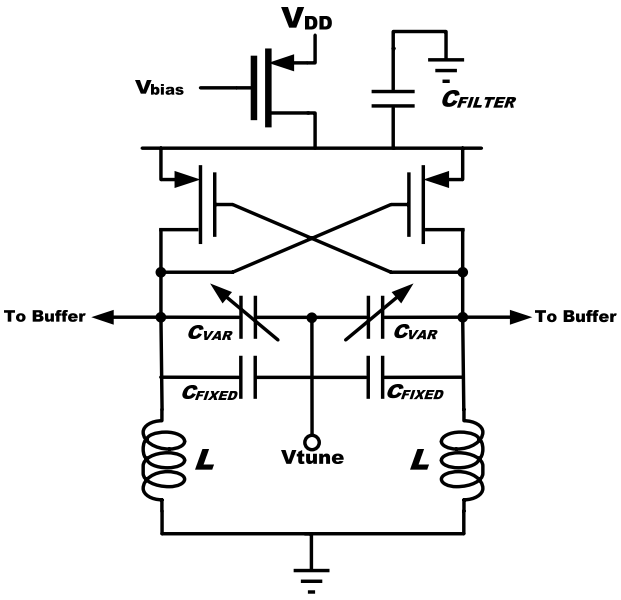


Figure 4.10 Circuit schematic of the VCO.

The tail current transistor is the largest contributor of the phase noise. The tail current noise is discussed in [14]. The switching action of the differential pair communicates noise in the tail currents like a single balanced mixer. Therefore the noise components of the tail current up-convert and down-convert to near the carrier frequency ω_0. The noise component of the tail current at ω_m up-converts to $\omega_0 \pm \omega_m$. Similarly, the noise at $2\omega_0 \pm \omega_m$ down-converts to $\omega_0 \pm \omega_m$. The two noise components can introduce phase noise. $1/f$ noise is one kind of the low frequency noise component at ω_m, and thermal noise is one kind of the high frequency noise component at $2\omega_0 \pm \omega_m$. There are several approaches to decrease tail current noise. In [15], the two distinct techniques which are inductor degeneration and capacitive filtering are applied to prevent the tail current noise from being converted into phase noise. Using a single capacitor parallel with the tail transistor can help reducing the corner frequency of the

up-converted *1/f* noise. *1/f* noise of the tail transistor can be reduced by making the tail transistor very large. Furthermore, because 1/*f* noise up-conversion is extremely dependent on the symmetry of the output waveform, it means that the output waveform must be half-wave symmetry to minimize 1/*f* noise up-conversion.

4.2.1.3 Varactor

The oscillation frequency is determined by the inductance and the capacitance. Therefore, the varactor characteristic determinates the frequency tuning range of the VCO. Since the junction capacitance provided by UMC018 is too large, the MOS varactor is used in the proposed VCO. In order to acquire the interesting frequency, the additional capacitance is put in parallel with the varactor.

Figure 4.11 shows the MOS varactor. Note that the source and drain of the PMOS transistor are connected with each other, and the bulk of the PMOS transistor is connected to VDD.

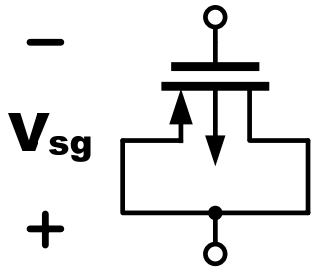


Figure 4.11 MOS varactor.

The C-V curve of the MOS varactor is shown in Figure 4.12, where the ratio of the maximum capacitance and minimum capacitance is about 2.4, i.e., $C_{max}/C_{min} \sim 2.4$.

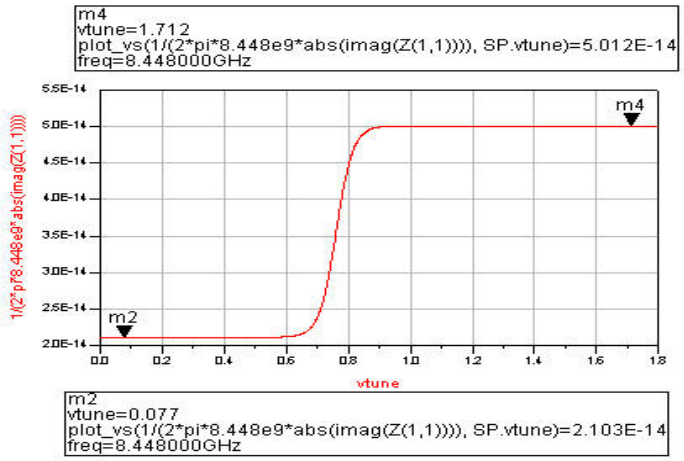


Figure 4.12 Tuning characteristic of the MOS varactor.

In Figure 4.13, our architecture uses a fixed capacitance parallel with the varactor.

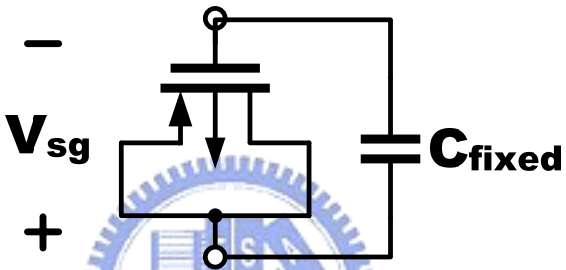


Figure 4.13 MOS varactor with fixed capacitance

The ratio maximum frequency of the oscillator to minimum frequency of the oscillator can be expressed by the following equation.

$$\frac{f_{\max}}{f_{\min}} = \sqrt{\frac{C_{\max} + C_{fixed}}{C_{\min} + C_{fixed}}} = \sqrt{\frac{333.4f}{304.5f}} = 1.046 \qquad (4.47)$$

Since the tuning ranging dose not require to be large, KVCO is very small.

Therefore, the phase noise will be better.

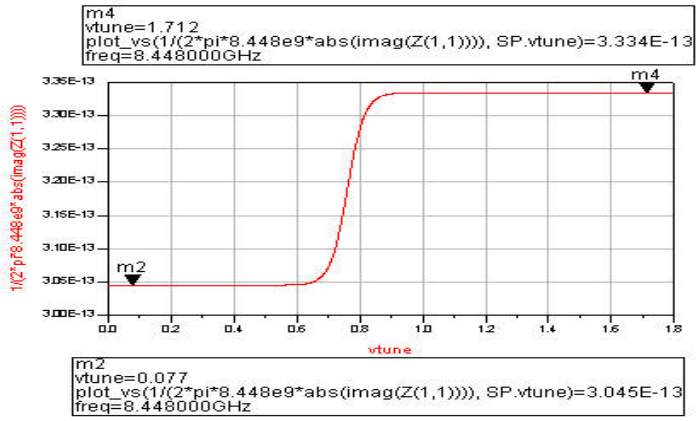


Figure 4.14 Tuning characteristic of the varactor with fixed capacitance

4.2.1.4 Design and Simulation

An oscillation amplitude of 1.06 $V_{diff,peak}$. Assuming F is 2.5 and α is 1.82, the calculated phase noise in the $1/(\Delta\omega)^2$ region is:

$$L(\omega+100k)=\frac{\frac{1}{2}\cdot kT\cdot 4.7\cdot[1+4.55]\cdot(\frac{8.448G}{100k})^2}{\frac{1.06^2}{2}}=-91.6dBc/Hz \tag{4.48}$$

$$L(\omega+1M)=\frac{\frac{1}{2}\cdot kT\cdot 4.7\cdot[1+4.55]\cdot(\frac{8.448G}{1M})^2}{\frac{1.06^2}{2}}=-111.6dBc/Hz \tag{4.49}$$

The simulated phase noise of the voltage-controlled oscillator is shown in Figure 4.15. The phase noise is -92.73 dBc/Hz at 100-kHz frequency offset and -116.2 dBc/Hz at 1-MHz frequency offset.

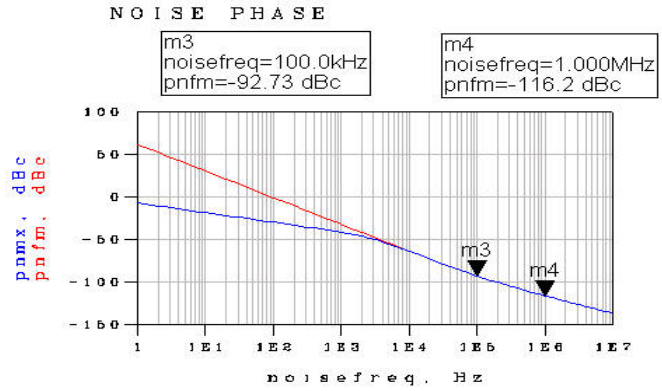


Figure 4.15 Simulated phase noise of the VCO.

The simulated tuning characteristic of the voltage-controlled oscillator is shown in Figure 4.16. The tuning range of the VCO is 200-MHz (2.37%). The desired frequency is from 8.448-GHz. The ratio of the maximum oscillation frequency to the minimum oscillation frequency can be obtained by the equation (4.47). Due to the parasitic capacitances, the ratio of the f_{max}/f_{min} is not equal to the ratio of the C_{max}/C_{min} in equation (4.47). It can be verified by using equation (4.50).

$$\frac{f_{max}}{f_{min}} = \frac{\dfrac{1}{2\pi\sqrt{L(C_{min}+C_{fixed}+C_p)}}}{\dfrac{1}{2\pi\sqrt{L(C_{max}+C_{fixed}+C_p)}}} = \sqrt{\frac{C_{max}+C_{fixed}+C_p}{C_{min}+C_{fixed}+C_P}} \qquad (4.50)$$

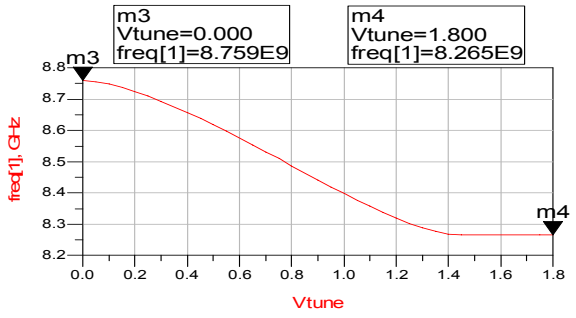


Figure 4.16 Simulated tuning characteristic of the VCO.

As shown in Figure 4.17, the output power versus the control voltage is about -0.72dBm.

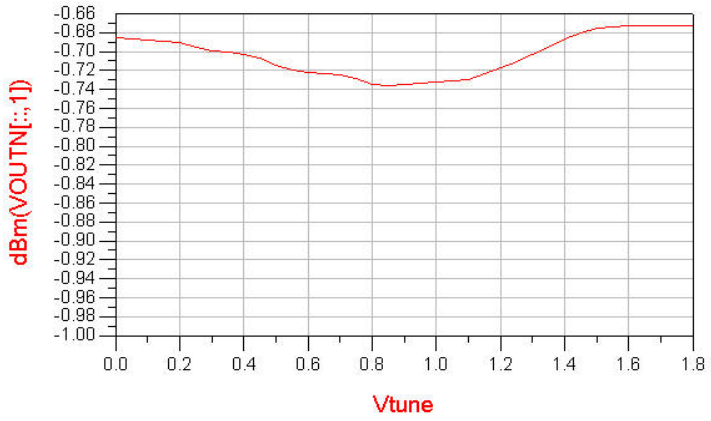


Figure 4.17 Output power versus the control voltage.

The power consumption of the VCO is 19.764mW. The simulated performance of the oscillator circuit is summarized in Table 4.2.

Parameters	Value
Phase Noise	-92.7 dBc/Hz at 100-kHz
	-116 dBc/Hz at 1-MHz
Tuning Range	494-MHz / (5.84%)
Output Power	-0.72 dBm
Power Consumption	11.7 mW (VCO core)
	19.76 mW (total)

Table 4.2 Simulated performance of the VCO circuit.

4.2.2 Quadrature Voltage-Controlled Oscillator

4.2.2.1 Oscillator Topology

There area many ways to generate quadrature signals, such as using the poly-phase filter, using the source current (SCL) logic after the VCO, and QVCO. The poly-phase filter consumes much power and needs a lot of area acquire accurate quadrature signals. Therefore, consider of the cost, the poly-phase filter is not adaptive. Using the SCL to generate the quadrature signals can save area. Since the oscillation frequency of the VCO is twice of the original operating frequency, the inductor and the capacitor are much smaller. But a VCO and a divider operated over 10-GHz are difficult. Therefore, the proposed architecture is QVCO, but the area of the QVCO is twice of the VCO.

In Figure 4.18, the VCO circuit is coupled by differential pair transistors (M1and M2) from outside. The transistors (M_1 and M_2) transform the voltage of Vin signal to the current. Since the Vin affects the total current (Id_1+Id_3 and Id_2+Id_4) at output, the phase of the output change in the coupling process.

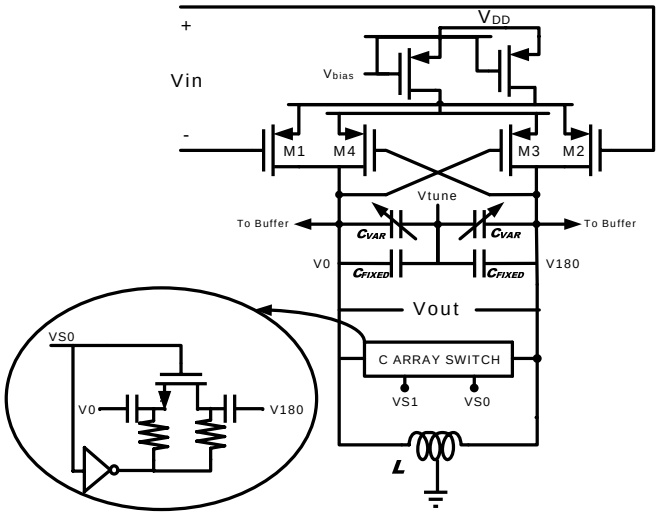


Figure 4.18 Couple to the VCO

Figure 4.19 shows a small signal model of Figure 4.18 Gm is the transconductance of M1 and M2. Rp is the impedance of the LC tank. The negative resistance is –R provided by the cross coupled pair.

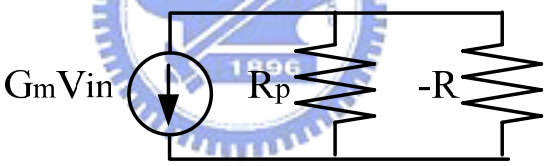


Figure 4.19 Small signal model of Figure 4.18

Figure 4.20 shows the small signal of the QVCO. The small signal model can be derived the following equation.

$$G_{m1} \cdot V_{in1} \cdot \frac{-R \cdot R_p}{R_p - R} = V_{in2} \tag{4.51}$$

$$G_{m2} \cdot V_{in2} \cdot \frac{-R \cdot R_p}{R_p - R} = V_{in1} \tag{4.52}$$

Assume V_{in1} and V_{in2} are not zero, the following equation can derive by equation (4.51) and (4.52)

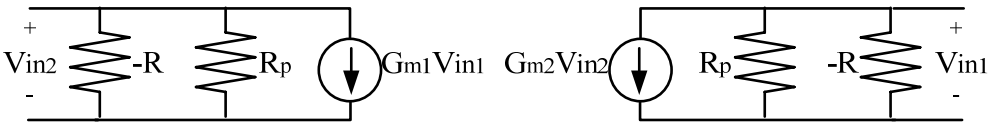


Figure 4.20 Small signal model of QVCO

$$G_{m1} \cdot V_{in1}^2 - G_{m2} \cdot V_{in2}^2 = 0 \tag{4.53}$$

If $G_{m1} = G_{m2}$, $V_{in1} = \pm V_{in2}$ can be derived by equation (4.53), and the effect is called "In-phase coupling." The two VCO operate at 0° and 180° respectively. If $G_{m1} = -G_{m2}$, $V_{in1} = \pm jV_{in2}$ can be derived by equation (4.53) and the effect is called "Anti-phase coupling." The two VCO operate at 90° and -90° respectively. Therefore the QVCO is anti-phase coupling circuit and can generate quadrature signals. Figure 4.21 shows the schematic in this work. The QVCO includes the capacitor arrays to overcome the problem of the process variation. The coarse tuning of the oscillation frequency is operated by 2-bit digital controlling signal, and the fine tuning of the oscillation frequency is operated by the controlled voltage.

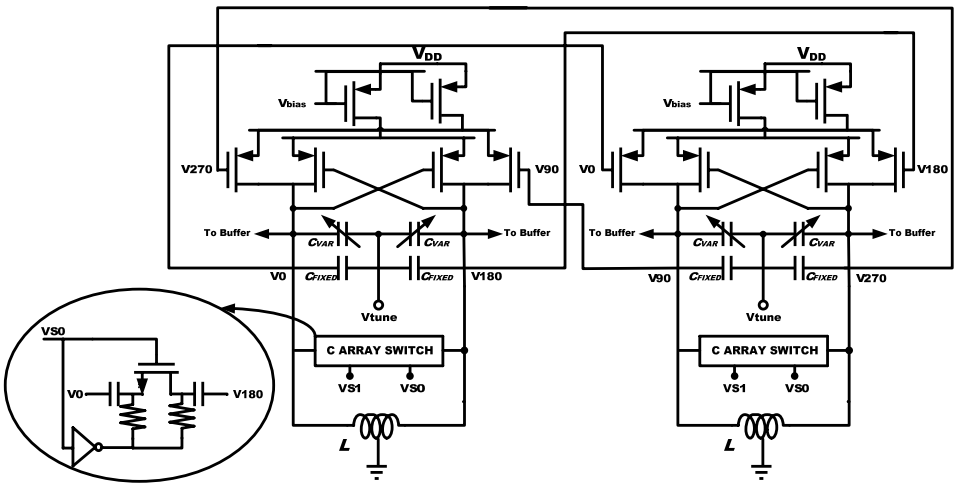


Figure 4.21 The QVCO in this work

4.2.2.2 Simulation Results

The tuning range of the QVCO is from 7.897-GHz to 8.982-GHz and is shown in Figure 4.22.

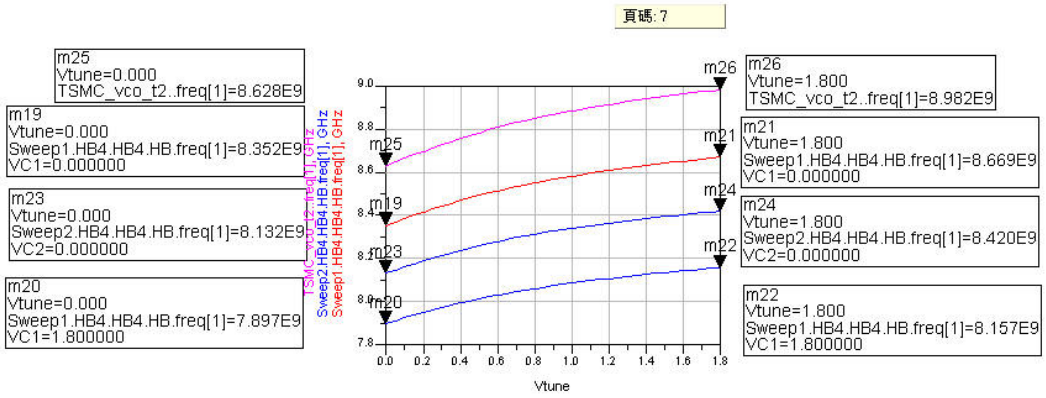


Figure 4.22 The tuning range of the QVCO

When the tuning voltage changes from 0V to 1.8V, the phase noise is shown in Figure 4.23 is lower than -95 dBc/Hz at 100-kHz frequency offset. Figure 4.24 shows the quadrature output of the QVCO.

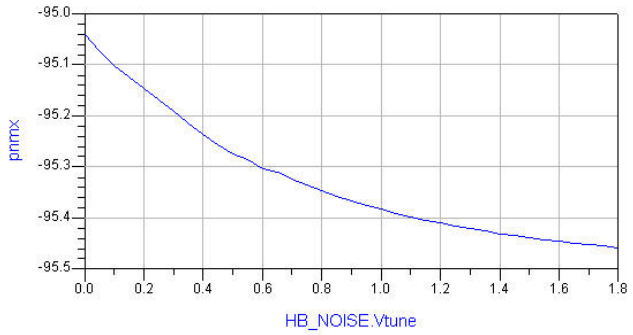


Figure 4.23 The phase noise of the QVCO

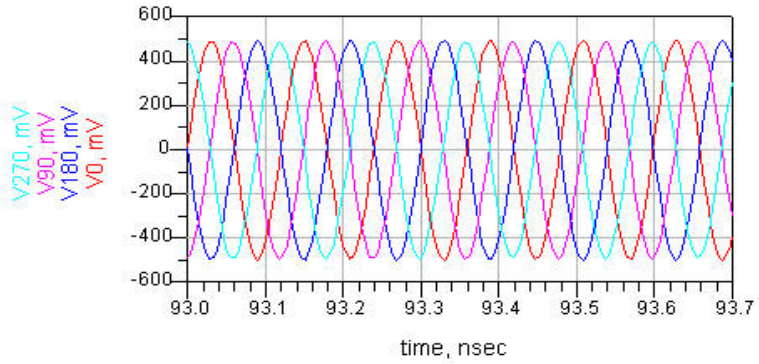


Figure 4.24 The quadrature output signals of QVCO

The simulated performance of the quadrature oscillator circuit is summarized in Table 4.3

Parameters	Value
Phase Noise	-95 dBc/Hz at 100-kHz
Tuning Range	1085-MHz / (12.8%)
Power Consumption	18.25 mW (QVCO core)
	54.87 mW (total)

Table 4.3 Simulated performance of the QVCO circuit.

4.2.3 Frequency Divider

For high-speed applications, the high-frequency divide-by-two circuit is realized by using Source-Coupled Logic (SCL).

4.2.3.1 Source-Coupled Logic (SCL)

As shown in Figure 4.25, a divide-by-two circuit consists of two latches in a negative feedback loop. Each of the latches is implemented by utilizing the source-coupled logic configuration.

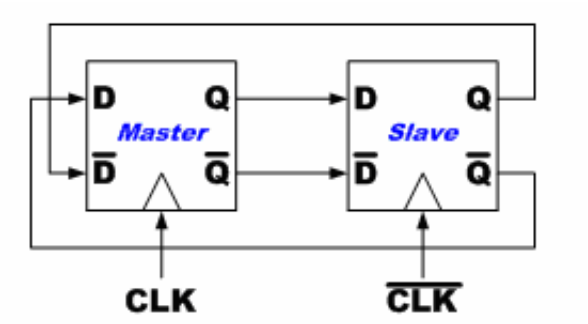


Figure 4.25 Block diagram of the divide-by-two circuit.

Figure 4.26 shows a typical source-coupled latch. The SCL consists of an input sampling pair M_3-M_4 and a regenerative pair M_5-M_6 with loading devices. In the sampling mode, the clock signal is high and the input sampling pair M_3-M_4 is active to sense the value at the input. In the regeneration mode, the cross-coupled pair M_5-M_6 forms a positive feedback loop. The operating speed is dominated by the RC time constant at the output node and the transconductance of the regenerative pair.

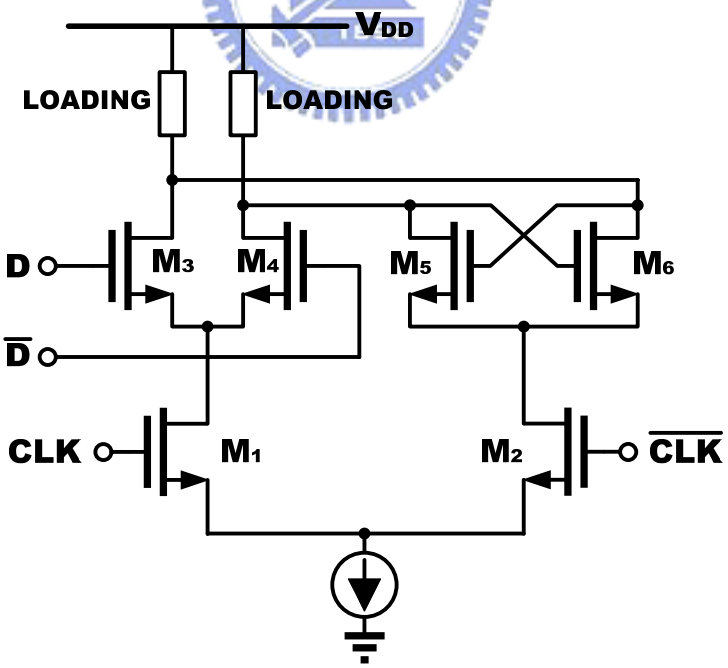


Figure 4.26 Typical D-latch using source-coupled configuration.

The internal voltage swing should be kept as small as possible to increase the operating speed of the frequency divider. Therefore, the time required for toggling the logic state is shorter. Increasing the current source and the supply voltage are helpful to increase the operating speed, but the power consumption will increase.

As shown in Figure 4.27 [16], in order to operate at low supply voltage, the current source is omitted in conventional SCL architecture. PMOS transistors operating in the linear region is regarded as the load of the SCL.

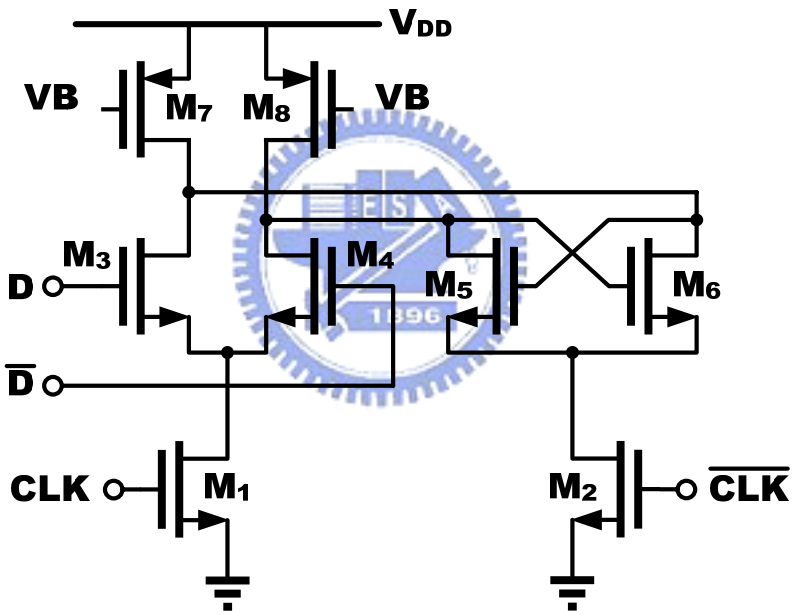


Figure 4.27 Circuit schematic of the D-latch.

Figure 4.28 shows the transient simulation result of the divide-by-2 circuit. Figure 4.29 shows the output frequency spectrum of the divide-by-2 circuit The input signal having a frequency of 8.448-GHz is applied to the input of the divider.

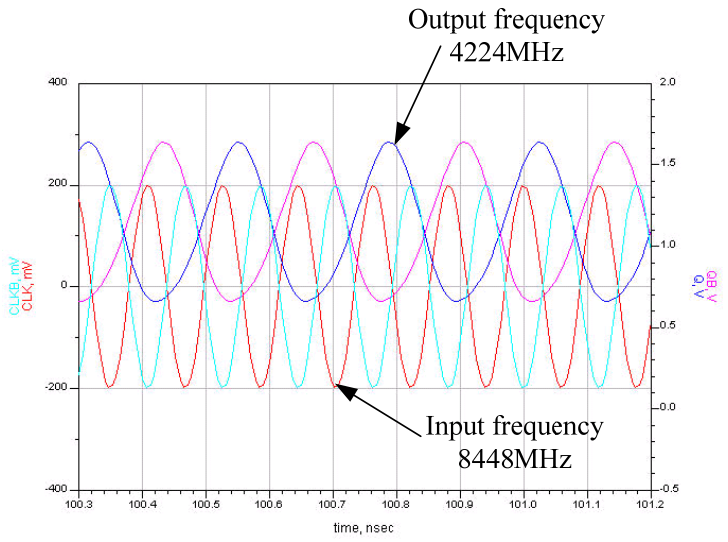


Figure 4.28 Transient simulation result of the divide-by-2 circuit

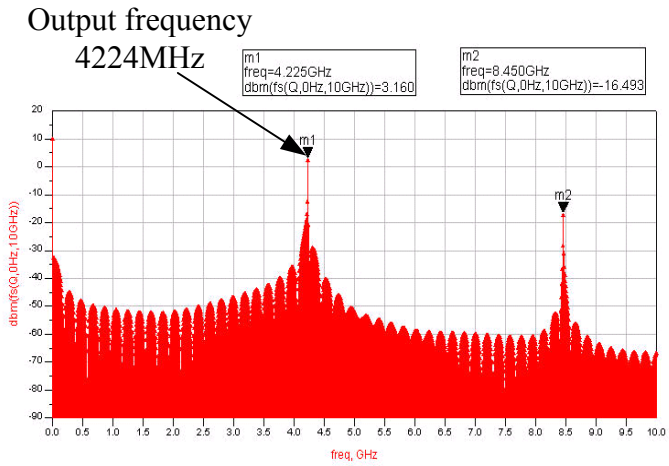


Figure 4.29 The output .frequency spectrum of the divide-by-2 circuit

4.2.4 Phase-Frequency Detector

The phase-frequency detector (PFD) compares the phase between the reference signal and the divided signal and produces the corresponding output signal containing information of phase difference.

Figure 4.30 shows the block diagram of the phase-frequency detector. The PFD consists of two resettable edge-triggered D flip-flops and one AND gate. Using edge-triggered D flip-flop makes the circuit avoid dependence of the output upon the

duty cycle of the inputs. The static CMOS logic is used for the implementation of the resettable edge-triggered D flip-flops.

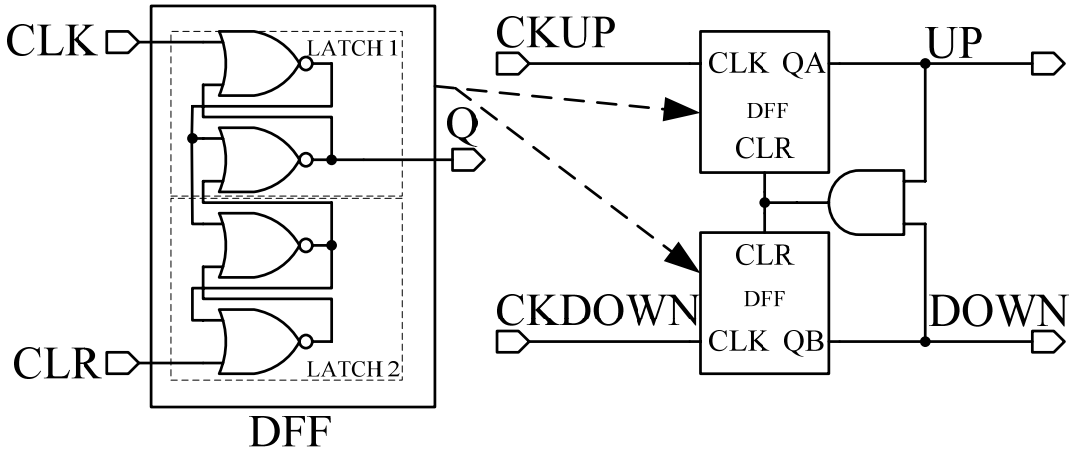


Figure 4.30 Block diagram of the sequential PFD.

Due to the finite rise time and fall time resulting from the capacitance at output nodes, if the phase difference between the two inputs is small, the pulse may not have enough time to reach a logical high level to turn on the current switches. Therefore, there is a small region where the charge pump switches cannot be effectively turned on, and that is called “dead zone”. To eliminate the dead zone problem, two inverters can be inserted in the reset path to generate enough delay.

Figure 4.31 shows the transient simulation results of the PFD. When the input frequencies of the reference signal is lagged behind the input frequencies of the divided signals, the increasing pulse width signal will be generated at the DOWN output of the CP.

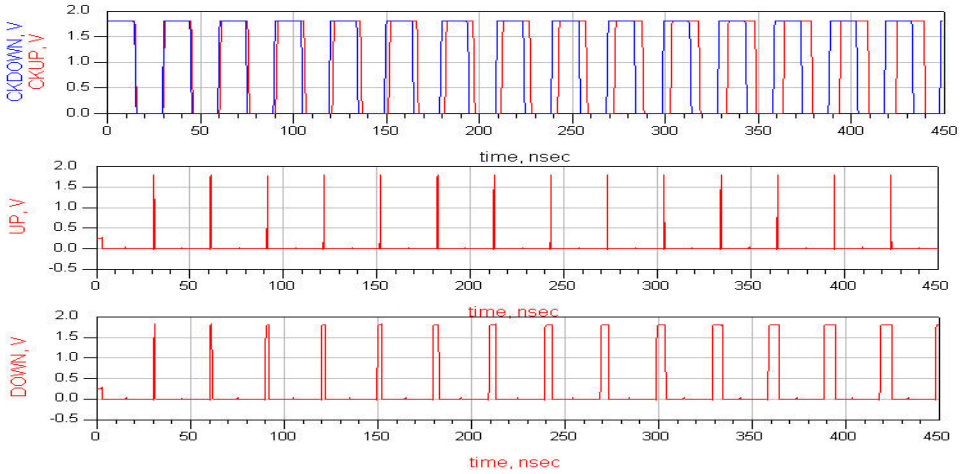


Figure 4.31 Transient simulation results of the PFD.

The simulated characteristic of the phase-frequency detector is shown in Figure 4.32

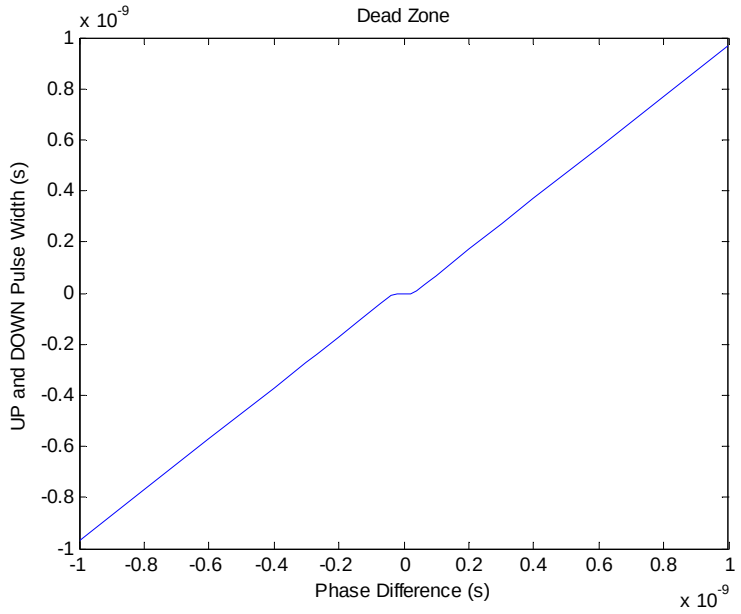


Figure 4.32 Characteristic of the PFD.

4.2.5 Charge Pump and Loop Filter

In the design of charge pump, there are several issues such as, current mismatch between the charge and discharge current sources (Figure 4.33), clock feedthrough of the switches (Figure 4.34), and charge sharing (Figure 4.35).

In Figure 4.33, if there is no current mismatch between the charge and discharge

current sources and the PLL is locked, the I_{charge} is equal to the $I_{discharge}$. If the current sources are mismatched, more or less current will charge and discharge controlled voltage respectively. Therefore, current mismatch should be as small as possible.

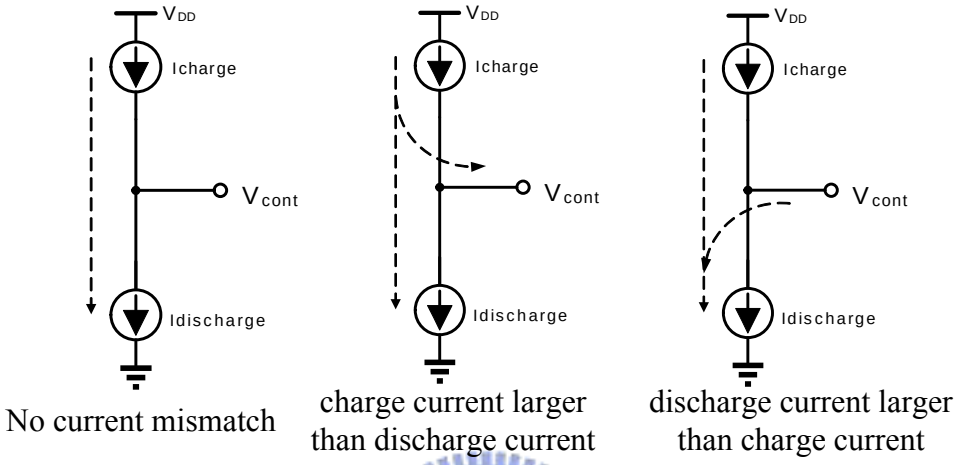


Figure 4.33 Current mismatch

In Figure 4.34, the switches of the CP directly connect to the output. When the voltage of the PFD is output from high to low, there is a current spike generated at the output of the CP. Therefore, the current switches should not be directly connected to the output of the CP.

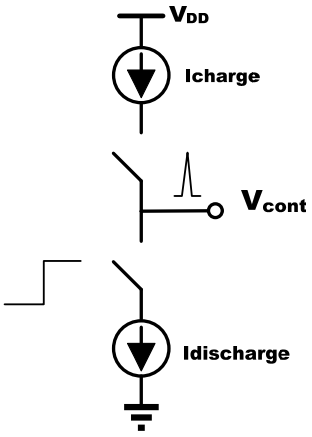


Figure 4.34 Clock feedthrough of the switches

In Figure 4.35, there are parasitic capacitances between the current source and the current switch. When the switch is closed, voltage node U is charged to VDD and node D is discharge to GND. Therefore, as the switches are turn on, the charge in the parasitic capacitances will affect the $V_{cont,}$ and the effect is called “charge sharing.”

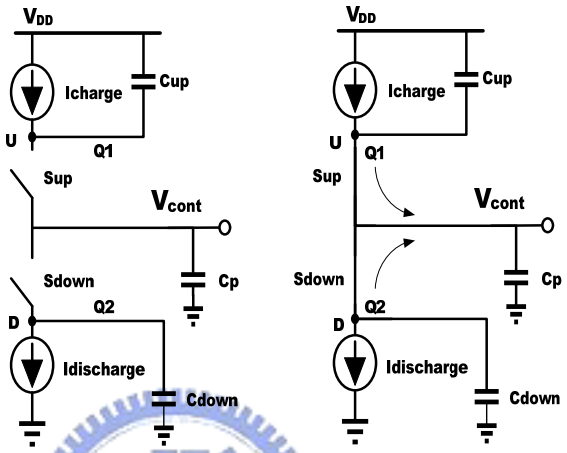


Figure 4.35 Charge sharing

The non-ideal effects of the CP will introduce the reference spurious. As shown in the Figure 4.36, in the integer-N architecture, the output sidebands around the carrier arise from the periodic ripple on the VCO control line.

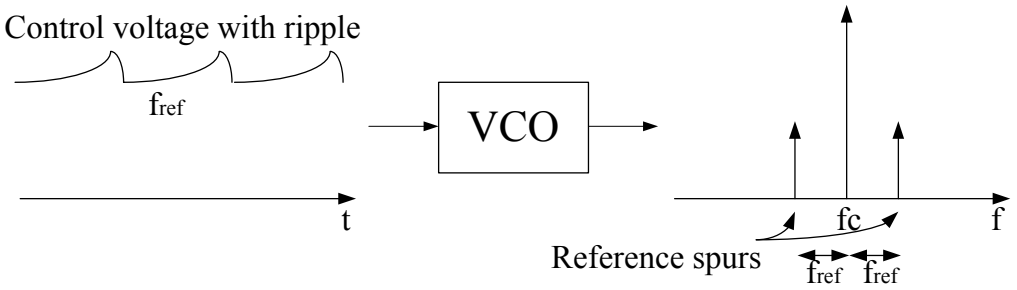


Figure 4.36 Reference spurs.

The ripple arises from the non-idealities of the phase detector and the charge pump. In the Figure 4.37, the charge injection and clock feedthrough problem between PMOS

and NMOS switches in the charge pump cause the ripple on the VCO control line. The mismatch of the charge and the discharge currents in the charge pump circuit and the mismatch of the magnitudes, widths, and timing of the UP and DN pulses in the phase frequency detector are the other reasons of the introduced ripple.

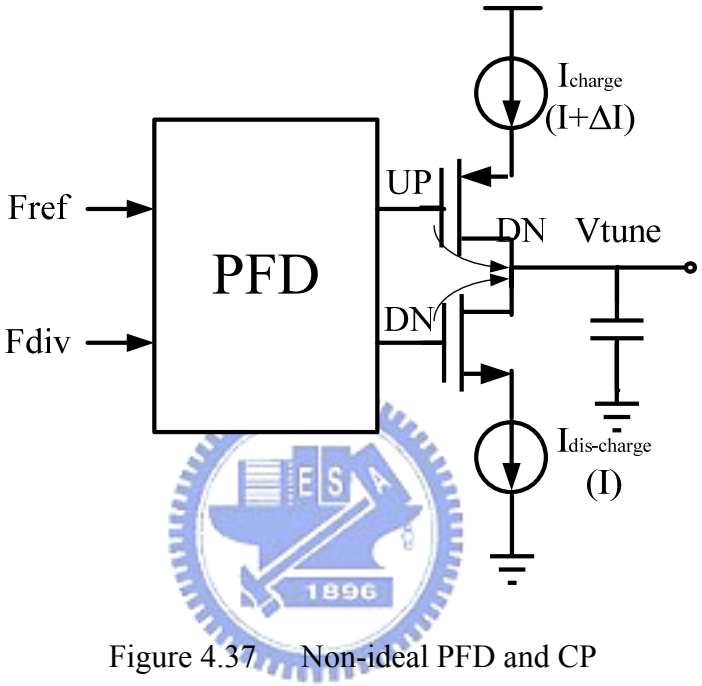


Figure 4.37 Non-ideal PFD and CP

The frequency of the ripple is the same as the reference frequency. The ripple will modulate the VCO frequency, and there are sideband spurs introduced by the ripple. The spacing between the carrier frequency and the sideband spurious is equal to the reference frequency. The spurious is called “reference spurious”. How the ripple introduces the sideband spurs can be explained by the following equation. The output frequency of the VCO is at equation (4.54). ω_0 is the free running frequency.

$$\omega_{out} = \omega_0 + K_{vco} \times V_{cont} \tag{4.54}$$

Assuming the ripple is a small sinusoidal signal, the control voltage is $V_c \cos(\omega_m t)$,

and ω_m is the frequency equal to the reference frequency.

$$V_{out}(t) = V_o \cos(\omega_0 t + K_{VCO} \int V_{cont}(t) dt) \tag{4.55}$$

$$V_{out}(t) = V_o \cos(\omega_0 t + K_{VCO} \frac{V_c}{\omega_m} \sin \omega_m t) \tag{4.56}$$

$$V_{out}(t) = V_o \cos \omega_0 t \cos(K_{VCO} \frac{V_c}{\omega_m} \sin \omega_m t) - V_0 \sin \omega_0 t \sin(K_{VCO} \frac{V_c}{\omega_m} \sin \omega_m t) \tag{4.57}$$

From the narrow-band FM approximation, if V_c is small enough, $K_{VCO} \frac{V_c}{\omega_m} << 1$ rad, then

$$\cos(K_{VCO} \frac{V_c}{\omega_m} \sin \omega_m t) \approx 1 \tag{4.58}$$

$$\sin(K_{VCO} \frac{V_c}{\omega_m} \sin \omega_m t) \approx K_{VCO} \frac{V_c}{\omega_m} \sin \omega_m t \tag{4.59}$$

$$V_{out}(t) \approx V_o \cos \omega_0 t - V_0 \sin \omega_0 t (K_{VCO} \frac{V_c}{\omega_m} \sin \omega_m t) \tag{4.60}$$

$$V_{out}(t) \approx V_0 \cos \omega_0 t - K_{VCO} \frac{V_c}{2\omega_m} V_0 [\cos(\omega_0 - \omega_m)t - \cos(\omega_0 + \omega_m)t] \tag{4.61}$$

We can see that the $\cos(\omega_0 - \omega_m)t$ and $\cos(\omega_0 + \omega_m)t$ are the reference spurs, and the relative magnitude of the sidebands is $\frac{K_{VCO} V_c}{2\omega_m}$

In the design of charge pump shown in Figure 4.38, the NMOS and PMOS switches are connected between the current source transistors and the supply rails. The problem of clock feedthrough and charge injection is lower.

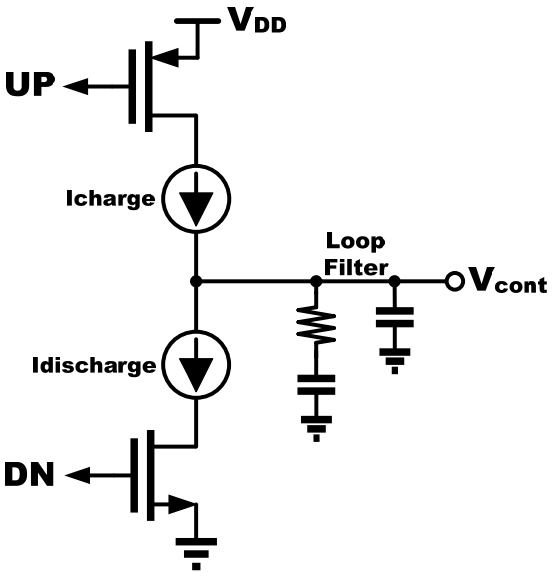


Figure 4.38 Modified charge pump circuit.

The pump-down circuit of the CP is shown in Figure 4.39 [16]. The channel length modulation will cause the mismatch between the UP and DOWN current sources. Therefore, the long channel devices are used in the design of the charge pump. The transistor M_1~M_2 generate the reference currents. The output current of the charge pump is designed to be about 210 μA when V_b=1.8 V. To reduce the mismatch in the current mirror due to the switch M_8 in the pump-down circuit, transistor M_6 is inserted such that the current in M_6 is more accurately scaled in M_8. (Note that the schematic of the pump-up circuit is not shown.)

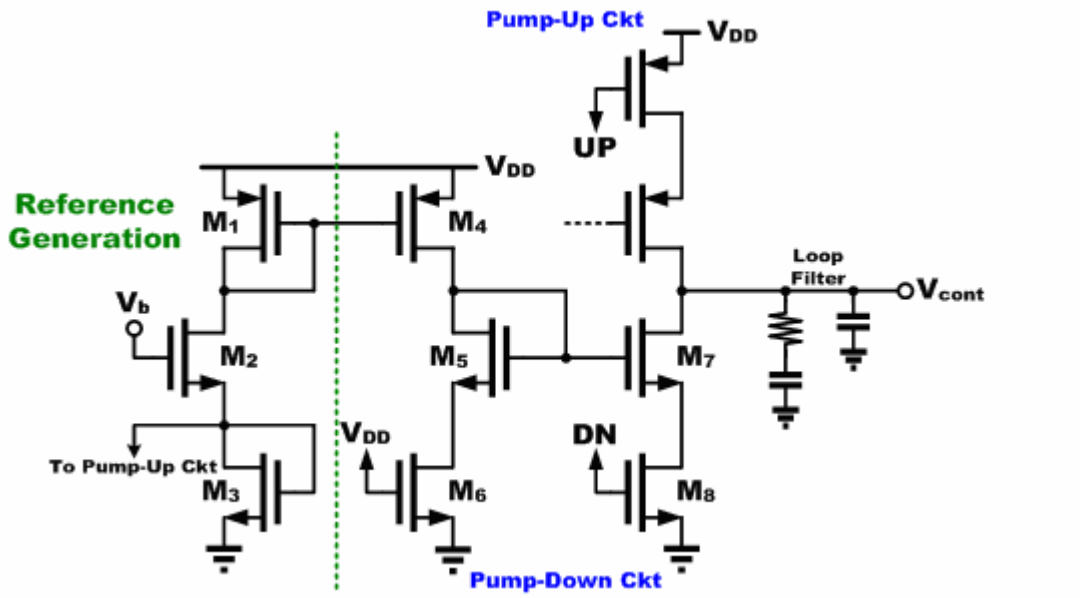
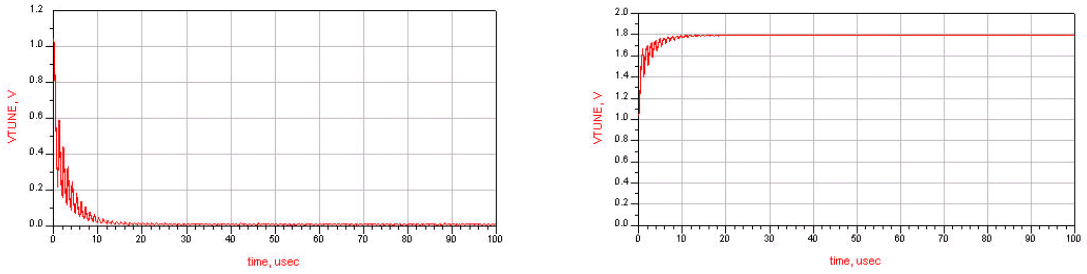


Figure 4.39 Circuit schematic of pump-down current source.

The loop filter is a second-order passive filter. The loop bandwidth and the phase margin of the synthesizer are chosen to be 300-kHz and 60 °, respectively. The values of the loop filter components have been calculated before.(R_Z = 8.84 Ω, C_Z = 224 pF, and C_P = 17.32 pF)

The transient simulation result of the combination of the PFD and CP with loop filter is shown in Figure 4.40. In Figure 4.40 (a), the input frequencies of the reference and divided signals are 33-MHz and 34-MHz respectively. The VCO control line is discharged to GND, indicating that the function of the combination of the PFD and CP works properly. Similarly, in Figure 4.40 (b), the input frequencies of the reference and divided signals are 34-MHz and 32-MHz respectively, and The VCO control line is charged to VDD.

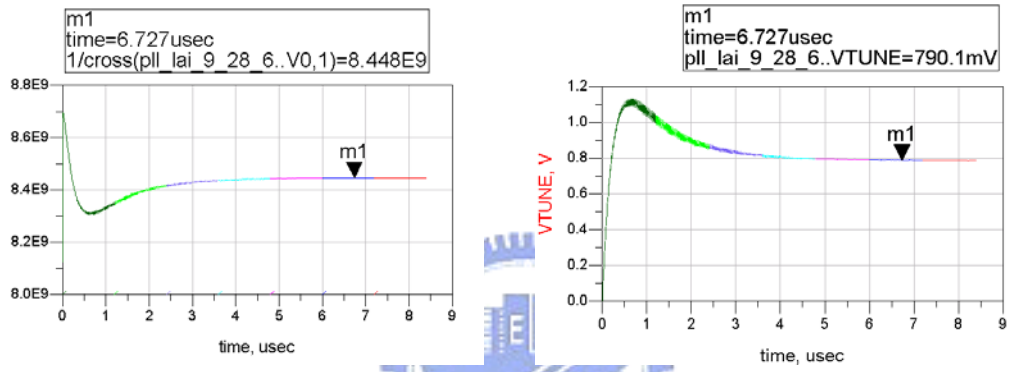


(a) Fref=33MHz
Fdiv=34MHz

(b) Fref=34MHz
Fdiv=33MHz

Figure 4.40 Transient simulation result of the PFD+CP with loop filter.

The transient simulation result of the PLL is shown in Figure 4.41.



(a) the frequency of the divider output is delay the reference frequency in the beginning.

(b) the reference frequency is delay the frequency of the divider output in the beginning.

Figure 4.41 Transient simulation result of the PLL.

4.3 Single Sideband Mixer and LC Buffer

The SSB mixer employs double-balanced topology to minimize spurious and requires quadrature inputs to perform frequency additions and substations. There are multiple Gm stages and current sources in the SSB mixer to cover wide input frequency range as shown in Figure 4.42. When the current source transistors M1 and M2 are turned on, the Gm stage transistor M3-M6 translate the input voltage of M3-M6 to the current and mix to the other input of the mixer. In the same way, when the current source transistors M7 and M8 are turned on, the Gm stage transistor M9-M12 translate

the input voltage of M9-M12 to the current and mix to the other input of the mixer. Therefore, the mixer can change the mixed frequency via the different Gm stages and the selected current source transistor.

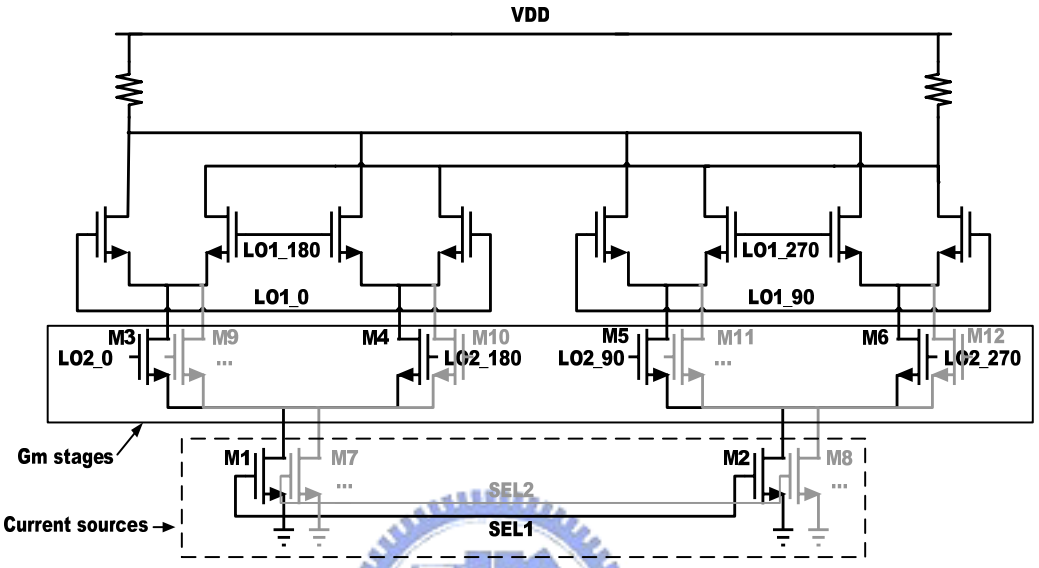


Figure 4.42 A SSB mixer with selection function

The last stage mixer needs to provide a pure carrier frequency, and filtering techniques can be applied to suppress spurious. In [5], the band pass load is combined in the SSB mixer shown in 4.43, and the band pass filter is programmed with the hopping frequency. Band selection is operated by adding the capacitor arrays to change the resonant frequency of the LC tank.

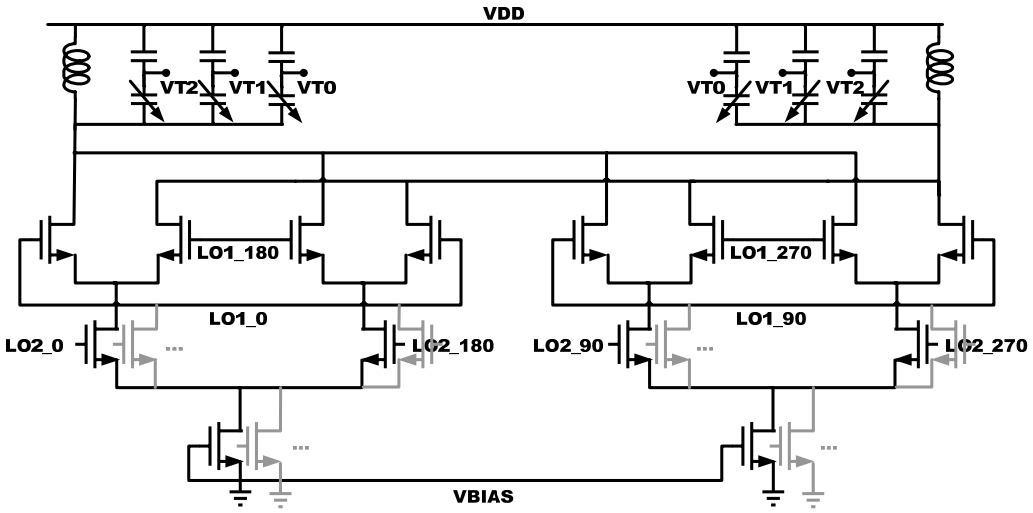


Figure 4.43 A SSB mixer with the LC load

The last three building blocks of the proposed frequency synthesizer shown in Figure 4.44 are selectors, passive mixers, and LC buffers. The architecture can be regarded as folding the LC loads in Figure 4.43 to the following stage. Therefore, the carrier frequency can be amplified by the LC buffer and the carrier swing will not be limit by small overdrive voltage in Figure 4.43. Furthermore, switching inductors and negative resistance are used to improve the operation range and quality factor of the LC tank respectively.

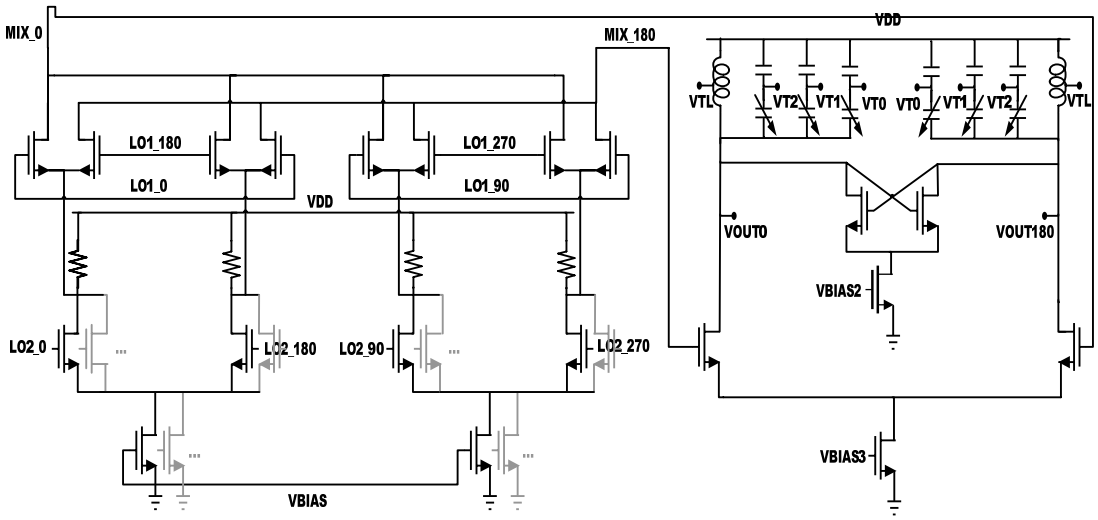
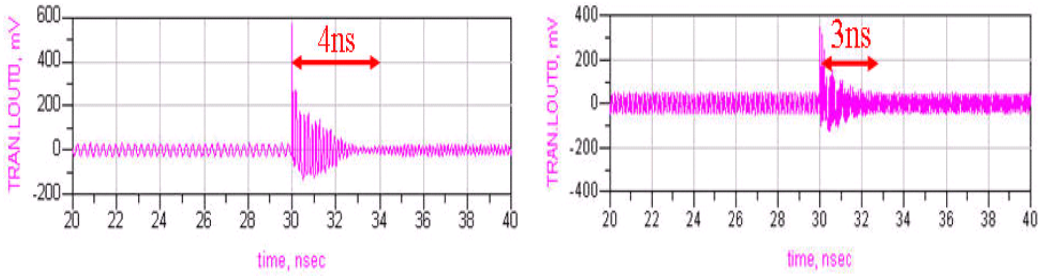


Figure 4.44 Schematic of the selector, the passive mixer, and the LC buffer

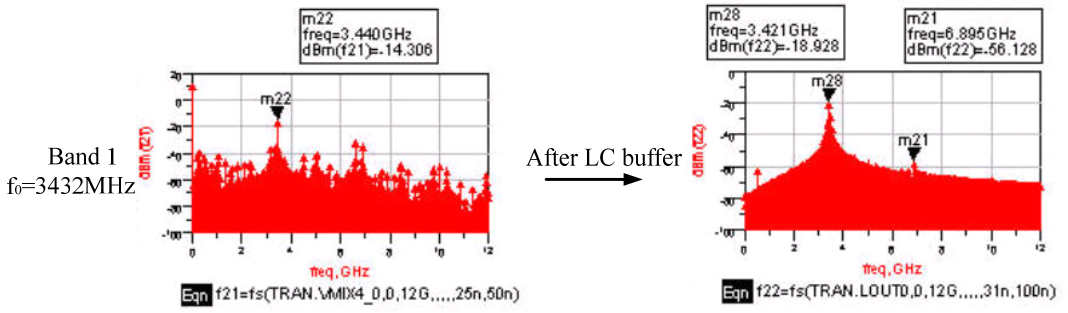
In Figure 4.45 (a) (b) show the carrier frequency changes form 3432-MHz to 6072-MHz and from 7128-MHz to 10296-MHz respectively. The switching time are less than 9.47ns.



(a) The carrier frequency changes from 3432MHz to 6072MHz (b) The carrier frequency changes from 7128MHz to 10296MHz

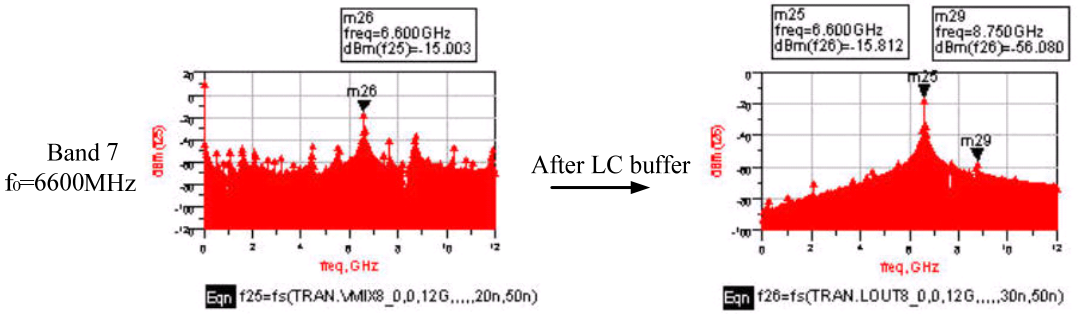
Figure 4.45 Switching time are less than 9.47ns

The output spectrum simulation results of the pssive mixer and the LC buffer are shown in Figure 4.46 and 4.47. The carrier frequency spectrums of 3432-MHz and 6600-MHz are shown in Figure 4.46 and 4.47 respectively. After the LC buffer, the output frequency spectrum is purer.



(a) Output spectrum of the passive mixer (b) Output spectrum of the LC buffer

Figure 4.46 Output frequency spectrums (f_0 =3432-MHz)



(a) Output spectrum of the passive mixer (b) Output spectrum of the LC buffer

Figure 4.47 Output frequency spectrums (f_0 =6600-MHz)

4.4 Summary

The phase error of 3432 MHz is 1.58 degrees and is shown in Figure 4.48. The simulated performance of the signal generator circuit is summarized in Table 4.4. The spurious are lower than -24dBc in all band groups of the UWB system. Since the resolution of the simulator, the period set in the eye diagram can not match precisely with the real period of the carrier. Therefore the phase errors in some bands are larger. When the offset frequency 264MHz is used, the spurs are worse. Because spurs generated by 264MHz are closer to carrier frequency and the quality factor of the BPF is not high enough leading poor spur suppression. (Note: Compare with 792MHz, 1320MHz, and 1848MHz) Switching time is less than 9.47ns. The phase noise of the QVCO is lower than -95 dBc/Hz at 100-kHz frequency offset.

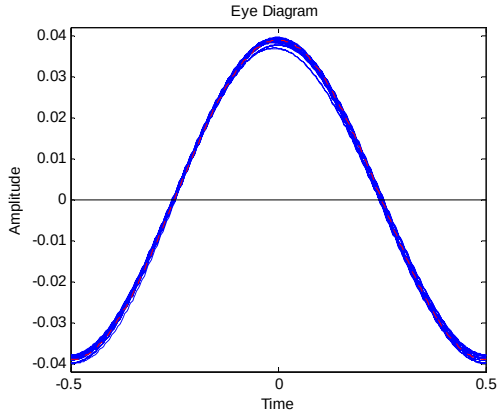


Figure 4.48 The phase error of 3432 MHz is lower than 1.58 degrees

Frequency band (MHz)	Output power (dbm)	Spurs (dbc)	Distance to spur (MHz)	Phase error (degree)
3432	-18.928	-37.2	3474	1.58
3960	-16.644	-30.744	1080	5.94
4488	-21.717	-32.618	1067	7.68
5016	-20.631	-32.584	1858	5.98
5544	-17.153	-32.057	1050	5.98
6072	-15.99	-39.904	2133	4.66
6600	-15.812	-40.268	2150	3.03
7128	-14.96	-33.073	2100	5.36
7656	-14.759	-39.281	3200	11.01
8184	-15.056	-24.764	1100	6.05
8712	-14.95	-26.634	1050	12.72
9240	-17.279	-35.731	1050	16.89
9768	-18.71	-30.284	2150	10.91
10296	-15.329	-31.766	2100	17.64

Table 4.4 Simulated performance of the signal generator circuit.

The performance comparison of the frequency synthesizer is summarized in Table 4.5.

	Process (μm)	Power (mW)	Spurious (dBc)	Phase noise (dBc/Hz)	@Offset (Hz)	Supply voltage (V)	Frequency range (GHz)	No. of bands	Architecture	Year
[3]	0.13 CMOS	45	-60(only one on)	-105	1M	1.5	3.4~4.5	3	PLL*3	2005 JSSC
[8]	0.18 CMOS	18	-20	N/A	N/A	1.8	3.4~4.5	3	PLL+SSB*3	2005 ISSCC
[4]	0.25 SiGe	27	-35	-104	1M	2.7	3.4~4.5	3	PLL*2+SSB	2005 ISSCC
[9]	0.18 SiGe	46	N/A	-110	1M	2.7	3.4~7.9	7	PLL+SSB*2	2005 JSSC
[2]	0.18 CMOS	116.28	-52	-109.6	1M	1.8	3.4~7.9	7	PLL*2	2005 JSSC
[5]	0.18 CMOS	48	-37	-103	1M	2.2	3.4~7.9	7	PLL*2+SSB	2005 ISSCC
[6]	0.09 CMOS	47	-20	-98	1M	1.1	3.4~9.2	12	PLL+SSB*2	2006 ISSCC
This work	0.18 CMOS	76.5	-24	-116.2 (QVCO)	1M	1.8	3.4~10.3	14	PLL+SSB*2	2006

Table 4.5 Performance analysis

Chapter 5
Layout and Implementations

5.1 Layout

5.1.1 Layout Considerations

The layout of differential high-frequency circuits should be as symmetric as possible. The active component should be as close as possible. The coupling effect should be concerned at high frequency, since degrades the performance of the layout. The circuit may need some shielding techniques on layout. An easy way is to use a additional ground or DC path inserted between two sensitive signals.

In order to prevent noise coupling by the power line, separation of analog VDD and digital VDD can reduce the coupling effect between analog circuits and digital circuits. Additional large capacitances can insert between bias lines and ground to make the bias voltage more stable.Guard rings can help to isolate the sensitive device from the substrate noise from other circuits.

5.1.2 Layout of the Phase-Locked Loop

The phase-locked loop consists of the analog circuits and digital circuits. The digital switching noise will significantly affect the performance of the analog circuits

through the power lines. Therefore, the power lines should be separated for the analog and digital circuits. The two differential outputs of the VCO is shielding with ground lines. The floor-plan of phase-locked loop is shown in Figure 5.1. The total chip area is $2.5\times2.5mm^2$. The layout of the frequency synthesizer is shown in Figure 5.2.

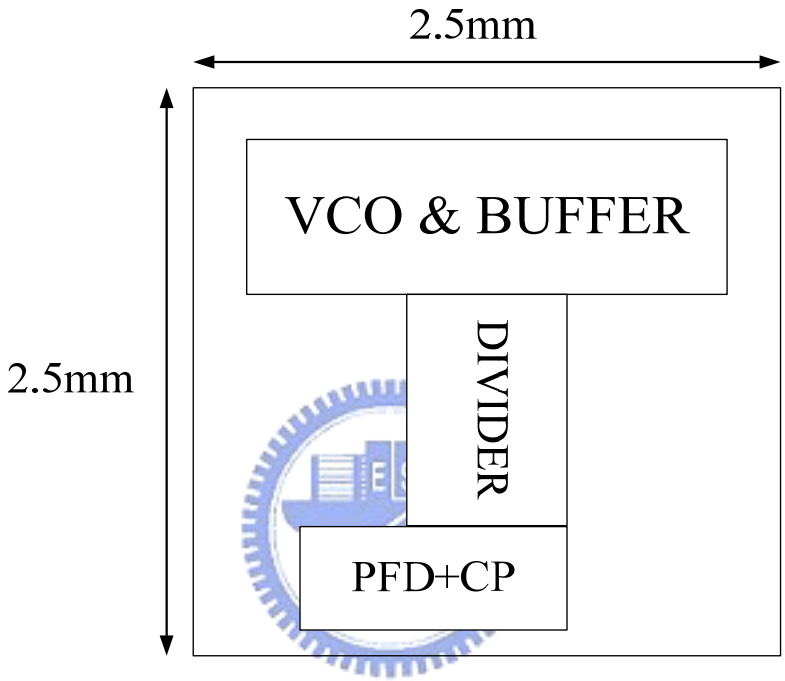


Figure 5.1 Floor-plan of the PLL

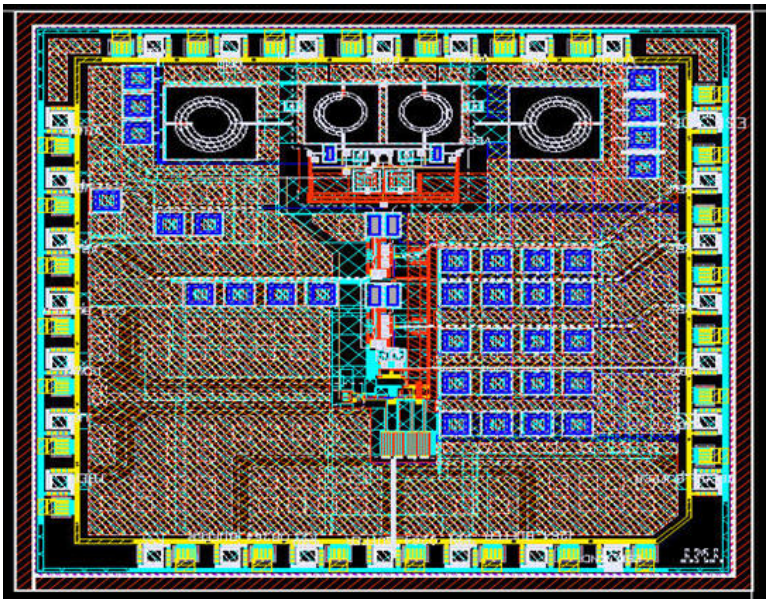


Figure 5.2 Layout of the PLL

5.1.3 Layout of the Signal Generator

The floor-plan of signal generator is shown in Figure 5.3. The total chip area is $2\times2.5mm^2$. The layout of the frequency synthesizer is shown in Figure 5.4.

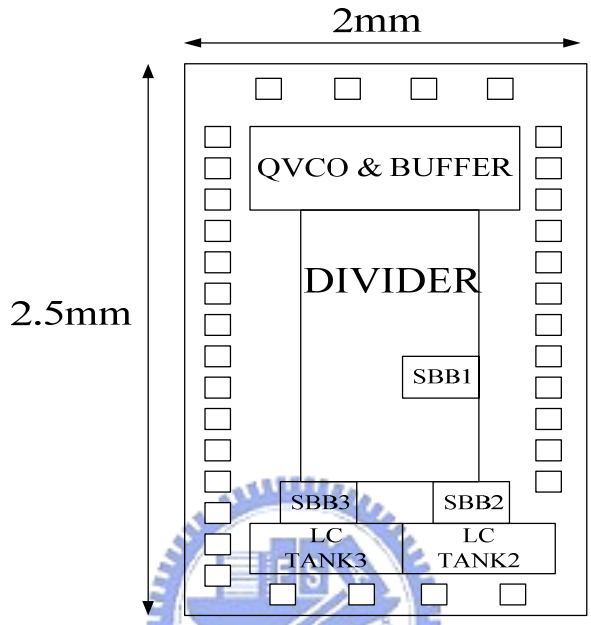


Figure 5.3 Floor-plan of the signal generator

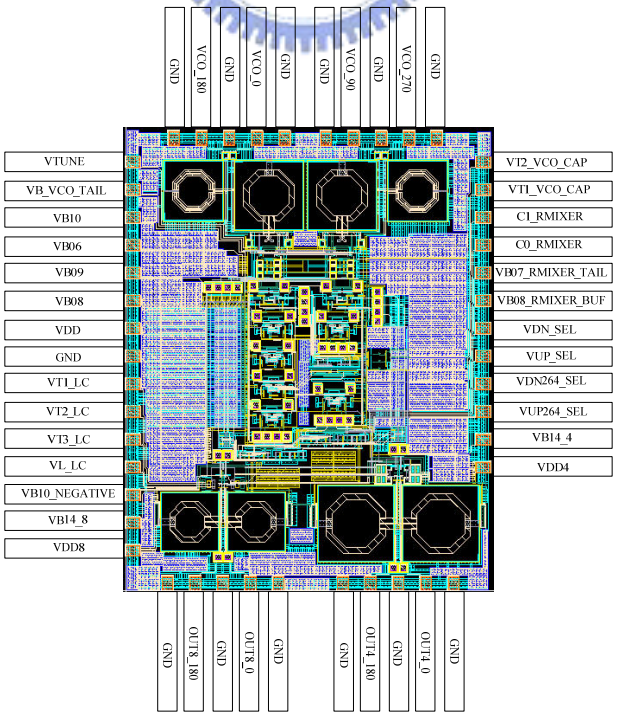


Figure 5.4 Layout of the signal generator

5.2 Measurement

5.2.1 On-Wafer Measurement

The building block VCO is measured on the wafer and discussed first. The VCO is fabricated in UMC 0.18-μm CMOS technology. Both the equipments and environments of the on-wafer measurement are provided by NDL.

5.2.1.1 VCO

Testing Setup

Figure 5.5 shows the testing setup for the phase noise and spectrum measurement of the voltage-controlled oscillator. It consists of a spectrum analyzer, a high-frequency ground-signal-ground-signal-ground (GSGSG) probe, a DC probe and a power supply box. One of the oscillator outputs is terminated by a load having an impedance of 50 Ω. And the other output is connected to the spectrum analyzer.

Figure 5.5 Testing setup for the voltage-controlled oscillator.

Layout and Die Photograph

The layout of the voltage-controlled oscillator is shown in Figure 5.6. The balanced output signal is available from the top bonding pads (GSGSG). The DC supplies and tune voltage are applied to the bottom side. Figure 5.7 shows the die

photograph of the voltage-controlled oscillator.

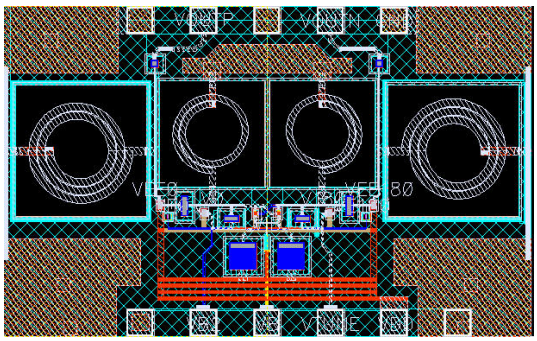


Figure 5.6 On-wafer layout of the VCO.

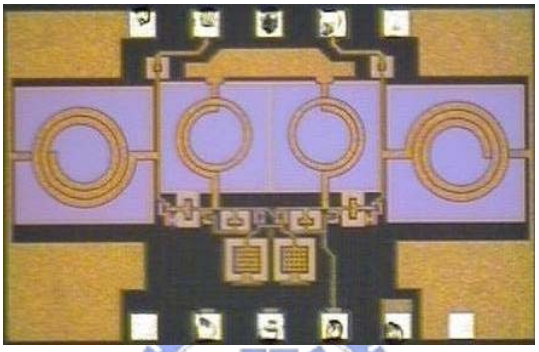


Figure 5.7 Die photograph of the VCO.

Measurement Results

The measured output spectrum at a frequency of 7.53-GHz is shown in Figure 5.8.

The output power including the cable loss is about -6.99dBm.

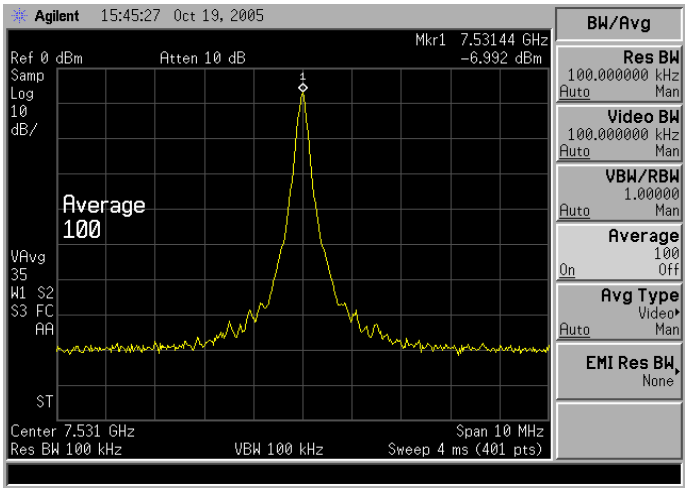


Figure 5.8 Measured output spectrum of the on-wafer VCO.

The tuning characteristic of the VCO is measured by stepping the control voltage and measuring the corresponding output frequency with the spectrum analyzer. The measured and simulated tuning characteristic of the VCO is shown in Figure 5.9. The tuning curve covers the desired frequency band from 7.47-GHz to 7.57-GHz. The VCO gain over the desired frequency band is about 55-MHz/V. For the control voltage range from 0V to 1.8V, a 100-MHz or 1.33% tuning range of the VCO is available.

The frequency tuning range is different from the post-simulation. If we run the EM simulation, the VCO oscillation frequency is lower than the post-simulation. The EM simulation of this work is a little different form the measurement result and to get closer EM result, a more accurate substrate model is required.

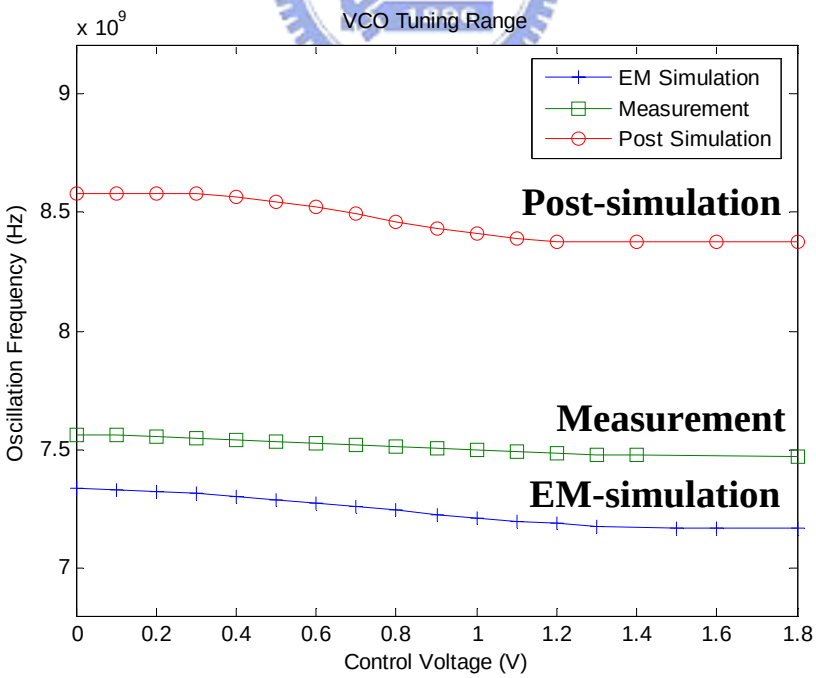


Figure 5.9 Measured tuning characteristic of the on-wafer VCO.

Figure 5.10 shows the phase noise measurement of the on-wafer voltage-controlled oscillator at a spot frequency of 1-MHz. (Note: The carrier frequency is 7.53-GHz and the control voltage is 0.5V) the measured phase noise is -79.8dBc/Hz at 100-kHz frequency offset and -101.66dBc/Hz at 1-MHz frequency offset.

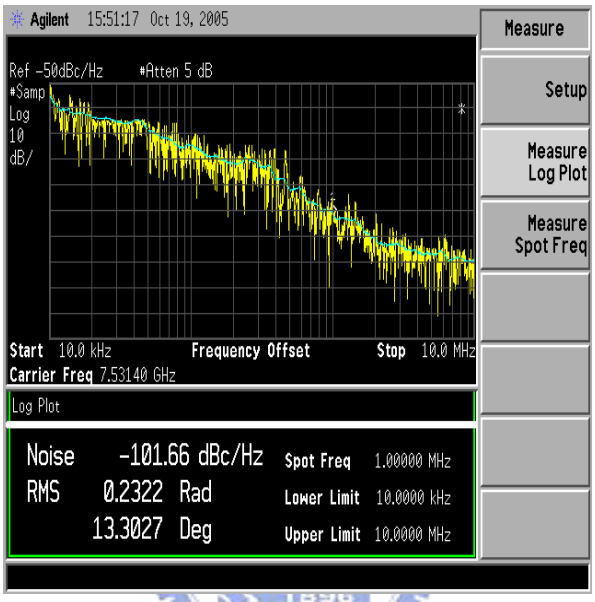


Figure 5.10 Measured phase noise of the on-wafer VCO.

The degradation of the phase noise performance results from the lack of on-chip supply decoupling capacitors. All power supplies and DC bias voltages are ideal voltage sources in simulation. The noisy power and DC supplies will significantly affect the performance of the circuit, especially the VCO. The on-chip decoupling capacitors or on-chip regulators should be added between the power lines. The VCO consumes 19.764mW from 1.8 V supply including output buffers.

5.2.1.2 Divider

Testing Setup

Figure 5.11 shows the testing setup for the measurement of the divider. It consists of a spectrum analyzer, two high-frequency ground-signal-ground-signal-ground (GSGSG) probes, a DC probe, an ESG, a balun, and a power supply box. The balun can convert the single-ended input signal to the differential output signal

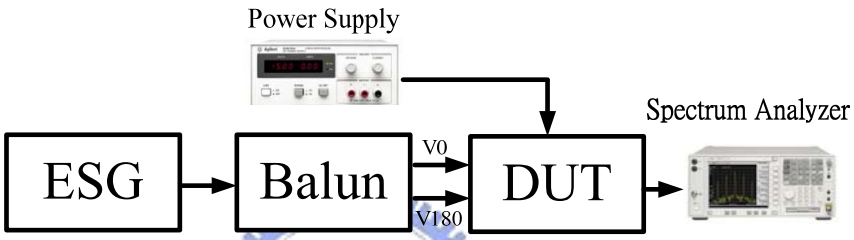


Figure 5.11 Testing setup for the divider.

Layout

The layout of the high-frequency divide-by-2 circuit is shown in Figure 5.12. The differential input signal from the balun is applied to the left bonding pads. The output divided signal is available from the right bonding pads. The DC supplies are applied to the top side.

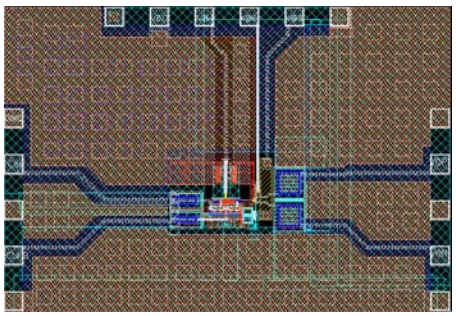


Figure 5.12 On-wafer layout of the divider

Measurement Results

Figure 5.13 and 5.14 show the measured minimum and maximum input operating frequency of the DTC respectively. The measured frequency that can be divided is 2.748-7.02GHz, which is lower than the expected 8.448GHz, due to the parasitic capacitance of the interconnected metal line between the divider and the buffers. This effect should be considered carefully in post-simulation.

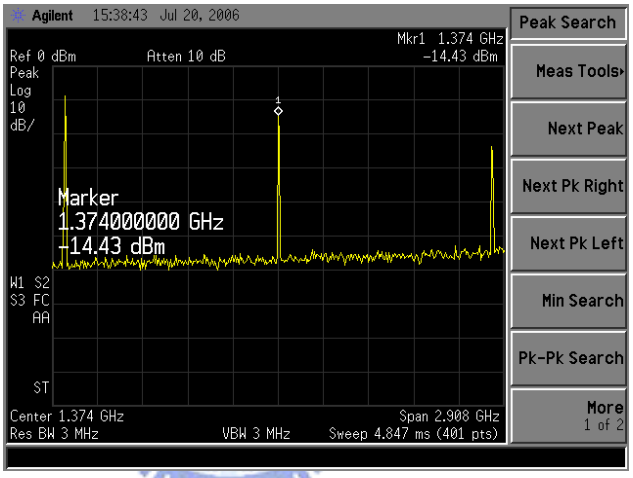


Figure 5.13 Measure output spectrum at the input frequency of 2.748-GHz.

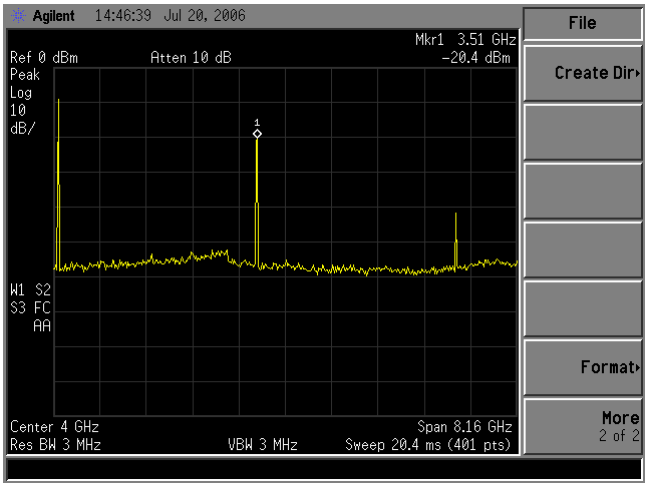


Figure 5.14 Measure output spectrum at the input frequency of 7.02-GHz.

5.2.2 Package Measurement

Figure 5.15 shows the testing board of the PLL. The PLL is fabricated in UMC 0.18-μm CMOS technology

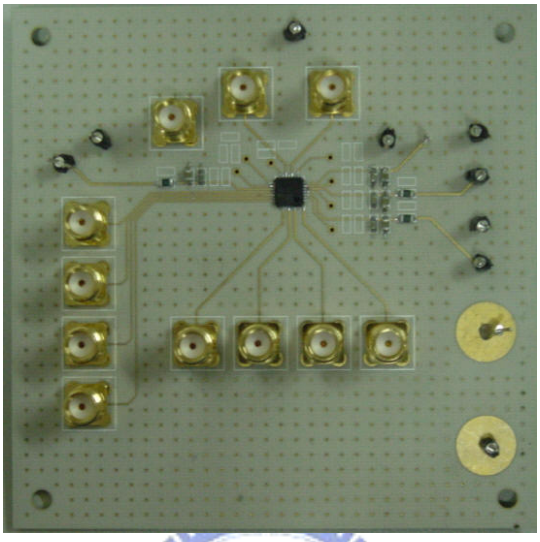


Figure 5.15 Testing board of the PLL

5.2.2.1 VCO

Testing Setup

In the package version, the testing setup for the phase noise measurement and spectrum measurement of the voltage-controlled oscillator is similar as on wafer version. When measuring the VCO, only the supply voltage of the VCO is turn on, and all other power supplies are off.

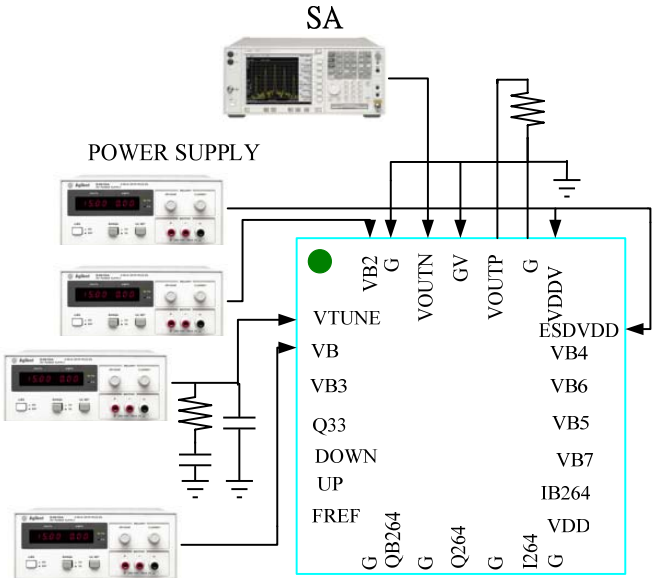


Figure 5.16 Testing setup of the VCO

Measurement Results

The measured output spectrum at a frequency of 7.455-GHz is shown in Figure 5.17. The output power including the cable loss is about -16.27dBm.

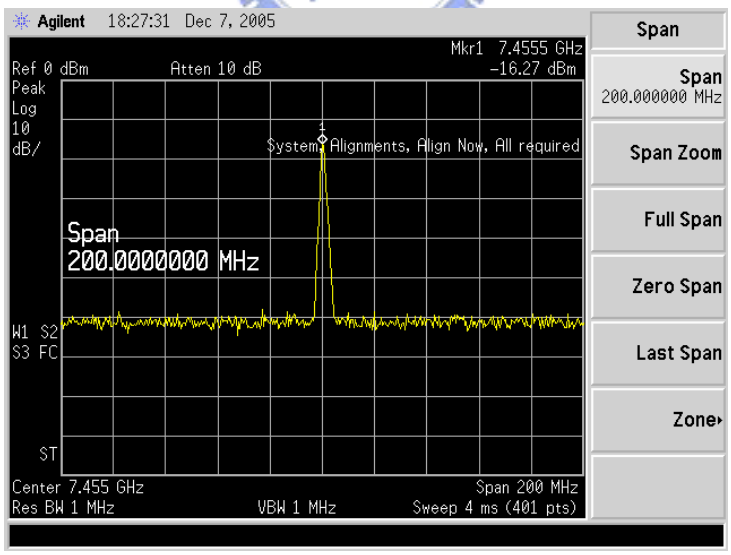


Figure 5.17 Measured output spectrum of the packaged VCO.

The measured and simulated tuning characteristic of the packaged VCO is shown in Figure 5.18. The tuning curve covers the desired frequency band from 7.4-GHz to

7.68-GHz. And the VCO gain over the desired frequency band is about 155.6-MHz/V. For the control voltage range from 0V to 1.8V, a 280-MHz or 3.7% tuning range of the packaged VCO is available. The frequency tuning range is different from the measurement result. The reason has been discussed before.

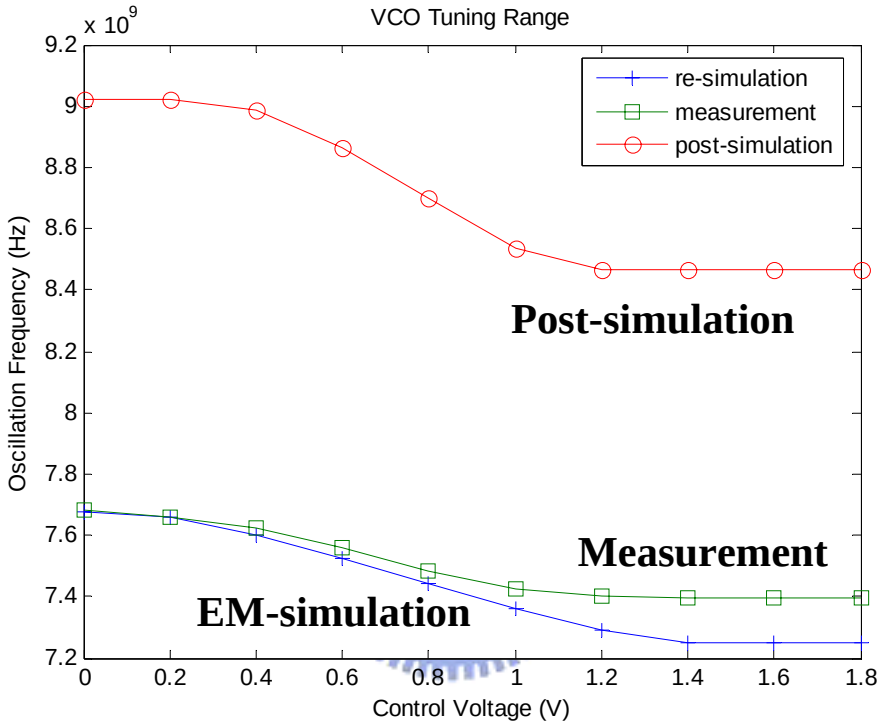


Figure 5.18 Measured tuning characteristic of the packaged VCO.

Figure 5.19 and Figure 5.20 shows the phase noise measurement of the packaged VCO at a spot frequency of 100-kHz and 1-MHz, respectively. (Note: The carrier frequency is 7.398-GHz and the control voltage is 1.8V) The measured phase noise is 74.62dBc/Hz at 100-kHz frequency offset and -92.99dBc/Hz at 1-MHz frequency offset.

Compared with the on-wafer measurement of the VCO, the performance of the packaged VCO is similar to that of the on-wafer VCO.

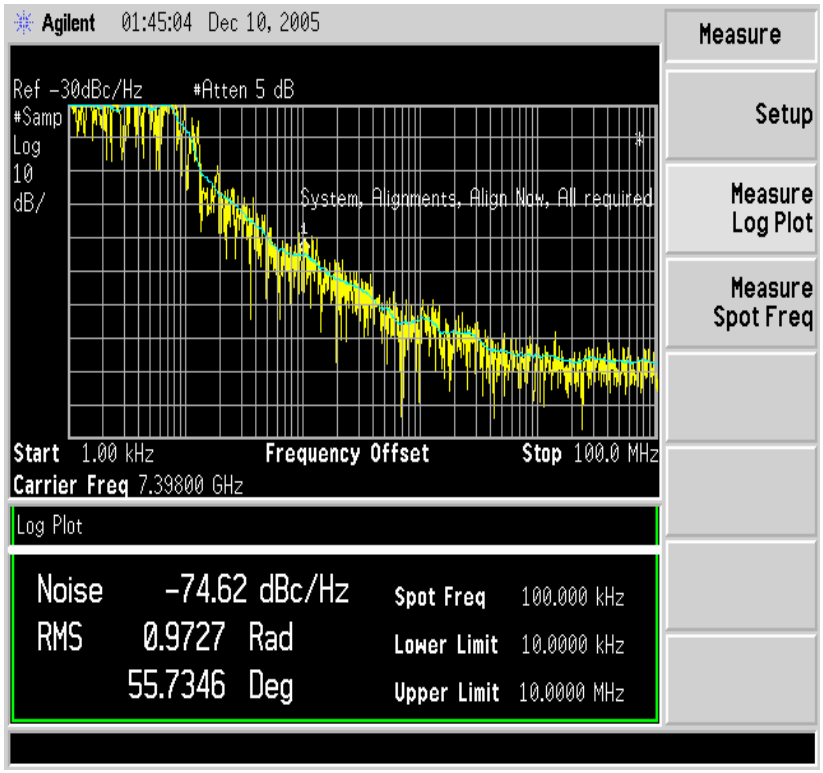


Figure 5.19 Measured phase noise of the VCO at 100-kHz frequency offset.

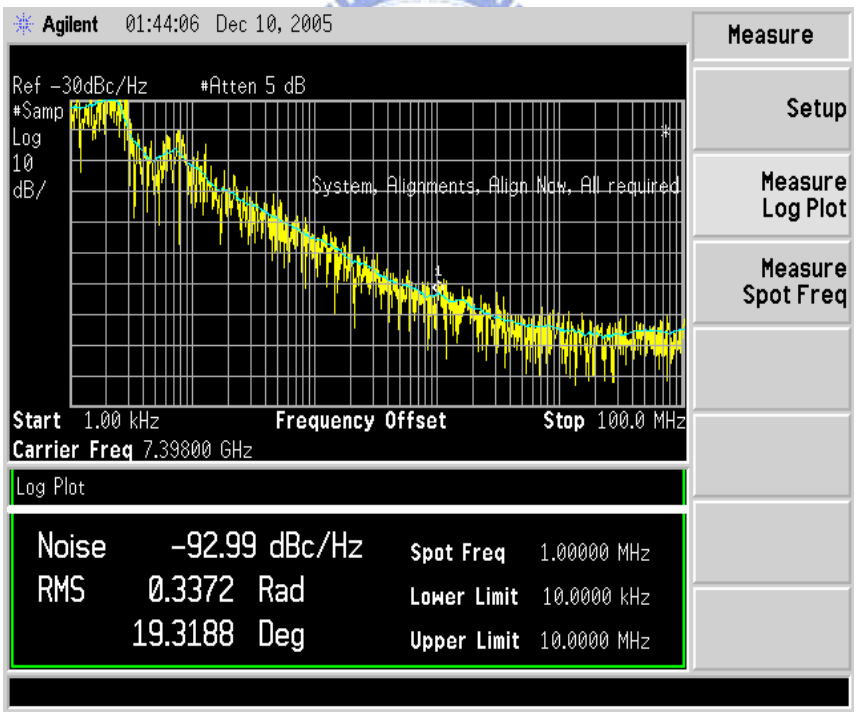


Figure 5.20 Measured phase noise of the VCO at 1-MHz frequency offset.

The performance comparison of the VCO is summarized inTable5.1.

	Design spec.	On wafer simulation	On wafer measurement	On wafer EM-simulation	Package simulation	Package measurement	Package EM-simulation
Osc frequency (Ghz)	8.448GHz	8.327~8.526	7.4682~7.5648	7.168~7.333	8.467~9.024	7.398~7.682	7.25~7.679
Tuning range (Mhz)	N/A	199	96.6	165	557	285	429
Phase noise@100khz (dBc/Hz)	-82 (fo=8.448GHz)	-93.12 (fo=8.448Ghz)	-79.8 (fo=7.5314Ghz)	-90.51 (fo=7.235Ghz)	-90 (fo=8.658Ghz)	-74.62 (fo=7.398Ghz)	-90.236 (fo=7.564Ghz)
Phase noise@1Mhz (dBc/Hz)	N/A	-116 (fo=8.448Ghz)	-101.66 (fo=7.5314Ghz)	-116.5 (fo=7.235Ghz)	-111 (fo=8.658Ghz)	-92.99 (fo=7.398Ghz)	-115.579 (fo=7.564Ghz)
Output power (dbm)	N/A	-0.721	-6.9	-4.772	-5.365	-23	-3.051

Table 5.1 The comparison between VCO simulation and measurement results

5.2.2.2 Phase Frequency Detector

Testing Setup

When measuring the output signal of the phase frequency detector, we turn on the power supply of the phase frequency detector, and close off the power supply of the VCO. A pulse generator can generate a reference clock and a reference clock with different phase. The oscilloscope can show the output waveforms of the PFD.

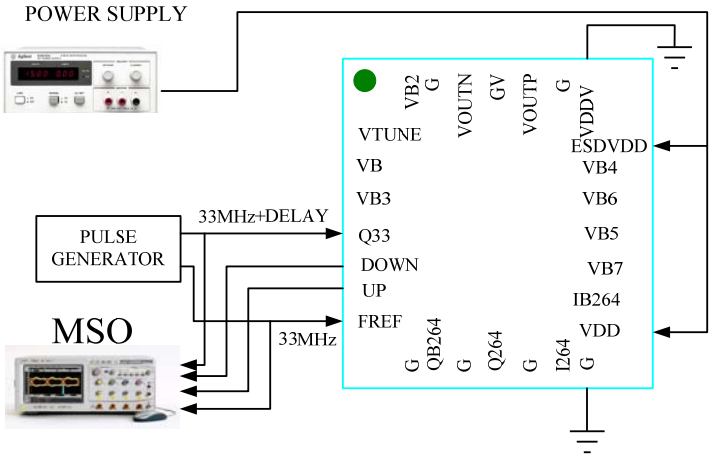


Figure 5.21 Testing setup of the PFD

Measurement Results

In Figure 5.22, when the reference frequency is lagged 22ns than the divider output frequency, there will be a wide impulse signal at the DOWN output and no impulse signals at the UP output. By the same way, in Figure 5.23, when the divider output frequency is 22ns later than the reference frequency, there will be a wide impulse signal at the UP output and no impulse signals at the DOWN output. If the frequency and phase are the same, we have no impulse signals at UP and DOWN. Therefore, the PFD works correctly.

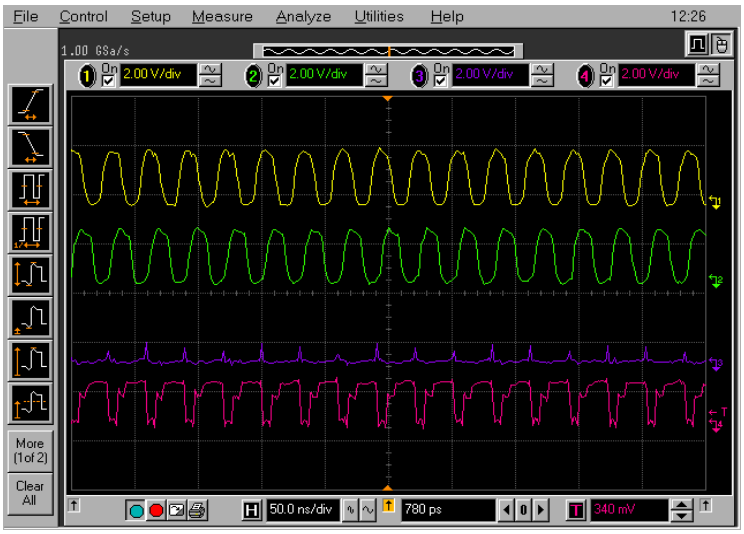


Figure 5.22 Reference frequency later 22ns than divider output frequency

Figure 5.23 Divider output frequency later 22ns than reference frequency

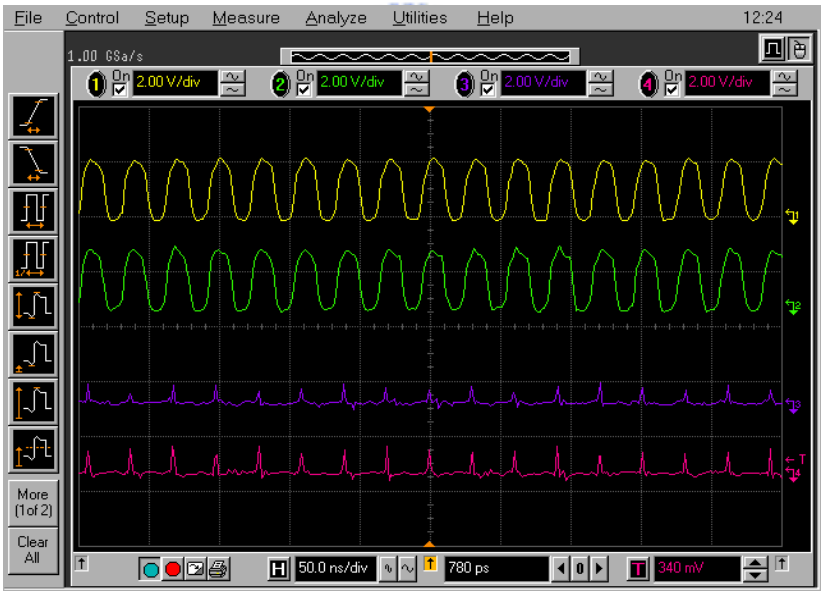


Figure 5.24 No delay

5.2.2.3 Phase Frequency Detector and Charge Pump

Testing Setup

When measuring the output signal of the phase frequency detector, we turn on the power supply of the phase frequency detector, and close off the power supply of the

VCO. The testing setup is similar as the testing setup of the PFD. The difference is that the output waveform of the VTUNE is measured.

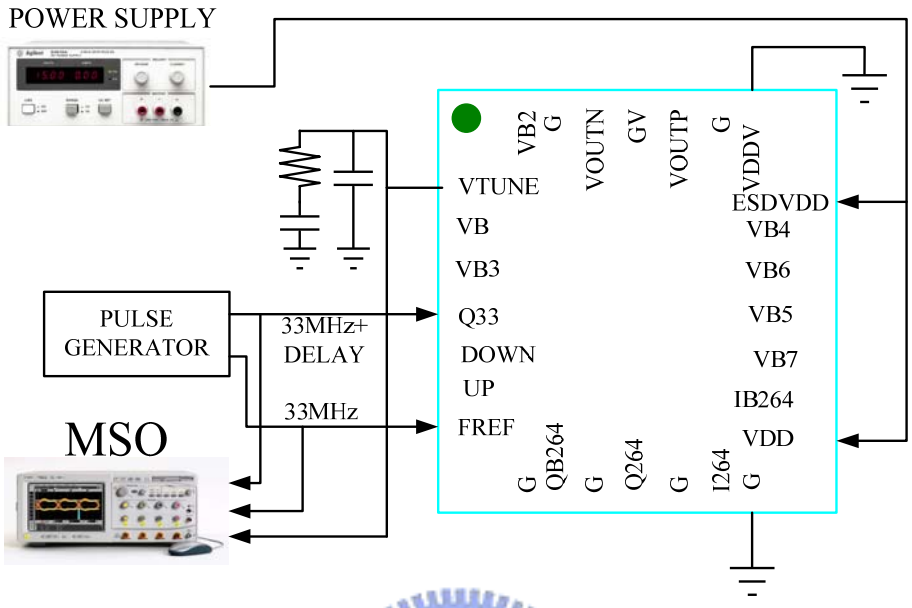


Figure 5.25 Testing setup of the PFD+CP+LP

Measurement Results

In Figure 5.26, when the reference frequency is 22ns later than the divider output frequency, there will be a wide impulse signal at the DOWN output and no impulse signals at the UP output. Therefore, the VTUNE will be discharged to zero by the charge pump. Conversely, if there have a wide impulse at the UP output, the VTUNE will be charged to VDD by the charge pump. If the phase and frequency are the same, the VTUNE is in the middle voltage between VDD and zero.

Figure 5.26 Reference frequency later 22ns than divider output frequency

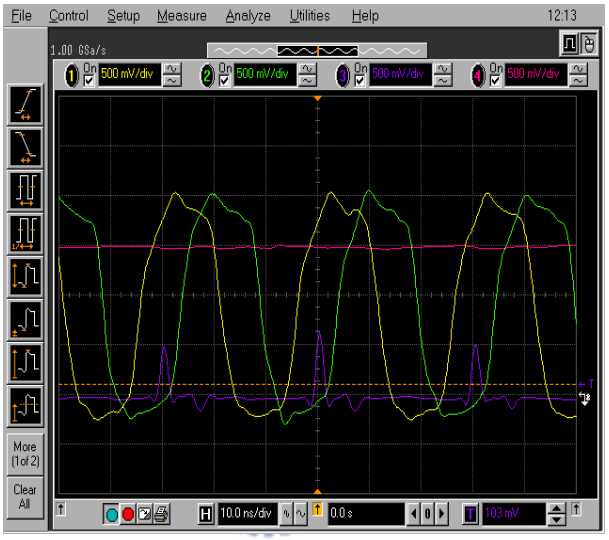


Figure 5.27 Divider output frequency later 22ns than reference frequency

Figure 5.28 No delay

5.2.2.4 Phase-Locked Loop

Testing Setup

When measuring the output signal of the PLL, we turn on the power supply of all circuits. In Figure 5.29, the frequency of the VCO can be measured by VOUTN. The waveform of the QB264 and Vtune can be measured by MSO.

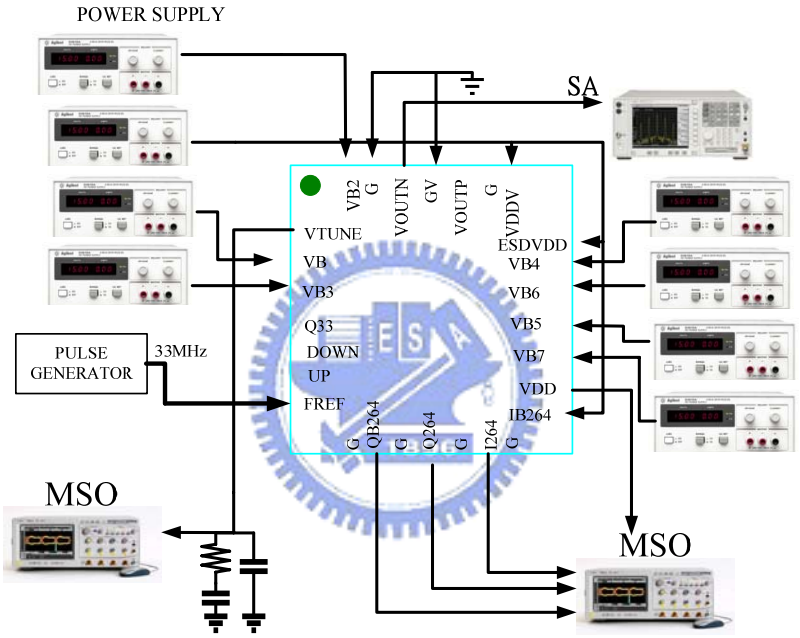


Figure 5.29 Testing setup of the PLL

Measurement Results

The PLL circuit is failed. Since the PFD, CP, and VCO works, the divider may be failed and causes the malfunction of the PLL. The post-simulation of the divider cell show that it work properly. Since the parasitic capacitance of metal lines between each cells are not considered in the post-simulation, the input swing of the divider may be not large enough to drive next stages.

Chapter 6
Conclusions and Future Works

6.1 Conclusions

The wireless frequency synthesizer has been designed and implemented for ECMA UWB WPAN with only one PLL being adopted. The fast switching time specification can be met by changing different transconductor stages of mixers or selectors. To synthesize frequencies with one PLL, the frequency planning are made by exploiting many intermediate frequencies generated by divide-by-two circuits. Therefore, the number of the SSB mixers required can be reduced and saved the power consumptions. Furthermore, the divide-by-two circuit can generate quadrature signals easily and relax the spurious problem. In the proposed architecture, the carrier frequency is generated by multistage mixing effect which is less then two times. A output buffer with LC tank is used to suppress spurious. In order to increase the quality factor and operating range of the LC tank, negative resistances and switching inductors are used in the LC buffer. The spurious suppression is -24dbc in all band group frequencies. Measurement shows the phase noise of the package VCO is –74.6dbc/Hz at 100-kHz frequency offset and the oscillation frequency is about 7.5-GHz. Since the operation frequency of the VCO is

very high, the LC tank is sensitive to the variation of the inductance and capacitance. Therefore, the parasitic inductor must take to consideration.

6.2 Future Work

To further improve spurious suppression, the quality factor of the LC tank can be made tunable by changing the different tail current of the negative resistance. In this way, the resonance bandwidth and impedance of the LC tank can be controlled by the bias voltage of the current transistor in the negative resistance. A detecting spurious circuit may be designed and fed back to the switches of the LC tank and the controlled voltage of the negative resistance to modify the filtering characteristic.

In order to mitigate the reference spurious problem, an additional NMOS in charge pump can make the delay between UP and DOWN signals the same. The insertion of more inverters in the reset path of the PFD can reduce the dead zone.

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論文題目：　Single Phase-Locked Loop Frequency Synthesizer Design for Ultra-wideband Wireless Applications

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