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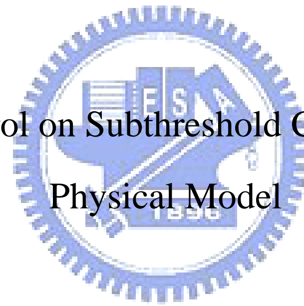
碩 士 論 文

背閘偏壓對於次臨界區電路不匹配效應之控制與其物理模型



Back-Gate Bias Control on Subthreshold Circuit Mismatch and its Physical Model

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指導教授：陳明哲 Prof. Ming-Jer Chen

中華民國 九十五 年 七 月

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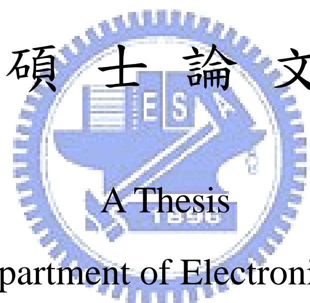

A Thesis

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摘　要

本論文研究背閘偏壓對於次臨界區的電路不匹配之效應與物理模型。我們已經量測及分析不同大小的電晶體，這些電晶體都被加以逆向及順向偏壓。我們首先觀察到，在次臨界區存在著比過臨界區更大的誤差。此種現象是因為在次臨界區中，電流與閘極電壓及製程參數成指數關係的結果。如將背閘逆向偏壓加入考慮，我們發現電流誤差隨著背閘逆向偏壓的加劇而增大，在次臨界區此一現象更加明顯。另一方面，電流誤差會隨著背閘順向偏壓的增大而改善。此種改良是因為閘控橫向電晶體在低注入情況下作用的結果。隨著分析從不同大小的電晶體所量測的結果，我們發現小尺寸的電晶體不只存在著更大的誤差，並且對於背閘偏壓更加敏感。從實驗的結果我們提出兩點建議：(一)次臨界區的電路需小心設計以免誤差；以及(二)閘控橫向雙

載子電晶體的作用可以被利用來改善誤差。

除了實驗外，我們亦推導出一個新的解析式的統計模型。此一模型可以成功地重現在次臨界區對不同元件在不同偏壓下所量測的結果。在此模型中，電流誤差被表達成以製程參數變動為因子的函數。所萃取出的參數變動值與元件面積平方根的倒數成正比，符合前人所提理論。對於在元件面積與誤差間的取捨，我們以一些例子來顯示，以背閘順向偏壓為參數此一模型可被利用來當成一種量化的最佳化設計工具。

Back-Gate Bias Control on Subthreshold Circuit Mismatch and its Physical Model

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Abstract

This thesis investigates the back-gate bias control on subthreshold circuit mismatch as well as its physical model. We have measured the MOSFETS operating in subthreshold (or called weak inversion) to above-threshold regions with different gate widths and lengths. These MOSFETS were characterized with back-gate reverse and forward biases. The first observation is that the devices operating in subthreshold region exhibit larger mismatch than those in above-threshold region. This is due to the exponential dependence of current on gate and bulk voltages as well as process variations. In the case of back-gate reverse bias, we have found that current mismatch increases as the magnitude of back-gate reverse bias increases. This phenomenon is more pronounced in subthreshold region than in above-threshold region. On the other hand, with the supply of back-gate forward bias, the current mismatch deceases

with increasing the back-gate bias in all operation regions. The improvement in match is due to the gated lateral bipolar action in low level injection. With the data measured from devices with different sizes, we have found that small size devices not only exhibit larger mismatch, but also are more sensitive to the back-gate bias. Two suggestions are drawn from the experiment data: (i) subthreshold circuits should be carefully designed to suppress the mismatch; and (ii) the gated lateral bipolar action can be utilized to improve the matching property of MOSFET's.

Besides the experiment, we have also derived a new simple analytical statistical model that has successfully reproduced the mismatch data in weak inversion for different back-gate biases and different device dimensions. With this model, the current mismatch can be expressed as a function of the variations in process parameters, namely, flat-band voltage and body effect coefficient. The extracted variations are shown to follow the inverse square root of the device area. Some examples have been given to demonstrate that the model is capable of serving as the quantitative design tool for the optimal design between the mismatch and device size with the back-gate forward bias as a parameter.

致　謝

轉眼間，兩年的碩士班生活即將接近尾聲，俗話說天下無不散的筵席，儘管心裡面有很多的依依不捨，但是這就是人生，這一階段的結束，代表又是另一階段的開始。

在此要深深感謝在這兩年裡給我幫助、鼓勵與陪伴我的人，首先要感謝我的指導老師陳明哲教授，在這兩年給我指導，並不只是做研究的方法，還有人生的態度、哲學，並且也讓我更加了解物理；接下來要感謝的是我實驗室的夥伴們，呂博與謝博給我專業的指導，阿志、阿貴與阿賢是我的好伙伴兼好戰友，許智育與李韋漢這兩個學弟都很好相處，也給了我不少的建議；另外還有我的朋友們的鼓勵與幫助，都是我的強心劑。

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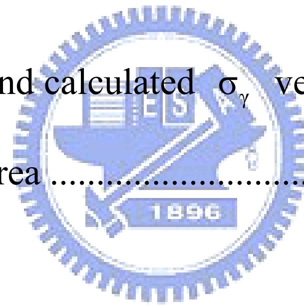

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Chapter 1

Introduction

1.1 Subthreshold Operation

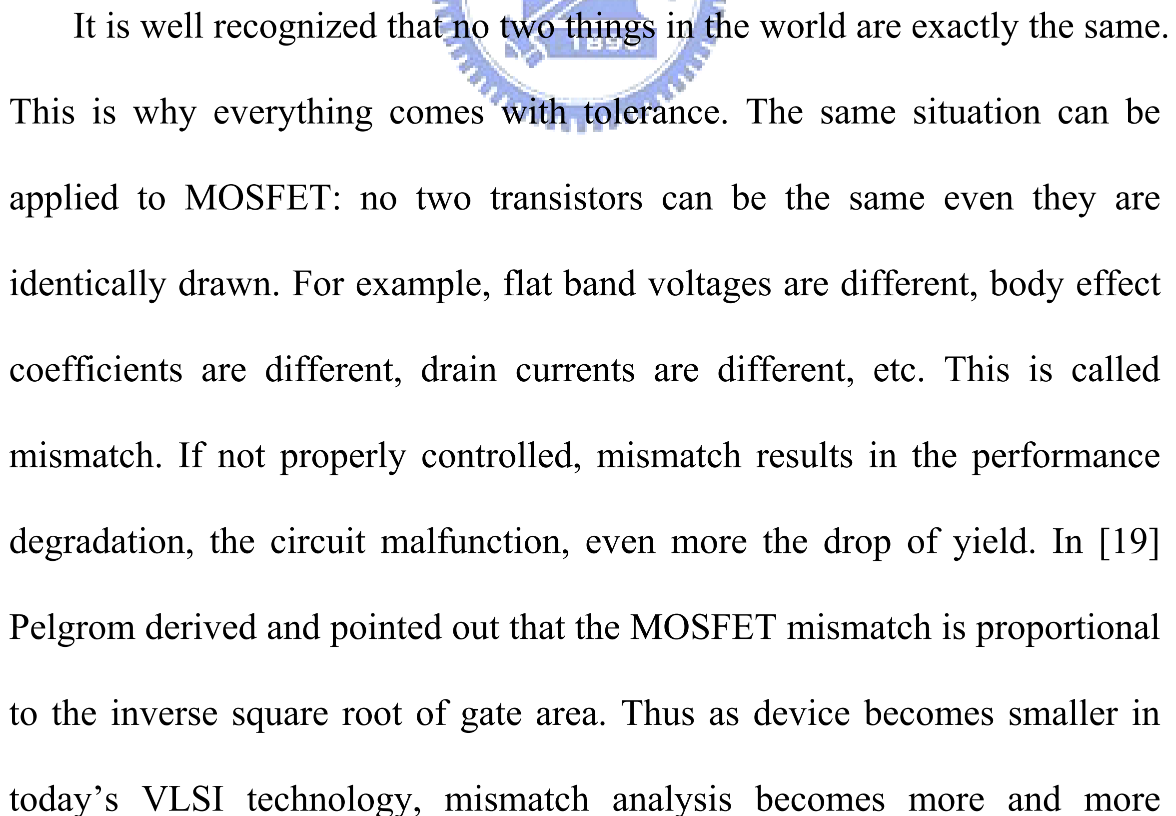
Traditionally the operation of MOSFETs utilizes the above-threshold region, especially the saturation region. In the saturation region, MOSFET is considered as the gate-controlled current source and the current is essentially independent of the drain voltage. On the other hand, subthreshold MOSFET conduction first attracted attention as the leakage current in the early seventies [2]. It is considered as the undesired feature with respect to the normal MOSFET operation and should be eliminated if possible.

In the early eighties, Eric Vittoz [1] suggested that subthreshold conduction of MOSFET can be used as the fundamental element for micropower integrated circuits. As the transistor density continuously grows in VLSI technology, how to reduce the power consumption becomes more and more important. Thus the subthreshold operation of MOSFET is becoming increasingly interesting because of the ability of low power consumption. Many researchers have started to apply the subthreshold characteristics of MOSFET to circuit design [2], [6], [7], [17]. There are

some advantages for operating MOSFET in subthreshold region: (i) extremely low power consumption; (ii) low voltage swing; and (iii) exponential dependence of drain current on gate voltage. In this thesis, we explore some characteristics of MOSFET operating in subthreshold region, such as mismatch application. The threshold voltage can be lowered via the back-gate forward bias, leading to implementation of cost-effective, low voltage, low power CMOS digital integrated circuits with reasonable speed.

1.2 Mismatch Analysis

1.2.1 Device Area and Back-Gate Bias



It is well recognized that no two things in the world are exactly the same. This is why everything comes with tolerance. The same situation can be applied to MOSFET: no two transistors can be the same even they are identically drawn. For example, flat band voltages are different, body effect coefficients are different, drain currents are different, etc. This is called mismatch. If not properly controlled, mismatch results in the performance degradation, the circuit malfunction, even more the drop of yield. In [19] Pelgrom derived and pointed out that the MOSFET mismatch is proportional to the inverse square root of gate area. Thus as device becomes smaller in today's VLSI technology, mismatch analysis becomes more and more

important.

In addition to device area, back-gate bias (or substrate-to-source bias) also plays an important role in the device mismatch. Since device characteristics depend on the back-gate bias, different back-gate bias causes different mismatch [16]. We have reported that back-gate reverse bias worsens the matching property, while back-gate forward bias improves it. Thus during the mismatch analysis we should take both device area and back-gate bias into account simultaneously.

1.2.2 Mismatch in Subthreshold Region

Subthreshold operation is good for low power design as stated above. One of the advantages is the exponential relation between drain current and gate voltage, but this relation is also the cause for large mismatch. In subthreshold operation the device characteristics have the exponential dependencies on process parameters, while in the above-threshold the dependencies follow square rule for saturation operation. Thus it is expected there exists larger mismatch in drain current as compared with that in above-threshold region. Because analog circuits deal with the continuous electrical signal rather than the discrete one as used in digital circuit, mismatch is especially important for analog circuits. Even worse, when the

back gate of the devices is reverse biased, the mismatch increases dramatically for subthreshold operation. Large mismatch means more probable failure, or lower yield. In order to reduce the mismatch effectively, subthreshold circuits usually use much larger area than the above-threshold ones do. However the above statement is only partially correct. As reported in this thesis, with back-gate forward bias we can reduce the mismatch effectively. Thus the disadvantage of larger mismatch and larger area can be compensated by a back-gate forward bias. This makes the subthreshold operation more attractive.

Recently mismatch analysis has attracted more attention and has been applied to circuit design [2]. However, due to present circuit design methodology most of the mismatch analysis works focus on the above-threshold [18]-[20]. The study of mismatch in weak inversion is still limited [2], [3]. In [2], Pavasovic showed that the inverse-square-root formula is still applicable to the subthreshold region; however the effect of the back-gate bias on mismatch is not simultaneously addressed. In [3], only one back-gate is demonstrated, but it clearly shows that back-gate reverse bias increases the mismatch. In this thesis, we extend the mismatch analysis by measuring devices with different gate widths and lengths which are biased in back-gate reverse and forward voltages. Also provided is the

design tool for optimizing the mismatch.

Chapter 2

Experiment of Mismatch

We have extensively measured and analyzed the current mismatch of a miniaturized n-channel MOS transistor operated in weak inversion with its p-well-to-n^+-source junction forward and reverse biased. The case of slightly forward biasing the well-to-source junction represents the action of a gated lateral bipolar transistor in low level injection. The measured dependencies of the mismatch in weak inversion on the back-gate forward and reverse biases have been successfully reproduced by a new simple statistical model. From the experimental data, we suggest that (i) subthreshold circuits should be carefully designed for suppression of mismatch arising from back-gate reverse bias, and (ii) a gated lateral bipolar action in low level injection may be utilized as a new method of improving the transistor matching.

2.1 Introduction

One of the fundamental factors limiting the accuracy of MOS circuits operated in the subthreshold or weak inversion region is the current mismatch between identically designed devices [1]-[2]. It is well known that

owing to exponential dependencies on the process variations, devices operating in subthreshold have a dramatically large mismatch in current as compared with that in the above-threshold region [1]-[4]. This poor control over the current match can cause a number of undesirable effects in the circuit level. Especially, in nanoscale devices, the effects are more and more serious. Traditionally several layout techniques such as making devices large and placing devices close to each other have been proposed for improving the transistor matching [5]. One of the practical examples by employing these techniques in subthreshold circuits can be found in [6], where the minimum size was 6μm × 6μm while the match-sensitive devices needed four to eight times as much area. However, to realize high density subthreshold MOS circuits with high accuracy, an understanding of current match for the small devices as well as match control is very important. In this thesis we will report detailed experimental mismatch data measured from a small-size n-MOSFET with p-well-to-n+-source junction forward and reverse biased. The case of slightly forward biasing the well-to source junction represents the action of an n-p-n gated lateral bipolar transistor in low level injection [7]-[9]. A new simple statistical model will be proposed to quantitatively interpret the observed dependencies of the mismatch on the back-gate reverse and forward biases. Also from our data we will suggest the

gated lateral bipolar action as a new method for improving the matching.

2.2 Experiment

The measurement of current mismatch for identical devices was achieved in terms of the dies on wafer as schematically shown in Fig. 2.1. All dies on wafer contain many n-channel MOS transistors with the same structure. They were fabricated using a 65 nm CMOS process. In our measurement of current mismatch, the p-well-to-n^+-source bias, V_{BS}, was fixed when sweeping V_{GS} from 0 to 1.2 V in a step of 25 mV. The drain currents were measured and recorded for subsequent analysis. This procedure was repeated for each V_{BS} varying from 0.4 V to 0 V as well as from 0 V to -0.8 V. The choice for the maximum forward bias V_{BS} of 0.4 V is to guarantee the action of the gated lateral bipolar transistor [7]-[9], as interpreted later. The measurement setup contained the HP4156B and a Faraday box for shielding the test wafer, all performed in an air-conditioned room with the temperature fixed at 298 K. The total measurement time of one die's n-channel MOS for these full ranges was about 3 hours. A total of **25** sample size was measured in one die. Fig. 2.2 depicts typical measured I-V characteristic with V_{BS} as a parameter from a single n-channel MOSFET. In Fig. 2.2 the operating regime of the interest in the work, i.e., weak

inversion, is the range of $V_{GS} > 0$ and $I_D < 10^{-8} \sim 10^{-7}$ A depending on the deviations from the exponential I-V relationship as will be clearly described later. The corresponding I-V curves are plotted in Fig. 2.3 for three different V_{BS} values of 0.4, 0, and -0.8V. It is clearly seen from Fig. 2.3 that (i) the back-gate reverse bias causes a relatively large spread in the I-V characteristics; and (ii) for fixed V_{BS} the spread decreases as the current increases. The statistical analysis of the our data in Fig. 2.3 is described in detail in next chapter.

Chapter 3

Dependence of Current Match on Back-Gate Bias

3.1 Analysis and Modeling

The drain current mismatch σ_{I_D} is defined as $\sigma_{I_D} = I_{D\ (SD)} / I_{D\ (mean)}$ where $I_{D\ (mean)}$ and $I_{D\ (SD)}$ are the mean and SD (standard deviation) of drain current for all the same dimensions of n-channel MOSFETs. We can calculate the mean and SD by means of a statistics tool. Fig. 3.1 shows the histogram of the drain current for different V_{BS} as a parameter. From Fig. 3.1 we can observe that (i) for given V_{BS} the distribution of I_D; (ii) the distribution broadens as V_{BS} varies from 0.4 V to -0.8 V.

Fig. 3.2 shows the data in terms of σ_{I_D} versus I_D for zero V_{BS}, where W/L is the gate width to length ratio. In Fig. 3.2 our data from three dimensions are plotted for comparison. Further investigation of Fig. 3.2 reveals that the mismatch in weak inversion decreases with increasing the device area. However, this dependence must be scaled to account for process variations. Also from Fig. 3.2 it can be seen that, over all weak inversion current densities, the mismatch is essentially independent of current. In the moderate and strong inversion regions the mismatch significantly rolls off.

The reasons for such dependencies are given in the following. In subthreshold the threshold voltage V_{th} affects exponentially the drain current I_D through the following expression [1], [2], [4], [13]:

$$I_D \propto e^{-\frac{q}{kT}\frac{V_{th}}{n}} \qquad (3.1)$$

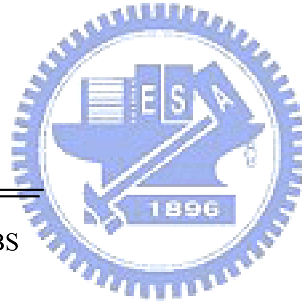
where V_{th} can be written as [13]:

$$V_{th} = V_{FB} + 1.5\phi_f + \gamma\sqrt{1.5\phi_f - V_{BS}}$$

$$\phi_f = \frac{kT}{q}\ln(\frac{N_A}{n_i})$$

$$\gamma = \frac{t_{ox}\sqrt{2q\varepsilon_{si}N_A}}{\varepsilon_{ox}}$$

$$n = 1 + \frac{\gamma}{2\sqrt{1.5\phi_f - V_{BS}}}$$



where V_{FB} is the flat-band voltage; N_A is the effective well doping concentration; n_i is the intrinsic concentration; t_{ox} is the oxide thickness; and ε_{si} and ε_{ox} are the silicon and oxide permittivities, respectively. According to (3.1), the variations in the fabrication process through N_A, t_{ox}, and V_{FB} cause a change in V_{th}, which in turn produces an exponential change in I_D. However, in the above-threshold region the dependence of the drain current on the threshold voltage is turned to the well-know polynomial form, i.e.,

$$I_D \propto V_{DS}(V_{GS} - V_{th}) \quad \text{or} \quad (V_{GS} - V_{th})^2 \qquad (3.2)$$

Therefore in the above-threshold region the variation in I_D is a weak function of the variation in V_{th} as compared with the exponential change in weak inversion.

The measured mismatch as a function of the bias V_{BS} is given in Fig. 3.3. It is noted from Fig. 3.3 that in the weak inversion region the mismatch increases with increasingly negative V_{BS} (from 0 V) and decreases with increasing the forward bias V_{BS}. Such significant change is not as noticeable as the current enters the moderate and then strong inversion regions. This is because the corresponding dependence of drain current on the voltage changes from the exponential (3.1) to the polynomial (3.2). Note that a mathematical technique combining (3.1) and (3.2) as originally proposed in [14] can be utilized to empirically smooth the I-V characteristics of the transition region.

Now we propose a new simple statistical model to quantitatively account for the above observed dependencies of the mismatch in weak inversion on the well-to-source bias. As revealed by (3.1), the our observed mismatch as a function of the V_{BS} can be attributed to the variations in the oxide thickness t_{ox}, the doping concentration N_A, and the flat-band voltage V_{FB}. For simplifying the derivation, we consider the body effect γ, which contains t_{ox} and N_A, as a single parameter responsible for the variations in

both t_{ox} and N_A. The variation in oxide charges and charged interface traps can essentially be reflected by the variation in the single parameter V_{FB}. The validity of this procedure can be verified experimentally later. Assuming no correlation between parameters, from (3.1) the variance of the current different, σ_{I_D}, can be derived as function of both the variance of the difference in the body effect coefficient, σ_γ, and the variance of the difference in the flat-band voltage, $\sigma_{V_{FB}}$, [15]:

$$\sigma_{I_D}^2 \cong \left(\frac{\gamma}{nV_T}\right)^2 (1.5\phi_f - V_{BS})\sigma_\gamma^2 + \left(\frac{V_{FB}}{nV_T}\right)^2 \sigma_{V_{FB}}^2 \qquad (3.3)$$

where V_T (=KT/q) is the thermal voltage. This new formulation explicitly describes the dependence of σ_{I_D} on V_{BS}, i.e., the current mismatch increases with increasingly negative reverse bias V_{BS}, while an increase in the forward bias V_{BS} can improve the transistor matching. The calculated results based on (3.3) with σ_γ = 2.767 % and $\sigma_{V_{FB}}$ = 1.018 % have been found to be capable of appropriately reproducing the measured data as depicted in Fig. 3.4. The corresponding parameter values t_{ox}, V_{FB}, and N_A as provided by the experiment's extract, which are also utilized later for identifying the regime of the gated lateral bipolar action in low level injection. From the above analysis and modeling, we can conclude that the mismatch becomes worse

with the back-gate reverse bias applied and the current match can be substantially improved by slightly forward biasing the well-source junction.

3.2 Detailed Interpretations

Based on the above results, we suggest utilization of a MOS transistor with its well-to-source junction slightly forward biased or equivalently a gated n-p-n lateral bipolar transistor in low level injection [8]-[10] in order to improve the matching in the weak inversion region. Now we give interpretations for the action of the gated lateral bipolar transistor. Fig. 3.5 shows the drain current versus gate bias characteristics with forward bias V_{BS} as parameter measured from one single n-channel MOSFET. According to our work [9]-[10], the measured I-V characteristics in Fig. 3.5 can be separated into two distinct regions: (i) the weak inversion region; and (ii) the strong inversion region. The condition for the surface inversion is $V_{GS} - V_{BS} > V_{th}$. Under this condition the opposite-polarity charges are induced at the surface beneath the gate and thus the drain current is dominated by drift component. The operating region of interest in this chapter is $0 < V_{GS} < V_{th} + V_{BS}$. In this region the surface emitter(source)-base(well) junction barrier beneath the gate is lowered and almost all the injected electrons flowing toward the drain(acting as a

collector) are limited to the surface depletion region [8]-[10], indicating that the pure bipolar collector current (which appears only for $V_{GS} < 0$) is relatively negligible. The drain (or collector) current in the regime of $0 < V_{th} + V_{BS}$ can be accurately described by [9]:

$$I_D = I_0 e^{\frac{q(\varphi_C + V_{BS})}{kT}}$$
$$\varphi_C = \frac{\gamma^2}{2} + (V_{GS} - V_{BS} - V_{FB}) - \frac{\gamma}{2}\sqrt{\gamma^2 + 4(V_{GS} - V_{BS} - V_{FB})} \quad (3.4)$$

where φ_C represents the surface potential for lowering the emitter-base junction barrier. In (3.4) the potential lowering is expressed as function of the process parameters such as the well doping concentration, the work function difference, and the gate oxide thickness as well as of the electrical parameters such as V_{GS} and V_{BS}. Note that the subthreshold current expression (3.3) can be derived from (3.4) using the Taylor series expansion [13]. Eq. (3.4) clearly reveals that the potential barrier can be lowered by the surface potential through the gate bias control, which causes an exponential change in the drain current.

Note that the pure lateral bipolar action in a MOS transistor with well-to-source junction forward biased has also been reported in [11], [12] for improving the matching. However, the our operating condition and the mechanism responsible both are completely different from those in [11], [12];

that is, in our work the pure lateral bipolar transistor action is relatively negligible since the surface carrier diffusion dominates the drain current, while in [11], [12] the pure lateral bipolar transistor action is totally responsible as cited there. Accurate comparisons can be presented in the following: (i) in [11], [12] the polarity of the V_{GS} is negative while in our work it is positive; and (ii) in [11], [12] the pure lateral bipolar action occurs at $V_{BS} > 0.3 - 0.4$ V while in our work the gated lateral bipolar action appears in low level regime of $0\ V < V_{BS} < 0.4V$.

3.3 Mismatch Model

According to [15], the variance or standard deviation $\sigma_{g(x,y)}$ of a function g(x,y) with two random variables x and y can be expressed as

$$\sigma^2_{g(x,y)} \cong (\frac{\partial g}{\partial x})^2 \sigma^2_x + (\frac{\partial g}{\partial y})^2 \sigma^2_y + 2(\frac{\partial g}{\partial x})(\frac{\partial g}{\partial y}) C_{ov}(x,y) \quad (3.5)$$

where σ_x and σ_y are the variances of x and y, respectively; and $C_{ov}(x,y)$ is the correlation coefficient between x and y. Thus the mismatch of the difference in the drain current I_D can be written as function of the variances in the associated process parameters:

$$\sigma^2_{I_D} \cong (\frac{\gamma}{nV_T})^2 (\frac{\partial V_{th}}{\partial \gamma})^2 \sigma^2_\gamma + (\frac{V_{FB}}{nV_T})^2 (\frac{\partial V_{th}}{\partial V_{FB}}) \sigma^2_{V_{FB}} \quad (3.6)$$

where σ_{I_D}, σ_γ and $\sigma_{V_{FB}}$ are the coefficient of variance of the difference in the I_D, the body effect coefficient γ, and the flat-band voltage V_{FB}, respectively. To facilitate the analysis, we assume $C_{ov}(V_{FB},\gamma) = 0$. This is a basic assumption in the field [18]-[20] since the process variations are independent of each other in nature. Note that the variations in the gate oxide thickness t_{ox} and channel effective doping concentration N_A are simultaneously reflected in the single parameter γ since γ includes both t_{ox} and N_A, i.e. $\gamma = t_{ox}\sqrt{2q\varepsilon_{si}N_A} / \varepsilon_{ox}$ where ε_{si} and ε_{ox} are the silicon and oxide permittivities, respectively. The following weak inversion current expression is considered for the derivation of the model [16]:

$$I_D = A\, e^{-\frac{q}{kT}\frac{V_{th}}{n}} \tag{3.7}$$

$$\ln I_D = \ln A - \frac{1}{V_T}\frac{V_{th}}{n}$$

where the critical voltage $V_{th} = V_{FB} + 1.5\phi_f + \gamma\sqrt{1.5\phi_f - V_{BS}}$; the Fermi level $\phi_f = \frac{kT}{q}\ln(\frac{N_A}{n_i})$; the slope $n = 1 + \frac{\gamma}{2\sqrt{1.5\phi_f - V_{BS}}}$; and n_i is the intrinsic concentration. From (3.7) the derivatives in (3.6) can easily be derived:

$$\frac{\partial V_{th}}{\partial \gamma} = \sqrt{1.5\phi_f - V_{BS}} \tag{3.8}$$

And

$$\frac{\partial V_{th}}{\partial V_{FB}} = 1 \tag{3.9}$$

Thus we obtain a compact model:

$$\sigma_{I_D} \cong \sqrt{\left(\frac{\gamma}{nV_T}\right)^2 (1.5\phi_f \text{-} V_{BS})\sigma_\gamma^2 + \left(\frac{V_{FB}}{nV_T}\right)^2 \sigma_{V_{FB}}^2} \tag{3.10}$$

Apparently, (3.10) analytically expresses the current mismatch in weak inversion as function of the coefficient of variance of the difference in V_{FB} and γ.

Fig. 3.6(a) shows four different gate width with the same length and Fig. 3.6(b) shows the same width with three different length for the coefficient of variance σ_{I_D} versus I_D.

Fig. 3.7 shows the measured drain current mismatch in weak inversion versus the back-gate bias with seven different dimensions.

From Fig. 3.8(a) and (b) we can observe that the coefficient of variance in V_{FB} and γ each effectively follow the inverse square root of the device area, in agreement with [18], [19]. Thus empirically we have

$$\sigma_\gamma = \frac{A_\gamma}{\sqrt{WL}} \quad \text{and} \quad \sigma_{V_{FB}} = \frac{A_{V_{FB}}}{\sqrt{WL}} \qquad (3.11)$$

where A_γ and $A_{V_{FB}}$ are the size proportionality constants for σ_γ and $\sigma_{V_{FB}}$, respectively. The extracted values lead to A_γ = 0.013464μm and $A_{V_{FB}}$ = 0.006441μm. Therefore, a combination of (3.10) and (3.11) can serve as an analytic design tool for properly calculating the mismatch with back-gate forward bias and device size both as input parameters.

Chapter 4

Conclusion

The current mismatch of a small gate area n-channel MOS transistor with its well-to-source junction forward and reverse biased has been extensively measured and analyzed. The n-channel MOS transistor with well-to-source junction slightly forward biased acts as a gated lateral bipolar transistor in low level injection. Our measured mismatch data for zero back-gate bias are close to the existing ones with comparable size. The measured data exhibit important observations: (i) back-gate reverse bias can make worse the mismatch in current; and (ii) current match can be substantially improved by the gated lateral bipolar action. The measured dependencies of the mismatch on the well-to-source forward and reverse biases have been successfully reproduced by a new simple statistical model.

The new simple mismatch model has successfully reproduced the extensively measured data. The extracted variations in the associated process parameters have been found to follow the inverse square root of the device area. The work of optimizing the trade-off between the match and the device size with back-gate forward bias as design parameter has been demonstrated based on the model.

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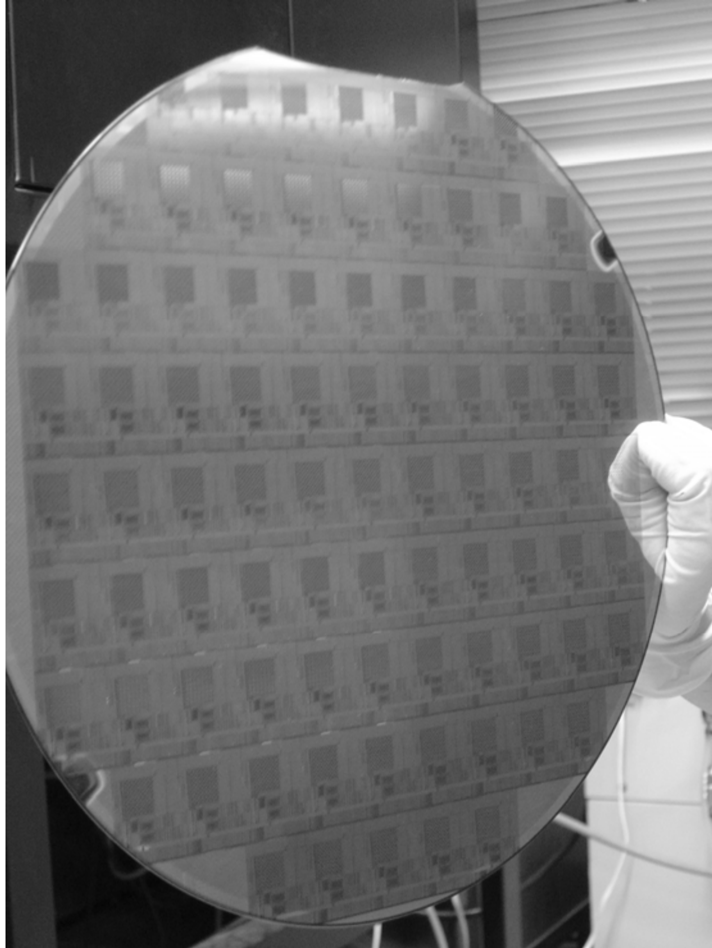

Fig. 2.1 The used dies on wafer. All dies on wafer contain many n-channel MOS transistors with the same structure.

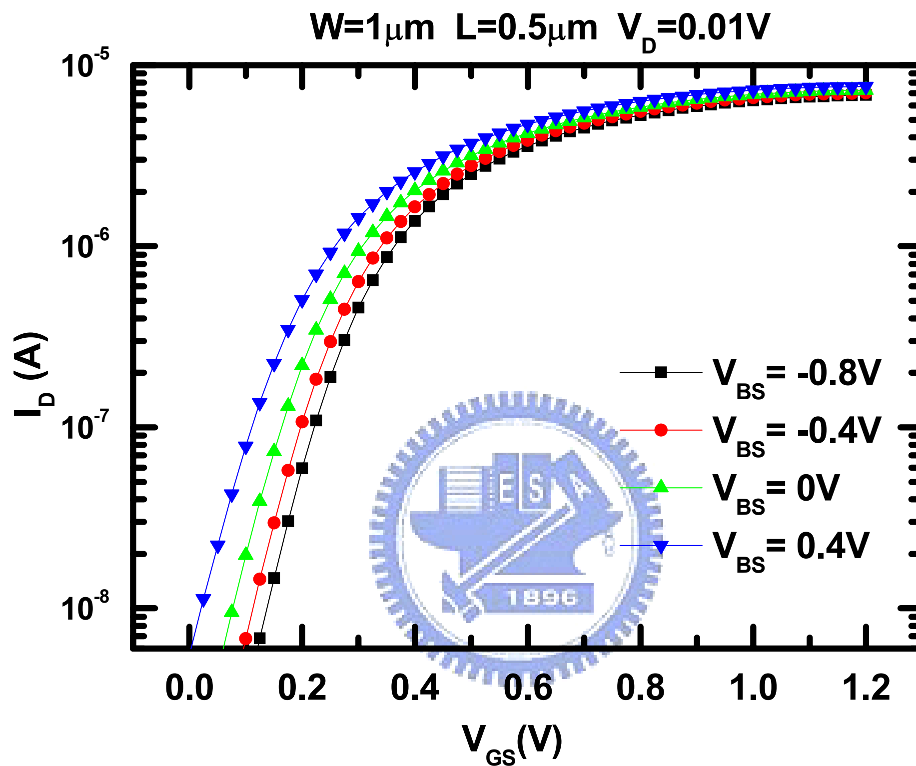

Fig. 2.2 The drain current versus gate voltage characteristics with back-gate bias as parameter from one of 25 n-channel MOSFETs in one die.

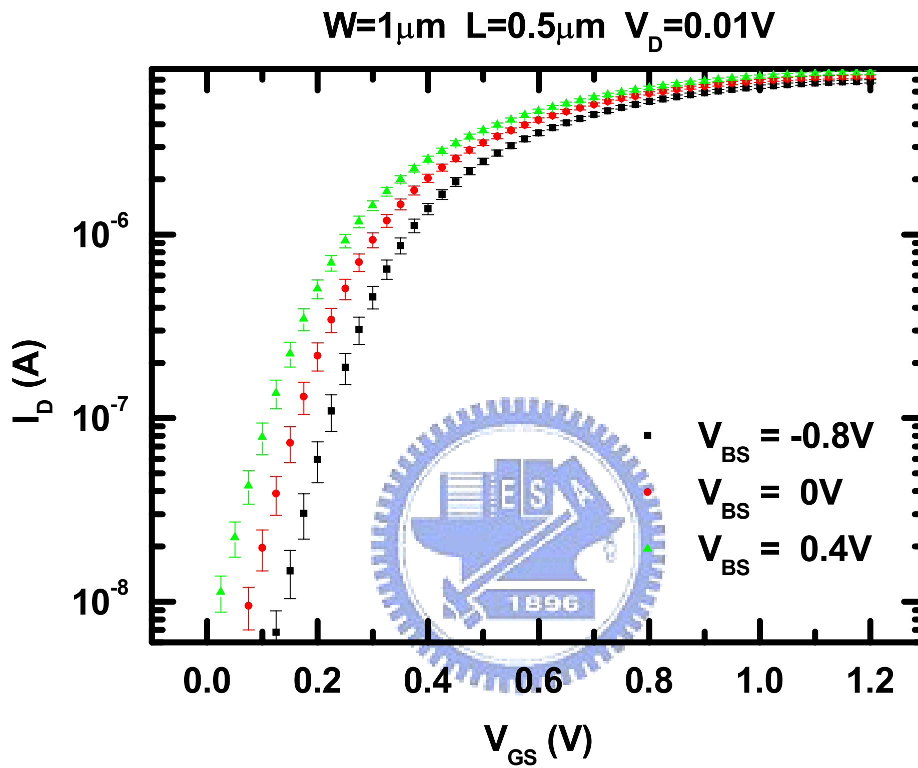

Fig. 2.3 The measured drain current versus gate voltage characteristics for three different back-gate biases.

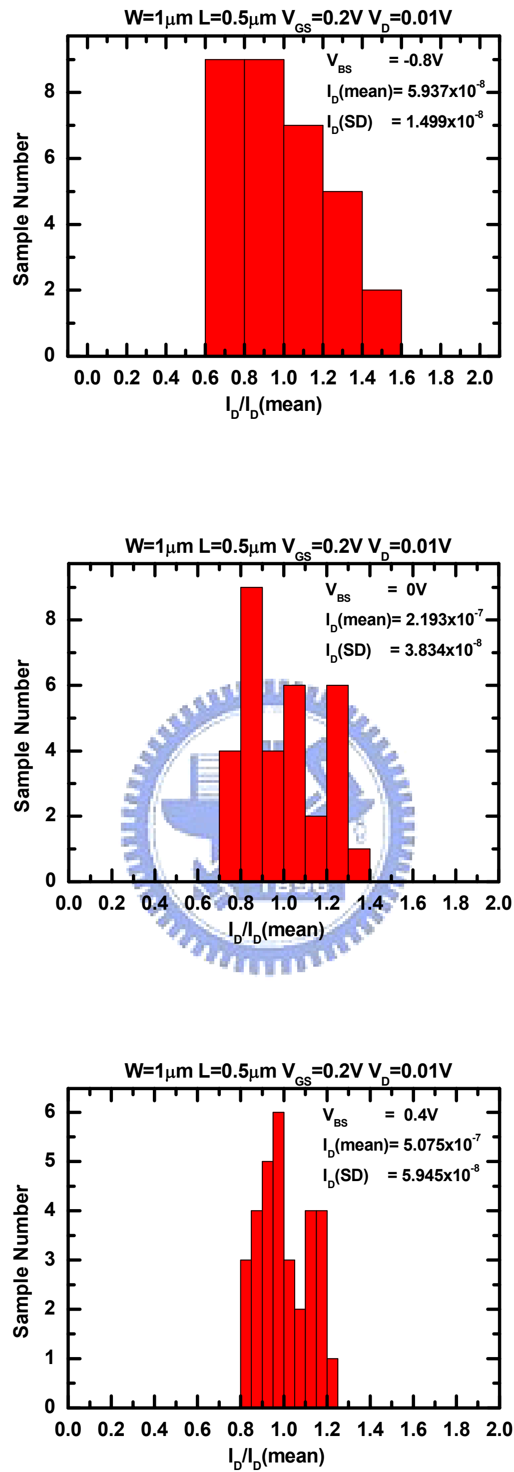

Fig. 3.1 The histogram for the NMOSFET dimension W/L = 1μm/0.5μm with three different V_{BS}.

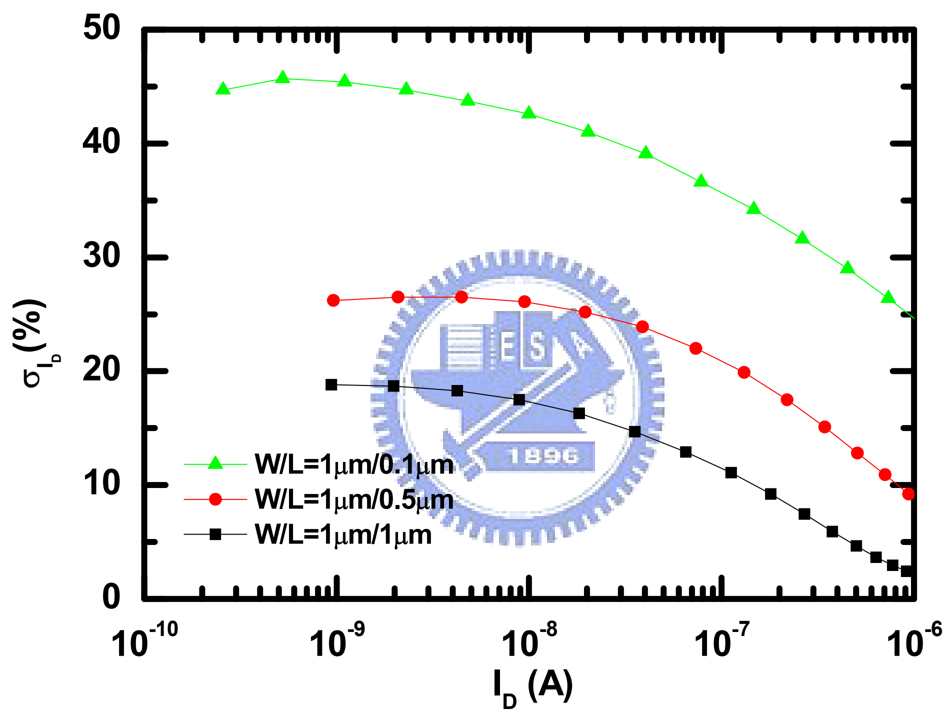

Fig. 3.2 The σ_{I_D} versus the drain current for zero back-gate bias.

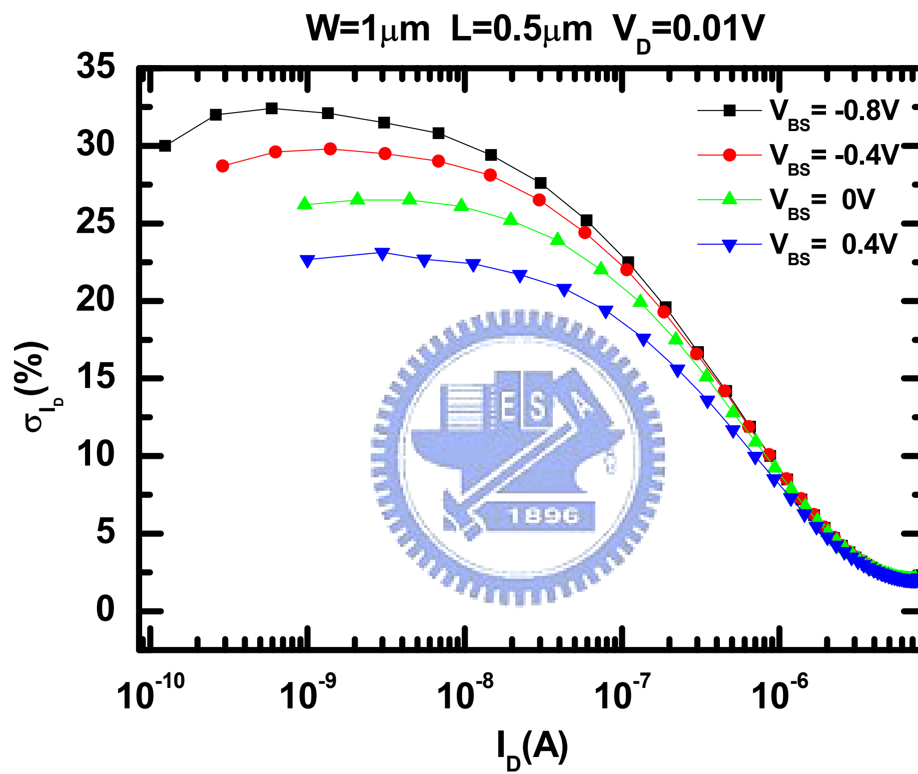

Fig. 3.3 The measured drain current mismatch versus the drain current with the back-gate bias as parameter.

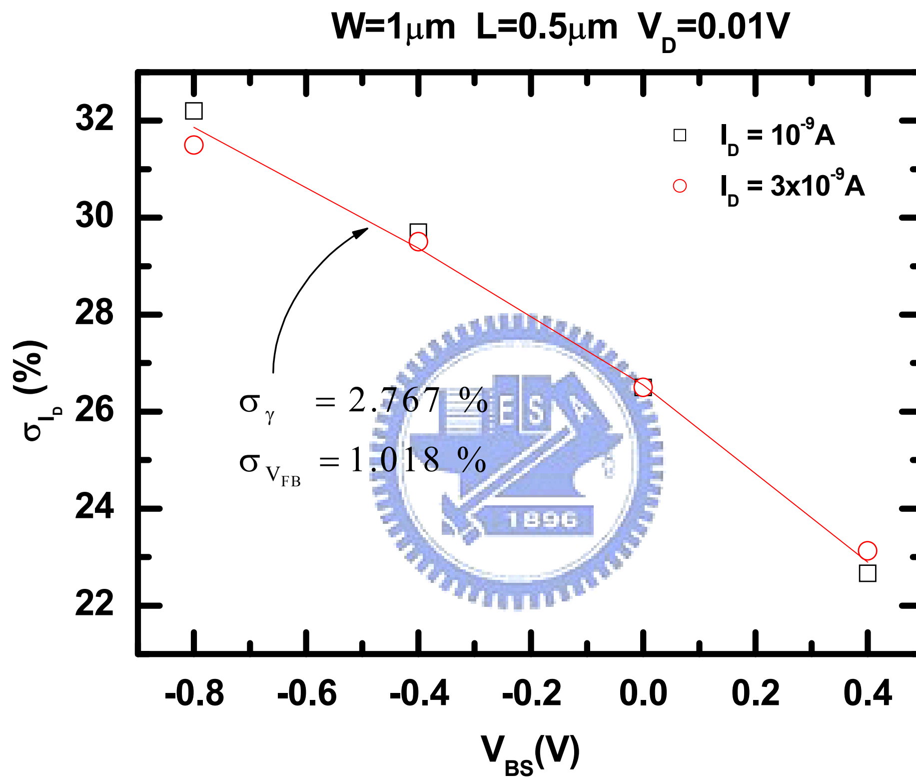

Fig. 3.4 The measured drain current mismatch in weak inversion versus the back-gate bias for two different drain currents. The calculated results from Eq. (2.4) are also shown for comparison.

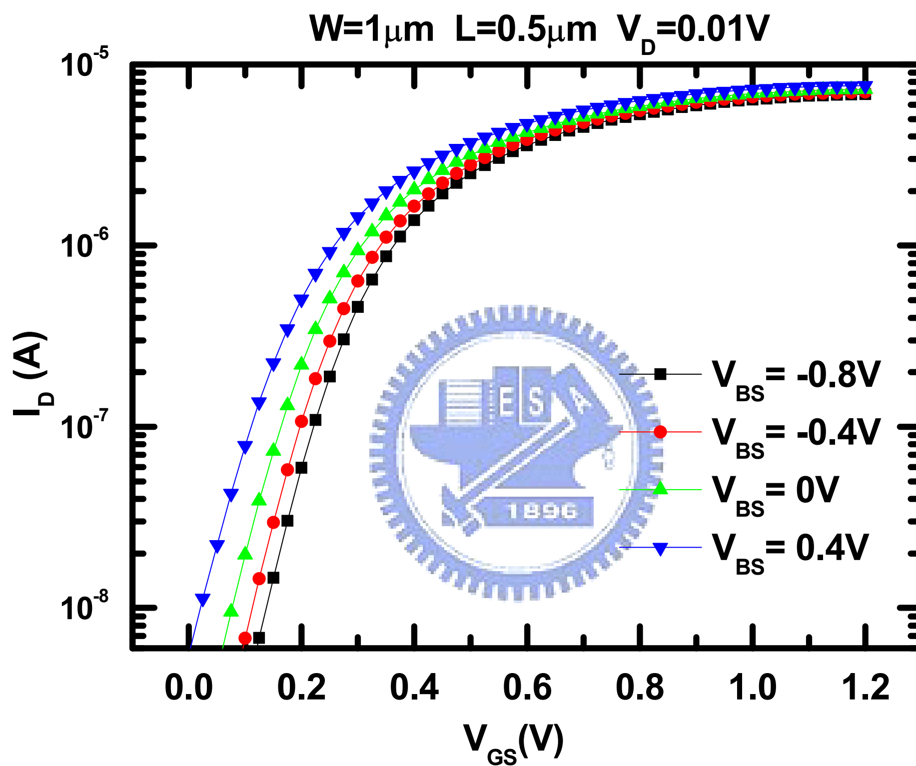

Fig. 3.5 The drain current versus gate voltage characteristics with back-gate bias as parameter.

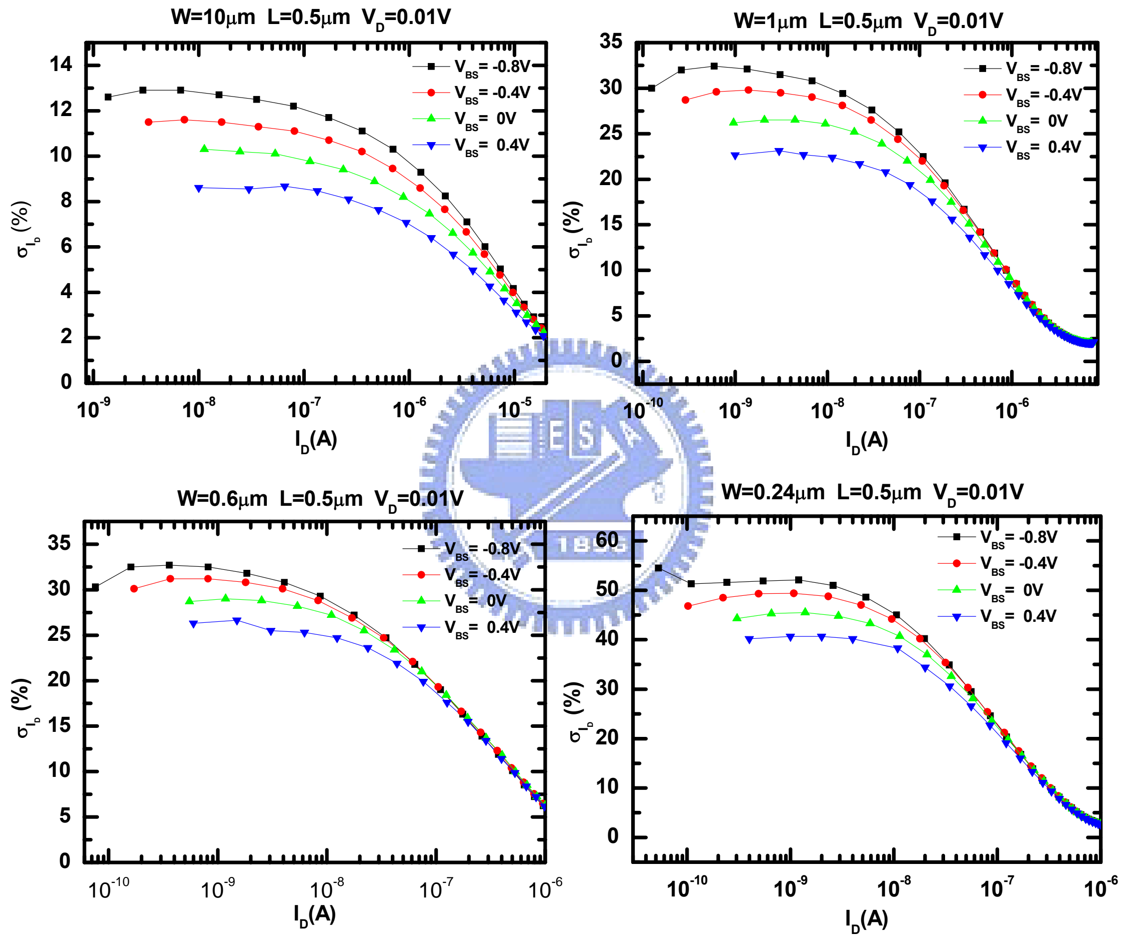

Fig. 3.6(a) Four different gate width with the same length for the coefficient of variance σ_{I_D} versus I_D.

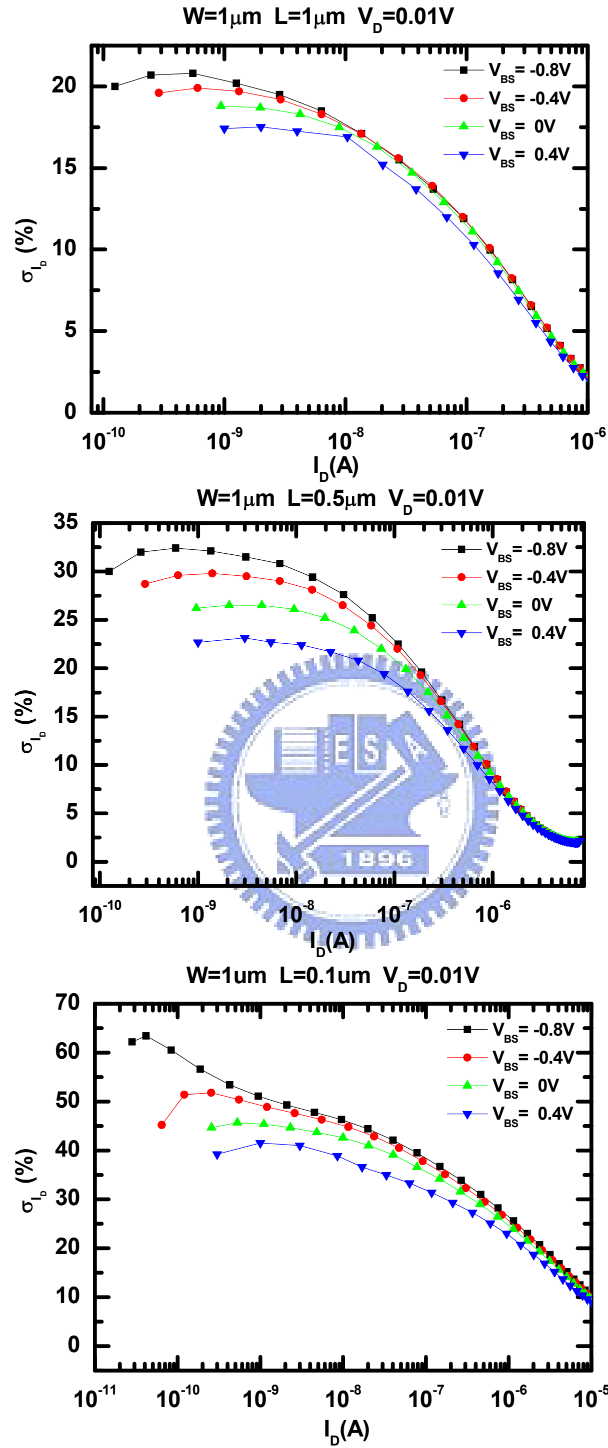

Fig. 3.6(b) The same width with three different lengths for the coefficient of variance σ_{I_D} versus I_D.

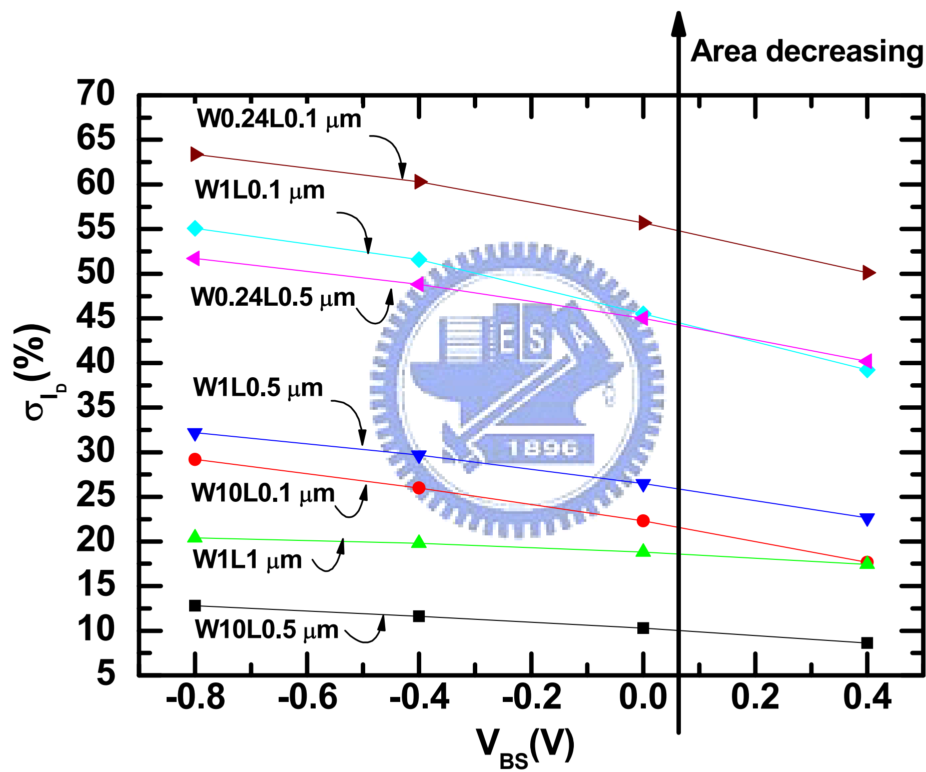

Fig. 3.7 The measured drain current mismatch in weak inversion versus the back-gate bias with seven different dimensions.

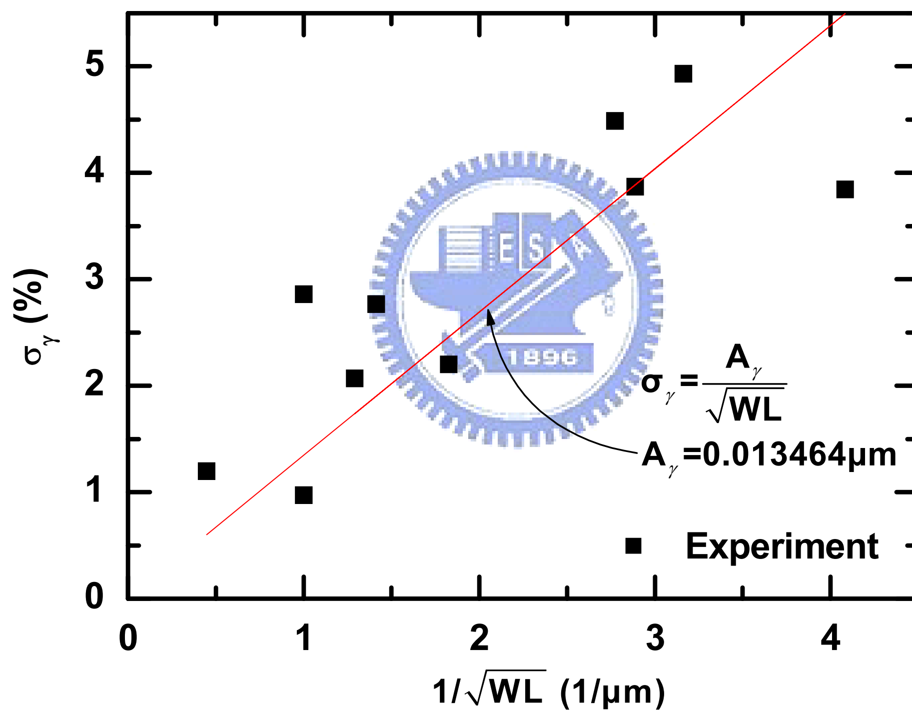

Fig. 3.8(a) The measure and calculated σ_γ versus the inverse square root of the device area.

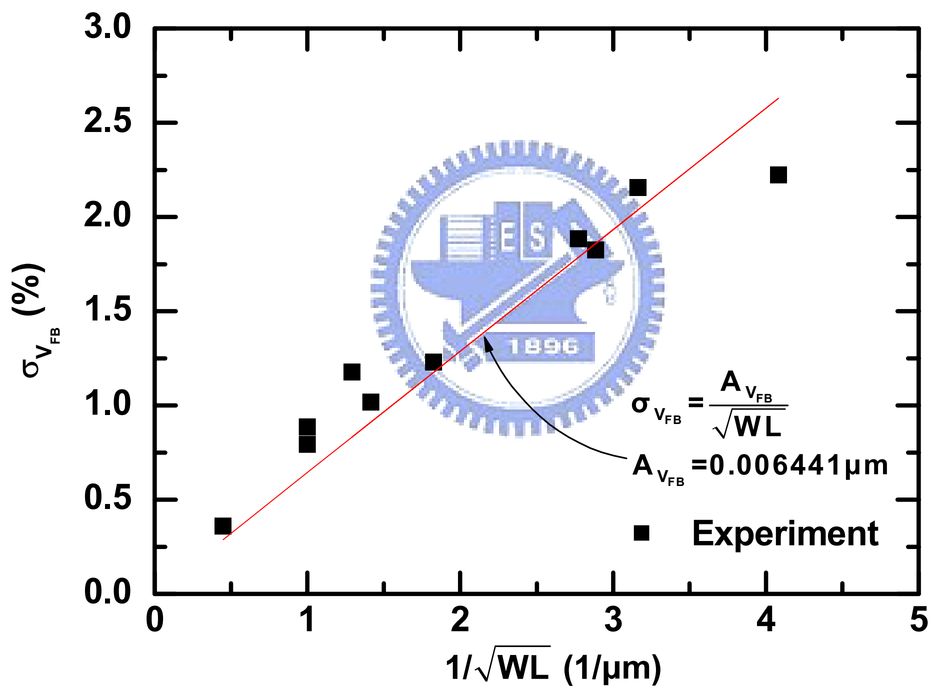

Fig. 3.8(b) The measure and calculated $\sigma_{V_{FB}}$ versus the inverse square root of the device area.