國立交通大學

電子工程學系 電子研究所

博士論文

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低溫活化下形成的接面研究

A Study of Low Temperature Activated Junction Formed by Implant Into Silicide Method

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中文摘要

隨著元件尺寸的微縮，為了確保元件的良好表現，有許多新的材料被導入元件的製程。然而這些新材料的熱穩定性並不十分一致，導致製程整合的複雜化。有些在其他特性表現不錯的材料也因此不被採用。究其原因，離子植入後的高溫活化是製程整合上的主要瓶頸。離子佈植進入矽合金法是一種能在低溫下活化載子的方法。本篇研究主要著重利用離子佈植進入鎳矽合金法在低溫活化形成的接面特性的相關研究。

第一部分，我們想研究低溫活化的可能機制。首先我們藉由製作金屬半導體二極體的測試結構，量測在不同的活化條件下，載子活化的情形，確認了低溫活化下，在金屬和半導體接面的載子具有相當高的活化程度。藉由此部分的研究成果，讓我們可以接著去設計實驗來觀察並且分析利用此離子佈植入鎳矽合金法在低溫活化形成的 PN 接面。接著，我們分析了深淺兩種不同的佈植深度所形成的接面行為的變化差異，提出了三個離子佈植入鎳矽合金法的在低溫活下可能的活化機制，包含了金屬促發的再結晶，固態長晶再結晶，以及基材本身活化。

第二部分，我們想對藉由離子佈植入鎳矽合金法形成之接面特性做進一步的了解。首先，根據第一部分的研究結果，為了研究 very shallow junction，我們降低了植入載子的濃度，觀察並且記錄了相關的電特性且與先前的高離子佈植的元件比較。接著，導入了第三段的熱製程溫度，觀察了元件的熱穩定度特性。藉由交叉比對實驗結果，我們對於該元件的製作和量測方法提出了我們的觀點。

A Study of Low Temperature Activated Junction Formed by Implant Into Silicide Method

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Abstract

Many new materials have been introduced to ensure the device with high quality as their physical lengths are scaled down. However, some materials may not have good thermal reliabilities, hence making the process integration more and more complex. As the result, some materials may have good characteristics in many aspects, but they couldn't be adapted to the fabrication process. The highest temperature appears in device fabrication is the dopant activation step after implantation and this step dominates the thermal reliability requirement for all materials. Implant into silicide method is one possible method to activate dopant at low temperature. And in this study, we focus on the characteristics of junction formed at low activation temperature by using implant into nickel silicide method.

In Part I, we want to clarify the possible mechanism that active the dopant at low temperature. At first, we fabricated Metal Semiconductor diode (MS diode) test structure at different activation conditions. By measuring and analyzing the dopant activation abilities of MS diodes formed at different conditions, we confirm the factor that even at low temperature activation, the dopant at the MS interface also has high activation ability. Based on this result, we can go a step further to design an experiment to observe and analyze behaviors of junction formed by the implant into nickel silicide method. Then, by comparing different behaviors of junctions (deeper and shallow) with two implantation energies, we proposed three possible corresponding dopant activation mechanisms at low temperature to the implant into nickel silicide method. Which includes doping activation at metal assisted re-crystallization region, solid phase regrowth region and bulk activation region. In part II, we want to understand characteristics of the junction formed by IIS method further. By the experimental results in Part I, for very shallow junction fabrication, we lowered the implantation dosages and then we record relative electrical properties and also compare results to the heavily implanted samples. Then, an added thermal treatment is adapted to explore the thermal reliability issue of these devices. By cross comparing experimental results, we proposed our viewpoints of the IIS method.

誌謝 (Acknowledgement)

寒夜客來茶當酒 風雨飄搖故人情

算算在交大的日子，連同碩士班一起，也過了六年。六年來的點滴，也讓我在固態電子的領域，從一片荒蕪，也慢慢的長出了一片綠地。首先，要感謝指導教授張國明老師的提攜，沒有老師的接受和鼓勵，我是不可能進入到這個領域。在我進入碩士班後，謝謝許鉦宗老師，游凱翔博士的幫忙，讓我的研究視野，能有進一步的拓展。上了博士班以後，張老師也總在後面默默的付出指導，幫忙的找資源，提供可以思考的方向，但從來不阻止學生的研究興趣。不怕學生犯錯，鼓勵學生從荊棘叢中走出一條屬於自己的道路。謝謝老師的教誨。

上了博士班後，尋找屬於自己能發揮的一小塊立足點，謝謝孫成業、楊志祥、林勝軍、林詩帆和張庭嘉幾位學弟，一同在實驗上的幫忙，讓我的論文和實驗可以順利的進行和完成。學弟，謝謝你們。

當我由學弟的角色，逐漸的變成博士班高年級的學長，也開始常常會聽到實驗室不同研究領域的學弟，問起各式不同的問題。除了拓展了我的視野外，幾年下來，面對不同研究的問題，只能在基本的原理原則下，嘗試的去解構不同情境下的問題的成因，再架構出比較可能比較可行的方向。在不斷的重新解構和架構下，抓重點的能力慢慢的也被培養了起來，古人說的教學相長，真的是很有道理。這也是我們實驗室博士班訓練中很有特色，我也很喜歡的一個地方。那些在我被自己研究數據和實驗忙的焦頭爛額下還敢來問我問題的學弟們，也謝謝你們。

相逢即是有緣，所有實驗室的成員讓我這六年來度過的相當愉快。特別感謝柏寧和士軒，總是在同一陣線上相互支持，也祝福你們早日完成研究。

論文的完成，實驗上，感謝所有奈米中心的技術員，以及國家毫微米實驗室的工作人員們的幫忙。研究就像瞎子摸象，感謝口試老師們幫忙來調整這隻大象的外觀，讓他越來越有樣子。還幫忙修改了論文中學生在許多細節上犯下的錯誤，謝謝所有的老師。

最後，感謝我的家人和女朋友，因為你們，才讓這一刻充滿歡喜。謝謝你們。

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Chapter 1

INTRODUCTION

1.1 General Background

Both shallow junction and high-k dielectric formation are important issues for manufacture of CMOS devices beyond the 45nm generation [1]. For ohmic contact consideration, traditional junction formation technology at source and drain (S/D) regions requires high temperature annealing (i.e. RTA 1000℃ 30s), but this high-temperature process will affect not only the original dopant concentration profile but also make some high-k dielectric crystallized [2,3]. For device integration consideration, there are many studies devotes to improve high-k dielectrics thermal reliability, including stack structure, mix materials, plasma treatments and introducing new materials. On the other hand, low temperature activation technique provides an alternative possibility to give solutions to these two difficulties.

1.2 Low Temperature Activation Techniques at S/D Regions

To date, there are three main techniques proposed for low temperature dopant activation, which are Solid Phase Epitaxial Regrowth (SPER) [4,5], Dopant Segregated Schottky junction (DSS) [6,7], and Implant Into Silicide (IIS) [8,9]. We will give a brief introduction to these three techniques at below:

1.2.1 Solid Phase Epitaxial Regrowth

The fabrication process about SPER technique is pre-amorphous crystal silicon to amorphous type and then implanting dopant. Main dosages will remain in the amorphous region and when activation process is performed, effective dopant activation will be achieved only to the dopant in the amorphous region. The most important concept for why the SPER process could achieve relative low temperature activation (most around the process window 700 to 800℃) is that dopant in amorphous silicon could activated at the density above the density of their thermal equilibrium solubility in the crystalline silicon [4]. However there are still two drawbacks about the SPER process. First, despite the thermal budget control for SPER, the main parameter should be considered for SPER process is the pre-amorphous depth. From the viewpoint of device fabrication, the pre-amorphous depth determines the junction's depth. For properly junction depth controlling consideration, a high cost low energy ion implanter is required. Secondly, to fully remove the implantation damage, a relative high thermal budget process [5], higher than activation itself required, is preferred. However, this high temperature process is not easy to control, if this regrowth process does not control well, there will be a negative impact to the junction performance. The implantation damage annealing process will limit the SPER's process window.

1.2.2 Dopant Segregated Schottky Junction

The fabrication process about DSS technique [6,7] is (a) pre-activation dopant in silicon by traditional method or SPER technique, and (b) change/control the junction from silicon p-n junction, i.e. p^+/n junction, to the silicide/p^+/n junction. The final junction depth of DSS technique is the silicide thickness plus the diffused junction depth which depends on the silicidation process. The DSS technique takes the advantage over traditional junction fabrication process by three factors. First, dopant segregation phenomenon at silicide/silicon interface will cause dopant piled up at the interface, this factor will increase the effective dopant concentration of the heavily doped junction. Secondly, the heavily doped region is well confined at a few nano-meter from the silicide interface. Thirdly, the thermal budget for silicidation process could below 700℃(depends on the material of silicide source), it is a low temperature process. Since the thermal budget of silicidation technique is lower than that of SPER process, it seems that the DSS method has lower thermal budget when compared with SPER process. However, since the DSS technique is used to fabricate the S/D regions of the MOS device, it needs to meet the spec of the MOS device at the S/D side, shallow junction. Although the final junction depth determined by silicidation process, the original junction depth is also very important. This is because DSS method must let the original activated junction fully reacted to become silicide, which means that, for well shallow junction controlling, the DSS method must base on the SPER process. As the result, the determination thermal budget for the DSS technique is the same as for the SPER process.

1.2.3 Implant Into Silicide

On the other hand, Implant Into Silicide technique provides an extremely simple process. IIS method forms junction without any additional steps or new manufacturing systems compared to the conventional junction formation process, instead, it just changes the sequence of the junction fabrication steps. As shown in Fig. 1.1, conventionally, silicidation is processed after the S/D junction activation process, but in IIS technique, it inserts the implantation and activation processes between the silicidation processes, i.e. after first silicidation RTA process. Most thermal budgets [8,9] needed in IIS method are below 700℃, and this is important to the integrating for high-k gate dielectric materials. Since some high-k materials [2] start to crystallize at 600℃, IIS could be a candidate to integrate with high-k material with gate first MOSFET fabrication process.

1.3 Motivation

There are many reports showed that they have successfully fabricated p/n junctions using IIS method, such like low contact resistance [10], low reverse current [11], high activation energy [11] and even been integrated in MOS device [12]. Although these researches illustrated very attracting results, the process window of IIS technique for these researches were different far from one to each other, from tens of seconds to a few hours. Is this implying that IIS technique is very robust and have a very wide process window? Although most studies have showed that the device fabricated by IIS method has a good performance, few literatures have been done on the topic of the mechanism of how the junction formation starts and why the IIS technique could achieve high activation at low activation temperature. In these study, we try to discuss and descript the junction formation behavior and some possible mechanisms of IIS technique.

1.4 Thesis Organization

This thesis is mainly composed of two parts. Part I (ch2 MS junction, ch3 $M/N^+/P$ junction, and ch4 $M/P^+/N$ junction) are focus on the mechanisms related to the junction formation and dopant activation issues of IIS method and Part II (chapter 5,6) tries to find a proper way to interpret the corresponding electrical properties of junctions formed by IIS method (ch5 Electrical Properties of Shallow Junction) and also covers some thermal reliability issue (ch6 Thermal Reliability of Junctions Formed by IIS Method). At the end, a final chapter (ch7) of the summary of this thesis and the future work of this study is also included.

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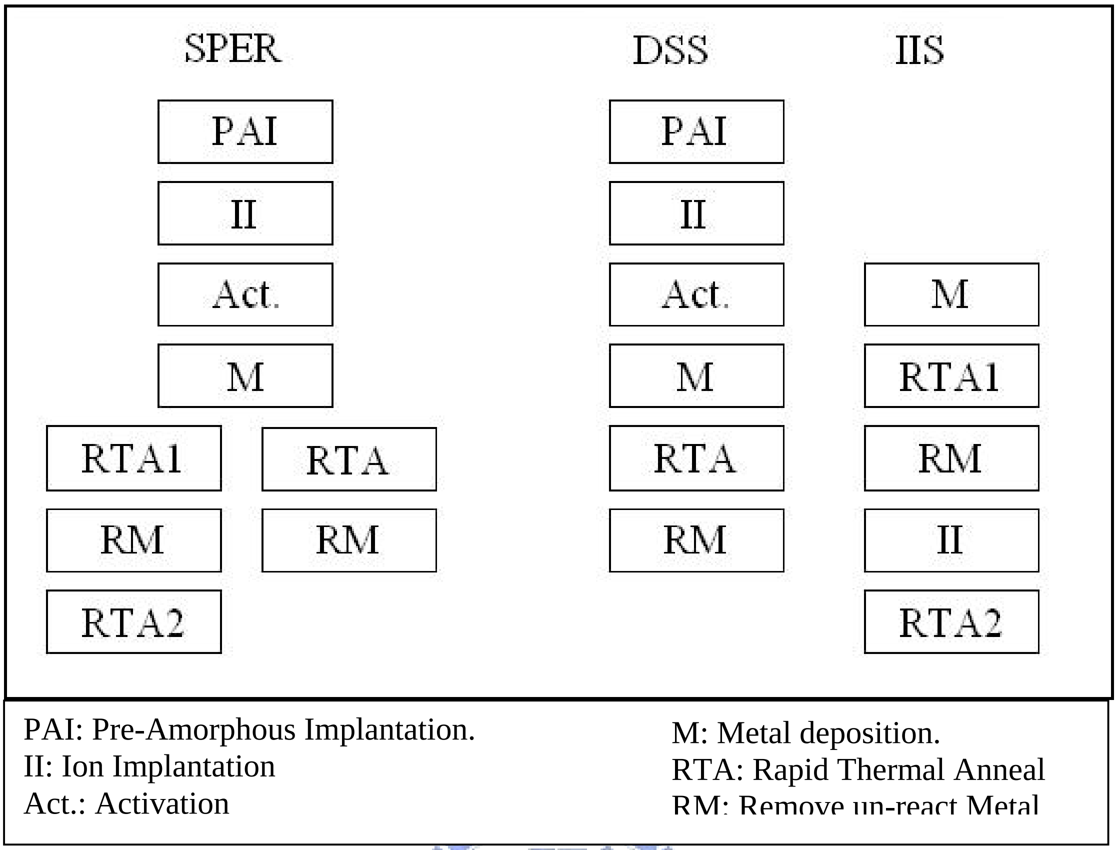

PAI: Pre-Amorphous Implantation.
II: Ion Implantation
Act.: Activation
M: Metal deposition.
RTA: Rapid Thermal Anneal
RM: Remove un-react Metal

Fig. 1.1. Schematic process flows of SPER, DSS and IIS techniques.

Chapter 2

MS JUNCTION

2.1 Introduction

Most efforts to study the Implant Into Silicide (IIS) method were based on p/n junction diode structure, however, before discussing p/n diodes, the properties at the silicide/silicon interface formed by IIS technology should be made clear at first. Since there is always a MS junction exists in series with the p/n junction, unless we know the MS junction properties, we could not fully understand the p/n diodes properties. As a result, we start our effort from discussing the MS junction behavior.

With carefully design of the process parameters, except the potential low temperature activation ability, the IIS method could provide two additional advantages to traditional S/D activation process. First, if the projection range of the implantation is located at silicide, the implantation damage in the silicon region could be minimized. Secondly, like the DSS technique, dopant in the silicide could be piled up at the silicide/silicon interface during the 2nd RTA step of the IIS method. The dopant segregation phenomenon could provide a possibility for the designer to lower the implantation dosage, as a result, the implantation damage could be further lowered.

Since we used the nickel silicide be the metal contact material, it is reported that the phase transition of NiSi to $NiSi_2$ is about 700℃, and with higher temperature treatment, the silicide will agglomerate. To avoid theses unwanted factors to affect our work, the high temperature treatment in this study is below 700℃. This is also a good process window for most high-k dielectrics [1, 2]. Furthermore, for properly integrating the IIS method and high-k dielectric, lower thermal budget is preferred. In this study, RTA (Rapid Thermal Annealing) system is adopted, and all thermal treatments were done not more than one minute.

2.2 Methods

SIMS has most frequently been adapted to show the dopant segregation phenomena at the silicide/silicon interface and the spreading resistance profiling (SRP) method has been used to analyze the dopant concentration at the bulk activated region [3-5]. However, SIMS spectrum does not provide the information about the activation and it is hard using SRP to study the doping profile at the silicide/silicon interface. In order to overcome these difficulties in measurements, in this chapter, we use the metal/semiconductor (MS) diode structure combined with I-V (current-voltage), C-V (capacitance-voltage), and SIMS measurements to explore the high activation ability at the silicide/silicon interface made by the IIS method. For the purpose of checking the activation ability near the silicide/silicon interface, a relative low dosage 1×10^{13} cm^{-2} is adapted in this study.

I-V measurement could give the information about the transportation mechanism at the M/S interface, and C-V measurement point a way to evaluate the doping density at the M/S interface. SIMS spectrum and AFM images are used as the reference for the device fabrication.

2.3 Device Fabrication

Stating material is (100) n-type (1 to 10 ohm-cm, phosphorous doped) and (100) p-type (1 to 10 ohm-cm, boron doped) wafer. A 200 nm thick silicon dioxide was thermally grown for isolation. Nickel silicide was formed by two-step rapid thermal annealing (RTA) process. A 20 nm thick nickel film was deposited by sputter system. All samples were under first step RTA at the condition 400℃ 30s. After removing the unreacted Ni, p-type substrate samples were implanted with BF_2 (1x10^{13} cm^{-2}, 20keV) and n-type substrate samples were implanted with arsenic (1x10^{13} cm^{-2}, 10keV). Before thermal coated Al as the back contact, samples were treated with 2nd RTA step 30 seconds at different temperatures from 400 to 650℃, 50℃ per step (400, 450, 500, 550, 600, and 650℃).

2.4. Results and Discussions

2.4.1 SIMS measurement

SIMS profile of the BF_2 doped sample with 2nd RTA 400℃ 30s is shown in Fig. 2.1, and it provides two messages. First, the peak boron concentration is appeared inside the nickel silicide film suggesting that the projected range at this study is in the silicide, which implies the implantation damage in the silicon is depressed. And secondly, dopant segregation phenomenon can be found at the silicide/silicon interface even at the short period with low temperature annealing (2nd RTA 400℃ 30s). The silicide thickness from SIMS measurement is about 23nm, and this value is confirmed by the SEM inspection.

2.4.2 C-V measurement

In this study, we adapted the capacitance-voltage measurement [6] to analyze the silicide/silicon interface. With depletion approximation, depletion width (*W*) in the silicon is estimated by

$$W = \frac{K_s \varepsilon_0 A}{C} \tag{3.1}$$

Where K_s is dielectric constant of silicon and A is the MS diode's contact area. And the effective doping density at depth W is given by

$$N_A(W) = \frac{2}{q K_s \varepsilon_0 A^2 d(1/C^2)/dV} \tag{3.2}$$

Averaged boron doping density within the depletion region extracted form C-V measurement is illustrated in Fig. 2.2. It shows that with higher 2nd RTA temperature, higher doping density is obtained. From C-V measurement results, two observations can be found. First, even at the lowest activation temperature (400℃), the effective doping density (N_{eff}) is higher than 10^{18} cm^{-3}, this convinces that IIS is an effective method to achieve low temperature activation. And secondly, at higher temperature annealing, N_{eff} becomes higher than 10^{19} cm^{-3}. Silicon begins to become the degenerate substance at this high doping level, and this property is good for silicide/silicon interface to form an ohmic contact. Furthermore, we compared the integral of the dopant concentration over depths from SIMS and C-V measurement results (n_{SIMS} and n_{CV}) in Fig. 2.3. It shows that the activation percentage (n_{CV}/n_{SIMS}) is very high. Over 50% dopant was activated over 2nd RTA 450℃. The summation process was taken from Vr = 0 to 0.2V and dopant within the depletion region at V=0 was not summed in the C-V measured data. Samples with high N_{eff} might not be fully depleted in this voltage range; as a result, under-estimated n_{CV} might occur in these high N_{eff} samples. There exist an abnormal activation calculation occurred at 2nd RTA 650℃ sample. This may be due to the incorrect high doping density obtained from equation (3.1) and (3.2) that using Maxwell-Boltzmann distribution. The Maxwell-Boltzmann distribution will over-estimate the N_{eff} when the material becomes degenerate [7] and as the consequence, the activated dopant obtained using N_{eff} will also be over-estimate. At this study, we only use the Maxwell-Boltzmann distribution to estimate the doping density. Although it may not good enough to extract the real concentration of the sample, it does reflect the high activation ability at the silicide/silicon interface, and shows that near the M/S interface, silicon is undoubtedly turning into the degenerate material.

Similarly, phosphorous doped samples exhibit the high activation ability. It can be found in Fig. 2.4 that with above 500℃ 2nd RTA, phosphorous doped samples also achieve high effective doping densities more than 1×10^{19} cm^{-3}, which make the silicon at the M/S interface to become ohmic contact.

It might be thought strange that why some samples with high concentrations (cm^{-3}) but have lower activated dopant densities (cm^{-2}) shown in Fig. 2.3 and Fig. 2.4. The main reason must be explained by our data analyzing processes.

1. We measured I-V characteristics at different temperatures and the results showed that at lower temperatures (< 35 ℃), the sample behaved different to that at higher temperatures from the Arrhenius plot. We think that samples have Thermionic/Field Emission (TFE) behavior. From the measurements, we had chosen the C-V measurement voltage range in this study to be below 0.2 volt in order to decrease the field emission effects. As a result, the C-V measurements in Fig.2.2 to Fig. 2.4 are at the voltage range from 0V to the reverse biased 0.2V, 5 mV per step.
2. The data used to obtain concentrations (cm^{-3}) are the average concentrations from Vr =0 to 50mV, because these data are close to the M/S interface.
3. The data of densities (cm^{-2}) are the summation from Vr = 0 to 0.2V, which are different to the voltage range used to obtain concentrations (cm^{-3}). [during

summation, $\sum$concentration (cm^{-3})*d (cm^{-1}), only concentrations > 1x10^{16} cm^{-3} were included].

4. Data shown in Fig. 2.2 to Fig. 2.5 are averaged value of 10 different test devices.

Also, there are two points should be stated:

1. The concentrations (cm^{-3}) are more sensitive to a high measured data than densities (cm^{-2}) will be.

Since densities (cm^{-2}) are obtained from concentration (cm^{-3})*d (cm^{-1}), where d is negative related to concentrations (cm^{-3}). We think that this is the key point to the question why some samples with high concentrations but have lower activated dopant densities. At Vr = 0 to 0.2V, some samples with high concentrations (cm^{-3}) may not be fully depleted. So the densities (cm^{-2}) collected in this voltage range are truly narrower than the samples with lower concentrations (cm^{-3}). This "narrow behavior" is just because the limitation from the measurement voltage range. We have thought to normalize the densities (cm^{-2}) of all samples at the same integral width, but if we do so, the under-estimated densities (cm^{-2}) at samples with lower concentrations (cm^{-3}) will become serious. At this section, our object is to show that the high activation ratio can be obtained, so we decide to hold out the original data at the cost of under-estimating the densities (cm^{-2}) at samples with higher concentrations. Even though, we still successfully showed that, truly, from the C-V measurements results, IIS proving a high activated doping ability at the silicide/silicon interface.

2.4.3 I-V Measurement

For direct determine if the M/S junction is ohmic contact or not, I-V measurement can be a good reference. The corresponding I-V characteristics of boron doped samples are illustrated in Fig. 2.5 all samples with 2nd RTA have linear I-V characteristics instead of schottky diodes regulation characteristics, which means that all samples behave more likely to be ohmic contacts than schottky contacts. In addition, the slopes of the I-V curves are increasing when raising the 2nd RTA temperature from 400 to 550℃. Since the silicide after 2nd RTA temperatures at the range between 400 to 650℃ is at the nickel mono silicide phase [8], the sheet resistance is the same at these temperatures. The different characteristics of I-V curves with different 2nd RTA temperatures should be contributed to the differences in contact resistance. This indicates that the contact resistance is decreasing with increasing 2nd RTA temperature. This is in good agreement to C-V measurement result that more boron is activated at higher 2nd RTA temperature and higher 2nd RTA temperature can form better ohmic contact. Phosphorous doped samples have similar I-V behaviors. Both BF_2 doped p-type substrate and P doped n-type substrate show ohmic contact behavior at low temperature activation with nickel silicide as the contact metal using IIS method.

2.4.4 AFM Inspection

Morphology inspection is required to further to clarify that previous C-V and I-V measurement results are not biased by silicide deformation. Samples (n-type substrate, phosphorous doped) without 2nd RTA and with 2nd RTA 30s at different temperatures (400, 500 ,600, and 700 ℃) are prepared. Fig. 2.6 shows the AFM inspection results for these samples (Area: 10 μm x 10 μm), and all RMS values are around 1nm. No agglomerations are discovered in these samples even at RTA 700 ℃ 30s, which are similar to other groups' results [8, 9]. Since fluorine can retard nickel silicide film's agglomeration [10], it is believed that BF_2 doped samples can also sustain RTA 700

℃ 30s without agglomeration occur. Since the experiments from 2.4.1 to 2.4.3 are taken under 700℃, it is believed that these results are not biased by silicide agglomeration effect.

2.5 Conclusions

From SIMS measurement, it exhibits that there are high dopant dosages pilled up at the M/S interface due to the dopant segregation phenomenon even under low thermal budget 2nd RTA control. This factor could limit the implantation damage mainly occurred in the silicide layer and provide a better M/S interface. C-V measurement shows that with higher 2nd RTA temperatures at the range 400 to 650℃, higher activation could be achieved at the M/S interface for both boron and phosphorous doped samples. Ohmic contact property could be found in I-V measurements, with higher 2nd RTA temperatures between 400 to 550℃, lower contact resistances are present. AFM inspections shows that no agglomeration of silicide film is occurred under 700 ℃ 30s. From these results, 2nd RTA 500 to 600℃ 30s may be a good process window for IIS method to future integration with high-k dielectric device.

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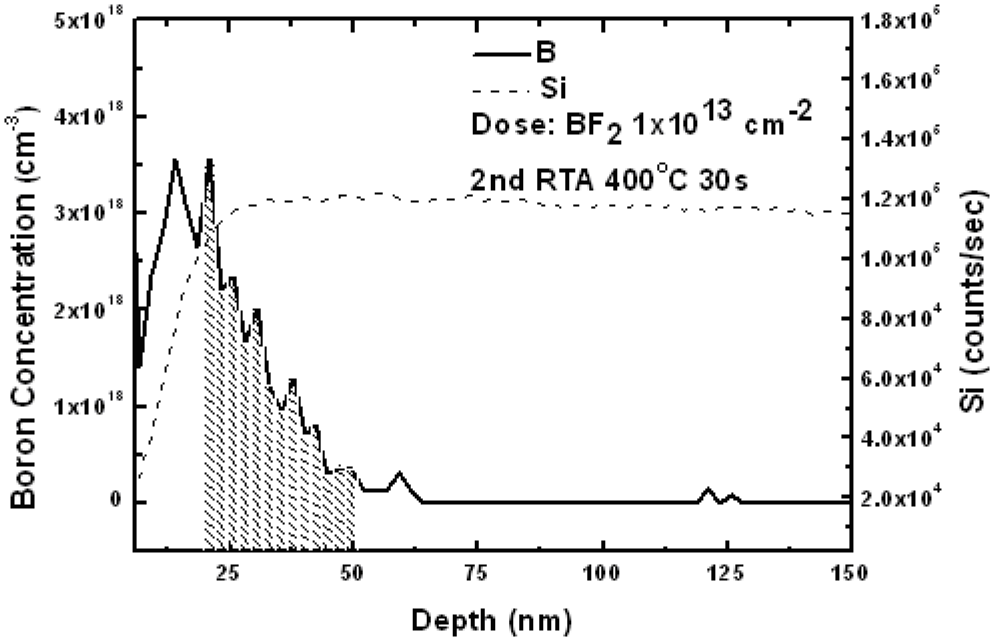


Fig. 2.1. SIMS profile of the BF_2 doped p-type substrate, with 2nd RTA 400℃ 30s. The dopant segregation phenomenon can be found at about 23nm from surface. The shadow area from 23nm to about 50nm is about 5×10^{12} cm^{-2}, which is defined as dopant implanted in Fig. 2.3.

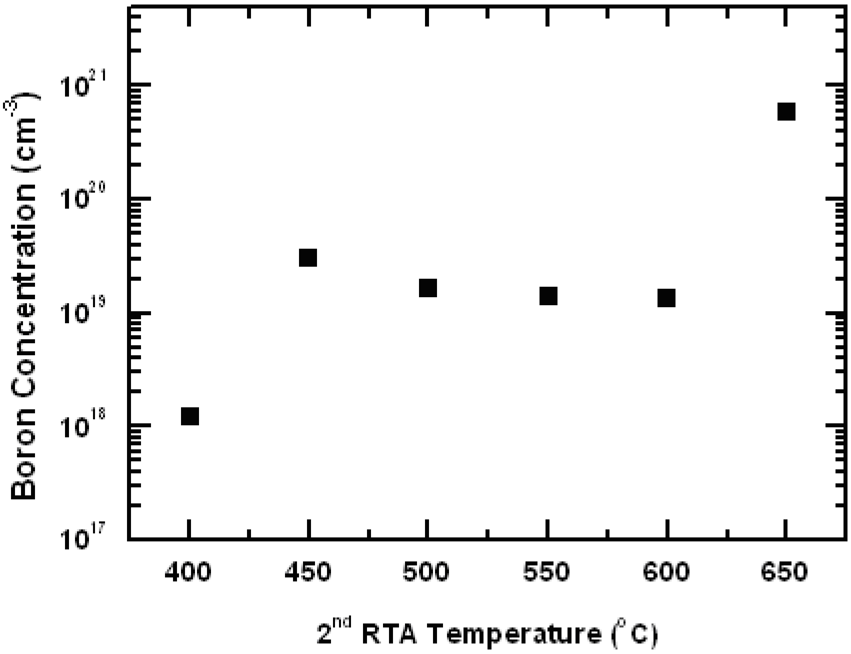


Fig. 2.2. Boron concentrations at different 2nd RTA temperatures extracted by C-V method

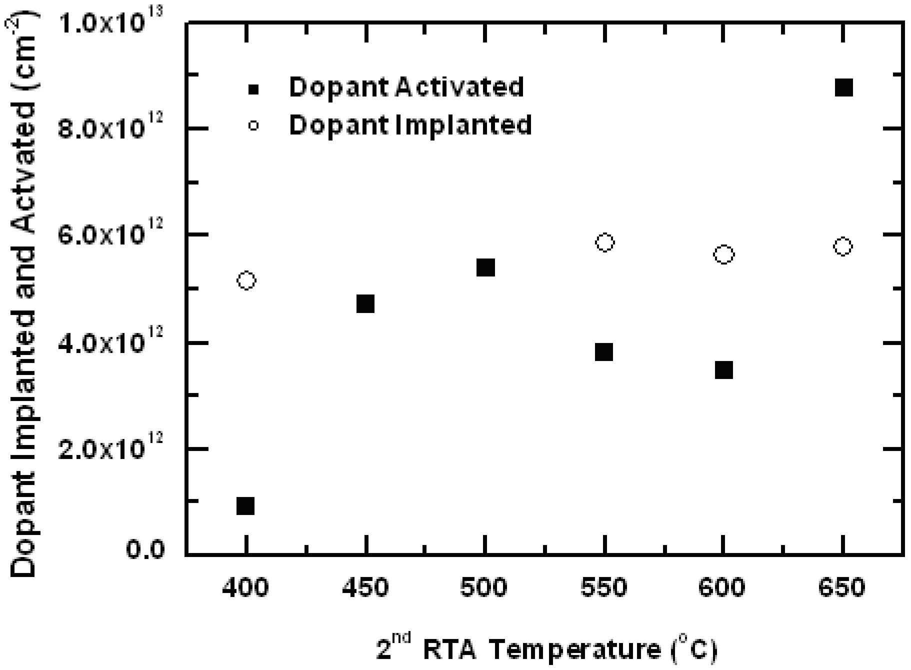


Fig. 2.3. Dopant (cm^{-2}) as the integral of the concentration over depths from C-V and SIMS profile (dopant activated and dopant implanted) versus different 2nd RTA temperatures.

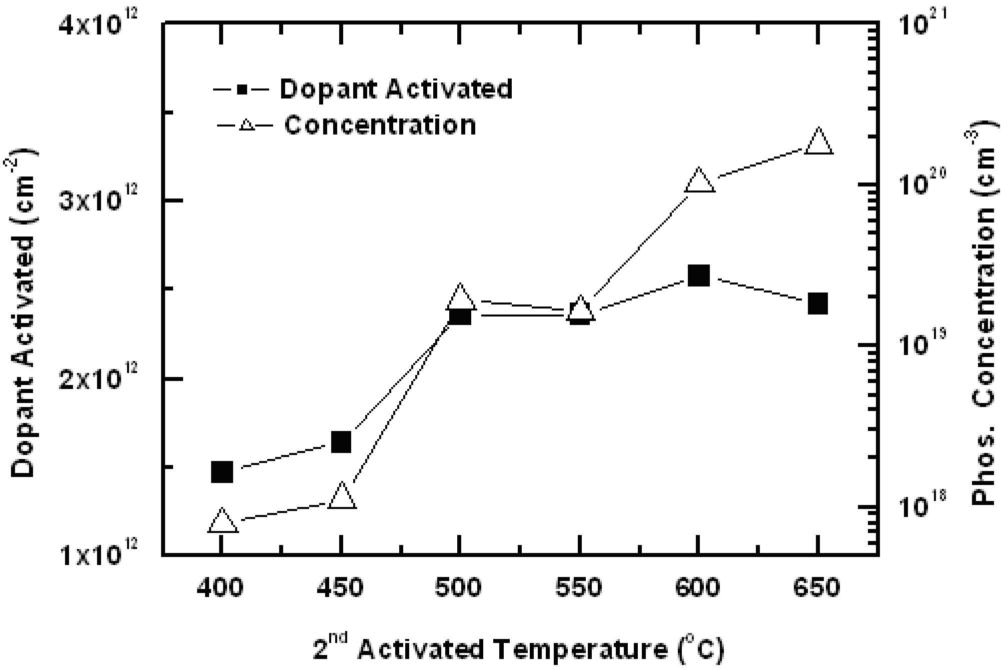


Fig. 2.4. Phos. concentration (cm^{-3}) calculated from C-V measurement, and activated dopant (cm^{-2}) as the integral of the concentration over depths from C-V measurement at different 2nd RTA temperatures.

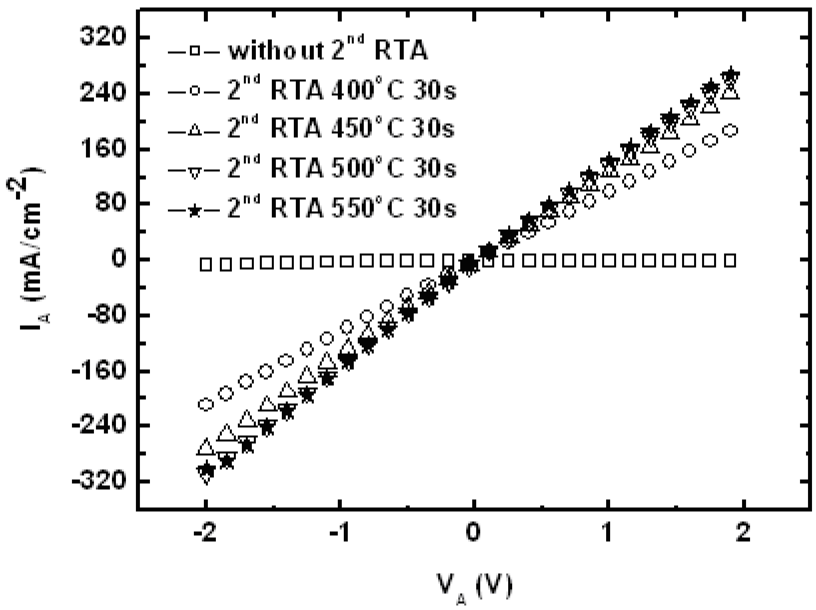
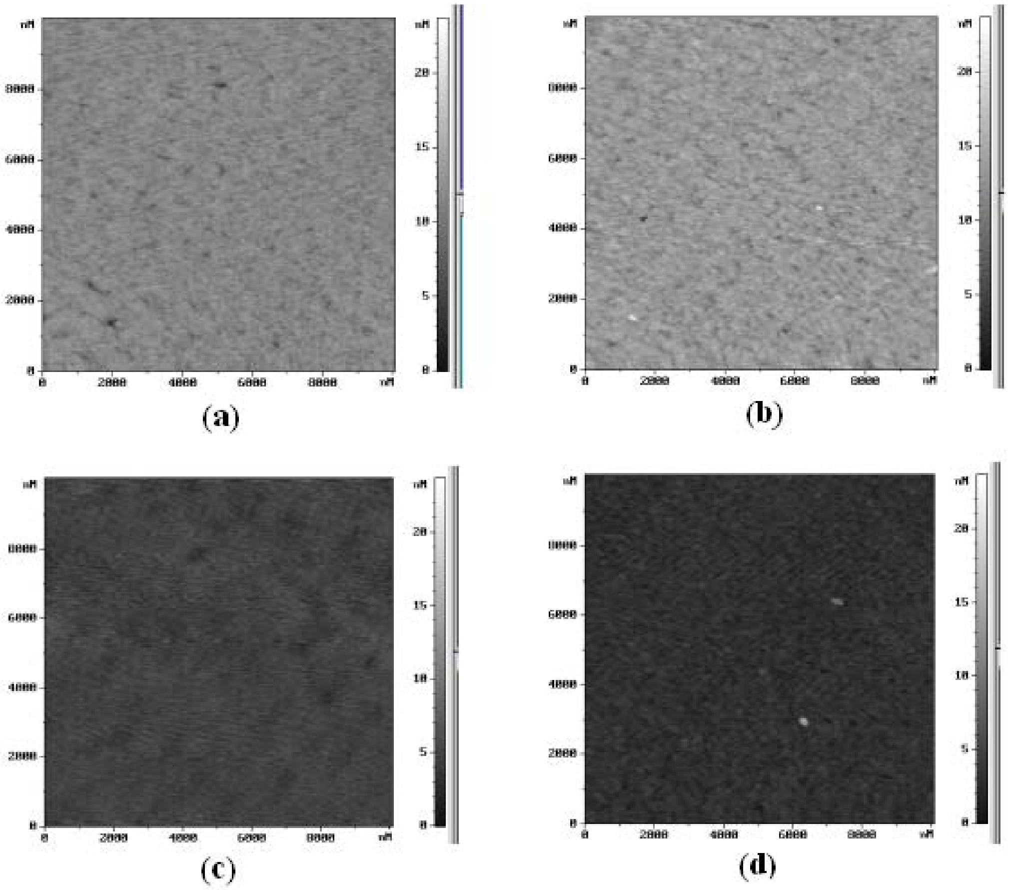


Fig. 2.5. I-V characteristics of boron doped samples. All samples with 2nd RTA behave more likely to ohmic contacts than schottky contacts.



(a) (b) (c) (d)

Fig. 2.6. AFM images show NiSi surface morphology with 30 second 2nd RTA at (a) 400 ℃ (b) 500 ℃ (c) 600 ℃ (d) 700 ℃.

Chapter 3

N^+/P JUNCTION

3.1 Brief Introduction and Design Idea

Based on our previous work [1], we could conclude that even at very low dosage ($1x10^{13}$ cm^{-2}), dopant activated at the silicide/silicon interface could drive the MS junction to become ohmic like. These experiment results showed that even with low temperature thermal treatment, junction formed by IIS [2-4] technique still had high dopant activation ability. But what is most important to us is that why IIS technique could exhibit this unusual property? There are no researches to answer this mechanic before.

To answer this question, first of our assumption is refer to the SPER [5-8] process. SPER process gives a good explanation of why dopant can be activated at lower temperature than traditional junction formation process. If there any linkage between SPER and IIS techniques? It is known that there will be an amorphous layer formed at silicide/silicon interface during the silicidation process. It is reasonable that what is happened in SPER process will also occur in IIS process. This provides the base of low temperature activation behavior for IIS technique. In addition, IIS usually needs less activation temperature comparing to SPER process. Our second assumption to the IIS technique is that silicide could lower the energy required for the SPER process. This factor is less discussed in CMOS process, but for TFT process, metal induced crystallization or lateral crystallization (MIC/MILC) is often been studied.

At this part, heavily doped phosphorous ($5x10^{15}$ cm^{-2}) is applied to our test device. Such a high dosage is commonly adapted in the traditional junction fabrication process. The projection range of the implantation was designed to locate in the silicide to let the implantation damage in silicon be minimized. The constraint for thermal treatments is the same as that in the chapter 1. Different to the metal/silicon interface discussed in chapter 1, chapter 2 focus on the silicide/N+/P test structures.

3.2 Device Fabrication

3.2.1 Device fabrication for I-V, C-V, SIMS measurements

Thirty-nanometer silicon dioxide was thermally grown on (100) p-type silicon wafer as the isolation oxide, after defining the active region, a 20nm nickel film was then deposited by E-gun evaporation system. All samples were treated with 1st RTA 350℃ 30s, after un-reacted Ni was removed, all samples were ion implanted with phosphorous (doping density: $5\text{x}10^{15}$ cm^{-2}), followed different 2nd RTA temperature treatments 60 seconds from 400℃ to 650℃, 50℃ per step. At the final step, Al was thermally coated as back contact. No post metal annealing was treated for thermal budget control consideration.

3.2.2 Device fabrication for FPP measurements

For four points probe test structure, starting material was (100) p-type silicon wafer, too. After thermal oxidation and active regions definition, 20nm nickel was deposited by e-gun system. Following processes were the same as described in section 3.2.1. However, for FPP test structure, after 2nd RTA, NiSi was removed using silicide etch solution (the etch selectivity of NiSi to bare Si is larger than 50). At the final step, Al was thermally coated as back contact. No post metal annealing was treated for thermal budget control consideration.

3. 3 Results and Discussions

3.3.1 C-V measurement

The effective phosphorous concentration (N_{eff}) estimated from C-V measurement [9] is demonstrated in Fig. 3.1. The measured capacitance is composed by of three different capacitances in series, silicide/silicon (M/S) junction capacitance, N^+/P junction capacitance, and back contact capacitance. Based on the results in chapter 2 (see also reference 10), it shows that there present a high dopant activation level at the M/S interface formed by IIS method, either it will become an ohmic contact or exits a relative large capacitance compared to the N^+/P junction capacitance where the lightly doped substrate dominate the small capacitance value. The M/S capacitance term could be neglect with little influence in the analysis. On the other hand, the area of the back contact is about the full wafer size, which is several orders of magnitude larger than the area of N^+/P junction, so the capacitance at the back contact can also not take into consideration. As the result, the measured capacitance was mainly contributed due to p-sub depletion junction at the N^+/P junction. From analyzing the C-V data, the p-sub doping density can be obtained from the differential capacitance-voltage profiling technique [9]. Fig. 3.1 shows the relationship between the depletion capacitance and the applied reverse voltage, the building voltage of the N^+/P junction can be obtained from the projection of the $1/C^2$-V curve to where $1/C^2 = 0$. The high linearity of the $1/C^2$-V curve implies that the abruptness of the N^+/P junction is good and is suitable to use the abrupt junction formula to express the experimental results. The N_{eff} is then calculated from the averaged substrate doping density and the building voltage. The relation of N_{eff} to the 2nd RTA temperature is shown in Fig. 3.2, it seems that the N_{eff} presents at the N^+/P interface is negatively related to the 2nd RTA temperature. The lowest N_{eff} extracted at this study is above 10^{19} cm^{-3}, which is four order larger than the substrate doping density. This supports the assumption that the capacitance measured is mainly due to the depletion in substrate at the N^+/P junction.

3.3.2 FPP and SIMS measurements

Some papers appointed that defects might cause dopant deactivated [11,12] at higher RTA temperature. However, from the study about the M/S junction [10], we did not find significant deactivation to take place at the silicide/silicon interface at the same process window in this study. In order to make clear what is the origin of the decreased N_{eff}, a test structure designed for FPP measurement is adapted. By removing nickel silicide using silicide etch solution (the etch selectivity of nickel silicide to bare Si is larger than 50 in our test), the results of measured resistance are displayed in Fig. 3.3. It shows that the resistances become smaller with higher 2nd RTA temperatures, which means that either doping concentration or the junction depth is extended with higher 2nd RTA temperature. Comparing the result to the SIMS profile in Fig. 3.4, suggesting that the lower N_{eff} measured at higher temperature is mainly due to that where the N^+/P interface presented are at the deeper position away from the M/S interface. The result implies that the dopant activation behavior is starting from the NiSi/Si interface and then extended to the silicon substrate. If the high activated doping concentration is related to the SRER process as we assumed in the previous chapter, it is recommended that the SPER process is starting from the M/S interface. As a consequence of C-V, FPP, and SIMS measurements, the suggested phosphorous activation behavior of the IIS method is illustrated in Fig. 3.5.

3.3.3 I-V measurement

In addition to analyze the junction forming behavior, I-V measurement are adapted. The N^+/P diode I-V measurement results are summarized as J_{on} (at V_A = -1V) and J_{off} (at V_A = 2V) exhibited in Fig. 3.6. The sample with 2nd RTA 550℃ 60s treatment has the lowest J_{off} value among all samples. The high J_{off} current densities presented at 2nd RTA temperature below 500℃ are explained as that there may exist high defect densities at the P/N junction interface. The defects may originate from the remained amorphous region where is still not recrystallized due to the short activation time or the low activation temperature. As the result, with increasing 2nd RTA temperatures, the SPER process continuous going, and the J_{off} currents decreased. At 2nd RTA 550℃ 60s, the SPER process seen to be completed (this can be observed by the relative consistent resistances measured in FPP method, see Fig. 3.3), the sample exhibits the maximum on/off ratio. However, the on/off ratios (Fig. 3.6) and N_{eff} (Fig. 3.2) diminish at 2nd RTA higher than 550℃ 60s. Since the SPER process looks like completed above 2nd RTA 550℃ 60s, the facts described above may originated by defect (dislocations start to form at the temperature range from 500 to 600℃ [13]) itself or by some defect induced dopant deactivation at the P^+/N interface. In addition, deactivation from phosphorous super-saturated solubility to thermal equilibrium solubility in silicon [14] might also play an important role when the thermal budget is higher than which required for SPER process completion. (The experiments of thermal stability about dopant super-saturated will be given in future publication.)

3.4 Conclusions

With the starting ideas that SPER and metal enhanced crystallization are the main responses to the high activation ability with IIS method in low activation temperature, we combine the SIMS, C-V, FPP, and I-V measurements to construct the doping activation behavior of the IIS method. All experiment results suggested that SPER process is starting from the M/S interface and extend into the silicon substrate. The best N^+/P interface is formed when SPER process is complete. After SPER process finished, samples with additional thermal budget treatment above 550℃ cause the defect formation at the bulk silicon and the dopant deactivation phenomenon may occur, both factors will decay the N^+/P junction's performance. Sample treated with 2nd RTA 550 ℃ 60s forms the best N^+/P junction among all controls in this study.

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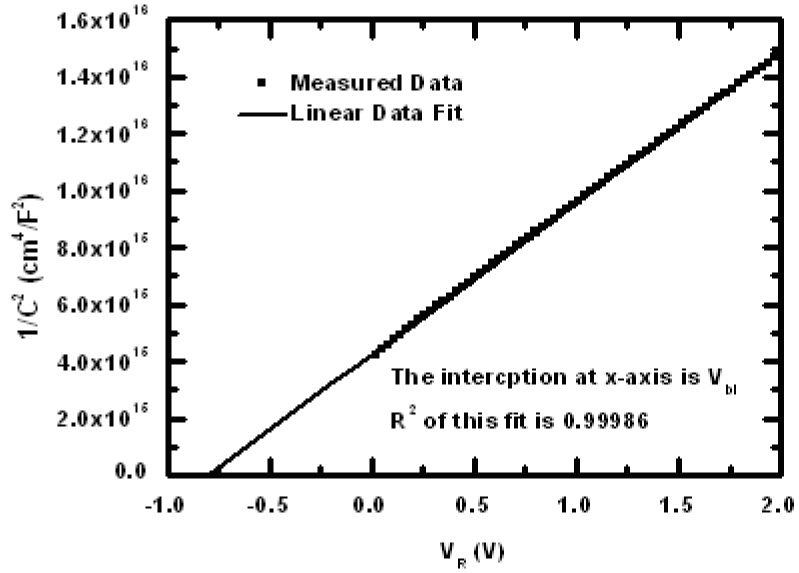


Fig. 3.1. An example of the measured1/C^2–V curve, the sample was treated with 2nd RTA 650℃ 60s.

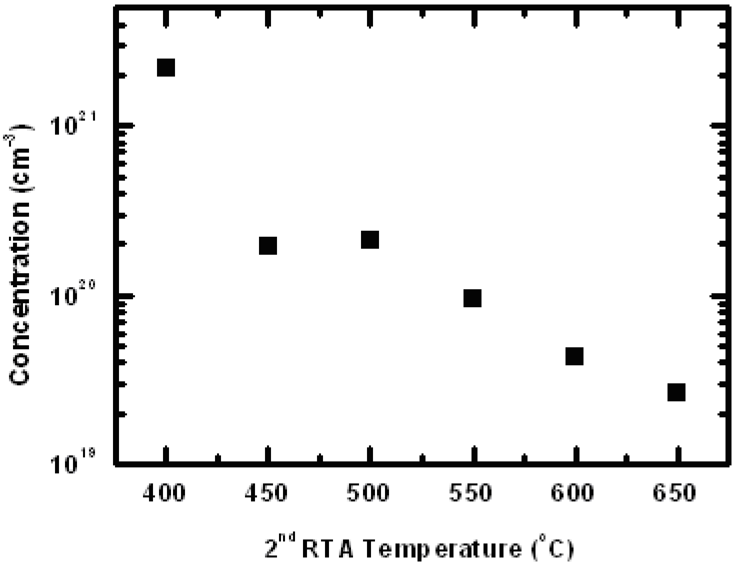


Fig. 3.2. Phos. doping density estimated from C-V measurement with different 2nd RTA temperatures.

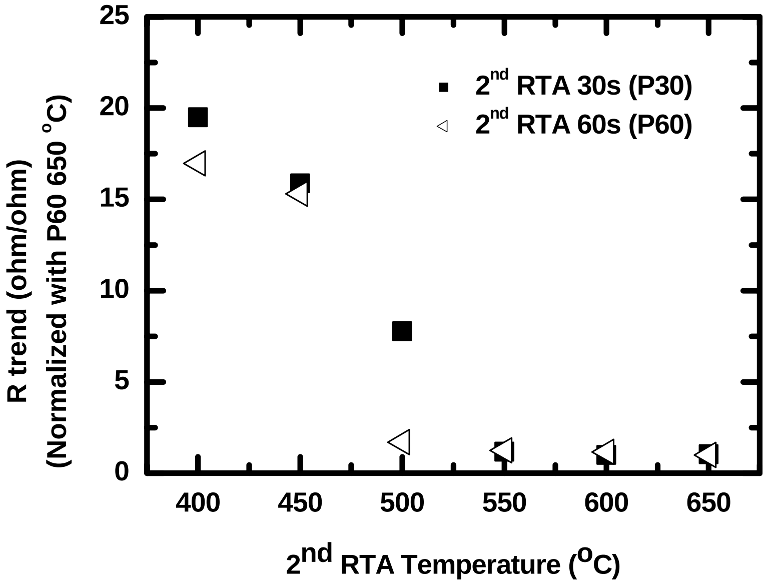


Fig. 3.3. Relative resistance ratio measured with FPP test structures at different 2nd RTA conditions

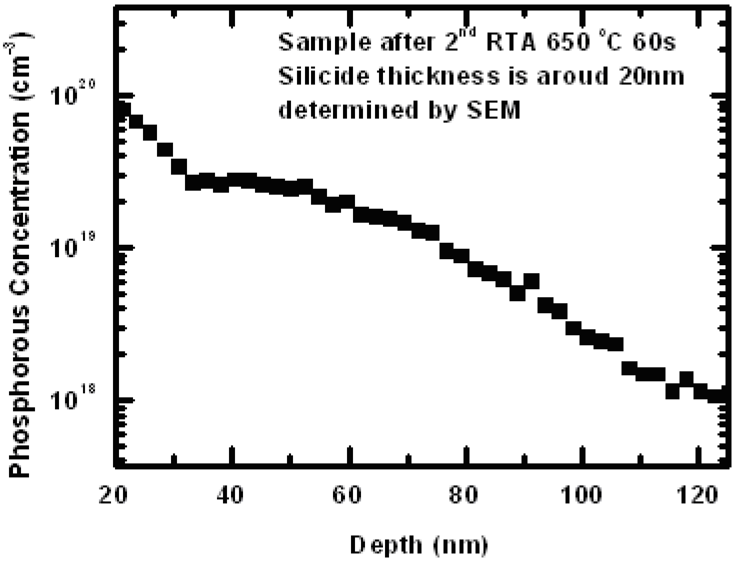
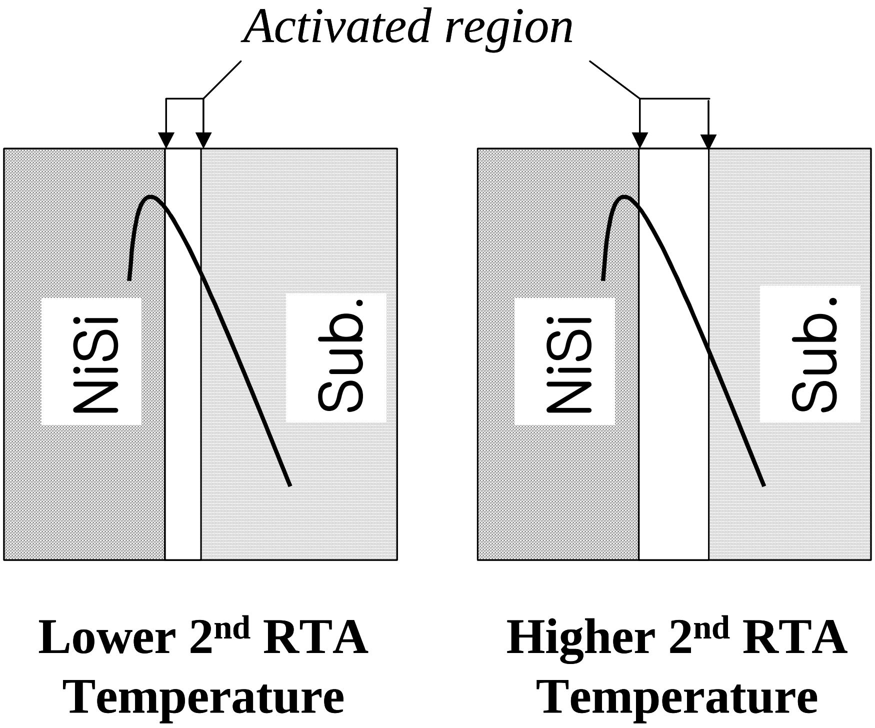


Fig. 3.4. SIMS profile of phosphorous doped sample treated with 2nd RTA 650℃ 60s.



Lower 2nd RTA Temperature **Higher 2nd RTA Temperature**

Fig. 3.5. The behavior of phosphorous activation is shown schematically. The P/N junction interface becomes deeper away from M/S interface with higher 2nd RTA temperature.

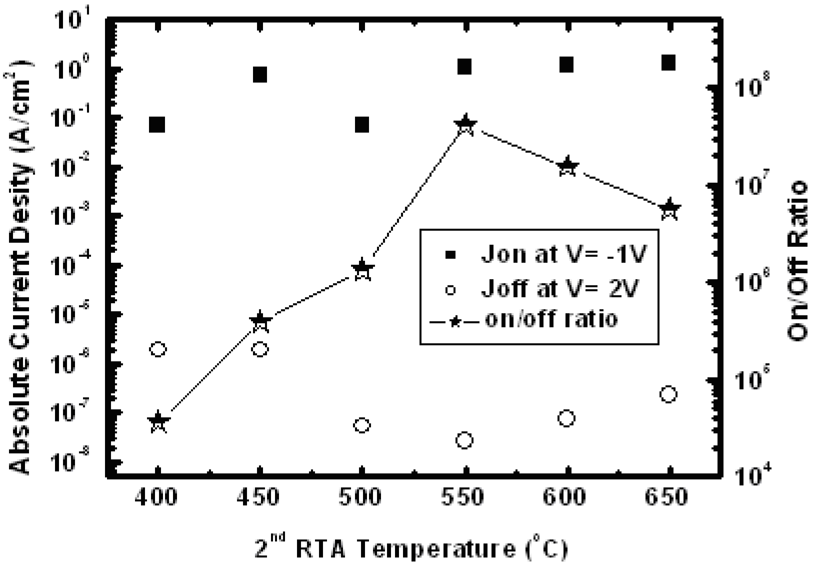


Fig. 3.6. Absolute J_{on}, J_{off}, current density and on/off ratio measured at different 2nd RTA temperatures.

Chapter 4

P$^+$/N JUNCTION

4.1 Brief Introduction and Design Idea

For the purpose to confirm the ideas made in chapter 2 (SPER and metal assisted metallization construct the low temperature dopant activation ability of IIS technique) and in chapter 3 (The SPER is starting from silicide/silicon interface and then extended into the silicon substrate) are valid, we designed an experiment similar to that in chapter 3 but differs in the implantation projection range design and the junction type. Boron was adapted as the implanted dopant in this study, due to its fast diffusion ability, and as a result the junction now we were treated was changed to silicide/P$^+$/N type. The projection range of this study was changed from in silicide (as in chapter 2 and chapter 3 did) to in the silicon. Since the peak dopant densities was located in the silicon region, we expected to see that with the C-V measurement, we could observe the “moving junction” behavior suggested in chapter 3.

4.2 Experiments

4.2.1 Device fabrication for I-V, C-V, SIMS measurements

Starting material was (100) n-type silicon wafer, after thermal oxidation and active regions definition, backside of the wafer was implanted with phosphorous $5x10^{15}$ cm^{-2} and annealed with furnace at 1000℃ 30 min. TaN 100 nm was sputtered on as the back contact. After dipped dilute HF to remove the native oxide at the active region, 20nm nickel was deposited by e-gun system. All samples were treated with 1st

RTA at 350℃ 30s, after unreacted Ni removed, all samples were ion implanted with BF_2 $5x10^{15}$ cm^{-2}. Then, samples were treated at 2^{nd} RTA 60s with different temperatures from 400℃ to 650℃, 50℃ per step.

4.2.2 Device fabrication for FPP measurements

For four points probe test structure, starting material was (100) n-type silicon wafer, too. After thermal oxidation and active regions definition, 20nm nickel was deposited by e-gun system. Following processes were the same as described in section 4.2.1. However, for FPP test structure, after 2^{nd} RTA, NiSi was removed using silicide etch solution (the etch selectivity of NiSi to bare Si is larger than 50). At the final step, Al was thermally coated as back contact. No post metal annealing was treated for thermal budget control consideration.

4.3. Results and Discussion

4.3.1 SIMS and C-V measurements

In comparison with N^+/P junction behavior studied in our previous work (reference 5, where the projected range is in the nickel silicide), a different doping profile is adapted in this study. As shown in Fig. 4.1, there are two peaks presented in SIMS profile (after 2^{nd} RTA 650℃ 60s). Peak 1 is formed due to dopant segregation [6] phenomena (NiSi film is about 23nm thick determined by SEM inspection), and Peak 2 is the projection range of this implantation.

From previous understanding [5], the effective boron concentration (N_{eff}) presented at the P/N interface estimated from C-V measurement in this study would not decrease monochromatically with the increasing 2^{nd} RTA temperatures, instead,

N_{eff} measured from increase 2nd RTA temperatures should have the trend such like some part of the SIMS profile. The C-V measurement result is demonstrated in Fig. 4.2, boron has the similar doping profile (but lower density due to not fully activated) to which obtained in SIMS measurement. This result supports our previous observation in chapter 3 that doping activation of the IIS method is starting from silicide/silicon interface toward the silicon substrate. Substrate doping densities extracted from C-V measurements are also shown in the Fig. 4.2 as a reference. It shows that phosphorous have a bit higher concentrations below 500℃ 2nd RTA. This behaviour might be due to samples treated at lower 2nd RTA temperatures have narrower activated region from the edge of NiSi/Si (M/S) interface, and there are some doping segregation phenomena of phosphorous at the M/S interface. As a result, samples with lower 2nd RTA temperatures, the P/N interface are closer to M/S interface than samples with higher 2nd RTA temperatures, and have a higher substrate concentration due to the doping segregation affect. This double confirms our previous observation in chapter 3.

4.3.2 I-V and FPP measurements

Fig. 4.3 shows the I-V measurement results of samples fabricated in section 4.2.1. The forward current (I_F) is defined at sample with 1V forward bias voltage, and the reverse (I_R) current is defined at sample with 2V reverse voltage. From the I_F/I_R ratio, it seems that the sample with 2nd RTA 550℃ 60s has the best performance at this measurement. The better performance of 2nd RTA 550℃ 60s than those samples with lower 2nd RTA temperatures can be contributed to two reasons. First, the activation process will also re-crystallize the amorphous layer at silicide/silicon interface caused by silicide formation process. With higher thermal budget, the better re-crystallization interface can be formed. Secondly, as shown in Fig. 4.1 and Fig. 4.2, the P^+/N junction position of 2nd RTA 550℃ 60s sample might be beyond the point 2 appeared in Fig. 4.1, where less doping defects (unactivated dopant and silicon interstitials) are present. However, the I-V behaviour above 550℃ is different to those observed about N^+/P junction in Fig 3.6, in N^+/P case, above 550℃, I_F/I_R ratios decreased with increasing 2nd RTA temperature.

To explain the I-V behaviour above 550℃, some other information about the junction formation should be measured as the reference. In Fig. 4.4, the relative resistance of these samples (after NiSi removed) measured with FPP test structure is displayed. The resistance reflects the combination interactions of the doping activation level and the junction depth. All resistances are normalized to the lowest measured value (2nd RTA 650℃ 60s). It exhibits that the resistance decreases gradually but has an abrupt decrease at 650℃ for N30 samples (treated with 2nd RTA 30s) and at 600℃ for N60 samples (treated with 2nd RTA 60s). In addition, the lowest resistance values measured in N30 and N60 samples are almost the same at the original data. This implies that above 2nd RTA 650℃ 30s or 2nd RTA 600℃ 60s, the bulk activation of boron is higher than the substrate doping density, and the p-type junction extended far into the substrate. As a result, the resistances measured under this bulk activation [7] condition are very similar. Bulk activation behaviour dominates the P^+/N junction formation at high thermal budget conditions. This explains the difference of the N^+/P and P^+/N junction's I-V behaviours above 550℃. In N^+/P case, the performance of junction formed at high thermal budget condition is dominated by defect formation or dopant deactivation, but for P^+/N case, bulk activation behaviour dominates.

The low I_F/I_R ratio of 600℃ 2^{nd} RTA sample (N600) in this study is due to the low forward current density measured at V_A = 1V. Fig. 4.5 shows the J-V curve of some samples treated at 2^{nd} RTA 550℃ 60s (N550-1), 600℃ 60 s (N600-1), and 650 ℃ 60 s (N650-1). The ideality factors of these three samples are all round 1.02. The low J_A of N600-1 is explained as follows: the law of junction is violated first of N600-1, which implies the voltage drop in the bulk regions occurring at lowest forward voltage in N600-1 sample. This means that the built-in voltage (Vbi) of the N600-1 sample is lowest among these samples. This observation confirmed the measured C-V data in Fig. 4.2, the N_{eff} is lowest at 2^{nd} RTA 600℃ 60s sample.

Besides, from Fig. 4.5, it is showed that J-V behaviour of N550-1 sample is different to the others. This doubly verified that higher than 2^{nd} RTA 550℃ 60s activation condition, the junction formation mechanism is much different. The N600 and N650 samples have lower leakage current at low reverse biased voltage due to lower defect densities presented at the junction depletion region. Bulk activation behavior extended the P/N junction far from the implantation caused defect region (i.e. Peak 2 in Fig. 4.1). Although the N600 and N650 samples take the advantage of the good electrical properties, they are not met the shallow junction requirement.

For more comprehensive understanding the P^+/N junction formation process, comparing with N^+/P junction formation in chapter 3 and the silicide/silicon interface formation processes in chapter 2 is needed. First, the boron activation densities are about 10^{17} to 10^{18} cm^{-3} in this study, however, for the N^+/P case, phosphorous could achieve 10^{19} to 10^{21} cm^{-3} doping activation level depending on different process conditions (Fig. 3.2). On the other side, boron activation densities near the silicide/silicon surface could also achieve 10^{19} to 10^{21} cm^{-3} doping activation level as shown in Fig 2.2 [8]. These two observations suggested that the activation abilities for boron and phosphorous are similar in metal assisted re-crystallize region (near the silicide/silicon interface). But a distance from the M/S interface, near the projection range located in silicon side in this study, where activation mainly correspond to the SPER [9] technique only, the dopant activation ability (10^{17} to 10^{18} cm^{-3}) is much lower than which with the metal assisted activation region (10^{19} to 10^{21} cm^{-3}). In short, metal assisted activation is more effective than SPER region at the temperatures below 600℃.

4.4 Conclusions

From the experiment results discussed in section 4.3.1 and 4.3.2, the activation of P^+/N junction formed with IIS method could be divided into three different mechanisms. First, near the silicide/silicon interface, metal assisted activation is presented, and secondly, at the heavily doped region where SPER caused activation behavior is observed. Finally, with higher activation temperature, above 600℃ in this study, bulk activation dominates the junction's position and its behavior. Boron could be activated at an effective doping density about 7×10^{17} cm^{-3} extracted from C-V measurement under 2nd RTA 450℃ 60s with the SPER caused activation mechanism. Among all process conditions in this work, samples treated at 2nd RTA 550℃ 60s have the best junction electrical characteristics before the bulk activation behavior dominates the device's properties.

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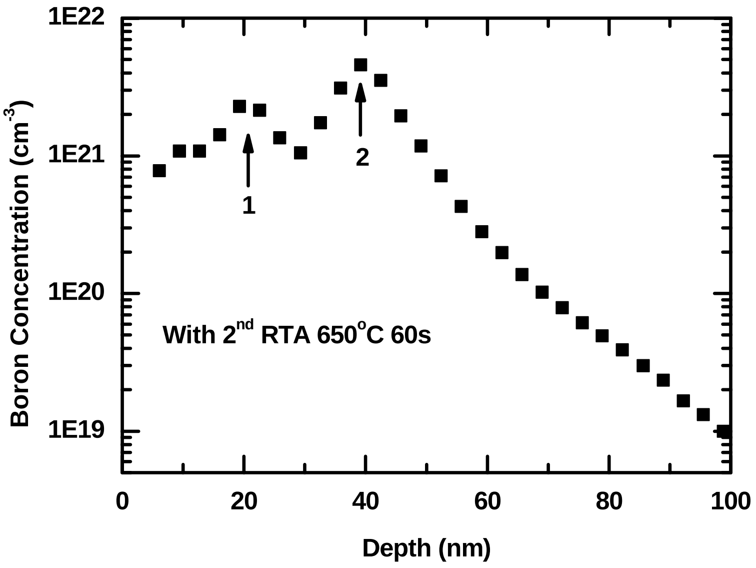

Fig. 4.1. SIMS profile of boron concentration with 2nd RTA 650℃ 60s

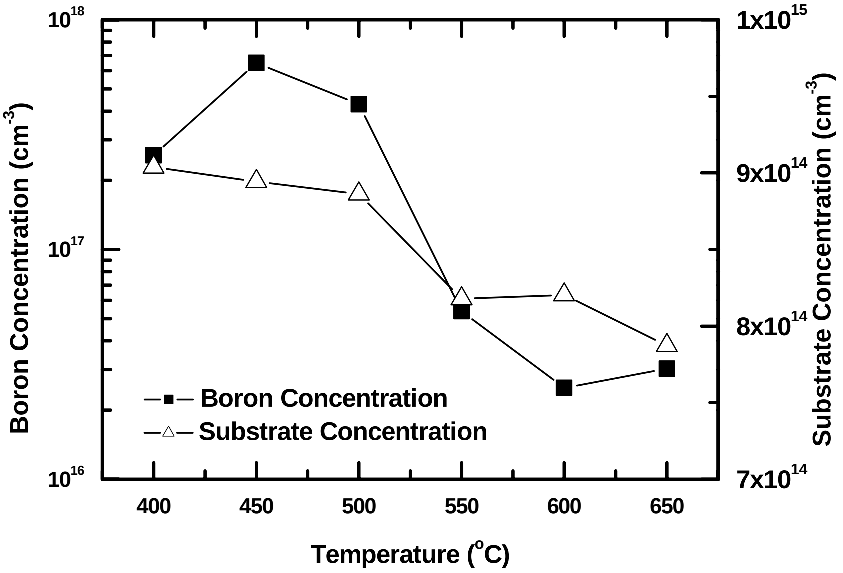

Fig. 4.2. Boron and substrate concentrations extracted with C-V measurement

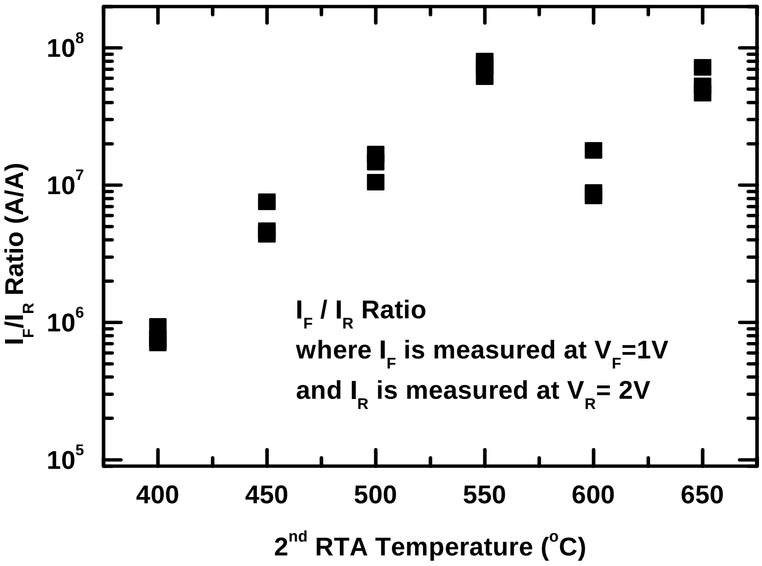

Fig. 4.3. I_F/I_R ratio with 2^{nd} RTA 60s at different temperatures

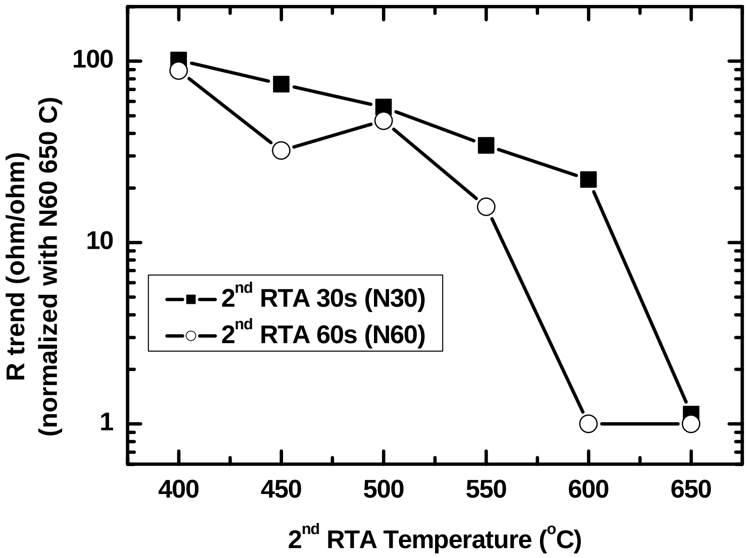

Fig. 4.4. Relative resistance ratio measured with FPP test structures at different 2nd RTA conditions

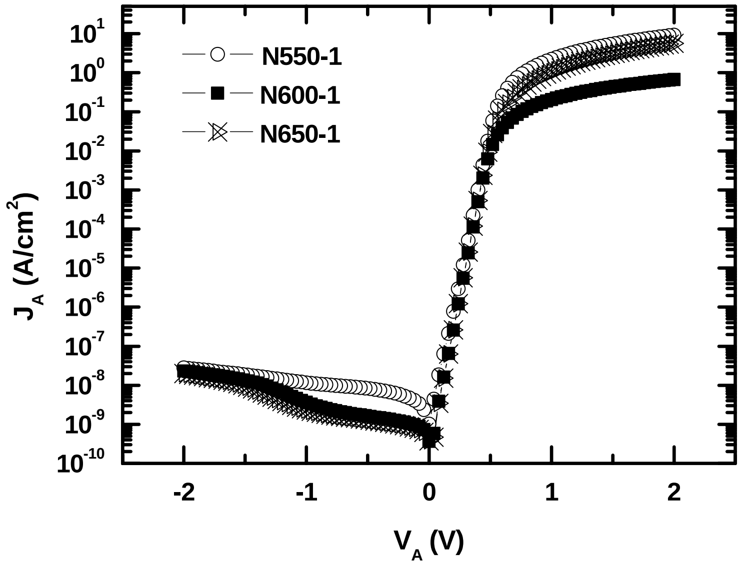

Fig. 4.5. The J-V characteristics of N550-1, N600-1, and N650-1 samples

Chapter 5

ELECTRICAL PROPERTIES OF SHALLOW JUNCTION

5.1 Brief Introduction and Design Idea

Schottky-liked PN junction is adapted to some of the next generation devices, such as DSSMOSFET reported by Toshiba [1], IBM [2], TSMC [3] and ASM [4]. The devices reported from reference 1 to reference 3 were fabricated with DSS method, and ASM adopted the IIS technology. Although each device processed with different conditions, all of these devices showed interesting electrical properties. Most devices had special junction behaviors characterized between traditional PN junction and MS junction. In this chapter, we want to devote our effort to study the shallow junction behavior.

Based on the understanding of the junction formation mechanisms described in previous chapters, we know that if we want to fabricate a shallow junction using IIS method, we must activate the junction in the metal assist activation region [5]. And if we want to optimize the junction’s electrical properties, to lower the defect density near the junction position is required. There are some defects might be generated in the junction formation process, like implantation defects and metal pollution. Some people wondered if there exist deep level defects by metal pollution originated from the implantation process: implanted dosage collides with the metal atom in the silicide and let the metal ion penetrate into the junction region. There are some reports showed that the second doubt listed above is not observed using the DLTS (Deep-Level Transient Spectroscopy) measurement [6,7] after two-step RTA. The best way to reduce the implantation defect is to lower the implantation energy.

Also, same as in chapter 2 and chapter 3, in this chapter we choose the low implantation energy to let the projection range falls in the silicide to minimize the implantation defects. In addition, since the un-activated dopant and the silicon interstitial replaced by the activated dopant are all playing the roles as the impurities in the junction, we lower the implantation dosages in order to lower the potential defects in the junction to improve the junction's performance.

5.2 Experiments

Two-port vertical diode structure was adopted in this study. Two different junction types were studied, M/N$^+$/P, and M/P$^+$/N. The starting material was (100) n-type and p-type silicon wafers, after thermal oxidation and active regions definition, backside of the n-type wafer was implanted with phosphorous 5x10^{15} cm^{-2} and backside of the p-type wafer was implanted with BF$_2$ 5x10^{15} cm^{-2}. All samples were then be annealed in furnace at 1000℃ for 30 minutes. TaN 100 nm was sputtered on as the back contact. After dipped dilute HF to remove the native oxide at the active region, 20nm nickel was deposited by e-gun system. All samples were then treated with 1st RTA at 400℃ for 30s. After un-reacted Ni removed, n-type substrate samples were ion implanted with BF$_2$ 5x10^{13} cm^{-2}, and p-type substrate samples were ion implanted with phosphorous 5x10^{13} cm^{-2}. Finally, samples were treated with 2nd RTA 60s at different temperatures from 450℃ to 600℃, 50℃ per step.

The major measurement methods used in this study were C-V, I-V, and I-V-T (I-V measurement in different temperatures is used to discuss the activation energy [6,8]) measurements. C-V measurements were processed with HP4284 at 50 kHz, and I-V measurements were measured with HP4156C.

5.3 Experiment Results

5.3.1 C-V measurement for M/P$^+$/N and M/N$^+$/P junctions

At this study, the implanted doses were one hundredth of that in chapter 3 and chapter 4. According to the previous knowledge, there are two possible results that might turn up in this study instinctively. First, since the implanted dose was lowered, the measured N_{eff} from the C-V data should not be higher than that obtained in chapter 3 and 4. On the other hand, from chapter 2, it was shown that even at very low implanted dosage ($1x10^{13}$ cm^{-2}), dopant activation at the silicide/silicon interface was high and compatible to the measured data with high implant dosage case ($5x10^{15}$ cm^{-2}, Chapter 3 and 4). Since junction fabricated in this study is supposed to have very shallow junction, as the result, the measured N_{eff} at this study should not be lower than what measured in chapter 2. Interestingly, the measured results in this study, as illustrated in Table 5.1, did not meet both intuitions just stated above.

Table 5.1 illustrates the N_{eff} extracted from C-V measurement results without considering bandgap narrowing effect. It seems that the N_{eff} obtained by C-V method with different implanted dosages activated at the same thermal budget does not relate to their implanted dosages. This phenomenon could be explained by the junction activation behavior discussed in previous chapters. The N_{eff} is not only represented the dosages but also the information of the junction position. The N_{eff} extracted from C-V measurement results adjusted with bandgap narrowing effect [9] is present in Table 5.2. It is interesting that for heavily boron doped samples, the higher the implanted dosages, the lower the N_{eff} concentrations near the P$^+$/N interface that we obtained. Since Boron has relative higher diffusion coefficient than phosphorous does [10,11] at the temperature lower than 600℃. The schematic graphs of boron and phosphorous with different implanted dosages diffused from silicide interface at same thermal budget are shown in Fig. 5.1. At the same thermal treatment, heavily doped sample diffused deeper than lightly doped sample, and at the same thermal treatment and same doping density, boron doped sample has almost double diffused region than phosphorous doped sample. For samples implanted with phosphorous $5x10^{13}$ (5E13) and $5x10^{15}$ (5E15) cm^{-2}, it could be found, in table 5.1, the highest activation level of these two different implanted samples was both occurred when treated at 500℃. It means that under this thermal treatment, devices are at their own best doping activation ability. Since these two samples were treated at the same temperature and had the same thermal budget, if we assume that the activated regions were the same and the diffusion coefficient was not different too much [12], 5E15 implanted samples should have higher N_{eff} than 5E13 implanted samples. But what is interesting is that the N_{eff} measured for 5E13 implanted samples are higher than 5E15 implanted samples at this temperature. Does this imply that that the 5E13 implanted samples have higher activation ability? Thus, this conclusion is not correct because with higher implanted dosages the samples become more amorphous and should have better activation ability. So the most rational explanation is that: Comparing with lightly implanted samples treated with the same thermal budget, the heavily doped samples have a more wide activated region, a deeper junction. This statement is true limited for 500℃ annealed sample, since below this temperature, samples are not really at there most stable condition (i.e. activation is still not complete). And samples with higher temperature treatment, some of the deactivation behavior might occur. On the other hand, the behaviors of samples doped with three different BF_2 dosages are easy to be understood. Since boron is fast diffuser in silicon, the N_{eff} measured with MS diode ($1x10^{13}$ cm^{-3}, N_{eff} near the silicide surface) are higher than the PN diode device. ($5x10^{13}$ cm^{-3}, N_{eff} extracted in the silicon). And the activation mechanism of the heavily doped one (5x10^{15} cm^{-3}, with the projection range inside the silicon) is most due to the SPER and bulk activation [5], hence, it has the lowest effective doping densities.

5.3.2 I-V measurement for M/P$^+$/N and M/N$^+$/P junctions

By the analysis stated in the 5.1, we know that lowering the implanted dosage should result in the lower defect densities in the junction (both MS and PN junctions). For a general junction, the saturated leakage current I_0 is given by [13]

$$I_0 = q[\frac{D_N}{L_N} n_{po} + \frac{D_P}{L_P} p_{no}] \propto n_i^{\,2} \propto T^3 \exp(\frac{eE_g}{kT}) \qquad (5.1)$$

The dominant term is the minority carrier densities in the lightly doped region, the substrate. Since the doping of the substrate is the same in our study, the devices with the lower defect density should have better performance in the leakage current.

The off state current densities (measured at reverse bias V_R = 2 volt) of 5x10^{13} cm^{-2} implanted and 5x10^{15} cm^{-2} implanted samples treated with different 2nd RTA temperatures are demonstrated in Fig. 5.2. It shows that the 5x10^{13} cm^{-2} implanted samples have higher reverse current densities than 5x10^{15} cm^{-2} implanted samples for both phosphorous and boron doped samples. Comparing the on/off ratios to the 5x10^{15} cm^{-2} implanted samples showed in chapter 3 and 4, the 5x10^{13} cm^{-2} implanted samples also have worse performance. The J_{on}, J_{off} and on/of ratio of 5x10^{13} cm^{-2} implanted samples are showed in Fig. 5.3. This negative behavior might due to the shallow heavily doped region (i.e. the P$^+$ layer of the M/P$^+$/N structure), not only play the role as the PN junction but also like the schottky barrier modulation layer of the silicide/silicon interface [1,14]. The schottky-like behavior could be observed from the I-V-T measurement at the junction with the reverse bias condition [8,15]. Fig. 5.4

shows the I-V-T measurement result of the 5x10^{13} cm^{-2} implanted M/N^{+}/P sample treated with 2nd RTA at 450℃ for 60s. The slope of the line is about –6.63, which corresponds to the activation energy at 0.58 eV. The activation energies (it is used as schottky barrier height, SBH, in the following paragraphs) of the 5x10^{13} cm^{-2} implanted samples extracted from I-V-T measurements are summarized in Fig. 5.5 (for M/P^{+}/N samples) and Fig. 5.6 (for M/N^{+}/P samples). Interestingly, from the I-V-T measurement, M/P^{+}/N samples showed the similar SBH versus Bias dependence through different 2nd RTA conditions, in contrast, M/N^{+}/P did not. This might be due to the difference in diffusion ability of phosphorous and boron. As mentioned in 5.3.1, boron is faster diffuser than phosphorous and would make a relative deeper junction than phosphorous did. The deeper junction might be more insensitive to the variation of the junction depth. As a result, M/P^{+}/N samples behave in a more similar way. When reverse voltage is higher than 0.08V, the SBH seems to be decreased with the increasing reverse voltage bias (see Fig. 5.5). There are two common accepted theories used to explain the negative relationship between the SBH and the bias voltage. One is the image-charge-induced schottky barrier lowering [16], and the other is the inhomogeneous schottky barrier height induced electron dipole effect [8]. According to image-charge-induced lowering effect,

$$\Delta\phi = \sqrt{\frac{qE}{4\pi\varepsilon_s}} \propto V^{1/2}$$

(5.2)

where $\Delta\phi$ is SBH lowering, and E is applied electric field. Fig. 5.7(a) is plotted as delta SBH versus $V^{1/2}$, where delta SBH, the value directly obtained from the I-V-T data subtracted by the highest measured value at each condition, is used to replace $\Delta\phi$, since $\Delta\phi$ is unknown. The result of the line fitting is not good, which implies using image-charge-induced barrier lowering is not suitable to explain the data measured with V_R higher than 0.08V alone. On the other hand, one expression to describe inhomogeneous schottky barrier height induced electron dipole effect is given by function 6 in reference 7.

$$V(0,z)=V_{bb}[1-\frac{z}{W}]^2+V_n+V_a-\Delta[1-\frac{z}{(z^2+R_0^2)^{1/2}}] \tag{5.3}$$

Where V_{bb} = uniform SBH (SHB^0)– V_n (E_c-E_F) – V_a (applied voltage), W is the depletion width, and z is the depth from the MS interface. R_o is the radius of the circular patch that has a lower SBH. The effective barrier height (ϕ_{eff}) related to applied voltage is simplified as [8]:

$$\phi_{eff}=SHB^0-\gamma(V_{bb}/\eta)^{1/3} \tag{5.4}$$

where γ = $3(\Delta R_0^2/4)^{1/3}$, $\eta=\varepsilon_{Si}/(qN_D)$. The data fitted to the simplified equation is shown in Fig. 5.7(b). Since the curvatures of the curves in Fig. 5.7(a) are positive and those in Fig. 5.7(b) are a little negative, it could be concluded that both schottky barrier lowering and inhomogeneous schottky barrier height induced electron dipole effects influence the behavior of the M/P^+/N diodes described above.

Fig. 5.9 (M/N^+/P) and Fig. 5.8 (M/P^+/N) compare the samples with the V_{bi} extracted from C-V measurement, the SBH extracted from IVT measurement at 1.2V reverse bias, and the leakage current at 2V reverse bias at 25℃ under different 2nd RTA treatments. There are three major factors could be found in these two figures. First, in both Fig. 5.8 and Fig. 5.9, leakage currents are all negatively related to the SBH measured from IVT method (i.e. the higher the barrier height, the lower the leakage current). Secondly, in Fig. 5.8, it could be found that V_{bi} is positive related to SBH for the M/N^+/P case. However, this phenomenon does not hold in the M/P^+/N case shown in Fig. 5.9. It might be due to that phosphorous is less diffusive than boron, and hence M/N$^+$/P samples have shallower heavily doped region than M/N$^+$/P samples do. This comes to the same observation in Fig. 5.5 and Fig. 5.6 just mentioned above. In the case of M/N$^+$/P samples, the doping density in the PN junction interface, derived from V_{bi}, is much close to the real doping activation situation near the MS interface. Thirdly, referring to Fig. 5.8, it shows that the schottky barrier height will increase with the increasing dopant activation density of the N$^+$ region in the M/N$^+$/P samples. The N$^+$ region plays a role like an interfacial layer that can modify the measured schottky barrier height.

The I-V curves at the forward biased region for the $5*10^{13}$ and $5*10^{15}$ cm^{-3} implanted samples activated at different 2nd RTA temperatures are summarized at figure 5.10. It could be seem that samples with low implant dosages have lower “on voltages”. Where samples with $5*10^{15}$ cm^{-3} implant dosages are the samples fabricated in Chapter 3 and Chapter 4. Those “on voltages” lowered more significantly for M/P$^+$/N samples than those of M/N$^+$/P samples since M/P$^+$/N samples with $5*10^{15}$ cm^{-3} implant dosages have the deepest junction width.

5.4 Discussions

There are some interesting observations that should be given more attention.

5.4.1 Meaning of C-V measurement results

First of all, what needed to be made clear is the experiment results obtained by C-V measurement. Some research papers use the $1/C^2 - V_R$ curve as a mean to obtain schottky barrier height of the MS interface and others treat it as a way to determine the built-in potential of the PN junction for the special device type that mentioned in section 5.2. The experiment results in this study showed that when the heavily doped layer is very shallow, like the M/N$^+$/P case, C-V measurement and I-V-T measurement results are positively related to each other. Contrarily, the experiment results become independent when the heavily doped layer is not so shallow (the M/P$^+$/N case), it implies that C-V measurement is not a suitable tool to describe the SBH in such a situation directly. Instead, this suggested that C-V measurement result is more suitable to be considered as a method to describe the doping activation behavior at the P/N interface (as we have mentioned in chapter 3) than to determine the schottky barrier height. In summary, C-V measurement data provides the information of the doping activation ability at the P/N interface. If the interfacial heavily doped layer is thin enough, the C-V results will provide a self-consistence result to the I-V-T measured results, which implied that the SBH modulation is positively related to the interfacial layer's doping density.

5.4.2 SBH modulation and junction depth

Secondly, although the bottom of the schottky-like behavior is still not clear, Figs. 5.5, 5.6 show that when the junction is not so shallow (M/P$^+$/N case), at V_R larger than 0.1V, the SBH extracted from I-V-T measurement lowers related from $V_R^{1/2}$ to $V_R^{1/3}$, which is thought to be contributed to both the image charge lowering effect and the inhomogeneous schottky barrier height induced electron dipole effect. However, with shallower heavily doped region (M/N$^+$/P case), this phenomenon ceased and had a deeper junction, as the traditional PN junction, and the activation energy extracted from the I-V-T method will not depend on the junction bias. In short, the relationship between the SBH modulation and the heavily doped region depth is not a simple linear dependence. Traditionally, the effect of heavily doped layer to modulate the SBH is estimated by $a*w$ product [14,17], where a is heavily doping density and w is junction depth. The analysis is based on the assumptions that no bandgap narrowing effects considered, fully depletion and thermal emission dominate. However, according to the doping densities shown in Table 5.2, this complexity might occur due to the transportation mechanisms that differ at the metal/semiconductor interface. For M/P$^+$ interface the TFE, thermal or field emission, dominates and for M/N$^+$ interface the tunneling mechanism is more significant. Also, the bandgap narrowing effects at the MS interface should not be ignored in such a situation. In addition, the assumption of fully depletion of the heavily doped region is difficult to maintain because the small depletion region caused in the heavily doped region is at the scale about 1nm. All these factors make strong couplings between the MS and the P/N interfaces. Theoretically, with a P$^+$ interface layer, the effective SBH should be higher than NiSi/n-Si case that is about 0.75eV. However, SBH in all samples with BF_2 $5*10^{13}$ cm^{-2} dosages, after 2nd RTA, is lower than 0.75eV obtained from I-V-T measurement. It implied that the coupling between the low SBH M/P$^+$ junction (smaller than 0.75eV) and high V_{bi} P$^+$/N junction is so strong and needs a new model to express such a device.

5.4.3 Abnormal increase of SBH at low reverse bias region

Thirdly, there exists an abnormal increase of SBH at low reverse bias region for the M/P$^+$/N samples (Fig. 5.5), and this phenomenon is seldom mentioned before. If we treat the M/P$^+$/N junction as a whole M'/N junction, from the general expression for the schottky junction, the current is given by:

$$I = A^* A T^2 \exp(\frac{-q\phi_B}{kT})(\exp(\frac{qV_F}{nkT}) - 1) \qquad (5.5)$$

where A* is Richardson's constant, and A is the diode area.

When applied bias voltage V is large, the last term will be almost -1. (i.e. for $V_F = -0.24$, $\exp(V_F/0.025) \sim 6*10^{-5}$ at RT). However, when applied voltage is smaller than 0.1 volt, the last term will be less than one as an attenuator but cannot be ignored (i.e. for $V_F = -0.08$, last term of eq. 5.5 is equal to 0.04 -1 = -0.96 at RT). This could also be obvious when we want to calculate the SBH from the I-V-T method at low bias region. The data become less linear when with the temperature increases.

On the other hand, from the suggestion at previous section, if we treated the $M/P^+/N$ junction as two individual MS and PN junctions, similar discussions and results will be obtained at the P^+/N junction. It is hard to distinguish our experiment results from an schottky junction or a PN junction. However, for PN junction, the activation energy is about 1.1eV (the bandgap of the silicon), which is much higher than our observations. By analyzing the results from sections 5.4.2 and 5.4.3, we couldn't deny the possibility that $M/P^+/N$ junction might be treated as two individual M/P^+ and P^+/N junctions but with strong interactions between them.

5.5 Conclusions

At section 5.3.1, the C-V measurement results show that there would have strong bandgap narrowing effects at the MS interface due to the high dopant activation ability of the IIS method. Also, by comparing the C-V measurement results of samples with different implanted dosages, it could be concluded that the speed of the doping activation process (junction extension depth) is related to the quantity of implanted dosages. That is, samples after the same thermal budget treatment, the higher the implanted dosage, the deeper the junction will be formed. Theoretically speaking, lower the implantation densities could be beneficial to the junction's performance by lowering the defect levels in the junction area. However, the experiment result shown in Fig. 5.2 does not satisfy the assumption. This situation might be contributed to the junctions formed at the different process conditions would have different transportation mechanisms. At section 5.3.2, the I-V and I-V-T experiment results show that with low implantation dosage ($5*10^{13}$ cm^{-2}), the heavily doped region played a role like a SBH modulation layer. The different forward biased current behaviors between the high and low dose implanted samples are shown in Fig. 5.10. The low dose implanted samples are believed to have shallower junction and have lower “on voltages”. At the $M/N^{+}/P$ samples, the doping densities extracted from C-V methods could be approximated the phosphorous doping activation densities near the M/S interface. It shows that with higher activated doping densities near the M/S interface, the higher the SBH would be obtained from the I-V-T measurement and the lower the reverse biased leakage current. And for the $M/P^{+}/N$ sample, the junction behaves with both the characters of M/P^{+} junction (when V_R<0.1V) and M/N (whole behavior). It implied that the $M/P^{+}/N$ junction in this study could be treated as two individual junctions in series but with strong coupling effects between them.

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Table 5.1. N_{eff} extracted from C-V measurement results without considering bandgap narrowing effects

as implanted	450℃ 60s	500℃ 60s	550℃ 60s	600℃ 60s
P*: $1\text{x}10^{13}$ cm^{-2}	$1.12\text{x}10^{18}$	$1.91\text{x}10^{19}$	$1.64\text{x}10^{19}$	$1.02\text{x}10^{20}$
P: $5\text{x}10^{13}$ cm^{-2}	$1.66\text{x}10^{19}$	$6.66\text{x}10^{21}$	$3.36\text{x}10^{21}$	$2.70\text{x}10^{19}$
P**: $5\text{x}10^{15}$ cm^{-2}	$1.94\text{x}10^{20}$	$2.12\text{x}10^{20}$	$9.6\text{x}10^{19}$	$4.35\text{x}10^{19}$
B*: $1\text{x}10^{13}$ cm^{-2}	$3.04\text{x}10^{19}$	$1.62\text{x}10^{19}$	$1.37\text{x}10^{19}$	$1.35\text{x}10^{19}$
B: $5\text{x}10^{13}$ cm^{-2}	$1.99\text{x}10^{18}$	$9.09\text{x}10^{18}$	$1.51\text{x}10^{18}$	$7.93\text{x}10^{17}$
B**: $5\text{x}10^{15}$ cm^{-2}	$6.49\text{x}10^{17}$	$4.29\text{x}10^{17}$	$5.39\text{x}10^{16}$	$2.50\text{x}10^{16}$

* Samples fabricated as in chapter 2 (M/N^+/N or M/P^+/P diode structure)

** Samples fabricated as in chapter 3 and 4 (M/P^+/N or M/N^+/P diode structure)

Table 5.2. N_{eff} extracted from C-V measurement results adjusted with bandgap narrowing effects

as implanted	450℃ 60s	500℃ 60s	550℃ 60s	600℃ 60s
P: 1×10^{13} cm^{-2}	9.20×10^{17}	4.80×10^{18}	4.29×10^{18}	1.27×10^{19}
P: 5×10^{13} cm^{-2}	4.41×10^{18}	1.45×10^{20}	9.75×10^{19}	5.87×10^{18}
P: 5×10^{15} cm^{-2}	1.84×10^{19}	1.95×10^{19}	1.23×10^{19}	7.76×10^{18}
B: 1×10^{13} cm^{-2}	3.81×10^{18}	2.56×10^{18}	2.3×10^{18}	2.28×10^{18}
B: 5×10^{13} cm^{-2}	6.33×10^{17}	1.76×10^{18}	5.22×10^{17}	3.29×10^{17}
B: 5×10^{15} cm^{-2}	2.88×10^{17}	2.24×10^{17}	4.88×10^{16}	2.36×10^{16}

* Samples fabricated as in chapter 2

** Samples fabricated as in chapter 3 and 4

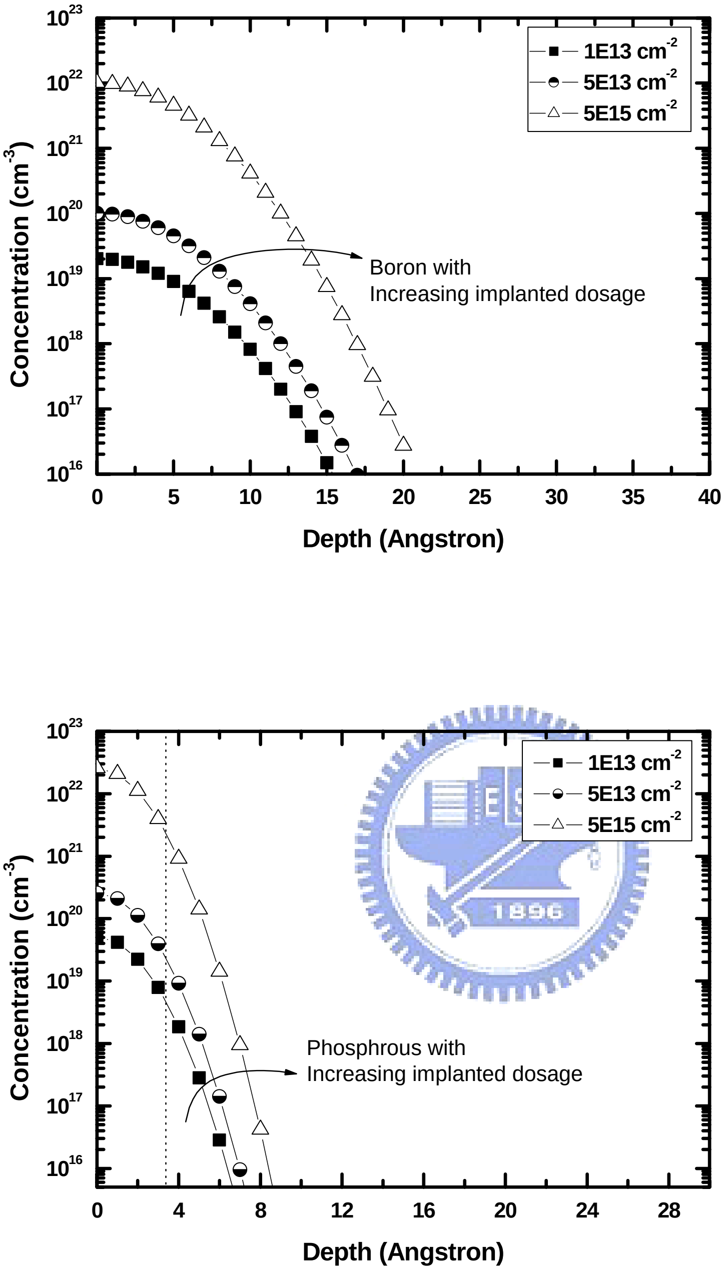


Fig. 5.1. (a) Boron and (b) phosphorous diffusion profiles calculated with the diffusion constant listed from references 9 and 10 (ignore implantation density effect)

Table 5.3. $\triangle E_{BNG}$ (bandgap narrowing effects in mV) calculates using reference 8

as implanted	450℃ 60s	500℃ 60s	550℃ 60s	600℃ 60s
P: $1x10^{13}$ cm^{-2}	34	57	56	74
P: $5x10^{13}$ cm^{-2}	56	139	126	61
P: $5x10^{15}$ cm^{-2}	83	84	74	66
B: $1x10^{13}$ cm^{-2}	54	48	46	46
B: $5x10^{13}$ cm^{-2}	30	43	28	23
B: $5x10^{15}$ cm^{-2}	21	19	9	7

* Samples fabricated as in chapter 2

** Samples fabricated as in chapter 3 and 4

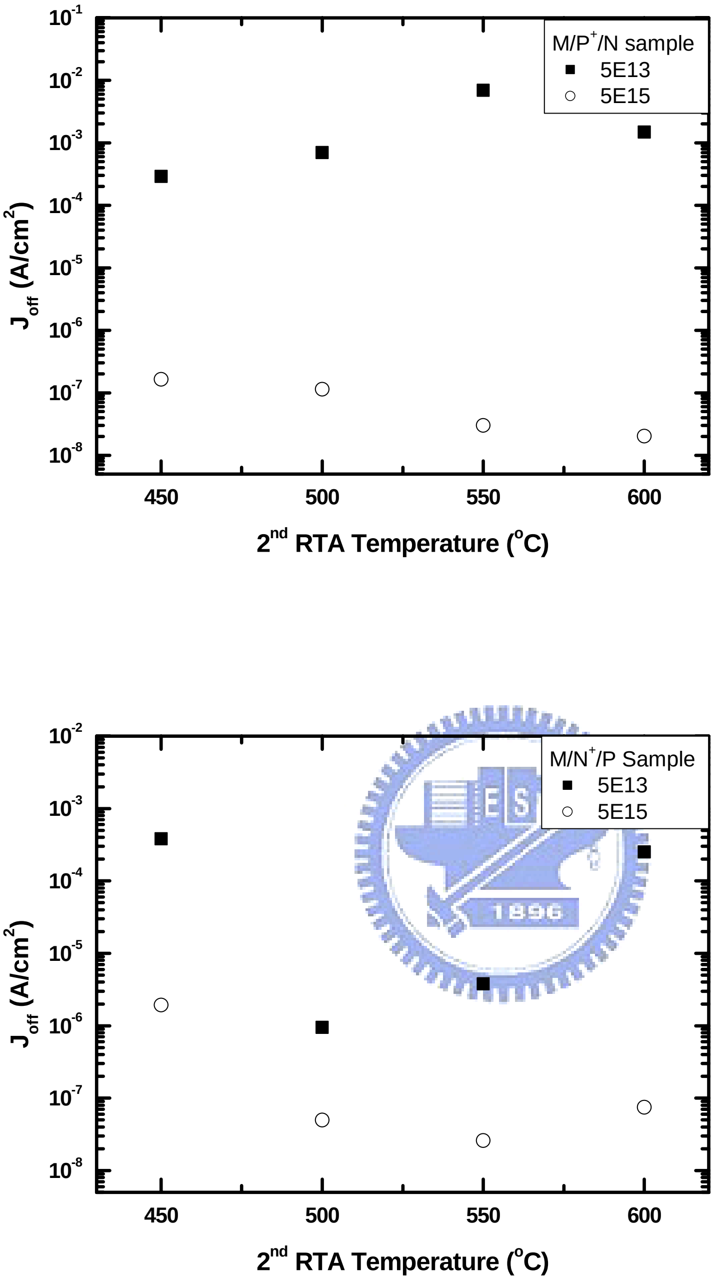


Fig. 5.2. Reverse current densities versus different 2nd RTA temperatures (a) M/P$^+$/N samples and (b) M/N$^+$/P samples

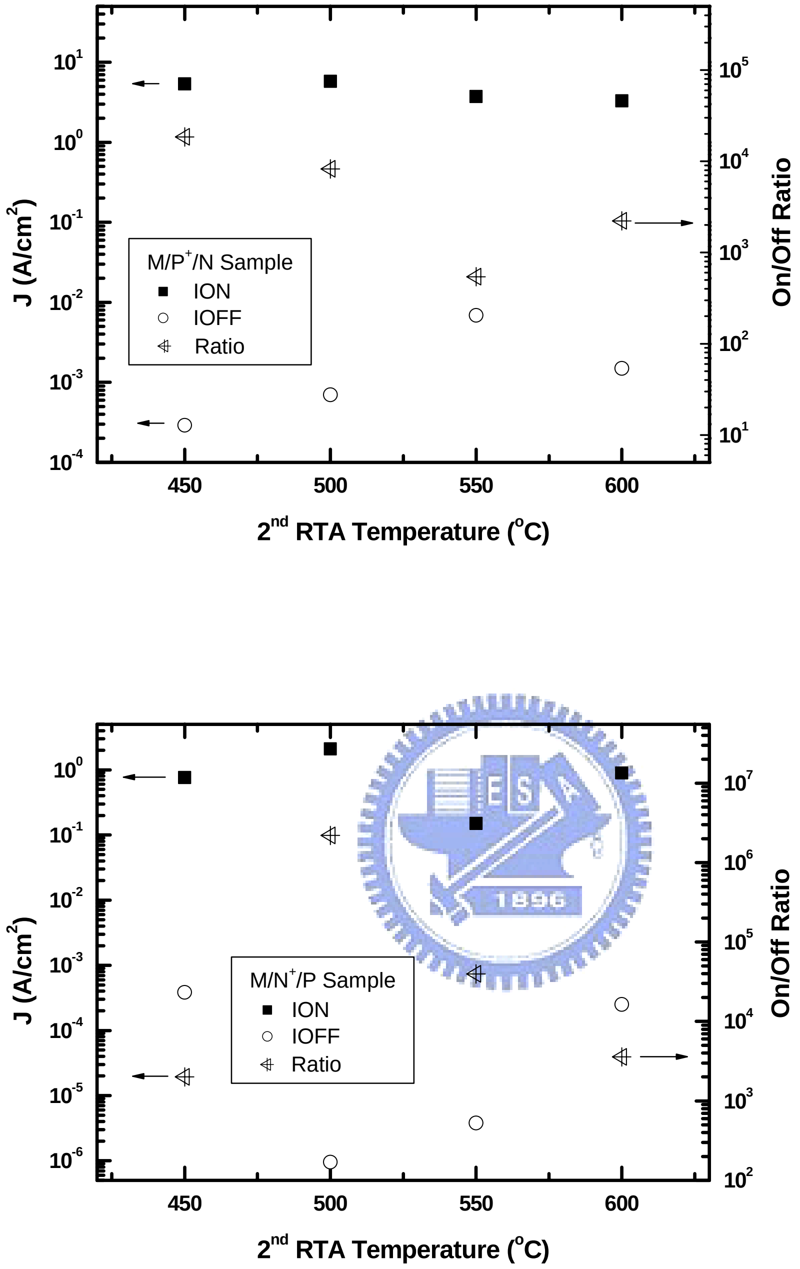


Fig. 5.3. Forward current densities (J_{on}), reverse current densities (J_{off}) and J_{on}/J_{off} ratio of the (a) M/P$^+$/N samples and (b) M/N$^+$/P samples

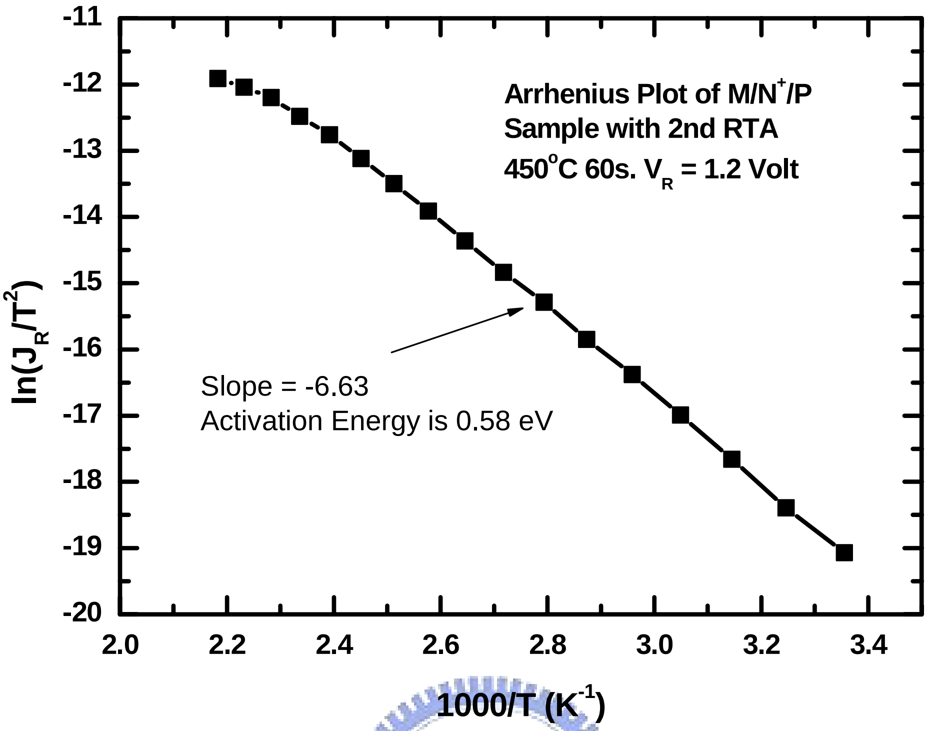


Fig. 5.4. Arrhenius plot of M/N^+/P sample with 2nd RTA at 450℃ for 60s. The slope of the $\ln(J_R/T^2)$-1000/T curve is about –6.63 which corresponds to the activation energy of 0.58 eV

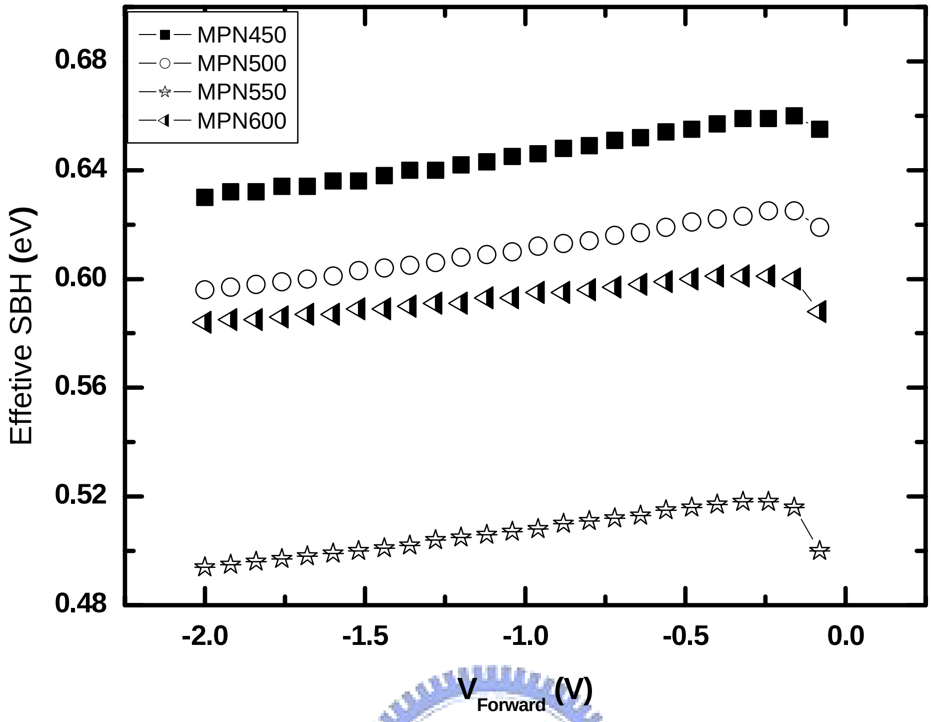


Fig. 5.5. Effective schottky barrier height extracted from I-V-T measurement of the M/P$^+$/N samples under reverse biased conditions

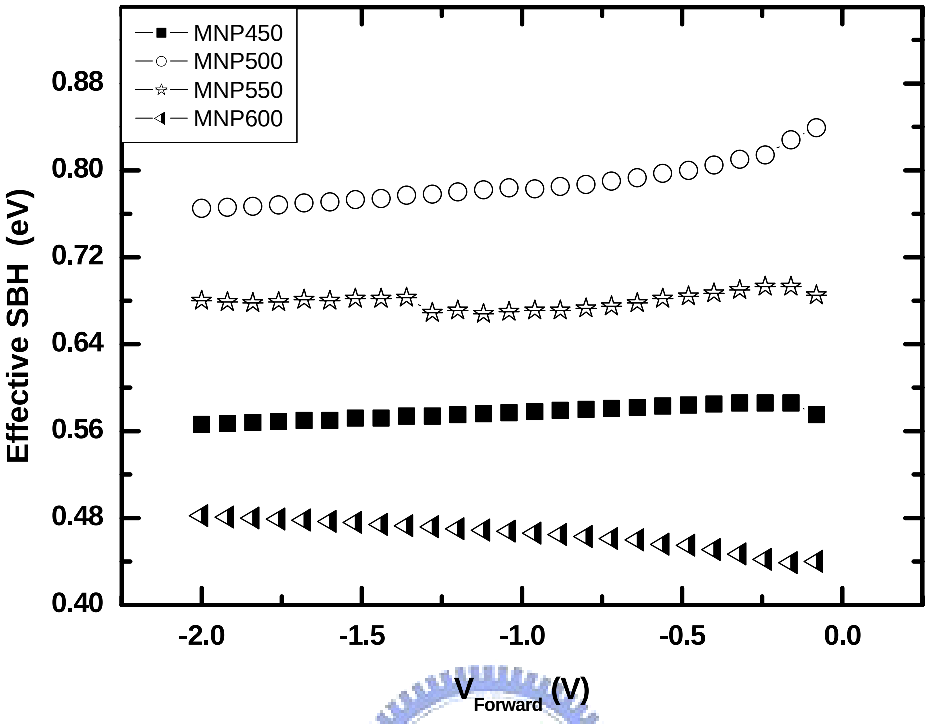
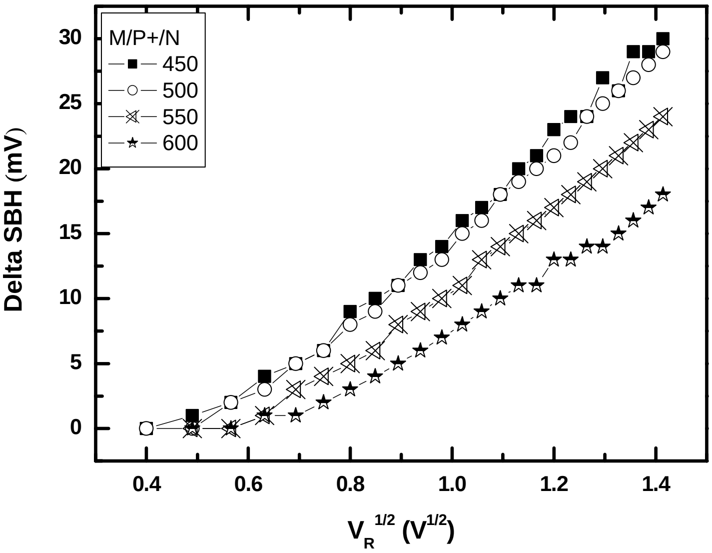


Fig. 5.6. Effective schottky barrier height extracted from I-V-T measurement of the M/N$^+$/P samples under reverse biased conditions



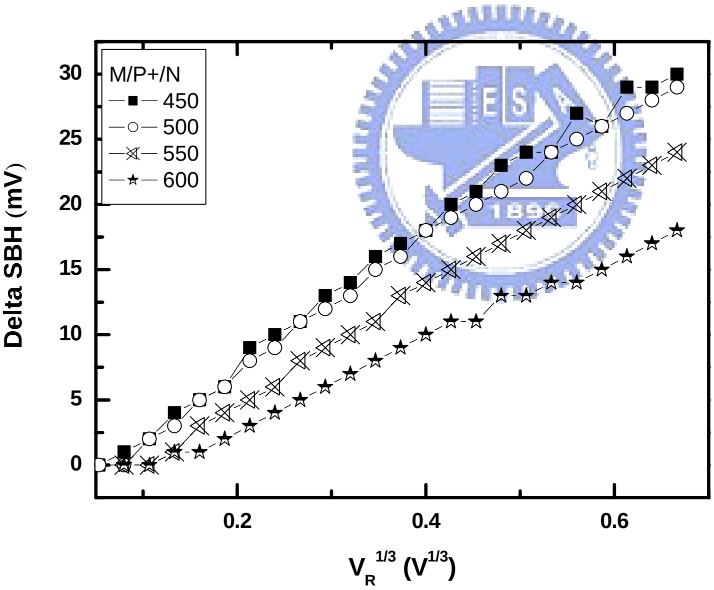


Fig. 5.7. Schottky barrier height lowering versus (a) $V_R^{1/2}$ and (b) $V_R^{1/3}$ which correspond to image-charge-induced schottky barrier lowering and inhomogeneous schottky barrier height induced electron dipole effect, respectively

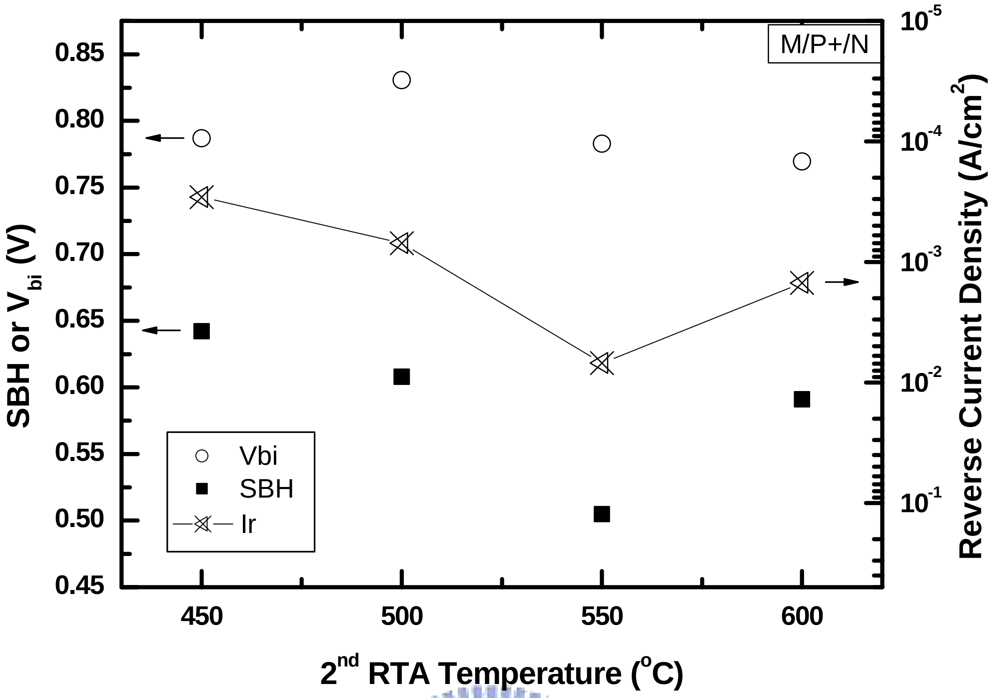


Fig. 5.8. V_{bi} (C-V method), SBH (I-V-T method) and Ir (I-V method) of M/P$^+$/N samples obtained from different 2^{nd} RTA temperatures

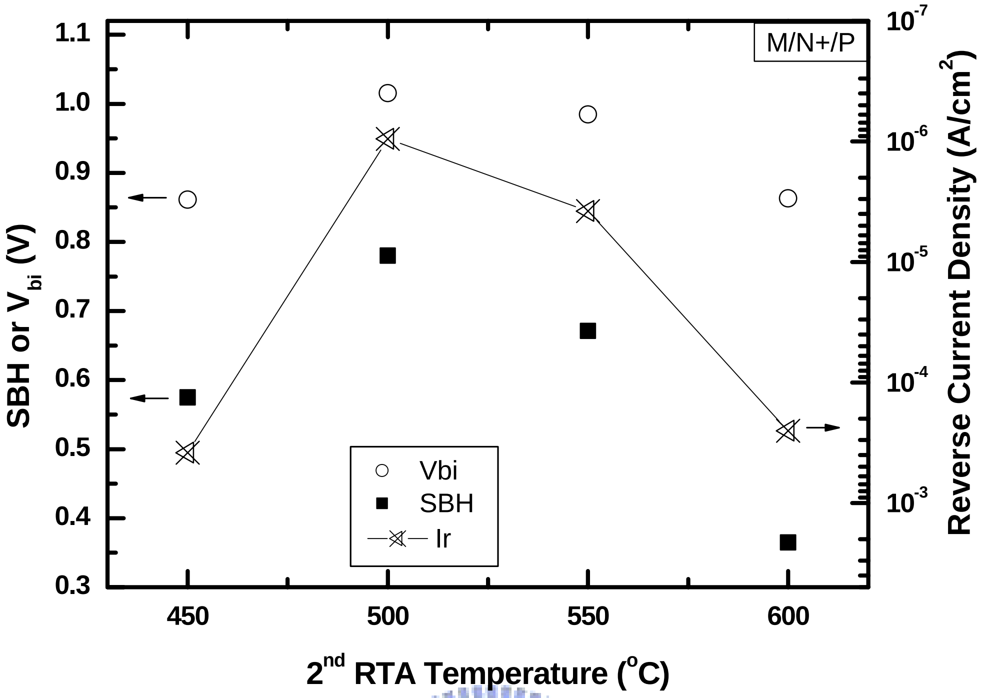


Fig. 5.9. V_{bi} (C-V method), SBH (I-V-T method) and Ir (I-V method) of M/N$^+$/P samples obtained from different 2nd RTA temperatures

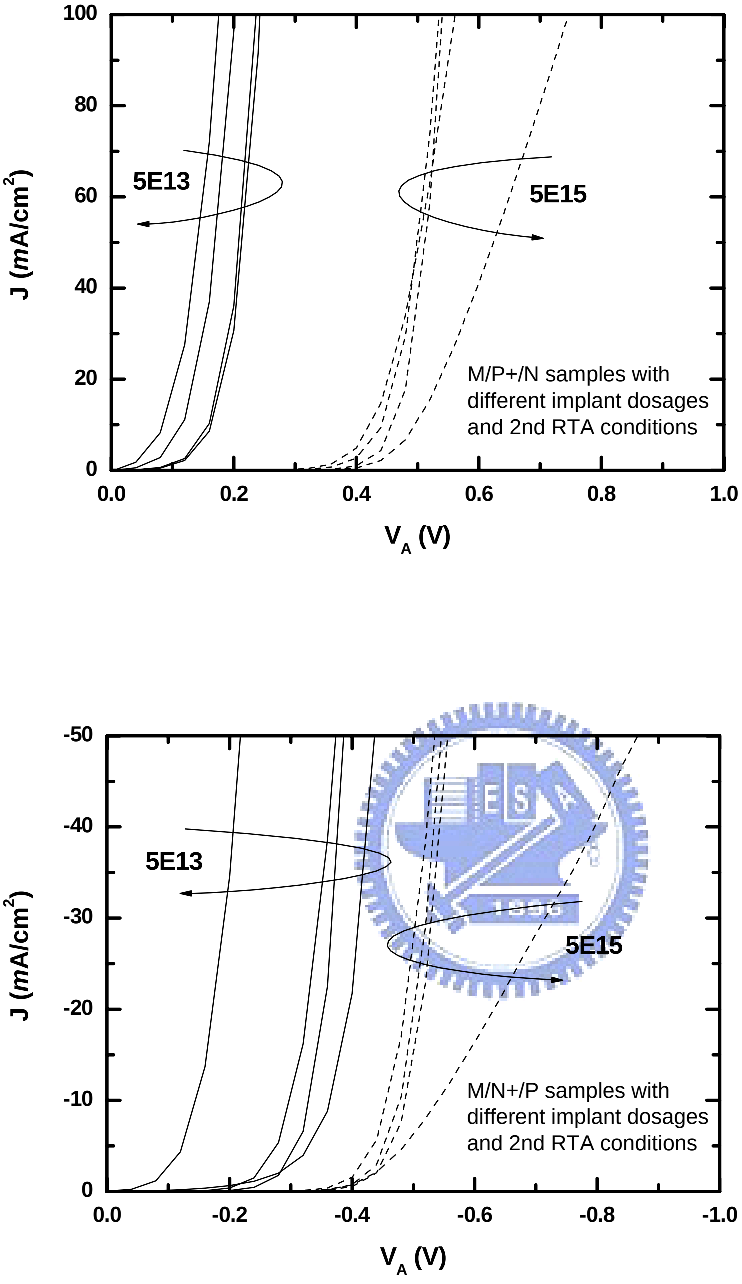


Fig. 5.10. Forward current density versus applied voltage for (a) M/P$^+$/N and (b) M/N$^+$/P samples with different dosages and 2nd RTA conditions

Chapter 6

THERMAL RELIABILITY OF JUNCTIONS FORMED BY IIS METHOD

6.1 Brief Introduction

Process integration of high-k dielectric is an important issue for manufacture of CMOS devices beyond the 45nm generation [1]. For ohmic contact consideration, traditional junction formation technology at source and drain (S/D) regions requires high temperature annealing, but this high-temperature process will affect not only the original dopant concentration profile but also make some high-k dielectric crystallized [2,3]. This made the integration of high-k dielectric material to gate first process difficult. Besides improving high-k dielectrics thermal reliability, implant into silicide (IIS) method provides an alternative possibility to give a solution to the integration of high-k gate material and gate first process by the relative low process temperature [4,5]. There are many studies showed that they had successfully manufactured PN junctions using IIS method, such like low contact resistance [6], low reverse current, high activation energy [7] and even been integrated in MOS device [8]. However, temperatures (around 400 to 600℃) used for IIS techniques are near the temperatures used in the back-end process conditions (i.e. some PE oxide are grown around 300℃ and forming gas annealing are often around 450℃). Few literatures have discussed the topic of how the post IIS thermal treatments impact on the device’s performance. In this study, additional RTA processes was introduced after the usual junction formation process done by IIS method to verified the thermal reliability issue.

6.2 Experiments

Two-port vertical diode structure was adapted in this study. Two different junction types were studied, $M/N^+/P$, and $M/P^+/N$. The starting material was (100) n-type and p-type silicon wafers, after thermal oxidation and active regions definition, backside of the n-type wafer was implanted with phosphorous 5×10^{15} cm^{-2} and backside of the p-type wafer was implanted with BF_2 5×10^{15} cm^{-2}. All samples were then be annealed with furnace at 1000℃ for 30 minutes. TaN 100 nm was sputtered on as the back contact. After dipped dilute HF to remove the native oxide at the active region, 20nm nickel was deposited by e-gun system. All samples were treated with 1st RTA at 350℃ 30s, after un-reacted Ni removed, n-type substrate samples were ion implanted with BF_2 5×10^{13} cm^{-2} or 5×10^{15} cm^{-2} and p-type substrate samples were ion implanted with phosphorous 5×10^{13} cm^{-2} or 5×10^{15} cm^{-2}. Finally, the usual samples were treated at 2nd RTA 60s with different temperatures from 450℃ to 600℃, 50℃ per step. The detailed process flow is the same as our previous works [4,5] (also the same in chapter 3,4) for heavily implanted samples and the same as in chapter 5 for lightly implanted samples. Their electrical properties were introduced in previous chapters. For the thermal reliability test, heavily implanted samples were added an extra 3rd RTA step and also a 4th RTA step at the same process temperature used in 2nd RTA step (i.e. 450℃ to 600℃, 50℃ per step). And for lightly implanted samples, an extra 3rd RTA or longer 2nd RTA treated samples are discussed.

The major measurement methods used in this study were I-V and C-V measurement. I-V measurements were measured with HP4156C, and C-V measurements were processed with HP4284 at 50 kHz.

6.3 Results and Discussions

6.3.1 Heavily implanted samples

6.3.1.1 I-V and C-V measurement results for M/P$^+$/N junction

For heavily implanted ($5x10^{15}$ cm^{-2}) M/P$^+$/N samples, the implantation peak was in the silicon (refer to Fig. 4.1). According to chapter 4 [5], the activation behavior could be divided into two mechanisms. At 2nd RTA thermal treatment lower than 550℃ 30s, SPER mechanism dominate the activation behavior and above 550℃ 30s, the bulk activation dominates. The I-V and C-V measurement results of the device treated with three different thermal conditions (Case 1: 2nd RTA 60s, Case 2: 3rd RTA 30s is added after Case 1, and Case 3: 4th RTA 30s after Case 2 is done) are shown in Fig. 6.1.

As shown in Fig. 6.1(a), with temperature between 400 to 500℃, the reverse bias current density (J_{off} at V_R=2V) is lowered with more thermal treatments (more RTA times). This could be explained by the C-V results shown in Fig. 6.1(b). Since the position of the PN junction deepens toward the heavily doped region, the higher the effective doping densities it activates, the lower the defects it faces. As the result, samples in Case 3 have better performance comparing to samples in Case 2 with the same temperature treatment. Also samples in Case 2 have better performance comparing to samples in Case 1 with the same RTA temperatures. And in this implantation condition, the SPER and bulk activation mechanisms encounter at 550℃. At Case 2, the device treated at 550℃ has the lowest J_{off} comparing to all samples (Case 1, 2, and 3) in this study. This might due to that SPER process is almost completed in this condition. In addition, leakage currents of samples in Case 2 with the thermal treatment above 550℃ are lower than those of Case 1. This improvement might due to the SPER process is not complete even though junction of samples treated with higher 2nd RTA temperatures, 600℃ and 650℃, in Case 1 are changed to be dominated by the bulk activation mechanism. As the result, with an additional thermal treatment (Case 2), the device's performance is improved. This also implies that both SPER and bulk activation mechanisms are co-exist and occur simultaneously when samples are thermal activated. Furthermore, in Case 3, the reverse bias currents have dramatically increased when 4th RTA are performed above 550℃ (Fig. 6.1(a)), however, at the same time, the C-V measurement results not change too much. The increase of J_{off} in Case 3 might mainly due to that defects are generated at these temperature range [9] (see also chapter 3).

6.3.1.2 I-V and C-V measurement results for M/N^{+}/P junction

For heavily implanted ($5x10^{15}$ cm^{-2}) M/N^{+}/P, the implantation peak was in the silicide (refer to Fig. 3.4). In this group, the junction activation might mainly due to the silicide assisted dopant activation (chapter 4 and reference 5). Here, three different thermal treatment cases are studied, Case 1: 2nd RTA 60s, Case 2: 3rd RTA 30s is added after Case 1, and Case 3: 4th RTA 30s after Case 2 is done. The corresponding I-V and C-V results are shown in the Fig. 6.2. For samples in Case 1 below 550℃, since the activation process is still not complete, with an additional thermal process (Case 2), the J_{off} is decreased due to the dopant activation, junction re-growth, and junction extending.. And for process temperature above 550℃, Fig. 6.2 shows that the J_{off} becomes worse when additional thermal process is treated (both Case 2 and Case 3). This is mainly thought of the defects in the silicon are generated at this temperature range. These phenomena are similar to the M/P^{+}/N junction just discussed above. However, there are still some differences between M/P^{+}/N and M/N^{+}/P junctions. First difference arises at the lower temperature range of the M/N^{+}/P junction that J_{off} in Case 3 increases significantly than in the Case 2. The origin of this decayed junction performance couldn't be explained by the dislocation generation, because most of dislocation generates at the temperature above 550℃. Furthermore, if the dislocation generation is the main reason for this decayed performance, we should find the similar phenomenon at the M/P$^+$/N junction but we didn't. The best explanation of this situation is to use the concept of the dopant de-activation due to the supersaturation of the phosphorous dopant in the silicon. First, since phosphorous is slow diffused, and the N$^+$/P junction position is close to silicide/silicon interface. The de-activation occurs in the heavily doped region might near the depletion region of the PN junction and become the defect centers to generate leakage current. Secondly, the relative high activated doping density of the M/N$^+$/P junction than M/P$^+$/N junction would make the de-activation more easily (the higher defect densities) to be observed. Thirdly, the leakage currents are higher in the lower temperature treatment situation, since the lower the temperature, the lower the solid solubility of the phosphorous in the silicon and the more significant supersaturation situation it is. These factors make the stronger de-activation occur at the M/N$^+$/P junction than M/P$^+$/N junction, especially in the low temperature treatment samples.

The C-V curves of the M/N$^+$/P junctions are distorted at the 600 and 650℃ treatments in Case 3. As shown in Fig. 6.3, the distortions have two different types. Type I (Fig. 6.3(a)) has the lower activated densities near the PN interface, or the more linear junction behavior it is. On the other hand, type II (Fig. 6.3(b)) distortion has the higher effective doping densities near the PN junction interface, or the hyper junction like behavior. Both two type distortion are found in the 600℃ treat samples, but only type I (linear junction like) distortions are found in 650℃ treat samples. The type I distortion is easy be understood by considering the dopant diffusing process.

With the added thermal process proceeding, phosphorous are sustained diffused into the boron-doped substrate and activated, this makes the P region of the N^+/P junction be counter-doped. Although the quantity is not huge, the depletion width changed of the lightly doped side could not be ignored when using C-V measurement method. As the result, the properties of the linear junction, or lower effective doping densities near the PN interface will be discovered. What is more interesting is the origin of the type II distortion. Since we know that the C-V measurement results are mainly due to the lightly doped region. In this case the boron-doped substrate is the dominated one, so the increasing of the boron doping densities might be the pile up of boron due to the dopant segregation behavior under the silicide formation process. This statement should be true for all cases and samples, but only some samples could find this phenomenon. Back to the first observations that no M/P^+/N samples find the type II junction behavior, this is rational because boron is faster diffuser in silicon than phosphorous is. The pile up of the phosphorous might be mostly in the heavily activated P^+ region and is not significant in the N side. On the other hand, the reason for why not all M/N^+/P samples have the type II junction behavior, the suggested explanation is described as follows: Although boron is faster diffuser than phosphorous in the same condition, however, in our interest case, phosphorous is much heavily doped than boron is, hence has a higher doping densities gradient and a deeper diffused region. Therefore, in most cases, boron piled up in the heavily N^+ region, and has little affect for the C-V measurement. However, with the added thermal treatment, for some samples, phosphorous might be deactivated and let the boron pile up region appear at the P side. As the result, type II junction behavior might only be measured in these samples.

6.3.2 Lightly implanted samples

The I-V measurement results of lightly doped sample are shown in Fig. 6.4. For lightly implanted samples, samples with three different kind thermal treatments are discussed. Case A: samples were treated with 2nd RTA 60s at different temperatures. Case B: An extra 3rd RTA 60s were introduced at the same temperature as 2nd RTA. Case C: samples were treated with 2nd RTA 120s at different temperatures.

For $M/P^+/N$ diode, shown in Fig. 6.4(a), for Case A, it looks like the activation process is best completed at 450℃, and J_{off} increases as temperature increases. There is a J_{off} drop at 600℃ for Case A. With added 3rd RTA, Case B, J_{off} become worse at 450℃ and 500℃, this might cause by the dopant de-activation due to the supersaturation. And for 550℃ and 600℃ samples, the J_{off} is improved. These improvement above 550℃ could also be found for the heavily doped case. The improvement might be contributed to the recovery of some defects that already generated in the previous thermal treatment. Although we don't know what is the defect type recovered in these samples, we can conclude that defects are both generated and recovered above 550℃ and the process widow for the defect recovery mechanism dominate is relative small and hard to control. Finally, for Case C, the J_{off} differs only a little among all samples and when comparing to Case A and Case B samples, it shows that Case C samples are not in the best conditions. All samples suffer same high defect levels.

Fig. 6.4(b) shows the I-V measurement results for the $M/N^+/P$ diode. Samples treated at 500℃ demonstrate the best performance in all the cases. Dopant de-activation under 500℃ and defect generated above 500℃ are both significant. This observation is similar to the result for the heavily implanted samples. Thermal treatment at 500℃ might have the widest time process window for the $M/N^+/P$ diode.

Also, samples treated at 650℃ in Case C, the defect recovery behavior is also be observed.

The C-V results of the lightly implanted samples are less reliable than heavily implanted samples. For heavily implanted samples, the abrupt junction assumption vanished only for M/N+/P diodes treated at Case 3 (RTA 60s+30s+30s) above 600℃. However, the abrupt junction assumptions only hold in Case A for lightly implanted samples. Resembling to the Type I and Type II C-V distortions in heavily implanted samples, as shown in Fig. 6.5, there are also two different kinds of C-V distortions in the lightly implanted samples. First of C-V distortion in lightly implanted samples is linear junction like behavior shown in Fig. 6.5(a) and this distortion are found in all samples in Case C and most samples in Case B (except samples treated at 600℃). The linear junction like behavior could be explained similar to the Type I distortions for heavily implanted case. When an additional thermal treatment processed (most samples in Case B), majority carriers not only diffused from the N^+ region into the p-substrate and also activated there. This situation is easy to be found with a long-term thermal treatment (Case C). This distortion could be concluded that junction is deepened from the silicide/silicon interface into the substrate, this supported our previous work in chapter 3 that real junction position of the PN junction is moved when device undergone thermal treatment. And with less defects in the substrate region, the easier C-V distortion behavior to be observed: light implanted case compare to heavily implanted case, and also Case C (deeper junction position, far from the silicide/silicon interface) versus Case A for light implanted case. This might due to the less the dopants, the slower the diffusing and activation speed. Hence, the non-uniform PN interface would easy be observed. The second kind of distortion, hyper junction like, is similar to the Type II C-V distortion in the heavily implanted case. Interestingly, this kind of distortion is only found in the M/N$^+$/P samples with additional thermal treated at 600℃ (the C-V results for corresponding lightly implanted M/P$^+$/N samples are shown in Fig 6.6 for comparing). This implied that the origin of this kind C-V distortion might due to the dopant itself, for example diffusion coefficient and activation behavior. This observation agrees to our suggested explanation in the previous section. In addition, the different of C-V and I-V results for samples demonstrated in Case B and Case C suggested that even samples are treated at the samples thermal budget, RTA 60s+60s versus RTA 120s at same temperature, the dopant and defect distributions differ one to another. Not only thermal treated at the stable temperature region is important at the junction formation process, the rising and cooling temperature processes also play an important role.

6.4 Conclusion

For junctions formed by IIS method, heavily implanted samples might have better thermal stability than lightly implanted samples. For heavily implanted case, although the C-V measurement result differs only a few, the I-V measurement changes a lot. The I-V measurement is more sensitive to the defect present in the junction area. There are at least two different mechanisms for junction degrading for IIS formed junction. Above 550℃, defect formation due to silicon itself might be the obvious one, and for temperatures lower than 500℃, de-activation caused by the supersaturation of dopant dissolved in the silicon might dominate. When junction is under an additional thermal process, there are two kinds of C-V distortion patterns could be observed. One distortion pattern has the characteristic that the activated doping density at the PN junction interface is more linearly distributed. This pattern corresponds to the junction extension process. On the other hand, the second C-V distortion pattern has observed that there is higher effective substrate doping density near the PN interface. This might due to the dopant segregation effect, and the observation of this distortion pattern is also related to the substrate and implanted dopant characteristics such like diffusion and de-activation attributes. In addition, the thermal budget is not the only key factor to the junction formation process, the heating and the cooling process also have significant impact to the junction formation.

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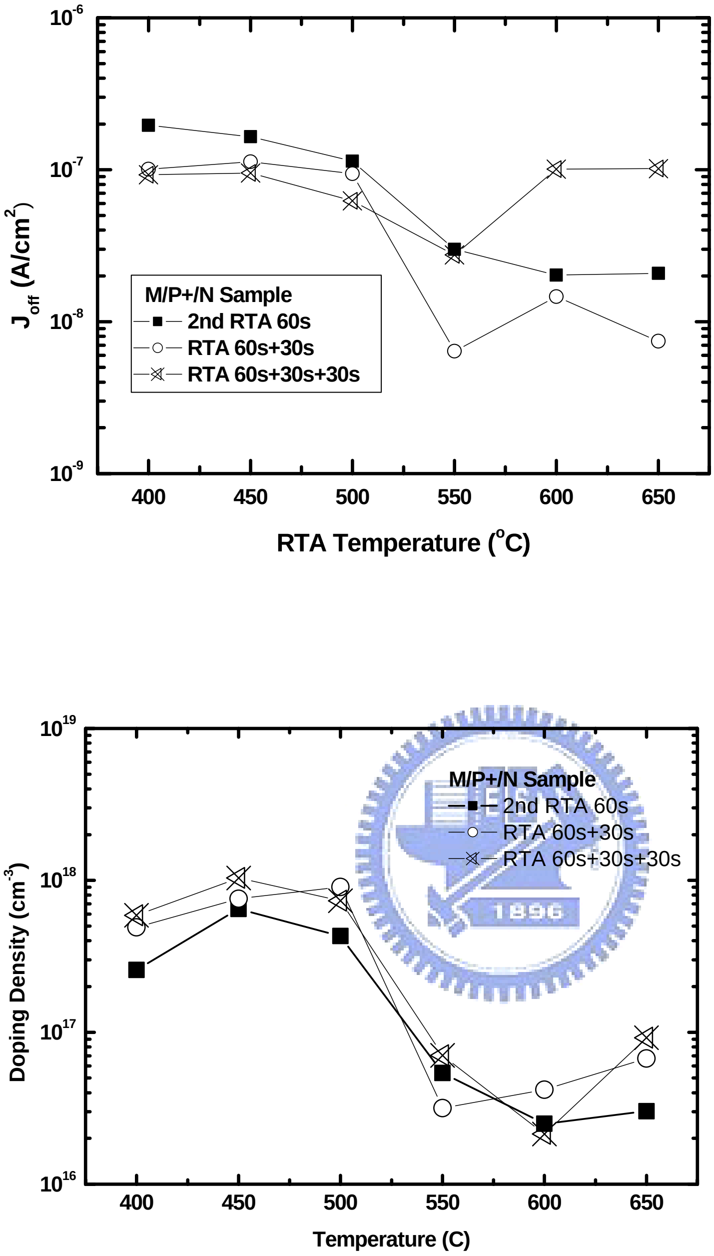

Fig. 6.1. (a) Reverse current density (I-V method) and (b) Effective doping density extracted from C-V method versus different process conditions for heavily implanted M/P^+/N samples

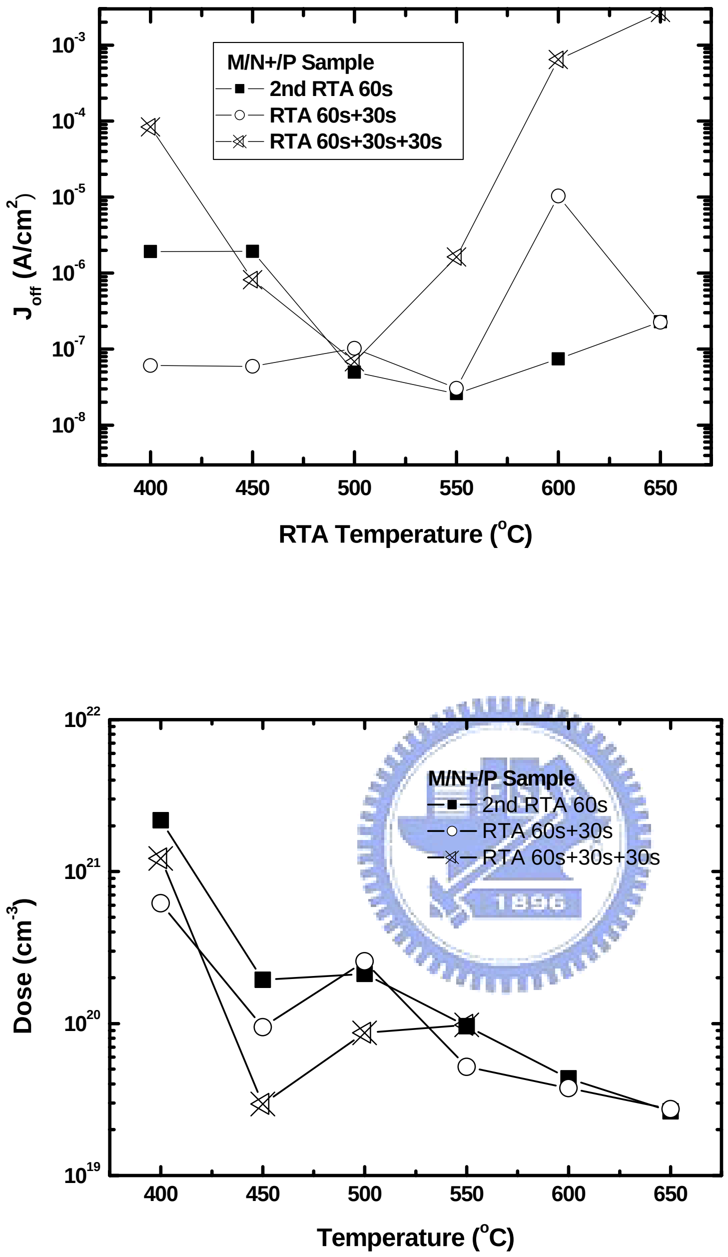

Fig. 6.2. (a) Reverse current density (I-V method) and (b) Effective doping density extracted from C-V method versus different process conditions for heavily implanted M/N$^+$/P samples

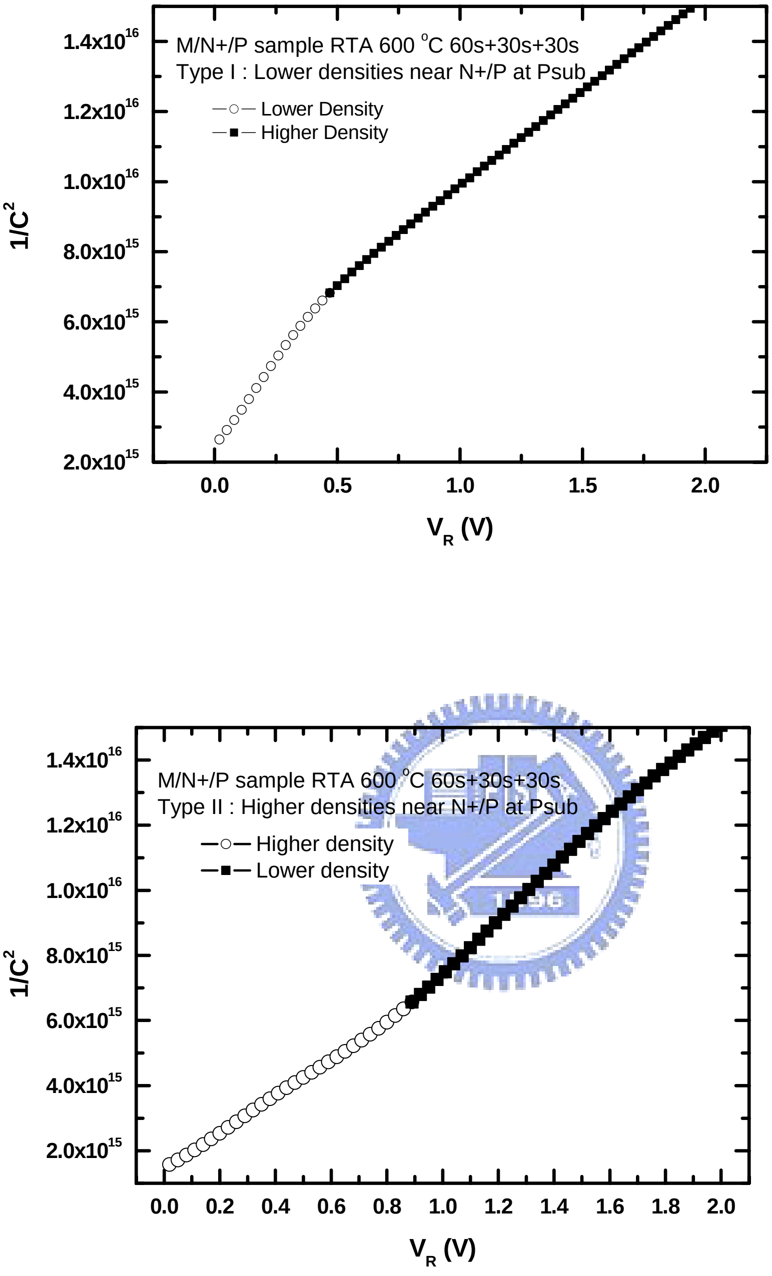

Fig. 6.3. (a) Type I C-V distortion and (b) Type II C-V distortion for the heavily implanted M/N$^+$/P samples with 600℃ RTA 60s+30s+30s

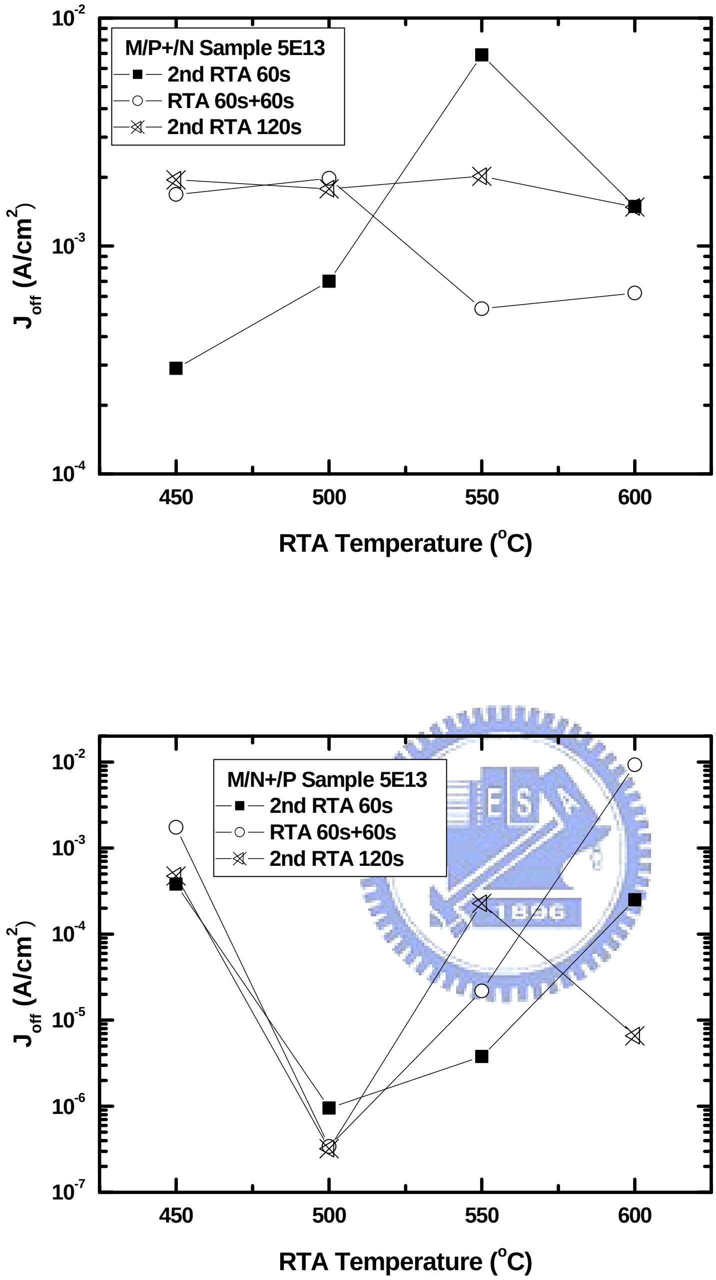

Fig. 6.4. Reverse current density (I-V method) for lightly implanted (a) M/P$^+$/N and (b) M/N$^+$/P samples verse different process conditions

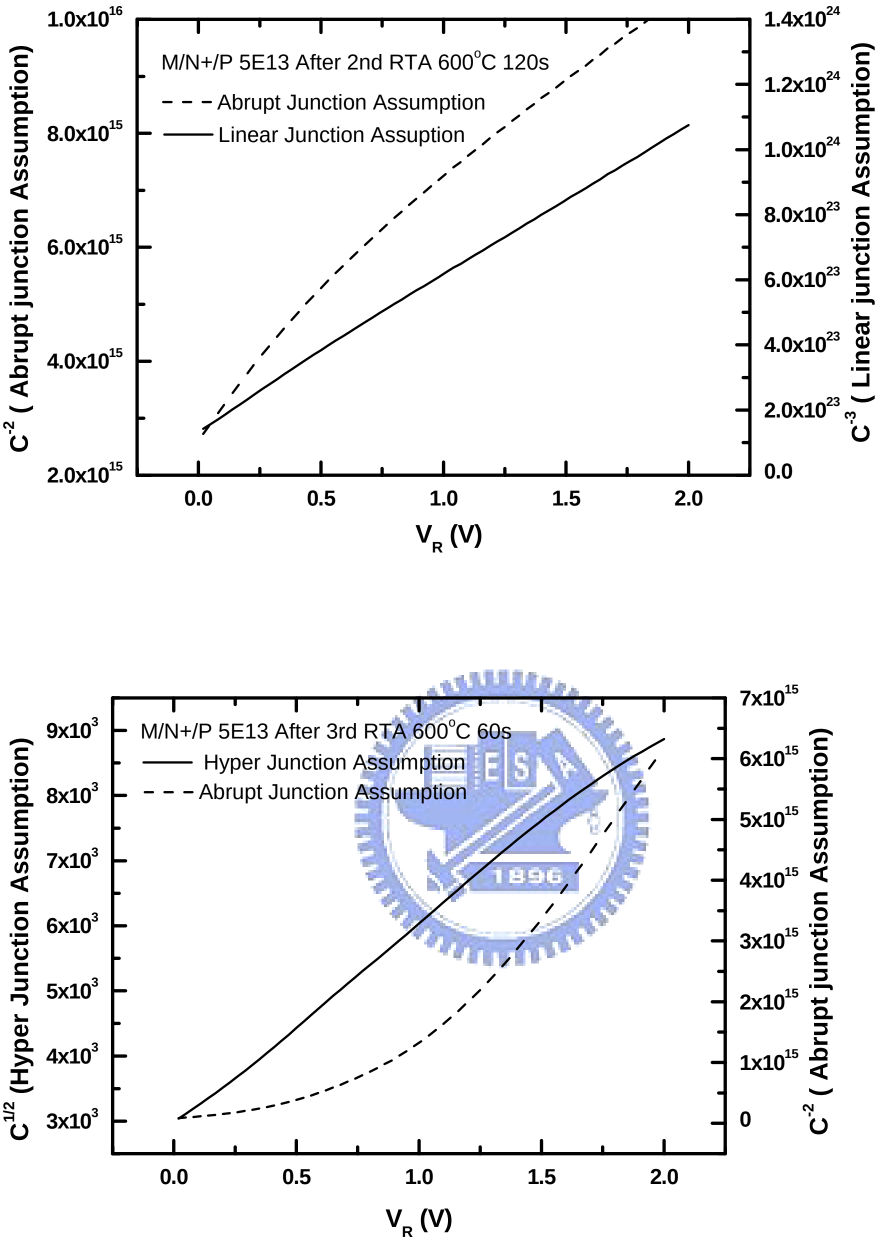

Fig. 6.5. Two different kinds of C-V distortions for lightly implanted M/N$^+$/P sample treated at RTA 600℃ (a) 120s (gradual junction like) and (b) 60s+60s (abrupt junction like)

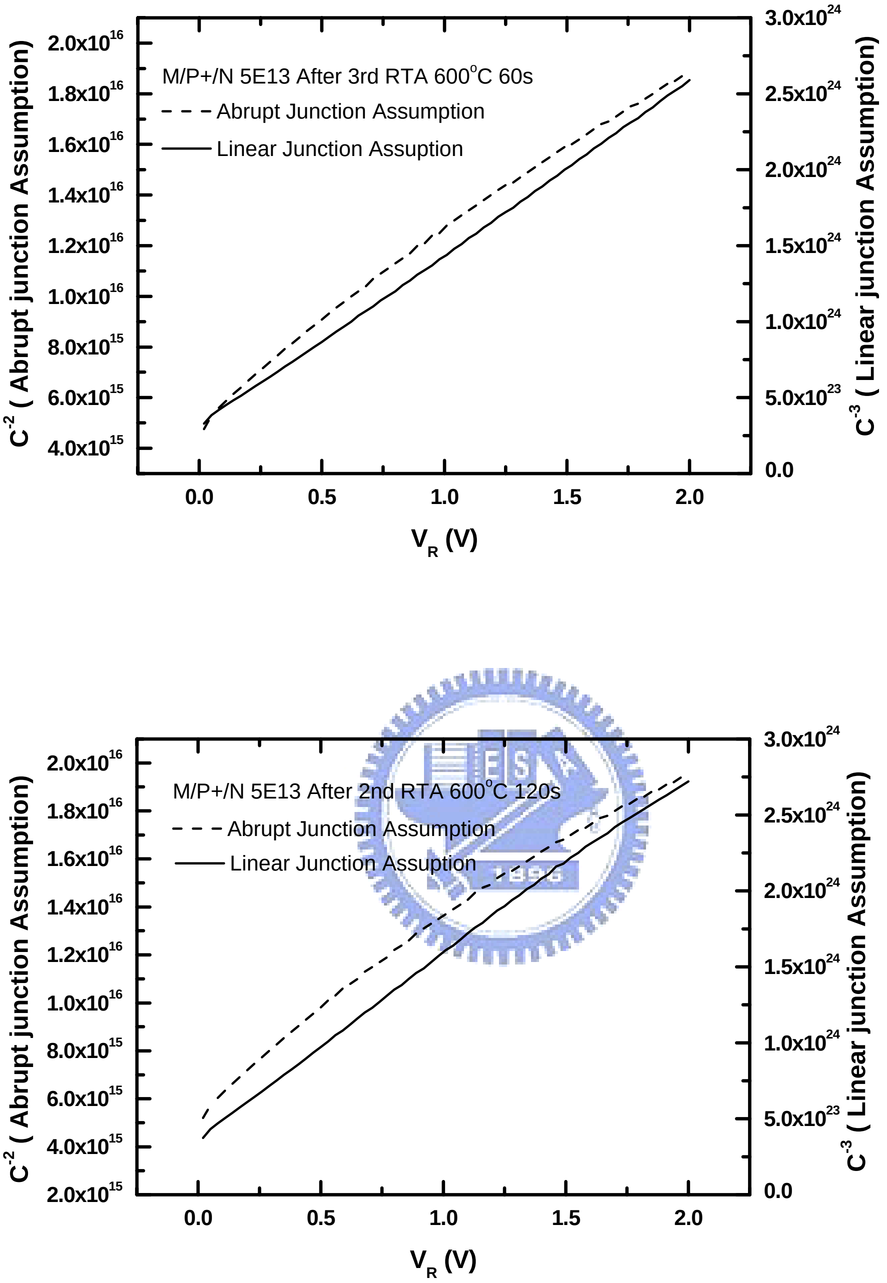

Fig. 6.6. Only one kind of C-V distortion for lightly implanted M/P$^+$/N sample treated at RTA 600℃ (a) 120s and (b) 60s+60s (both gradual junction like)

Chapter 7

SUMMARY AND FUTURE WORK

7.1 Summary

At first part of this thesis, we described and tried to explain the junction formation behaviors of the IIS method how it formed and why dopant could activate at low temperature. The junction formation process of IIS method could be contributed to three mechanisms: first, near the silicon/silicon interface, metal assisted activation is notable, and secondly, at the heavily doped region where SPER caused activation behavior is obvious, and finally, with higher activation temperature, above 600℃ in the case in chapter 4, bulk activation dominates the junction's position and its behavior. Before bulk activation dominates the junction's behavior, the junction formation process is starting at the M/S interface and then extending into the silicon substrate. The mechanism, which would be the dominated one of the junction formation process, depends on the implantation energy (projection range), implanted dosage (quantity of the impurity), diffusion coefficient of the dopant, thermal solubility of the dopant, and the thermal treatment condition itself (both temperature and time). For boron and phosphorous studied in this study, boron not only has faster diffusion coefficient than phosphorous but also has higher (bulk) activation ability at low temperature range ($\leq$ 650℃). This makes boron doped sample when activated using IIS method easy fall in SPER caused activation or bulk activation dominate region. These factors make boron doped sample hard to form very shallow junction (where heavily doped region is fully depleted during device operation, the region is estimated fall around 1 nm range). On the other hand, phosphorous doped sample which junction activation is mostly dominated by metal assisted activation could be used to form very shallow junction.

In second part of this thesis, based on the understanding of the junction's behavior in the first part, we try to connect the junction's electrical properties and the junction's physical properties. However, the physical properties are difficult to be direct measured, most physical parameters used here were just qualitatively described but not quantitatively determined. Experimental results showed that for M/N$^+$/P samples, doping densities extracted from C-V methods could be used to approximate the phosphorous doping activation densities near the M/S interface. It showed that with higher activated doping densities near the M/S interface, the higher the SBH would be obtained from the I-V-T measurement and the lower the reverse biased leakage current. And for M/P$^+$/N samples, the junction behaves with both the characters of M/P$^+$ junction (when V_R<0.1V) and M/N (whole behavior). Combined with C-V measurement results, it implied that the M/P$^+$/N junction in this study could be treated as two individual junctions in series but with strong coupling effects between them. And for thermal reliability issue, junctions formed by IIS method, heavily implanted samples might have better thermal stability than lightly implanted samples. In addition, comparing to C-V measurement method, I-V measurement is more sensitive to the defect present in the junction area and more suitable be used to observe the thermal reliability issue of the junction. When junction is under an additional thermal process, there were two kinds of C-V distortion patterns observed in this study. One distortion pattern had the characteristic that the activated doping density at the PN junction interface was more linearly distributed. This pattern corresponded to the junction extension process. On the other hand, the second C-V distortion pattern had observed that there was higher effective substrate doping density near the PN interface. This might due to the dopant segregation effect, and the observation of this distortion pattern was also related to the substrate and implanted dopant characteristics such like diffusion and de-activation attributes.

7.2 Future Work

We have widely discussed the junction formed by IIS method at many aspects from the low temperature activation ability, junction formation behavior (also provide possible mechanisms), some relationships between the process parameters to the electrical properties and also some notes on the thermal reliability issues. But there are still many works could be studied. We divided the future work into two parts: 7.2.1 junction characteristics modeling, and 7.2.2 applications.

7.2.1 Junction characteristics modeling

Modeling most depends on correct physical parameters for doping densities and junction depth, however, these data are still hard to direct measured for us at this time. Most other researches use SIMS to explain the dopant distribution, but lack of the activation information. In this study we use C-V measurement method but C-V method has its spatial resolution limitation, restricted by Debye length. That is why in this study we only use C-V method as a tool to describe the “average” behavior, but not focus on the exact doping quantity calculation. And the junction depth here we are interested in is about 1nm deep. It is hard to use SRP method to precisely determined the junction’s position, since many factors will effect the experimental result, such like interface roughness and band narrowing effect of the heavily doped region. Some special kinds of TEM might tell the junction position, but TEM could tell only localized information and lack of information about the activation ability. These are topics should be classified but undone, waited for some more studies devote on.

After physical parameters are determined, the systematical study for large sample size diodes should be measured to model the I-V behavior. Recent studies have some predictions to junction’s behavior by simulation. But the assumptions are hard to be verified in the device fabrication. That originates from lacking information about the device parameters just stated above in 7.2.1. In this study, we used comparing to determine the relative junction depth and doping levels. Only could conclude some relationship between process parameters and final junction’s behavior qualitatively. More accurate model need pay more effort to establish.

7.2.2 Applications

Although the model of the IIS formed junction is not clear, we can also take the advantage of the high activation ability in low temperature to many different kinds of applications: 1. Gate first process integrates with high-k material. 2. S/D contact for the TFT device. 3. Contact for solar cell.

Gate first process for high-k device is limited by the thermal reliability of the high-k dielectric. If using IIS method at S/D region might provide more choices for the high-k dielectric selection. TFT S/D contact activation limited by the substrate property. Traditionally, TFT S/D activation need long time period, for introducing IIS method, the S/D contact formation process might be improved. Also, the contact issue for solar cell is limited by the dopant diffusion (p-i-n) structure, high temperature might thin the intrinsic layer and worse the photo-electric efficiency, but contact resistance will also worse the voltage generated of the solar cell. Introducing IIS method to solar cell might improve the contact resistance and provide better cell performance.

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博士論文題目：

中文：藉由離子佈植進入矽合金法在低溫活化下形成的接面研究

英文：A Study of Low Temperature Activated Junction Formed by Implant Into Silicide Method