Chapter 1

Introduction

1.1 Motivation to study MIM capacitors

Radio frequency (RF) and mixed-signal integrated circuits employ capacitor elements for decoupling, filtering, and oscillating etc. In the past, these capacitors have typically been polysilicon–insulator–polysilicon (PIP) and MOS devices [1.1]-[1.2]. However, as polysilicon and substrate tend to exhibit depletion effects, the impact of associated parasitic capacitance cause undesirable capacitance variations with voltage bias fluctuations. Although this is not a problem in many integrated circuits, in analog mixed-mode circuits (such as analog-to-digital converters, for example), this cannot be tolerated due to the precision requirements for scaled process technologies [1.3]–[1.6]. Cross-coupled capacitors have been employed to alleviate this large variation of capacitance with applied voltage (VCC) without any unconventional approach [1.3]. However, the resistance of the capacitor plates is high, and the excessive capacitive loss to the substrate results in poor quality factor (Q) at very high-frequency applications. This motivates the need for a capacitor with electrodes exhibiting little or no depletion effect. Therefore, the MIM capacitor has

been the most popular analog/mixed-signal/RF (AMS/RF) capacitor, due to an inherent advantage that metal provides depletion-free, high-conductance electrodes suitable for high-speed applications at low cost. The planar MIM capacitor structure offers the advantage of flexibility in inserting it below the top metal level of a multilevel backend of line process, where capacitive loss to the Si substrate is minimized [1.7]. Alternatively, it can be inserted between two intermediate metal levels for applications requiring such a design [1.7]-[1.8]. In contrast to nonplanar MIM capacitors, this approach utilizes state-of-the art production toolsets and is designed to be fully planar and integratible into a backend process consisting of two or more levels of wiring. Furthermore, this planar design is inherently scaleable to different capacitor values and flexible to alternative dielectric materials, in single or multiple layers.

In mixed-signal circuits, the level of performance obtainable is ultimately limited by the accuracy of the passive components employed. This is in turn dependent on properties between individual capacitor elements and by the stability of these elements to maintain values independent of fluctuations in the operating conditions, such as voltage applied and temperature. Shifts in capacitance lead to distortions in analog signals, which can be up-converted to higher frequencies in mixers and nonlinear circuit applications [1.1], [1.2], [1.5], [1.6], [1.9]. The variation

in the capacitance with the applied voltage and temperature is known as the voltage (VCC) and thermal (TCC) coefficient of capacitance, respectively. The requirements for a precise capacitor are a) small capacitance variation on a chip, and b) low VCC and TCC coefficients, defined, respectively, as [1.2], [1.10]:

$$VCC = \frac{10^6}{C}\frac{dC}{dV}\frac{ppm}{V} \tag{1}$$

$$TCC = \frac{10^6}{C}\frac{dC}{dT}\frac{ppm}{K} \tag{2}$$

where V is the voltage applied between the plates of the capacitor, and T is the capacitor temperature. For simplicity, the dependence of capacitance on voltage and temperature can also be approximated by

$$C(V) \approx C_o(1 + VCC1 \times V + VCC2 \times V^2) \tag{3}$$

$$C(T) \approx C_o(1 + TCC1 \times T + TCC2 \times T^2) \tag{4}$$

where VCC1 and TCC1 are linear voltage and temperature coefficient of capacitance and VCC2 and TCC2 are the quadratic voltage and temperature coefficients of capacitance, respectively. The emphasis is on the capacitors second-order voltage linearity since it is critical for the dynamic range of analog circuit as highlighted in the ITRS 2004 [1.12]. The first-order component of voltage linearity can be cancelled out by differential techniques such as cross-coupled arrangement [1.3]. There was a great amount of effort on studying and reducing the capacitor dispersion phenomenon with varying applied voltage [1.9]–[1.11].

1.2 Motivation to study MIM capacitors using high-κ dielectrics

For mixed-signal and RF devices, especially in mobile applications, it is essential to reduce the capacitor area because the area percentage of capacitor significantly increases with the scaledown of logic parts. Furthermore, the capacitors used for electrostatic discharge can occupy a significant section of circuit area. In RF applications, a high degree of linearity is required for capacitors to minimize harmonic generation and improve balancing. Integration of high-quality and high-density MIM capacitors is a challenge for the RF transceiver roadmap. The need to integrate new materials in a cost-effective manner to realize high-density MIM capacitors follows the guideline published in the ITRS roadmap [1.12]. Potential solutions for MIM capacitors include the introduction of high-k dielectrics now being developed for future use for gate dielectrics[1.13]-[1.27]. Therefore the high-κ dielectrics used in MIM capacitors have evolved from SiON (κ~4-7) [1.14]-[1.16], Al_2O_3 (κ=10) [1.24], HfO_2 (κ~22) [1.18]-[1.22], Ta_2O_5 (κ~25) [1.23], [1.26] to Nb_2O_5 (κ~40) [1.27]. However, the demonstration of MIM with these films is yet able to achieve properties such as nondispersive, good linearity and high breakdown with low leakage concomitantly, at high unit capacitance. Furthermore, since ICs benefiting from high performance interconnects will invariably operate at frequencies exceeding

1 GHz, it is important that the dielectric constant and its anisotropy be carefully characterized at these frequency. In the reported high-κ MIM, the electrical measurements were performed at much lower frequencies where on-chip and test setup parasitic could be neglected. In addition, it is also essential to study the interface of the electrode/high-κ dielectric interface, especially the bottom electrode which is being exposed to the precursors during the deposition. Since it is know that leakage can be interface or bulk dominated. In addition, it has been reported the traps present in the dielectric resulted in the dispersive capacitor behavior. It is thus, useful to investigate the types of traps or fixed charges in the film in order to minimize the defective population via process optimization.

1.3 The measurement of the Devices

To investigate the electrical characteristics of our devices, we measured the leakage current, stress induced leakage current using HP 4156A semiconductor parameter analyzer. Besides, HP4284A precision LCR meter was used to evaluate the capacitance and the conductance ranging from 100 kHz to 1 MHz. Furthermore, to investigate the characteristics of our devices at the frequency above 1 MHz, we measured the scattering parameter using HP8510C network analyzer and the test set. The measurement set-up for S-parameter is shown in Fig. 1-3. Network analyzer generates a calibrated RF signal and has three input measuring channels. These are

commonly called the R, the A, and the B channels. The R channel is used to measure the incident voltage, and the A and B channels measure reflected and transmitted voltages. Then, we can obtain S_{11} and S_{21} by calculating A/R and B/R in polar form, respectively. The S_{12} and S_{22} can also be obtained using the same way except changing the input voltage channel. The noise figure and associated gain were measured by HP85122A and ATN-NP5B noise parameter extraction system up to 6 GHz. There are three major categories of measurement type that the system can supply: DC, S-parameters, and noise parameters. The first two categories mainly support the noise parameter measurement.

1.4 Innovation and Contribution

First, In this thesis, we have developed the Ir/TiTaO/TaN capacitor has high κ value of 45, high capacitance density of 10-23 fF/μm^2 and low leakage current without crystallization, even after backend processing. This improvement is due to the added TaO inside the TiO matrix that blocks the TiO crystallization from material science. To further reduce the leakage current in small bandgap (E_G) TiTaO, a high work-function (ϕ_B) Ir (5.2 eV) electrode is used to give >one order of magnitude lower leakage current than Al. This performance of the TiTaO MIM capacitors is accompanied by small capacitance reduction and voltage-dependence of capacitance (ΔC/C) at RF regime. These MIM capacitors should be suitable for precision RF

circuits.

Second, we report improvements in the thermal leakage current by integrating both high ΔE_C TiHfO dielectric and high work-function (ϕ_m) Ni as a high work function top electrode. Economically it is also better to use Ni than Ir, which has been reported and used previously in CMOS. This avoids sacrificing the overall κ value by using a multi-layer or laminate structure, and results in better voltage linearity, which is important for analog/RF ICs.

Third, we further improve κ to 147~169 and capacitance density to 28-49 $fF/\mu m^2$, or capacitance-equivalent-thickness (CET) of 1.25-0.70 nm for unified multi-functional SoC. Such large capacitance density with low leakage current was achieved by using very high-κ $SrTiO_3$ (STO) with formed micro-crystals (3~10 nm). This small poly grain size is also important to reduce variation among devices. In addition, a plasma nitridation was applied to bottom TaN that prevents CET degradation by forming interfacial TaON during STO post-deposition anneal (PDA) or using expensive conductive noble electrodes, such as Pt, Ru, and Ir. Moreover, we have studied STO MIM capacitor for RF application. Very high capacitance density of 44 $fF/\mu m^2$, high κ value of 147 and small capacitance variation with frequency and voltage are obtained at the same time that demonstrates the excellent device performance for RF application. These high performance capacitors can drastically

reduce the RF capacitor area, yet can be fabricated with full compatibility with current VLSI process lines.

Finally, we have studied the stress reliability of low energy-bandgap, high-κ $SrTiO_3$ metal-insulator-metal capacitors under constant-voltage stress. By using a high work-function Ni electrode (5.1 eV), we reduced the degrading effects of stress on the capacitance variation ($\Delta C/C$), the quadratic voltage-coefficient-of-capacitance (VCC-α) and the long term reliability, compared with using TaN. The improved stress reliability for Ni electrode capacitors is attributed to a reduction of carrier injection and trapping.

[1]	Year of Production		2010	2012	2013	2015	2016	2018
	Technology Node		hp45		hp32		hp22	
	DRAM ½ Pitch (nm)		45	35	32	25	22	18
[2]	Minimum Supply Voltage	Digital design (V)	0.7	0.7	0.65	0.65	0.6	0.6
[3]		Analog design (V)	1.8–1.2	1.8–1.2	1.8–1.0	1.8–1.0	1.5–1.0	1.5–1.0
[4]	NMOS Analog Speed Device	T_{ox} (nm)	0.5–0.8	0.5–0.8	0.4–0.6	0.4–0.6	0.4–0.5	0.4–0.5
[5]		g_m/g_{ds} at $5 \cdot L_{min\text{-}digital}$	100	100	100	100	100	100
[6]		1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	150	150	100	100	75	75
[7]		σV_{th} matching ($mV \cdot \mu m$)	2.5	2.5	2	2	1.5	1.5
[8]	NMOS Analog Precision Device	T_{ox} (nm)	3–2	3–2	3–1.3	3–1.3	2.5–1.3	2.0–1.3
[9]		Analog V_{th} (V)	0.3–0.2	0.3–0.2	0.3–0.2	0.3–0.2	0.3–0.2	0.3–0.2
[10]		g_m/g_{ds} at $10 \cdot L_{min\text{-}digital}$	300	300	300	300	300	300
[11]		1/f Noise ($\mu V^2 \cdot \mu m^2/Hz$)	200	200	150	150	100	100
[12]		σV_{th} matching ($mV \cdot \mu m$)	7.5	7.5	6	6	5	5
[13]	Analog Capacitor	Density ($fF/\mu m^2$)	5	5	7	7	10	10
[14]		Voltage linearity (ppm/V^2)	<100	<100	<100	<100	<100	<100
[15]		Leakage ($fA/[pF \cdot V]$)	7	7	7	7	7	7
[16]		σ Matching ($\% \cdot \mu m$)	0.4	0.4	0.3	0.3	0.2	0.2
[17]	Analog Reststor	Parasitic capacitance ($fF/\mu m^2$)	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02	0.1–0.02
[18]		Temp. linearity ($ppm/^oC$)	30–60	30–60	30	30	30	30
[19]		1/f-current-noise per current² ($1/[\mu m^2/Hz]$)	6×10^{-19}	3×10^{-19}	3×10^{-19}	3×10^{-19}	2×10^{-19}	2×10^{-19}
[20]		σ Matching ($\% \cdot \mu m$)	1.7	1.7	1.5	1.5	1.2	1.2
[21]	Bipolar Analog Device	g_m/g_{ce} at $W_{e\text{-}min}$ *	1050	1050	1000	1000	950	950
[22]		1/f-noise ($\mu V^2 \cdot \mu m^2/Hz$)	1.5	1.5	1	1	0.7	0.7
[23]		σ current matching ($\% \cdot \mu m^2$)	20	20	20	20	20	20

Figure 1-1 The International Technology Roadmap of analog and mixed-signal capacitors

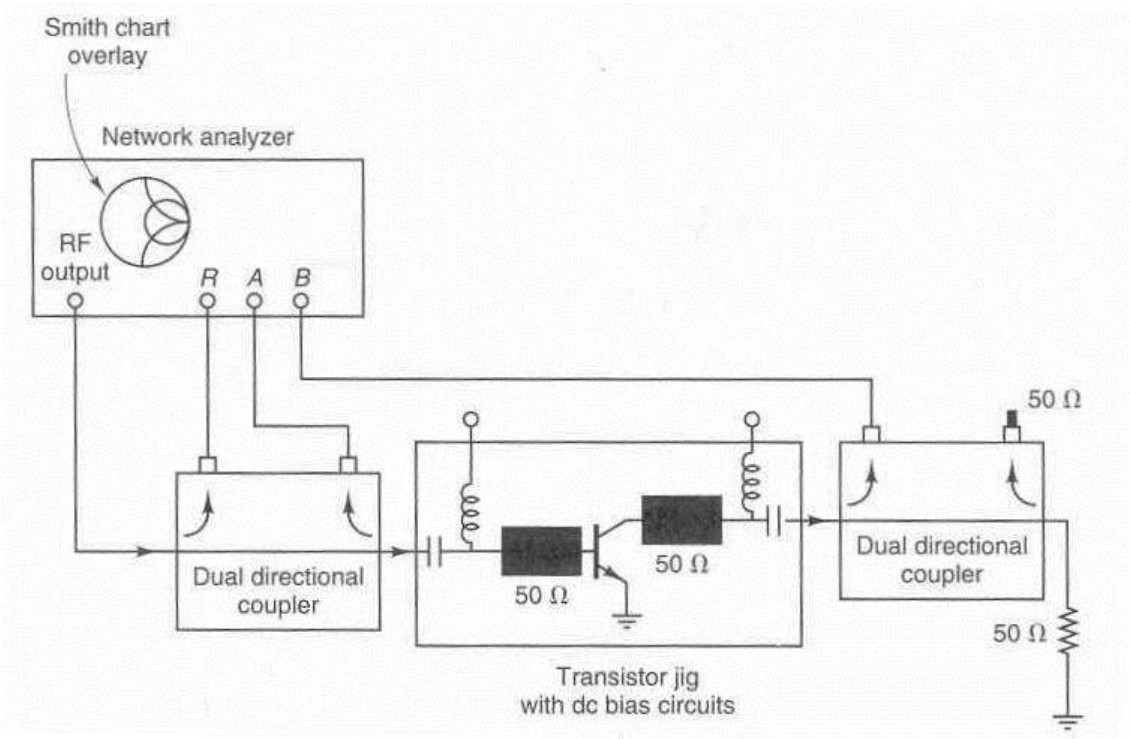


Figure 1-2 The measurement set-up for S-parameter

Figure 1-3 The illustration of HP85122A and ATN-NP5B noise measurement system

Chapter 2

High-κ Ir/TiTaO/TaN Capacitors Suitable for Analog IC Applications

2.1 Introduction

To achieve continuing improvements in mixed signal and RF integrated circuit performance, the sizes of both the active MOSFETs and the passive MIM capacitors [2.1]-[2.16] need to be scaled down. The technology challenge for the MIM capacitor is to achieve high capacitance density, low leakage current and small voltage linearity of the capacitance simultaneously [2.17]. To meet these device requirements, the use of high-κ dielectrics for the MIM capacitors is the only viable choice. This is because decreasing the dielectric thickness (t_d) needed for high capacitance density ($\varepsilon_0\kappa/t_d$) increases the leakage current and degrades the capacitor's voltage linearity.

In this paper we report novel Ir/TiTaO/TaN capacitors which show high capacitance density, small leakage current and low voltage linearity, simultaneously. The TiTaO dielectric capacitors also show good thermal stability, such as low leakage current after a 400°C thermal cycle associated with its backend process. This contrasts with TiO_2 dielectric capacitors which give high leakage current after 400°C

processing [2.16]. The excellent device performance arises from using the very high-κ TiTaO dielectric (κ=45) and high work-function Ir (5.2 eV). These are the first results that meet all the ITRS roadmap requirements for analog capacitors in the year 2018 - such as 10 fF/μm^2 capacitance density, leakage current <5.8 fA/[pF•V], and capacitance voltage linearity <100 ppm/V^2 [2.17].

2.2 Experimental

After depositing 2 μm SiO_2 on a Si wafer, the lower capacitor electrode was formed using PVD-deposited TaN/Ta bi-layers. The Ta was used to reduce the series resistance and the TaN served as a barrier layer between the high-κ TiTaO and the Ta electrode. Then $Ti_xTa_{1-x}O$ (x~0.6) dielectric was deposited by PVD, followed by a 400^{o}C oxidation and annealing step to reduce the leakage current. Different TiTaO thicknesses of 41 and 28 nm were used to study the voltage linearity in the devices. Finally, Ir was deposited and patterned to form the top capacitor electrode. The fabricated devices were characterized by *C-V* and *J-V* measurements using an HP4155B semiconductor parameter analyzer and an HP4284A precision LCR meter.

2.3 Results and discussion

Figure 2-1 shows the *C-V* characteristics of high-κ Ir/TiTaO/TaN MIM capacitors. Capacitance densities of 10.3 and 14.3 fF/μm^2 were measured for the 41 and 28 nm TiTaO dielectric devices, which give capacitance-equivalent thicknesses

(CET) of 3.4 and 2.4 nm, respectively. A high-κ value of ~45 was obtained from the measured capacitance density in the TiTaO dielectric. The ITRS requirement for analog capacitors, by 2018, is a density of 10 fF/μm^2, along with low leakage current and capacitance voltage linearity.

Figure 2-2 (a) shows the *J-V* characteristics of Ir/TiTaO/TaN MIM capacitors with 3.4 and 2.4 nm CET. High breakdown voltages of 14 and 20 V were measured for the 10.3 and 14.3 fF/μm^2 density device, well above values required for most analog function applications. The lower leakage current for electrons injected from the top Ir electrode, compared with the lower TaN electrode, is due to the higher work-function of Ir compared with TaN, as shown in the energy band diagram in Fig. 2-2 (b). The low leakage current of 1.2×10^{-8} A/cm^2 at 2V, or 5.8 fA/[pF•V], obtained for the 10.3 fF/μm^2 density device, meets the ITRS-required low leakage current of <7 fA/[pF•V] [2.17]. Such a low leakage current is due to the amorphous structure of the TiTaO being preserved, even after the backend processing involving 400^{o}C oxidation and N_2 annealing. This was confirmed by X-Ray Diffraction measurements.

For analog capacitors a low capacitance voltage linearity is important. Figure 2-3 (a) shows a *ΔC/C-V* plot for Ir/TiTaO/TaN MIM capacitors with 10.3 and 14.3 fF/μm^2 density. The *ΔC/C* decreases rapidly with decreasing capacitance density from 14.3 to 0.3 fF/μm^2, which is consistent with the decreasing trend of the leakage

current, as shown in Fig. 2-2 (a). We obtained a quadratic voltage linearity (α) of 89 ppm/V^2 for the capacitance, and a first order voltage linearity (β) of 178 ppm/V. These are the lowest reported values [2.1]-[2.16] needed to meet the 10 fF/μm^2 density for analog capacitors, as specified in the ITRS roadmap. Figure 2-3 (b) shows the variation of α as a function of CET or *1/C*. We note that the effect of β can be cancelled by circuit design [2.17]-[2.18]. An exponential decrease of α with increasing CET or *1/C* was observed for all the Ta_2O_5, HfO_2, Tb-doped HfO_2 and Ir/TiTaO/TaN capacitors [2.2], [2.7]-[2.8]. This may be due to the trap-related leakage current that has the exponential dependence with CET [2.6]. For the same CET or capacitance density value, the TiTaO device has the lowest α – this is due to the high κ value of 45 which exceeds the κ~22-25 values for HfO_2 and Ta_2O_5. We note that the exponential decrease with increasing *1/C* is important when designing capacitors to meet different requirements.

Table 2-1 summarizes the important device parameters for the analog capacitors. The high capacitance density, low leakage current at 2 V and low voltage linearity meet all the requirements described in the in the ITRS roadmap for analog capacitors. Such excellent capacitor device performance is due to the very high κ of 45 in the TiTaO dielectric, and the high work-function Ir electrode.

2.4 Conclusion

We have developed novel high-κ Ir/TiTaO/TaN capacitors which have high capacitance density (10.3 fF/μm^2), small leakage current at 2 V (1.2×10^{-8} A/cm^2), and low voltage linearity of the capacitance (89 ppm/V^2). These excellent results meet the ITRS roadmap requirements for precision analog capacitors for the year 2018. The good performance is due to the very high κ (45) achieved in the TiTaO dielectric and the high work-function (5.2 eV) provided by the Ir electrode.

Table 2-1. Comparison of various high-κ capacitors. All the requirements of the ITRS roadmap at 2018 are satisfied by the Ir/TiTaO/TaN capacitor.

	ITRS @ 2018	Ta_2O_5 [2.2]	Tb-HfO_2 [2.8]	HfO_2 [2.7]	**This work**	
C Density ($fF/\mu m^2$)	10	9.2	13.3	12.8	10.3	14.3
J (A/cm^2)	-	2×10^{-8} (1.5V)	1×10^{-7} (2V)	8×10^{-9} (2V)	1.2×10^{-8} (2V)	2×10^{-7} (2V)
J/(C•V) (fA/[pF•V])	<7	14.5 @1.5V	38 @2V	2.9 @2V	5.8 @2V	—
α (ppm/V^2)	α<100	3580	2667	1990	89	634
β (ppm/V)		2060	332	211	178	414

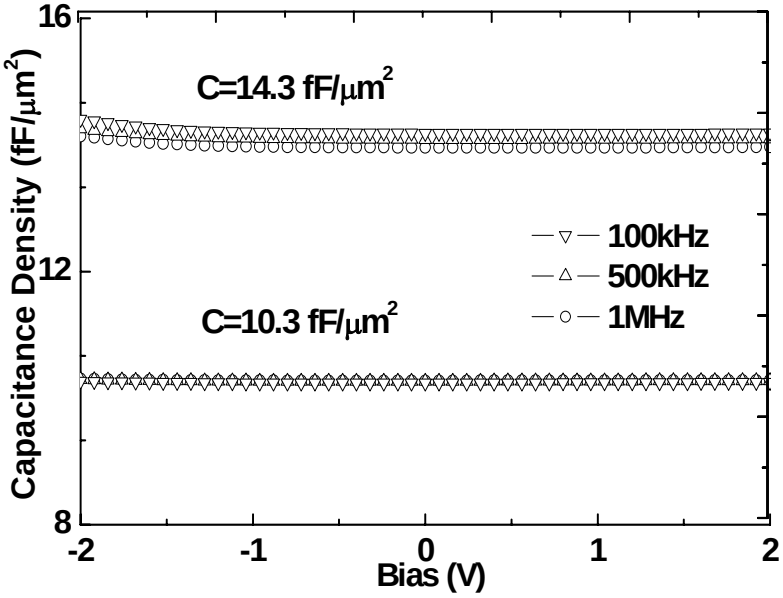
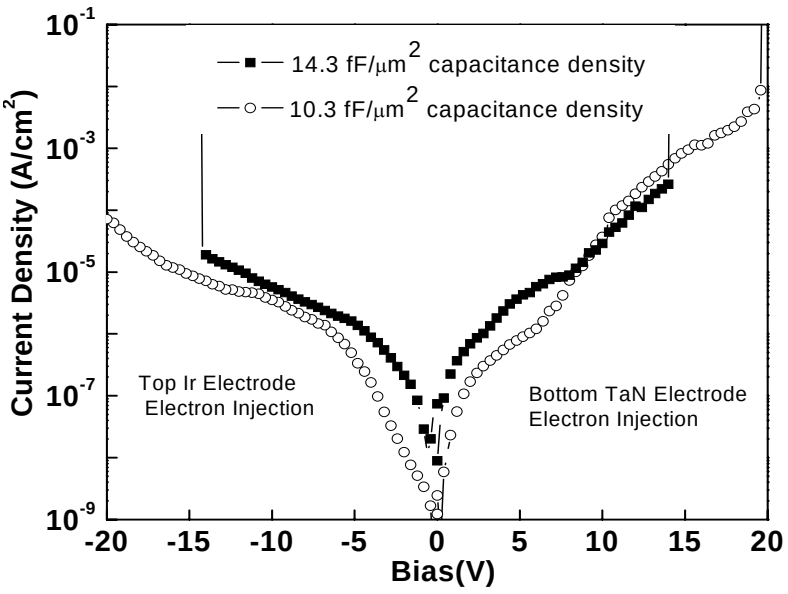
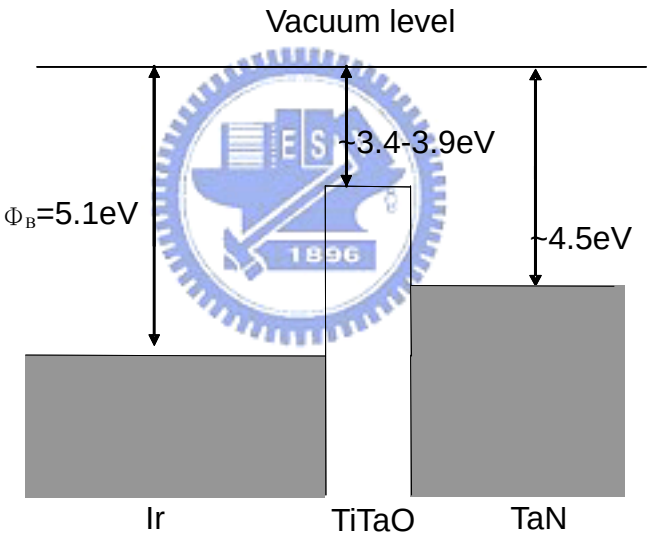


Figure 2-1 *C-V* characteristics of Ir/TiTaO/TaN TiTaO MIM capacitors.

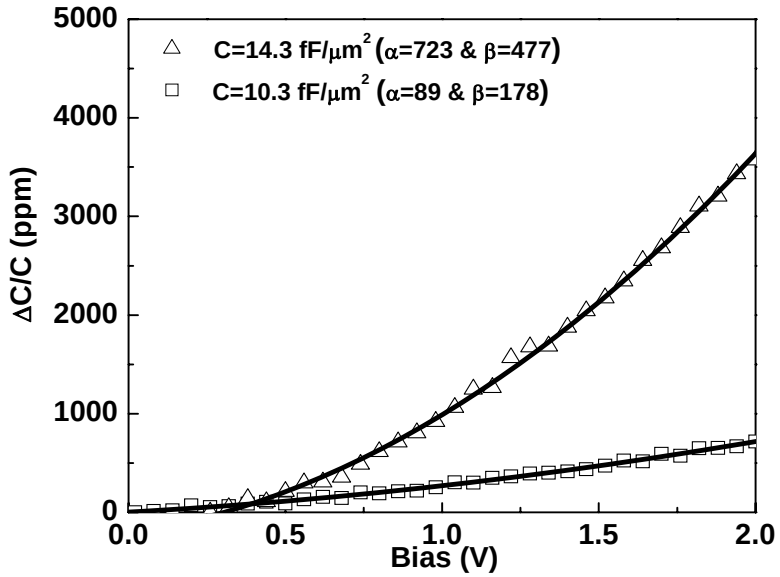


(a)

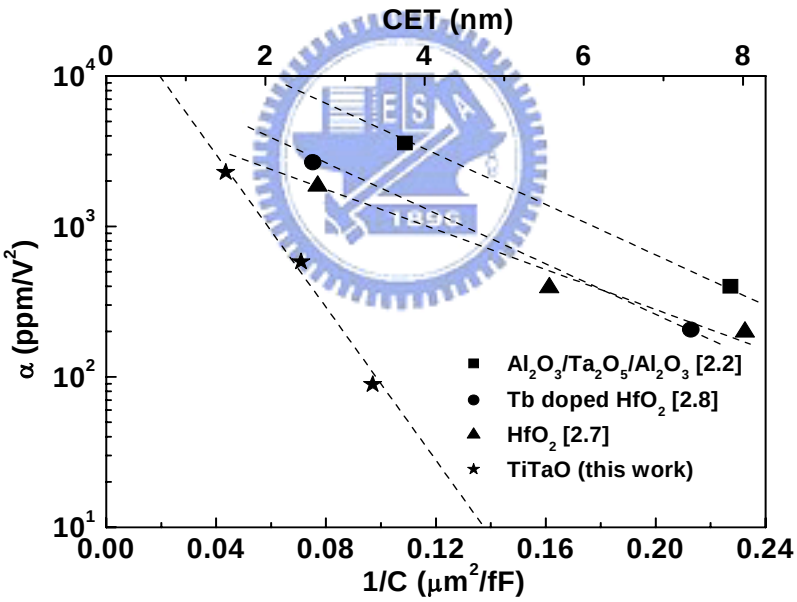


(b)

Figure 2-2 (a) *J-V* characteristics of Ir/TiTaO/TaN MIM capacitors. (b) Band diagram of the Ir/TiTaO/TaN MIM structure. The leakage current is lower when electrons are injected from the top Ir electrode than from the lower TaN electrode.



(a)



(b)

Figure 2-3 (a) *ΔC/C-V* and (b) *ΔC/C-1/C* plot for Ir/TiTaO/TaN MIM capacitors.

Chapter 3

Very High Density (23 fF/μm^2) RF MIM Capacitors Using High-κ TiTaO as the Dielectric

3.1 Introduction

According to International Technology Roadmap for Semiconductors (ITRS), continuous down-scaling of the size of MIM capacitors is required to reduce chip size and the cost of analog and RF ICs. The use of a high-κ dielectric [3.1]-[3.10] is the only way to achieve this goal, since decreasing the dielectric thickness (t_d) to achieve high capacitance density ($\varepsilon_0\kappa/t_d$) degrades the leakage current, loss tangent and voltage dependence of the capacitance ($\Delta C/C$). Hence the high-κ dielectric in MIM capacitors has evolved from using SiON (κ~4-7) [3.2]-[3.3] and Al_2O_3 (κ=10) [3.8] to HfO_2 (κ~22) [3.5]-[3.7] or Ta_2O_5 (κ~25) [3.9]. To increase the κ value beyond 25, the dielectric TiO_2 is a potential candidate, since it can display very high-κ (~80). However, the large leakage current from crystallization of the TiO_2 is a major limitation for device applications. Here we report the use of TiTaO as the dielectric, and show capacitors with low leakage current and without crystallization, even after

backend processing. We report devices with a record high density of 23 fF/μm^2, a high-κ value of 45 (beyond the previous κ~25 barrier), and low leakage current of 1.2×10^{-6} A/cm^2. This performance of the TiTaO MIM capacitors is accompanied by a small voltage-dependence of capacitance (ΔC/C) of only 770 ppm at 1GHz. Compared with current technology these high performance capacitors can drastically reduce the RF capacitor area, yet can be fabricated with full compatibility with current VLSI process lines.

3.2 Experimental

High-κ TiTaO MIM capacitors were fabricated on 4-in Si wafers. First, a 0.5μm thick isolation SiO_2 was deposited on the Si substrates. The bottom capacitor electrodes were formed by depositing 0.05μm TaN on a 1 μm Ta layer, followed by patterning. Then 17 nm thick $Ti_xTa_{1-x}O$ (x~0.6) was deposited on the TaN/Ta electrode, followed by 400^{o}C oxidation and annealing. Finally, Al was deposited and patterned to form the top capacitor electrode and RF transmission lines. For comparison purposes devices with TiO_2 as the dielectric was also fabricated using the same process. The fabricated RF MIM capacitors were characterized using an HP4284A precision LCR meter from 10 KHz to 1 MHz, and an HP8510C network analyzer for the S-parameter measurements from 200 MHz to 20 GHz [3.8]-[3.10]. The series inductance and RF pads were de-embedded from a ‘though’ and ‘open’ transmission

lines [3.11], respectively. The RF frequency capacitance was extracted from the measured S-parameters using an equivalent circuit model [3.10].

3.3 Results and discussion

Figure 3-1 shows the X-Ray Diffraction patterns of 28 nm thick TiO_2 and TiTaO layers, which were used to examine the thermal stability on their amorphous structure. Significant crystallization of the TiO_2 was measured after a 400^oC O_2 treatment for 10 min which became worse after subsequent 30 min N_2 annealing. In contrast the TiTaO was amorphous after the same thermal cycle. This good stability after backend thermal treatment is important in reducing the leakage current in RF MIM capacitors.

Figure 3-2 (a) and 3-2 (b) show the C-V and J-V characteristics of TiTaO and TiO_2 MIM capacitors. For the TiTaO device a record high capacitance density of 23 $fF/\mu m^2$ was measured, giving a high-κ value of ~45, which is greater than the κ~22-25 value for HfO_2 and Ta_2O_5 which are used in DRAM. However the TiO_2 MIM capacitor showed an abnormal capacitance variation at voltages above ±0.75 V. In contrast, constant capacitance values, with little voltage and frequency dependence, were found for the TiTaO MIM capacitor. The poor C-V for the TiO_2 MIM capacitor is related to its large leakage current, Fig. 3-2 (b), which may be due to the current conduction through grain boundaries of the poly-crystalline TiO_2. The TiTaO MIM capacitors have ~5-7 orders of magnitude lower leakage current than that for the TiO_2

devices. For a large 8 pF capacitor, 20 μm × 20 μm in size, the leakage current was as low as 8 pA (1.2×10^{-6} A/cm^2) at 1V, and lower than the leakage current of sub-100nm transistors [3.11]. The leakage current, injecting electrons from the Al contact, is lower than that from using the lower TaN electrode. This is due to the better interface for the Al, which also gives better voltage and frequency dispersion in the C-V curves.

Figure 3-3 shows the measured S-parameters for a TiTaO MIM capacitor. The capacitance at RF frequencies can be extracted from S-parameters using the equivalent circuit model shown in the insert. The frequency dependent capacitance value is shown in Fig. 3-4 (b). The small capacitance reduction of 1.8% from 100 kHz to 10 GHz indicates good device performance over the IF to RF range.

Figure 3-4 (a) displays the ΔC/C-V characteristics, where the data >1 MHz were calculated from the measured S-parameters using a circuit-theory derived equation [3.10]. The RF capacitance value, ΔC/C at 2V, 1st order voltage linearity (β) and quadratic voltage linearity (α) [3.5] are shown in Fig. 3-4(b). The rapid ΔC/C reduction with increasing frequency above MHz regime may be due to the trapped carriers being unable to follow the high frequency signal [3.10], [3.12]. Here the typical carrier lifetime of trap-related Shockley-Read-Hall recombination is in the range ms to μs. The small ΔC/C of 550 ppm, low α of 81 ppm/V^2 and β of 98 ppm/V at 1 GHz are sufficient to meet the requirements of high-speed analog/RF IC

applications.

3.4 Conclusion

Very high 23 fF/μm^{2}capacitance density, with a capacitance reduction of only 1.8% from 100 kHz to 10 GHz, and a small 550 ppm ΔC/C at 1 GHz were simultaneously achieved in novel high-κ TiTaO MIM capacitors processed at 400^{o}C. These MIM capacitors should be suitable for precision RF circuits.

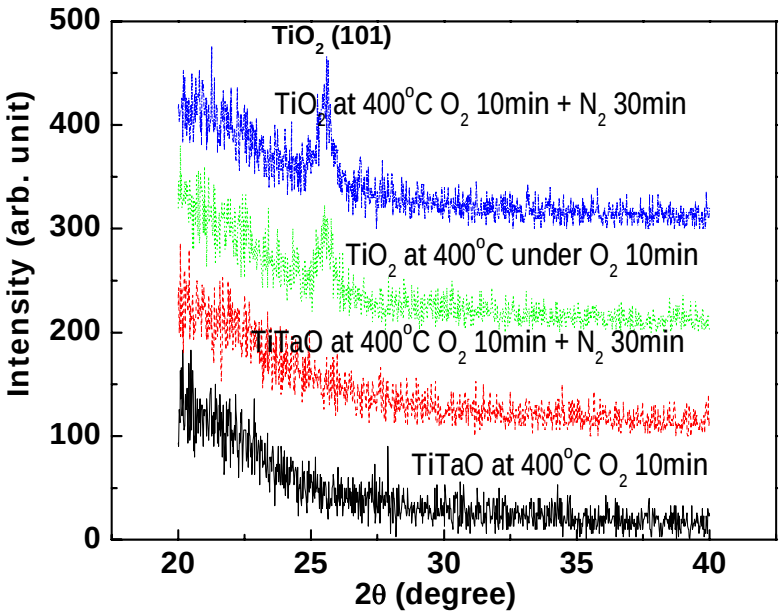
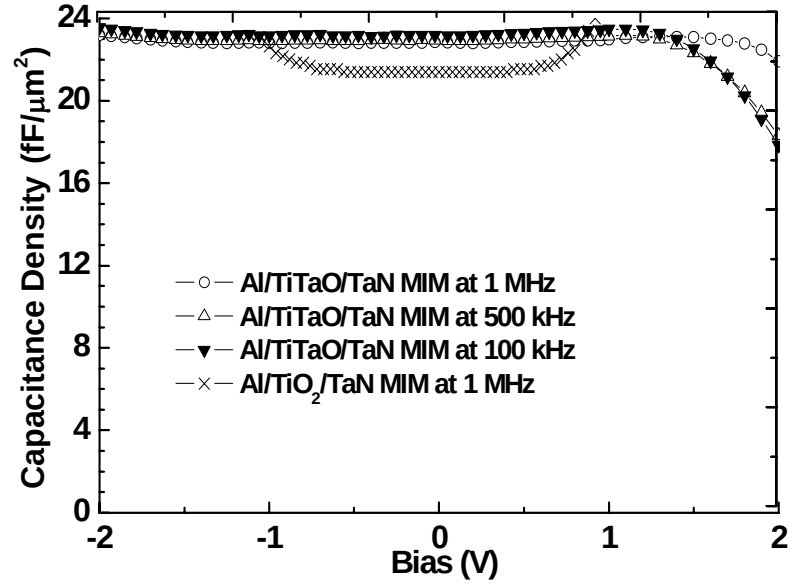
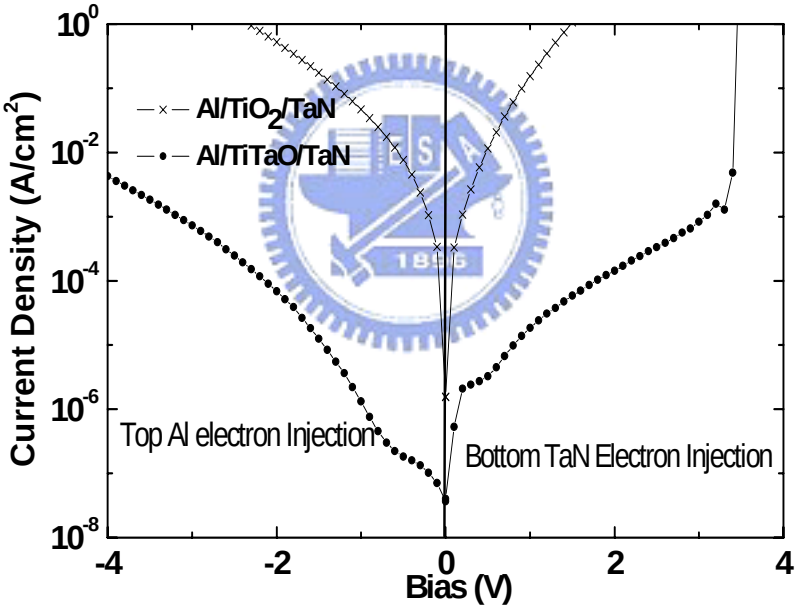


Figure 3-1 XRD patterns of TiO_2 and TiTaO dielectric layers, ~28 nm thick, after 400°C O_2 oxidation and N_2 annealing.



(a)



(b)

Figure 3-2 (a) C-V and (b) J-V characteristics of TiO_2 and TiTaO capacitors. The leakage current is lower in the TiTaO capacitors.

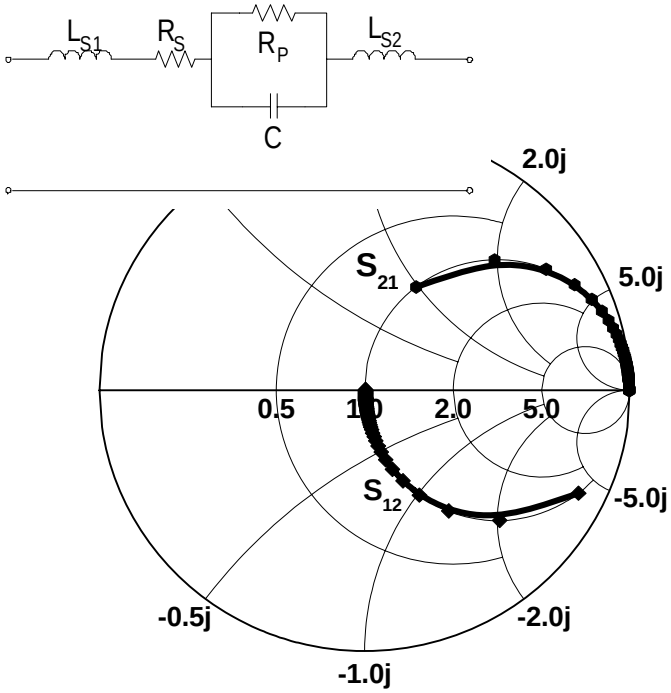
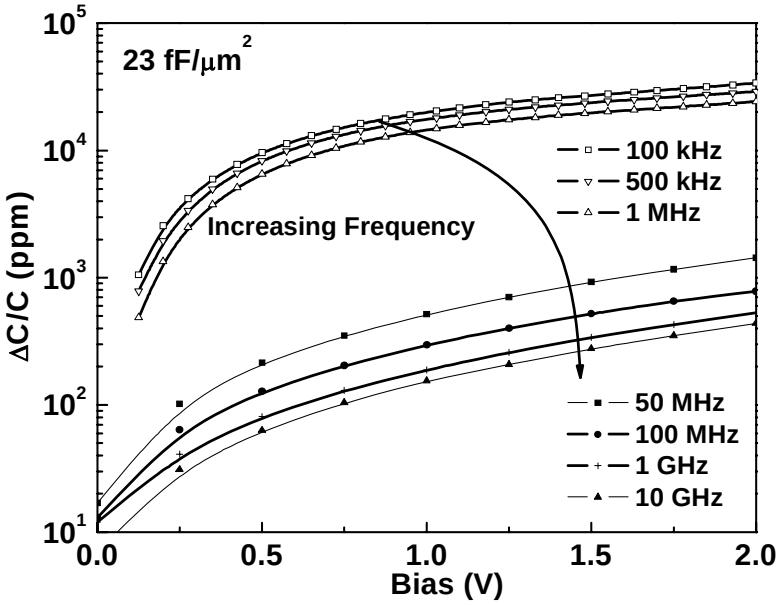
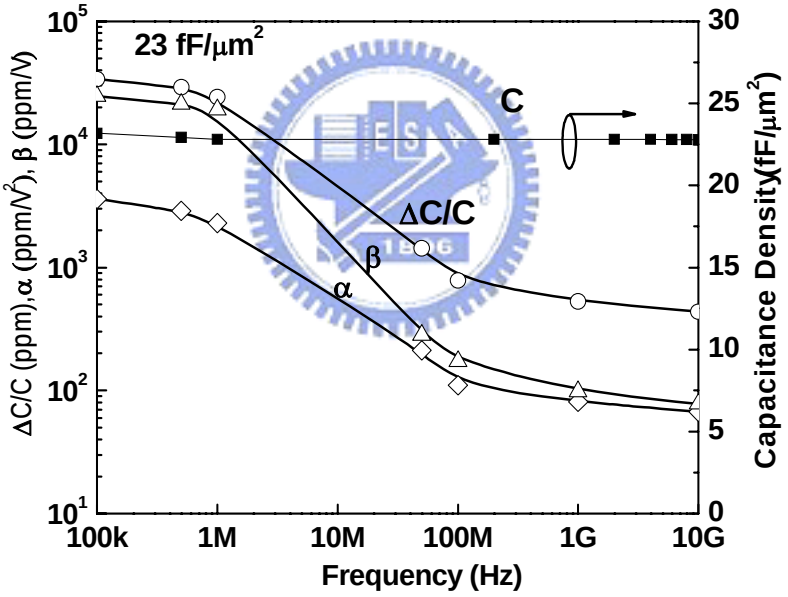


Figure 3-3 The scattering parameters of a TiTaO MIM capacitor, from 200 MHZ to 20 GHz. Insert: the equivalent circuit model used for capacitance extraction.



(a)



(b)

Figure 3-4 (a) The ΔC/C-V characteristics of a TiTaO MIM capacitor. The data for frequencies >1 MHz were obtained from the S-parameters. (b) Frequency dependent capacitance density, ΔC/C, α and β for a TiTaO MIM capacitor biased at 2V.

Chapter 4

Thermal Leakage Improvement by Using a High Work-Function Ni Electrode in High-κ TiHfO MIM Capacitors

4.1 Introduction

MIM capacitor development aims to achieve high capacitance density devices using a simply integration process, to yield multiple functions for System-on-Chip (SoC) applications. To meet these requirements, the using higher κ dielectric is the only choice since the decreasing dielectric thickness (t_κ) increases the unwanted leakage current exponentially. Therefore, the technological trend has been to increase the κ value in the dielectrics, from Al_2O_3, HfO_2-Al_2O_3 [4.1], Nb_2O_5 [4.2], to TiTaO [4.3~4.5] or TiHfO (κ~45-50). Based on this concept, previously we showed high density MIM capacitors by using high κ TiTaO dielectrics, discussed in the above section. Relative low leakage currents were obtained due to the decreased electric field in thick high-κ insulator. However, the unwanted drawback is the smaller bandgaps (E_G) and degraded conduction band offset (ΔE_C) to metal electrode result in a large leakage current at operational temperatures, as shown in Fig.4-1(a); so that the stored charge leaks from the capacitor ($Q=C\cdot V$). This is also a challenge in flash

memory [4.7] and is unavoidable during IC operation, where there is a large device density in the circuit and high DC power dispassion. A possible solution is to add a high E_G dielectric to form a multi-layer [4.8] or laminate structure [4.1], but the overall κ value and voltage coefficient of capacitance (VCC) are then degraded. To overcome this problem, in this paper we report the integrating both high ΔE_C TiHfO dielectric and high work-function (ϕ_m) metal electrode to further reduce the leakage current, without sacrificing the capacitance density. Figure 4-1 (b) shows the possible high ϕ_m metals in the Periodic Table and Ni is the only low cost non-Noble metal with highest ϕ_m of 5.1 eV, if excluding the expensive noble metals of Pd, Os, Ir, Pt and Au. By using high ϕ_m Ni (5.1eV) for high-κ TiHfO capacitors, the leakage current at 125°C is reduced by nearly two orders of magnitude compared with control devices using an Al electrode (ϕ_m = 4.1 eV). Economically it is also better to use Ni, which has been reported and used previously in CMOS [4.9].

4.2 Experimental

The devices were fabricated by first depositing 2 μm SiO_2 on a Si wafer, and then forming the lower capacitor electrode using PVD-deposited TaN/Ta bi-layers. The Ta was used to reduce the series resistance and the TaN served as a barrier layer between the high-κ TiHfO and the Ta electrode. Then the $Ti_xHf_{1-x}O$ (x~0.6) dielectric was deposited by PVD, followed by a 400°C oxidation and annealing step to reduce

the leakage current. Finally, Ni or control Al was deposited and patterned to form the top capacitor electrode. Devices of various sizes were made, those measured were typically 20 μm x 20 μm in area. The fabricated devices were characterized by *C-V* and *J-V* measurements using an HP4155B semiconductor parameter analyzer and an HP4284A precision LCR meter.

4.3 Results and discussion

A. Electrical C-V & J-V characteristics:

Figure 4-2 (a) shows the *C-V* characteristics at various frequencies for [Ni or Al]/ TiHfO /TaN MIM capacitors having ~11 fF/μm^2 capacitance density. The Ni electrode devices show better frequency dispersion and voltage independence (small VCC) than those using Al. This indicates that the magnitude of the barrier height ϕ_m of the upper electrode is important in improving the device performance. In Figure 4-2(b) the *J-V* characteristics of the TiHfO MIM capacitors, measured at 25 ^{o}C and 125^{o}C, show that the advantage of the Ni electrode is preserved at the higher temperature, even though the leakage currents are both increased exponentially.

B. ΔC/C and VCC α

Capacitor voltage linearity is an important parameter for an MIM capacitor in silicon RF and mixed signal IC applications. This voltage dependence can be obtained by fitting the measured *C-V* characteristics using a second order polynomial expression of the form:

$$\Delta C(V)=C_0(\alpha V^2+\beta V) \quad . \tag{1}$$

Here C_0 is the capacitance at 0 V, α and β represent the quadratic and linear voltage coefficients of capacitance, respectively. Since the effect of the linear β term can be compensated by appropriate circuit design (by using a differential method [4.10~4.13], the α term is the main parameter for the voltage dependence. Figure 4-3(a) depicts the variation of $\Delta C(V)/C$ as a function of voltage for the [Ni or Al]/TiHfO/TaN capacitors, at different frequencies. The lines in the figure are fits to the data using the expression above. The Ni top electrode not only reduces the leakage current but also improves the frequency dispersion, $\Delta C/C$, and α. This improvement of the voltage dependence may arise from the higher barrier height ϕ_m between the electrode and the dielectric, which leads to a lower carrier concentration [4.14~4.15]. In general the dispersive behaviors, such as the voltage and frequency dependence, are believed to be related to the existence of bulk-dielectric traps near the dielectric/metal interface. Different traps induce charges with different time constants and strongly modulate the capacitor charges at certain frequencies. Therefore, when the applied frequency is high, VCC is low since the induced charges are unable to follow the AC signal [4.2~4.6].

In addition the stability of the devices after a thermal treatment of 350^{o}C for 1 hr was good, as indicated from the *J-V* and $\Delta C/C$-*V* characteristics shown in Fig. 4-3(b). This suggests that the devices are suitable for the fabrication of MIM structures in back-end-of-the-line (BEOL) processes.

C. Current conduction mechanism

To investigate the large leakage current difference for the [Ni or Al]/TiHfO/TaN MIM capacitors, an understanding of the mechanism of conductivity is necessary. This is also useful in the development of advanced MIM devices. According to space-charge-limited current (SCLC) theory [4.16~4.18], the *J-V* characteristics should initially be ohmic (*J*~*V*) at low applied bias. As the applied voltage is increased, a strong injection of the charge carriers into the bulk of the film occurs, giving $J \sim V^2$. Fig. 4-4 shows the *log(J)* versus *log(E)* dependence. The slopes of the curves, in both the low- and high-field regimes are not in agreement with the ohmic and SCLC mechanisms.

To investigate further we have plotted *ln(J)* versus $E^{1/2}$ for Schottky emission (*SE*) or Frenkel-Poole (*FP*) conduction, as shown in Figs. 4-5(a) and (b) i.e.

$$J \propto \exp\left(\frac{\gamma E^{1/2} - V_b}{kT}\right) \quad , \tag{2}$$

where

$$\gamma = \left(\frac{e^3}{\eta \pi \varepsilon_0 K_\infty}\right)^{1/2} \quad . \tag{3}$$

The constant η is equal to 1 or 4 for the *FP* or *SE* cases. The fits to the experimental data give slopes γ of 1.65×10^{-5} or 3.32×10^{-5} eV $(m/V)^{1/2}$ for the *SE* or *FP* mechanisms respectively, by using a refractive index n =2.45 for $Ti_xHf_{1-x}O$ (x~0.6) [4.19]. This n value is consistent with a linear interpolation of the reported 2.57 value

for TiO_2 and 1.85 for HfO_2 [4.20]. The leakage current at 25°C for the Al electrode on TiHfO/TaN is consistent with an *SE* description at low field and *FP* at high field through a trap-conduction mechanism. However the leakage at 125°C appears to be dominated by the *SE* process, due to the small energy barrier ϕ_b. In contrast the leakage at 125°C for the Ni case is still governed by the *SE* and *FP* at low- and high-field, respectively, which is due to the large ϕ_b, as shown in inserted thermal equilibrium-band diagram.

Since the low-field conduction for both Ni and Al electrodes at 125°C is governed by *SE*, we have plotted the detailed $ln(J/T^2)$-$E^{1/2}$ relation in Fig. 4-6(a), to extract ϕ_b. A Schottky barrier height of 0.3 eV or 1.4 eV for Al/TiHfO or Ni/TiHfO was obtained, where the significantly larger ϕ_b using Ni accounts for the ~two orders of magnitude lower leakage current compared with devices using Al. From the extracted ϕ_b and the reported ϕ_m data, the conduction band of the dielectric with respect to the vacuum level is at 3.8 eV – this gives an E_G for $Ti_xHf_{1-x}O$ of 4.3 eV with x~0.6. Since the conduction mechanism at high electric field for the Ni electrode on TiHfO is governed by a *FP* mechanism, we also plotted the *ln(J/E)-1/KT* relationship in Fig. 4-6(b). The extracted trap energy is 1.2 eV from the conduction band of TiHfO, as shown in the inserted plot. This value is less than the *SE* energy of 1.4 eV, which supports the contention that the high-field conduction should be described as a *FP*

process rather than a *SE* one. This result also explains that the conduction mechanism for the low ϕ_m Al electrode case should be governed by *SE* since its *SE* barrier height is only 0.3 eV whereas the FP case requires 1.2 eV. Thus the use of a high ϕ_m electrode, such as Ni, is vital when using high κ dielectrics which have small E_G values.

D. Performance comparison

Table 4-1 summarizes the important device data for MIM capacitors with various high-κ dielectrics and work-function metals. The thermal leakage decreases with increasing ϕ_m of the metal electrode from Al to Ni. High ~11 fF/μm^2 density, small quadratic VCC α of 361 ppm/V^2 and low 1×10^{-7} A/cm^2 leakage current at 125°C were simultaneously measured in the Ni/TiHfO/TaN devices, which is comparable with or better than other reported data. The VCC α is strongly dependent on the capacitance density and electric field [4.1~4.6], [4.21~4.24]: an exponential decrease of α with increasing capacitance effective thickness (CET), or *1/C,* was observed for all the capacitors, as shown in Fig. 4-7. The VCC α is also dependent on the specific high-κ dielectric, where Ta_2O_5 exhibits superior VCC compared with HfO_2 and Al_2O_3 [4.8]. In addition, the metal-dielectric interface is also important for the VCC α and formation of such an interfacial layer degrades the capacitance performance [4.23]. Overall, MIM capacitors incorporating a higher ϕ_m top electrode and a higher κ

dielectric provide a practical approach to achieve low thermal leakage and good VCC simultaneously, without reducing the capacitance density - as in a multi-layer or laminate structure.

4.4 Conclusion

An unavoidable drawback for higher κ dielectrics in capacitors is the small bandgap and the related reduction in the band-offset, which results in a large leakage current at elevated temperatures. We report improvements in the thermal leakage current by using Ni as a high work function top electrode for high-κ TiHfO capacitors. This avoids sacrificing the overall κ value by using a multi-layer or laminate structure, and results in better voltage linearity, which is important for analog/RF ICs.

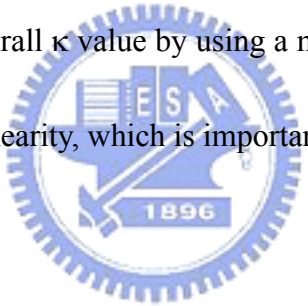
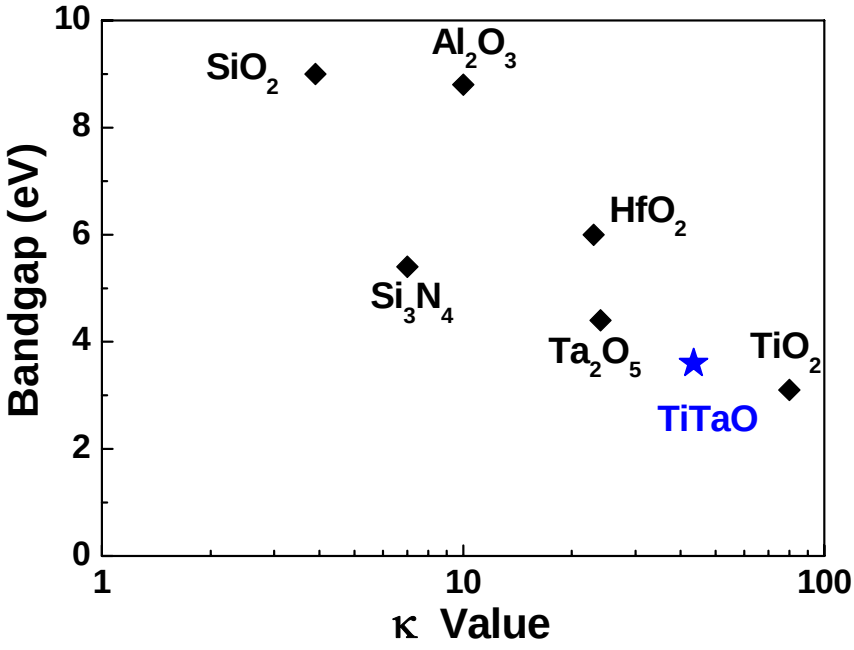
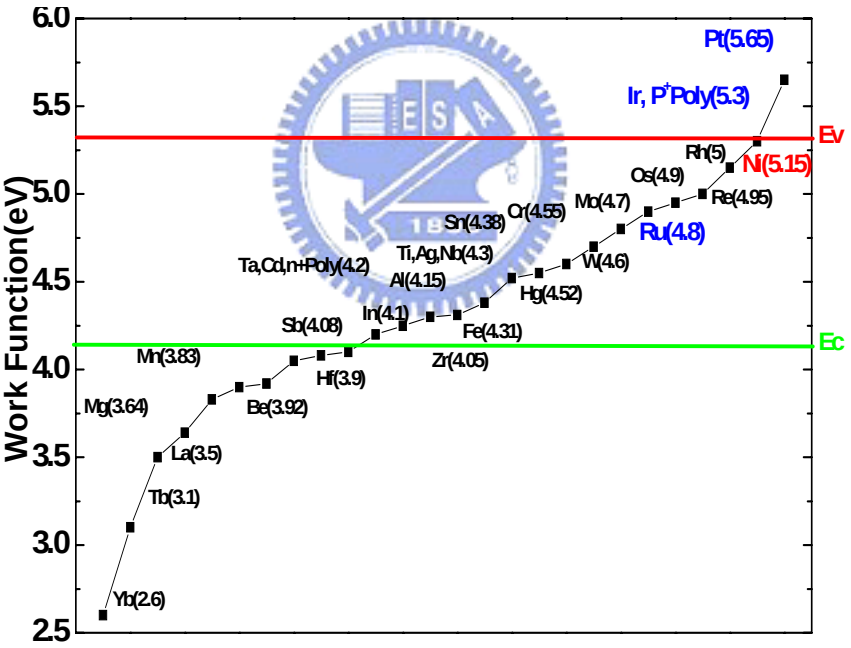


Table 4-1. Comparison of important device data for MIM capacitors with various high-κ dielectrics and work-function metals.

	HfO_2 [4.21]	Tb-HfO_2 [4.22]	Al_2O_3-HfO_2 [4.1]	Nb_2O_5 [4.2]	TiTaO [4.3]		**This work**	
Top metal	Ta	Ta	TaN	Ta	Ir	Ir	Ni	Al
Lower metal	TaN	TaN	TaN	Ta	TaN	TaN	TaN	TaN
C Density ($fF/\mu m^2$)	13	13.3	12.8	17.6	10.3	23	10.8	10.6
J (A/cm^2) @25 °C	6×10^{-7} (2V)	1×10^{-7} (2V)	8×10^{-9} (2V)	7×10^{-7} (1V) 8×10^{-6} (2V)	1×10^{-8} (2V)	2×10^{-6} (1V) 2×10^{-5} (2V)	9×10^{-9} (2V)	2×10^{-7} (2V)
J (A/cm^2) @125 °C	2×10^{-6} (1V)	2×10^{-7} (2V)	6×10^{-9} (1V) 5×10^{-8} (2V)	4×10^{-7} (1V) 1×10^{-5} (2V)	—	—	1×10^{-7} (1V) 9×10^{-6} (2V)	6×10^{-6} (1V) 9×10^{-5} (2V)
α (ppm/V^2)	831	2667	1990	—	89	2289	361	460
κ	~ 15	~ 20	~ 18	~ 30	45	45	~ 45	~ 45
Thickness (nm)	10	14	13	16	41	14	40	40

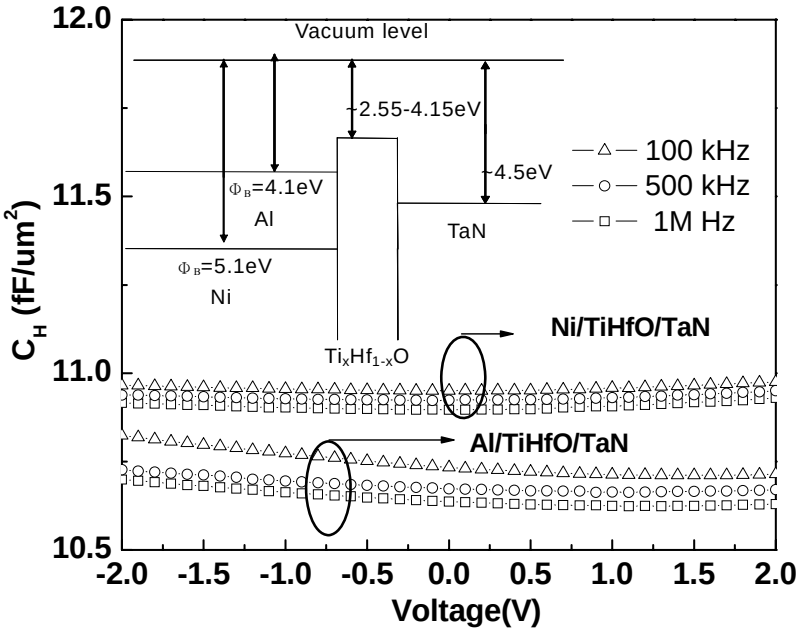


(a)

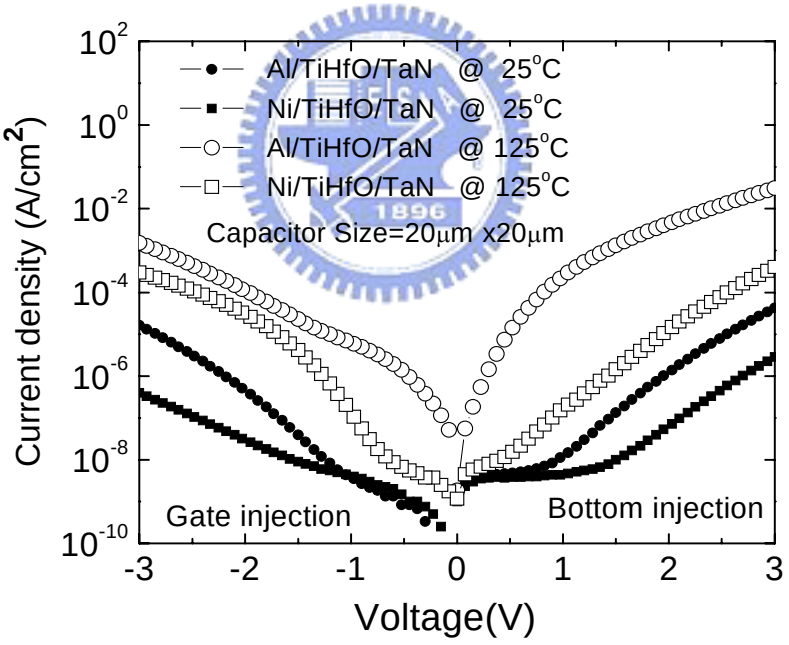


(b)

Figure 4-1(a) Comparison of the band gap and dielectric constant with various high-k dielectrics (b) The possible high work-function metals in the Periodic Table.

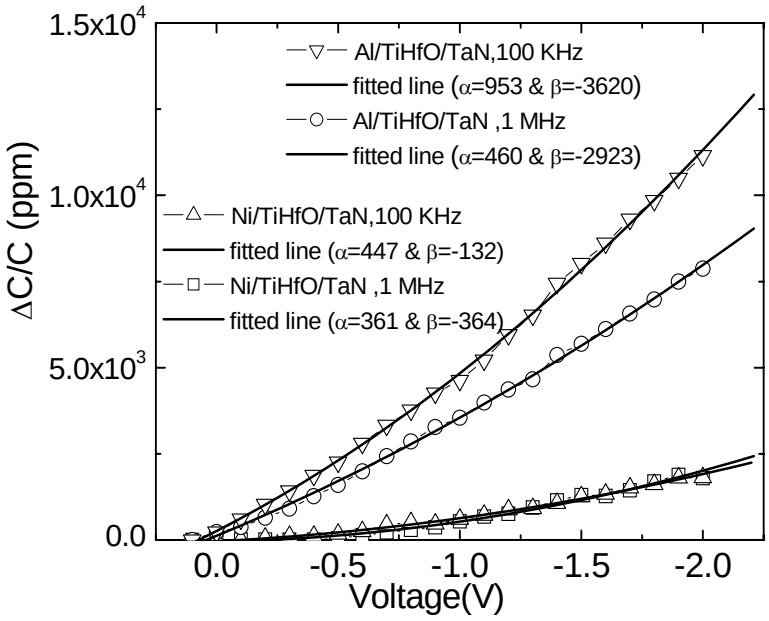


(a)

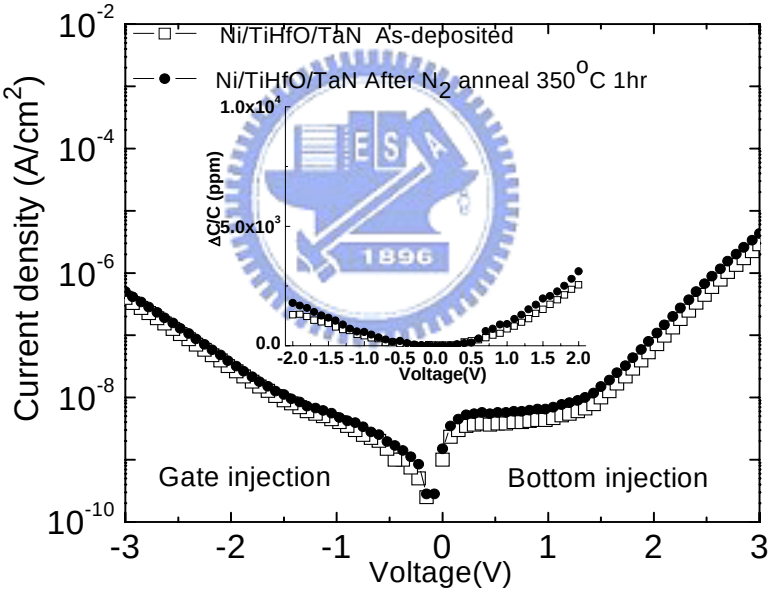


(b)

Figure 4-2 (a) *C-V* characteristics of [Ni or Al]/TiHfO/TaN capacitors, measured at various frequencies (b) *J-V* characteristics of [Ni or Al]/TiHfO/TaN capacitors measured at 25 °C and 125°C.



(a)



(b)

Figure 4-3 (a) *ΔC /C - V* characteristics of [Ni or Al]/TiHfO/TaN capacitors and (b) *J-V* and *ΔC/C-V* (insert) for the Ni-based capacitors.

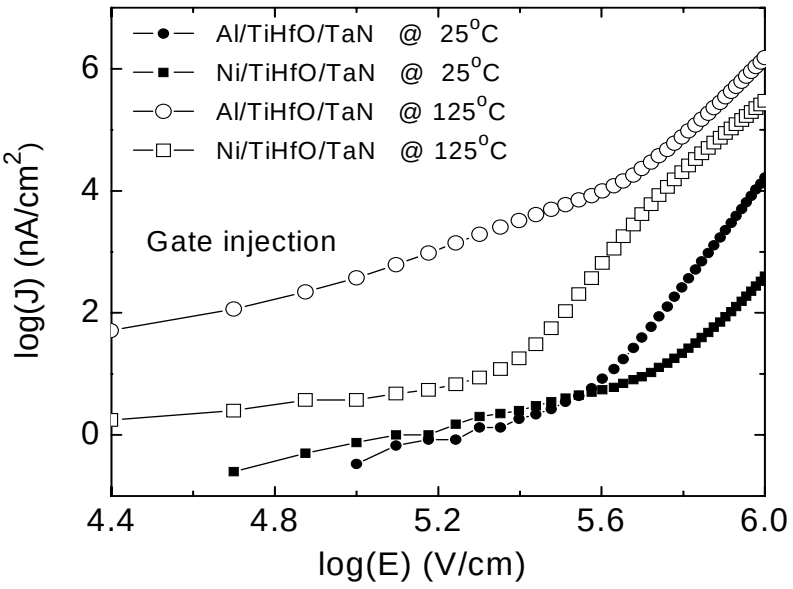
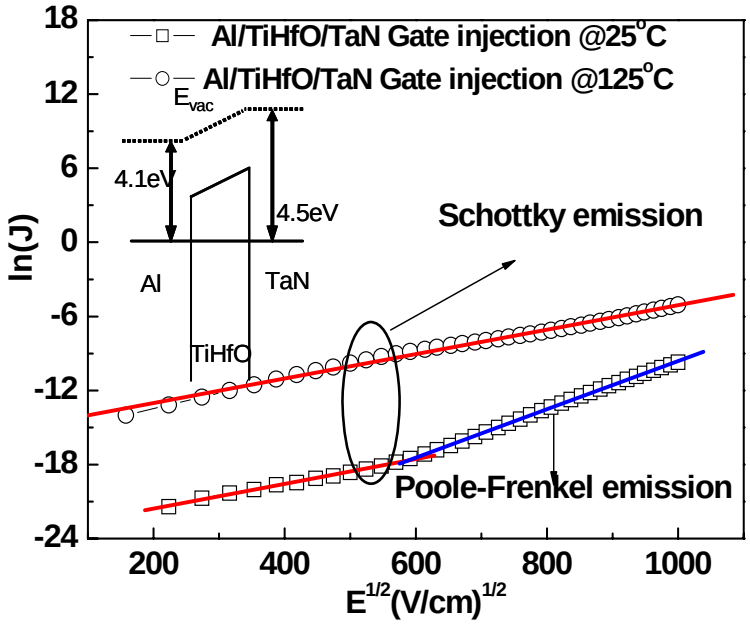
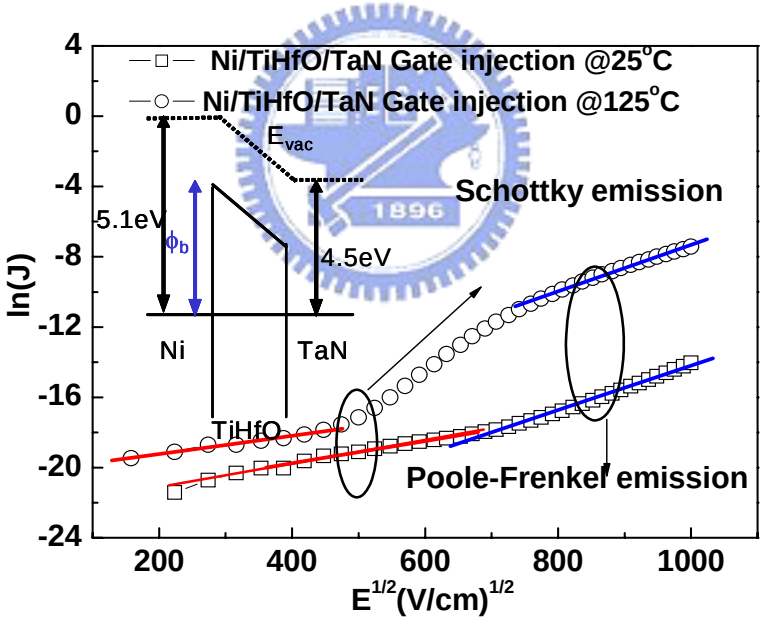


Figure 4-4 *log(J)* versus *log(E)* plots of [Ni or Al]/TiHfO/TaN capacitors measured at 25 °C and 125°C

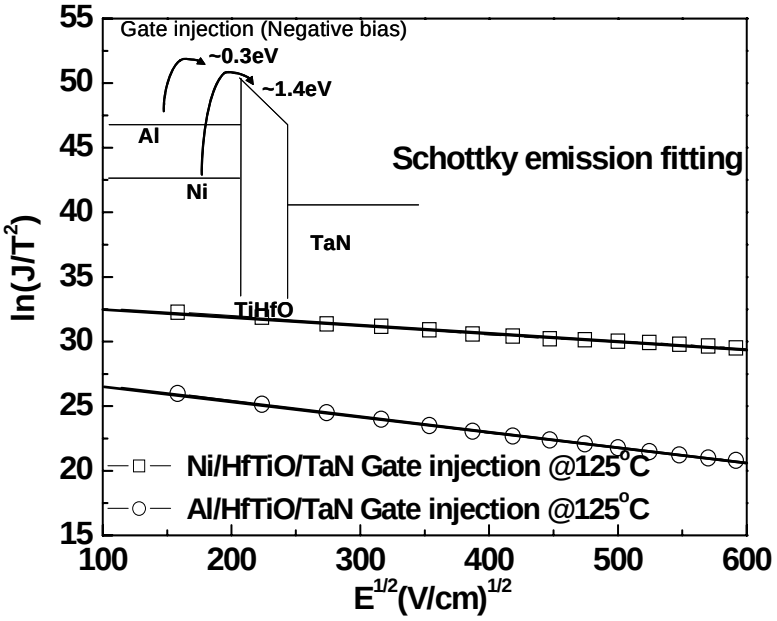


(a)



(b)

Figure 4-5 Measured and simulated J-$E^{1/2}$ of (a) Al/TiHfO/TaN and (b) Ni/TiHfO/TaN devices and inserted band diagrams under thermal equilibrium.



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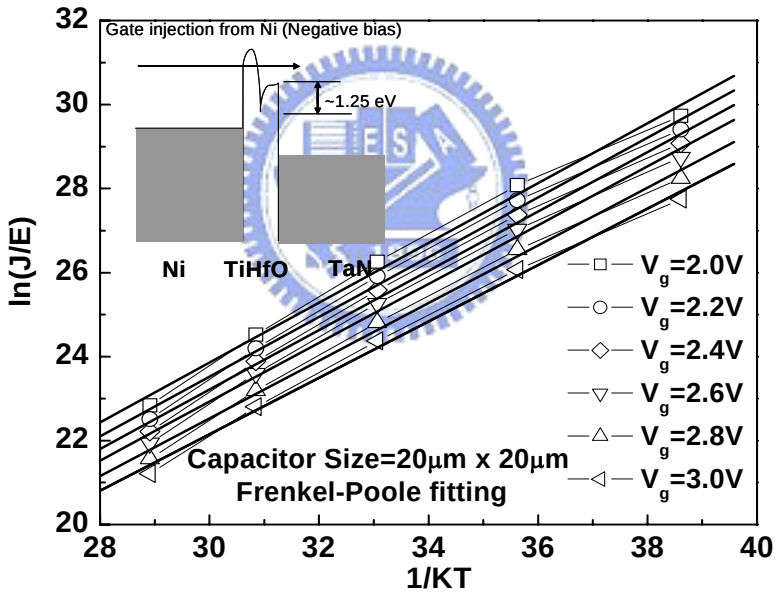


(b)

Figure 4-6 (a) The Schottky Emission (SE) fitting of [Ni or Al]/TiHfO/TaN capacitor data at low electric field, and (b) the FP fits of a Ni/TiHfO/TaN capacitor data at high field. The related band diagrams are included.

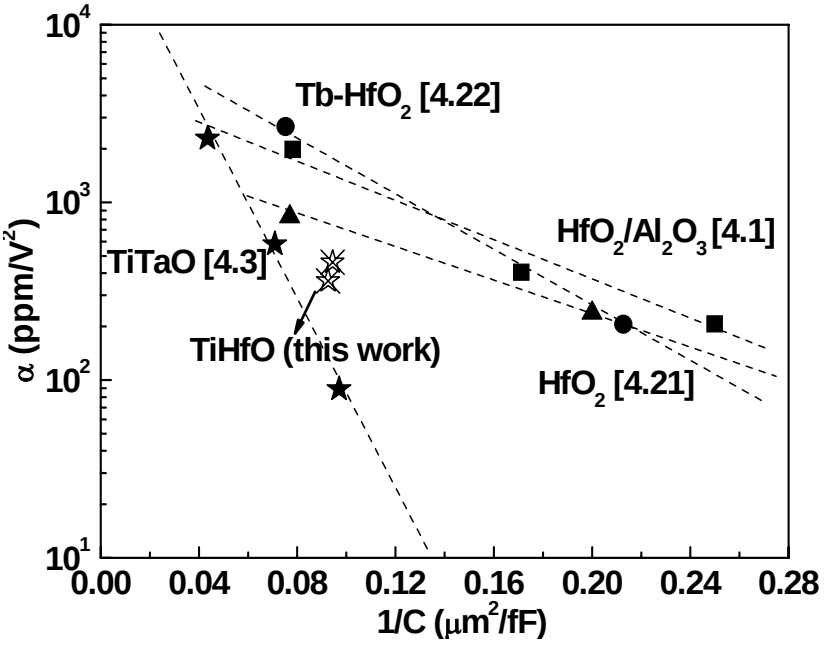


Figure 4-7 *ΔC/C-1/C* plots. An exponential decrease of α with increasing dielectric thickness was observed.

Chapter 5

High Performance $SrTiO_3$ Metal-Insulator-Metal Capacitors for Analog Applications

5.1 Introduction

According to the International Technology Roadmap for Semiconductors (ITRS) [5.1], the capacitance density of future MIM capacitors has to increase to help reduce chip sizes and the cost of integrated circuits (ICs). Besides the high capacitance density ($\varepsilon_0\kappa/t_d$) and the limited thermal budget necessary for back-end integration, a low leakage current and small voltage-dependence of the capacitance ($\Delta C/C$) are also necessary for analog functions. To meet these requirements high dielectric constant (κ) materials [5.2~5.19] provide the only solution, since decreasing the dielectric thickness (t_d) to increase the capacitance density degrades both the leakage current and $\Delta C/C$ performance. Therefore the high-κ dielectrics used in MIM capacitors have evolved from SiON (κ~4-7) [5.3~5.5], Al_2O_3 (κ=10) [5.13], HfO_2 (κ~22) [5.7~5.11], Ta_2O_5 (κ~25) [5.12], [5.15] to Nb_2O_5 (κ~40) [5.16] or TaTiO (κ~45) [5.17~5.19].

$SrTiO_3$ (STO) is a potential candidate to increase the κ value beyond a value of 45, It has the well-known perovskite-type structure and has a para-electric phase above 105K, and high κ value of ~300 at room temperature. This makes it an

attractive candidate for DRAM [5.20~5.24] due to the high charge storage capacity and para-electricity (no fatigue or aging problems). To achieve the high κ value, the STO requires a heat treatment at 450~500^{o}C under an oxygen ambient for crystallization [5.20~5.23]. Therefore, it also requires a Pt or RuO_2 lower electrode [5.21] to withstand the high temperature oxidation, but the high cost and availability of noble metals pose concerns for mass production.

To address this issue we have fabricated STO MIM capacitors on a conventional TaN electrode, where a NH_3 plasma treatment on the lower TaN has been used to improve the electrode stability and capacitance density degradation by forming interfacial TaON during the post-deposition anneal (PDA). We obtained a 28 fF/μm^2 capacitance density, a small quadratic voltage coefficient of capacitance (α) of 92 ppm/V^2 and low 3×10^{-8} A/cm^2 leakage current at 2 V. This performance meets the specifications for analog capacitors as set out by the ITRS for the year 2018.

5.2 Experimental

The MIM capacitors were fabricated on 4 μm SiO_2 which had been deposited on a Si wafer. The lower capacitor electrodes were formed by depositing 0.05 μm TaN on a 1 μm Ta layer, where the thick Ta was chosen to reduce the parasitic resistance of the electrode and the TaN served as a barrier layer for the STO. After patterning the lower electrode, the TaN was treated by NH_3 plasma nitridation at 100 W, to improve

the lower interface. The 43 and 55 nm STO (Sr/Ti = 1.1) dielectric layers were then deposited using RF magnetron sputtering. This was done using a ceramic STO target in a 4:1 Ar/O_2 gas mixture at a total pressure of 10 mTorr. This was followed by 400~450^oC furnace annealing for 30 min to ~1 hour under an oxygen ambient - for crystallization and quality improvement. Finally, TaN/Al was deposited and patterned to form the top capacitor electrode. Cross-sectional Transmission Electron Microscopy (TEM) and Secondary Ion Mass Spectroscopy (SIMS) were used to study the metal interface and dielectric properties. The fabricated MIM capacitors were characterized by current-voltage (*J-V*) and capacitance-voltage (*C-V*) measurements using an HP4156C curve tracer and HP4284A precision LCR meter, respectively.

5.3 Results and discussion

A. Electrical J-V & C-V characteristics:

Figures 5-1 (a) and (b) show the *C-V* and *J-V* characteristics of TaN/STO/TaN capacitors respectively, which were processed differently. The capacitance density increased from 17 to 28 fF/μm^2 with increasing O_2 PDA temperature and the use of the nitrogen plasma (N^+) treatment on the TaN. At the same time better frequency dispersion, lower leakage current and higher breakdown voltage of the MIM devices were obtained. Application of the N^+ treatment on the lower TaN improved the capacitor density from 28 to 35 fF/μm^2, and decreased the leakage current by nearly

an order of magnitude at < 2 V.

Examination of the device performance at 125°C (Figure 5-2(a)) shows that the N^+ treatment still improves the leakage current at positive bias. The leakage current and capacitance density under various process conditions are summarized in Figure 5-2 (b). The higher O_2 PDA temperature and N^+ treatment generally improve the leakage current and capacitance density of the TaN/STO/TaN capacitors.

To address the ITRS requirements for low leakage current for analog capacitors (at year 2018) we also fabricated high performance MIM capacitors of other thicknesses. This was done in an attempt to achieve the ITRS goals of 10 fF/μm^2 density, J/(C•V) < 7 fA/[pF•V] and α < 100 ppm/V^2 [5.1]. Fig. 5-3 shows the *J-V* characteristics of a 28 fF/μm^2 density capacitor (inserted figure) with a 55 nm thickness, fabricated under the optimal conditions of a 450°C PDA and N^+ treated TaN. A low leakage current of 3×10^{-8} A/cm^2 at 2 V was measured, giving a J/(C•V) of 5.4 fA/[pF•V]. This meets the ITRS leakage current requirement at 2018 along with 2.8 times better capacitance density. The leakage current under reverse bias (top electron injection) is markedly higher than that under positive bias (injection from the lower electrode). This may be due to the surface roughness originating from the crystallized STO. However the crystallization is needed for the STO to display a high κ value.

B. Current conduction mechanism

To investigate the large leakage current difference for different voltage polarities, we have plotted *ln(J)* versus $E^{1/2}$ in Figs. 5-4 (a) and (b) for electrons injected from the lower and top electrodes, respectively. A linear *ln(J)*-$E^{1/2}$ relation is shown, although a strong process dependence and a different slope are observed. The different slopes in the *ln(J)*-$E^{1/2}$ plot suggest different current conduction mechanisms. It is known that both Schottky emission (*SE*) or Frenkel-Poole (*FP*) conduction can give such a linear *ln(J)*-$E^{1/2}$ relation with different slopes (γ), as indicated by the following equations [5.22]:

$$J \propto \exp\left(\frac{\gamma E^{1/2} - V_b}{kT}\right) \qquad (1)$$

$$\gamma = \left(\frac{e^3}{\eta \pi \varepsilon_0 K_\infty}\right)^{1/2} . \qquad (2)$$

Here k is Boltzmann's constant, T is the temperature in K, e is the electron charge, ε_0 is the permittivity in vacuum, K_∞ is the high-frequency dielectric constant (= n^2, where n is the refractive index), and η is a constant with its value equal to 1 or 4 for *FP* or *SE*, respectively. The different slopes, γ, for the *SE* and *FP* cases arise from the different energy barriers V_b, corresponding to the work function of the metal-electrode/dielectric in the *SE* case or the trap energy level in the dielectric for the *FP* case. The fits to the experimental data give slopes of 1.58×10^{-5} or 3.16×10^{-5} eV

$(m/V)^{1/2}$ for the *SE* or *FP* mechanisms respectively, by using n =2.4 for STO [5.22], [5.26] in the above equations.

Following the good agreement between the measured data and calculated data (using eqn. (1)) we investigated the dependence of the leakage current on process conditions and voltage polarity. For electrons injected from the top TaN electrode the current conduction mechanism changes from *SE* at low electric fields to *FP* at higher fields. The *FP*-dominated high-field conduction arises because the trapped electrons can gain energy and be emitted from trapped states and contribute to the leakage current. The smaller *SE* current for the device with lower electrode N^+ treatment is related to the smoother STO/TaN surface, as determined by Atomic Force Microscopy (AFM), where the STO rms roughness improved from 11.2 nm to 5.9 nm. For the lower electrode injection case, the current conduction mechanism depends on whether the TaN electrode had the N^+ treatment. For the N^+ treated case, the current conduction mechanism is the same as for top electrode injection, i.e., *SE* at low field which changes to *FP* at high field. However, for the lower TaN electrode without N^+ treatment, the *FP* mechanism applies at both low and high fields. These results indicate a higher trap density or deeper trap energies in STO or the STO/TaN interfacial layer when the lower TaN electrode does not have the N^+ treatment.

C. Material characterization

We measured the SIMS depth profile of the devices to study the origin of the improved leakage current for the N^+-treated case. As shown in Fig. 5-5, even under the existing background level of SIMS system, a higher oxygen concentration can be observed in the lower TaN layer without N^+ treatment. The interfacial TaON was formed during the STO oxidation annealing, but degraded the capacitance effective thickness (CET), capacitance density, and overall κ value. In sharp contrast, the device with N^+ treatment on the lower TaN shows less inter-diffusion and a better interface. In addition, less nitrogen was found in the STO for the treated sample. It is important to note that such an interfacial layer is also responsible to the higher leakage current at low field, as discussed at above, and which may be due to the higher trap density from the oxygen deficiency as shown by SIMS. This would lead to trap-assisted *FP* conduction.

The fabricated STO/TaN was also examined by XRD and TEM. As shown in the XRD spectra of Figure 5-6(a), the crystalline phase of STO is dependent on the PDA temperature and time. The STO crystallization starts after 450^{o}C PDA and the degree of crystallization (XRD intensity) increases with increasing PDA time. Because the κ value of perovskite-type STO is known to increase with increasing degree of crystallization, this result explains the larger capacitance density in Fig. 5-1(a) at the higher PDA temperature. The crystallized STO is confirmed by the cross-sectional

TEM of Fig. 5-6(b) and its enlargement in Fig. 5-6(c). At 43 nm STO thickness, a high κ value of 169 and improved lower STO/TaN interface, compared with previous work [5.17], were found for the 35 fF/μm^2 density device (0.99nm CET). The micro-crystals, consistent with the XRD measurements, had a grain size of 3~10 nm as indicated in the TEM image. Such micro-grained STO is essential in producing thin consistent STO layers for devices [5.25].

D. $\Delta C/C$, α, and TCC

The α is an important parameter of MIM capacitors for analog applications. The undesirable voltage dependence can be obtained by fitting the measured *C-V* characteristics with a second order polynomial equation:

$$\Delta C(V)=C_0(\alpha V^2+\beta V) \quad (3)$$

Here C_0 is the capacitance at 0 V, α and β represent the quadratic and linear voltage coefficients of capacitance, respectively. Since the effect of the linear β term can be compensated by circuit design using a differential method [5.27], the α term is the main factor in the voltage dependence. Figure 5-7(a) and (b) show the $\Delta C/C$-*V* dependence on N^+ treatment and capacitance density, respectively. Good fits to eq. (3) were obtained in all the cases and yielded α. The N^+ treatment can dramatically reduce α from 1978 ppm/V^2 to 542 ppm/V^2, at 1MHz. This significantly better α is consistent with the improved leakage current and interface properties shown above.

An even better α was measured as the STO thickness was increased, although a trade-off of the capacitance density is needed. Under the best conditions - 450°C PDA and N^+ treated lower TaN - a small α of 92 ppm/V^2 was obtained in a 28 fF/μm^2 capacitor. This meets the ITRS specifications for year 2018, with nearly 3 times better capacitance density. The frequency dispersion of the capacitance can have a significant impact in precision analog circuit applications [5.28]. As shown in figure 5-7(c), significantly better frequency dispersion of the capacitance was measured for positive bias than negative bias. This is consistent with lower leakage current in the lower electrode injection case, and may be due to the better STO/TaN interface, as discussed above.

Since modern ICs usually operate at elevated temperature, the temperature-coefficient of the capacitance (TCC) is important. Figure 5-8(a) shows the temperature dependence of the normalized capacitance for STO MIM capacitors with and without the plasma treatment. The TCC increases with increasing temperature but decreases with increasing frequency [5.7]. It is also strongly dependent on processing conditions. As summarized in Fig. 5-8(b), higher PDA temperatures and N^+ treatment improved the TCC characteristics. This is similar to the α improvement, which suggests that the primary mechanism determining the TCC is also trap-related.

E. Performance comparison

Figure 5-9 shows the dependence of α as a function of CET or the inverse capacitance density (*1/C*). An exponential decrease of α with increasing CET or *1/C* was observed for the Ta_2O_5 [5.12], HfO_2 [5.10], Tb-doped HfO_2 [5.8], TiTaO [5.18] and STO MIM capacitors. This is due to the trap-related leakage current which also has an exponential dependence on CET [5.7]. For the same CET or capacitance density value, the STO device has the lowest α. This is due to the high κ value of 147~169 which exceeds the κ~22-45 values for HfO_2, Ta_2O_5 and TiTaO. The *α–1/C* dependence is important to choosing the required C density and also meeting the analog specifications of a low α.

The important device parameters for the analog capacitors are summarized in Table 5-1. Among the various high-κ capacitors, the TaN/STO/TaN capacitor shows the best performance meeting the ITRS roadmap requirements for 2018 and with 2.8 times better capacitance density.

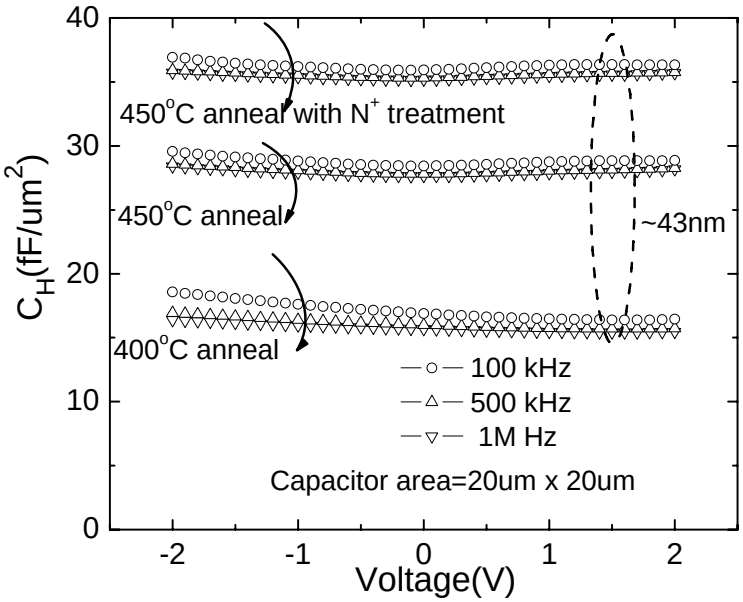
5.4 Conclusion

We have developed TaN/$SrTiO_3$/TaN capacitors with a capacitance density of 28-35 fF/μm^2 by using a high-κ (κ=147~169) $SrTiO_3$ dielectric containing nm-sized micro-crystals (3~10 nm). A small capacitance effective thickness (CET) was achieved by reducing the interfacial TaON using an N^+ treatment on the lower TaN

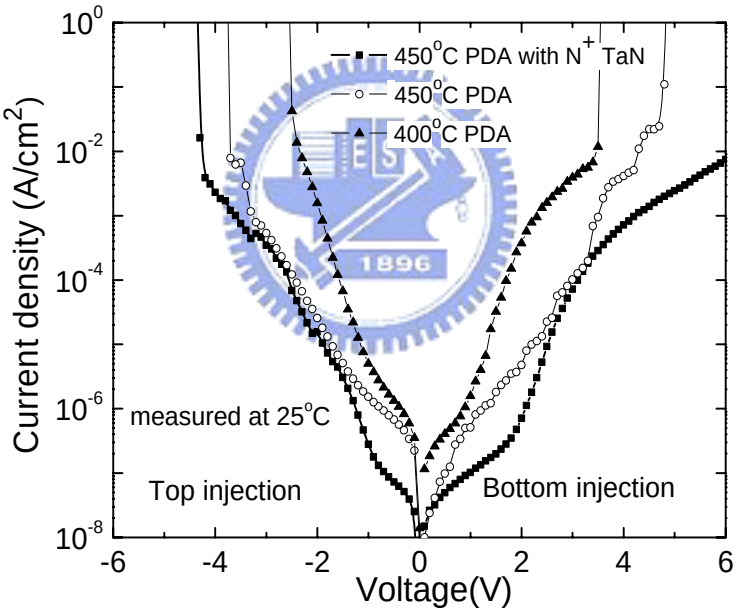
electrode during post-deposition annealing. The small (92 ppm/V^2) voltage coefficient of the capacitance and 3×10^{-8} A/cm^2 leakage current at 2 V exceed the ITRS requirements for analog capacitors at year 2018.

Table 5-1. Comparison of various high-κ capacitors. The TaN/STO/TaN capacitor shows the best performance, exceeding the requirements of the ITRS roadmap for 2018.

	ITRS @ 2018	Ta_2O_5 [5.12]	Tb-HfO_2 [5.8]	HfO_2 [5.10]	TiTaO [5.17]	**This work**
C Density ($fF/\mu m^2$)	10	9.2	13.3	12.8	10.3	28
J (A/cm^2)	-	2×10^{-8} (1.5V)	1×10^{-7} (2V)	8×10^{-9} (2V)	1.2×10^{-8} (2V)	3×10^{-8} (2V)
J/(C•V) (fA/[pF•V])	<7	14.5 @1.5V	38 @2V	2.9 @2V	5.8 @2V	5.4 @2V
α (ppm/V^2)	α<100	3580	2667	1990	89	92

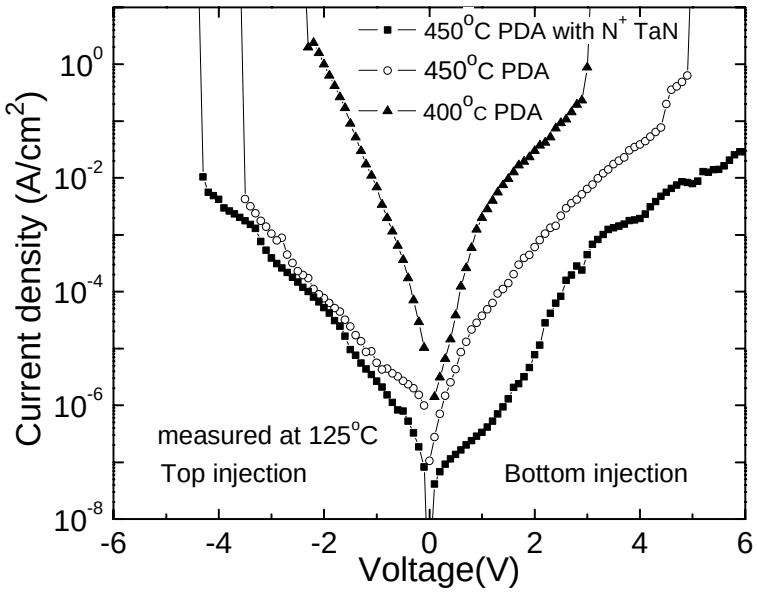


(a)

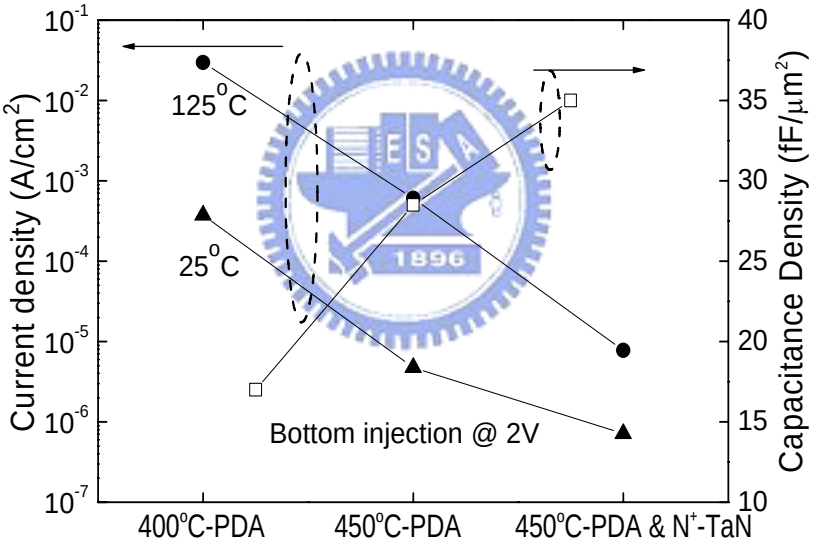


(b)

Figure 5-1 (a) *C-V* and (b) *J-V* characteristics of TaN/STO/TaN MIM capacitors processed under various conditions. The 400ºC PDA yields a capacitance density of 17 fF/μm^2 which increases to 28 fF/μm^2 for a 450ºC PDA and is better with the N$^+$ treatment (35 fF/μm^2).



(a)



(b)

Figure 5-2 (a) *J-V* characteristics for the devices in Fig. 1 measured at 125ºC. (b) Comparison of the *C-V* and *J-V* characteristics of TaN/STO/TaN MIM capacitors.

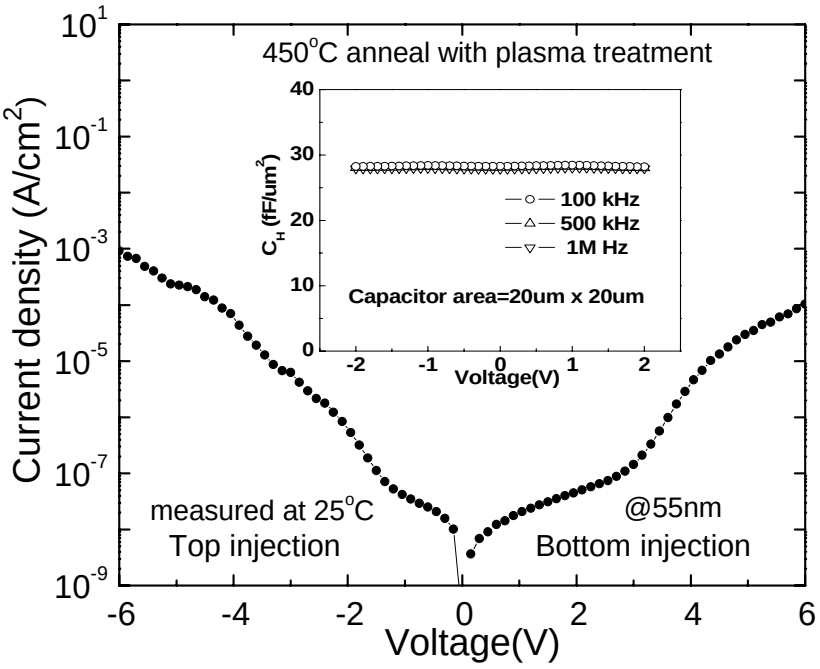
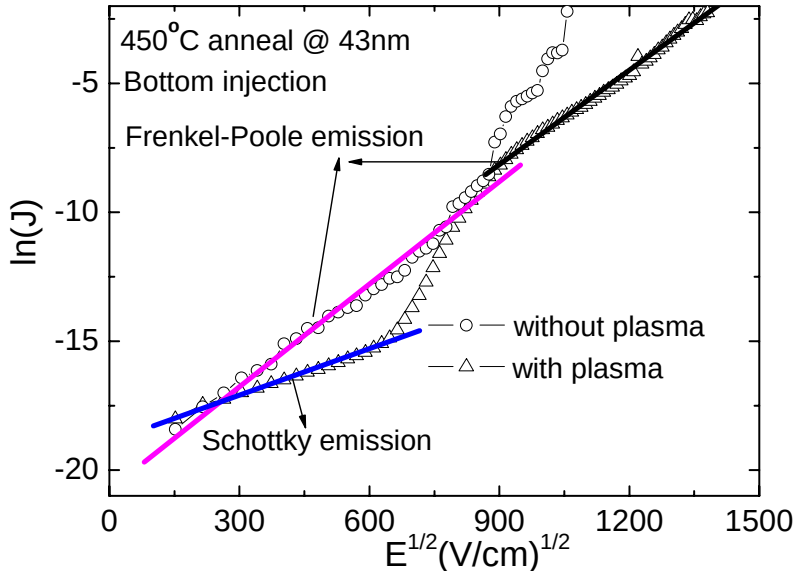
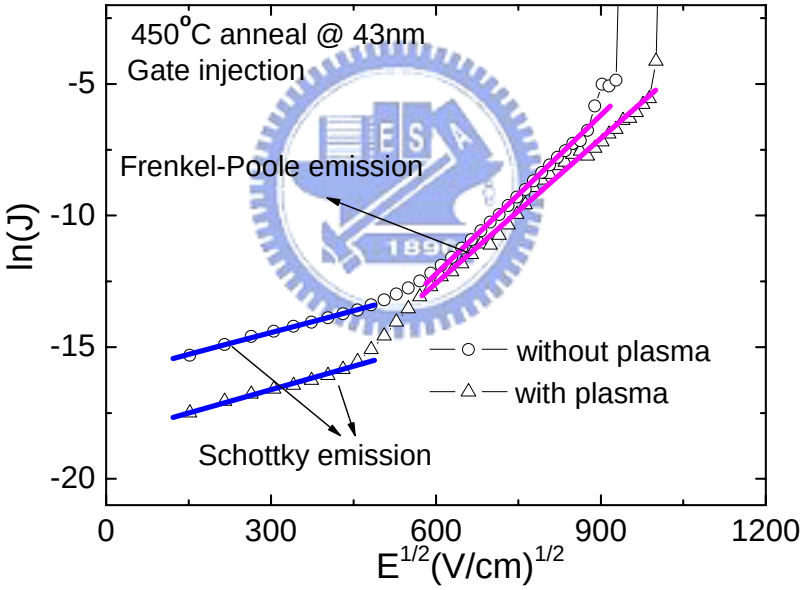


Figure 5-3 *J-V* and *C-V* (insert) characteristics of an STO MIM capacitor using the optimum process conditions.



(a)



(b)

Figure 5-4 Plot of *ln(J)* versus $E^{1/2}$ under electron injection from (a) the lower and (b) the top electrode.

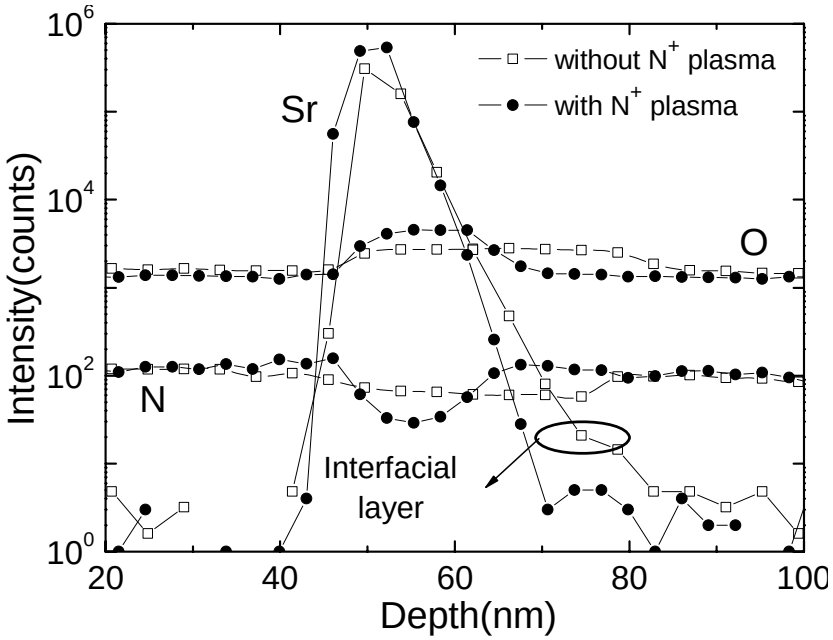
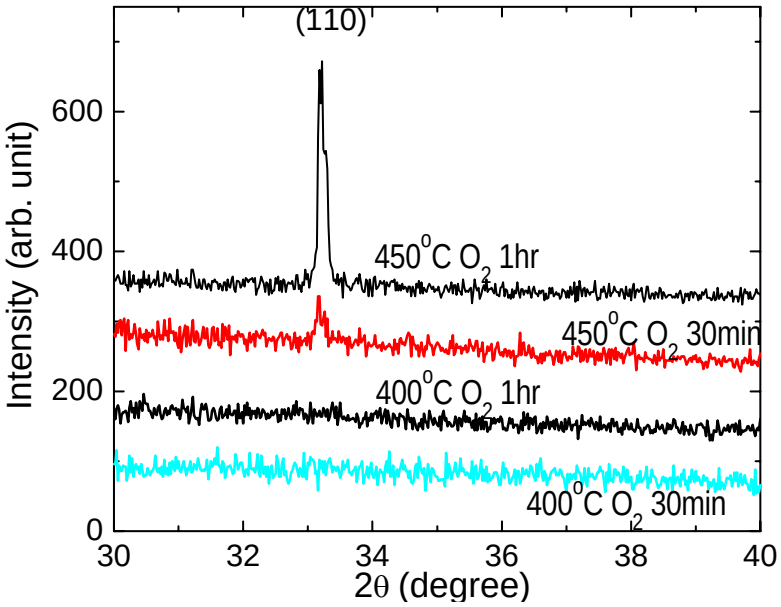
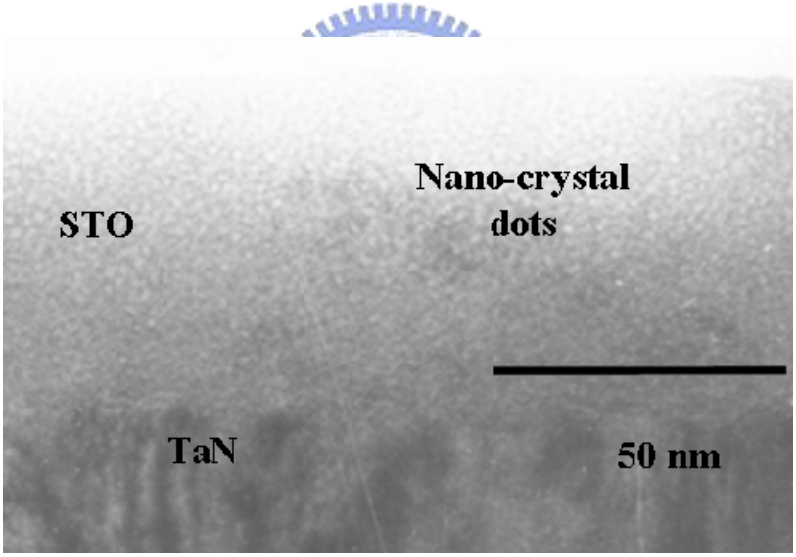


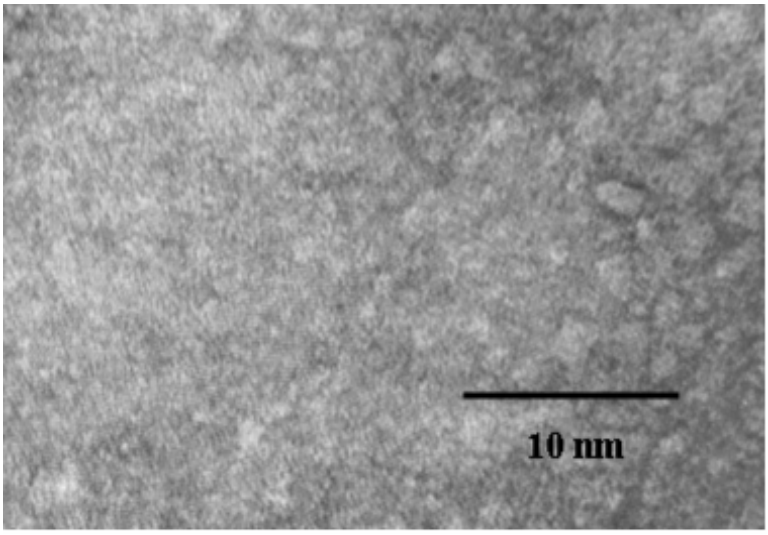
Figure 5-5 SIMS profile of STO/TaN with or without N^+ treatment on the lower TaN.


(110)
600
400
200
0
Intensity (arb. unit)
450°C O2 1hr
450°C O2 30min
400°C O2 1hr
400°C O2 30min
30
32
34
36
38
40
2θ (degree)

(a)

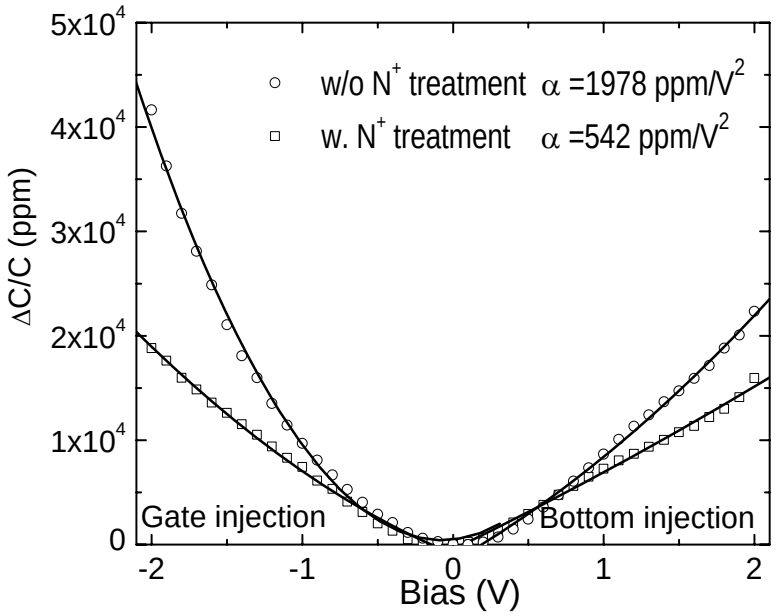

STO
Nano-crystal
dots
TaN
50 nm

(b)

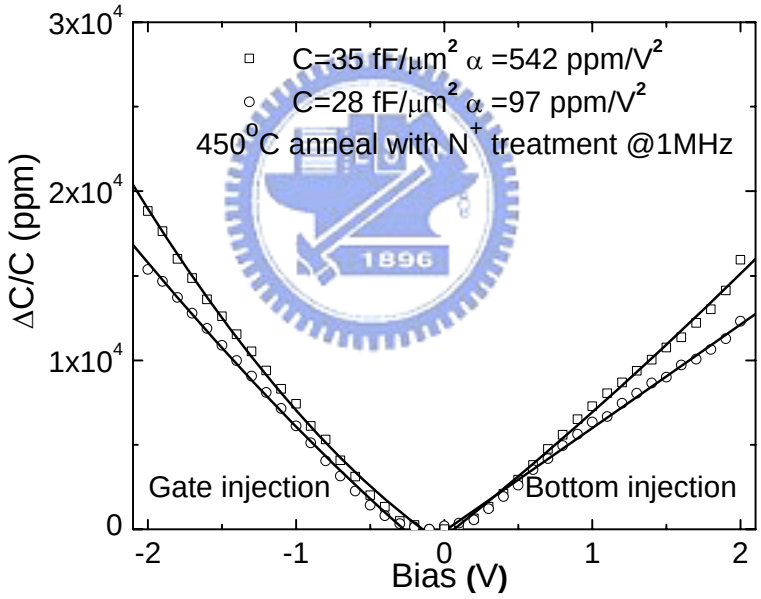


(c)

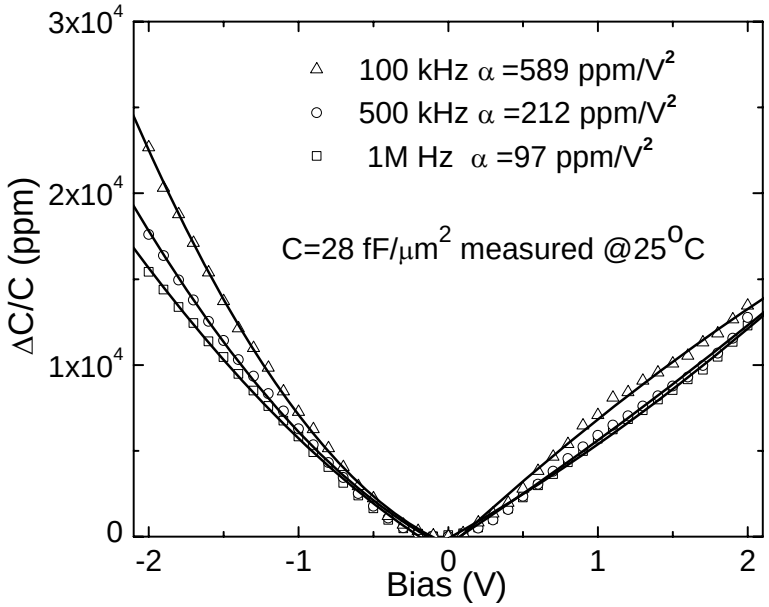
Figure 5-6 (a) The XRD spectra of STO after a 400-450^{o}C O_2 PDA. Crystallization of STO was found at 450^{o}C O_2 PDA. (b) Cross-sectional TEM of STO/N^{+}-treated-TaN with an enlarged STO image in (c).


5x10^4
4x10^4
3x10^4
2x10^4
1x10^4
0
ΔC/C (ppm)
w/o N+ treatment α =1978 ppm/V2
w. N+ treatment α =542 ppm/V2
Gate injection
Bottom injection
-2
-1
0
1
2
Bias (V)

(a)

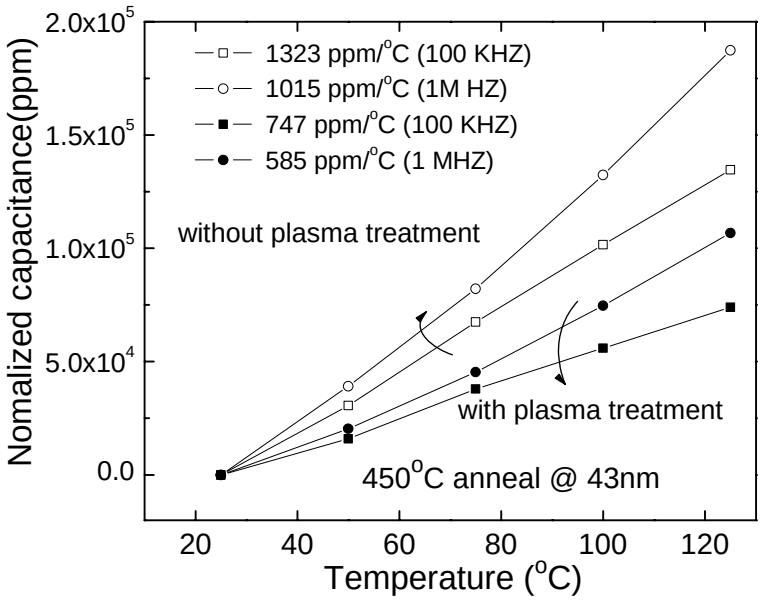

3x10^4
2x10^4
1x10^4
0
ΔC/C (ppm)
C=35 fF/μm2 α =542 ppm/V2
C=28 fF/μm2 α =97 ppm/V2
450oC anneal with N+ treatment @1MHz
Gate injection
Bottom injection
-2
-1
0
1
2
Bias (V)

(b)

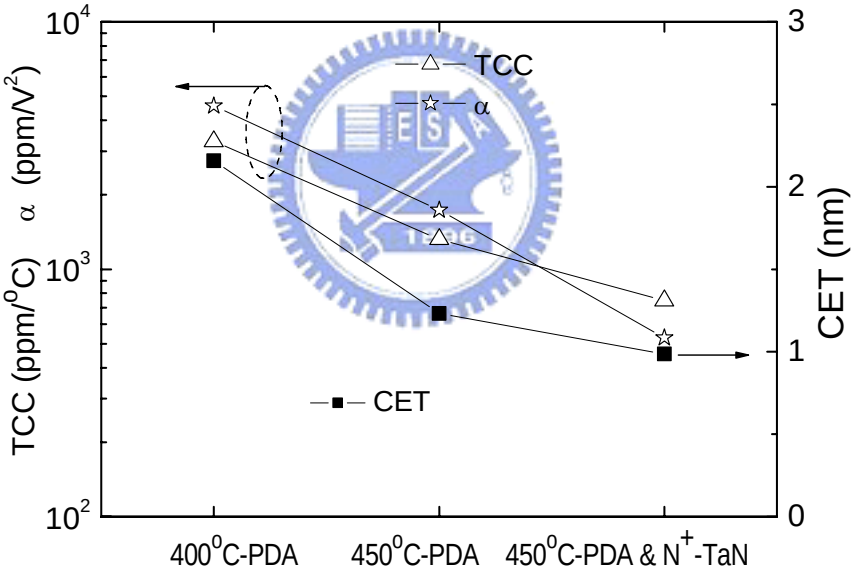


(c)

Figure 5-7 *ΔC/C-V* characteristics for STO MIM capacitors and the dependence on (a) plasma-nitridation on the lower TaN and (b) different capacitance densities of 28 to 49 fF/μm^2(c) Frequency dispersion of the 28 fF/μm^2 density capacitor.



(a)



(b)

Figure 5-8 (a) Temperature-dependent normalized capacitance for MIM capacitors with or without plasma-nitridation of the lower TaN. (b) The α, TCC and CET as a function of various treated MIM capacitors.

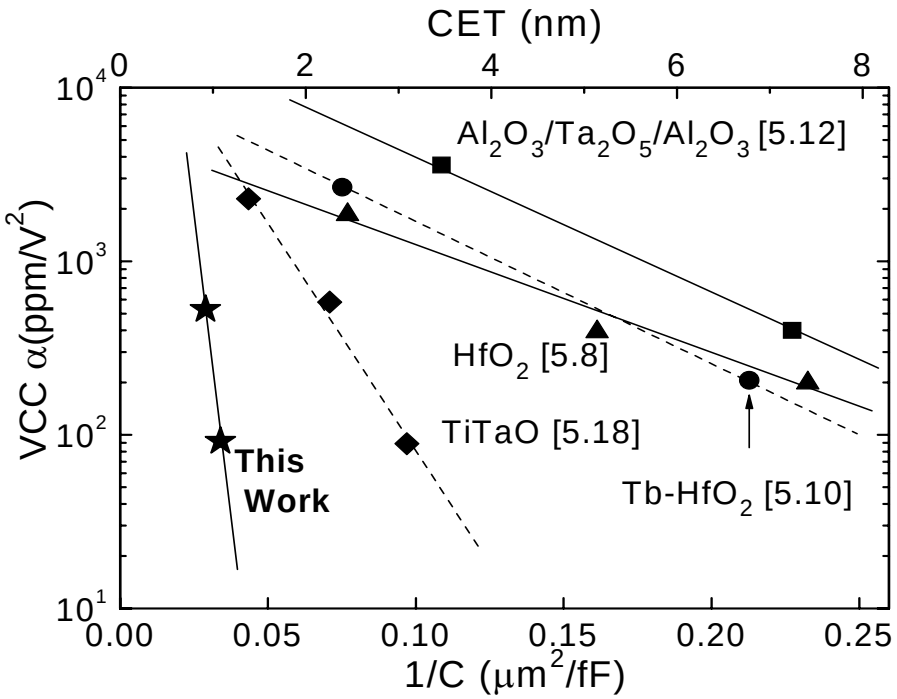


Figure 5-9 *ΔC/C-1/C* plot of TaN/STO/TaN and various high-κ MIM capacitors. The exponential decrease with increasing 1/C is important for designing capacitors for different applications.

Chapter 6

Very High Density (44 fF/μm^2) $SrTiO_3$ MIM Capacitors for RF Applications

6.1 Introduction

Based on the International Technology Roadmap for Semiconductors (ITRS), continuous down-scaling the device size of RF capacitor is needed to reduce the die size and lower the cost. To meet this requirement, higher capacitance density ($\varepsilon_0\kappa/t_d$) is required and the using higher dielectric constant (κ) material is the only choice [6.1~6.16]. This is because the decreasing dielectric thickness (t_d) results in the degraded device performance of higher leakage current and poorer voltage-dependence of capacitance ($\Delta C/C$). Since the high κ Strontium Titanate ($SrTiO_3$) [6.20~6.22] dielectric has a very high κ value (reachable to 300) beyond HfO_2 (κ~22-24), Nb_2O_5 (κ~40) [6.11], TaTiO (κ~45) [6.15~6.16] or HfTiO, it is important to study the possibility for RF application. In addition, the $SrTiO_3$ (STO) is also listed in the DRAM manufacture roadmap [6.17], and therefore the STO capacitor may be used for Analog, RF and DRAM simultaneously to realized low process cost and multi-functional system-on-chip (SoC). In this paper, we have

studied STO MIM capacitor for RF application. Very high capacitance density of 44 fF/μm^2,high κ value of 147 and small ΔC/C of 752 ppm at 2 GHz are obtained at the same time that demonstrates the excellent device performance for RF application.

6.2 Experimental

After depositing 2 μm SiO_2 on Si wafer, the lower capacitor electrode was formed using PVD-deposited TaN/Ta bi-layers. After patterning the bottom electrode, the TaN was treated by NH_3 plasma nitridation. Largely improved interfacial TaON formation, oxygen deficiency and capacitance density degradation are achieved after post-deposition anneal (PDA) [6.18]. Then the 26 and 30 nm thick STO were deposited on the TaN/Ta electrode by PVD, followed by 450^{o}C post-deposition anneal (PDA) for 1 hour under oxygen environment. Finally, the TaN/Al was deposited and patterned to form the top capacitor electrode. The fabricated RF MIM capacitors were characterized using an HP4284A precision LCR meter to 1 MHz, and an HP8510C network analyzer for the S-parameter measurements to 10 GHz [6.8~6.9]. The series parasitic impedance and parallel RF pads were de-embedded from a 'though' and 'open' transmission lines [6.15], [6.23], respectively. The capacitance at RF frequency was extracted from the measured S-parameters using an equivalent circuit model [6.8~6.9], [6.15~6.16].

6.3 Results and discussion

Figures 6-1(a) and 6-1 (b) show the *C-V* and *J-V* characteristics of STO MIM capacitors, respectively. Very high capacitance density of 44 and 49 fF/μm^2 or capacitance-equivalent thickness (CET) of 0.78 and 0.70 nm were measured with low leakage of 5×10^{-7} and 6×10^{-6} A/cm^2, respectively. Such small CET is even useful for ITRS 45nm node DRAM at year 2010. The leakage current under positive bias (electron injected from bottom TaN) is slightly lower than that under reverse bias (electron injected from top TaN). It may be due to the rough top STO surface from STO crystallization that creates localized higher electric field in top TaN/STO. The surface roughness between dielectric and electrode is usually responsible for asymmetric performance of MIM capacitors [6.19]. In addition, it is important to notice that the leakage current of 5×10^{-7} A/cm^2 is low enough for RF IC application due to the very high capacitance density of 44 fF/μm^2: for a typically large 1 pF capacitor used in RF IC, the leakage current is as low as 0.1 pA at 1 V and significantly lower than the leakage current of sub-100nm transistors [6.23]. Furthermore, a near constant capacitance value with little voltage and frequency dependence is obtained for the STO MIM capacitor, which is important for RF IC under large voltage swing condition.

To study the current conduction mechanism of TaN/STO/TaN MIM capacitors,

we have plotted *ln(J)* versus $E^{1/2}$ in Fig. 6-2. Here both Schottky emission (*SE*) or Frenkel-Poole (*FP*) conduction can give a linear *ln(J)*-$E^{1/2}$ relation with different slopes (γ), as shown by the following equations:

$$J \propto \exp\left(\frac{\gamma E^{1/2} - V_b}{kT}\right) \tag{1}$$

$$\gamma = \left(\frac{e^3}{\eta \pi \varepsilon_0 K_\infty}\right)^{1/2} \quad . \tag{2}$$

The K_∞ is the high-frequency dielectric constant (= n^2; n is the refractive index and equals to 2.4 for STO [6.21~6.22]), and η is a constant with value of 1 or 4 for *FP* or *SE*, respectively. From the good matching between measured and eq. (1) calculated data, the current conduction mechanism changes from *SE* at low electric fields to *FP* at higher fields.

In order to investigate the device RF characteristics of STO MIM capacitors, the S-parameters were measured. Fig. 6-3 (a) shows the measured S-parameters for TaN/STO/TaN capacitors, and the capacitance value is extracted by using the equivalent circuit model shown in Fig. 6-3(b). The MIM capacitor is modeled by R_p and C, where the R_p originates from the high-κ dielectric loss. In addition, the R_s, L_{s1}, and L_{s2} represent the parasitic impedances in the coplanar transmission line used for RF measurements. Good matching between measured and modeled S-parameters are shown in Fig. 6-3(a), indicating the good accuracy for capacitance extraction at RF

regime beyond the limited 1 MHz of LCR meter.

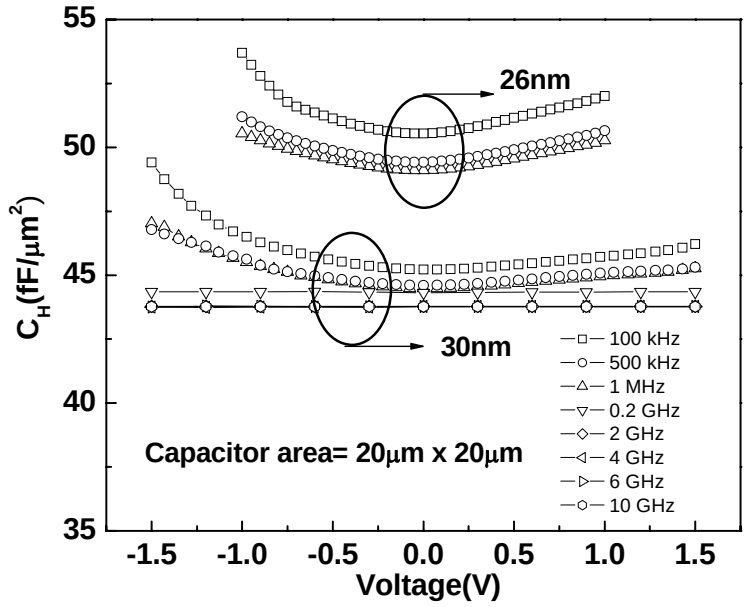
The obtained capacitance density is plotted in Fig. 6-4(a). Small capacitance reduction of only 3.5% to 10 GHz is indicative of the good device performance over the whole intermediate frequency (IF) to RF range [6.6~6.7]. However, such extracted capacitance density at RF regime is not sensitive enough to calculate the small *ΔC/C* variation- important for precision capacitors operated under large signal swing. We have used the previous circuit-theory-derived equation [6.8] to calculate the *ΔC/C-V* from measured S-parameters and the results are shown in Fig. 6-4(b). The measured *ΔC/C-V* can be fitted with a second order polynomial equation, where linear (β) and quadratic (α) voltage coefficients of ΔC/C were obtained. Since the β effect can be canceled by circuit design using differential method, α is the key parameter to cause the unwanted voltage-dependent *ΔC/C*. The obtained *ΔC/C* and α are also plotted in Fig. 6-4(a). Fortunately, both α and *ΔC/C* decrease with increasing frequency into RF region, which is attributed to the trapped carriers being unable to follow the high frequency signal with typical carrier lifetimes in the range ms to μs [6.8~6.9], [6.15~6.16]. Therefore, high capacitance density of 44 fF/μm^2, small ΔC/C of 752 ppm, and low α of 54 ppm/V^2 at 2 GHz are important for high-speed RF IC applications.

The device quality (Q) factor and corresponding capacitance extracted from

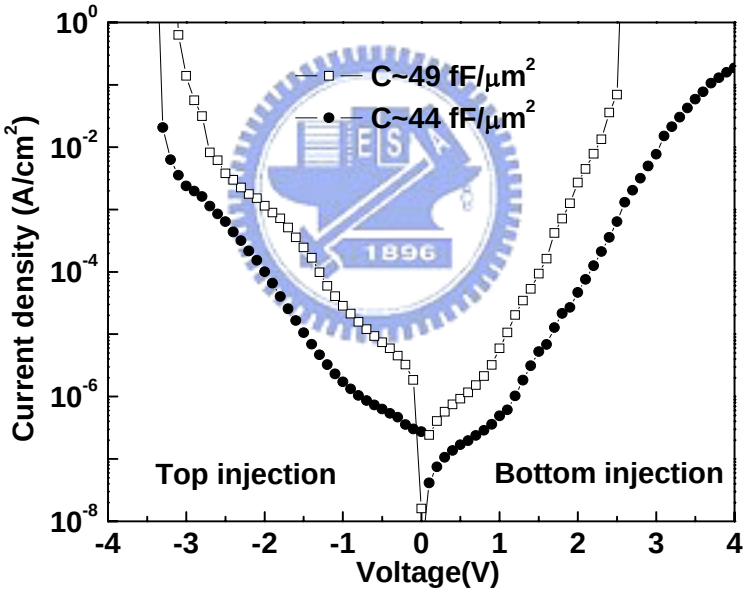
circuit model [6.6] using the S-parameters at RF frequencies is shown in Fig. 6-5(a). It should be noted that a good Q-factor >50 is obtained for RF application before resonant frequency (f_r) of ~13 GHz, where the relative low f_r is due to the large capacitance. Furthermore, since the advanced ICs are usually operated at higher temperature due to power dissipation, the temperature-coefficient on capacitance (TCC) is another important factor. Figure 6-5(b) shows the TCC obtained from normalized capacitance of STO capacitor as a function of temperatures. Again, the TCC decreases with increasing frequency with TCC values close to previous TiTaO devices [6.15].

6.4 Conclusion

Very high 44 fF/μm^2 capacitance density, small capacitance reduction of 3.5% to 10 GHz and a small α of 54 ppm/V^2 at 2 GHz were simultaneously achieved in TaN/STO/TaN capacitors processed at 450^{o}C and important for RF application. This high density MIM capacitor is important for largely down-scaling the capacitance size and integration with DRAM.



(a)



(b)

Figure 6-1 (a) *C-V* and (b) *J-V* characteristics of STO MIM capacitors. The *C-V* results from 100 kHz to 1 MHz are measured from LCR meter and the data from 0.2 GHz to 10 GHz are obtained from the S-parameters. High capacitance density of 44 and 49 fF/μm^2 were measured with low leakage density of 5×10^{-7} and 6×10^{-6} A/cm^2.

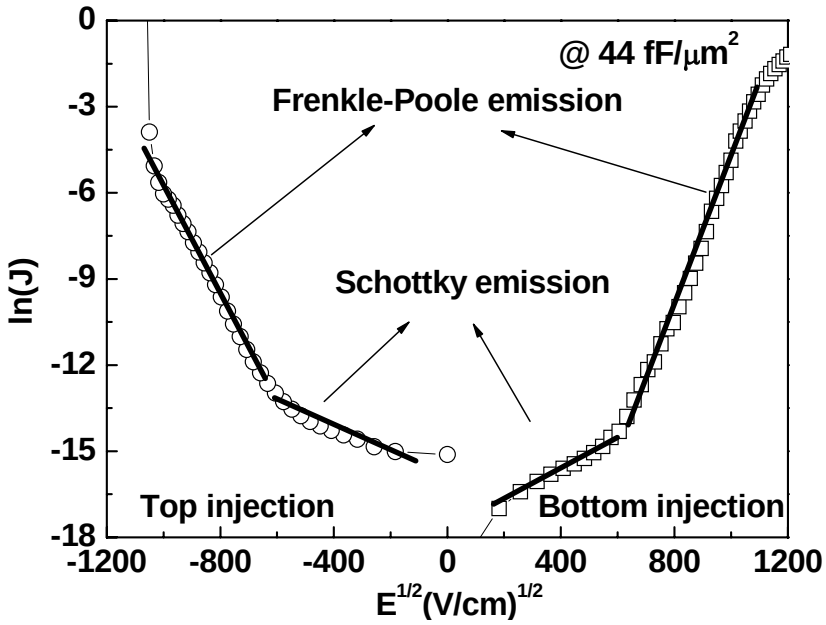
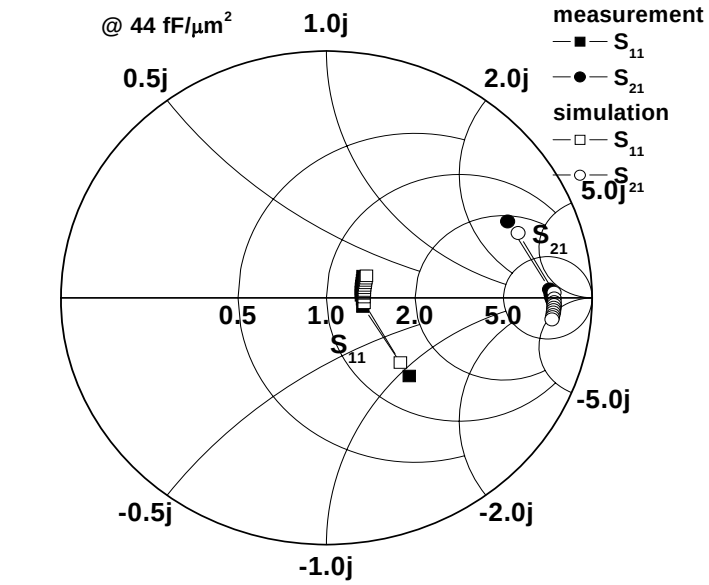
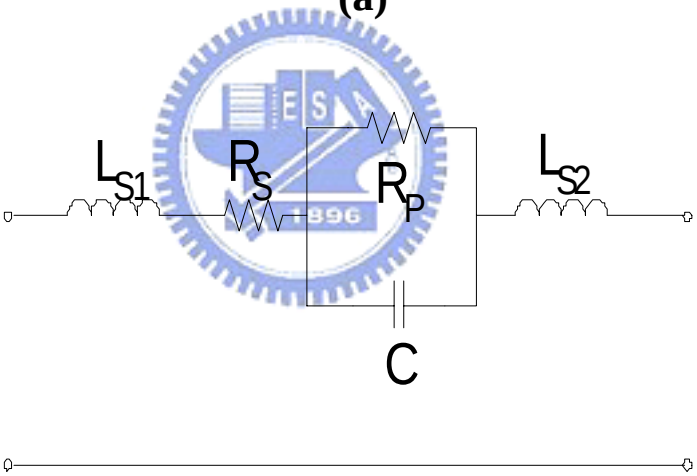


Figure 6-2 Measured and simulated J-$E^{1/2}$ of STO MIM capacitors.

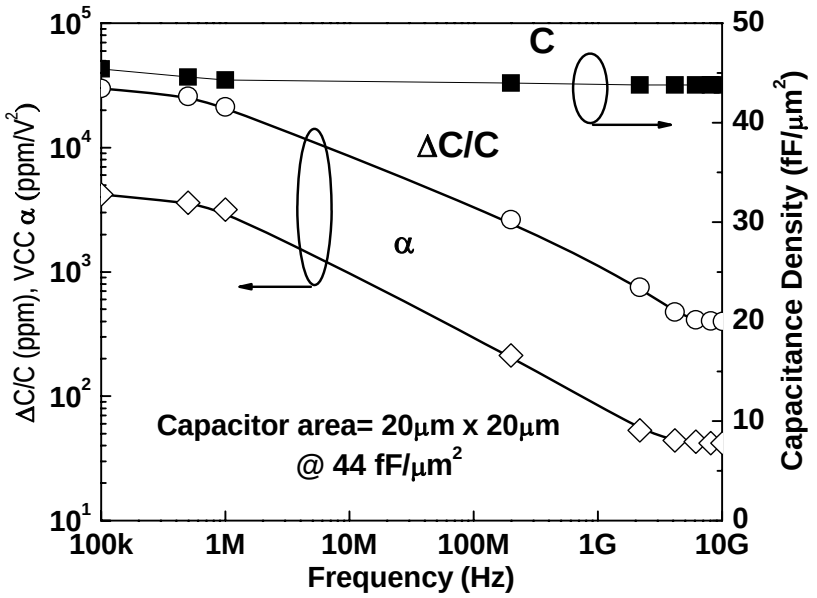


(a)



(b)

Figure 6-3 (a) Measured and simulated two-port S-parameters for STO MIM capacitors, from 500 MHZ to 10 GHz and (b) equivalent circuit model for capacitor simulation in RF regime.



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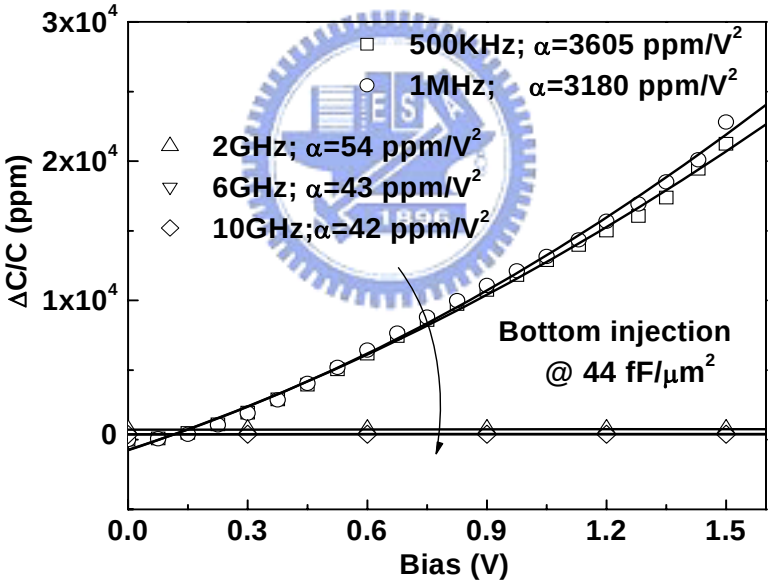
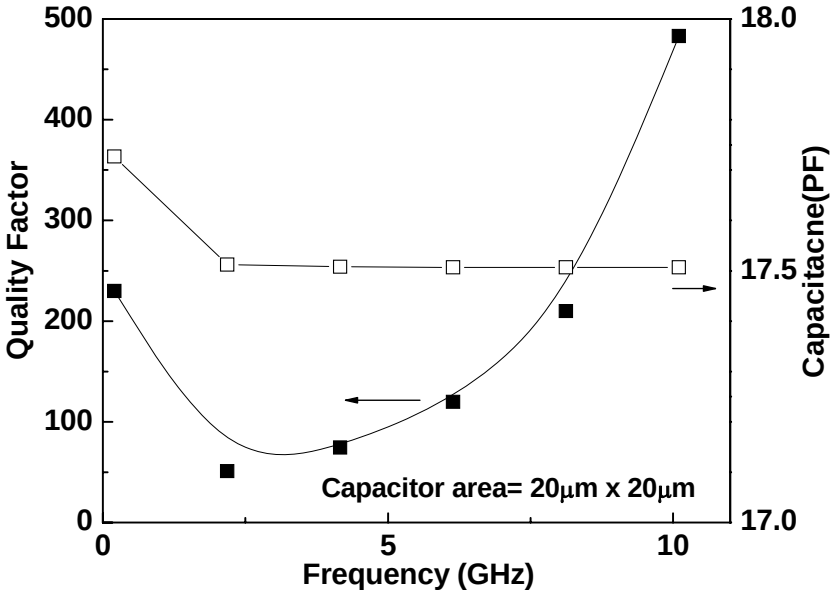


(b)

Figure 6-4 (a) Frequency dependent capacitance density, ΔC/C and α for a STO MIM capacitor biased at 1.5V. The data for frequencies >1 MHz were obtained from the S-parameters. (b) The *ΔC/C-V* characteristics of a STO MIM capacitor at RF regime.



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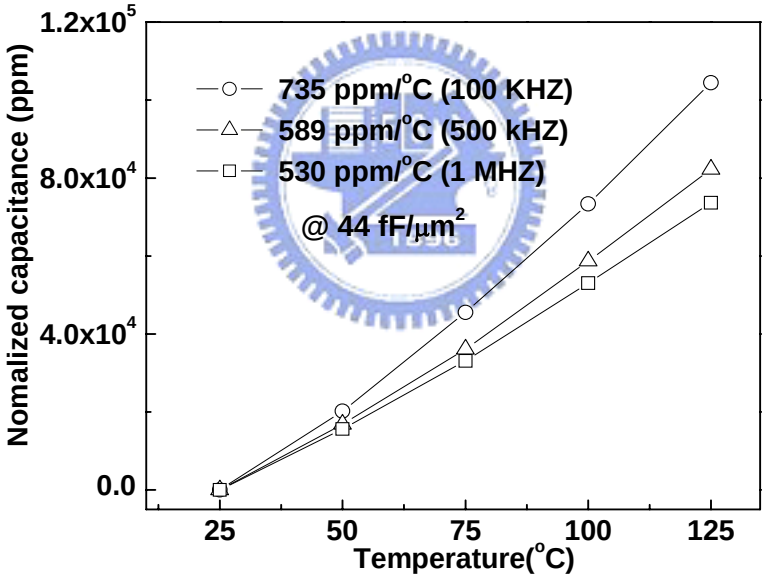


(b)

Figure 6-5 (a) Q-factor of TaN/STO/TaN MIM capacitors biased at 1.5V (b) The temperature-dependent normalized capacitance (TCC) with different frequency. The capacitor size is 20 μm×20 μm.

Chapter 7

Use of a High Work-Function Ni Electrode to Improve the Stress Reliability of Analog $SrTiO_3$ Metal-Insulator-Metal Capacitors

7.1 Introduction

When scaling down the device size of Metal-Insulator-Metal (MIM) capacitors [7.1~7.12] used for Analog, RF and DRAM functions in ICs, it is necessary to continuously increase the capacitance density ($\varepsilon_0\kappa/t_\kappa$) [7.1]. To achieve this goal the only choice is to increase the κ value of the dielectrics, which have evolved from Al_2O_3, HfO_2-Al_2O_3 [7.2~7.5], Nb_2O_5 [7.6], TiTaO (κ~45-50) [7.7~7.9] to $SrTiO_3$ (STO; κ~50-200) [7.10~7.14]. However, few studies of the stress reliability of the analog characteristics of MIM devices have been reported [7.4~7.5], beyond considerations of the simple time-dependent dielectric breakdown, despite its importance for circuit applications. This stress degradation is especially a concern in low-breakdown field and small-bandgap STO materials, which also leads to high leakage currents because of the small conduction band discontinuity (ΔE_C) with respect to Si [7.15]. Here we describe the stress reliability of the analog characteristics

of STO MIM capacitors. The use of high-work-function Ni instead of TaN electrodes not only reduces the high temperature leakage current, but also improves the constant-voltage stress degradations of the capacitance variation ($\Delta C/C$) and the quadratic voltage-coefficient-of-capacitance (VCC-α). The improved stress tolerance arises from reduced carrier injection and trapping in the MIM capacitor. Ni also provides a more cost-effective solution than high work-function Noble metals.

7.2 Experimental

The process to integrate the MIM capacitors into a VLSI backend process began with depositing a 2-μm-thick SiO_2 isolation layer on the Si substrates. Then the TaN/Ta layers were deposited by sputtering and subsequently treated in a nitrogen plasma, which largely improves oxygen deficiency and capacitance density degradation by forming interfacial TaON during post-deposition anneal (PDA) [7.10~7.12]. A 25nm-thick sputtered STO dielectric was then deposited, followed by a 420^{o}C furnace anneal for 30 min under an oxygen ambient, to improve the dielectric quality. This lower thermal-budget process, compared with previous nano-crystal STO approaches [7.10~7.11], is desirable for backend integration, but comes at the expense of a lower κ value. Finally, TaN or Ni was deposited and patterned to form the top capacitor electrode. The fabricated devices, having a 20-μm×20-μm area, were characterized by C-V and J-V measurements using an HP4156B semiconductor

parameter analyzer and an HP4284A precision LCR meter, respectively.

7.3 Results and discussion

Figure 7-1 shows the *J-V* characteristics of STO MIM devices. For negative bias, with electron injection from the upper electrode, use of Ni as the electrode gave ~two orders of magnitude lower leakage current at 125°C than devices using TaN. At positive bias, the leakage current is also reduced. This is due to additional voltage drop by band bending shown in the inserted thermal equilibrium-band diagram, which is originated from the higher work-function of Ni (5.1 eV) than TaN (~4.5 eV). Thus, improved leakage currents are obtained at both positive and negative bias [7.7]. The effect of voltage stress on the *C-V* characteristics is also shown in Fig. 7-2(a). The TaN top electrode gives slightly larger capacitance than the Ni electrode, which may be due to process variation and difference in capacitance from the space charge effect by different work-function [7.16]. However, such only 9% difference in capacitance can not explain the one to two orders of magnitude leakage current difference shown in Fig. 7-1. Furthermore, the desired smaller $\Delta C/C$ value after stress is displayed when using a Ni electrode. These results are for the 25°C case rather than the normally-used 85~125°C [7.17]. This is because the stress-induced degradation of $\Delta C/C$ was larger at 25°C than at 125°C, as shown in Fig. 7-2(b) – we suggest that this may be due to the charge de-trapping in the small bandgap STO MIM capacitor at elevated temperatures.

The higher ΔC/C at 125°C is due to the higher carrier injection at higher temperature, which gives much higher carrier concentration and a smaller relaxation time and leads to a larger capacitance variation [7.3~7.4]. In addition, the STO mixed with amorphous and crystalline phase by low temperature process achieves acceptable wafer uniformity, as shown in Fig. 2 (b) and (c) [7.18].

For analog/RF functions in a circuit, both a small $\Delta C/C$ and $VCC\text{-}\alpha$ are required. Here $\Delta C/C$ can be expressed as $VCC\text{-}\beta \times V + VCC\text{-}\alpha \times V^2$, where $VCC\text{-}\beta$ is the linear coefficient of the VCC. Figure 7-3 shows the effect of constant-voltage stress on the $\Delta C/C$-V characteristics of STO MIM capacitors with TaN or Ni electrodes. By using Ni the required small $\Delta C/C$ and $VCC\text{-}\alpha$ were achieved, regardless of the stress. In general the stress produced a lower $VCC\text{-}\alpha$, which is related to the charge trapping in the STO and the STO/metal interface. The trapped charges decrease the carrier mobility in the dielectric by electrostatic scattering, which in turn produces a smaller $VCC\text{-}\alpha$, according to a free-carrier-injection model [7.3~7.4].

The $\Delta C/C$ for a 10 year operational span is also important. Figure 7-4(a) shows the $\Delta C/C$ as a function of stress voltage for 10 year-reliability, this data was obtained from the $\Delta C/C$ plot by extrapolating to that time, as shown in Fig.7-4(b). Here the stress was performed at 25°C rather than 125°C, which should be a worse case as indicted by the results in Fig. 7-2(b). Here again the capacitors with a Ni electrode

show smaller *ΔC/C* for a stress extrapolated to 10 years than TaN case. Thus, the reduced charge injection by higher work-function electrode causes less trap or defect formation during the stress, which in turn suppress new dipole generation and achieve better *ΔC/C*. Besides, the relative smooth surface and mixed amorphous nano-crystalline STO [7.18], formed by low temperature process, may also reduce the charge trapping in interface and grain boundaries, respectively. It is worth noting that only <1% 10-year ΔC/C is obtained by linear-extrapolation to1 V. This is suitable for achieving good reliability for analog applications at 45 nm node and beyond operated at 1 V and less. Thus the high work-function Ni electrode not only decreases the leakage current in our devices but also improves the *ΔC/C* arising from charge trapping, and the stress reliability.

Furthermore, since the advanced ICs are usually operated at higher temperature due to power dissipation, the temperature dependences of VCCs and normalized capacitance (TCC) are other important factors, as shown in Figure 7-5. It is worth noting that these temperature dependences both become smaller with using Ni electrode. In sum, using the high work function Ni was found to not only determine electrical performance, but also largely improve its temperature dependences and reliability.

7.4 Conclusion

We have studied the stress reliability of low energy-bandgap, high-κ $SrTiO_3$ metal-insulator-metal capacitors under constant-voltage stress. By using a high work-function Ni electrode (5.1 eV), we reduced the degrading effects of stress on the capacitance variation ($\Delta C/C$), the quadratic voltage-coefficient-of-capacitance (VCC-α) and the long term reliability, compared with using TaN. The improved stress reliability for Ni electrode capacitors is attributed to a reduction of carrier injection and trapping.

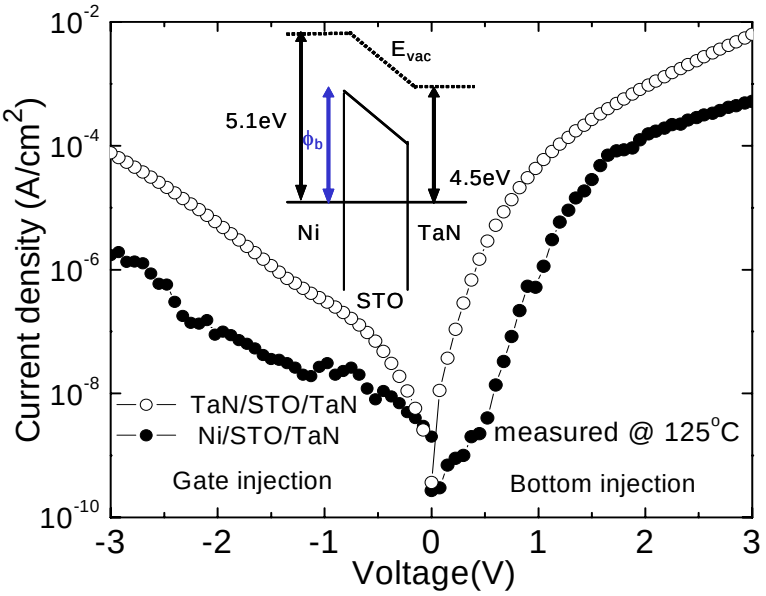
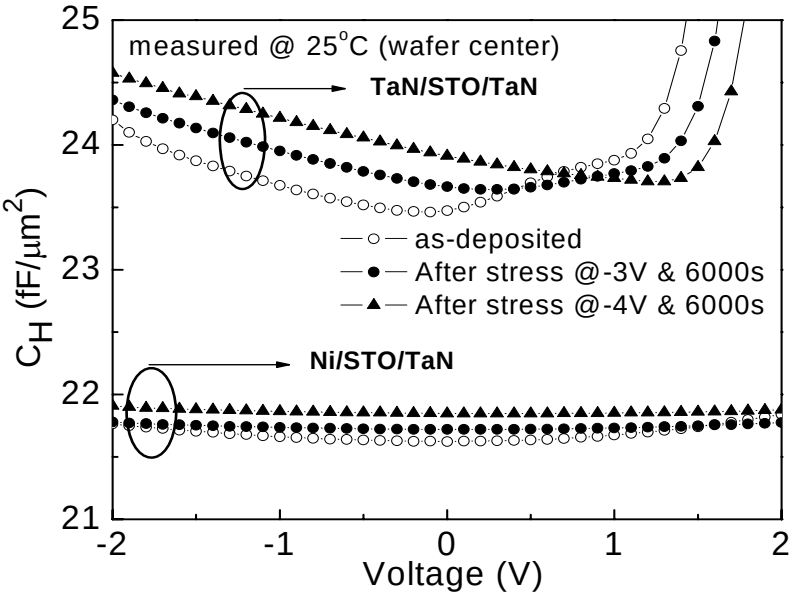
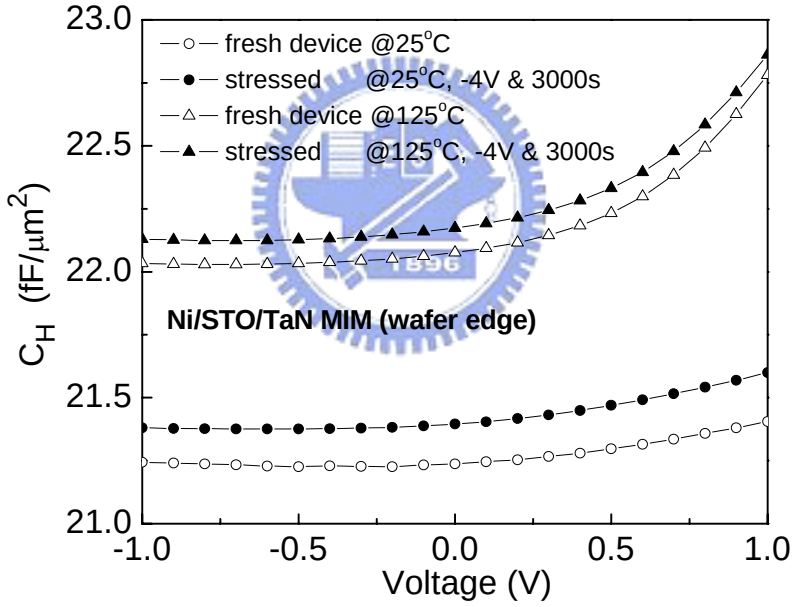


Figure 7-1 *J-V* characteristics of [Ni or TaN]/STO/TaN capacitors, measured at 125°C. The inserted figure is the band alignment of the STO MIM device with TaN or Ni as the upper electrode.



(a)



(b)

Figure 7-2 (a) *C-V* characteristics of [Ni or TaN]/STO/TaN capacitors before and after different voltage stress at 25°C. (c) *C-V* characteristics of Ni/STO/TaN capacitors before and after constant-voltage stress at 25 and 125°C.

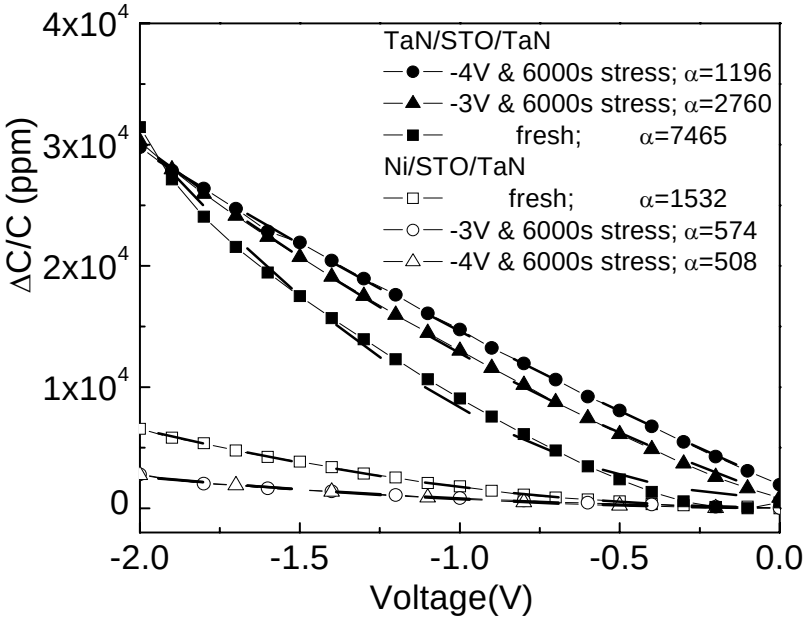
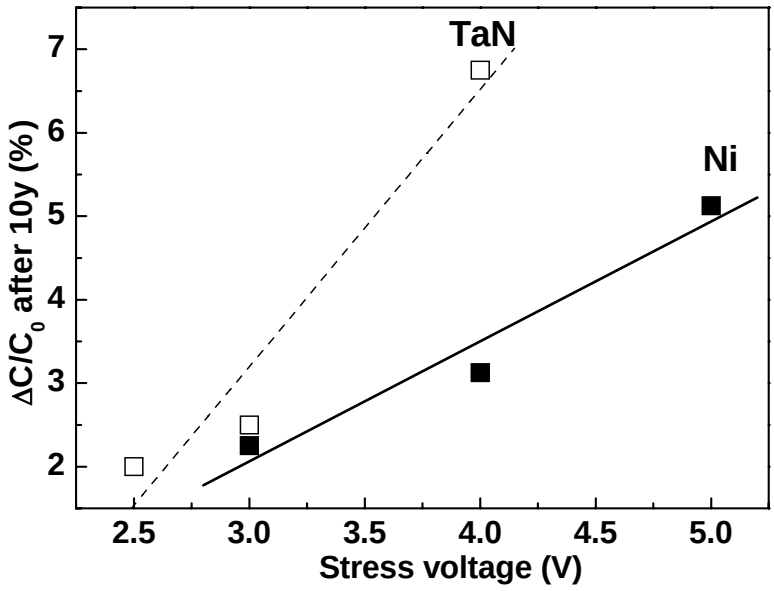
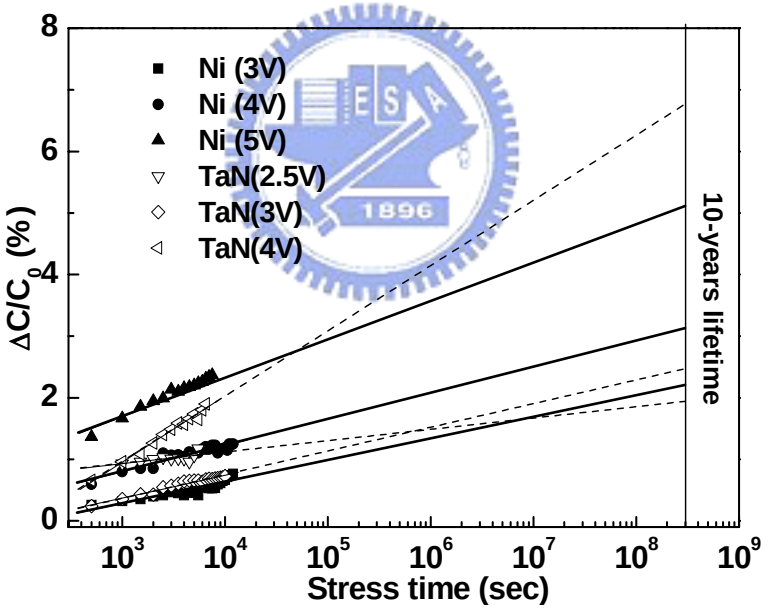


Figure 7-3 *ΔC/C-V* characteristics of MIM capacitors with Ni, and with TaN electrodes.



(a)



(b)

Figure 7-4 (a) The *ΔC/C* vs. stress voltage for a 10 year reliability period (b) The *ΔC/C* values for 10 year-stress were obtained from the figure of the extrapolated *ΔC/C* vs. stress time to 10 years.

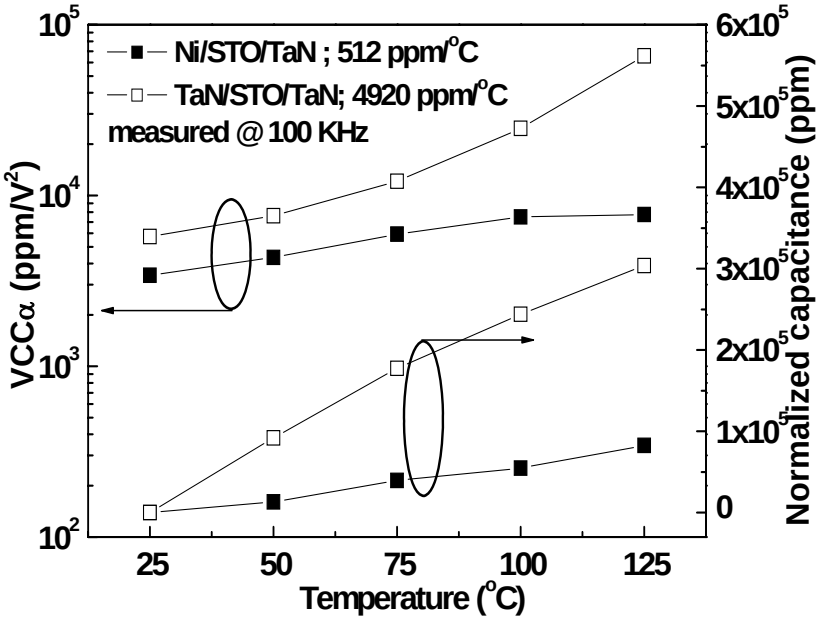


Figure 7-5 Temperature dependences of VCC α and normalized capacitance with Ni and TaN electrode.

Chapter 8

Conclusion

We have demonstrated new results to advance this technology. For the first time, high 10.3 fF/μm^2 density, low 89 ppm/V^2 voltage linearity and small 1.2×10^{-8} A/cm^2 leakage current are all measured in novel high-κ TiTaO (κ=45) MIM capacitor with high work-function Ir, which meet well the ITRS roadmap requirement for analog IC at year 2018. For higher speed analog/RF ICs, both very high 23 fF/μm^2 density and low 131 ppm/V^2 voltage linearity are obtained using the fast VCC decay mechanism with frequency >0.1GHz.

Furthermore, we report improvements in the thermal leakage current by using Ni as a high work function top electrode for high-κ TiHfO capacitors. This avoids sacrificing the overall κ value by using a multi-layer or laminate structure, and results in better voltage linearity, which is important for analog/RF ICs.

To increase the κ value beyond 45, we have fabricated STO MIM capacitors on conventional TaN electrode, where a NH_3 plasma treatment on bottom TaN is used to improve electrode stability and capacitance density degradation by forming interfacial TaON during post-deposition anneal (PDA). High 28 fF/μm^2 density, small quadratic voltage linearity (α) of 92 ppm/V^2 and low 3×10^{-8} A/cm^2 leakage current at 2 V are simultaneously measured, which beyond all the spec of ITRS at year 2018 for analog capacitors with almost 3 times better capacitance density. Further improving to 44 fF/μm^2 and low α of 54 ppm/V^2 are obtained for higher speed Analog/RF ICs at 2 GHz.

In addition, the stress reliability of low bandgap STO MIM capacitors was investigated. The stress degradation of $\Delta C/C$, VCC-α and the 10-year extrapolated reliability can be improved by using a high work-function Ni rather than a TaN electrode. Ni electrodes also have an added economic advantage over high work-function Noble metals.

Recommendation

The possible influences on voltage dependence of capacitance are summarized as the following section:

(A). Barrier height between dielectric and electrode:

Not only thermal leakage, VCC and TCC, bout also the stress degradation of $\Delta C/C$, VCC-α and the 10-year extrapolated reliability can be improved by using a high work-function Ni rather than a TaN electrode, as the above mention. According to free carrier injection model [8.1], this improved performance may be attributed to a reduction of carrier injection and trapping. Furthermore, based on schottky barrier model [8.2], the space charge accumulation at the electrode interface by Schottky potential of material electrodes may degrade MIM performance, especially for VCC and TCC. The space charge capacitance can be affected by the metal work function and the oxygen vacancies accumulation at electrode interface (interfacial layer). When the metal work function is large, the width of space charge capacitance will become large and the barrier height of the interface of dielectric/metal will become high. Therefore, high work function electrode should be considered for improving MIM capacitors.

(B). Interfacial layer:

The interfacial layer is responsible for higher leakage current, degraded VCC and

TCC, as discussed at above, and which may be due to the higher trap density from the oxygen deficiency. In addition, it could be also expected to work as parasitic series capacitors Ci with small capacitance. For this reason, lower fabricated temperature or NH_3 plasma treated TaN should be used to suppress interfacial layer growth from inter-diffusion and reaction between dielectric and electrode.

(C). Material properties:

Moving forward to construct high-k MIM capacitor, the most popular high-k materials are Al_2O_3, Ta_2O_5 and HfO_2 as a result of their readiness in DRAM and as gate dielectric. Although Ta_2O_5 exhibits superior VCC and TCC, it has poor leakage performance. Therefore, the Ta_2O_5 /HfO_2 /Ta_2O_5 stack with NH_3 plasma annealed at both interfaces of electrode and dielectric films has reported a low VCC2 of 16.9 ppm/V^2 [8.3]. In addition its thermal linearity is about 95 ppm/K and its leakage is midrange between the single layer Ta_2O_5 and HfO_2 , ~1E^{-7} A/cm^2 at 3.3 V, 125^oC. Another well engineered high- stack is that SiO_2/HfO_2. It makes use of the nullification effect of negative parabolic capacitance–voltage (C–V) curve of SiO_2 by the strong positive parabola of HfO_2 that produced a MIM with 14 ppm/V^2 at 7fF/μm^2 [8.4]. Hence, the proper dielectric of multi layer or compound material, such as TiTaO in this thesis is important for the development of advanced MIM devices.

(D). Surface roughness:

The surface roughness could induce higher leakage and *ΔC/C* due to local electric field enhancement. It is interesting that the amorphous dielectric, such as TiTaO and TiHfO exhibit the bottom injection is the worse case due to poly-crystallized lower electrode. However, the crystallized material, such as $SrTiO_3$ shows the gate injection is the worse case from degraded top interface, which is significant with increasing dielectric thickness. Consequently, using amorphous

dielectric and electrode may be a good method for this concern.

(E). Dielectric thickness:

The VCC α is strongly dependent on the capacitance density and electric field across on dielectric: an exponential decrease of α with increasing capacitance effective thickness (CET), or *1/C,* was observed for all the capacitors. In other words, for the same CET or capacitance density value, the higher-κ dielectric has the lower *VCC-*α due to lager thickness and decreased electric field. The α*–1/C* dependence is important to choosing the required C density and also meeting the analog specifications of a low α.

Overall, MIM capacitors incorporating a higher ϕ_m top electrode and a higher κ dielectric provide a practical approach to achieve low thermal leakage and good VCC simultaneously, without reducing the capacitance density - as in a multi-layer or laminate structure.