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電子工程學系 電子研究所

博 士 論 文

橫向擴散的射頻金氧半場效電晶體之佈局設計與熱特性分析

Layout Design and Thermal Characterizations of RF LDMOS

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國 立 交 通 大 學

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中文摘要

近年來，射頻橫向擴散金氧半場效電晶體(RF LDMOS)已廣泛地應用在手機基地台中，作為功率放大器的主要元件。為了能因應新一代通訊標準的需求，LDMOS 的特性必須不斷的加以改進。在本論文中，我們將探討兩種結構：ring 和 fishbone 的直流、高頻和射頻功率特性。在 fishbone 結構中，我們設計了具有不同漂移(drift)區長度、閘極長度、閘極指根數目與結構單元數目的元件。其中，具有較短漂移區長度的元件雖有較小的崩潰電壓，但其直流、高頻特性以及線性度均比較長漂移區長度的元件來的好。為了得到較低的開啟態電阻(on-resistance)以及緊密的排列結構，我們採用了一種四邊形的 ring 結構。在傳統的 MOSFET 中，寄生汲極電容指的是 n^+ 的汲極和 p 型基底間的接面電容。因此，汲極通常擺在內側來降低寄生電容。而在 LDMOS 的元件中，寄生電容指的是 deep n-well (DNW)和 p 型基

底間的接面電容。所以汲極擺在外側的結構並不會提高汲極電容。再者，由於 ring 結構排列較 fishbone 緊密，使得 DNW 的面積減小，汲極電容降低。為了能更進一步了解元件參數對高頻特性的影響，我們以小訊號等效電路將其參數萃出作為分析比較。實驗結果顯示，ring 結構之所以有較佳的特性是由於其寄生的汲極電阻比 fishbone 來的小。在 ring 結構中，汲極擺在閘極外側能有效的增加汲極面積，降低汲極電阻，進而達到降低元件開啟態電阻的目的。我們所設計的 ring 結構可以在相同的崩潰電壓基礎下降低開啟態電阻，並將最大震盪頻率(f_{max}) 提升 24.5%。此外輸出功率、功率增益以及附加功率效率均有較佳的表現，而線性度則和 fishbone 結構不相上下。由於 ring 結構只更動光罩之設計，製程流程並無改變，因此實為一大優點。

由於功率元件深受溫度的影響，因此元件的溫度效應也將一並討論。由之前的實驗結果得知，LDMOS 有較大的的寄生汲極電阻。因此需扣除寄生電阻的影響才能得到正確的溫度引起之 f_T 變化對轉導變化的關係。ring 結構由於排列較的較緊密，因此有較大的熱阻和較小的熱容，也就是自我熱效應比 fishbone 嚴重。在脈衝量測下，不論直流還是高頻特性均顯示 ring 有較好的特性。因此若是在脈衝模式操作下，ring 結構將會有更佳的特性表現。

另一方面，元件的電容特性也有完整的分析。由於 LDMOS 的通道為

非均勻參雜且具有漂移區，因此電容會有峰值產生。而在較大的汲極偏壓下，我們首次發現 ring 結構的電容會出現第二個峰值。這是因為 ring 結構的轉角處電流密度較小，使得閘極需偏壓在較大的電壓下才會進入類飽和。藉由溫度的變化來研究電容的改變，我們發現電容主要是受到臨限電壓、類飽和電流和漂移區的空乏電容所影響。因此在建立電容模型時，必須將這些效應考慮進去，以提升模擬的準確度。此外，根據實驗的結果來選擇電容對溫度較不敏感的偏壓區域對於電路的設計也極為重要。

Layout Design and Thermal Characterizations of RF LDMOS

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A Dissertation
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Abstract

RF LDMOS is nowadays widely used for base station applications. To meet the demands imposed by new communication standards, the performance of LDMOS is subject to continuous improvements. In this thesis, two types of layout structures, ring and fishbone, were studied for DC, high-frequency, and RF power characteristics. For fishbone structures, variation of drift lengths and channel widths, different numbers of gate fingers and cells were investigated. The structure with smaller L_{Drift} has better on-resistance, f_T, f_{max}, and linearity, but smaller breakdown voltage. To achieve lower on-resistance and a more compact device size, we adopted a “ring” structure in the layout design. In the traditional design, drain inside was usually used to lower the parasitic drain capacitance. For MOSFET, the conventional parasitic drain capacitance refers to the n^+ drain to p-substrate junction capacitance. Hence, the drain was always surrounded by the transistor channel and source to reduce the area. In LDMOS, however, the parasitic drain capacitance refers to the deep n-well (DNW) to p-substrate junction capacitance. Therefore, drain capacitance would not increase in a drain outside structure. Since the ring has more compact device size the area of DNW is smaller than the fishbone. This smaller area leads to a lower drain capacitance in the ring structure. In

order to determine the effect of device parameters on high-frequency characteristics more clearly, small-signal equivalent circuit was built to be analyzed. From the simulation results, the smaller drain parasitic resistance in the ring could be the key factor for improving f_T and f_{max}. For having the drift region, drain parasitic resistance is larger in the LDMOS than in the MOSFET and become an important parameter. In the ring structure, drain outside design has an advantage over drain inside in having larger area for output terminal. The extra areas in the corner would have lowered the drain parasitic resistance and improve the on-resistance. By using the ring structure, higher drain current and transconductance were shown by the reason of larger equivalent W/L and lower drain parasitic resistance. Also, f_{max} were enhanced by about 24.5% due to the lower drain parasitic resistance. As for microwave power characteristics, output power, power gain and power added efficiency (PAE) were improved with a similar linearity compared to the fishbone. Its reveals that the ring structure had a better performance and similar breakdown voltage compared to the fishbone structure, without altering the process flow.

For high-power applications, temperature is an important issue. For conventional MOS transistors in RF applications, the temperature effect was investigated by studying the temperature dependence of f_T, which is proportional to the transconductance. Owing to the higher drain resistance in the LDMOS transistors, the f_T is also affected by drain resistance. By de-embedding the effect of drain resistance, we show the real relation between the temperature-induced variation of f_T and transconductance. In order to study the self-heating effect on the performance of LDMOS, I-V and RF characteristics were also measured under a pulsed condition. From the extracted thermal resistance and thermal capacitance, the effect of self-heating was more severe in ring structure. In the pulsed-mode measurement, the ring has better drain current, f_T and f_{max} than the fishbone structure. Although the ring structure showed lower static drain current than the fishbone structure at high gate biases due to the significant self-heating effect, its current drive capability could be improved using a pulsed-mode

operation.

In another part of this thesis, we discussed and analyzed the capacitance characteristics completely. For having a non-uniform doping channel and the existence of the drift region, C_{GS}+ C_{GB} and C_{GD} exhibit a peak in LDMOS. In the ring structure, the second peaks in a capacitance-voltage curve have been observed at high drain voltages for the first time. While the corner region of the drift in the ring shows lower current density than the edge region, it needs higher gate voltage to enter quasi-saturation. By increasing the gate voltage, the current in the corner region is high enough to make the velocity of electrons in the drift saturated. Therefore, the corner operates in quasi-saturation and second peaks are generated. The thermal effects on capacitances were also investigated. Because the capacitances are affected mainly by the threshold voltage, quasi-saturation current and drift depletion capacitance, the variation of the capacitances with temperature is more complicated than that in conventional MOSFET, and it depends on the bias condition. Based on the result we analyzed, we can well model the temperature-dependence capacitance by adding these parameters and also can choose a bias condition with lower temperature sensitivity in capacitances.

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Chapter 1

Introduction

1.1 Introduction to RF LDMOS

The Lateral-Diffused MOS (LDMOS) transistors are traditionally used in switching applications for a high voltage device and enter to the RF power application in the early 70's. The first publication of LDMOS for microwave operation was demonstrated in 1972 [1]. Until now, LDMOS are used in a wide range of applications requiring RF power amplification like: Wireless infrastructure (GSM, EDGE, WCDMA, and WiMAX); Broadcast; pulsed radar; industrial, scientific and material (ISM) applications; avionics and military application [2]. Up to 2005, Si LDMOS covered about 90 percent of the high power RF amplification applications in the 2GHz and higher frequency range, according to market analyst company Yole Développement. Now, Wireless infrastructure still represents the largest segment for RF power semiconductors. RF power amplifiers are key components in base stations for personal communication systems and require for low cost, high efficiency, and good linearity [3]. For frequencies ranging from 450 MHz to 2.7 GHz, LDMOS transistor technology has played a predominant role in the power amplifier applications due to its advantages in performance, cost, reliability, and power capability [4]. LDMOS process was introduced and targeting the base stations market in the early 1990s [5]. This technology has already gone through a lot of gradual progress so far. The market for base-station power amplifiers in wireless communication systems has grown rapidly in recent years. Silicon based LDMOS have been used for wireless technologies like GSM, EDGE, CDMA, WCDMA and WiMAX [6]. Now, capable of operation at frequency up to 3.5GHz and 3.8GHz for WiMAX are on the market [7-8].

1.1.1 Advantages Compared to the Bipolar Technology

The advantages of using LDMOS for high power high frequency applications are on the following points:

High linearity: the process controlled short channel length makes the device works in velocity saturation. The linear relation of drain current and gate voltage leads to a constant transconductance and improve the linearity.

Higher gain: the power gain can be improved by the lower source inductance and lower feedback capacitance. The former can be done by tying the source and P-body together to the RF ground. In bipolar, the backside collector requires insulating from the ground and the top side emitter needs bond wire to connect to the ground. The additional bond wire introduces high inductance and limits the power gain. Also, the LDMOS is a lateral structure device which has lower feedback capacitance compared with a bipolar transistor. In addition, the LDMOS has negative temperature coefficient and does not need ballast resistor which used in bipolar and degrade the bipolar's power gain. Therefore, the LDMOS provides higher gain than bipolar for the same output power level. This means that less amplifier stages are needed, and thus gives higher reliability and lower cost.

Thermal stability: LDMOS has no thermal runaway problem due to its negative temperature coefficient. The higher drain current leads to higher temperature which lowers the channel mobility and resulting in a drop in drain current. On the other hand, the temperature coefficient in bipolar is positive and more prone to thermal runaway

High ruggedness: LMODS has positive temperature coefficient of channel resistance and high drain-source breakdown voltage. Consequently, LDMOS has excellent ruggedness into an output mismatch VSWR typically 10:1 whereas the bipolar can only accept 3:1 [9-10].

1.1.2 Advantages Compared to Other Materials

The current states of technology for base station application include GaAs and wide

bandgap materials: SiC and GaN. GaAs based power devices can achieve higher drain efficiency and linearity due to a higher electron mobility and higher saturation velocity then silicon. However, lower thermal conductivity about 0.46 W/cm K limits the applicability of GaAs for the high power final stage amplifiers which is needed in base station transmitters. Also, the conventional GaAs-based FET's have serious limitations in terms of operation voltage as compared with LDMOS and typically suitable for handset application [11]. The wide bandgap materials, SiC and GaN, have high electric breakdown voltage field and high saturation velocity. However, even a superior technology must be cost competitive. High cost (for the expensive substrate) in comparison to LDMOS and GaAs shows the must significant barrier to market adoption for GaN and SiC [12]. For LDMOS, the high thermal conductivity about 1.5 W/cm K with the drift region design achieve quite high operation voltage which makes this technology suitable for base station power amplifier.

1.2 Motivation

By scaling down the gate length and the drift length, the performance can be significantly improved with lower on-resistance and higher transconductance. However, the scaling may have reached the limit of high-voltage endurance during power-amplifying operations. In the conventional LDMOS, there is a trade-off between the on-resistance and the breakdown voltage; the drain current and the breakdown voltage. Several researchers have proposed solutions to these trade-offs such as using a double-doped offset [13], or a stacked or step drift region [14-16], or even the strain structure [17]. As well as by changing the device process flow, the trade-off between the on-resistance and the breakdown voltage can also be solved by optimizing the layout design. In this thesis, two types of layout structures, ring and fishbone, were studied for DC, high-frequency, and RF power characteristics.

Since the power transistors are operated at high power densities, the device temperature is high due to self-heating effect. Therefore, temperature is an important issue and need to be

investigated. The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are critical figures of merit for evaluating the performance of RF transistors. According to its structure, the parasitic drain resistance of the LDMOS becomes more important than that of the conventional MOSFET for the present drift region. However, in most of the studies, the effect of the parasitic resistance was not considered when analyzing the temperature effect on the device characteristics [18-20]. By de-embedding the effect of the parasitic source and drain resistors from the measured S-parameters, the temperature dependence of the intrinsic f_T can be analyzed. Several researchers have investigated the effects of temperature on the reliability and dc performances of LDMOS transistors [21-23]. However, the temperature effects on the high-frequency characteristics of LDMOS have seldom been addressed. In addition, the device capacitances influence the input, output and feedback capacitances, which are important in the dynamic operation, and have large impact on device high-frequency performance. The capacitance characterization and modeling of LDMOS transistors have been studied widely [24-28]. Nevertheless, the temperature effects on the capacitance characteristics of LDMOS transistors are not mentioned in previous literatures. In this thesis, the DC, high-frequency, and RF power characteristics of LDMOS transistors with different layout structures were studied at various temperatures. Also, the temperature effects on capacitance characteristics were analyzed.

1.3 Thesis Organization

The content in this thesis includes the following parts.

Chapter 1 introduces the LDMOS for RF applications and the motivation of this thesis.

Chapter 2 presents two layout structures, ring and fishbone. The DC, high-frequency and RF power performance were analyzed with various drift length and channel width. Also, small-signal model parameters were extracted to investigate the effect of different parameters on f_T and f_{max}.

Chapter 3 presents thermal effects on DC and RF performance of RF LDMOS with ring and fishbone structures. By de-embedding the effect of the parasitic source and drain resistors, the temperature dependence of the intrinsic f_T can be analyzed. In addition, Pulsed I-V and RF characteristics were measured to investigate the self-heating effect on the performance of an LDMOS.

Chapter 4 presents the unusual behavior in capacitance of RF LDMOS with ring and fishbone structures. The capacitance characteristics have also been studied at various temperature conditions. Both capacitance versus gate voltage with different drain voltage and capacitance versus drain voltage with different gate voltage were investigated.

Chapters 5 summarize the conclusions of this thesis.

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Chapter 2

Characterization of RF LDMOS with Different Layout Design

2.1 Introduction

In high-power applications, the RF transistors are usually implemented in a "fishbone" structure, as shown in Fig. 2.1(a), due to the self-heating concern. All the gate fingers are divided into several subcells, in each of which, 2-10 gate fingers are grouped together. For RF performance concern, multi-finger layouts are used to design wide MOSFETs for reducing the gate resistance and source/drain junction capacitance. Since the gate resistance would limit the power gain attainable at a certain frequency and thus f_{max}. The DC and RF characteristics were affected by the gate finger length and width, number of gate fingers, number of cells, and drift region length and could be improved through layout optimization [1-5]. The drain resistance which includes accumulation layer resistance, JFET resistance, and epi-resistance are the main component in VDMOS to have influence on the on-resistance. Some literatures present various geometries for the on-resistance minimization but all focus on VDMOS and confine to the DC characteristics [6-10]. Here, in order to achieve lower on-resistance and a more compact device size, we adopted a "ring" structure which is different from the "fishbone" in the LDMOS layout design (see Fig. 2.1(b)). Two types of layout structures for DC, high-frequency, and RF power characteristics were investigated.

2.2 RF LDMOS with Fishbone Structure

RF LDMOS transistors were fabricated using a 0.5 μm LDMOS process. The schematic cross section of the device is shown in Fig. 2.2. The drain region was extended under the field oxide (FOX) and consisted of a lightly doped N-well drift region and an N^- region with higher doses for on-resistance control. The source region and the p-body were tied together to

eliminate extra surface bond wires to reduce the source inductance and improve the RF performance in a power amplifier configuration [11]. The gate oxide thickness was 135 Å and the mask channel length (L_{CH}) was 0.5 μm . The drift length ($L_{Drift}=L_{OV}+L_{FOX}$) was varied for 3.0 μm, 3.6 μm, and 4.2 μm. For the fishbone structure, three samples with finger width L_F=10 μm were investigated in this study. Sample 1: with 6 cells, each cell had 2 fingers, and total channel width was W=120 μm (see Fig. 2.3(a)). Sample 2: with 12 cells, each cell had 2 fingers, and total channel width was W=240 μm. Sample 3: with 4 cells, each cell had 6 fingers, and total channel width was W=240 μm (see Fig. 2.3(b)).

2.2.1 DC Characteristics

Table 2-1 lists the extracted on-resistance (R_{on}) for the three samples with various drift length. The R_{on} was extracted from the linear forward *I-V* characteristics at gate voltage V_{GS}=2 V and normalized to the total width. For a fixed drift length, the three samples had similar value of R_{on}. As the drift length increased, the R_{on} increased due to a larger drain series resistance. Fig. 2.4 shows the *I–V* characteristics of the LDMOS with different drift length. The device with larger L_{Drift} showed a lower drain current and transconductance. Also, the breakdown voltage was higher with a larger L_{Drift} device. For a larger L_{Drift}, the higher resistance in the drift region leaded to a large voltage drop which increased the carrier velocity and eased to enter the velocity saturation. The velocity saturation in the drift region is called “quasi-saturation” while intrinsic MOS is still in linear operation. This effect is generally observed at high gate voltages. As the device enter the quasi-saturation, the gate control ability decreases which limits the drain current level and delays the transition between linear and saturation regime. At gate voltage V_{GS}=4V in Fig. 2.4(b), larger L_{Drift} made the device enter the saturation slower and limited the drain current level clearly. Also, the transconductance for L_{Drift}=4.2 μm in Fig. 2.4(a) started to fall as the gate voltage higher than 3.5V.

2.2.2 High-frequency Characteristics

To characterize the high-frequency performance, the S-parameters were measured on-wafer from 0.1 to 20 GHz using an HP8510 network analyzer and then de-embedded by subtracting the OPEN dummy. Fig. 2.5 shows the high-frequency characteristics of sample 2 with L_{Drift}=3.0 μm. The maximum stable gain/maximum available gain (MSG/MAG) and short-circuit current gain (h_{21}) were calculated from S parameters. The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) were determined as the frequency where the current gain was 0 dB and the frequency where MAG was 0 dB, respectively. The transistors were measured at drain voltage V_{DS}=28 V with different gate voltages. f_T and f_{max} had maximum values at V_{GS}=2 V, where the transconductance showed a peak. With increasing the gate voltage, both f_T and f_{max} decreased owing to the mobility degradation and quasi-saturation effects.

The dependences of the cutoff frequency and maximum oscillation frequency on the drift length for the LDMOS with different geometries are compared in Table 2-2. The transistors were biased at V_{GS}=2 V and V_{DS}=28 V to obtain the maximum value of f_T. From Table 2-2, the f_T and f_{max} both decreases with increasing L_{Drift}. By analyzing a MOSFET small-signal equivalent circuit, we can determine the effect of device parameters on high-frequency characteristics more clearly. We adopted a simple model (shown in Fig. 2.6) and extracted the equivalent circuit parameters of the LDMOS by the method described in ref. 12. After de-embedding the extrinsic parasitic resistances and the substrate-related parameters, the intrinsic components can be directly extracted from intrinsic Y-parameters (Y_i) by the following equations [13]:

$$C_{gd} = -\frac{1}{\omega}\mathrm{Im}(Y_{i,12})$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{i,11}) - \omega C_{gd}}{\omega} \cdot (1 + \frac{(\mathrm{Re}(Y_{i,11}))^2}{(\mathrm{Im}(Y_{i,11}) - \omega C_{gd})^2})$$

$$C_{ds} = \frac{1}{\omega}\mathrm{Im}(Y_{i,22} + Y_{i,12})$$

$$R_i = \frac{\mathrm{Re}(Y_{i,11})}{(\mathrm{Im}(Y_{i,11}) - \omega C_{gd})^2 + (\mathrm{Re}(Y_{i,11}))^2}$$

$$R_{ds} = \frac{1}{\mathrm{Re}(Y_{i,22})}$$

$$g_{m0} = \sqrt{((\mathrm{Re}(Y_{i,21}))^2 + (\mathrm{Im}(Y_{i,21}) + \omega C_{gd})^2) \cdot (1 + \omega^2 C_{gs}^2 R_i^2)}$$

$$\tau = \frac{1}{\omega} arc\sin(\frac{-\omega C_{gd} - \mathrm{Im}(Y_{i,21}) - \omega C_{gs} R_i \,\mathrm{Re}(Y_{i,21})}{g_m})$$

The cutoff frequency can be expressed in a simple way of $f_T = g_m/2\pi(C_{gs}+C_{gd})$ which is related to the intrinsic transconductance (g_m) and input intrinsic capacitances ($C_{in}=C_{gs}+C_{gd}$). Fig. 2.7 shows these parameters with respect to the drift length. As the L_{Drift} increased, the decreasing of g_m and increasing of C_{in} resulting in the degradation of f_T. In addition, the ratios of g_m to C_{in} were similar for fixed drift lengths which indicate that f_T were comparable for these three samples. The approximate maximum oscillation frequency can be expressed as follows: [14]

$$f_{\max} \sim \frac{f_T}{\sqrt{4 g_{DS} R_g + 8\pi f_T C_{gd}(R_g + \alpha R_d)}}$$

From Table 2-2, f_{max} shows lower value with higher L_{Drift} due to the decreasing of f_T and increasing of drain resistance. With fixed L_{Drift}, f_{max} was similar in sample 1 and 2 but showed higher value in sample 3. Compare sample 1 with sample 2, two times increasing of total finger numbers in sample 2 leaded to two fold increase of C_{gd} and g_{ds}; two fold decrease of R_g and R_d [15]. For having the same finger numbers in each one cell, the devices area also increased two times for sample 2 (i.e. two times in C_{jdb}). The drain-to-substrate junction capacitance (C_{jdb}) refers to the deep n-well (DNW) to p-substrate/p-body junction capacitance

(see Fig. 2.2) and this capacitance also has impact on f_{max} [16]. Therefore, the effects of these parameters were compensated and no variations were observed in f_{max}. In sample 3, the number of fingers in one cell was 6 rather than 2 in sample 2. This indicates that the device area was lowered than sample 2 and less than two times than sample 1. Consequently, the lower C_{jdb} can not be canceled by the increase of R_g and R_d; and sample 3 exhibits higher f_{max} than sample 1 and 2.

2.3 Comparison of Two Layout Design: Fishbone and Ring

The fishbone structure used in this study had 6 cells which each cell had 6 fingers with finger width L_F=10 μm. For the ring structure, the width of each gate ring was 4×10 μm and all the rings were arranged as a 3x3 array in one device. In each ring, the source region was surrounded by the drain region, while the gate was located between the source and the drain (see Fig. 2.1). To compare the performance of the fishbone and ring structures fairly, both structures had the same total channel width (W=360 μm).

2.3.1 DC Characteristics

The *I–V* characteristics of the LDMOS with different layout structures are shown in Fig. 2.8. In low- and medium-bias regions, the ring structure showed a higher drain current and transconductance than the fishbone structure. This attribute to the lower drain parasitic resistance (R_d). In addition, the breakdown voltage of the ring structure was similar to that of the fishbone structure (V_{BD}≅46-52V for drift length L_{Drift} =3.0-4.2 μm). Hence, the ring structure had better DC performance than the fishbone structure. However, when the devices were biased at higher gate and drain voltages, the transconductance and drain current of the ring structure decreased and became smaller than those of the fishbone structure. From the output *I–V* characteristics of the ring structure, we observed a negative output resistance in the

high-current region. It indicated the self-heating effect in the ring structure was significant due to the compact layout area. With high current density in the transistor, the rise in device temperature due to the dissipated power became significant. The increased device temperature would reduce the carrier mobility and saturation velocity [17]. The device self-heating could be improved by increasing the distance between rings. The drain-source on-resistance is an important parameter for describing the performance of LDMOS transistors. The on-resistance (R_{on}) was extracted from the linear forward I–V characteristics at gate voltage V_{GS} = 2 V, since it was predominated by the drift region under such a condition. The extracted R_{on} was plotted against the drift length in Fig. 2.9. As the drift length increased, the on-resistance increased in both structures due to a high drain parasitic resistance. R_{on} was related to the drain current and was dependent on the drain resistance. Therefore, R_{on} was lower in the ring structure than that in the fishbone structure and was interpreted as being due to a lower drain resistance.

2.3.2 High-frequency Characteristics

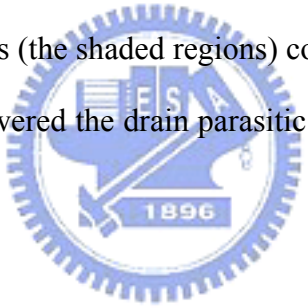
The dependences of the cutoff frequency and maximum oscillation frequency on the drift length for the LDMOS with different layout structures are compared in Fig. 2.10. The transistors were biased at V_{GS}=2 V and V_{DS}=28 V to obtain the maximum value of f_T. It was observed that f_T and f_{max} both decreased with increasing L_{Drift} because the g_m decreased and both C_{in} and drain resistance increased with increasing L_{Drift}. In Fig. 2.10, we also found that f_T and f_{max} for the ring structure had higher values than those for the fishbone structure. This might be attributed to the reduction of drain parasitic resistance. In addition, the difference in f_{max} between the fishbone and ring structures was larger than the difference in f_T.

By analyzing a MOSFET small-signal equivalent circuit, we can determine the effect of device parameters on high-frequency characteristics more clearly. Using extracted parameters from the existing device and altering one parameter at the time, the effect of model

parameters on the cutoff frequency and maximum oscillation frequency can be visualized. The influences of model parameters on f_T and f_{max} are shown in Fig. 2.11. The x-axis showed the parameter value departure from the initial value in percent. The y-axis showed the change in frequency in percent. Parameters not shown in the figure had approximately the same value for the ring and fishbone structures or had a minor influence on f_T and f_{max}. Table 2-3 lists the parameters that have more influence on f_T and f_{max} for the fishbone structures with different drift length. When L_{Drift} shorten to 3.0 μ m, transconductance (g_m) and gate-source capacitance (C_{gs}) were the two major parameters that improve the f_T and f_{max}. To investigate the superior high-frequency performance on ring structure, parameters that affect the f_T and f_{max} were analysis for fishbone and ring. The parameters that affect f_T more significantly (see Fig. 2.11(a)) are listed in Table 2-4. In conventional MOSFET, the intrinsic parameters, g_m, C_{gs}, and gate-drain capacitance (C_{gd}), were usually considered to explain the change in cutoff frequency due to the simple express $f_T=g_m/2\pi(C_{gs}+C_{gd})$. However, the existence of the drift region in LDMOS makes the extrinsic parameter, drain resistance (R_d), become more important and can not be ignored. R_d represents the drain contact resistance and part of the drift region. As R_d decreased from 18.06 Ω to 7.789 Ω, f_T could be improved by as much as 3.56% for the ring structure. In addition, the lower C_{gd} and higher C_{gs} in the ring structure caused about 1.57% and -2.8% changes in f_T due to different layout design. As for g_m and drain-to-substrate junction capacitance (C_{jdb}), the impact on f_T was too small to be considered. By analyzing f_{max}, we found that the intrinsic parameters like g_m, C_{gs}, and C_{gd}, showed a minor influence when we changed the device structure. Hence, we only considered the influence of extrinsic parameters. The extrinsic parameters that affected f_{max} more significantly (see Fig. 2.11(b)) are listed in Table 2-5. As R_d decreased from 18.06 Ω to 7.789 Ω, f_{max} could be improved by as much as 21.5% for the ring structure. In addition, the lower C_{jdb} in the ring structure also increases f_{max} by about 14.27%, due to the smaller device area. For the gate resistance (R_g), the different layout design in the ring structure increases R_g and

decreased f_{max} by about 10.52%. Using the ring structure, we estimated that f_T improved by about 2.72% (f_T was 3.77 GHz for the ring structure and 3.67 GHz for the fishbone structure) and f_{max} improved by about 24.5% (f_{max} was 10.18 GHz for the ring structure and 8.183 GHz for the fishbone structure). Therefore, R_d could be the key factor for improving f_T and f_{max} by using the ring structure.

Figure 2.12 shows the extracted drain parasitic resistance versus the drift length for LDMOS transistors with different layout structures. As L_{Drift} increased, the drain parasitic resistance increased. Note that for higher breakdown voltages, L_{Drift} needed to be longer, resulting in poor on-resistance, f_T, and f_{max}. Nevertheless, R_{on} and f_{max} for the ring structure appeared superior to those for the fishbone structure. The improvements of DC and RF characteristics were attributed to the minor drain resistance (see Fig. 2.12). The drain region of the ring structure had extra areas (the shaded regions) compared with the fishbone structure, and the extra areas would have lowered the drain parasitic resistance, as shown in the inset of Fig. 2.12.



2.3.3 RF Power and Linearity

As well as the high-frequency characteristics, the microwave power characteristics were also investigated using the load-pull measurement. In our study, the input was terminated to 50 ohms and the load impedances were tuning for maximum output power. For having the value of f_{max} in the range from 8 GHz to 11 GHz, the devices were measured at 900 MHz with gate bias V_{GS}=2 V and drain bias V_{DS}=28 V. Figure 2.13 shows the output power, power gain and power added efficiency (PAE) with different drift lengths. In Fig. 2.13, the power characteristics were similar among these two transistors at low input power and show discrepancy when input power was larger than 1-dB compression point (P_{1db}). The main reason for gain compression was attributed to the clipping effect. The border of output I-V curve will cause output waveform to be clipped for MESFET, PHEMT and HBT [18-20]. The

clipping effect can also been found in LDMOS. Figure 2.14 shows the drain current versus gate voltage with input and output waveform for different drift lengths. Part of the AC-signals on the drain current would be cut off as the input power becomes larger enough. At this condition, the average drain current increased with the increasing input power (see Fig. 2.15) and the power gain has been compressed. This is because the dynamic load line exceeds the border of DC I-V. As the drift length increased, larger on-resistance decreased the drain current which makes the negative duty cycle of output waveform enter the cutoff region earlier. This indicates that the average drain current started to increase earlier (see Fig. 2.15) and the gain compression occurs prior. Consequently, the transistor with longer drift length showed lower value of output power, power gain and PAE when input power was larger than P_{1db}. Figure 2.16 shows the RF power characteristics for different layout structures. The ring structure exhibits a better performance than the fishbone.

Since the dc behaviors were changed, the linearity would also be affected with various drift lengths. The input and output third-order intercept points (IIP3 and OIP3) for fishbone with various drift lengths are listed in Table 2-6. Also, the ring and fishbone for fixed L_{Drift} =3.6 μm were compared. For the fishbone structures, the transistor with longer drift length showed poor linearity. With fixed L_{Drift}, IIP3 and OIP3 was similar in the fishbone and ring structure (as shown in Fig. 2.17).

2.4 Summary

Fishbone with various layout designs for RF applications were investigated. The structure with smaller L_{Drift} has better on-resistance, f_T, f_{max}, and linearity, but smaller breakdown voltage. It shows a trade-off between the on-resistance and the breakdown voltage in the conventional LDMOS. Fishbone and ring structures for RF applications were also compared. The ring structure had a better performance than the fishbone structure, without

altering the process flow. The higher drain current and transconductance in the LDMOS with the ring structure were due to lower drain parasitic resistance. In addition, the f_T and f_{max} were also enhanced for the ring structure due to the lower drain parasitic resistance. Our results suggested that, using a ring structure, a higher breakdown voltage can be achieved using a longer L_{Drift} without degrading DC and RF characteristics.

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Table 2-1 The extracted on-resistances for three samples with various drift lengths.

	L_{DRIFT} (μ m)	R_{on} (Ω-mm)
Sample 1	3.0	49.46
	3.6	55.17
	4.2	58.28
Sample 2	3.0	50.85
	3.6	55.81
	4.2	57.69
Sample 3	3.0	52.55
	3.6	56.13
	4.2	58.49

Table 2-2 Cut-off frequency and maximum oscillation frequency for three samples with various drift lengths.

	L_{DRIFT} (μ m)	f_T (GHz)	f_{max} (GHz)
Sample 1	3.0	4.50	7.91
	3.6	3.75	6.91
	4.2	3.56	6.68
Sample 2	3.0	4.20	7.76
	3.6	3.62	6.94
	4.2	3.48	6.34
Sample 3	3.0	4.32	8.64
	3.6	3.68	7.87
	4.2	3.54	6.95

Table 2-3 Extracted g_m, R_d, C_{gd}, and C_{gs} for fishbone structure with various drift lengths. The f_T and f_{max} differences between the L_{Drift}=3.6 μm and 3.0 μm due to the change of model parameters are also listed.

	g_m (A/V)	R_d (Ω)	C_{gd} (F)	C_{gs} (F)
Fishbone L_{Drift}=3.6 μm	29.69m	16.05	133.5f	877.2f
Fishbone L_{Drift}=3.0 μm	27.08m	18.06	130.0f	951.0f
f_T Difference	8.87%	0.68%	-0.48%	6.77%
f_{max} Difference	6.88%	2.78%	-0.86%	5.4%

Table 2-4 Extracted g_m, R_d, C_{gd}, C_{gs}, and C_{jdb} for different layout structures. The f_T differences between the fishbone and ring structures due to the change of model parameters are also listed.

	g_m (A/V)	R_d (Ω)	C_{gd} (F)	C_{gs} (F)	C_{jdb} (F)
Fishbone L_{Drift}=3.6 μm	27.08m	18.06	130.0f	951.0f	244f
Ring L_{Drift}=3.6 μm	27.11m	7.789	119.0f	985.0f	149f
f_T Difference	0.11%	3.56%	1.57%	-2.8%	0.1%

Table 2-5 Extracted R_d, C_{jdb}, and R_g for different layout structures. The f_{max} differences between the fishbone and ring structures due to the change of model parameters are also listed.

	R_d (Ω)	C_{jdb} (F)	R_g (Ω)
Fishbone L_{Drift}=3.6 μm	18.06	244f	1.997
Ring L_{Drift}=3.6 μm	7.789	149f	4.489
f_{max} Difference	21.5%	14.28%	-10.52%

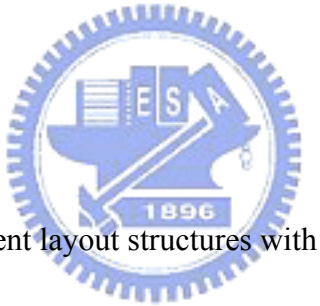


Table 2-6 IIP3 and OIP3 for different layout structures with various drift length

	IIP3 (dBm)	OIP3 (dBm)
Fishbone L_{Drift}=3.0 μm	29.18	41.60
Fishbone L_{Drift}=3.6 μm	21.84	34.31
Ring L_{Drift}=3.6 μm	21.51	34.29

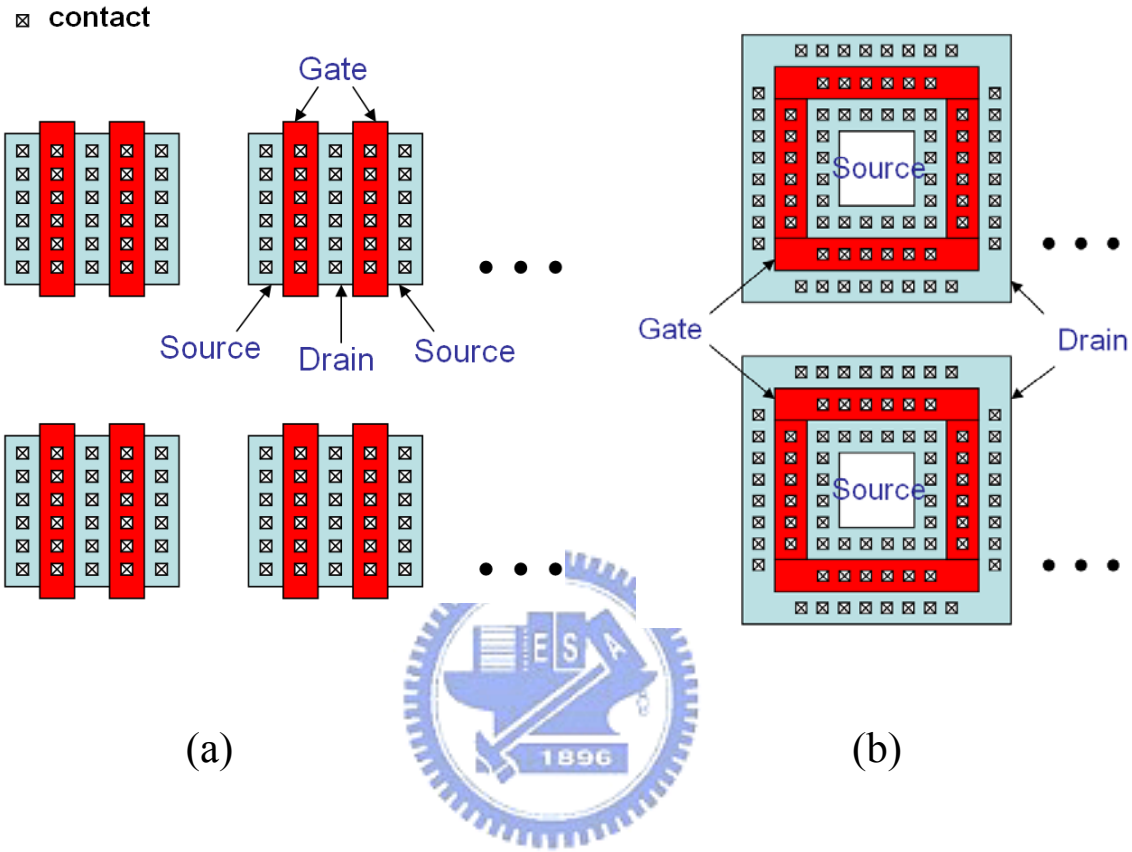


Fig. 2.1 LDMOS layout structures: (a) fishbone and (b) ring.

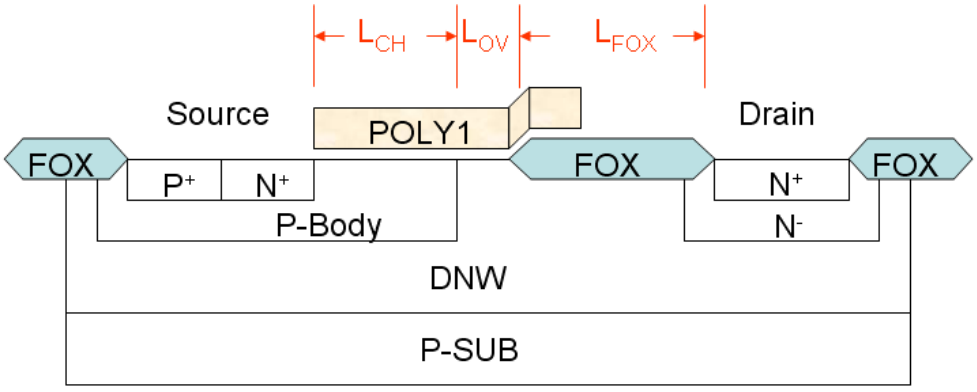
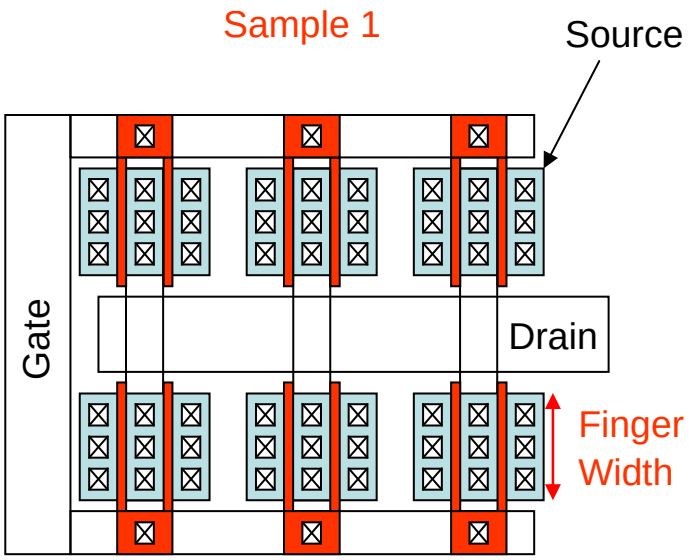
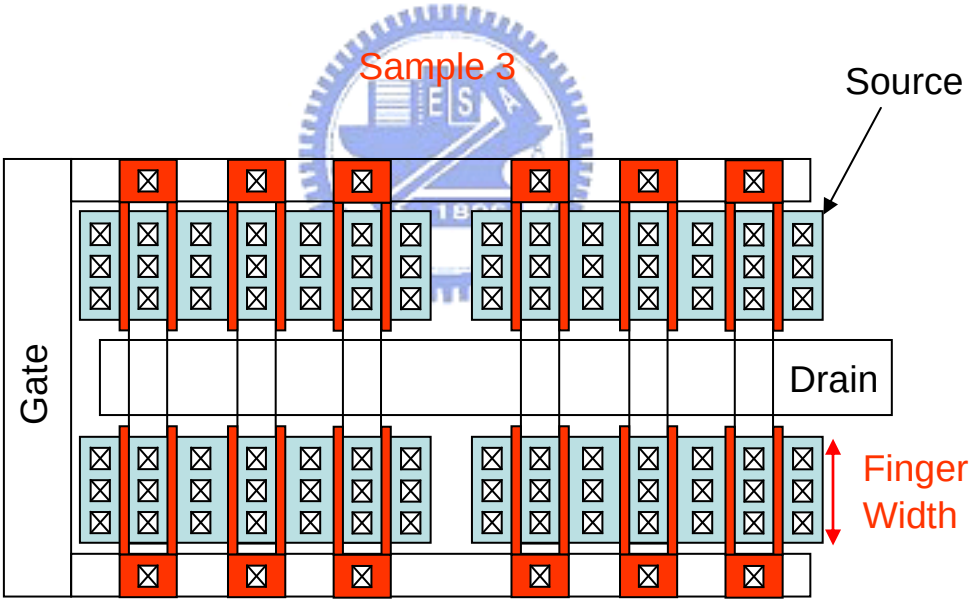


Fig. 2.2 Schematic cross section of an LDMOS transistor.



Total channel width=120 μ m

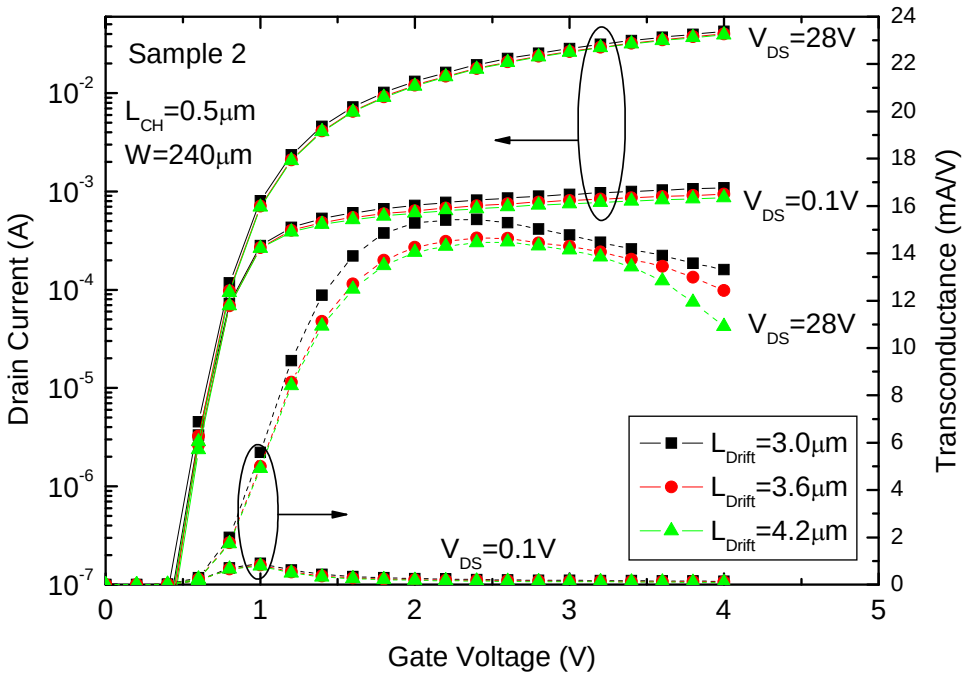
(a)



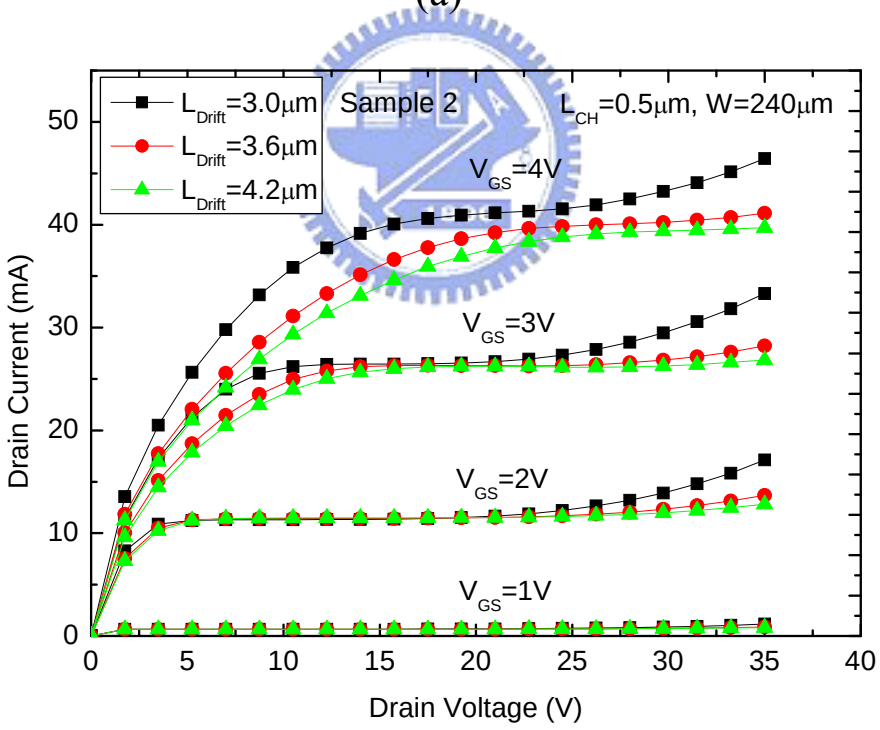
Total channel width=240 μ m

(b)

Fig. 2.3 Fishbone layout structures: (a) Sample 1 and (b) Sample 3.

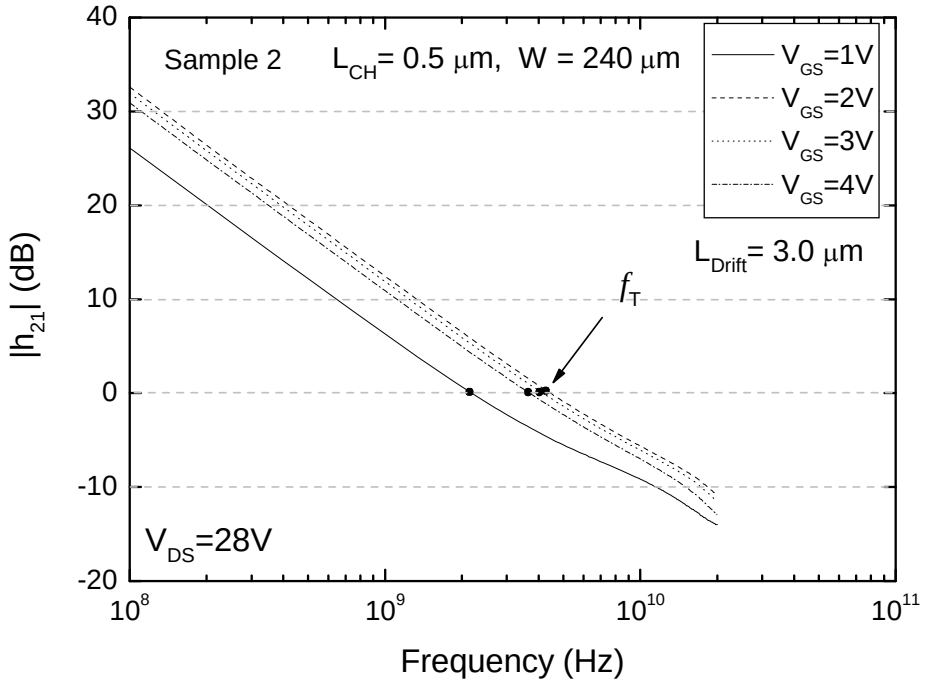


(a)

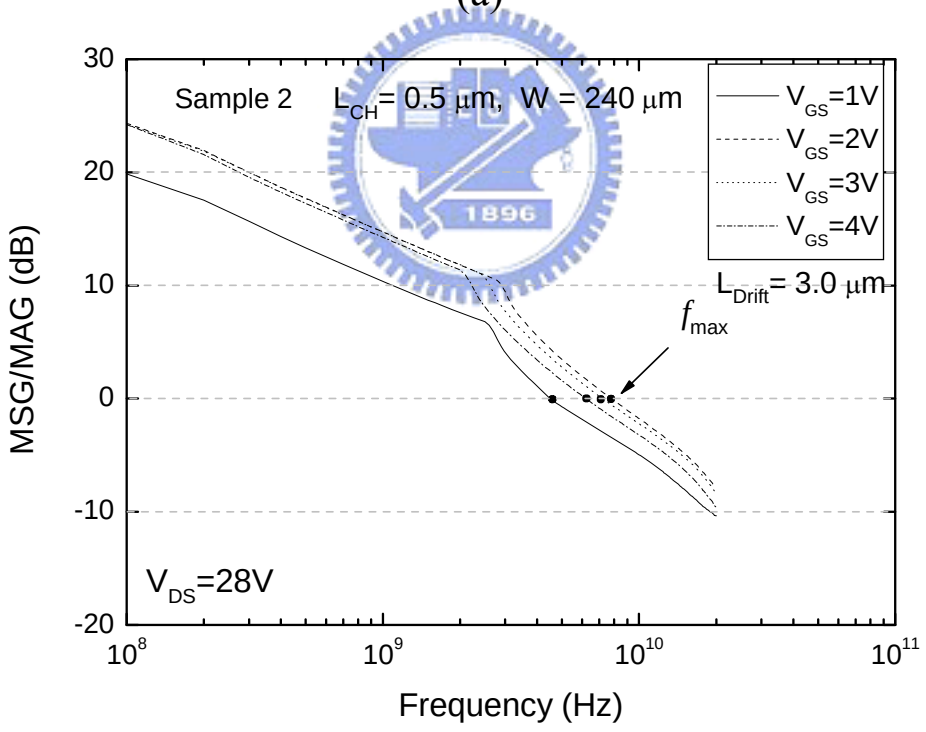


(b)

Fig. 2.4 (a) Subthreshold and (b) output characteristics of LDMOS transistors with different drift lengths.



(a)



(b)

Fig. 2.5 Dependence of (a) |h21| and (b) MSG/MAG on frequency obtained from S-parameter measurements.

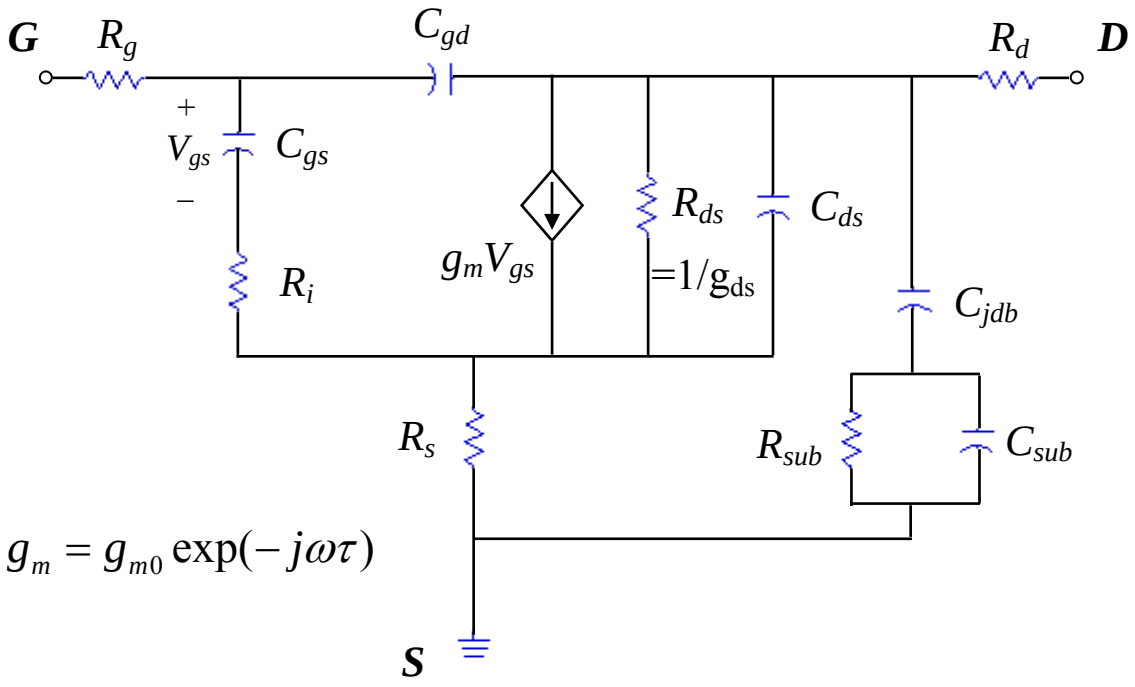


Fig. 2.6 A simple equivalent circuit model of the LDMOS.

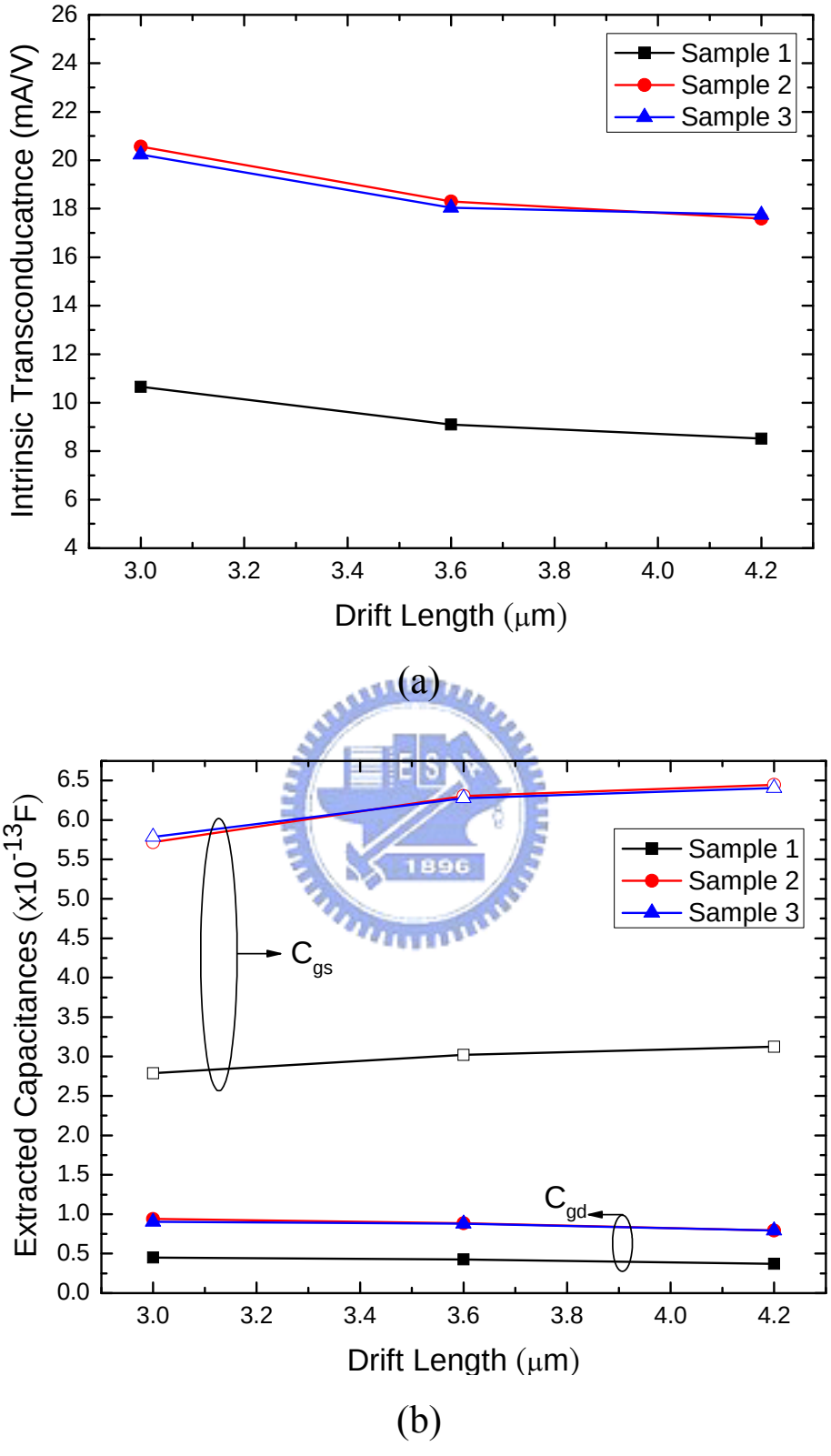
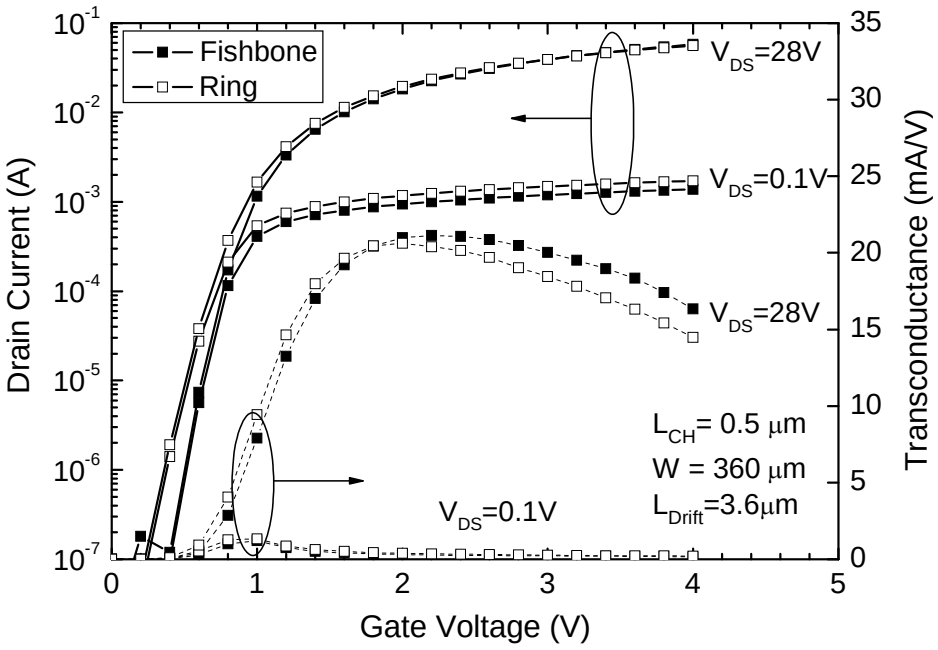
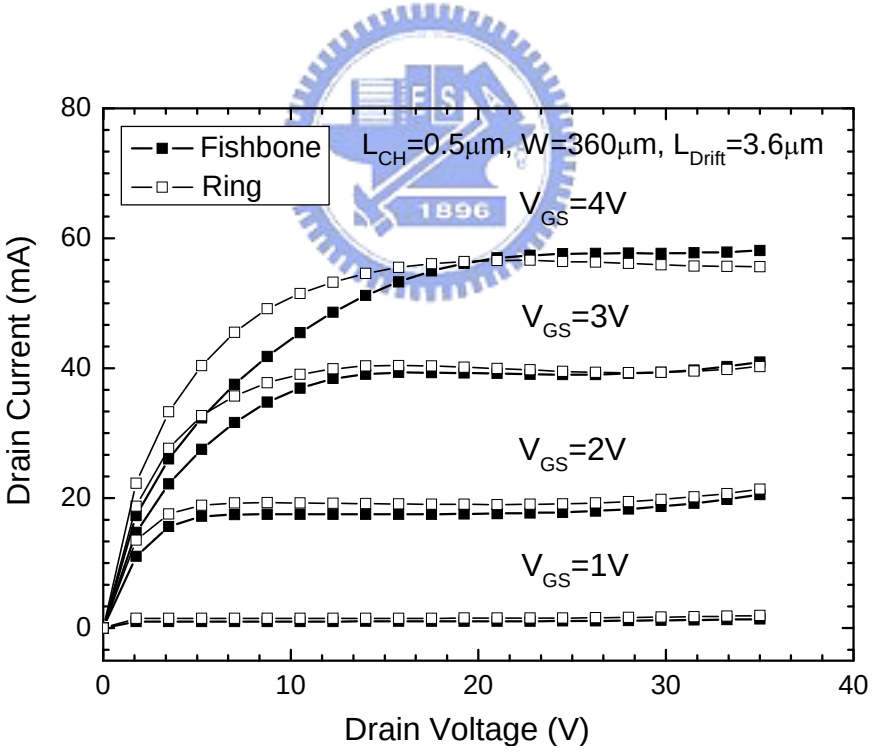


Fig. 2.7 (a) Intrinsic transconductance and (b) C_{gs} and C_{gd} versus drift length with different samples.



(a)



(b)

Fig. 2.8 (a) Subthreshold and (b) output characteristics of LDMOS transistors with different layout structures.

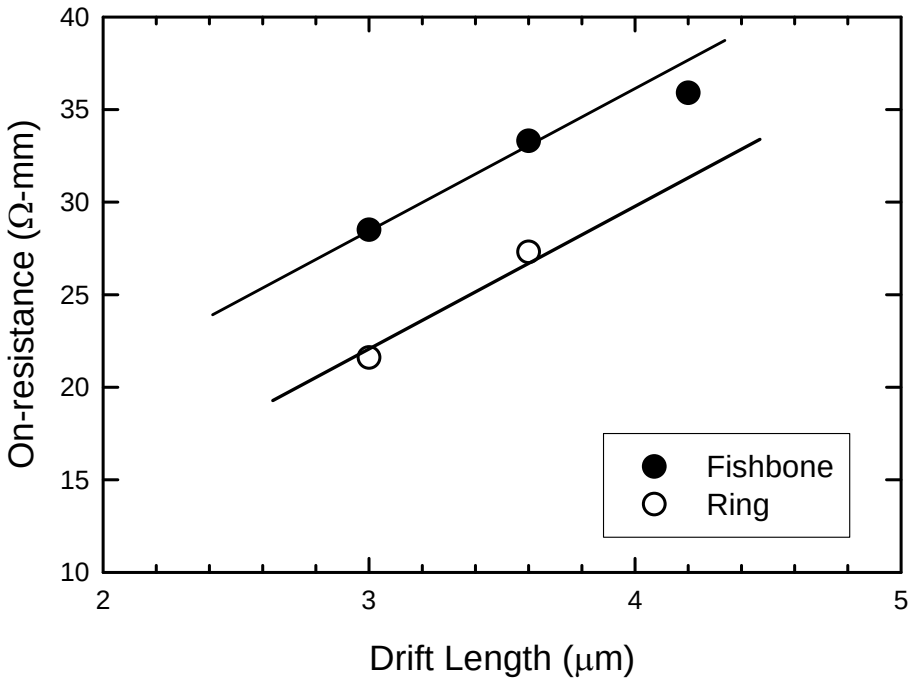


Fig. 2.9 R_{on} versus L_{Drift} for different layout structures.

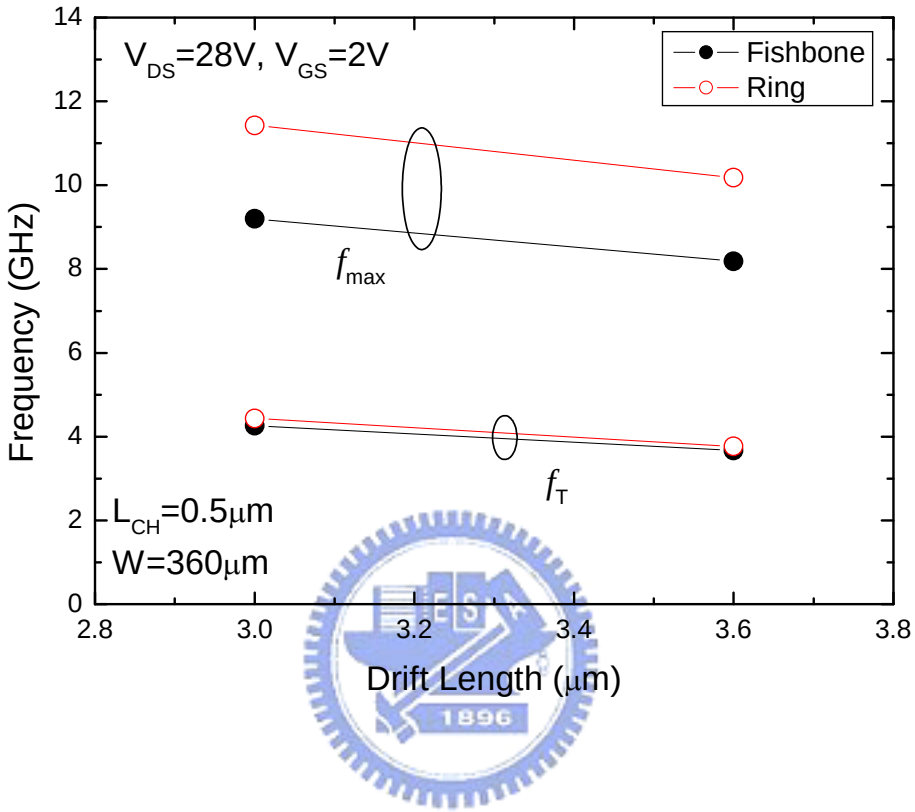


Fig. 2.10 Cut-off frequency and maximum oscillation frequency versus the drift length.

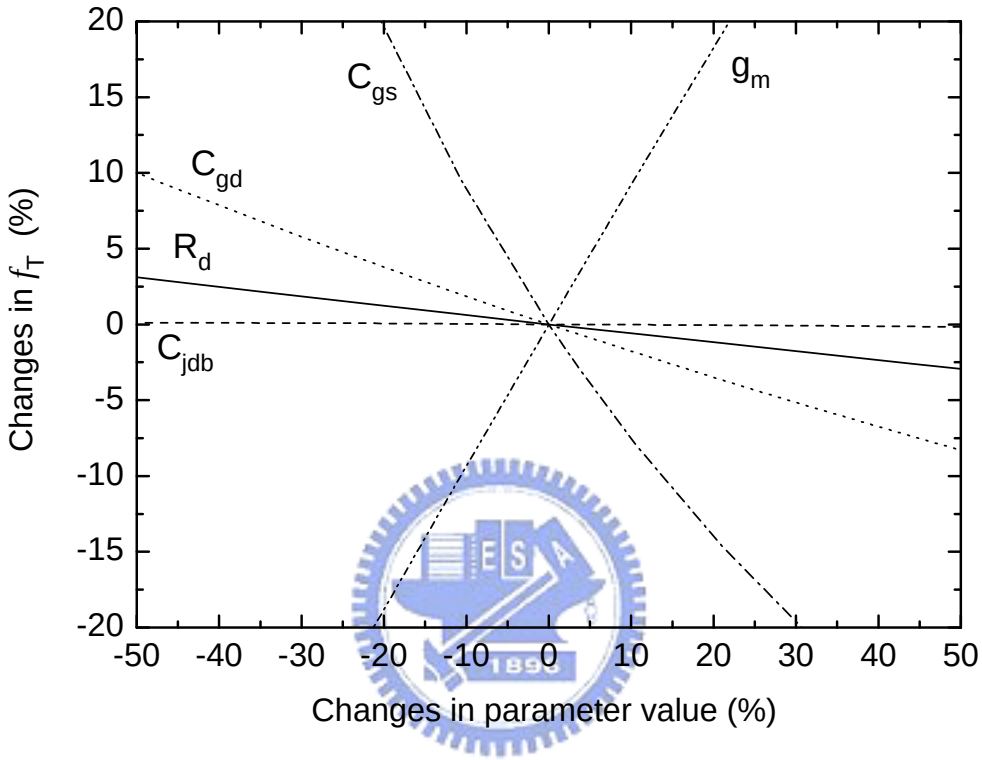


Fig. 2.11 (a) Effects of small-signal model parameters on f_T.

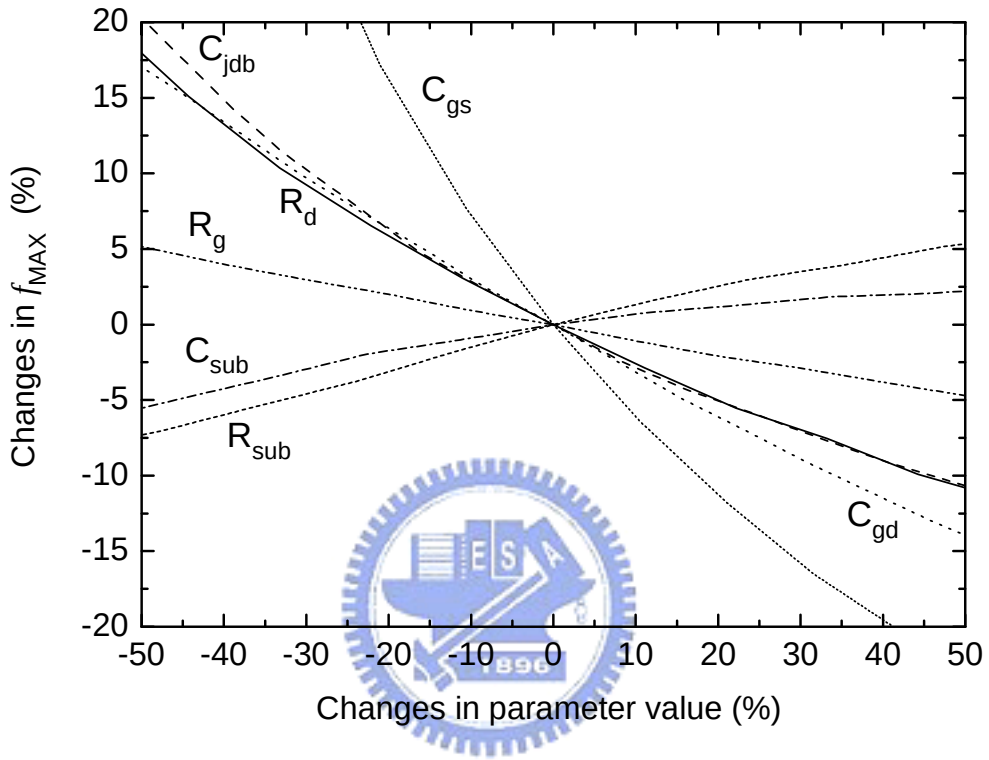


Fig. 2.11 (b) Effects of small-signal model parameters on f_{max}.

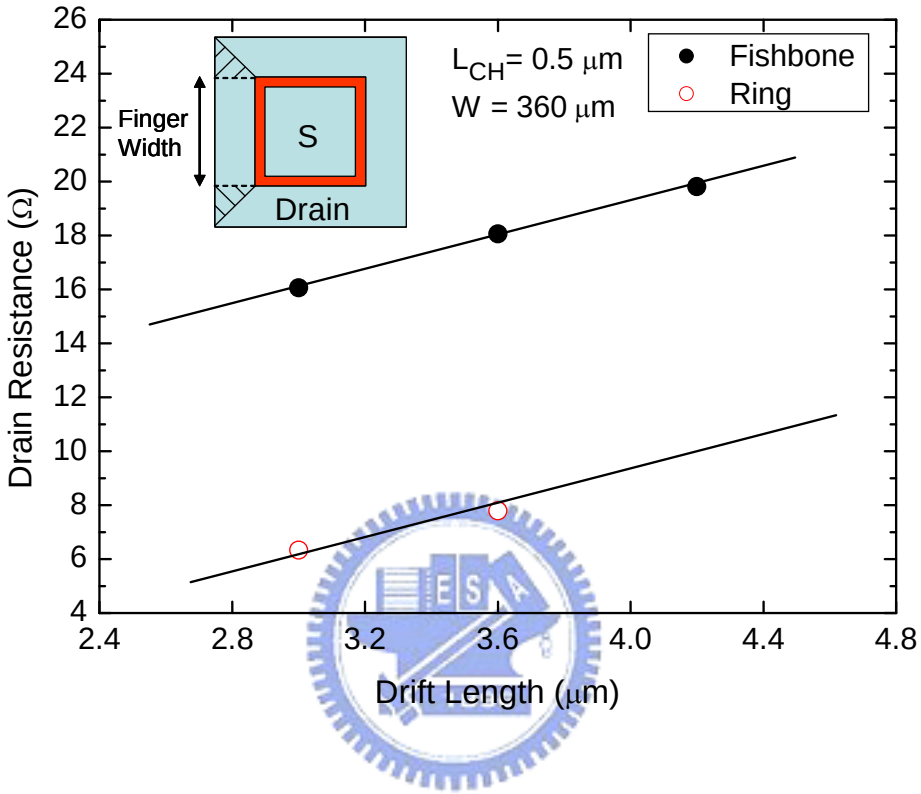


Fig. 2.12 R_d versus L_{Drift} for LDMOS with different layout structures. The inset shows that the drain region of the ring structure had extra areas (the shaded regions) compared with the fishbone structure.

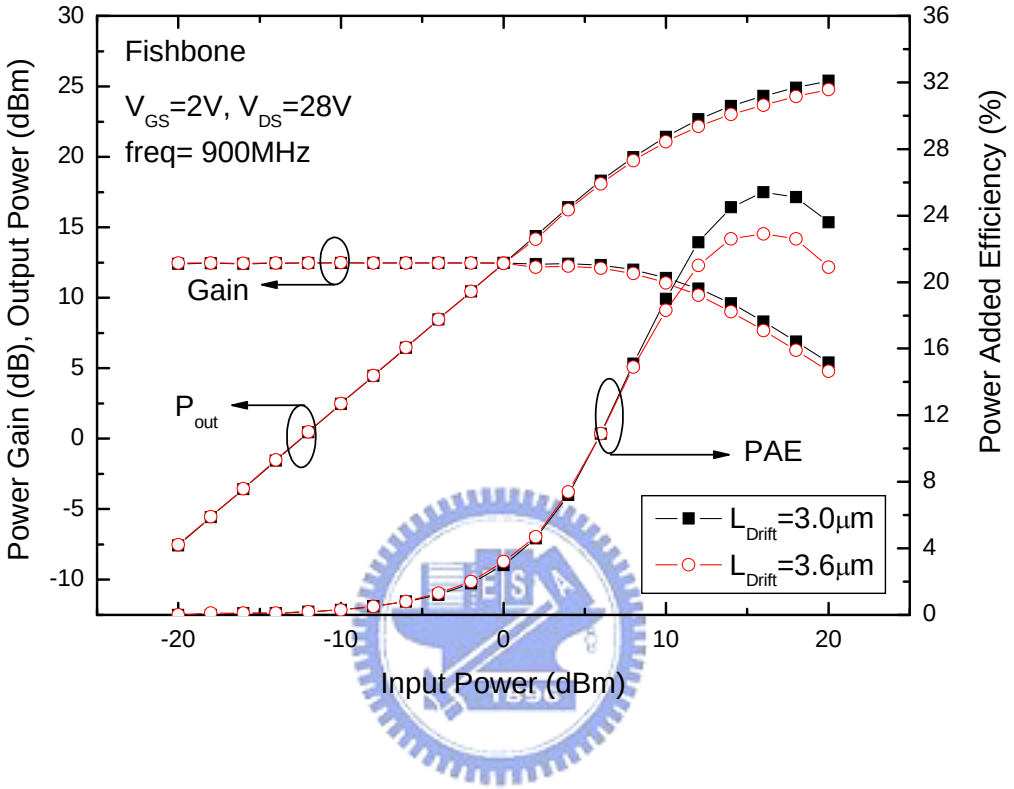


Fig. 2.13 Output power, power gain and PAE versus input power with different drift lengths.

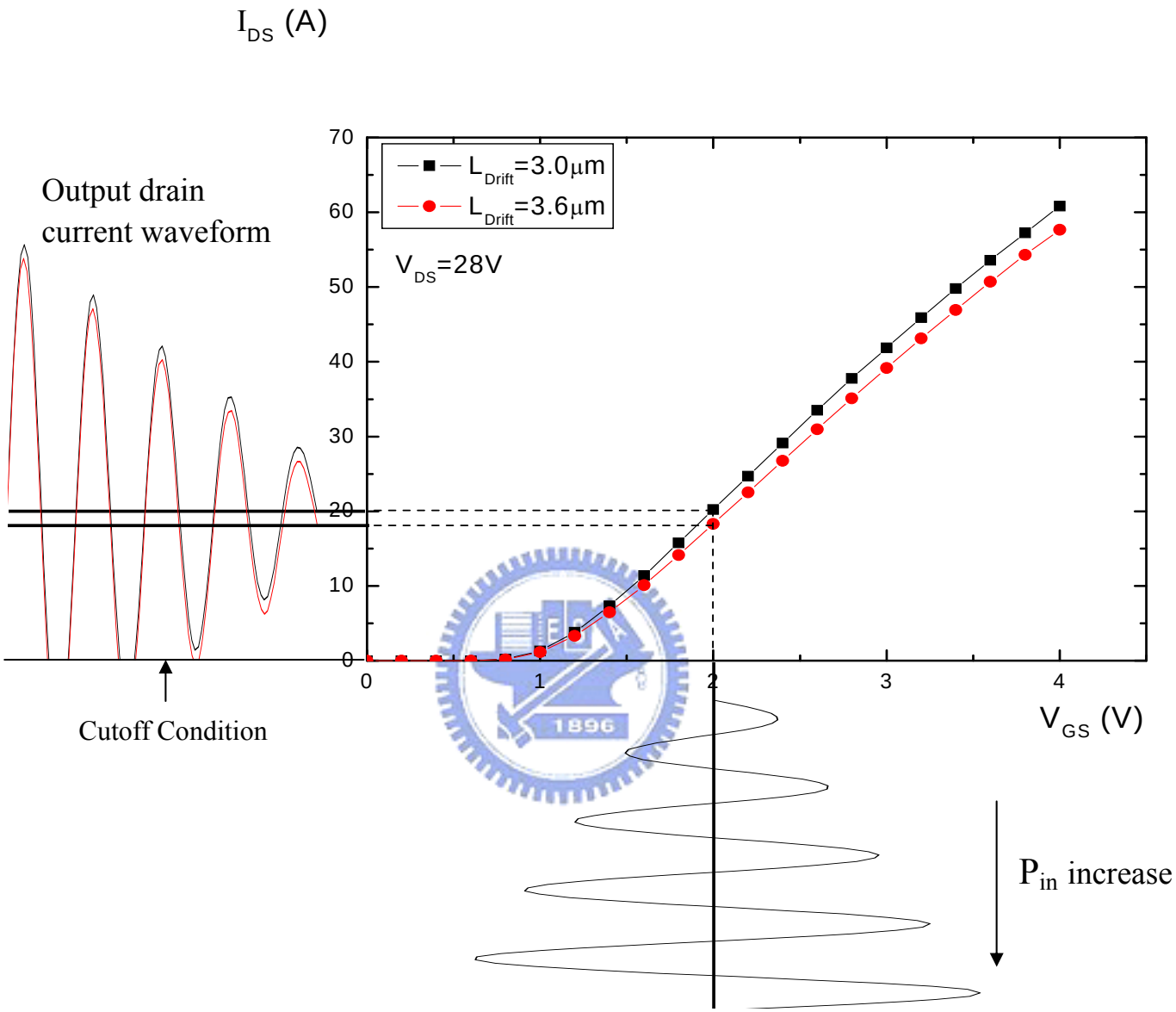


Fig. 2.14 Drain current versus gate voltage with different drift lengths. The input signal was bias at V_{GS}=2V and the negative duty cycle of output signal was clipped by the cutoff region.

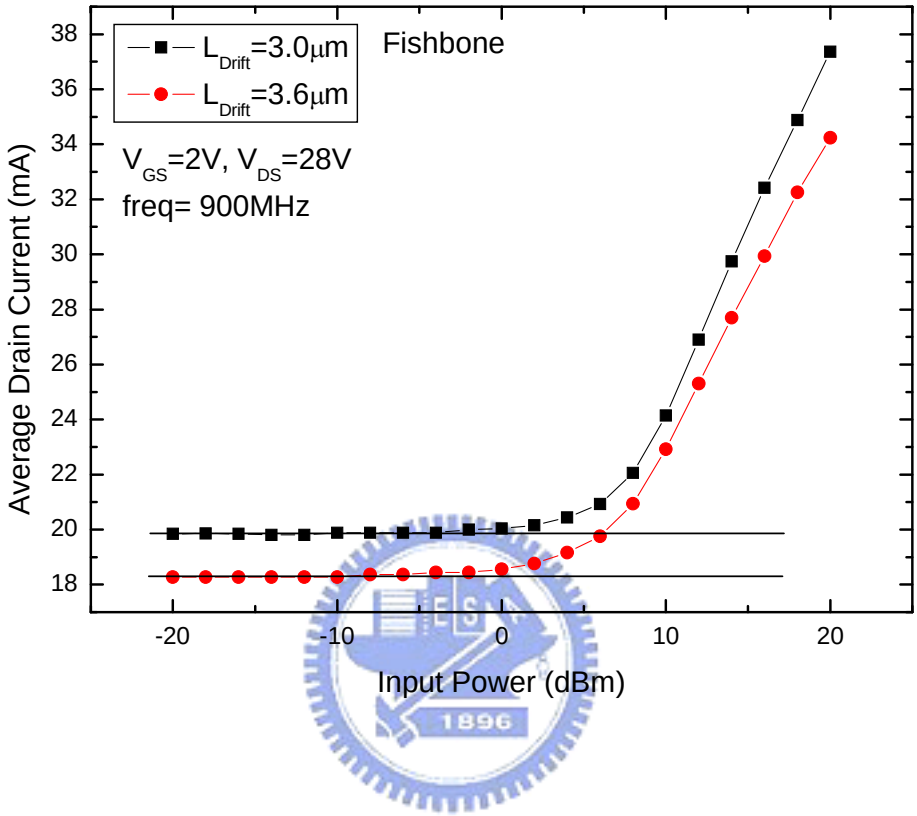


Fig. 2.15 Average drain current as a function of the input power with different drift lengths.

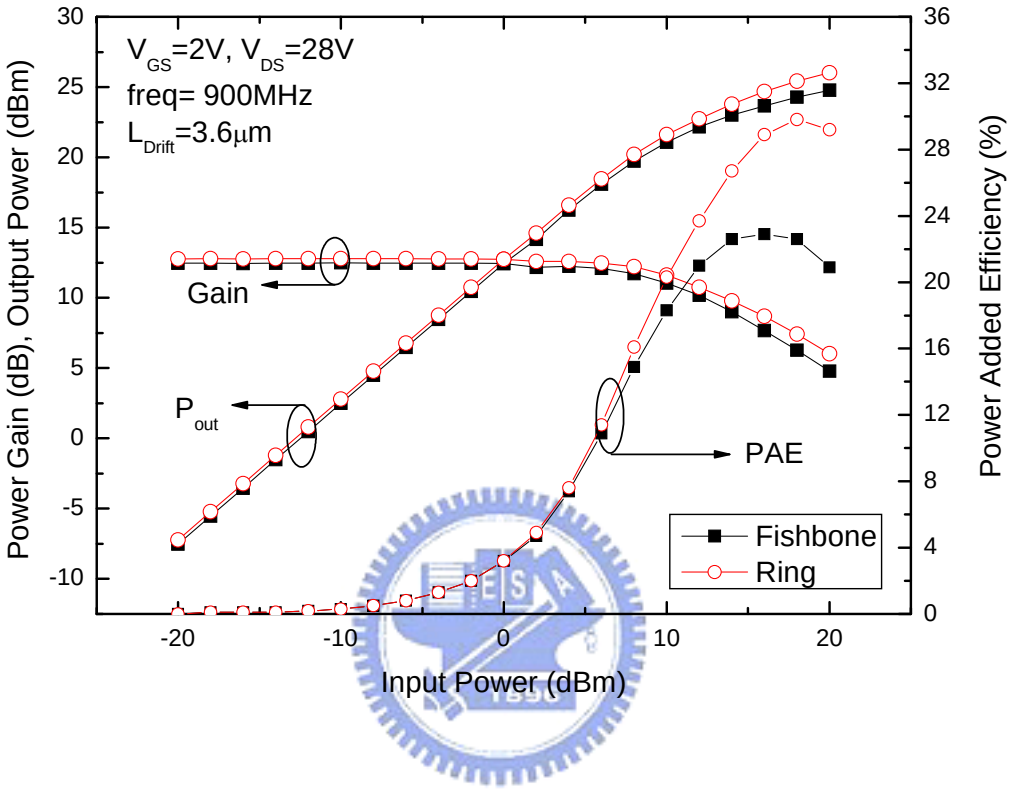


Fig. 2.16 Output power, power gain and PAE versus input power with different layout structures.

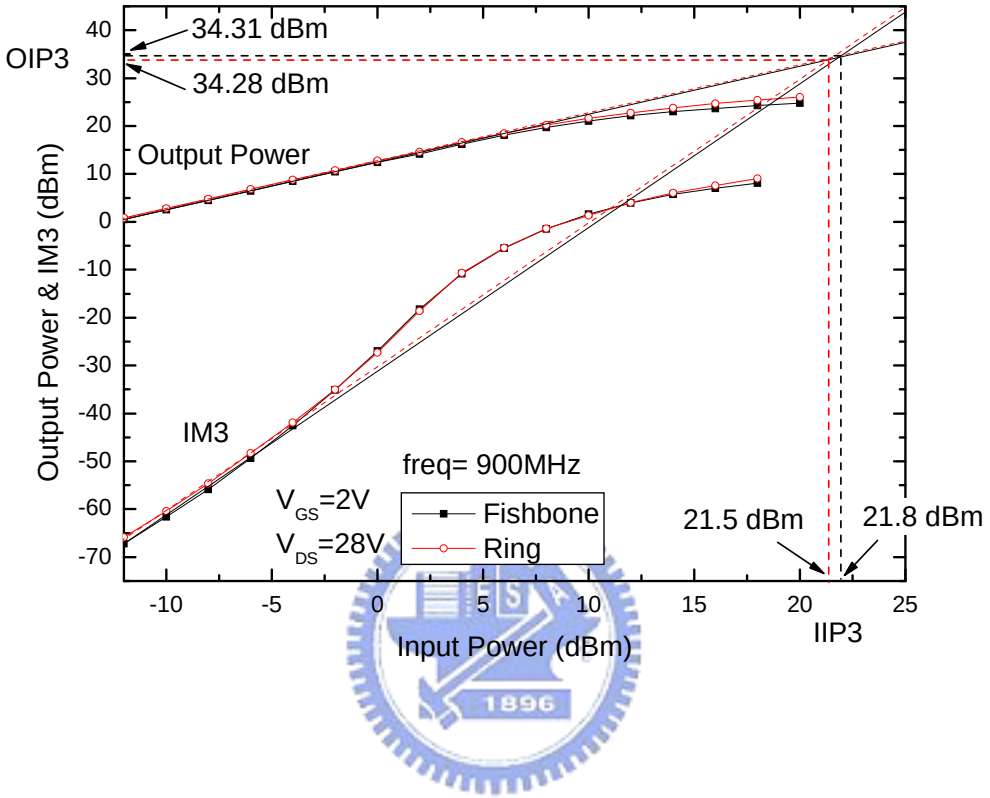


Fig. 2.17 Output power and third-order intermodulation power versus input power with different layout structures.

Chapter 3

Thermal Effects on DC and RF Performances of RF LDMOS

3.1 Introduction

For high-power applications, temperature is an important issue. The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are critical figures of merit for evaluating the performance of RF transistors. For conventional MOS transistors in RF applications, the temperature effect was investigated by studying the temperature dependence of f_T, which is proportional to the transconductance [1]. With an increase in temperature, the f_T and f_{max} have been shown to decrease. According to its structure, the parasitic drain resistance of the LDMOS becomes more important than that of the conventional MOSFET for the present drift region. However, in most of the studies, the effect of the parasitic resistance was not considered when analyzing the temperature effect on the device characteristics [1-3]. By de-embedding the effect of the parasitic source and drain resistors from the measured S-parameters, the temperature dependence of the intrinsic f_T can be analyzed. Several researchers have investigated the effects of temperature on the reliability and dc performances of LDMOS transistors [4-6]. However, the temperature effects on the high-frequency characteristics of LDMOS have seldom been addressed.

In this chapter, the DC and high-frequency characteristics of LDMOS transistors with different layout structures were studied at various temperatures. To study the self-heating effect, the pulsed current-voltage (I-V) and RF characteristics of LDMOS transistors are also discussed. The differences between the cw- and pulsed-mode measurements on drain current, cutoff frequency and maximum oscillation frequency are compared.

3.2 Characteristics of RF LDMOS at various Temperatures

3.2.1 DC Characteristics

The DC characteristics of the LDMOS transistor with different layout structures at 0 and 50°C are compared in Fig. 3.1. At low gate voltages (V_{GS}<1 V), the transconductance (g_m) and drain current at 50°C were higher those that at 0°C owing to the decrease in the threshold voltage. At high gate voltages, because the channel mobility decreased with increasing temperature, the g_m and drain current at 50°C became lower than that at 0°C. In low- and medium-bias regions, the ring structure showed a higher drain current and g_m than the fishbone structure. For a high drain bias (V_{DS}=28 V), the drain current and extrinsic g_m had zero-temperature-coefficient biases near V_{GS}=1.3 V and V_{GS}=1 V, respectively. The zero-temperature-coefficient bias point results from the negative temperature coefficients of both the effective mobility and threshold voltage [5].

Figure 3.2 shows the threshold voltage plotted against temperature. The threshold voltage variations were -1.66 and -1.68 mV/^{0}C for the fishbone and ring structures, respectively. The values in the literature varied from −1 to −4 mV/K with the most frequently noted value of −2 mV/K for the conventional CMOS [7]. For the LDMOS transistors, the threshold voltage variation in our study was smaller than the proposed values of -5.2 mV/^{0}C [5], -3.2 mV/K [8], and -2.8 mV/^{0}C [9]. This results from the lighter doping in the double-diffused channel.

The extracted channel mobility for different temperatures is shown in Fig. 3.3. The LDMOS channel mobility was deducted from the first-order one-dimensional model in the linear mode [5]:

$$\frac{\partial I_d}{\partial V_d} = \mu_{eff}(T)\frac{W}{L}C_{ox}(V_g - V_{th}(T))$$

This method is applicable for low drain voltages. The temperature dependence of the channel mobility can be modeled as $\mu = \mu_0 * (T/T_0)^{-m}$, where m=1.35 for the fishbone structure and 1.36 for the ring structure. For intermediate inversion layer concentrations (N=0.5-5×10^{12}

cm^{-3}) at room temperature, the phonon-scattering-limited channel mobility has been observed to be dependent on N and T ($\mu_{ph} \propto T^{-n} N^{-1/\gamma}$), where γ=3-6 and n=1-1.5 [10]. Therefore, the mobility in our devices was dominated by the phonon scattering.

3.2.2 High-frequency Performance

The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) versus the gate voltage for the LDMOS transistors at various temperatures are shown in Fig. 3.4. The ring structure had better high-frequency performance than the fishbone structure owing to a lower drain resistance [11]. In addition, both f_T and f_{max} decreased with increasing temperature for the two structures. The degradations of f_T and f_{max} were attributed to the lower g_m, as shown in Fig. 3.5. The variations in f_T and intrinsic g_m were 17 and 20%, respectively at V_{GS}=2 V, as temperature changes from -25 to 50°C. Because the temperature dependence of f_{max} was also affected by the drain resistance (R_d) and drain-substrate junction capacitance (C_{jdb}), the variation in f_{max} was approximately 15%. It should be noted that the f_T and g_m had zero-temperature-coefficient bias points near V_{GS}=1 V. In Fig. 3.5, at a higher gate voltage, both the intrinsic and extrinsic g_m values of the ring structure were lower than those of the fishbone structure owing to the self-heating effect. Owing to the series resistance, the intrinsic g_m for the two structures was higher than the extrinsic g_m. The variation in both the intrinsic and extrinsic g_m values were approximately 20% at V_{GS}=2 V as temperature changes from -25 to 50°C. However, the variation changed to 17% for the fishbone structure and 15% for the ring structure at a high gate voltage (V_{GS}=4 V). The higher gate voltage leaded to severe surface scattering and lowers the effective mobility. As the gate voltage increased, the effect of surface scattering was more prominent resulting in smaller changes in g_m and also in f_T and f_{max} with temperature.

Figure 3.6 shows the variations in extrinsic and intrinsic f_T values versus the variation in

intrinsic g_m at V_{GS}=2 V when temperature changes from 25°C. The usual approximate relation of extrinsic f_T and intrinsic g_m can be expressed as follows [12]:

$$f_T = \frac{g'_{m0}}{2\pi\sqrt{(C'_{gs}+C'_{gd})^2(1+\frac{r_d}{R'_{ds}\,||\,R_{sub}})^2-(g'_{m0}C'_{gs}R'_{gs}-C'_{gd})^2}} \quad (1)$$

where $g'_{m0} = g_{m0}/(1+g_{m0}R_s)$. The extrinsic f_T in eq. (1) was extrapolated assuming a -20 dB/decade roll-off for the short-circuit current gain $|h_{21}|$. R_{gs} refers to the channel resistance and leads to an additional term related to the g_m in the denominator. The sign of this term in the denominator was negative, making the slope of the extrinsic f_T variation versus the intrinsic g_m variation larger than 1. This was contradictory to our measured results in Fig. 3.6(a). Moreover, in eq. (1), the small-signal equivalent circuit can be viewed as a dual-feedback circuit in which R_s is the local series-series feedback element and C_{gd} is the local shunt-shunt feedback element [12]. Even though R_s makes the extrinsic g_m smaller than the intrinsic g_m by a factor of 1/(1 + g_m R_s), it also decreased C_{gs} and C_{gd} by the same factor and thus should not affect f_T.

In LDMOS, however, the effect of drain parasitic resistance was also important, which was ignored in eq. (1). Tasker and Hughes reported a more rigorous derivation for short-circuit current gain of a FET that takes source and drain resistance into account [13]:

$$f_T = \frac{g_m}{2\pi\left\{(C_{gs}+C_{gd})\cdot\left[1+(R_S+R_d)/R_{ds}\right]+C_{gd}\cdot g_m\cdot(R_S+R_d)\right\}} \quad (2)$$

According to eq. (2), the sign of the term related to the g_m in the denominator was positive, making the slope of the f_T variation versus the intrinsic g_m variation smaller than 1. In Fig. 3.6(a), the extrinsic f_T included the effects of source and drain resistances and the values of the curve slope were smaller than 1. This might be attributed to the effect of (R_s+R_d) being more prominent than the effect of R_{gs}. Furthermore, the fishbone and ring structures we studied here had difference drain resistances, resulting in the distinct values of the curve slopes in Fig. 3.6(a). To eliminate the effect of parasitic resistance, the intrinsic f_T was

extrapolated after de-embedding the effect of the parasitic resistors from the measured S-parameters. As shown in Fig. 3.6(b), the curve slopes of the intrinsic f_T variation versus the intrinsic g_m variation for the fishbone and ring structures are quite similar (0.95 for fishbone and 0.94 for ring) and approach 1.

Figure 3.7 shows the variation in extrinsic and intrinsic f_{max} versus the variation in the intrinsic g_m at V_{GS}=2V when temperature changes from 25°C. The approximate relation of the extrinsic f_{max} and intrinsic g_m can be expressed as follows [14]:

$$f_{\max} \sim \frac{f_T}{\sqrt{4g_{DS}R_g + 8\pi f_T C_{gd}(R_g + \alpha R_d)}} \tag{3}$$

The intrinsic g_m dependence of f_{max} comes about through the f_T we mentioned above. The positive relation of f_T in the denominator results in a lower value for the curve slope in Fig. 3.7(a) than that in Fig. 3.6(a). After de-embedding the effect of the parasitic resistors from the measured S-parameters, the curve slopes of the intrinsic f_T variation versus the intrinsic g_m variation for the fishbone and ring structures are quite similar (0.704 for fishbone and 0.709 for ring which shown in 3.7(b)). In addition, the parasitic drain resistance in the denominator indicates that the R_d had a larger effect on f_{max}. Therefore, the ring structure, which had a lower drain parasitic resistance, showed more improvement on f_{max} than f_T.

3.2.3 S-parameters Characteristics

Figure 3.8 shows the measured and simulated S-parameters of the fishbone and ring structures at various temperatures. The transistors were measured at V_{GS}=2 V and a drain voltage (V_{DS}) of 28V for the maximum value of f_T. In order to demonstrate the temperature dependence of the S-parameters, the model parameters of the small-signal equivalent circuit of the LDMOS transistors were extracted. The simulated results are also shown in Fig. 3.8. As illustrated in Fig. 3.8, the deviation of S11 with temperature was not marked. This suggests that the input impedance was affected by temperature slightly. Because the g_m decreases with

increasing temperature, both S21 and S22 change significantly. At low frequencies, S21 can be approximated by [15]

$$S_{21} = -2 \cdot g_m^{'} \cdot R_L \cdot \frac{Z_O}{Z_O + R_d} \tag{4}$$

where Z_O=50Ω and R_L=R_{DS}‖(R_d+ Z_O). It is proportional to g_m. However, at low frequencies, $S_{12} = 2 \cdot sC_{gd}^{'} \cdot Z_O$ is only related to the gate-to-drain capacitance (C_{gd}). Therefore, S21 changed significantly owing to the decrease in g_m, and S12 showed minor changes owing to the slight variation in C_{gd} with increasing temperature. It is interesting that the temperature-induced variation in S22 in the ring structure is lower than that in the fishbone structure. Figure 3.9 shows the measured and simulated results of |S22| for the fishbone and ring structures. The extracted R_d and C_{jdb} of the ring structure were 7.8Ω and 149fF, respectively, which were lower than those of the fishbone structure (the extracted R_d and C_{jdb} are 18Ωand 244 fF, respectively) [11]. This is a possible reason for the lower S22 variation in the ring structure with different temperatures.

3.3 Pulsed I-V/RF Characteristics of RF LDMOS

To study the self-heating effect on the performance of an LDMOS, we measured its I-V and RF characteristics under a pulsed condition. Figure 3.10 shows the timing diagram of the pulsing sequence. The quiescent biases for gate and drain were set to 0. The typical duration of the pulses for such measurements was 5 μs with a period of 1 ms. These values allow the devices to cool sufficiently during the off time of the pulse period. The measured data was sampled for a short delay time (t_p=1.5 μs) to eliminate the self-heating effect. Figure 3.11 shows typical output characteristics of an LDMOS under static- and pulsed-mode measurements. At low gate voltages (V_{GS}<2 V), the measured static current of the LDMOS was similar to the pulsed current. However, the measured static current was lower than the pulsed current at high gate voltages due to higher thermal heating in the steady state. In an

LDMOS, the channel temperature rises because of the power dissipation, and the carrier phonon scattering rate increases, which degrades the carrier mobility [16]. At high gate biases, the self-heating effect was shown to be significant due to increased power dissipation. In the saturation region, the channel length modulation and the impact ionization at high drain biases were also compensated by the self-heating effect. In the pulsed-mode operation, the self-heating effect was eliminated by the short pulse measurement with a low duty cycle.

Figure 3.12 shows the output characteristics of LDMOS transistors with different layout structures under the pulsed condition. Unlike the results in Fig. 2.8(b), without the self-heating effect, we found that the drain current of the ring structure was higher than that of the fishbone structure under all bias conditions. This suggests that the ring structure has better performance than the fishbone structure, when the transistors are used in pulsed-mode power amplifier applications.

The influence of the self-heating effect on high-frequency characteristics was investigated by pulsed RF measurement. The dependences of the cutoff frequency and maximum oscillation frequency on the gate voltage under cw and pulsed conditions wee shown in Fig. 3.13. The drain voltage was 28 V. At low gate voltages, the influence of device self-heating was minor. This resulted in approximately equal values under cw and pulsed conditions. As the gate voltage increased, the self-heating effect became more prominent, leading to larger difference between the measured values under cw and pulsed conditions. It was observed that the self-heating effect had a noticeable impact on RF performance. The degradation of RF performance by the self-heating effect was due to the decrease in transconductance, which depends directly on the temperature-dependent carrier mobility [17]. f_T and f_{max} under the pulsed condition were improved by eliminating the self-heating effect. In Fig. 3.13, the ring structure also showed a greater difference in measured results between cw and pulsed conditions than the fishbone structure. This indicated that the self-heating effect was more significant in an LDMOS with a ring structure.

By using the pulse measurement system, the thermal resistance (R_{TH}) and thermal capacitance (C_{TH}) can also be obtained for fishbone and ring structures. Fixing the bias at V_{GS}=4 V and V_{DS}=28 V, R_{TH} was derived by estimating the power dissipation at intersect point of static (at 25°C) and pulsed IV curve (35°C -100°C) [18-19]. The temperature rise was proportional to the power dissipated in the device channel and the slope of this line was R_{TH}. The R_{TH} extracted by $T_C\ (Power) = 25 + R_{TH} \cdot Power$ is 64.81°C/W in the fishbone and 82.14°C/W in the ring (shown in Fig. 3.14) where T_C is the channel temperature. Figure 3.15 shows the thermal transient at room temperature which was measured from transient drain current using the formula:

$$\Delta T = \frac{I_D(t) - I_{Di}}{I_{DS} - I_{Di}} \cdot R_{TH} \cdot Power$$

where I_{Di} is the initial drain current and I_{DS} is the static drain current as shown in the inset of Fig. 3.15. C_{TH} then can be extracted by fitting the equation: $\Delta T = \Delta T_S \cdot [1 - e^{-\frac{Time}{R_{TH}C_{TH}}}]$ [20]. C_{TH} was 0.53 μJ/°C in the fishbone and 0.34 μJ/°C in the ring. Consequently, the ring structure had more self-heating.

3.4 Summary

The effects of temperature on the DC and high-frequency characteristics of RF LDMOS transistors were investigated in this chapter. The transconductance, threshold voltage, and channel mobility decrease with increasing temperature. The decrease in transconductance degrades the f_T and f_{max} at high temperatures. Owing to the higher drain resistance in the LDMOS transistors, the f_T is also affected by drain resistance. After de-embedding the effect of drain resistance, the temperature-induced f_T variation is almost proportional to the g_m variation. In addition, we found that the temperature dependence of f_{max} is also affected by the drain resistance and drain-substrate junction capacitance. The measured S-parameters at various temperatures were also discussed. Because the LDMOS transistors with the ring

structure have a lower drain resistance and a lower drain-substrate junction capacitance, the variation in S22 with temperature is smaller than that in the fishbone structure. Furthermore, the self-heating effect of LDMOS transistors was also investigated by measuring the pulsed current-voltage (I-V) and pulsed RF characteristics. Although the ring structure showed lower static drain current than the fishbone structure at high gate biases due to the significant self-heating effect, its current drive capability could be improved using a pulsed-mode operation.

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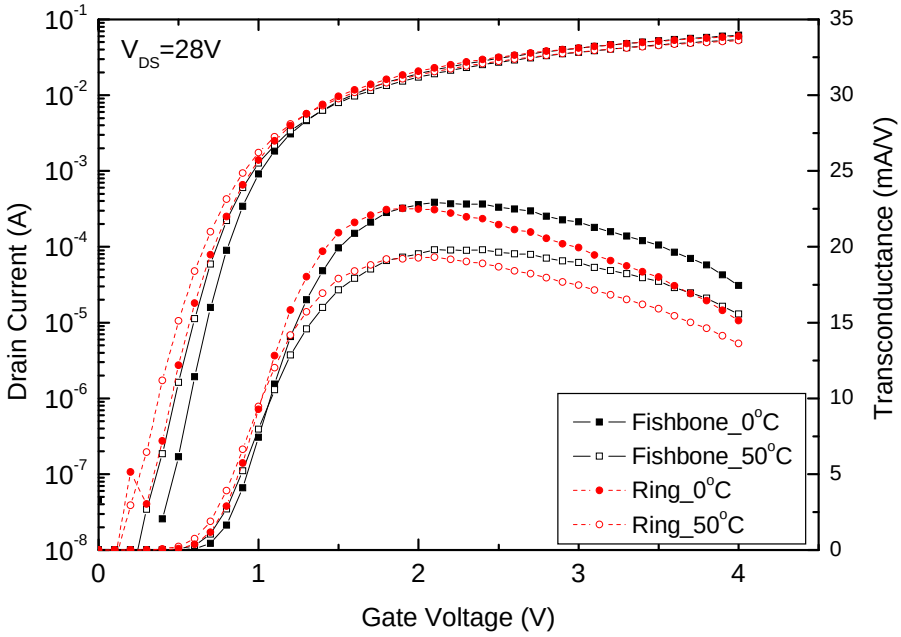
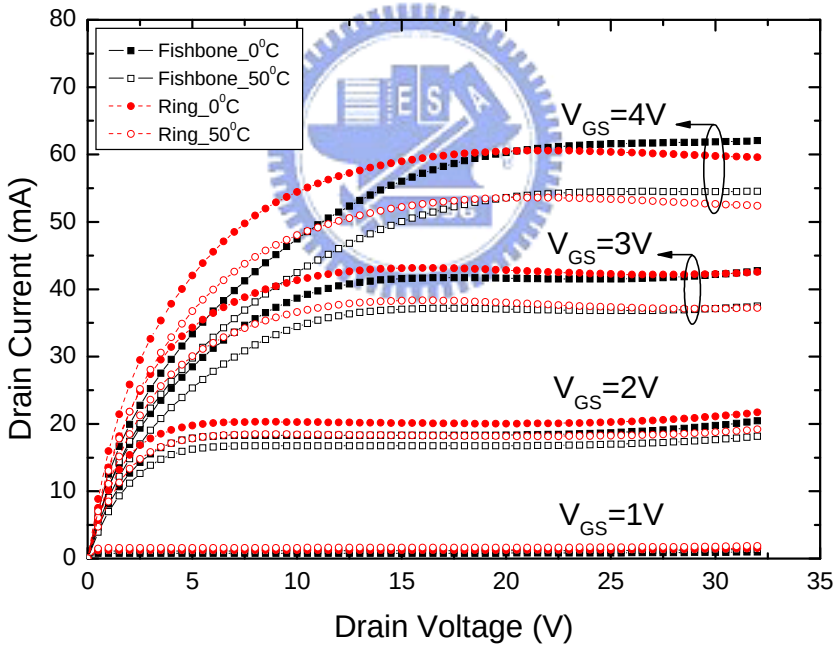


(a)



(b)

Fig. 3.1 (a) Subthreshold and (b) output characteristics of LDMOS transistors with different layout structures at 0 and 50°C.

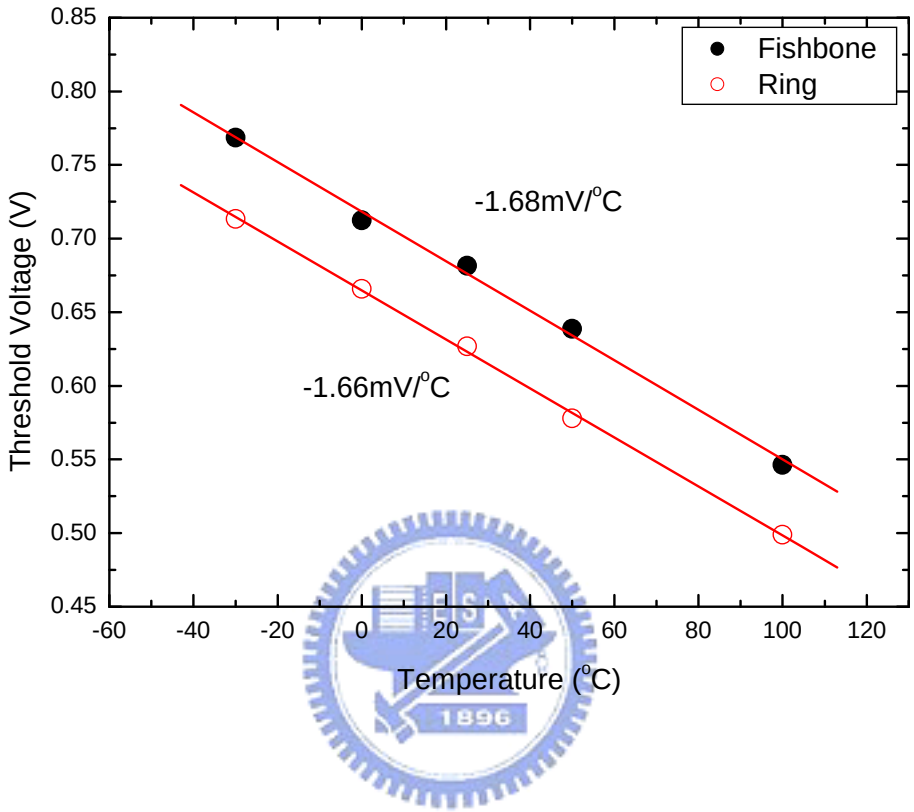


Fig. 3.2 Threshold voltage variation with temperature for different layout structures.

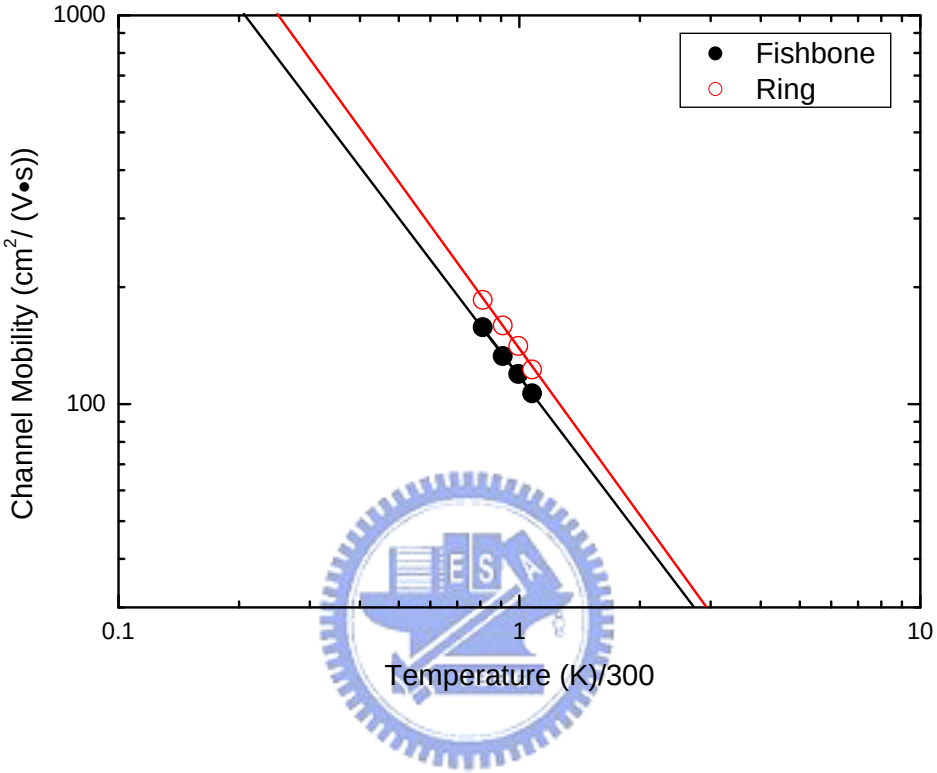


Fig. 3.3 Temperature dependence of channel mobility for different layout structures.

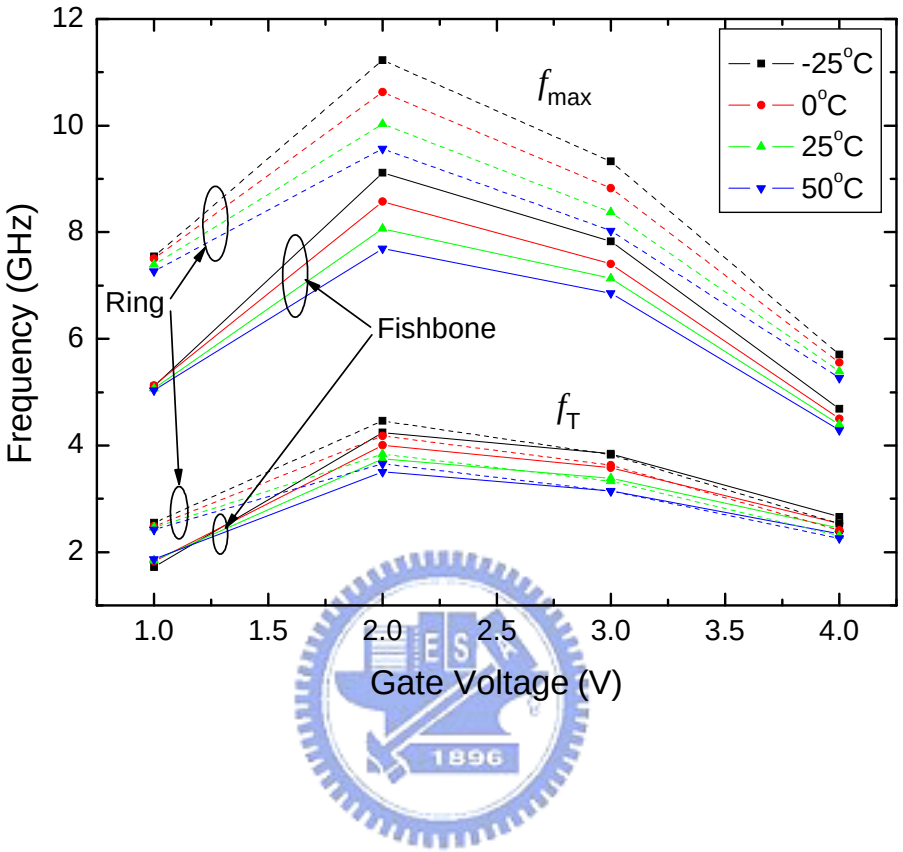


Fig. 3.4 Cutoff frequency and maximum oscillation frequency versus gate voltage at various temperatures.

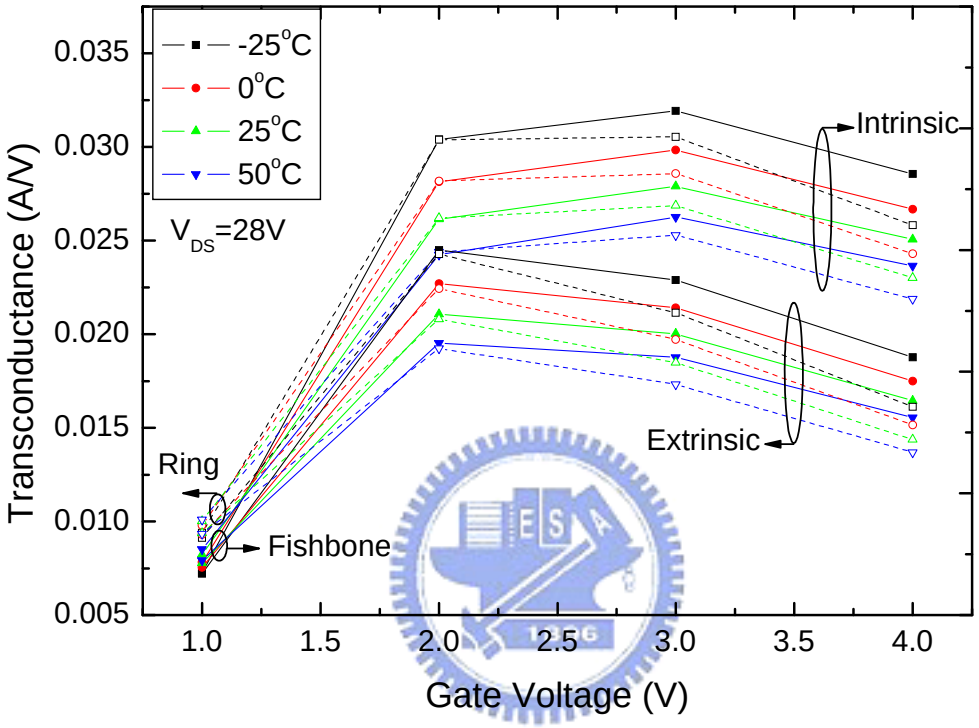
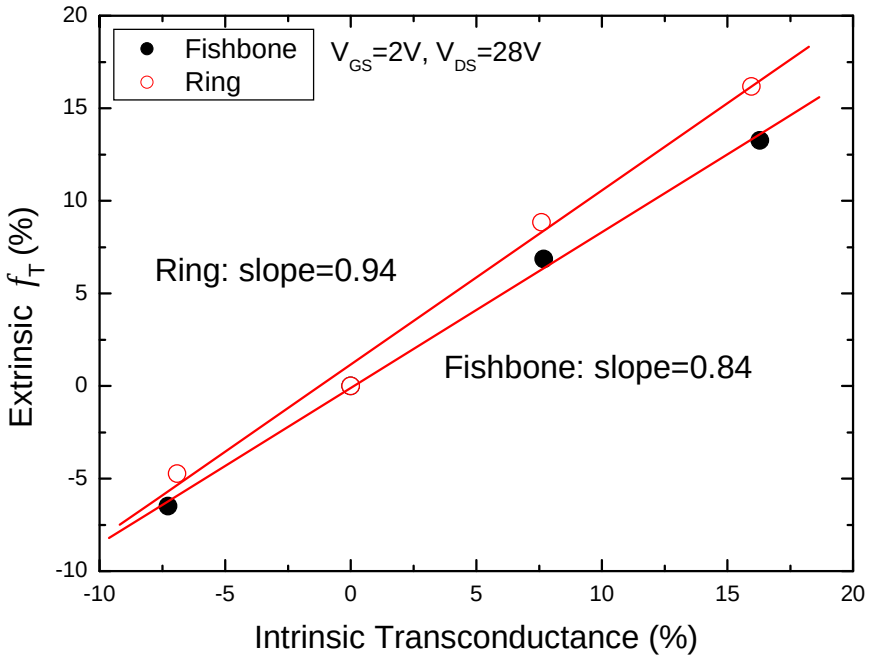
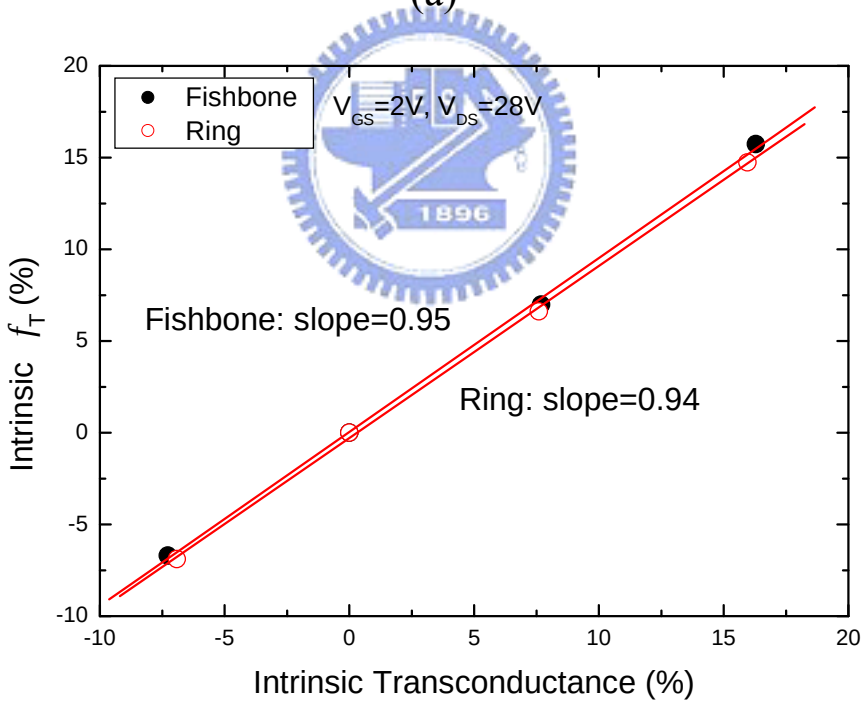


Fig. 3.5 Extrinsic and intrinsic transconductances versus gate voltage at various temperatures for different layout structures.

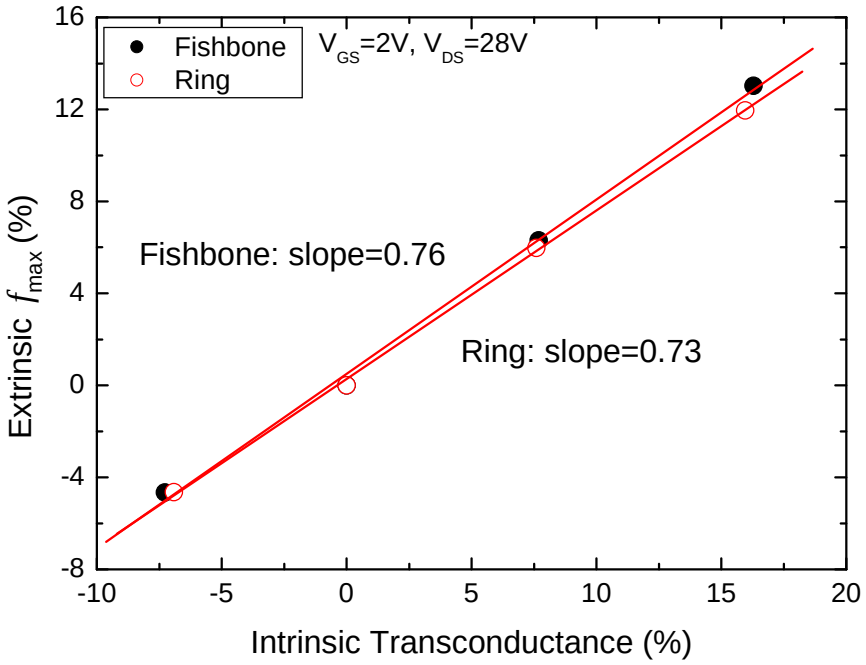


(a)

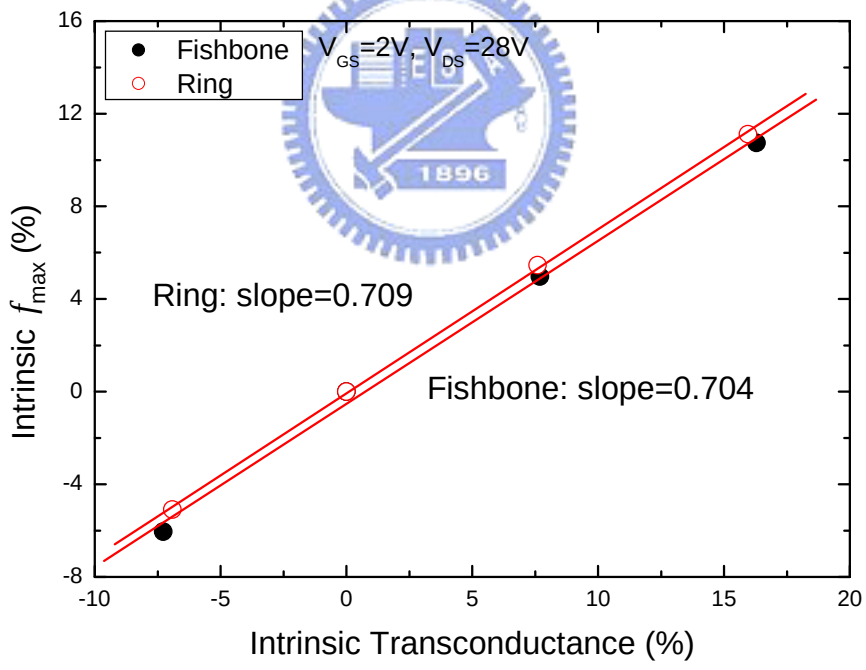


(b)

Fig. 3.6 (a) Extrinsic f_T and (b) intrinsic f_T variations versus intrinsic transconductance variation when temperature changes from 25°C.

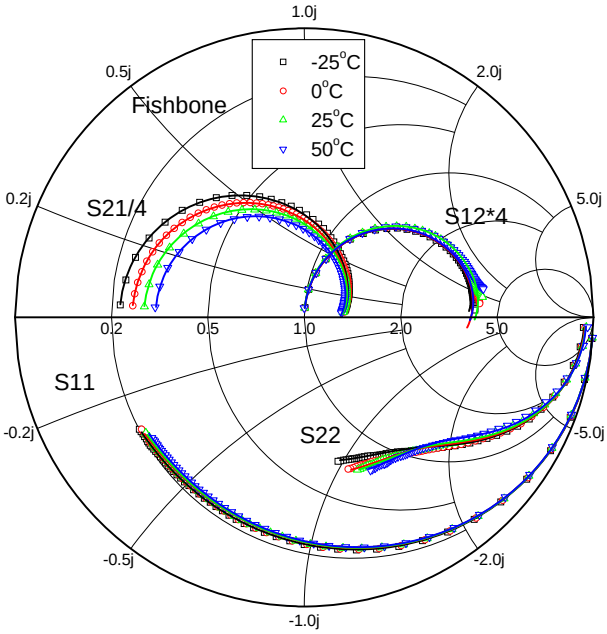


(a)

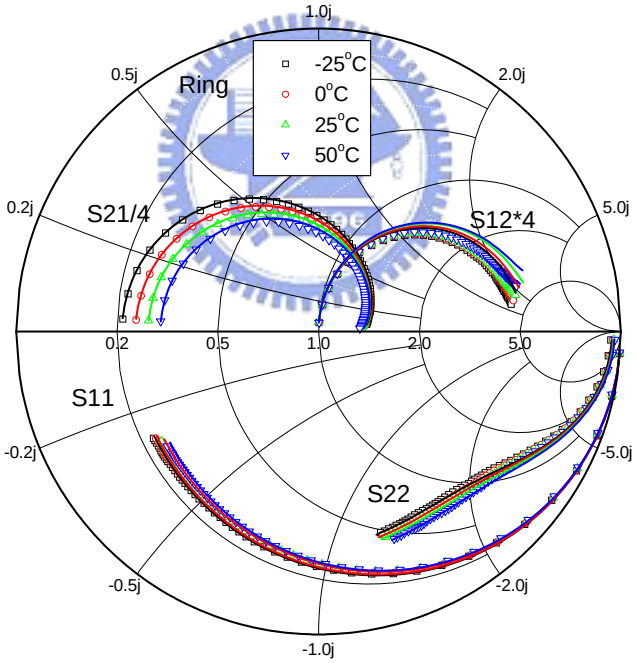


(b)

Fig. 3.7 Extrinsic f_{max} variation versus intrinsic transconductance variation when temperature changes from 25°C.



(a)



(b)

Fig. 3.8 Measured (open symbols) and simulated (solid line) S-parameters of transistors with (a) fishbone and (b) ring structures from 0.1 to 10 GHz.

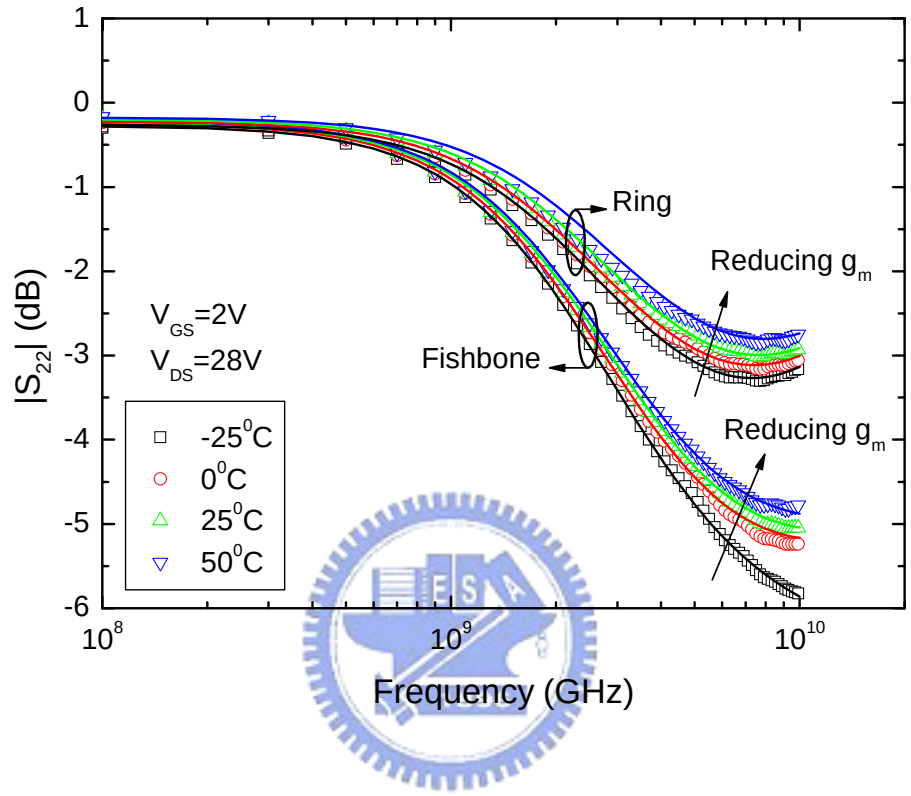


Fig. 3.9 Measured (open symbols) and simulated (solid line) $|S_{22}|$ of transistors for different layout structures from 0.1 to 10 GHz.

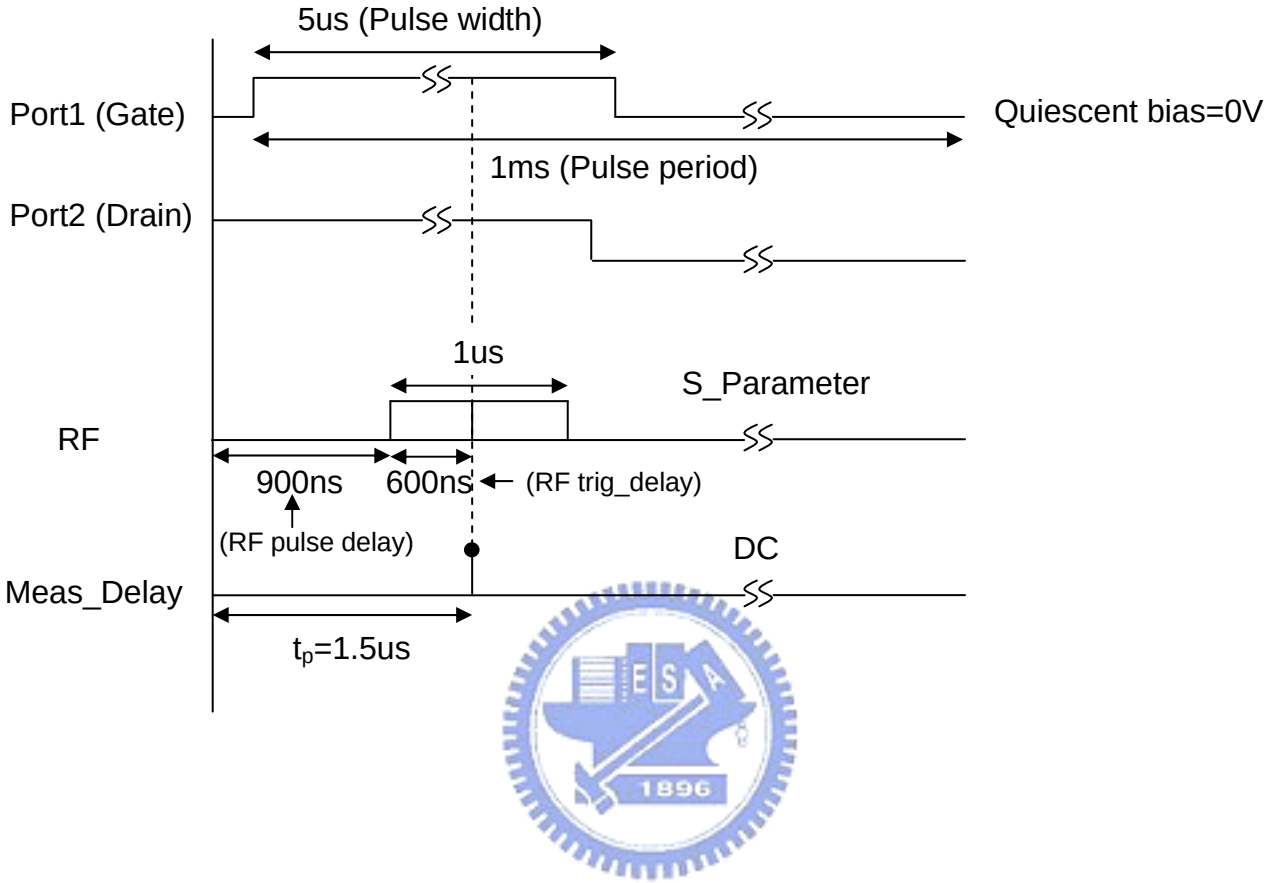


Fig. 3.10 Timing diagram showing the relationship of the applied bias, the RF input signal, and the sample points for pulsed measurement.

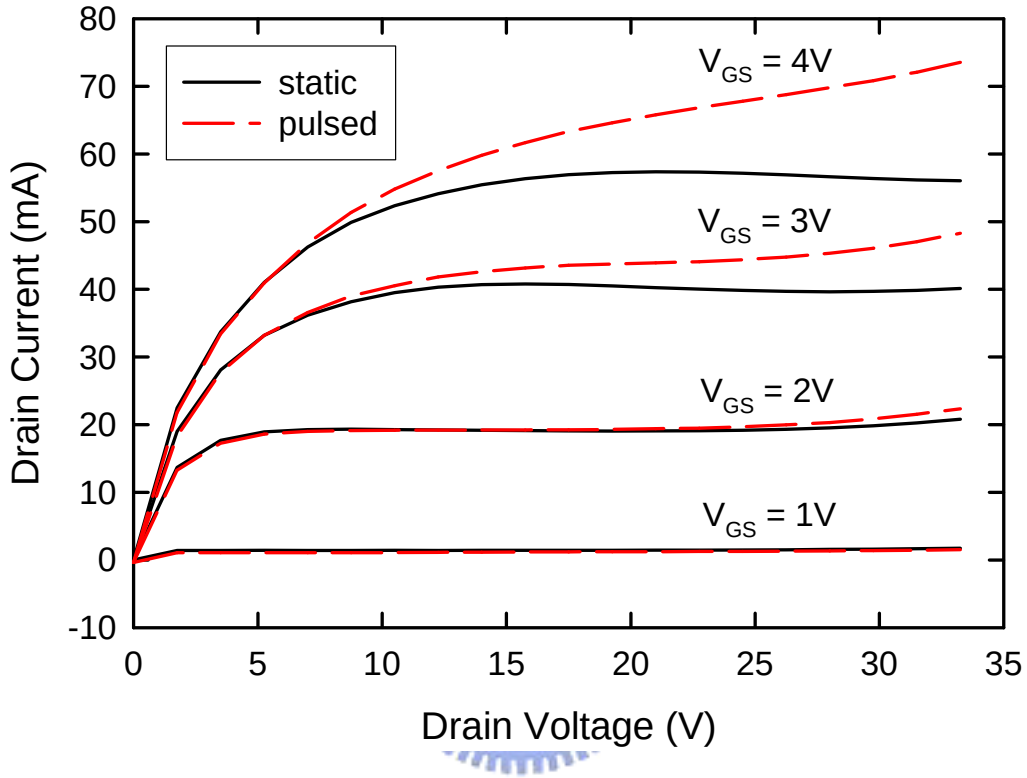


Fig. 3.11 Output characteristics of an LDMOS under static and pulsed conditions.

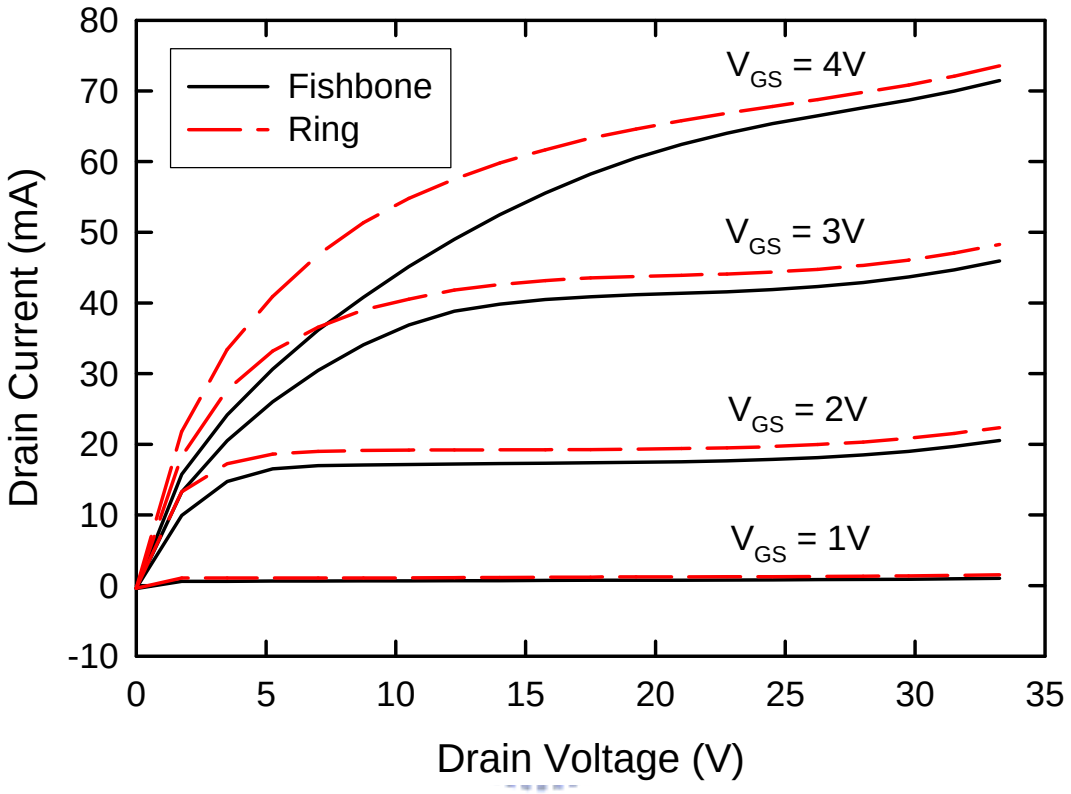
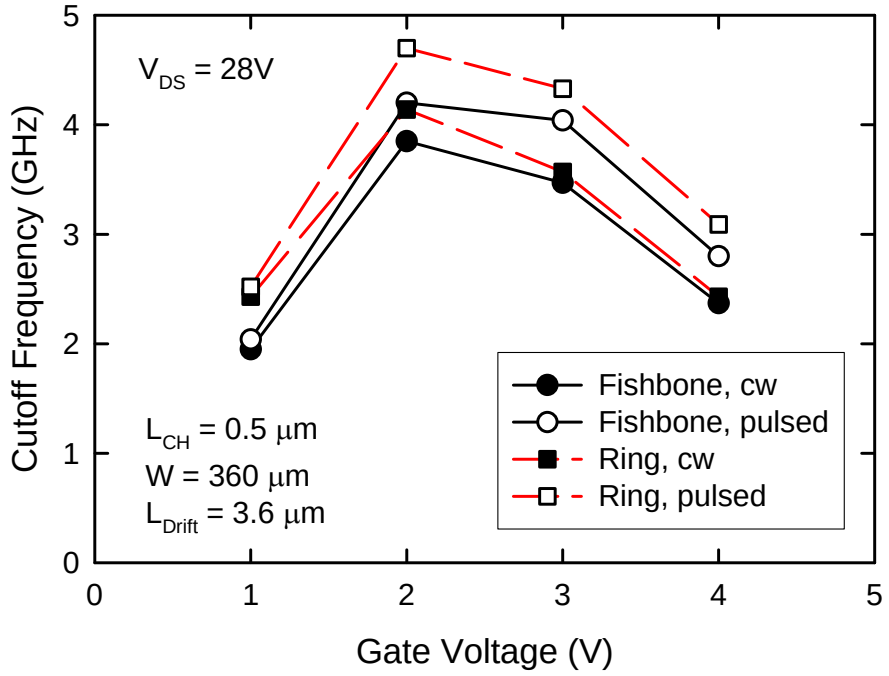
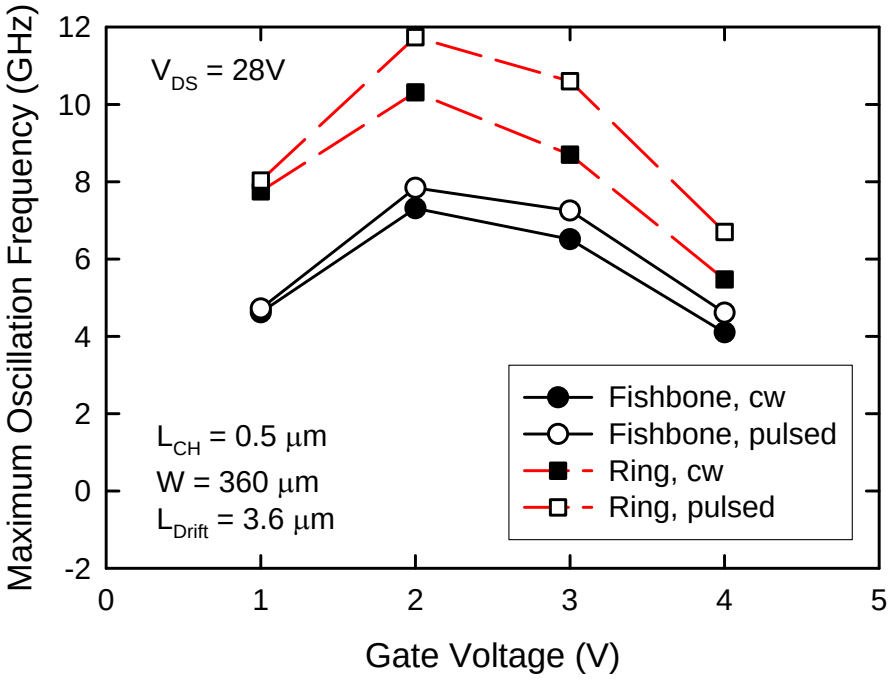


Fig. 3.12 Output characteristics of LDMOS transistors with different layout structures under pulsed condition.



(a)



(b)

Fig. 3.13 (a) Cutoff frequency and (b) maximum oscillation frequency versus the gate voltage under cw- and pulsed-mode measurements.

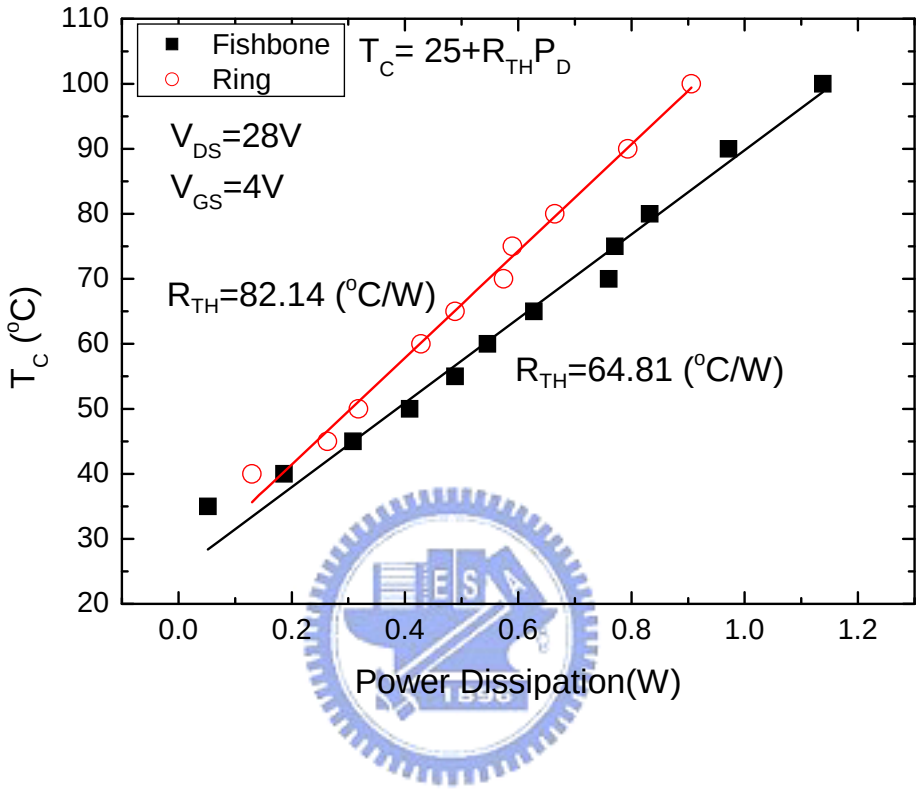


Fig. 3.14 Channel temperature versus power dissipation with different layout structures.

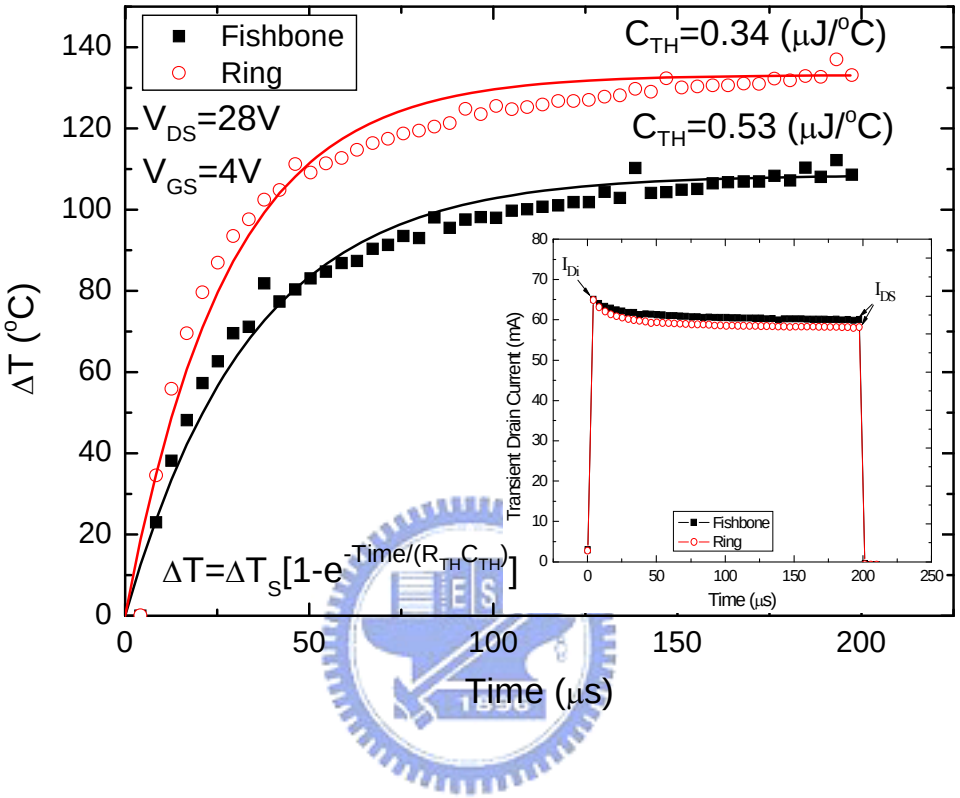


Fig. 3.15 Thermal transient response with different layout structures. The inset shows the transient drain current for both fishbone and ring.

Chapter 4

Thermal Effects on Capacitance Characteristics of RF LDMOS

4.1 Introduction

Because the device capacitances influence the input, output and feedback capacitances, which are important in the dynamic operation, and have large impact on device high-frequency performance, the capacitance characterization and modeling of LDMOS transistors have been studied widely [1]-[5]. As compared to the conventional MOSFET, a non-uniform doping channel and a drift region in LDMOS result in the unusual behavior in capacitances [6], [7]. Since the power transistors are operated at high power densities, the device temperature is high due to self-heating effect. Therefore we are interested to know the temperature effects on the capacitance characteristics of LDMOS transistors, which are not mentioned in previous papers. In this work, the capacitance characteristics of LDMOS transistors with different layout structures were studied at temperatures from -25^0C to 125^0C.

4.2 Capacitances versus V_{GS}

The capacitances we analyzed in this chapter were extracted form the S-parameters. Using an HP8510 network analyzer, S-parameters were measured on-wafer from 0.1 to 5GHz for different temperatures and then de-embedded by subtracting the OPEN dummy. Different control biases were applied from an HP4142B source measure unit to sweep from accumulation to strong inversion. The gate-to-source/body capacitance (C_{GS}+ C_{GB}) and gate-to-drain capacitance (C_{GD}) has been extracted from the de-embedded S-parameters at low frequency range by the formula described in chapter 2. In order to improve the RF performance, the source and P-body have been tied together to the RF ground. Therefore, the extracted gate-to-source capacitance (C_{GS}) and gate-to-body capacitance (C_{GB}) can not be

separated.

For fishbone structure, the extracted C_{GS}+ C_{GB} and C_{GD} as functions of gate voltage (V_{GS}) for drain voltage V_{DS}=0.1, 0.5, 3 and 5V at room temperature are shown in Fig. 4.1. At low drain bias (V_{DS}=0.1 V), the C_{GS}+ C_{GB} presents a similar behavior to the conventional MOSFET. For the lateral non-uniformly doped channel in LDMOS, the doping concentration was lower at the drain side than the source side. Hence, the drain end will be inverted prior to the source end, resulting in a peak in C_{GD} [5]. As the drain end was inverted, the accumulation electron charge sheet in N-type drift region will cause C_{GD} to increase as gate voltage (V_{GS}) increases. Once the V_{GS} exceeds the threshold voltage (i.e. source end was inverted), the C_{GD} starts to fall as the electron charge sheet is no longer connected only to the drain.

By increasing the drain voltage (V_{DS}>0.5 V), both C_{GS}+C_{GB} and C_{GD} present peaks. Because the inversion charges may be injected from the intrinsic MOSFET to the depleted area of the drift, the C_{GD} and C_{GS}+C_{GB} increase with increasing gate voltages and the C_{GS}+C_{GB} even rises over the limit of inversion [2]. In LDMOS, existed drift region resulting in the effect of quasi-saturation. Before the device entered the quasi-saturation regime, the drain side channel voltage (V_{ch}) increased as the V_{GS} increased just like in the conventional MOSFET. Then, V_{ch} decreased as the V_{GS} increased after the device enter the quasi-saturation regime [8]. Therefore, the C_{GS}+C_{GB} could exceed the value of total gate oxide capacitance due to change in surface potential in the drift goes negative where the change in gate voltage was still positive [9]. In the quasi-saturation regime, the surface potential variation becomes small gradually leads to the fall of the C_{GS}+C_{GB} and C_{GD}. Accordingly, the C_{GS}+C_{GB} and C_{GD} reach maximum at the onset of quasi-saturation. In Fig. 4.1, the corresponding drain currents at drain voltages V_{DS}=3 and 5 V were also presented. Because the higher drain voltage leads to a higher gate voltage at the onset of quasi-saturation, the peaks shift to higher gate voltages. In addition, the peak value increases in C_{GS}+C_{GB} and decreases in C_{GD} as the V_{DS} increases as shown in Fig. 4.1. It attributed to the charge partitioning under the gate when varying the

drain voltage.

When the gate voltages exceed the threshold voltage and the device was biased at saturation region (0.8 V<V_{GS}<1.2 V and V_{DS}>0.5 V in Fig. 4.1), the values of C_{GS}+C_{GB} decreased as the drain voltage increases. Fig. 4.2 shows the simulated C_{GS}+C_{GB} for four test structures: (a) uniform doped channel and without drift region, (b) non-uniform doped channel and without drift region, (c) uniform doped channel and with drift region, (d) non-uniform doped channel and with drift region. ISE TCAD was used as simulator and the structures we simulated are shown in Fig. 4.3. For non-uniform doped structure, the doping at source end of the channel was highest and decreases toward the drain side in the channel region. From the simulation results, only structures with drift region had this phenomenon. This indicates that the decrease in C_{GS}+C_{GB} can be attributed to the existence of drift region. For the device without drift region, C_{GS}+C_{GB} only with respect to the channel as shown in Fig. 4.3 (a). In the structure with drift region, part of the electrons in drift contributed to the C_{GS}+C_{GB} (shown in Fig. 4.3 (b)). As the drain voltage increased, the depletion region became large which resulting in lower number of electrons. Hence C_{GS}+C_{GB} was decreased.

For the ring structure, however, additional peaks in C_{GS}+C_{GB} and C_{GD} were observed when biasing at high drain voltage (V_{DS}=5 V) (see Fig. 4.4). As shown in Fig. 4.5, the currents flow from drain to source with uniform distribution in the full region of the fishbone structure. However, in the ring structure, the corner region of the drift showed lower current density than the edge region [10], [11], and thus it needed higher gate voltage to enter quasi-saturation. At the first peak, although the edge of the square ring operated in quasi-saturation region, the corner was still in pre-quasi-saturation. By increasing the gate voltage to 3.2 V, the current in the corner region was high enough to make the velocity of electrons in the drift saturated. Therefore, the corner operates in quasi-saturation and second peaks were generated in the C_{GS}+C_{GB} and C_{GD}.

4.3 Capacitances versus V_{DS}

For the fishbone structure, the extracted $C_{GS}+C_{GB}$ and C_{GD} as functions of drain voltage for V_{GS}=1, 1.2, 1.5 and 2 V at room temperature are shown in Fig. 4.6. Unlike the conventional MOSFET, $C_{GS}+C_{GB}$ showed peaks for various gate biases and these peaks appear at the same biases as that in Fig 4.1. As for C_{GD}, the peak appeared when the gate was biased at lower voltages and then vanished at higher gate voltages. Figure 4.7 shows the extracted $C_{GS}+C_{GB}$ and C_{GD} as functions of drain voltage for the ring structure. At low gate bias (V_{GS}<1.5 V), the $C_{GS}+C_{GB}$ presented a similar behavior to the fishbone structure. By increasing the gate voltage (V_{GS}>1.5 V), $C_{GS}+C_{GB}$ exhibited a hump not a peak shown in Fig. 4.7. According to Figure 4.4, as the drain voltage increased the first peak would meet the second peak at fixed gate voltage. Therefore, $C_{GS}+C_{GB}$ changed slowly with drain voltage in the ring and presented a hump. As for C_{GD}, the ring showed a similar behavior to the fishbone structure.

4.4 Thermal Effect on Capacitances versus Gate Voltage

Fig. 4.8 shows the influence of temperature on $C_{GS}+C_{GB}$ and C_{GD} of the fishbone structure. At V_{DS}=0.1 V, the transistor operated in linear region and the temperature dependence of $C_{GS}+C_{GB}$ was similar to the conventional MOSFET. With increasing temperature, the threshold voltage decreased and the flat band voltage increased due to higher intrinsic carrier concentration [12]. In our devices, the variation of the threshold voltage with temperature was -1.66 $mV/^0C$, which equaled the shift of the C_{GD} peak. In addition, the lower threshold voltage at higher temperature also indicated that the source end was inverted easier. Therefore, the peak in C_{GD} will shift to the lower gate voltage. Also, it results in the reduction of C_{GD} with increasing temperature when the transistor operates in weak and moderate inversion regimes.

At V_{DS}=5 V, the transistor operates in saturation region and the temperature coefficients of C_{GS}+C_{GB} and C_{GD} were positive in weak and moderate inversion regimes, due to the reduction of threshold voltage. From Fig. 4.8(b), we know that the shift of the C_{GS}+C_{GB} curve at V_{GS}=V_{TH} was about -1.52 mV/^{0}C, which approached the temperature coefficient of the threshold voltage (~ -1.64 mV/^{0}C). At higher gate voltages (V_{GS}>2 V), the values of capacitances were determined by the onset of quasi-saturation and by the drift depleted region. Because the quasi-saturation current decreased with increasing temperature (see the inset in Fig. 4.8(b)), the peak value of capacitances was decreased. It should be noted that the C_{GD} showed different behavior with temperature between low and high drain biases when the transistors operated at higher gate voltages (V_{GS}>2.5 V). At low drain voltage, the C_{GD} was dominated by the accumulation charge which formed below the thin oxide in the drift region and decreased slightly with increasing temperature (see Fig. 4.8(a)). At high drain voltages, the C_{GD} now was dominated by the drift depletion capacitance and increases with increasing temperature (see Fig. 4.8(b)). Consequently, Fig. 4.8(b) can be divided into three parts. In region I, the temperature coefficients were positive due to the reduction of V_{TH}. In region II, capacitances were affected by the quasi-saturation current and decrease with increasing temperature. In region III, C_{GD} was dominated by the drift depletion capacitance and increased with increasing temperature. Since the temperature variation of capacitance peaks was significantly affected by the drift region, device optimization could be done by changing the drift region length and drift doping concentration.

For the ring structure, the temperature dependence of capacitances was similar to that of the fishbone structure at V_{DS}=0.1 V (see Fig. 4.9(a)). Because the capacitance behavior was mainly related to the threshold voltage at low drain biases, the influence of corners can be neglected. At V_{DS}=5 V, the temperature coefficients of C_{GS}+C_{GB} and C_{GD} were positive in weak and moderate inversion regimes, due to the reduction of threshold voltage, as shown in Fig. 4.9(b). The shift of the C_{GS}+C_{GB} curve at V_{GS}=V_{TH} was about -1.42 mV/^{0}C, which

approaches the temperature coefficient of the threshold voltage (~ -1.56 mV/^{0}C). At higher gate voltage (V_{GS}>2 V), the peaks of C_{GS}+C_{GB} decreased with increasing temperature due to lower quasi-saturation current (see the inset in Fig. 4.9(b)). However, the peaks of C_{GD} increased with temperature, which was contrary to the trend in a fishbone structure. At the first peak, although the edge of the square ring has been in quasi-saturation region, the corner was still in pre-quasi-saturation. Therefore, the increase of C_{GD} peak with temperature indicated that the temperature-induced variation of C_{GD} was dominated by the corner. At the second peak, the corner has also been in quasi-saturation region, however, the C_{GD} in the edge has been dominated by the drift depletion capacitance. Because the drift depletion capacitance was very sensitive to the temperature as indicated in Fig. 4.8(b), the temperature-induced variation of C_{GD} now was dominated by the edge.

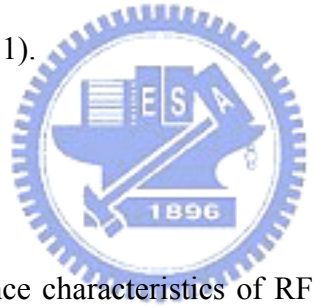
4.5 Thermal Effect on Capacitances versus Drain Voltage

Fig. 4.10(a) shows the influence of temperature on C_{GS}+C_{GB} and C_{GD} with different drain voltages at V_{GS} =1 V. The temperature coefficients of C_{GS}+C_{GB} and C_{GD} were positive at V_{DS} >0.5 V. Because the transistors operated in the median inversion region, the capacitances were mainly affected by threshold voltage. Hence the increases of capacitances were due to the reduction of threshold voltage. At V_{DS} <0.5 V, the transistors operated in linear region, and the source side was inverted easier at high temperatures. Therefore, the C_{GS}+C_{GB} increased and C_{GD} decreased with increasing temperature. At higher V_{DS}, C_{GS}+C_{GB} became independent of the drain voltage and increased with increasing temperature. This is because part of the electrons in drift contributes to the C_{GS}+C_{GB} as shown in Fig. 4.3 (b) and C_{GS}+C_{GB} also affected by the depletion width. For higher temperature, the depletion width became shorter which means large electrons can be provided to the C_{GS}+C_{GB}.

Fig. 4.10(b) shows the influence of temperature on C_{GS}+C_{GB} and C_{GD} with different

drain voltages at V_{GS} =2V. The transistors operated in the strong inversion region, and the variations of capacitances with temperature were different as compared to that in Fig. 4.10(a). At V_{DS} <0.5V, where the transistor operated in linear region, the C_{GS}+C_{GB} increased and C_{GD} decreased slightly with increasing temperature. At 0.5V< V_{DS} <6V, for transistor was entering the quasi-saturation region, the C_{GS}+C_{GB} decreased with increasing temperature, which is like as the capacitance behavior in Fig. 4.8(b). For C_{GD}, its temperature coefficient was positive at lower gate voltages and became negative at higher gate voltages, due to the combined effects of quasi-saturation and depleted drift. At V_{DS} >6 V, where the transistor operated in saturation region, the influence of temperature on C_{GS}+C_{GB} became smaller. At this time, the C_{GD} was dominated by the drift depletion capacitance, and thus the C_{GD} increased with temperature.

For the ring structure, the temperature dependence of capacitances was similar to that of the fishbone structure (see Fig. 4.11).



4.6 Summary

In this chapter, the capacitance characteristics of RF LDMOS transistors with different temperatures and layout structures were studied. Since LDMOS transistor has a lateral non-uniform doping channel and a drift region, peaks in C_{GS}+C_{GB} and C_{GD} have been observed. In addition, the variation of the capacitances with temperature is more complicated than that in conventional MOSFET, and it depends on the bias condition. In a conventional fishbone structure, the peaks in capacitances decrease with increasing temperature. For the ring structure, two peaks in a capacitance-voltage curve have been observed at high drain voltages due to the additional corner effect. Besides, peaks in C_{GS}+C_{GB} decrease and peaks in C_{GD} increase with increasing temperature at high drain voltages. These observations are important for circuit design to choose a bias condition with lower temperature sensitivity in capacitances. Moreover, since the capacitances are affected mainly by the threshold voltage,

quasi-saturation current and drift depletion capacitance, temperature effects on these parameters must be considered in the LDMOS capacitance model.

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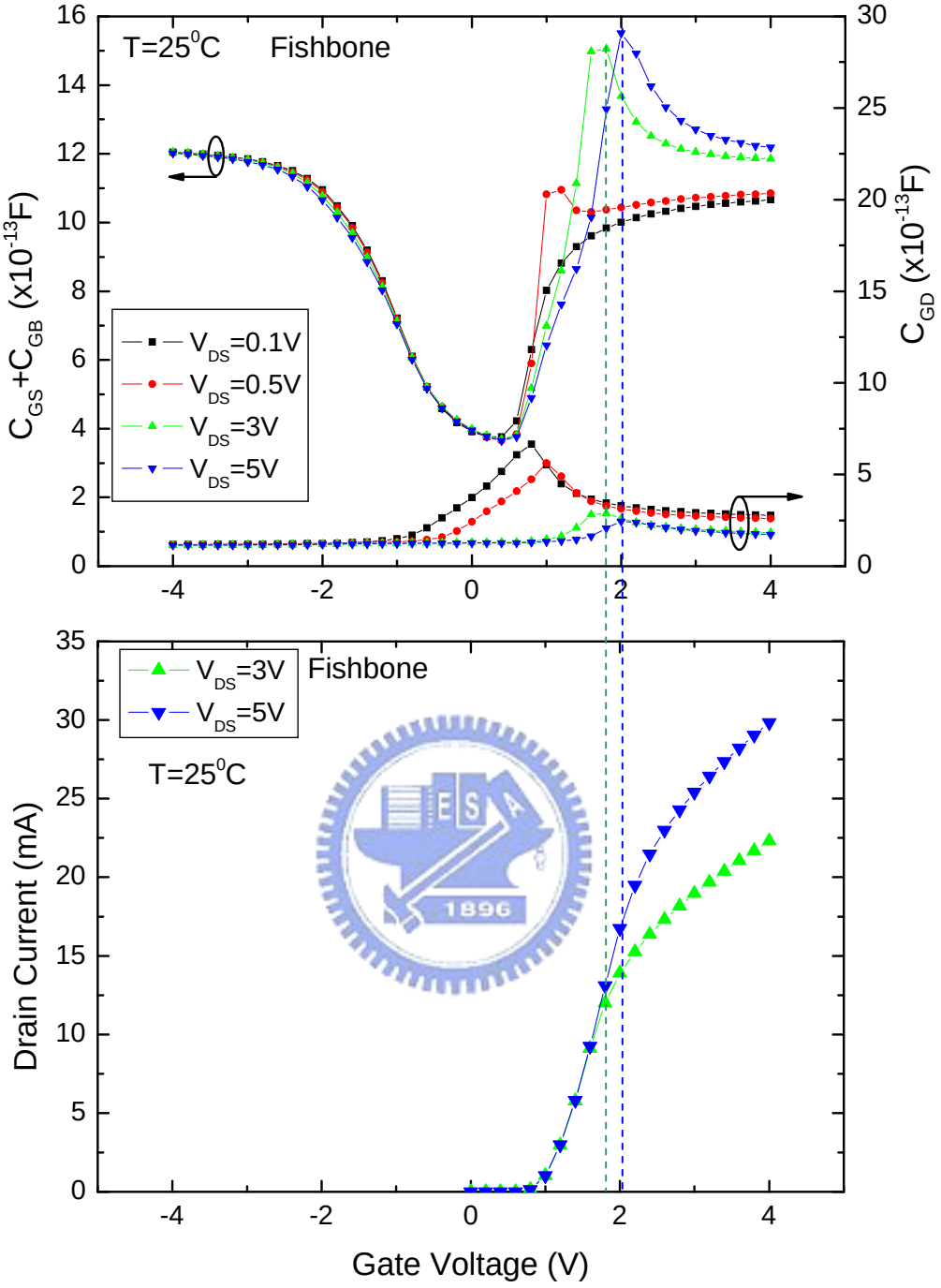


Fig. 4.1 Extracted $C_{GS}+C_{GB}$, C_{GD} and the drain current versus gate voltage at different drain biases for the fishbone structure.

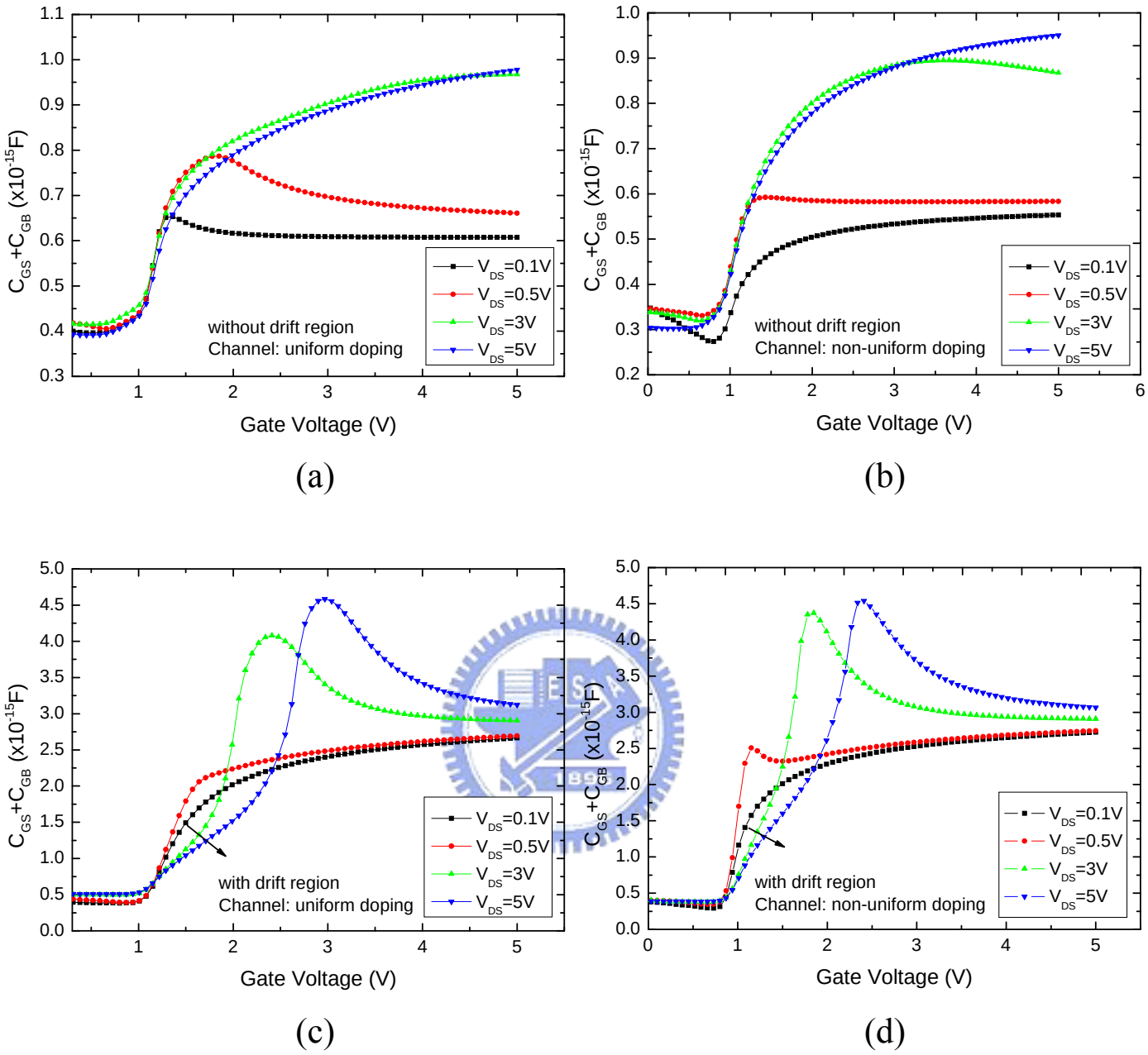
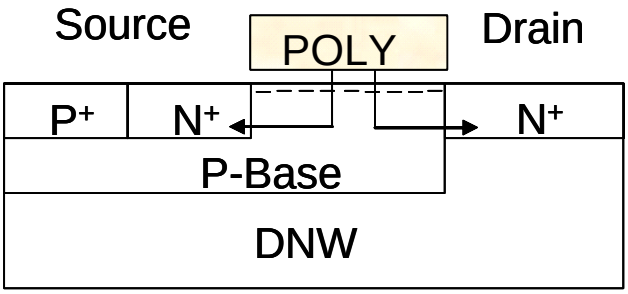
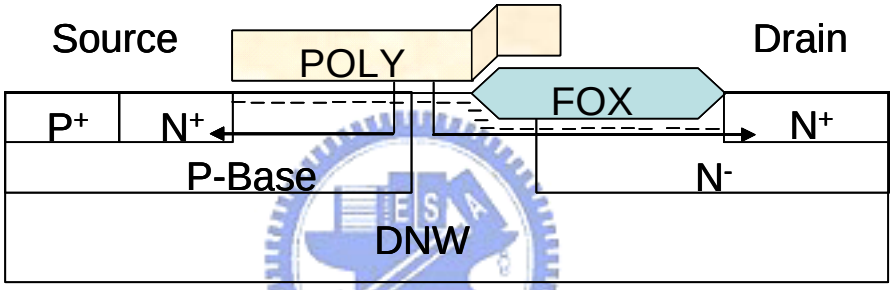


Fig. 4.2 Simulated $C_{GS}+C_{GB}$ for four test structures: (a) uniform doped channel and without drift region, (b) non-uniform doped channel and without drift region, (c) uniform doped channel and with drift region, (d) non-uniform doped channel and with drift region.



(a)



(b)

Fig. 4.3 Device configurations (a) without drift region and (b) with drift region when gate voltage exceed the threshold voltage and drain voltage is low.

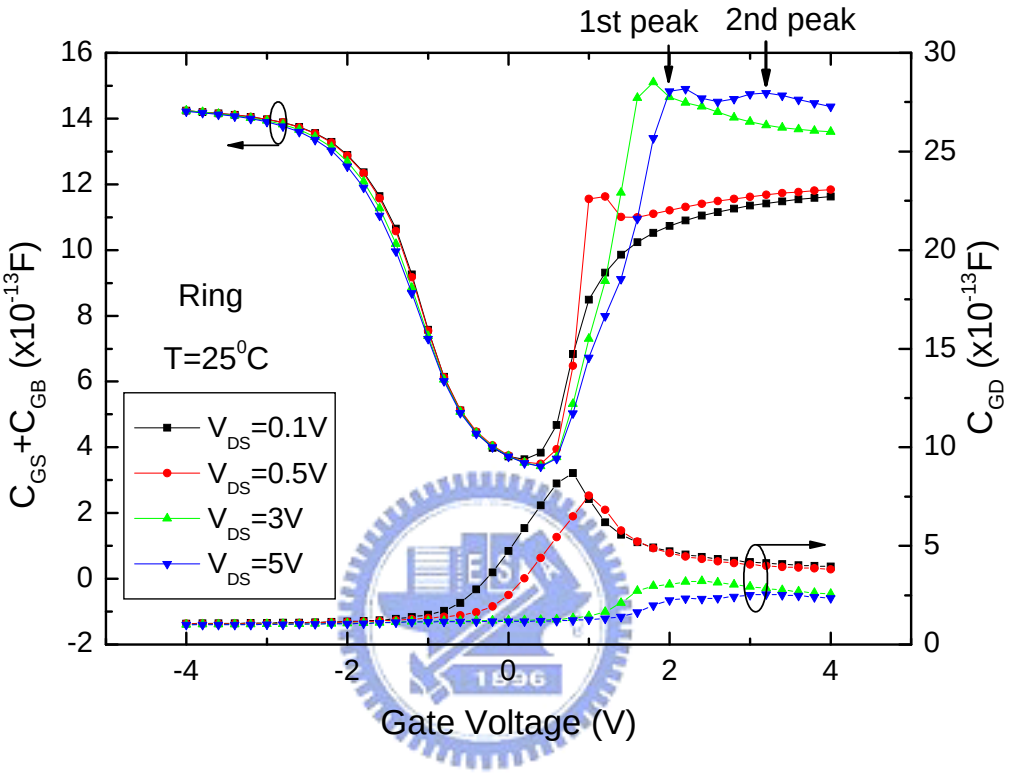


Fig. 4.4 Extracted C_{GS}+C_{GB} and C_{GD} versus gate voltage at different drain biases for the ring structure.

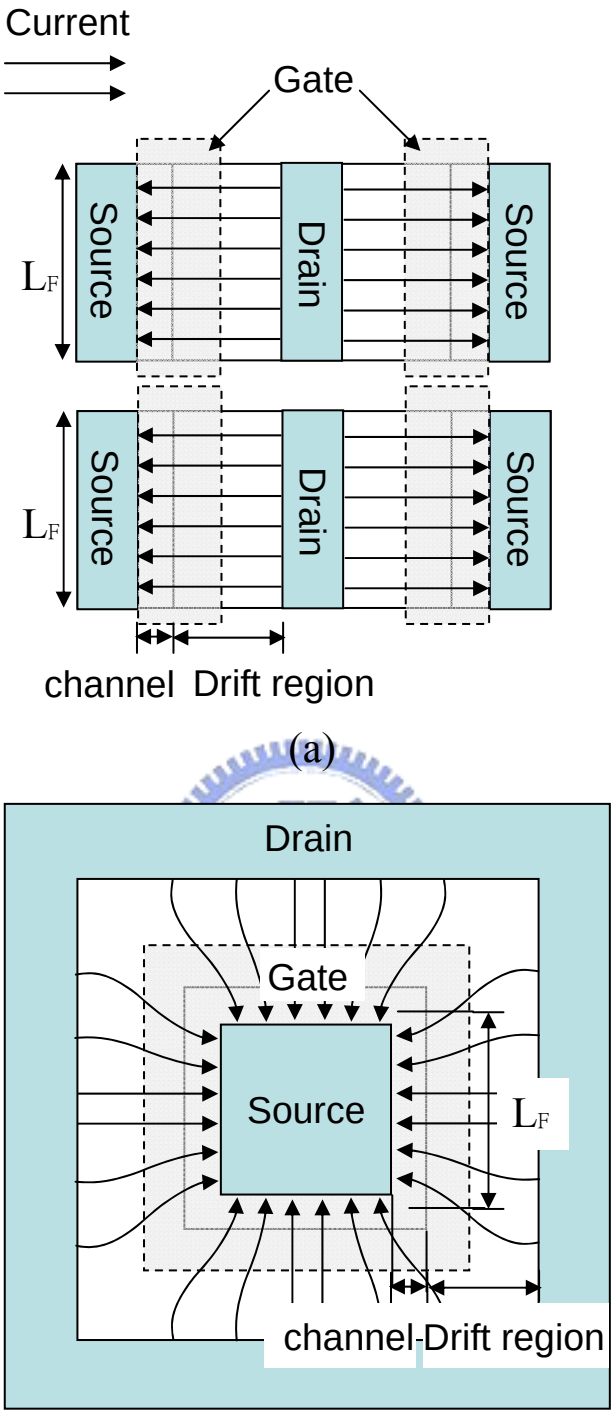


Fig. 4.5 Schematic view of layout structure and current distribution: (a) fishbone structure and (b) ring structure.

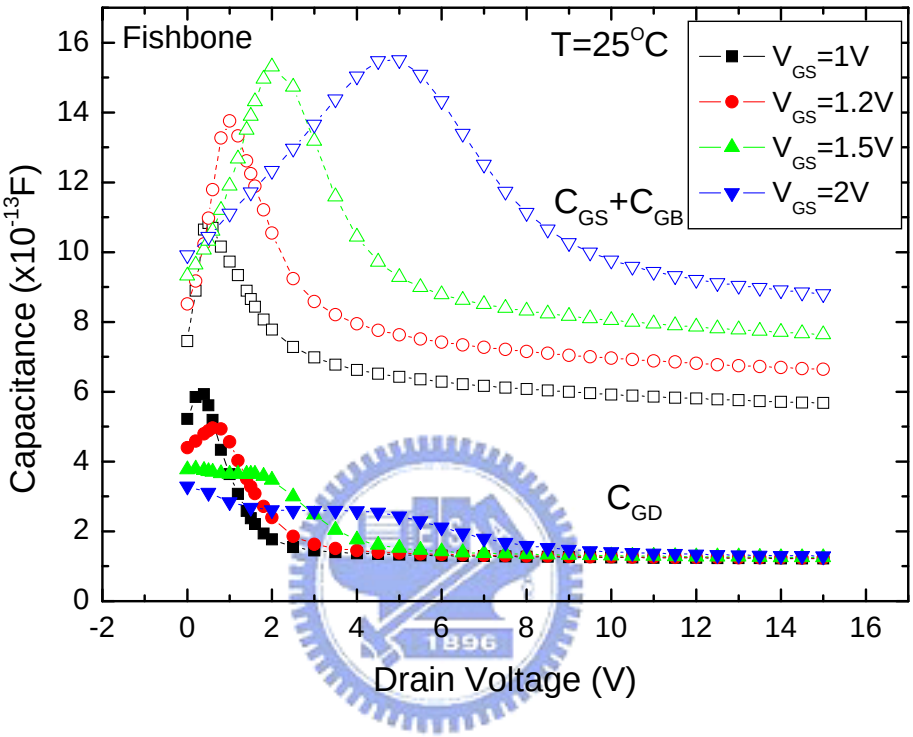


Fig. 4.6 Extracted C_{GS}+C_{GB} and C_{GD} versus drain voltage at different gate biases for the fishbone structure.

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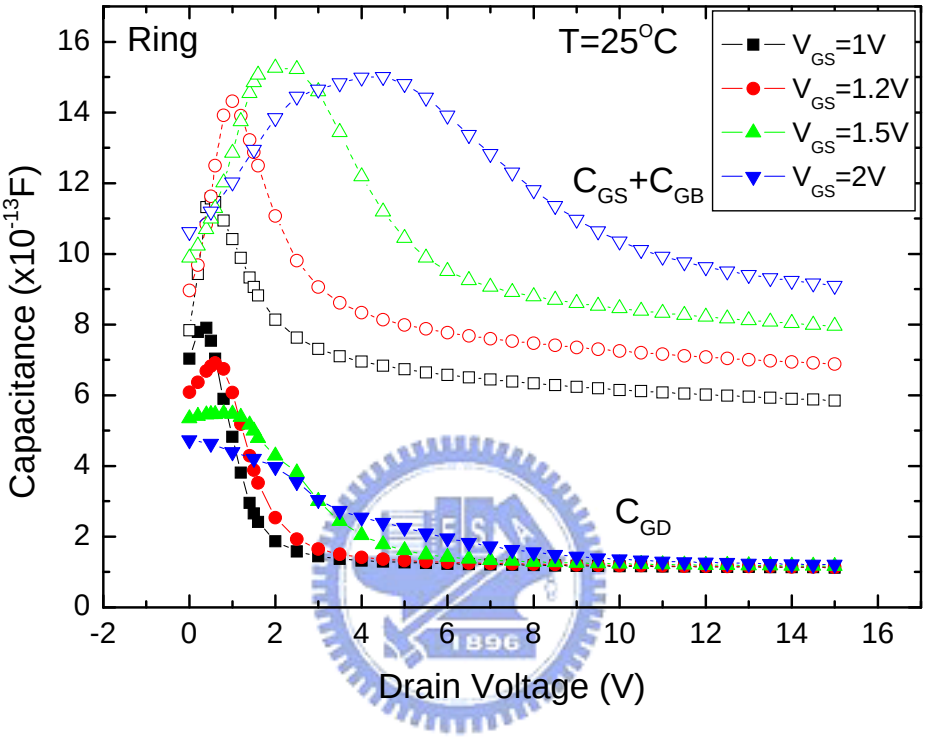
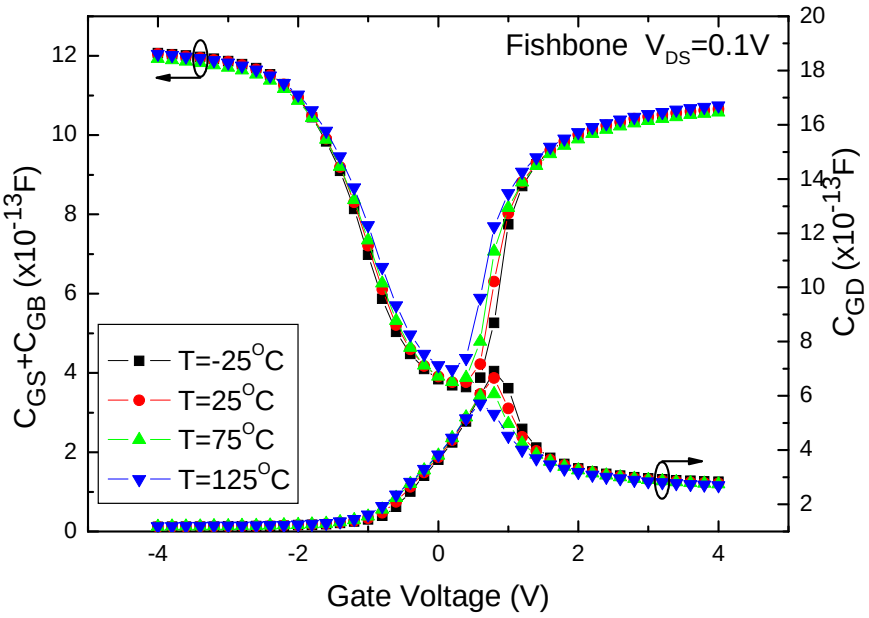
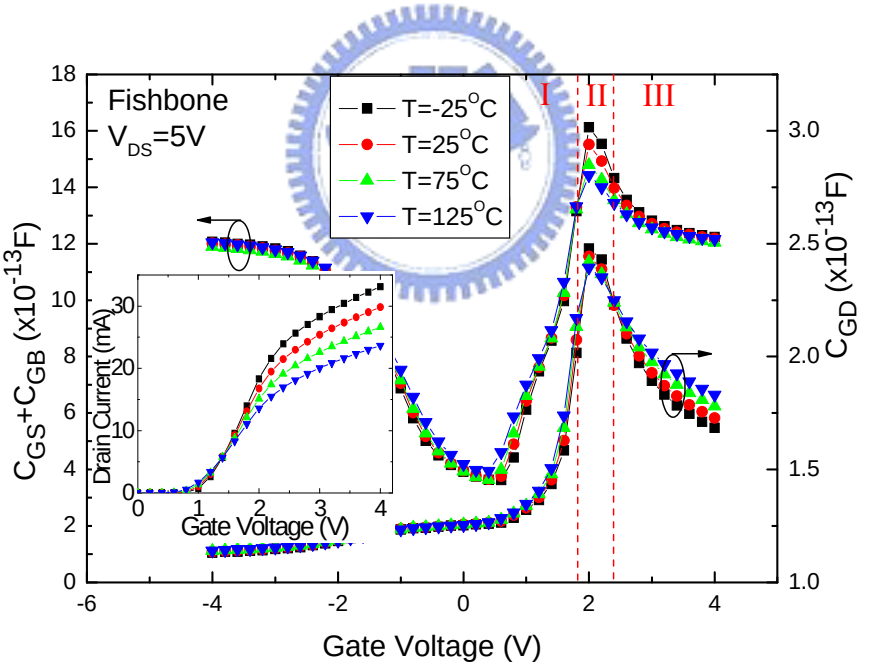


Fig. 4.7 Extracted C_{GS}+C_{GB} and C_{GD} versus drain voltage at different gate biases for the ring structure.

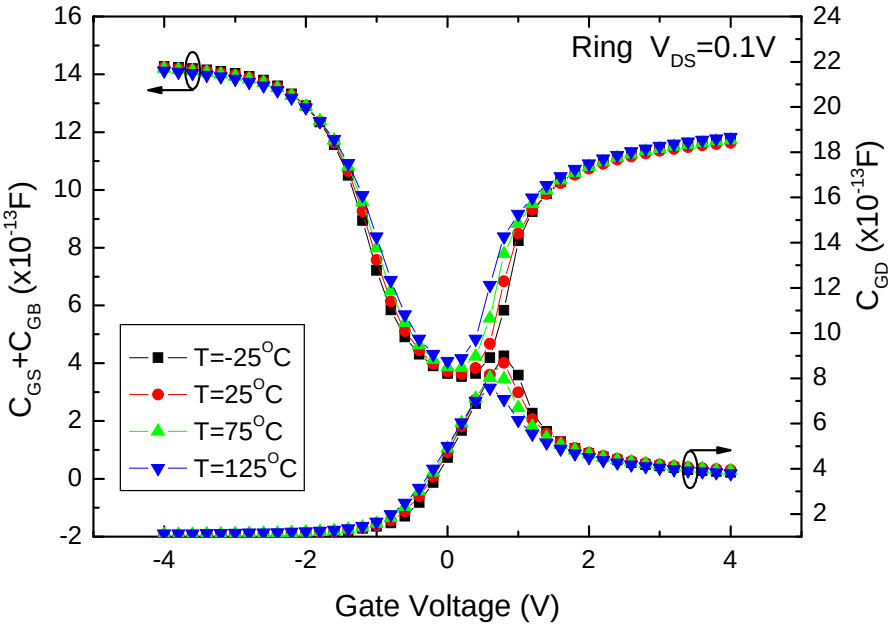


(a)

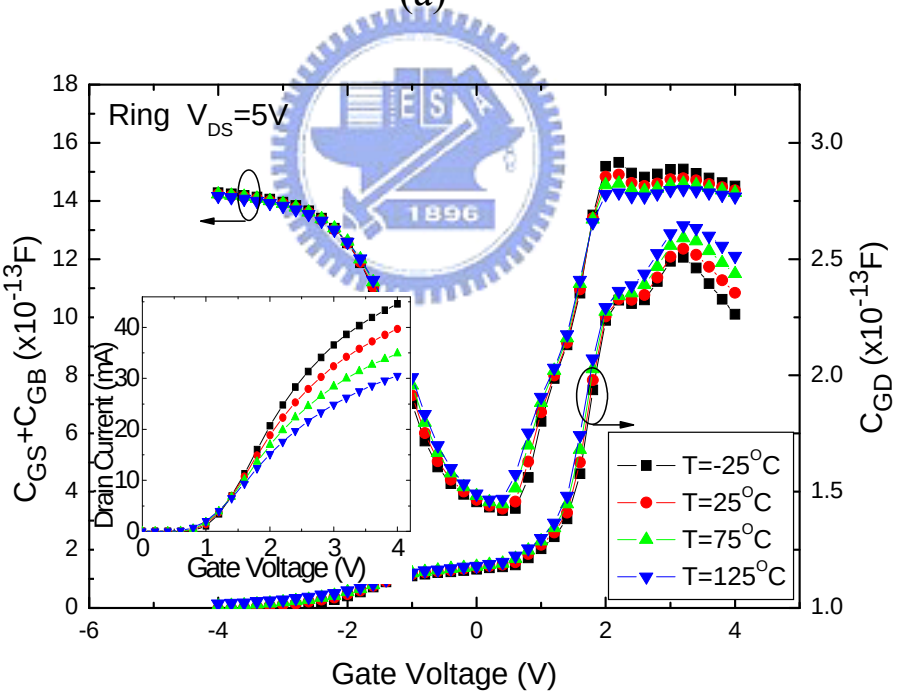


(b)

Fig. 4.8 Extracted $C_{GS}+C_{GB}$ and C_{GD} versus gate voltage with various temperatures at drain voltage (a) V_{DS}=0.1 V and (b) V_{DS}=5 V for a fishbone structure. The inset shows the drain current versus gate voltage with various temperatures.

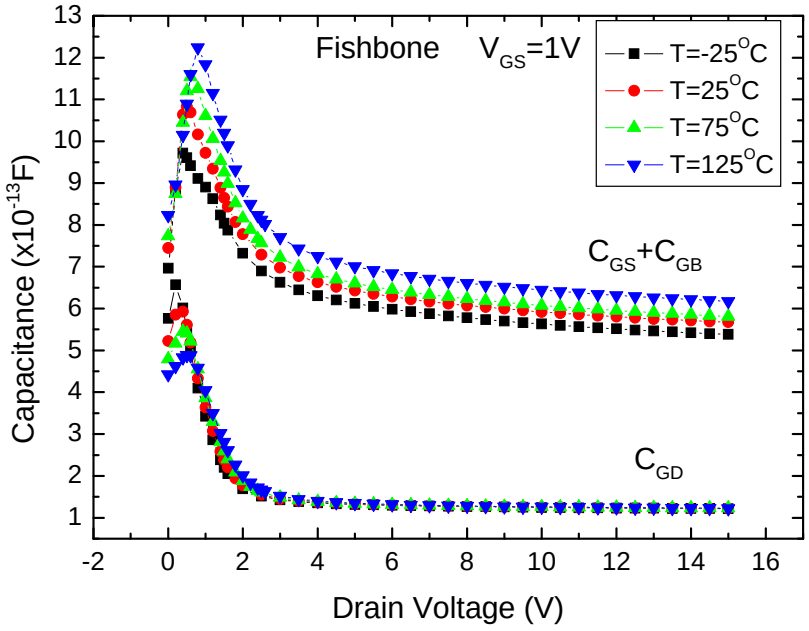


(a)

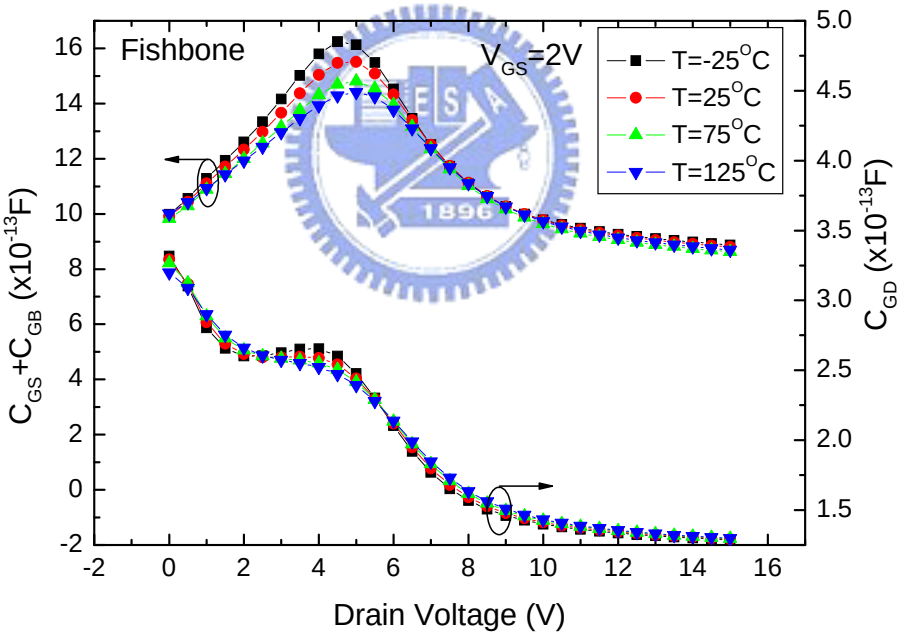


(b)

Fig. 4.9 Extracted $C_{GS}+C_{GB}$ and C_{GD} versus gate voltage with various temperatures at drain voltage (a) V_{DS}=0.1 V and (b) V_{DS}=5 V for a ring structure. The inset shows the drain current versus gate voltage with various temperatures.

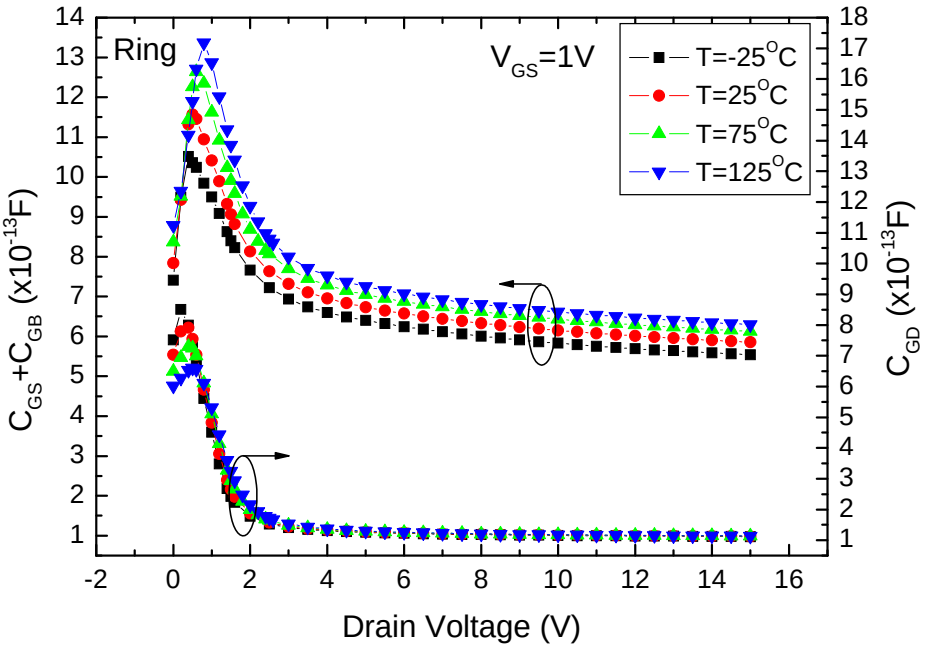


(a)

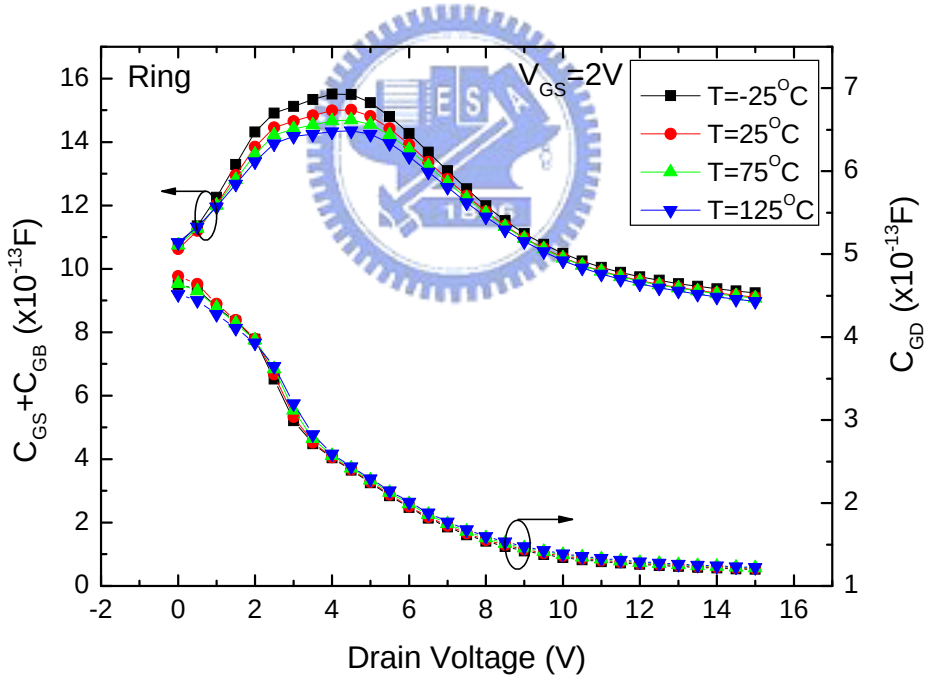


(b)

Fig. 4.10 Extracted $C_{GS}+C_{GB}$ and C_{GD} versus drain voltage with various temperatures at (a) V_{GS}=1 V and (b) V_{GS}=2 V for a fishbone structure.



(a)



(b)

Fig. 4.11 Extracted $C_{GS}+C_{GB}$ and C_{GD} versus drain voltage with various temperatures at (a) V_{GS}=1 V and (b) V_{GS}=2 V for a ring structure.

Chapter 5

Conclusions and Suggestion for Future Work

5.1 Conclusion

We have investigated the DC, AC, high-frequency, and RF power characteristics of LDMOS transistors with different layout designs. Based on the same breakdown voltage, we found that the transconductance, on-resistance, cutoff frequency, maximum oscillation frequency, even the power performance and linearity were improved using the ring structure. In the traditional design, the ring (also called enclosed, edgeless, or donut in other literatures) structure was used to lower the parasitic capacitances for more linear and faster devices [1-2]. For MOSFET, the conventional parasitic drain capacitance refers to the n+ drain to p-substrate junction capacitance. Hence, the drain was always surrounded by the transistor channel and source to reduce the area. In LDMOS, however, the parasitic drain capacitance refers to the deep n-well (DNW) to p-substrate junction capacitance. Therefore, drain outside or inside for ring structure has no impact on drain capacitance. Since larger area for output terminal could improve the on-resistance, ring structure with drain outside layout would be the better choice for the LDMOS. This layout design can improve the performance without altering the process flow.

In chapter 2 fishbone with various drift lengths and channel widths were investigated. The structure with smaller L_{Drift} has better on-resistance, f_T, f_{max}, and linearity, but smaller breakdown voltage. Fishbone and ring structures were also compared. The higher drain current and transconductance in the LDMOS with the ring structure were due to lower drain parasitic resistance. The f_T and f_{max} were also enhanced for the ring structure due to the lower drain parasitic resistance.

In chapter 3, we investigated the thermal effect on DC and high-frequency characteristics

of fishbone and ring structures. The result shows that the f_T and f_{max} were degraded at high temperatures due to lower transconductance. Because the drain resistance is higher in the LDMOS than the conventional MOSFET, the f_T is also affected by drain resistance. By de-embedding the effect of drain resistance, we show the real relation between the temperature-induced variation of f_T and g_m. we also found that the temperature dependence of f_{max} is affected by the drain resistance and drain-substrate junction capacitance. To study the self-heating effect, DC and high-frequency characteristics were measured under pulse condition. From the extracted R_{TH} and C_{TH}, the effect of self-heating was more severe in ring structure. In the pulsed-mode measurement, the ring has better drain current, f_T and f_{max} than the fishbone structure. Although the ring structure showed lower static drain current than the fishbone structure at high gate biases due to the significant self-heating effect, its current drive capability could be improved using a pulsed-mode operation.

Capacitance characteristics were analyzed completely in chapter 4. The thermal effects on capacitances were also investigated. For having a non-uniform doping channel, C_{GD} exhibits a peak at the threshold voltage. For existence of the drift region, C_{GS}+ C_{GB} and C_{GD} show a peak at the onset of quasi-saturation. In the ring structure, the second peaks in a capacitance-voltage curve have been observed at high drain voltages due to the additional corner effect. Because the capacitances are affected mainly by the threshold voltage, quasi-saturation current and drift depletion capacitance, the variation of the capacitances with temperature is more complicated than that in conventional MOSFET, and it depends on the bias condition. Based on the result we analyzed, we can well model the temperature-dependence capacitance by adding these parameters and also can choose a bias condition with lower temperature sensitivity in capacitances.

5.2 Suggestion for Future Work

Since the thermal effects on drain current and capacitance were investigated clearly in

our study, the temperature dependent current and capacitance equations can be derived. In the future, the drain current, substrate current, gate capacitance, and junction capacitance models can be built in terms of surface potential. Eventually, a complete large signal model for RF LDMOS can be built.

In addition, the reliability issue of RF LDMOS is another important topic. The special DC behavior of LDMOS has been under study for several years [3-5]. The substrate current shows a second peak at high gate voltage [4]. The hot hole injection in the drift region after stress results in the degradation of on-resistance and increase of breakdown voltage, while it does not affect the threshold voltage [5]. Most of the reliability issues focus on DC performance, and seldom address the high frequency and RF power characteristics. In the future, the hot carrier effects on high frequency and power characteristics can to be investigated.

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