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電子工程學系電子研究所

博 士 論 文

應變金氧半場效電晶體機械應力萃取與其相關物理模型建立之研究

Mechanical Stress Assessment and Physical Model Development in Strained MOSFETs

研 究 生 ： 謝振宇

指導教授 ： 陳明哲 博士

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國立交通大學

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摘要

Abstract in Chinese

近來，金氧半場效電晶體中機械應力已引起大量的注意，特別是在電性(如：載子遷移率、驅動能力及漏電流)及物理現象(如：摻雜擴散及介電層缺陷)的改變。因此本論文將會展示如何評估元件中各處應力量值。接著，在處理上述議題時，相對應的理論模型或分析將可被建立基於提出的方法之上。

首先，針對具有1.27奈米閘極氧化層且經由佈局技巧所產生的通道方向應力的n型金氧半場效電晶體進行導帶電子直接穿隧電流量測。藉由已知製程參數及已發表形變位能常數，計算不同電壓下閘極電流變化百分比可以得到通道平均應力量值。為驗證此法的精確性，在相同元件上進行載子遷移率的量測。所產出的壓阻係數與發表的數值高度相符。而佈局技巧也同時成功藉由經驗公式所檢驗。

其次，利用不同的通道寬度，量測在具有壓縮應力淺溝槽絕緣層下的閘極穿隧電流。每單位通道寬度之閘極電流隨著寬度下降，呈現增加的趨勢。在這窄縮的方向，兩個基本的效應須同時考慮：一為在淺溝槽絕緣層邊緣的寬度修正，另一為增長的通道應力。為了區別此兩因素，一個新的解析寬度依存閘極穿隧電流模型已被成功的建立及使用。而所得到的寬度修正效應在較為窄小的元件中，相較應力具有壓倒性的重要。然而，對於較寬的元件，此兩效應的影響是相當的。萃取出之寬度修正量值及應力大小可以直接重現汲極電流變化。特別的是，寬度修正與應力對閘極電流的影響趨勢相同，但對汲極

電流影響相反。

再者，不同閘極邊緣至淺溝槽絕緣層寬度下元件的次臨界電流被量測並轉換成源極/汲極延伸區應力值。此萃取出的局部應力大小與在相同元件上，藉由閘極穿隧電流及載子遷移率所評估的通道應力趨勢相符。閘極邊緣穿隧電流可以直接導出閘極與延伸區重疊長度的量值。特別是，在壓縮應力下造成摻雜擴散縮短的長度及應變引發的活化能量值與製程模擬結果相符。亦成功建立一個以物理導向的解析模型，將側向擴散長度表為延伸區應力的函式。

最後，在p型通道金氧半場效電晶體上的低頻雜訊量測得出：隨淺溝槽絕緣層拉伸應力在寬度方向的增加將會導致氧化層界面缺陷的減少。在此，兩種可能的物理緣由被提出：在氧化過程中，(一)較為鬆弛的介面應變；以及(二)單位面積下較為減少的過量矽原子。

Mechanical Stress Assessment and Physical Model Development in Strained MOSFETs

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Abstract in English

Recently, mechanical stress in MOSFETs has gained much attention due to significant changes in electrical performance (mobility, drive capability, leakage etc.) and process issues (dopant diffusion, gate oxide integrity etc.). Therefore, this dissertation is aimed at demonstrating how to measure stress quantities in each part of the devices and address the induced changes. Based on the proposed methods, the underlying physical framework can be established while meeting the above issues.

We first measure the conduction-band electron direct tunneling current through 1.27-nm gate oxide of *n*-MOSFETs that undergo longitudinal stress via a layout technique. With known process parameters and published deformation potential constants as input, fitting of the measured direct tunneling current versus gate voltage leads to channel stress. To examine the accuracy of the method, a link with the mobility measurement on the same device is conducted. The resulting piezoresistance coefficient is shown to be in good agreement with literature values. The layout technique used is validated as well.

Then, gate direct tunneling current under STI compressive stress is measured in a wide range of the drawn gate width W (= 0.11, 0.24, 0.6, 1.0 and 10 μm). The *apparent* gate current per unit width exhibits an increasing trend with decreasing W. In this narrowing direction, two

fundamentally different effects are encountered: One of the delta width (ΔW) near the STI edge and one of the enhanced STI stress in the channel. To distinguish between the two effects, a new analytical width-dependent direct tunneling model is developed and applied. Reasonable agreement with data is achieved. The resulting delta width effect is found to dominate over the stress effect especially in the narrow devices, while for the wide ones, they will be comparable. The extracted ΔW and the underlying channel stress (with the uncertainties identified) straightforwardly produce a good fitting of the drain current variation counterpart. Specifically, it is justified that the delta width and STI stress are co-operative in constituting gate current variation but both have opposite effects on the drain current one.

Third, drain subthreshold current is measured as a function of the gate edge to STI spacing and is transformed into the source/drain extension corner stress. The extracted local stress is quantitatively reasonable with those of the channel as created by the gate direct tunneling measurement in inversion, and the mobility measurement. In addition, its dependencies on the gate edge to STI spacing confirm the validity of the layout technique in controlling the stress. The gate edge direct tunneling (EDT) measurement in accumulation straightforwardly leads to the quantified gate-to-source/drain-extension overlap length. Particularly, a retarded diffusion length and the resulting strain-induced activation energy both are in satisfactory agreement with those of the process simulation. A physically oriented analytic model is therefore reached, expressing the lateral diffusion length as a function of the corner stress.

Finally, low-frequency noise measurement on *p*-channel MOSFETs yields the density of the gate-oxide interface states, exhibiting a decreasing trend with increasing STI tensile stress in the channel width direction. Two plausible physical origins of the interface-state density suppression in narrow devices are proposed: relaxed interface strain and reduced excess silicon per unit area during the thermal oxidation.

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Chapter 1

Introduction

1.1 Overview and Motivation

During the quest for increasing device density in integrated circuits, many problems are encountered and need to be solved. As some problems are alleviated, new issues emerge. One of the problems gaining importance in silicon fabrication is process-induced mechanical stress. Many of the processes used in silicon IC fabrication individually and cooperatively contribute to the development of stress in the silicon active areas. Of prime interest is the mechanical stress generated in the isolation process flow. Shallow Trench Isolation (STI) is steadily becoming the predominant isolation technology and is continually challenged as design rules are scaled further [1.1]. One practical topic associated with this trend is that the STI induced mechanical stress in the active region can be controlled with the layout design. This drives the study forward.

Effects of mechanical stress can be divided into two categories: (1) energy band shift and (2) physical behavior modification during the manufacturing process. For the first issue, it is well known that stress can alter the energy structure, which in turn, affects the electrical performance such as the mobility [1.2]–[1.4], the threshold voltage [1.5], and the gate direct tunneling current [1.6]–[1.8]. These properties are strongly related to strain-induced band distortion and warping which actually change the energy level, population, effective mass, and scattering time in each valley. As for the second part, stressed or strained regions have also been shown to influence the physical behaviors like the hot carrier immunity [1.9], the diffusion of dopants [1.10]–[1.12], and the gate oxide integrity [1.13]–[1.15]. Such

phenomena were closely contributed by point defects migration and bonding relaxation under different stress conditions. All of above are the major concerns either during manufacturing or in operation. Thus, systematic connection and clarification between the status or magnitude of stress and its physical characteristics in a certain device are urgent and crucial.

1.2 Goal

Mechanical stress influences the physical mechanisms in the fabrication process as well as device operation. Such areas may include point defect diffusion kinetics, extended interfacial defect interactions, and band structure modification. Thus, an accurate stress evaluation is necessary for further investigation of its effects. The goal of this work is primarily to develop a technique where stress can be obtained from the electrical measurement. Once the STI stress in the system is understood, stress or strain dependent models can be established to clarify contradictory issues. Stress evaluation also is helpful in the development and analysis of isolation process technologies.

Dopant diffusion changes have become more prominent recently as a result of increasing mechanical stress in magnitude as the dimensions of the MOSFET are scaled down. Traditionally, the final doping profile prediction is utilized by technology aided-computer design (TCAD) and it may consume a lot of time due to the complexity of transistor structure. However, an approach to immediately reflecting the control of diffusion was still lacking. Thus, another goal of this research is to construct a stress or strain induced diffusion model to trace back the degree of dopant migration with the help of edge direct tunneling.

One of the goals is to clarify the influence of tensile and compressive stress on gate oxide integrity. Such results can relate to reliability issues. All of these would give useful insight into the next generation transistor design involved with the stress effects.

1.3 Dissertation Organization

The purpose of this work focuses on the assessment of the STI stress quantities as well as the physical model establishment. Based on the extracted values and status of stress, we can extend the issues to modeling of strain-induced dopant diffusion and gate oxide integrity. At this point, this dissertation is organized into seven chapters.

Chapter 2 begins with the mechanics of materials. The definitions of stress and strain are first reviewed. Their dependencies on each other are associated with the elasticity. Meanwhile, the theory of strain-induced energy band shift both on conduction and valence bands is introduced and will be used in later chapters.

As for the main parts of the dissertation, first of all, we present a simple method to electrically assess the average mechanical stress in channel region using the gate direct tunneling current changes. In this study, shallow trench isolation-induced mechanical stress can serve as the dominant source in the channel due to the thermal expansion and the layout technique will be utilized to produce a variety of stress. The different approaches to determining stresses in longitudinal and transverse directions were detailed in Chapter 3 and 4, respectively. Confirmative evidence is verified by piezoresistance coefficient. Especially, in the narrowing direction, the delta width effect together with the stress effect is adopted to clarify the anomalous trend of gate tunneling current.

Second, in Chapter 5, we show how to transform the drain subthreshold current change to the source/drain corner stress. With the modeling of edge direct tunneling current, it leads to the underlying gate-to-source/drain extension overlap length. Therefore, a physically-oriented analytic model is successfully established, expressing the lateral diffusion as a function of corner stress.

In Chapter 6, low-frequency noise measurement will be conducted to extract the oxide integrity in the channel narrowing direction in Chapter 6. Using the stress extraction technique built in previous chapters, the effect of stress on interface states during the oxidation will be demonstrated.

Finally, Chapter 7 delivers a conclusion to the research work, and also addresses the future work as extension of this dissertation.

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Chapter 2

Strain Effect on Electronic Band Structure

2.1 Review of Mechanics of Materials

The property of solid materials to deform under the application of an external force and to regain their original shape after the force is removed is referred to as its elasticity. The external force applied on a specified area is known as *stress*, while the amount of deformation is called the *strain*. In this section, the theory of stress, strain and their interdependence is briefly discussed.

2.1.1 Stress and Strain

Stress - Stress is the distribution of internal body forces of varying intensity due to externally applied forces [2.1], [2.2]. Consider a general body subjected to forces acting on its surface: Passing a plane through the body cutting it along surface A and letting the force, which is transmitted through an incremental area ΔA of A by the part on positive side Q, be denoted by ΔF. The force ΔF may be resolved into components ΔF_N and ΔF_S, as illustrated in Fig. 2.1(a), along unit normal N and unit tangent S, respectively, to the plane Q. The force ΔF_N is called normal (perpendicular) stress and ΔF_S is shear (tangential) stress on area ΔA. The magnitude of the average forces per unit area is $\Delta F/\Delta A$. The concept of stress at a point is obtained by letting ΔA become an infinitesimal. The limiting ratio $\Delta F/\Delta A$ as ΔA goes to zero defines the stress vector as given by

$$\sigma = \lim_{\Delta A \to 0} \frac{\Delta F}{\Delta A} \tag{2.1}$$

Similarly, the limiting ratios of $\Delta F_N/\Delta A$ and $\Delta F_S/\Delta A$ define the *normal stress vector* σ_N and the *shear stress vector* σ_S that act on a point in the plane Q. These vectors are described by the relations

$$\sigma_N = \lim_{\Delta A \to 0} \frac{\Delta F_N}{\Delta A}, \ \sigma_S = \lim_{\Delta A \to 0} \frac{\Delta F_S}{\Delta A} \tag{2.2}$$

Three stress vectors acting on three mutually orthogonal planes intersecting at that point can then determine the stress state as shown in Fig. 2.1(b). The stress tensor is composed of the three stress vectors and is sufficient to define the stress state in any element in a body. To illustrate the tensor nature of stress present at point in the continuous body, consider a cubic element of infinitesimal dimensions. For simplicity of notation, let the cube be aligned perpendicular with the system axis. The stress vector T_x acting on the plane normal to the x-direction is the following:

$$T_x = \sigma_{xx} \cdot \vec{x} + \tau_{xy} \cdot \vec{y} + \tau_{xz} \cdot \vec{z} \tag{2.3}$$

The nine stress components relative to rectangular coordinate axes may tabulated in array form as follows:

$$\sigma_{ij} = \begin{bmatrix} \sigma_{xx} & \tau_{xy} & \tau_{xz} \\ \tau_{yx} & \sigma_{yy} & \tau_{yz} \\ \tau_{zx} & \tau_{zy} & \sigma_{zz} \end{bmatrix} \tag{2.4}$$

where σ_{ij} represents the stress array called stress tensor, σ_{ii} are the normal stress components acting on the faces perpendicular to i-direction and τ_{ij} are the shear stress components oriented in the j-direction on the face with normal in the i-direction. At mechanical equilibrium, it can be shown that three pairs of shear stresses are equal that lead to the result

$$\tau_{ij} = \tau_{ji} \tag{2.5}$$

Hence, a column vector of six independent components can then describe the state of stress at a point:

$$\sigma^T = \begin{bmatrix} \sigma_{xx} & \sigma_{yy} & \sigma_{zz} & \tau_{xy} & \tau_{yz} & \tau_{zx} \end{bmatrix} \tag{2.6}$$

Strain – The application of stress to a body in equilibrium causes it to undergo deformation or strain. It is the geometrical measure of deformation representing the relative displacement between particles in the material body. *Normal strain* is defined as the amount of stretch or compression along a material line element while *shear strain* is a degree of distortion associated with the sliding of plane layers over each other within a deforming body.

Consider a two-dimensional deformation of an infinitesimal rectangular material element with dimensions as shown in Fig. 2.2. From the geometry, we can write

$$\overline{A'B'} = \sqrt{\left(dx + \frac{\partial u_x}{\partial x} dx \right)^2 + \left(\frac{\partial u_y}{\partial x} dx \right)^2} \tag{2.7}$$

Under the assumption of small displacement, which means $\nabla u << 1$, the length of $\overline{A'B'}$ can reduce $dx + (\partial u_x / \partial x) dx$. The normal strain in x - direction of the element is defined as

$$\varepsilon_{xx} = \frac{\overline{A'B'} - \overline{AB}}{\overline{AB}} \approx \frac{\partial u_x}{\partial x} \tag{2.8}$$

The shear strain is the change of the angle between two originally orthogonal axes. For small rotation (i.e. $\alpha, \beta << 1$) and infinitesimal approximation, we get

$$\alpha \approx \tan\alpha = \frac{\frac{\partial u_y}{\partial x} dx}{dx + \frac{\partial u_x}{\partial x} dx} \approx \frac{\partial u_y}{\partial x}, \quad \beta \approx \tan\beta = \frac{\frac{\partial u_x}{\partial y} dy}{dy + \frac{\partial u_x}{\partial y} dy} \approx \frac{\partial u_x}{\partial y} \tag{2.9}$$

Thus, the shear strain can be written as

$$\gamma_{xy} = \alpha + \beta = \frac{\partial u_y}{\partial x} + \frac{\partial u_x}{\partial y} = \gamma_{yx} \tag{2.10}$$

By expanding this definition in three dimensions, the strain can be related to the displacements by the following strain components:

$$\varepsilon_{xx}=\frac{\partial u}{\partial x},\ \varepsilon_{xy}=\varepsilon_{yx}=\frac{1}{2}\left(\frac{\partial u}{\partial y}+\frac{\partial v}{\partial x}\right)=\frac{1}{2}\gamma_{xy}=\frac{1}{2}\gamma_{yx}$$
$$\varepsilon_{yy}=\frac{\partial v}{\partial y},\ \varepsilon_{yz}=\varepsilon_{zy}=\frac{1}{2}\left(\frac{\partial v}{\partial z}+\frac{\partial w}{\partial y}\right)=\frac{1}{2}\gamma_{yz}=\frac{1}{2}\gamma_{zy} \tag{2.11}$$
$$\varepsilon_{zz}=\frac{\partial w}{\partial z},\ \varepsilon_{xz}=\varepsilon_{zx}=\frac{1}{2}\left(\frac{\partial u}{\partial z}+\frac{\partial w}{\partial x}\right)=\frac{1}{2}\gamma_{zx}=\frac{1}{2}\gamma_{xz}$$

where u, v, and w are the displacements in the x, y, and z directions, respectively. The results analogous to those of stress theory hold, and therefore the symmetric array of strain tensor (ε_{kl}) can be arranged as:

$$\varepsilon_{kl}=\begin{bmatrix}\varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz}\\ \varepsilon_{yx} & \varepsilon_{yy} & \varepsilon_{yz}\\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz}\end{bmatrix} \tag{2.12}$$

Similar to stress, only six independent components are required to then define the state of strain at a certain point:

$$\varepsilon^{T}=\begin{bmatrix}\varepsilon_{xx} & \varepsilon_{yy} & \varepsilon_{zz} & \varepsilon_{xy} & \varepsilon_{yz} & \varepsilon_{zx}\end{bmatrix} \tag{2.13}$$

2.1.2 Stress-Strain Relationship

The relationship between the stress tensor and the deformation is known as a constitutive relation. All structural materials possess the property of elasticity. When the force is removed, the body will return to its original shape if it is an ideal elastic body and it had not reached its yield stress. For an elastic solid, the stress tensor is linearly proportional to the strain tensor over a specific range of deformation:

$$\sigma_{ij}=c_{ijkl}\varepsilon_{kl} \tag{2.14}$$

where c_{ijkl} is the tensor of stiffness constants. In order to relate each of the nine elements of the second rank strain tensor to each of the nine elements of the second rank stress tensor, c_{ijkl} consists of a fourth rank tensor of 81 elements. However, due to the symmetries involved for

the stress and strain tensors under equilibrium, c_{ijkl} can reduce a tensor of 36 elements. Crystal silicon has diamond cubic crystal geometry resulting from its strong directional covalent bonds. For such crystals, c_{ijkl} has the following form due to their cubic symmetry:

$$c_{ijkl} = \begin{bmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44} \end{bmatrix} \tag{2.15}$$

Thus, for silicon the tensor of elastic stiffness constants reduces to the three independent components: c_{11}, c_{12}, and c_{44}. Of practical interest is the strain arising from a certain stress condition. The strain components can be obtained by inverting Hook's law and utilizing the compliance coefficients,

$$\varepsilon_{ij} = s_{ijkl}\sigma_{kl} \tag{2.16}$$

The stiffness and compliance tensors are linked through the above relation. Consequently, the three independent compliance coefficients can be calculated as [2.3],[2.4]

$$\begin{aligned} s_{11} &= \frac{c_{11} + c_{12}}{c_{11}^2 + c_{11}c_{12} - c_{12}^2} \\ s_{12} &= \frac{c_{12}}{c_{11}^2 + c_{11}c_{12} - c_{12}^2} \\ s_{44} &= \frac{1}{c_{44}} \end{aligned} \tag{2.17}$$

The compliance coefficients for Si, together with the stiffness coefficients, are listed in Table 2.1 [2.5].

2.2 Strain-induced Energy Splitting

The effect of stress on the resistivity of Si was first investigated by Smith [2.6]. This finding was contributed to the modification of the electronic band structure. Microscopically, stress breaks the symmetry of lattice which can then cause the energy shift and band distortion. In the following these effects are discussed in detail.

Deformation potential theory originally developed by Bardeen and Shockley [2.7] was used to investigate the interaction of electrons with acoustic phonons. It was later generalized to include different scattering modes by Herring and Vogt [2.8]. The technique was applied to strained systems by Bir and Pikus [2.9].

Within the framework of this theory, the energy shift of a band extremum l is expanded in terms of the components of the strain tensor ε_{ij}.

$$\Delta E^{(l)} = \sum_{ij} \Xi_{ij}^{(l)} \varepsilon_{ij} \tag{2.18}$$

The coefficients of this expansion are called the deformation potential tensor. This tensor is characteristic of a given non-degenerate band in the solid. The symmetry of the strain tensor is also reflected in that of the deformation potential tensor, giving

$$\Xi_{ij}^{(l)} = \Xi_{ji}^{(l)} \tag{2.19}$$

The maximum number of independent components of this tensor is six which can reduce two or three for a cubic lattice. They are usually denoted by Ξ_u, the uniaxial deformation potential constant, and Ξ_d, the dilatation deformation potential constant. The deformation potential constants can be calculated using theoretical techniques such as density functional theory [2.10], the non-local empirical pseudo-potential method [2.11], or ab-initio calculations. However, a final adjustment of the potentials is obtained only after comparing the calculated values with those obtained from measurement techniques [2.12]–[2.14]. The deformation potential constants used in this work are listed in Table 2.1 [2.15].

The general form of the strain-induced energy shifts of the conduction band valleys for an arbitrary strain tensor can be written as

$$\Delta E_C^{(i,j)} = \Xi_d^{(j)} Tr(\varepsilon) + \Xi_u^{(j)} a_i^T \cdot \varepsilon \cdot a_i \tag{2.20}$$

where a_i is a unit vector of the *i*th valley minimum for the *j*th valley type. The first term in Eq. (2.20) shifts the energy level of all the valleys equally and is proportional to the hydrostatic strain. The difference in the energy levels of the valleys arises from the second term in Eq. (2.20). In this method, strain effect only shifts the band edge while it does not cause the band warping. In this study, the stress along <110> direction on (001) surface can first be transformed into strain. Then, by applying Eq. (2.20), the quantities of band shift for Δ_2 and Δ_4 valley can be expressed as

$$\begin{aligned} \Delta E_{c,\Delta_2} &= (\Xi_d + \frac{\Xi_u}{3})(S_{11} + 2S_{12})\sigma + (\frac{\Xi_u}{3})(S_{12} - S_{11})\sigma \\ \Delta E_{c,\Delta_4} &= (\Xi_d + \frac{\Xi_u}{3})(S_{11} + 2S_{12})\sigma - (\frac{\Xi_u}{6})(S_{12} - S_{11})\sigma \end{aligned} \tag{2.21}$$

It is noteworthy that the approximation is reasonable under moderate stress [2.16] while it may need to include the effect band warping for large stress because of the strong influence of effective mass change.

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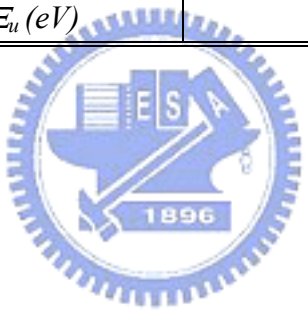
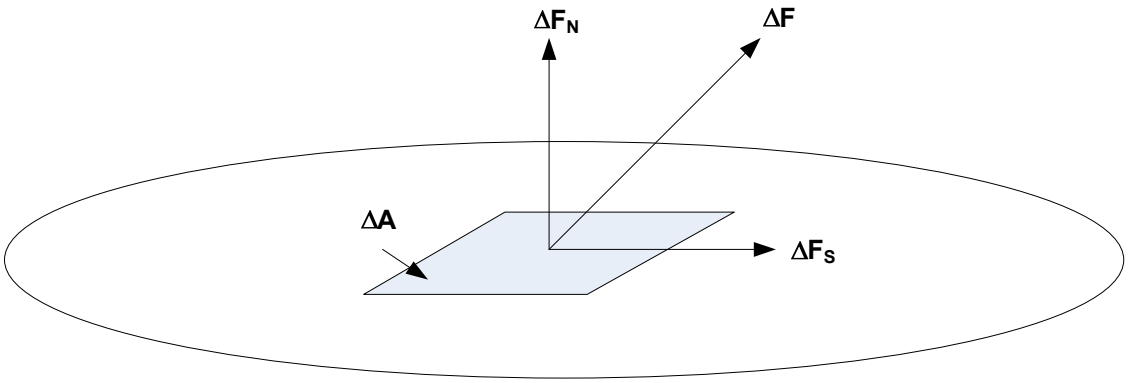
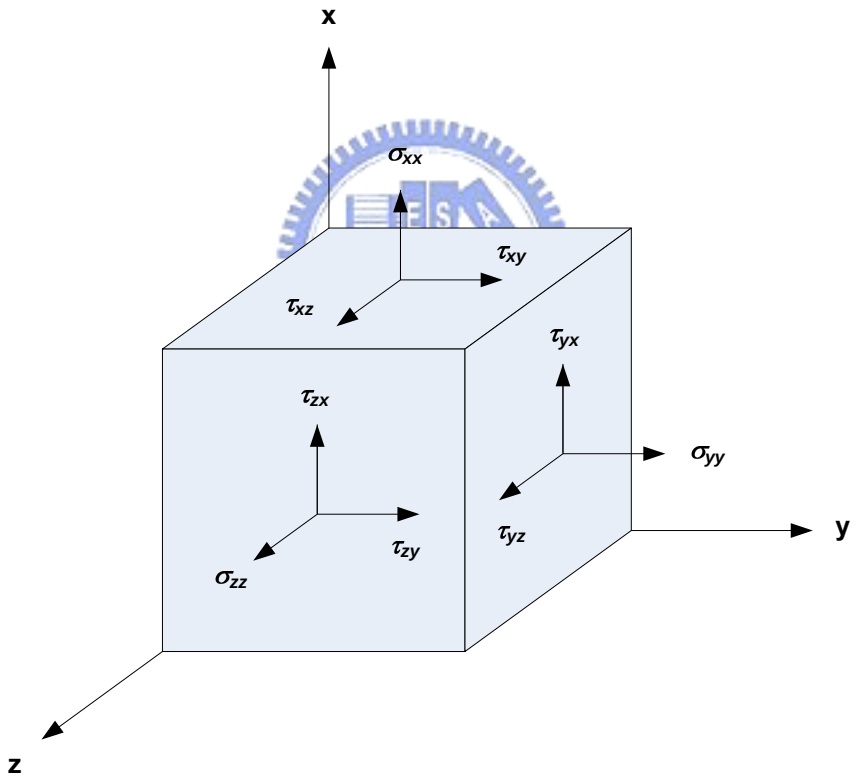
Table 2.1 Compliance and stiffness coefficients, Luttinger parameters, deformation potential constants, and split-off energy for silicon.

Stiffness Coefficients	
c_{11} (10^{12}dyne/cm^2)	1.657
c_{12} (10^{12}dyne/cm^2)	0.639
c_{44} (10^{12}dyne/cm^2)	0.796
Compliance Coefficients	
s_{11} (10^{-12}m^2/Nt)	7.68
s_{12} (10^{-12}m^2/Nt)	-2.14
s_{44} (10^{-12}m^2/Nt)	12.6
Deformation Potential Constants	
Ξ_d (eV)	1.13
Ξ_u (eV)	9.16





(a)



(b)

Fig. 2.1 (a) Schematic of an arbitrary force ΔF acting on an infinitesimal area ΔA, along with the resolved components: normal ΔF_N and shear terms ΔF_S. (b) A cubic element located within a continuous body with stress tensor components shown.

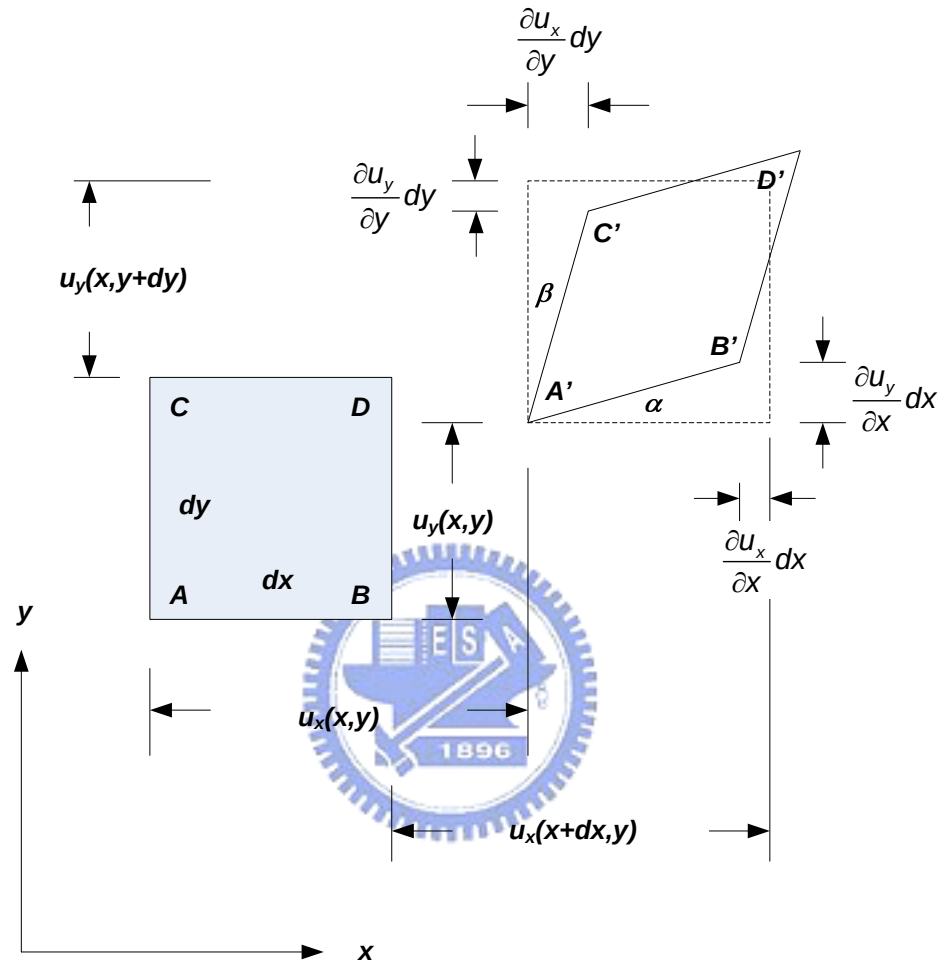


Fig. 2.2 Two-dimensional geometric deformation of an infinitesimal material element.

Chapter 3

Measurement of Channel Stress Using Gate Direct Tunneling Current in Uniaxially Stressed *n*-MOSFETs

3.1 Introduction

It is well recognized that the mechanical stress in MOSFETs can significantly affect many electrical properties such as the mobility [3.1]–[3.3], the hot carrier immunity [3.4], the threshold voltage [3.5], and the gate direct tunneling current [3.6]–[3.8]. Thus, the ability to quantitatively determine the magnitude of the underlying mechanical stress, as well as its status (compressive or tensile), is essential. Three fundamentally different methods have been introduced in this direction: (i) wafer bending jig [3.9]; (ii) sophisticated stress simulation [3.10]; and (iii) Raman spectroscopy [3.11]. Obviously, the *electrical* approach to the mechanical stress was lacking to date. However, it is noteworthy that the gate direct tunneling current has been well studied under externally applied mechanical stress [3.6]–[3.8]. Particularly in the citation [3.8], the deformation potential constants [3.12]–[3.14] have been experimentally determined with the values consistent with theoretical works [3.15]. Therefore, with known deformation potential constants, it is plausible to measure mechanical stress by means of the gate direct tunneling current.

In this chapter, we show how to transform the gate direct tunneling current in stressed devices into the value of the stress, achieved without adjusting any parameters. Confirmative evidence is presented in terms of the piezoresistance coefficient electrically created on the

same device.

3.2 Experiment

The n^+ poly-silicon gate *n*-MOSFETs were fabricated in a state-of-the-art manufacturing process. The device process flow is depicted in Fig. 3.1. Also plotted in the Fig. 3.2 are the schematic cross section and topside view of the test device. Three key process parameters were obtained by capacitance-voltage (C−V) fitting: n^+ poly-silicon doping concentration = 1×10^{20} cm^{-3}, gate oxide thickness = 1.27 nm, and substrate doping concentration = 4×10^{17} cm^{-3}. In this process, the STI induced compressive stress was applied. The gate length along the <110> direction is 1 μm large enough that the following effects can be effectively eliminated: external series resistance and short channel or drain induced barrier lowering (DIBL). The gate width is wide (10 μm), indicating that the transverse stress is relatively negligible. Layout technique was utilized to produce a variety of stress in terms of the gate edge to STI sidewall spacing, designated *a*, with four values of 10, 2.4, 0.495, and 0.21 μm. A decrease in *a* means increased magnitude of longitudinal stress. A considerable number of contacts were formed on the source/drain diffusion along the gate width direction, far away from the STI in the <110> direction. The spacing between the diffusion contact and the gate edge is fixed in this work. It has been reported that silicide can introduce stress into channel and its effect can be eliminated by well controlling the silicide formation [3.10]. Thus, the silicide process was fine tuned for the device under study to minimize its effect as compared with STI stress.

The gate direct tunneling current was measured in inversion conditions with the source, drain, and substrate all tied to ground. Also characterized was the mobility on the same device at V_d = 25 mV. The change of the conduction-band electron direct tunneling current at V_g = 1

V and the mobility at V_g = 0.5 V, all with respect to a = 10 μm, are plotted in Fig. 3.3 versus gate to STI spacing. It can be seen that a decrease in the gate to STI spacing can produce an increase in both the gate current while degrading the mobility.

3.3 Stress Extraction

Existing direct tunneling models [3.16], [3.17] on the basis of the triangular potential approximation [3.18] in the channel, taking into account the poly-silicon depletion, can readily apply with some slight modifications such as incorporating stress dependencies of the subbands. The electrons in inversion primarily populate the two lowest subbands [3.8]: one of the two-fold valley Δ_2 and one of the four-fold valley Δ_4. The corresponding stress dependencies are well defined in the literature [3.8], [3.12]–[3.14]:

$$E_{\Delta 2}(\sigma) = \left(\frac{9hqE_{eff,\Delta 2}}{16\sqrt{2m^*_{\Delta 2}}}\right)^{\frac{2}{3}} + \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11} + 2S_{12})\sigma + \left(\frac{\Xi_u}{3}\right)(S_{12} - S_{11})\sigma \tag{3.1}$$

$$E_{\Delta 4}(\sigma) = \left(\frac{9hqE_{eff,\Delta 4}}{16\sqrt{2m^*_{\Delta 4}}}\right)^{\frac{2}{3}} + \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11} + 2S_{12})\sigma - \left(\frac{\Xi_u}{6}\right)(S_{12} - S_{11})\sigma \tag{3.2}$$

where the quantization effective masses $m^*_{\Delta 2}$ = 0.92 m_0 and $m^*_{\Delta 4}$ = 0.19 m_0; and the elastic compliance constants S_{11} = 7.68 × 10^{-12} m^2 /N and S_{12} = −2.14 × 10^{-12} m^2/N. The hydrostatic and shear deformation potential constants Ξ_d = 1.13 eV and Ξ_u = 9.16 eV [3.5], close to those of Ref. [3.8], were cited here. Stress along <110> direction can be resolved into two different components: normal and shear stress terms in <100> coordination. Shear terms can cause the band distortion, which in turn, influences the effective mass. This effect becomes significant when applied strain approaches 1% and beyond, whose magnitude is much greater than that in our study case. Thus, it is reasonable to assume that effective mass change can be neglected under moderate stress in the subsequent calculation. One of the expressions for the effective

electric field E_{eff} can be found elsewhere [3.8]. With the aforementioned process parameters as input, the two lowest subband levels with respect to the Fermi level E_f can be determined. The stress dependencies of the lowest subbands under different gate voltages were found to be consistent with those in earlier works [3.8]. The inversion-layer carrier density per unit area can further be calculated by $N_i = (k_B T / \pi\hbar^2) g_i m_{di} \ln(1 + \exp((E_f - E_i) / k_B T))$ [3.16]–[3.18], where the subscript i denotes Δ_2 or Δ_4, $k_B T$ is the thermal energy, g_i is the degeneracy of the valley, and m_{di} is the density of state effective mass. It is then a straightforward task to calculate the WKB tunneling probability, taking into account the corrections for reflections from the potential discontinuities [3.19]. Here the electron effective mass in the oxide for the parabolic type dispersion relationship was used with $m_{ox} \sim 0.50\ m_0$, which is equivalent to $m_{ox} = 0.61\ m_0$ for the tunneling electrons in the oxide using the Franz type dispersion relationship [3.20]. The oxide can be thought of as an amorphous material. The irregular arrangement of oxide atoms makes its band structure and the electron tunneling effective mass in this layer difficult to be determined, especially for the strain condition. The theoretical calculation or experimental extraction of tunneling mass considering stress effect was still lacking. Thus, in this work, we assume that the electron effective mass in the oxide remains unchanged with stress varying. This assumption works well in predicting the strain-induced gate tunneling current [3.8]. The SiO_2/Si interface barrier height in the absence of stress is 3.15 eV. Consequently, without adjusting any parameters, the conduction-band electron direct tunneling current density can be calculated as a function of the stress σ [3.8]:

$$I_g(\sigma) = \frac{qN_{\Delta 2}(\sigma)}{\tau_{\Delta 2}(\sigma)} + \frac{qN_{\Delta 4}(\sigma)}{\tau_{\Delta 4}(\sigma)} \tag{3.3}$$

The tunneling lifetime in Eq.(3.3) can be related to the transmission probability T: $\tau_{\Delta 2}(\sigma) = \pi\hbar/(T_{\Delta 2}(\sigma)E_{\Delta 2}(\sigma))$ and $\tau_{\Delta 4}(\sigma) = \pi\hbar/(T_{\Delta 4}(\sigma)E_{\Delta 4}(\sigma))$.

With the above approach, we found that the uniaxial channel stress of around 0, ~0, -120,

and -280 MPa for gate to STI spacing of 10, 2.4, 0.495, and 0.21 μm, respectively, can reproduce gate direct tunneling current versus gate voltage characteristics. The corresponding gate current change is plotted in Fig. 3.4 versus extracted channel stress with gate voltage as a parameter. It can be seen that the magnitude of the gate current change increases linearly with the stress, consistent with those published elsewhere [3.8]. Again in agreement with the citation [3.8], the slope of the straight line in Fig. 3.4 increases with decreasing gate voltage. This trend also points out that the accuracy of the proposed method can be considerably improved by lowering gate voltages.

3.4 Confirmative Evidence

The measured mobility change percentage versus extracted stress is shown in Fig. 3.5. The straight line through the data points yields the slope or piezoresistance coefficient of -33.5×10^{-12} dyne^{-1} cm^2, close to that (-31.5×10^{-12} dyne^{-1} cm^2) in the literature [3.21].

To testify to the layout technique mentioned above, we quote existing relationship between the effective channel stress and the gate to STI spacing, which was derived from the stress simulation [3.10]:

$$\sigma(a) = \sigma(a_{\min})(1 + V_{m\sigma}\frac{a - a_{\min}}{a}) \tag{3.4}$$

where $a_{\min}$ represents a minimum gate to STI spacing and V_m is the maximum $\sigma(a)$ variations (i.e. when $a \rightarrow \infty$) with respect to $\sigma(a_{\min})$. The extracted stress can be adequately described by Eq. (3.4) with $V_{m\sigma} = -1.05$, as demonstrated in Fig. 3.6. Indeed, the projected stress for a = 10 μm, the reference point mentioned above, approaches zero. Therefore, the layout technique holds true in this work.

Finally, the electrical method accompanied with the layout technique was also applied to

other devices (with a sample size of 10) on the same wafer. The corresponding stress-induced variations in gate direct tunneling current were found to be comparable with those in Fig. 3.4.

3.5 Conclusion

With known process parameters and published deformation potential constants as input, fitting of gate direct tunneling current versus gate voltage data has led to the value of the underlying channel stress. A link with the mobility measurement on the same device has been conducted. The resulting piezoresistance coefficient has been in good agreement with literature values. The layout technique has also been validated.

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Fig. 3.1 Device formation process flow.

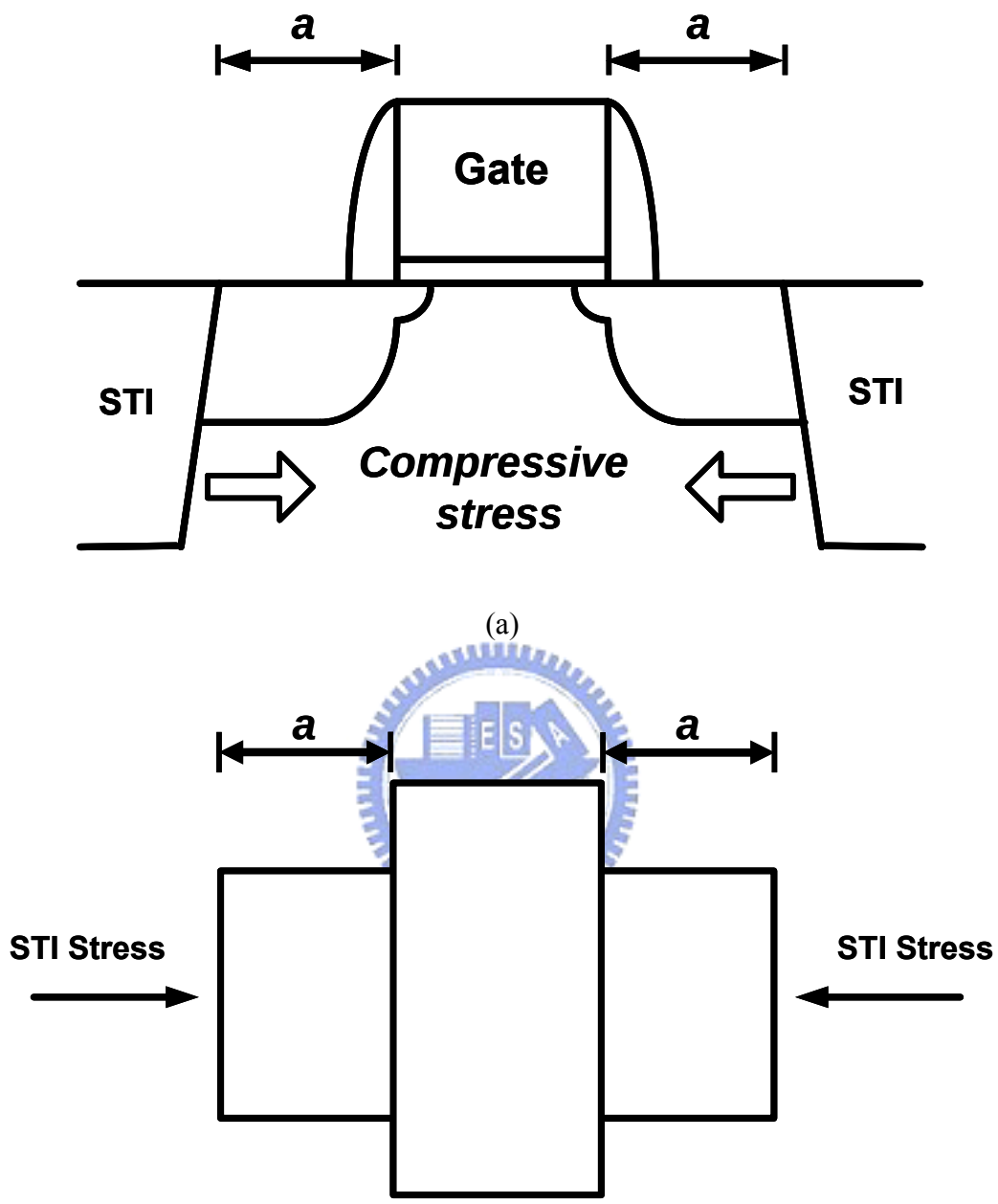

Fig. 3.2 (a) Schematic cross section and (b) topside view of the device under study. The gate edge to STI sidewall, *a*, is highlighted. The stress condition is compressive due to the lower thermal expansion rate of STI oxide compared to silicon.

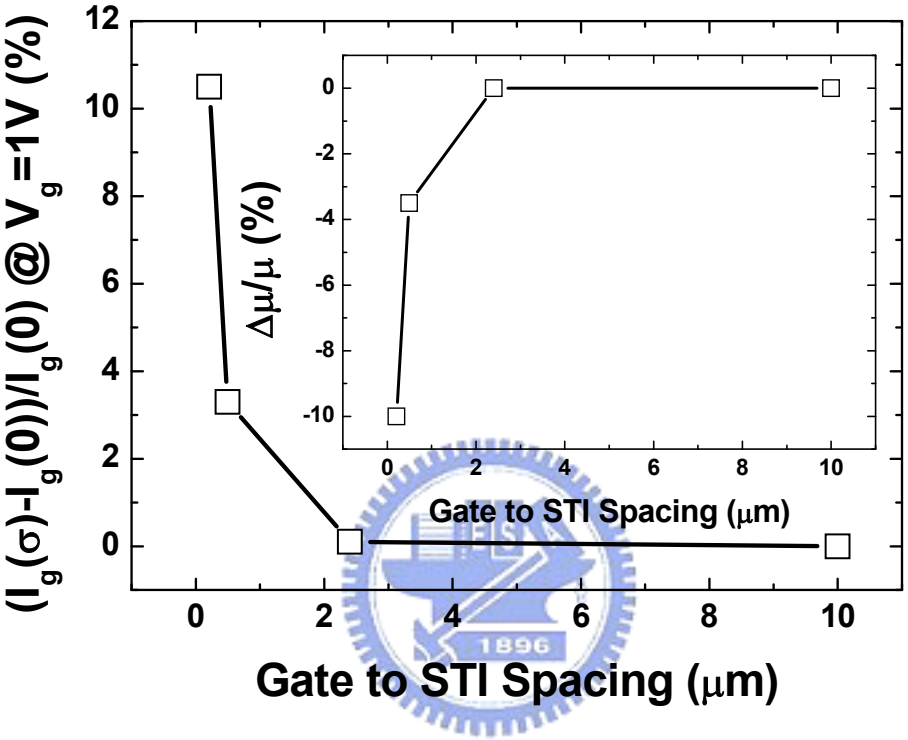

Fig. 3.3 The relative change of the gate direct tunneling current at V_g = 1V versus gate to STI spacing. The inset shows the mobility variations versus the gate to STI spacing.

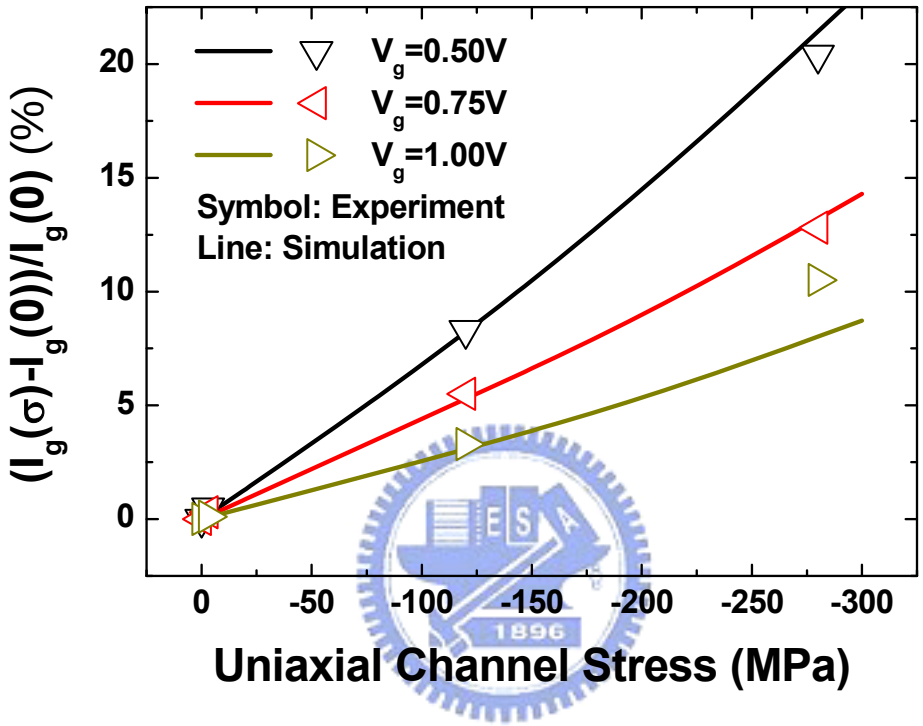

Fig. 3.4 The relative change of the gate direct tunneling current versus extracted uniaxial compressive channel stress for V_g = 0.5, 0.75, and 1V. The symbols are experimental data. The fitting line is drawn only for accommodating the trend.

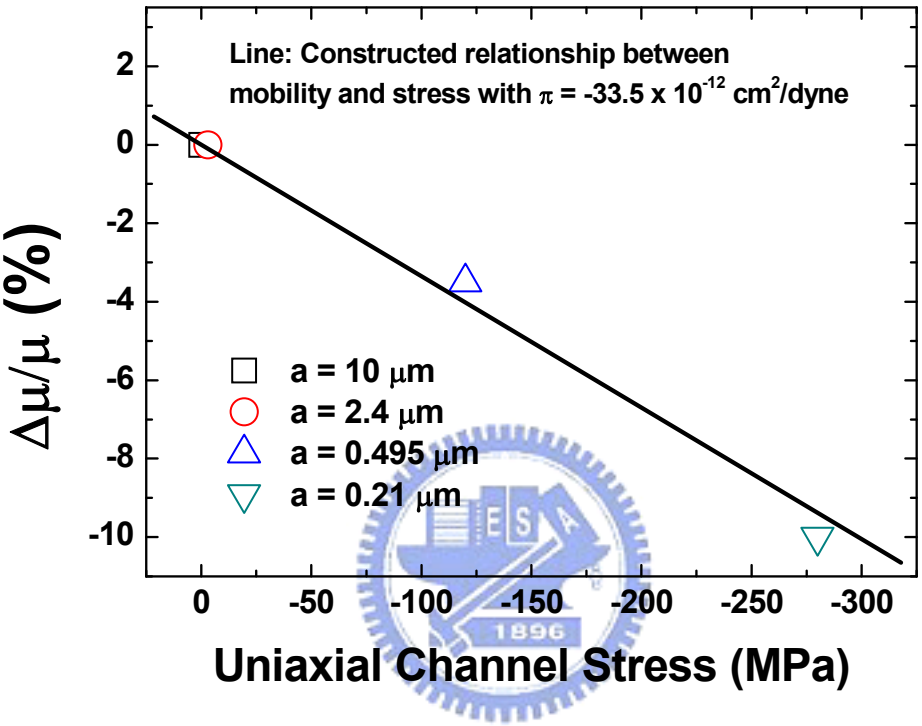

Fig. 3.5 The measured mobility change versus extracted stress. Fitting the data yields the value of piezoresistance coefficient π = -33.5 × 10 $^{-12}$ dyne^{-1} cm^2.

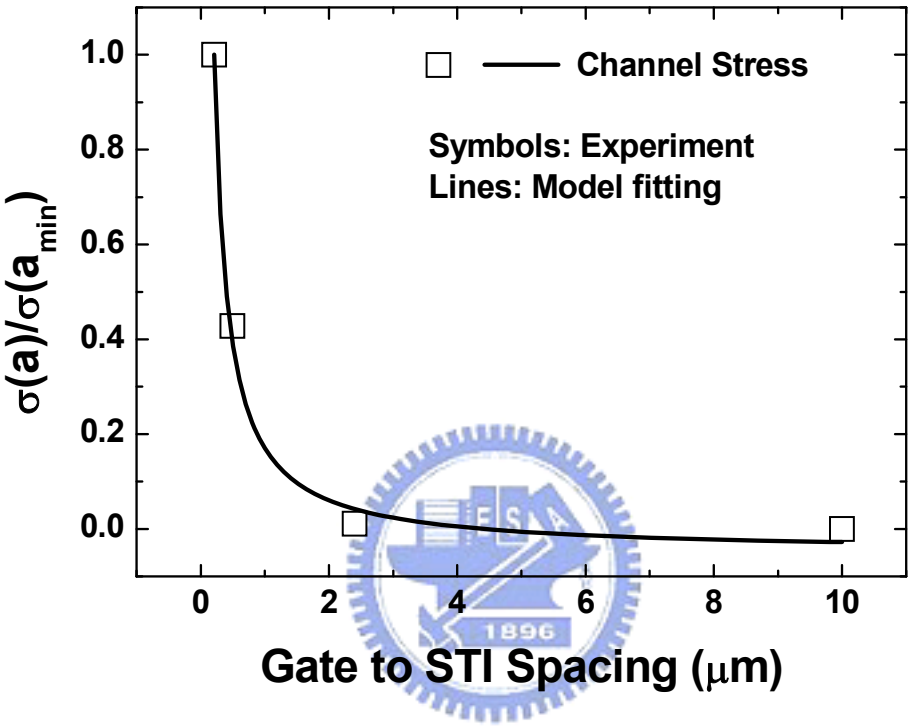

Fig. 3.6 The extracted stress, divided by that of the minimum *a*, versus the gate to STI spacing, along with a fitting curve from Eq. (3.4).

Chapter 4

Distinguishing Between STI Stress and Delta Width in Gate Direct Tunneling Current of Narrow n-MOSFETs

4.1. Introduction

The significance of the shallow trench isolation (STI) induced mechanical stress in highly scaled MOSFETs has been widely recognized [4.1]. The linkage between layout design and the underlying STI stress has also been well constructed [4.2]-[4.4]. Further applications pertaining to the layout dependencies of the STI stress altered dopant diffusion [4.5],[4.6], gate direct tunneling [4.6],[4.7], threshold voltage [4.6]-[4.8], subthreshold leakage [4.6],[4.8], and mobility [4.2],[4.4],[4.6],[4.7], have all been successfully demonstrated. However, care must be taken especially in the narrowing direction. The reasons are that on the one hand, the STI channel stress can be enhanced; however, on the other hand, the delta width ΔW due to STI corner rounding as schematically shown in Fig. 4.1 is of increasing importance. Thus, the ability to distinguish the delta width effect from the STI stress effect is essential. Two such examples on the drain current variation have recently been published [4.9],[4.10]. However, so far, effects on the gate direct tunneling current counterpart were not yet addressed in the open literature. In this work, we elaborate on how to unambiguously elucidate the STI stress altered gate direct tunneling current measured in the presence of n-MOSFET narrowing.

4.2 Experiment

The n^+ poly-silicon gate n-MOSFETs on (001) wafer were fabricated in a state-of-the-art manufacturing process. Three key process parameters were obtained by a capacitance-voltage (C−V) fitting: n^+ poly-silicon doping concentration = 1×10^{20} cm^{-3}, gate oxide thickness = 1.27 nm, and channel doping concentration = 3×10^{17} cm^{-3}. In this process, STI induced compressive stress was applied. The gate length L, the gate edge to STI spacing in source diffusion, and the gate edge to STI spacing in drain diffusion, all in the channel length direction <110>, were fixed at the same value of 0.5 μm. The gate edge to STI spacing in the source diffusion is equal to that of the drain: The cross-sectional view of the test device is schematically shown in Fig. 4.1. The gate width W spanned in a wide range of 0.11, 0.24, 0.6, 1.0 and 10 μm. The gate direct tunneling current was measured in inversion with the source, drain, and substrate all tied to the ground. The change percentage of the *apparent* gate current per unit width, namely the actual gate current divided by corresponding W, with respect to W = 10 μm, is plotted in Fig. 4.2 for V_g = 1 V versus W.

4.3 Data Fitting and Parameter Extraction

As illustrated in Fig. 4.1, the actual channel width designated W_{eff} is the drawn gate width plus the delta width: $W_{eff} = W + \Delta W$. The corresponding stress altered gate tunneling current density can be expressed as a linear function of both the average longitudinal channel stress σ_x and the average transverse channel stress σ_y , which was obtained via a triangular potential based quantum simulation while incorporating the longitudinal and transverse stress dependencies of the subbands [4.11]:

$$\frac{\dfrac{I_g(\sigma)}{W+\Delta W}-\dfrac{I_g(0)}{W_{ref}+\Delta W}}{\dfrac{I_g(0)}{W_{ref}+\Delta W}}=a_x\sigma_x+a_y\sigma_y \tag{4.1}$$

Here the proportionality constants a_x and a_y both are equal to -2.9 × 10^{-10} m^2/Nt. The same proportionality constant value was also utilized in our previous work concerning the longitudinal channel stress [4.6],[4.7]. On the basis of the two-dimensional STI stress distributions [4.3],[4.10], a certain relationship can be found: $\sigma_y = k \log(W/W_{ref})$, where k is constant. Since only for sufficiently small W can the gate current variation be significantly noticed, the transverse channel stress at reference W_{ref}(=10 μm) can be reasonably ignored.

By substituting the above logarithm form into (4.1), a new analytic model for the *apparent* gate tunneling current change can be straightforwardly derived:

$$\frac{\Delta J_{g,app.}(\sigma)}{J_{g,app.}(\sigma_{ref})}=\frac{\dfrac{I_g(\sigma)}{W}-\dfrac{I_g(\sigma_{ref})}{W_{ref}}}{\dfrac{I_g(\sigma_{ref})}{W_{ref}}}=\frac{1+a_x\sigma_x+a_y k\log\dfrac{W}{W_{ref}}}{1+a_x\sigma_x}\frac{W+\Delta W}{W_{ref}+\Delta W}\frac{W_{ref}}{W}-1 \tag{4.2}$$

Here, the reference stress σ_{ref} corresponds to a fixed longitudinal stress under which the data were measured. First of all, according to the previous work [4.6],[4.7], σ_x under the same gate to STI spacing (= 0.5 μm, taking into account the effect of the source/drain diffusion regions) was estimated to be -107 MPa. Then, least-squares fitting using (4.2) produced k = 130 MPa and ΔW = 58 nm. The fitting quality is excellent in a wide range of W, as shown in Fig. 4.2. The extracted ΔW is close to that of the existing simulated device structure in the same manufacturing process (see Fig. 5 of Ref. [4.3]). Therefore, in our work the logarithmic form is a good approximation for W down to 0.11 μm, comparable with that (0.15 μm in the drain current fitting) of the citation [4.10]. Further calculations were conducted for the two cases: (i) stress only, namely Eq.(4.2) with ΔW = 0 and (ii) delta width only or Eq.(4.2) with σ_x = 0 and k = 0. The results are together plotted in Fig. 4.2 for comparison. It can be seen that the delta width effect dominates over the stress effect in the narrow devices, while for the wide ones,

they are comparable. Note that both effects are co-operative in constituting gate current variation.

Obviously, ΔW is the principal factor in the data fitting. Thus, under constraint of ΔW = 58 nm, we performed additional calculations for different values of k. The results are given in Fig. 4.3. Here, the uncertainty range of k between 70 and 200 MPa appears to ensure reasonable fitting. On the other hand, we changed σ_x to those between -70 and -200 MPa; however, no noticeable change in the calculation results (directly from (4.2)) can be found (not shown here). Note that if σ_x is much larger in magnitude than σ_y, Eq.(4.2) reduces to the case of delta width only. Further calculation was conducted concerning the possibility that the narrowing action in the transverse direction may affect σ_x, although the STI-to-STI spacing in the channel length direction has been fixed. The corresponding calculated gate current change for σ_x at W = 0.11 μm relative to σ_x (= -107 MPa) at W = 10 μm is given in Fig. 4.4. Fig. 4.4 reveals that the effect of varying σ_x due to the narrowing action on the fitting quality is considerably weak.

4.4 Confirmative Evidence and Discussion

Extra measurement of drain current was carried out on the same devices. The change percentage of the *apparent* drain current per unit width at V_d = 1V and V_g = 1V is inserted to Fig. 4.2. The existing piezoresistance coefficients were cited for the fractional mobility change [4.12]: $\Delta\mu(\sigma)/\mu(0) = \pi_x\sigma_x + \pi_y\sigma_y$ where π_x = -3.16 × 10^{-10} and π_y = -1.76 × 10^{-10} m^2/Nt. The measured threshold voltage shift was less than 5 mV, indicating that the gate voltage minus the threshold voltage V_{th} remains unchanged. Thus, according to the long-channel saturation drain current expression: $I_{dsat} = \mu C_{inv}(W+\Delta W)(V_g-V_{th})^2/2L$ where C_{inv} is the gate capacitance in inversion, another analytic model, having the same expression as

(4.2) but with a_x and a_y replaced by π_x and π_y, respectively, can be created for the *apparent* drain current variation. Although the mobility in near-equilibrium may be not the same as that in the saturation regime of operation, the same piezoresistance coefficients can essentially apply to the *relative* mobility change due to the applied mechanical stress. This argument remains reasonable for the long-channel devices as used in this work. The calculated results agree with data as shown in the Fig. 4.5. Analogous to gate current case, the measured drain current was separated into the delta width only and the channel stress only. However, these two distinct effects exhibit opposite trends. Again, the effect of varying σ_x due to the narrowing action appears to be weak, as demonstrated in Fig. 4.4.

4.5 Conclusion

We have systematically examined the delta width and channel stress effects on gate direct tunneling current of narrow n-MOSFETs under STI compressive stress. Both effects have been decoupled using a new analytic direct tunneling model. The validity of the extracted transverse channel stress and delta width has been confirmed. The effect of varying longitudinal channel stress due to the narrowing action has also been addressed. The corroborating evidence in terms of the drain current variation has further been established.

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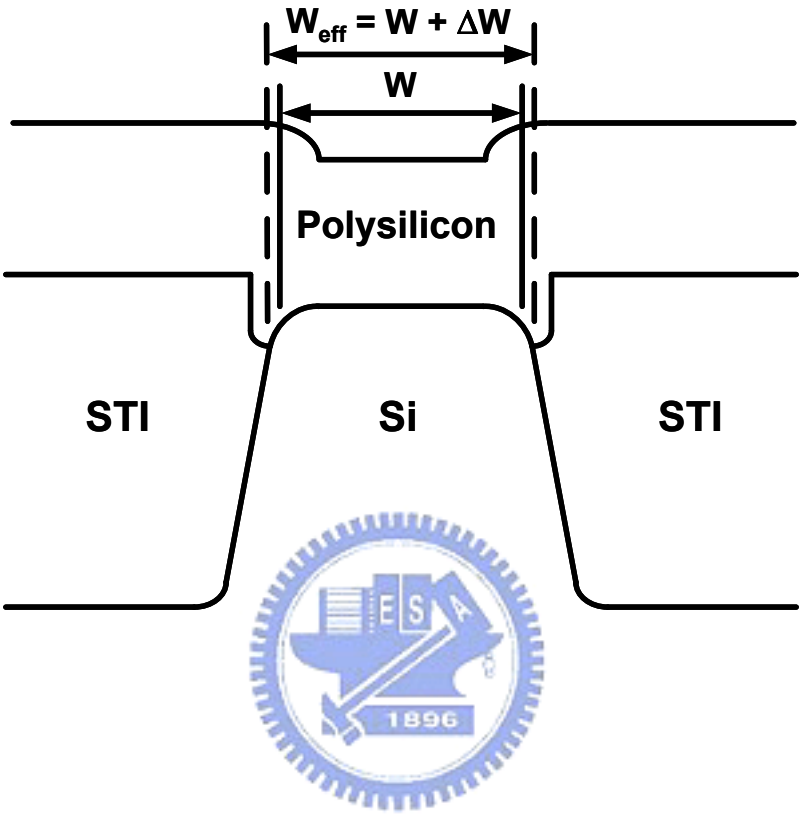

Fig. 4.1 The cross-sectional view of the device in the channel width direction, which can be schematically drawn from the existing simulated device structure in a state-of-the-art manufacturing process [4.3]. The effective channel width designated W_{eff} is the drawn width W plus the delta width ΔW.

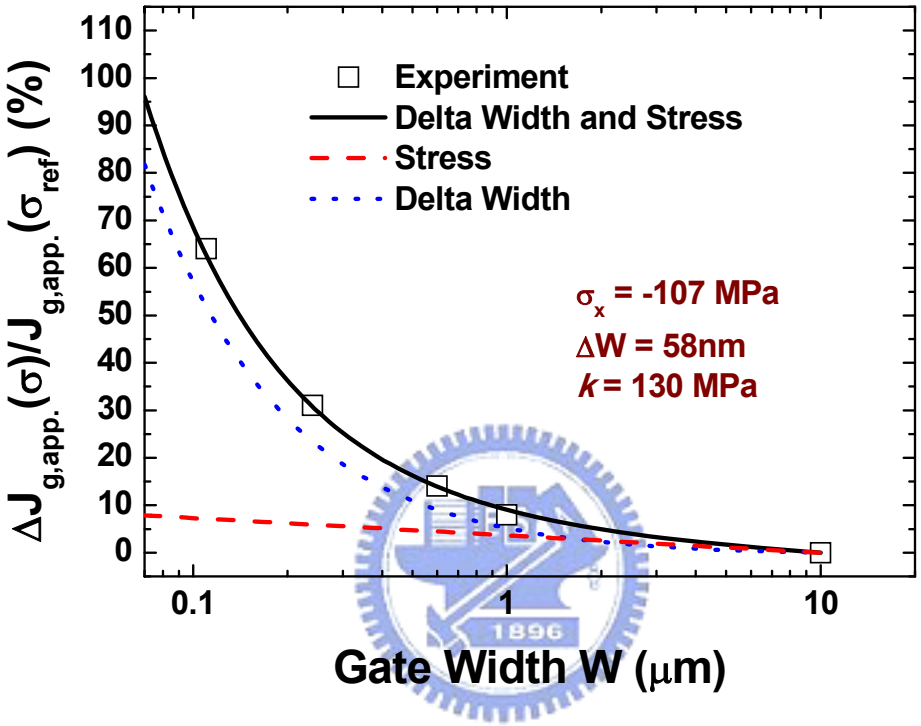

Fig. 4.2 The relative change of the *apparent* gate current per unit width at V_g = 1V versus drawn gate width. The lines represent the calculated results. It is worth noting that for the narrowest case W = 0.11 μm, the delta width effect contributes 52% while the remaining (7.3%) stems from the stress induced SiO_2/Si barrier lowering. The combination of both effects produces a 63% change in the *apparent* gate current density. For sufficiently large W, however, the delta width and channel stress effects become comparable. ΔW = 58 nm, σ_x = -107 MPa, and k = 130 MPa.

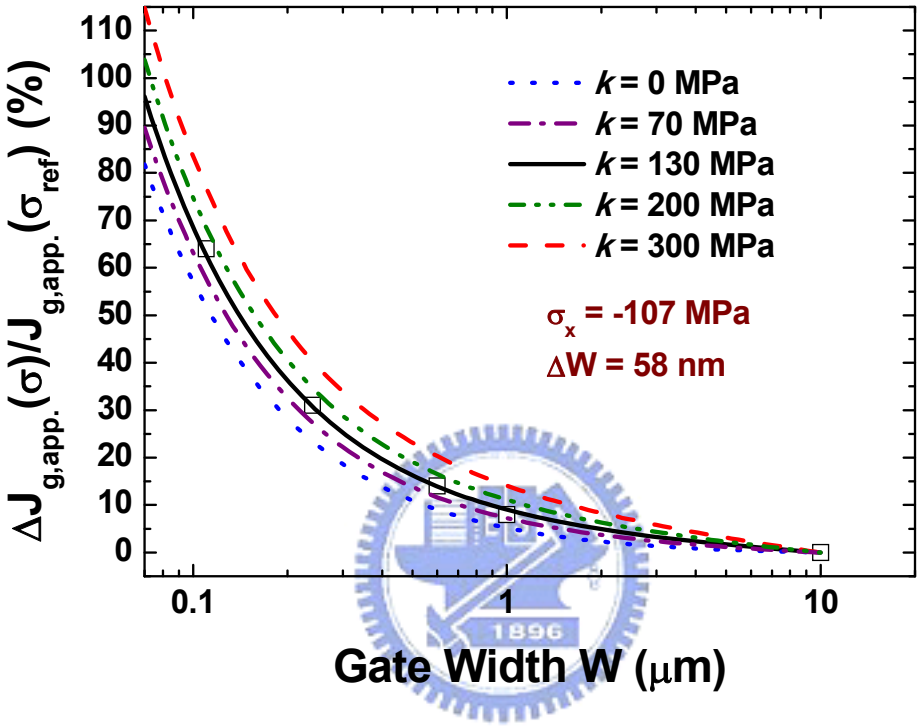

Fig. 4.3 Comparison of experimental data (symbols) corresponding to Fig. 4.2 with the calculated results. ΔW = 58 nm, σ_x = -107 MPa, and with k from 0 to 300 MPa.

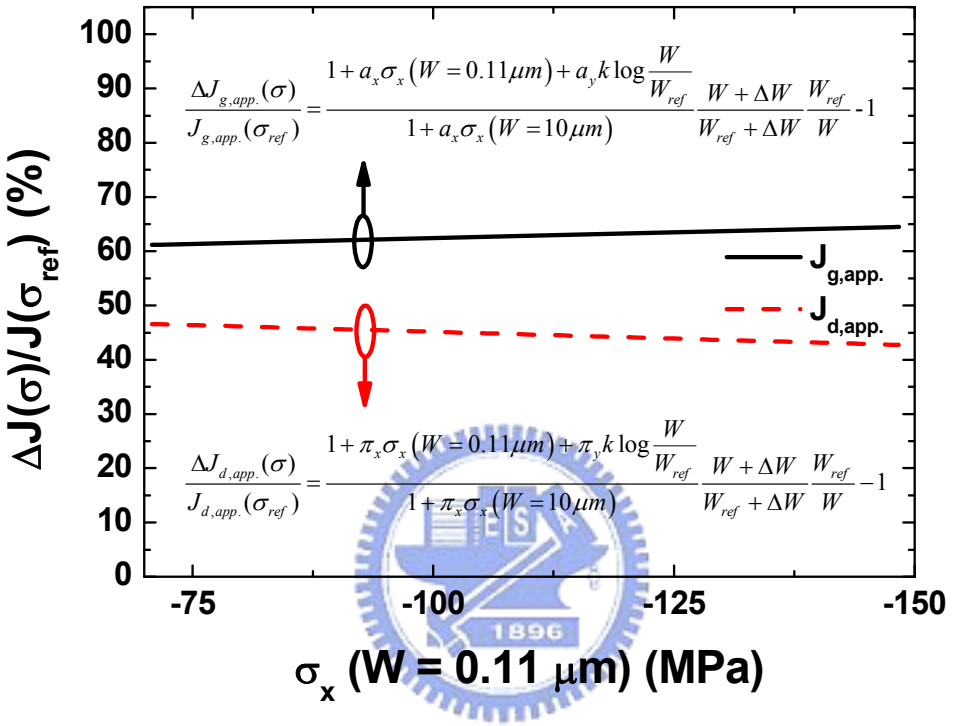

Fig. 4.4 Calculated gate and drain current change versus σ_x (from -70 to -150 MPa) at W = 0.11 μm relative to the nominal σ_x (= -107 MPa) at the reference W = 10 μm. The formulas used are inserted. ΔW = 58 nm and k = 130 MPa.

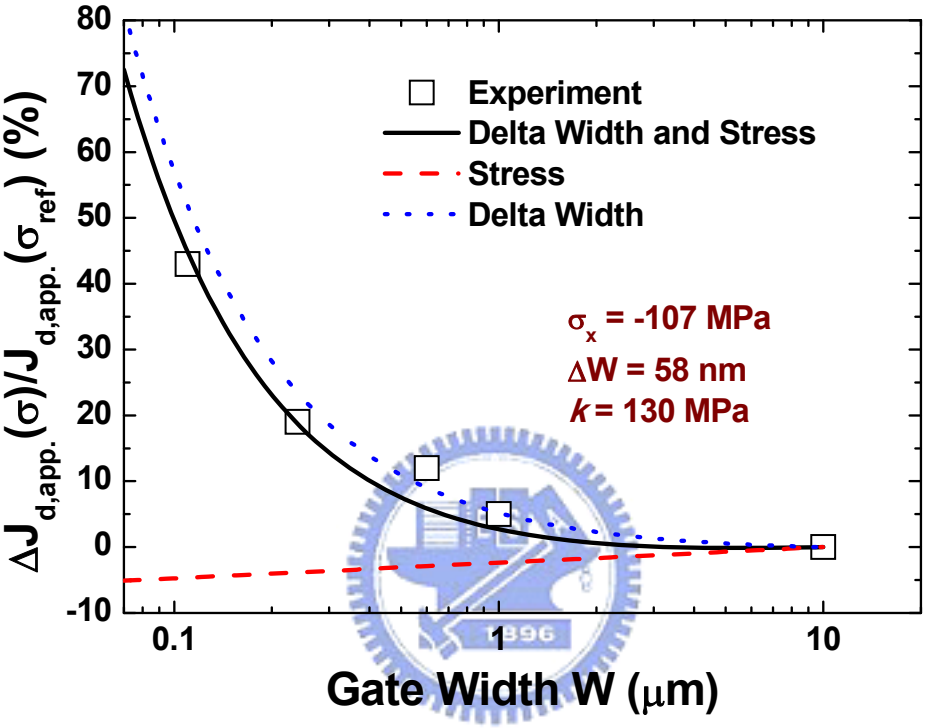

Fig. 4.5 The relative change of the *apparent* drain current per unit width at V_d = 1V and V_g = 1V versus drawn gate width, along with the calculated results. Note that the piezoresistance coefficients used are the typical bulk values, which are close to those of the inversion-layer ones of state-of-the-art strained n-MOSFETs [4.12], valid only for the channel <110> direction on (001) wafer as studied in this work.

Chapter 5

Electrical Measurement of Local Stress and Lateral Diffusion Near Source/Drain Extension Corner of Uniaxially Stressed *n*-MOSFETs

5.1 Introduction

Mechanical stress has been widely recognized to be one of the key issues in the area of highly scaled MOSFETs. So far, there have been two distinct directions concerning the significance of the mechanical stress. On the one hand, the mechanical stress experienced during the manufacturing process can enhance or retard the dopant diffusion, thereby influencing the final doping profile of the device. There have been significant studies with emphasis on the material aspect covering a wide range of experimental findings and confirmations [5.1]–[5.8], as well as the atomistic calculations and physical models [5.1], [5.9]–[5.12]. Extension to the actual devices has been achieved by means of the sophisticated device/process coupled simulation, namely the technology computer-aided design (TCAD) [5.10], [5.13], [5.14]. On the other hand, the presence of the mechanical stress can also alter the band structure of the formed device, which in turn can significantly affect properties such as mobility [5.15]–[5.17], hot carrier immunity [5.18], threshold voltage [5.19], and gate direct tunneling [5.20]–[5.23]. Besides the mentioned TCAD technique [5.10], [5.13], [5.14], there have been several methods applied on the formed devices with which the magnitude of the underlying stress and its status both can be determined: 1) wafer bending jig [5.24]; 2) stress/strain simulation and modeling [5.25]; 3) Raman spectroscopy [5.26]; and 4) gate direct

tunneling [5.23].

Indeed, the ability of tracing the electrical measurements on the formed devices back to the stress related dopant diffusion in the manufacturing process is essential. Traditionally, this was done with the TCAD method [5.10], [5.13], [5.14], as mentioned above. In this paper, we present the *electrical* approach to the local mechanical stress around the source/drain extension corner of uniaxially stressed *n*-MOSFETs, which can straightforwardly determine the underlying lateral diffusion. The validity of the proposed method will be addressed in detail.

5.2 Experiment

The detail of the test devices involving the fabrication process flow, key process parameters, and schematic cross section and topside view can all be found in Chapter 3.

5.3 Corner Stress Extraction and Validation

Measurement of the subthreshold current is adopted to quantify the mechanical stress around the source/drain extension diffusion corner. The measured subthreshold current change with respect to the reference device, namely a = 10 μm, is shown in Fig. 5.1, revealing a decreasing trend with decreasing gate-to-STI spacing. The subthreshold characteristics can be expressed as

$$I_{sub.} = \mu C_{ox} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 \exp\left(\frac{q(V_G - V_{th})}{mkT}\right)\left(1-\exp\left(\frac{-qV_D}{kT}\right)\right) \qquad (5.1)$$

where μ is the mobility, C_{ox} is the gate oxide capacitance per unit area, W and L represent the channel width and length, respectively, V_{th} is the threshold voltage, kT is the thermal energy,

and m is the body effect coefficient with a value between 1.3 and 1.4. Under same gate bias and large drain voltage, the difference of subthreshold current can be rearranged as follow

$$\ln\left(1+\frac{I_{sub.}\Delta(\sigma)}{I_{sub.}(0)}\right)=\ln\left(1+\frac{\Delta\mu(\sigma)}{\mu(0)}\right)-\frac{\Delta V_{th}(\sigma)}{mkT} \tag{5.2}$$

Thus, with the measured subthreshold current change and threshold voltage shift as shown in Fig. 5.2 can the mobility variations be directly resulted. By means of piezoresistance coefficient, the corresponding corner stress can be obtained as demonstrated in Fig. 5.3. Since the subthreshold current is mainly affected by the source to channel barrier, it is inferred that the calculated stress must be located around the source/drain corner.

The extracted corner stress is found to be comparable with those of the channel as created by other electrical measurements on the same device. First, by incorporating the stress dependencies of quantized energies [5.22], [5.23], [5.27]–[5.29] into a triangular potential method [5.30] in the channel, a WKB tunneling approach [5.31] was adopted to quantify the conduction-band electron direct tunneling current. As a consequence, the uniaxial channel stress of 0, ~0, -120, and -280 MPa was extracted for gate to STI spacing of 10, 2.4, 0.495, and 0.21 μm, respectively, each of which can reproduce experimental gate direct tunneling current versus gate voltage characteristics. The detailed extraction process can be found in Chapter 3. The corresponding gate current change is plotted in Fig. 3.4 versus extracted channel stress with gate voltage as a parameter. It was found that 2-fold subband Δ_2 lies a few kT below four-fold subband Δ_4 at high gate voltages and therefore electrons primarily populate Δ_2 whereas for low gate voltages, electrons populate both Δ_2 and Δ_4. Hence, at low gate voltages, stress not only gives rise to a change in barrier height but also an increased population in Δ_4. This effect becomes weakened for high gate voltages due to the dominating Δ_2 electrons. As a result, the gate current change due to the stress increases with decreasing gate voltage (refer to [5.22] for the detailed interpretations). Second, the mobility at V_D = 25

mV was characterized. The measured mobility change percentage versus extracted stress is shown in Fig. 3.5. A straight line used to fit the data points yields the slope or piezoresistance coefficient of -33.5 × 10 $^{-12}$ dyne^{-1} cm^2, close to that (-31.5 × 10 $^{-12}$ dyne^{-1} cm^2) in the literature [5.2]. The inset depicts the corresponding mobility change as a function of the gate edge to STI spacing.

Finally, to testify to the validity of the layout technique, we quote existing relationship between the effective stress and the gate to STI spacing, which was derived from the stress simulation [5.25]:

$$\sigma(a) = \sigma(a_{\min})(1 + V_{m\sigma}\frac{a - a_{\min}}{a}) \tag{5.3}$$

where $a_{\min}$ represents the minimum gate to STI spacing and $V_{m\sigma}$ is the maximum $\sigma(a)$ variations (i.e. when $a \rightarrow \infty$) with respect to $\sigma(a_{\min})$. Evidently, as displayed in Fig. 5.4, the extracted channel stress and corner stress for a given gate to STI spacing are close to each other, indicating that the stress distribution beneath the gate oxide is considerably uniform. In addition, the corner stress follows the same trend as the channel counterpart. The resulting $V_{m\sigma}$ values are comparable as well: -1.05 for the channel stress and -1.02 for the corner stress. Good fitting quality in both stress cases confirms the validity of the layout technique in *controlling* the stress.

5.4 Lateral Diffusion Extraction and Confirmation

The electron direct tunneling from the accumulated poly-silicon surface down to the underlying silicon was measured versus negatively biased gate voltage with the source, drain, and substrate all tied to the ground. It can be seen in Fig. 5-5 that the resulting substrate current, which essentially is equal to the electron gate to substrate tunneling current, increases

with decreasing a. Such dependency reflects the increasing magnitude of lateral compressive stress in the poly-silicon. The confirmative evidence of this origin is that for a given gate to STI spacing, the corner stress and channel stress both are comparable and since the tunnel oxide is rather thin, the lateral compressive stress at the surface of the poly-silicon is reasonably close to that of the underlying silicon. In contrast, the simultaneously measured source/drain or edge direct tunneling (EDT) current decreases with decreasing a, as shown in Fig. 5.5. To determine the underlying gate-to-source/drain-extension overlap length where the EDT prevails, the existing edge direct tunneling models [5.33]–[5.35] on the basis of the triangular potential approximation [5.30] can readily apply with some slight modifications such as incorporating stress dependencies of the subbands in the accumulated poly-silicon surface. First of all, the oxide field E_{ox} at the gate edge is determined through the following expression:

$$V_{DG} - V_{FB} = V_{poly} + t_{ox}E_{ox} + V_{DE} \tag{5.4}$$

where V_{DG} is the applied source/drain to gate voltage, V_{FB} is the flatband voltage, t_{ox} is the gate oxide thickness, and V_{poly} and V_{DE} are the potential drops in the n^+ poly-silicon and source/drain extension region, respectively. The accumulated electrons mainly populate in the first subband E_1 due to the lowest quantized energy dominating. Then, relating the sheet charge density to the number of occupied subband states can establish the charge conservation relationship:

$$q\left(E_{fn} - E_1\right)\frac{\eta m_d}{\pi\hbar^2} = \varepsilon_{ox}E_{ox} = Q \tag{5.5}$$

where E_{fn} is the quasi-Fermi level in n^+ poly gate, η is the degeneracy factor and Q is the available charge for tunnel process. The corresponding stress dependency of the quantized energy is well defined in the literature [5.22], [5.23], [5.27]–[5.29]:

$$E_1(\sigma) = \left(\frac{9hq\varepsilon_{ox}E_{ox}}{16\varepsilon_{Si}\sqrt{2m_z}}\right)^{\frac{2}{3}} + \left(\Xi_d + \frac{\Xi_u}{3}\right)(S_{11} + 2S_{12})\sigma + \left(\frac{\Xi_u}{3}\right)(S_{12} - S_{11})\sigma \tag{5.6}$$

where the elastic compliance constants $S_{11} = 7.68 \times 10^{-12}$ m^2 /N and $S_{12} = -2.14 \times 10^{-12}$ m^2/N. The hydrostatic and shear deformation potential constants $\Xi_d = 1.13$ eV and $\Xi_u = 9.16$ eV [5.19], close to those of Ref. [5.22], were cited here. With the aforementioned parameters as input, the lowest subband level with respect to the Fermi level can be quantified. Employing the lowest subband approximation to the accumulated n^+ poly gate and the deep depletion approximation to the source/drain extension region as drawn in Fig. 5.6, the following expressions can therefore be derived:

$$V_{poly} \approx \frac{E_{fn}}{q} = \varepsilon_{ox}E_{ox}\frac{\pi\hbar^2}{q^2\eta m_d} + \frac{E_1}{q} \tag{5.7}$$

$$V_{DE} = \frac{\varepsilon_{ox}^2 E_{ox}^2}{2q\varepsilon_{Si}N_{DE}} \tag{5.8}$$

where N_{DE} is the dopant concentration of source/drain extension. Here, the quantization effective masses $m_z = 0.98\ m_0$ and $m_d = 0.19\ m_0$, and $\eta = 2$ were adopted to approximate the band structure for <100> oriented poly-silicon grain [5.31]. Then, it is a straightforward task to calculate the WKB tunneling probability, taking into account the corrections for reflections from the potential discontinuities [5.31]. Here the electron effective mass in the oxide for the Franz type dispersion relationship was used with $m_{ox} = 0.61\ m_0$. The SiO_2/Si interface barrier height in the absence of stress is 3.15 eV. Consequently, the edge electron direct tunneling current density can be calculated as a function of the stress σ:

$$I_{EDT}(\sigma) = WL_{TN}\frac{qQ}{\tau_1(\sigma)} \tag{5.9}$$

where q is the elementary charge, W is the channel width, and L_{TN} is the gate-to-source/drain-extension overlap length. The tunneling lifetime in above equation can be connected with the transmission probability T: $\tau_1(\sigma) = \pi\hbar/(T_1(\sigma)E_1(\sigma))$.

Then with known process parameters and published deformation potential constants [5.19] as input, the measured EDT was reproduced well as displayed in Fig. 5.7. Electron tunneling onto the forbidden silicon energy gap occurs in -0.1 V < V_G < 0 V; however, an appreciable gate current was measured there. This indicates the existence of the oxide traps or interface states. Only at more negatively biased gate voltages where the EDT dominates can the effect of the traps be alleviated. In addition, it was found that the gate edge direct tunneling current is several orders of magnitude larger than the gate-to-substrate current and hence is dominant over the gate voltage range of interest. The extracted gate-to-source/drain overlap L_{TN} spans a range of 6.1, 6.0, 5.7, and 5.0 nm for a of 10, 2.4, 0.495, and 0.21 μm, respectively as demonstrated in Fig. 5.8. The L_{TN} values are found to be comparable with those in the literature [5.33]–[5.35]. The shift of around 1.1 nm, caused by dopant retarded lateral diffusion for stress change from 0 to -440 MPa, is reasonable with respective to the process simulation [5.13]. In the cited work [5.13], a device/process coupled simulation was carried out to produce the lateral doping profile from the source through the channel to the drain, with and without the strain dependencies. The resulting doping profiles reveal the diffusion retardation of about 1.8 nm as caused by a stress change from -10 to -500 MPa. It is therefore inferred that the extracted local stress and lateral diffusion shift are in satisfactory agreement with those of the process simulation published elsewhere [5.13].

The gate-to-source/drain-extension overlap length designated L_{TN} is essentially proportional to the square root of dopant diffusivity D. The stress dependent dopant diffusivity can be expressed as [5.1], [5.4], [5.12]:

$$D(\varepsilon) = D(0)\exp(\frac{-Q\varepsilon}{kT}) \tag{5.10}$$

where Q is the strain induced activation energy and ε is the uniaxial strain. ε can be related to the uniaxial stress σ with the Young's modulus Y: $\sigma = Y\varepsilon$. Then the effect of the stress on the extension overlap length can be derived as

$$\frac{L_{TN}(\sigma)}{L_{TN}(0)} = \exp(\frac{-Q\sigma}{2kTY}) \tag{5.11}$$

The extracted extension overlap length is plotted in Fig. 5.9 versus the uniaxial corner stress. Fitting of the data yields a value of $-Q/kT = 129$. Assuming a typical temperature of $T = 1300$ K for the manufacturing process, the activation energy Q of -15.7 eV results, which is reasonable relative to those (-14 eV for arsenic and -30 eV for phosphorus) of the process simulation [5.13]. Therefore, a physically oriented analytic model is reached, expressing the lateral diffusion length as a function of the corner stress.

5.5 Conclusion

With the aid of the layout technique, the source/drain extension corner stress has been for the first time extracted by using the subthreshold current measurement, and has been compared with the channel stress obtained by the additional measurements on the gate direct tunneling in inversion and mobility. The validity of the layout technique has been confirmed as well. With known process parameters and published deformation potential constants as input, fitting of the gate edge direct tunneling data has led to the value of the underlying lateral diffusion. The retarded lateral diffusion length and the strain induced activation energy both have been quantitatively consistent with those of the process simulation. A physically oriented analytic model has been reached, expressing the lateral diffusion as a function of the corner stress.

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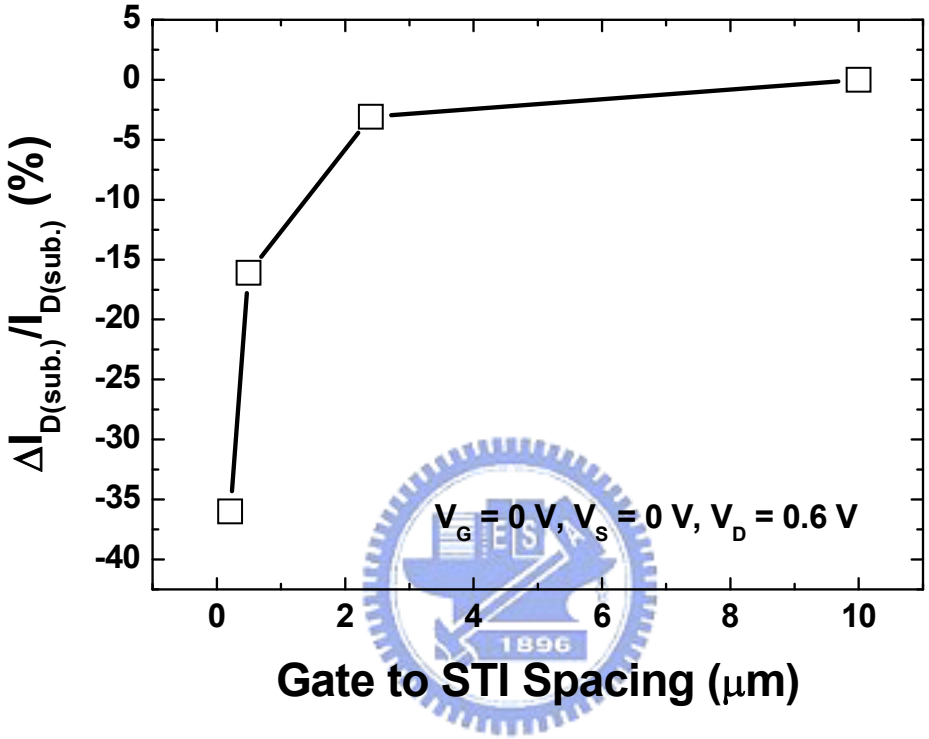


Fig. 5.1 The measured subthreshold current change versus gate to STI spacing.

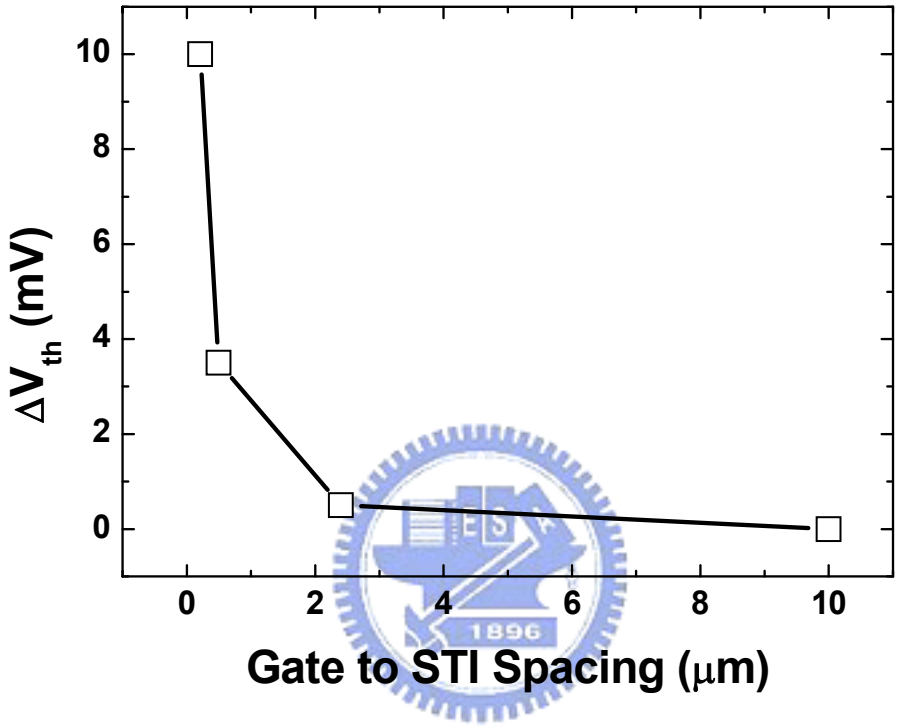


Fig. 5.2 Measured threshold voltage shift versus gate to STI spacing.

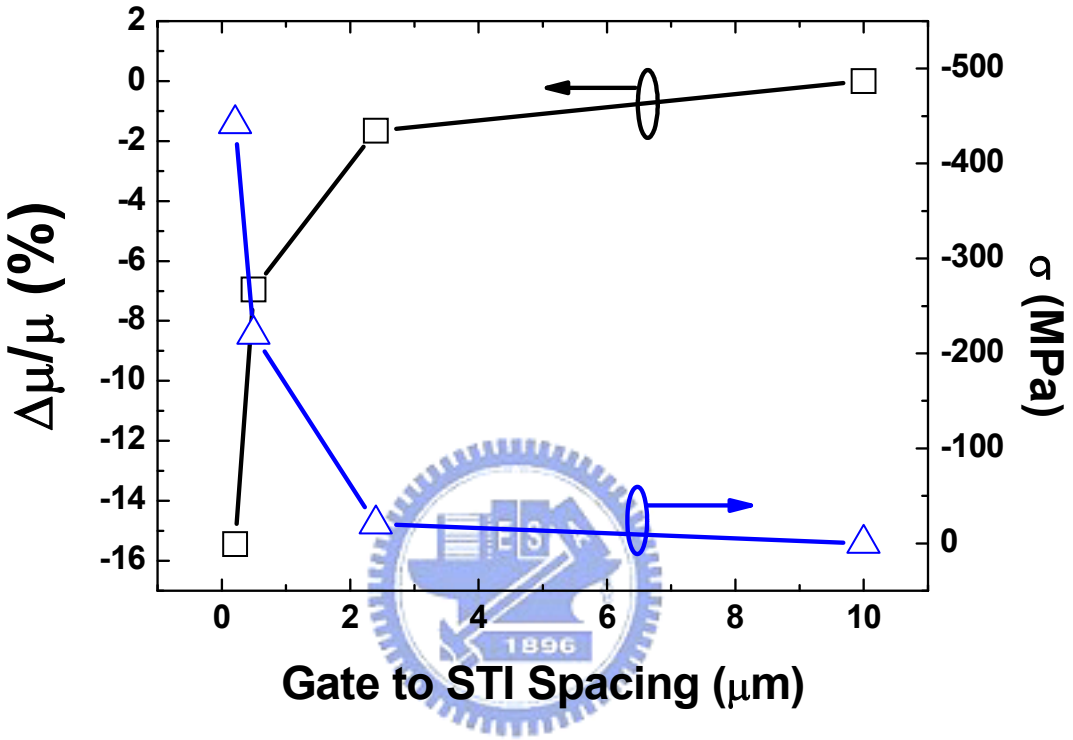


Fig. 5.3 The extracted mobility variations and source/drain extension corner stress versus gate to STI spacing.

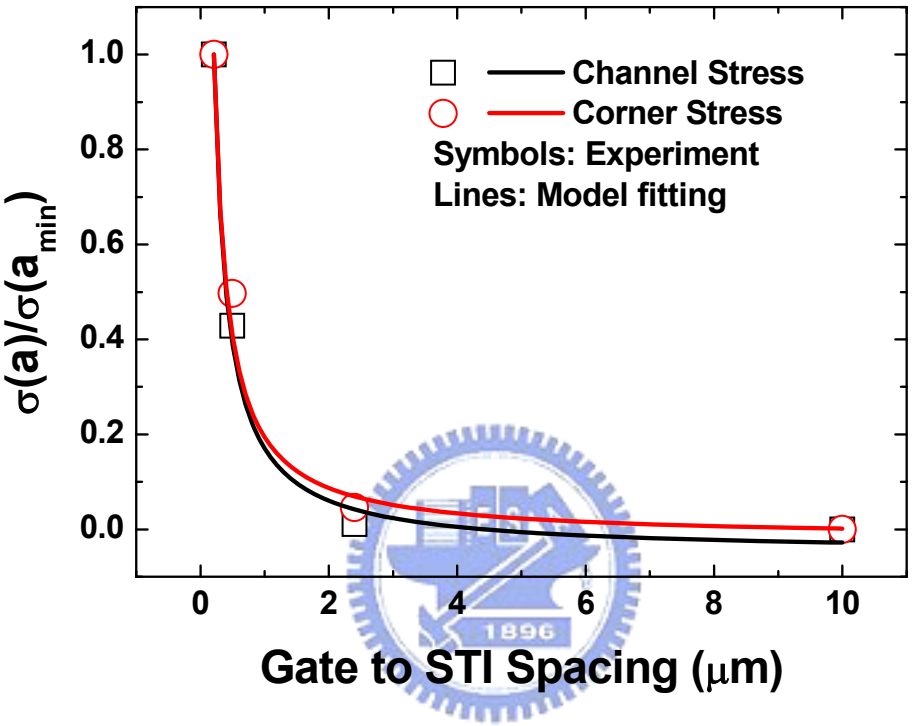


Fig. 5.4 The plot showing the extracted channel and corner stress, divided by that of the minimum *a*, versus the gate to STI spacing, along with fitting curves from the citation [5.25].

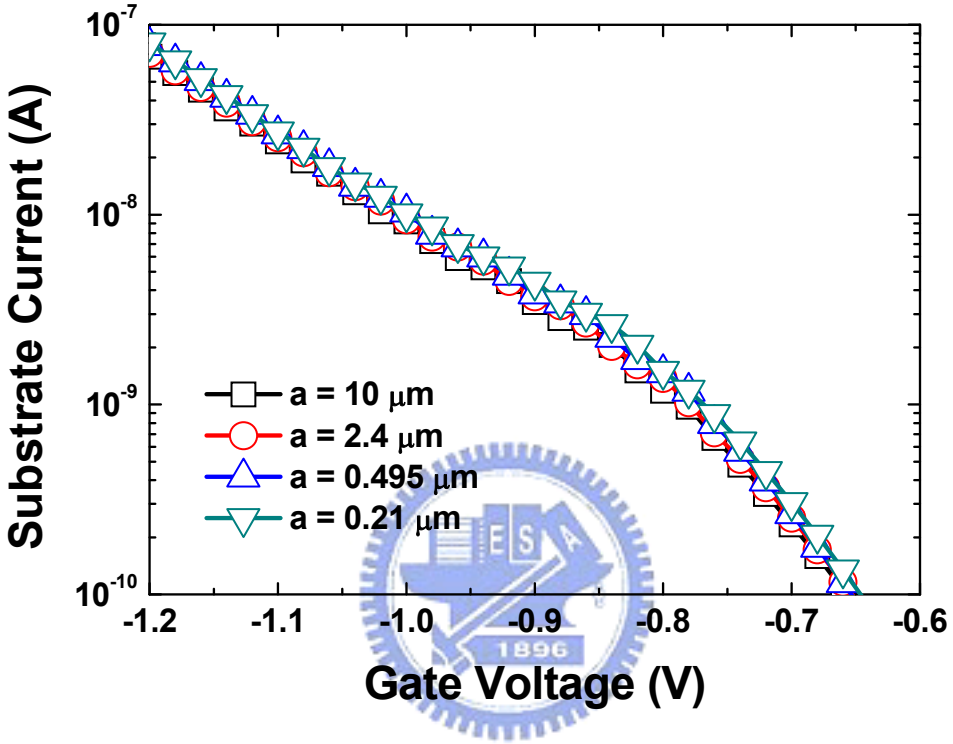


Fig. 5.5 Plot of the measured substrate current versus negative gate voltage.

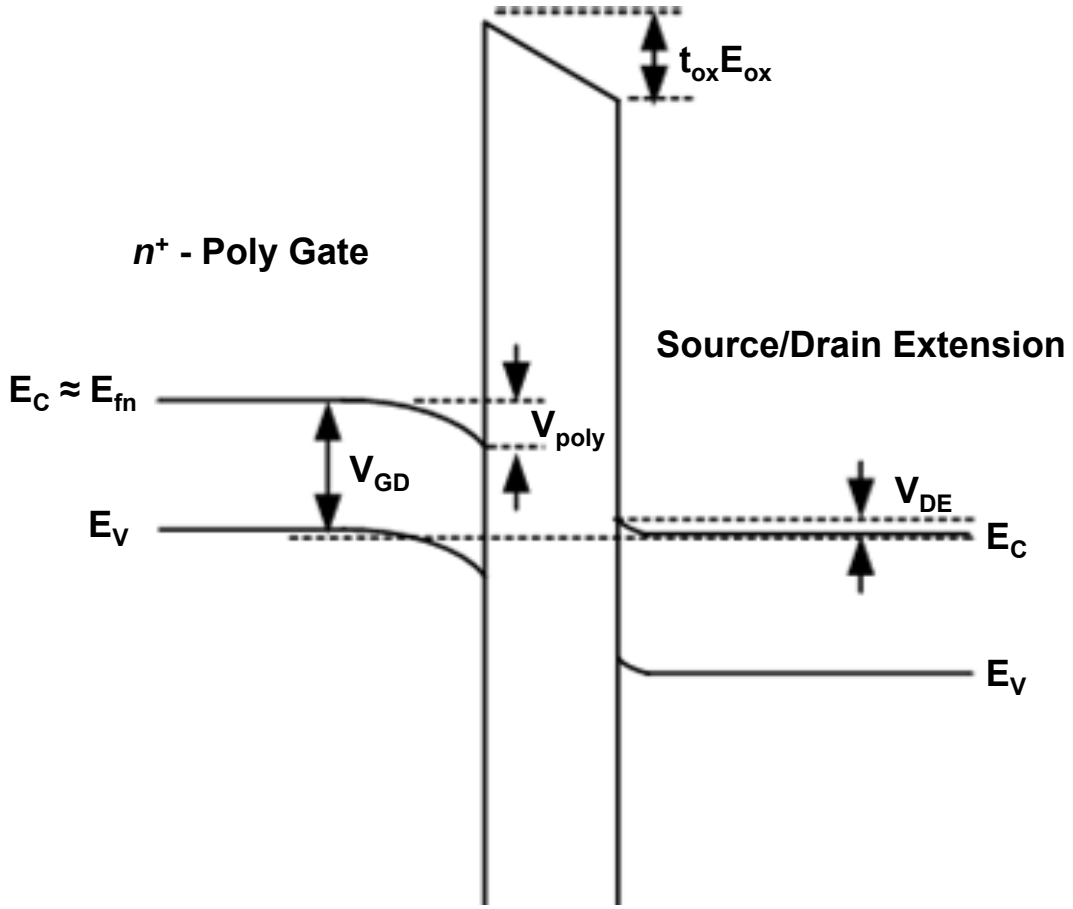


Fig. 5.6 Band diagram drawn along n^+ poly-gate/SiO_2/diffusion extension.

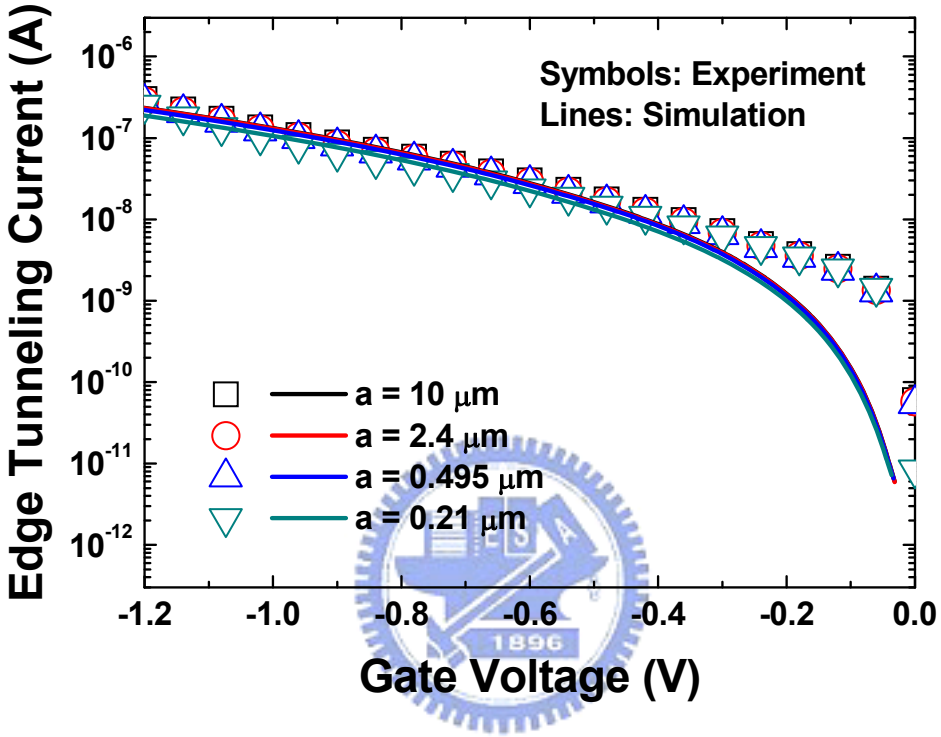


Fig. 5.7 Comparison of calculated and measured edge direct tunneling current versus negative gate voltage.

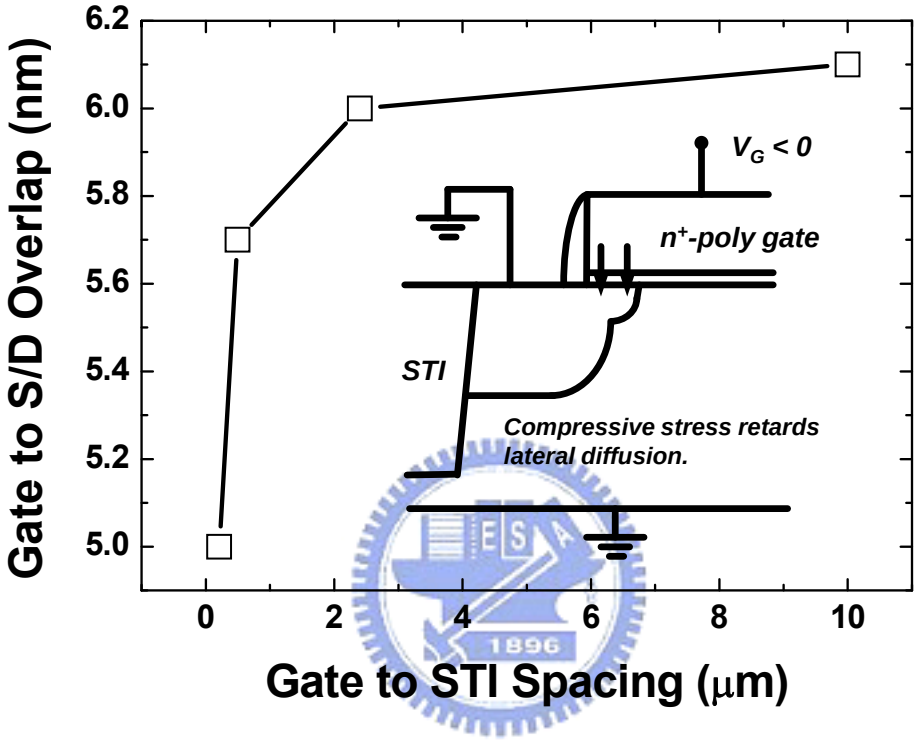


Fig. 5.8 The extracted gate to source/drain extension overlap length versus gate to STI spacing. The decreasing trend with decreasing *a* can be related to the retarded lateral diffusion under the influence of the compressive stress.

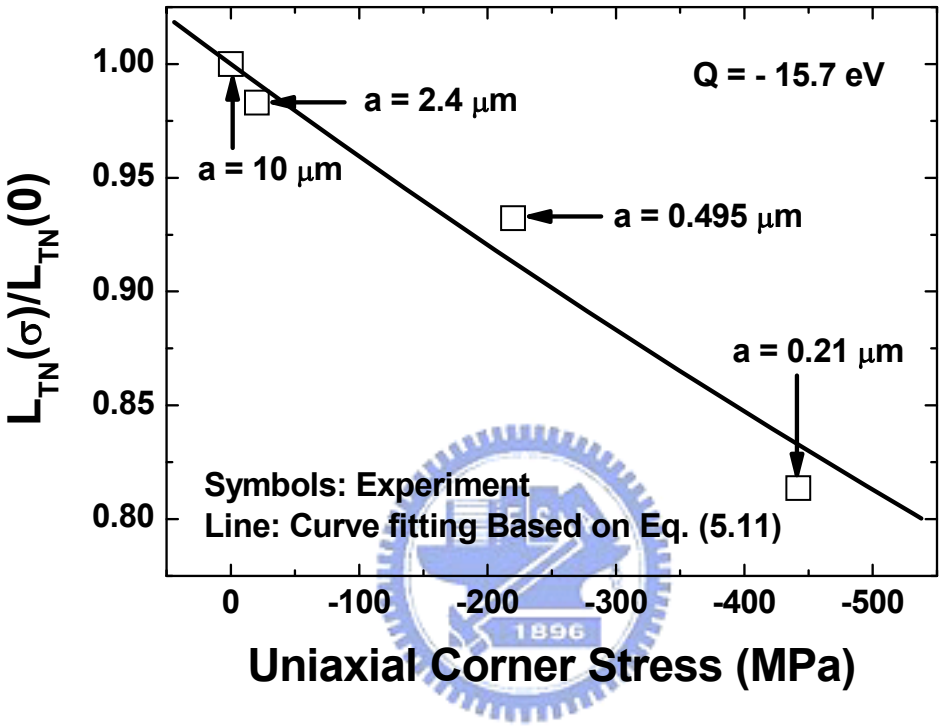


Fig. 5.9 The extracted (symbols) extension overlap length change versus corner stress. Also shown is a fitting line from Eq. (5.11).

Chapter 6

Effect of STI Mechanical Stress on *p*-Channel Gate Oxide Integrity

6.1 Introduction

Strained silicon has currently been adopted in the high-performance nanotechnologies. There have been two fundamentally different approaches used to achieve this goal: (i) strained silicon on a relaxed buffer layer; and (ii) process strained silicon through the shallow trench isolation (STI), capping layer, silicide, or an embedded source/drain stressor [6.1],[6.2]. Examination of the interfacial properties or gate oxide integrity associated with strained devices is essentially crucial. Recently, a low-frequency noise measurement on strained *n*-MOSFETs has revealed underlying gate oxide integrity [6.3],[6.4]. In this work, the noise measurement is conducted on *p*-channel counterparts with the varying STI mechanical stress in the channel width direction.

6.2 Experiment

Devices under test were *p*-MOSFETs fabricated in a state-of-the-art manufacturing process. In this process, strain engineering was implemented using the shallow trench isolation (STI) technique. The STI mechanical stress under study was applied in the width direction as drawn in Fig. 1, achieved with the channel length fixed at 0.5μm while varying channel widths (0.11, 0.24, 0.6, 1, and 10 μm). Reduction in channel width means more

tensile stress in that direction. This argument was experimentally corroborated in terms of the enhanced drain current per unit width in Fig. 6.1 versus channel width. Technique concerning delta width and STI effects can be quoted in Chapter 4 to clarify the status of stress (tensile or compressive). The threshold voltage and low-field mobility of the devices were extracted from the linear regime of operation [6.5]. The low-frequency noise measurement setup detailed elsewhere [6.6] was employed. The measurement frequency ranged from 3 Hz to 100 kHz. Noise measurements were conducted under quasi-equilibrium conditions (V_D= –0.05V) with the gate overdrive (V_{OV}) as a parameter.

6.3 Results

As seen in Fig. 6.2, it is clear that $S_{id}/I_D^2 \propto 1/(V_{GS}-V_T)$, indicating that the mobility fluctuations or the Coulomb scattering part cannot be ignored. Therefore, the following so-called correlated mobility-number fluctuation approach was utilized for the input-referred voltage noise power spectral density [6.7]:

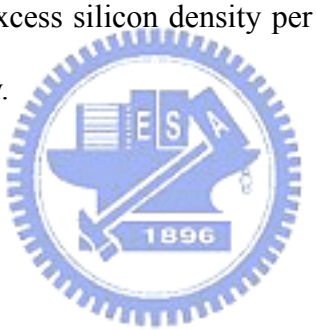
$$S_{Vg} = \left[1 + \alpha \mu_{eff} C_{EOT} \left(V_{GS} - V_T\right)\right]^2 \left(q^2 k_B T \lambda N_t / C_{EOT}{}^2 WLf\right) \tag{6.1}$$

where α is the effective scattering coefficient, μ_{eff} is the low-field effective mobility, C_{EOT} is the gate oxide capacitance per unit area, q is the elementary charge, k_B is Boltzmann's constant, T is the absolute temperature, λ is the tunneling distance (~0.1nm), W is the channel width, L is the channel length, and N_t is the interface-state density. Based on (1) and S_{Vg} data in Fig. 6.3, both N_t and α were determined from the $S_{Vg}{}^{0.5}$ versus -(V_{GS}-V_T) characteristics. The results are shown in Fig. 6.4 and 6.5. It can be seen that on the average, for decreasing channel widths from 10 μm down to 0.11 μm, the interface-state density decreases whereas the scattering coefficient undergoes a relatively small change.

6.4 Physical Origins

Analogous to the ESR on (100) Si/SiO_2 interface [6.8], the interface defects investigated here can be attributed to the group of P_b centers as a result of the mismatch between the Si substrate and SiO_2 network. The network/lattice mismatch primarily originates from the volume expansion upon oxidation of Si. Obviously, with an enhanced tensile stress to relax the intrinsic interface strain, the network/lattice mismatch is diminished, leading to a reduction in P_b centers.

Another physical interpretation can be established by directly quoting the earlier works by Deal, et al. [6.9], as illustrated in Fig. 6.6. More tensile strain produces augmented lattice spacing or equivalently reduced excess silicon density per unit area, which in turn gives rise to decreased interface-state density.



6.5 Conclusion

The noise measurement on *p*-MOSFETs has revealed that an enhanced tensile stress in the channel narrowing direction can improve the gate oxide integrity. Its physical origins were related to relaxed interface strain and reduced excess silicon per unit area during the oxidation.

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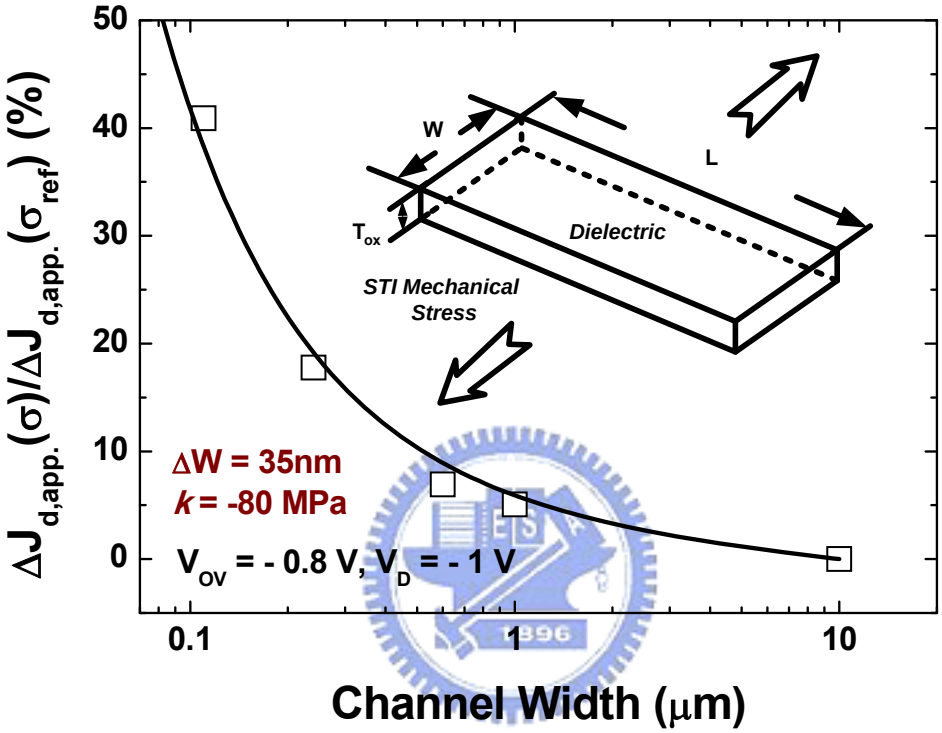

Fig. 6.1 Measured drain saturation current enhancement factor versus channel width. The inset shows the schematic illustration of STI mechanical stress in the width direction.

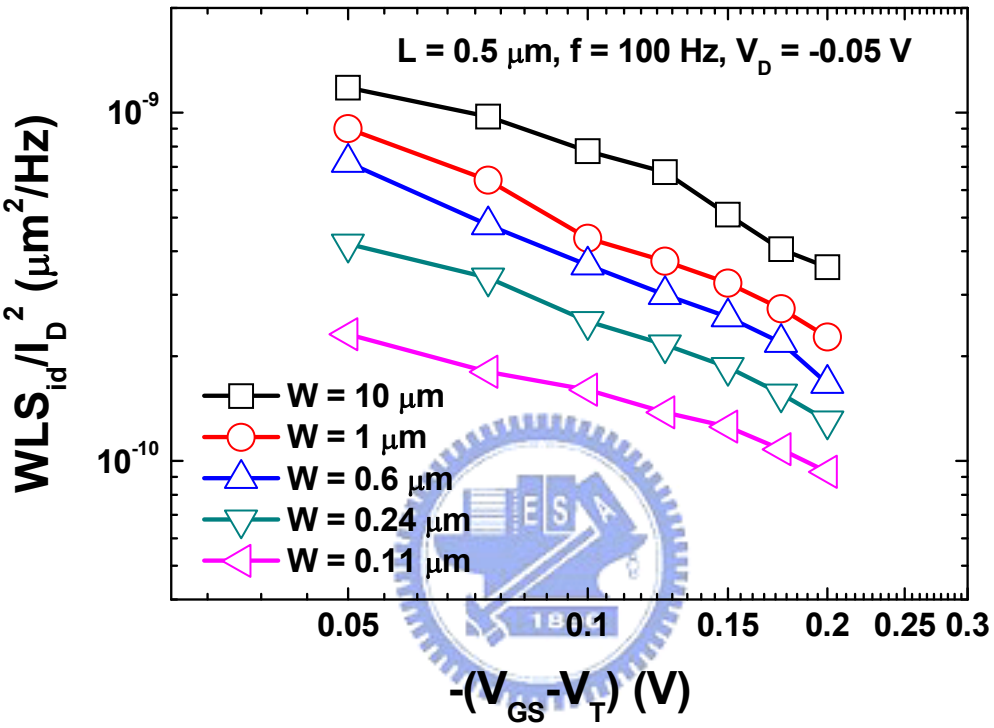

Fig. 6.2 Normalized experimental drain current noise spectral density versus gate overdrive for different channel widths.

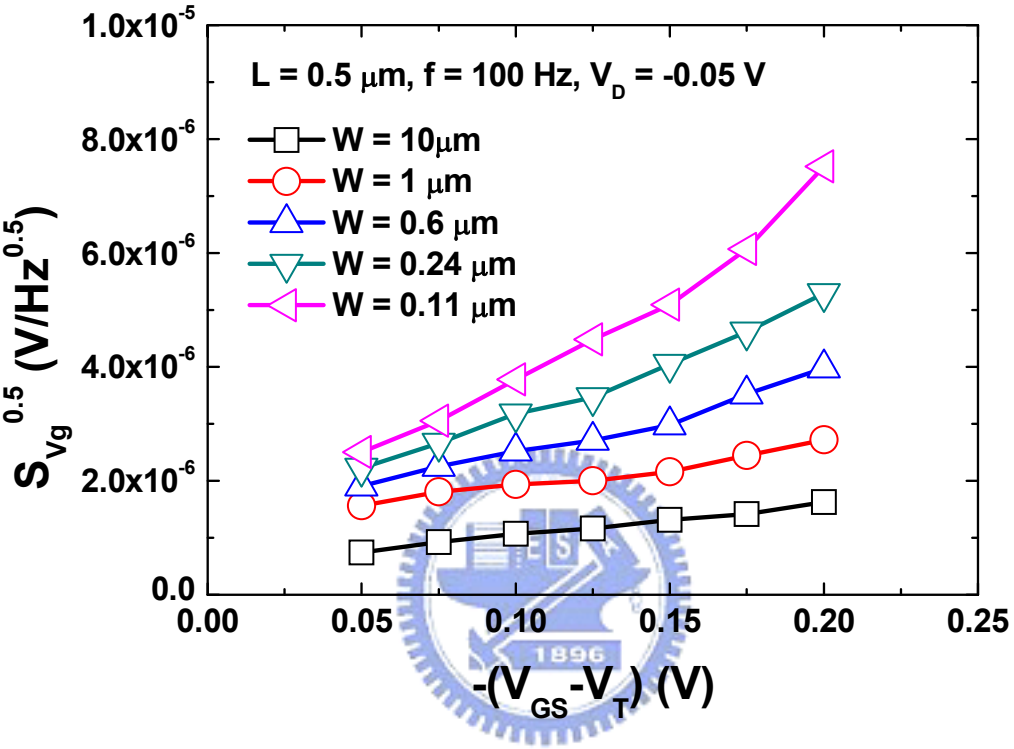

Fig. 6.3 Square root of measured input-referred noise voltage spectral density versus gate overdrive.

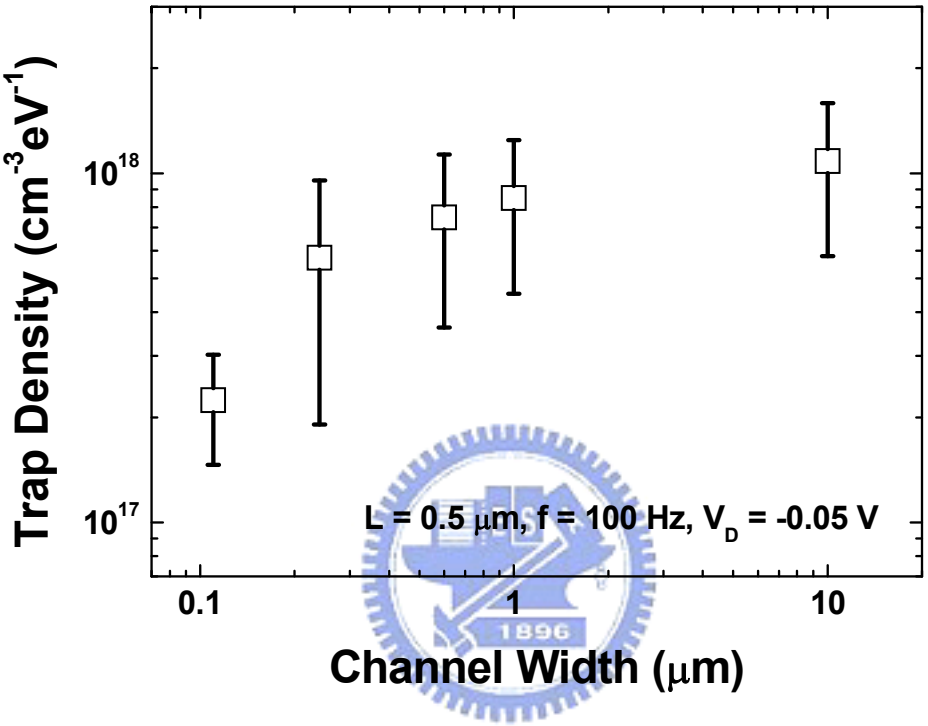

Fig. 6.4 Extracted effective interface-state density from Fig. 6.3.

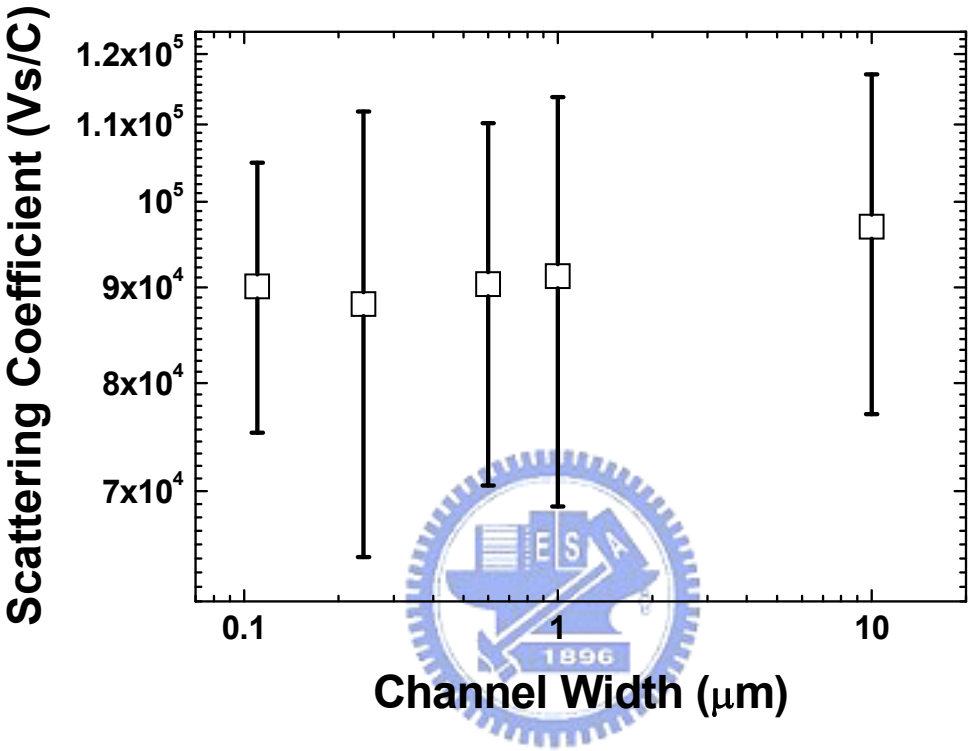

Fig. 6.5 Extracted effective scattering coefficient from Fig. 6.3.

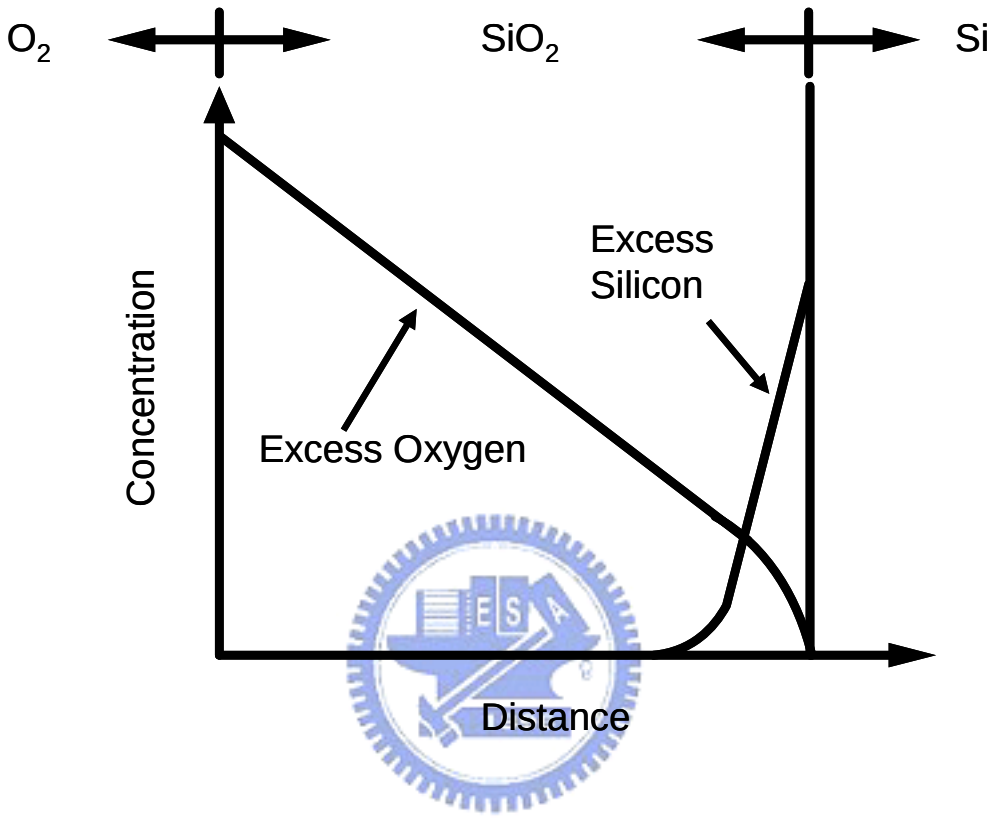

Fig. 6.6 Schematic illustration of the distribution of the excess species in an oxide film during oxidation [6.9].

Chapter 7

Conclusions and Future Work

7.1 Conclusions

This dissertation concerns the assessment of mechanical stress and modeling of physical behaviors in strained MOSFETs. Brief summaries of this work are listed as follows:

First of all, with known process parameters and published deformation potential constants as input, fitting of gate direct tunneling current versus gate voltage data has led to the value of the underlying channel stress. A link with the mobility measurement on the same device has been conducted. The resulting piezoresistance coefficient has been in good agreement with literature values. The layout technique has also been validated.

Second, we have systematically examined the delta width and channel stress effects on gate direct tunneling current of narrow n-MOSFETs under STI compressive stress. Both effects have been decoupled using a new analytic direct tunneling model. The validity of the extracted transverse channel stress and delta width has been confirmed. The effect of varying longitudinal channel stress due to the narrowing action has also been addressed. The corroborating evidence in terms of the drain current variation has further been established.

Then, with the aid of the layout technique, the source/drain extension corner stress has been for the first time extracted by using the subthreshold current measurement, and has been compared with the channel stress obtained by the additional measurements on the gate direct tunneling in inversion and mobility. The validity of the layout technique has been confirmed as well. With known process parameters and published deformation potential constants as input, fitting of the gate edge direct tunneling data has led to the value of the underlying

lateral diffusion. The retarded lateral diffusion length and the strain induced activation energy both have been quantitatively consistent with those of the process simulation. A physically oriented analytic model has been reached, expressing the lateral diffusion as a function of the corner stress.

Finally, the noise measurement on *p*-MOSFETs has revealed that an enhanced tensile stress in the channel narrowing direction can improve the gate oxide integrity. Its physical origins were related to relaxed interface strain and reduced excess silicon per unit area during the oxidation.

7.2 Recommendation for Future Work

In this work, uniaxial stress along longitudinal or transverse direction has been successfully extracted. Here, the dimension length in one direction is larger than the other one. However, when the device dimension shrinks drastically in both, the uniaxial hypothesis would not work properly. Thus, a study extending to 2D or 3D case is needed.

Intentional strain technology such as SiGe stressor, contact etch stop layer has also widely applied in the industry. Usually, the magnitude of stress will exceed 1GPa and may reach 3GPa. Hence, the shear term in k・p method incorporating with deformation potential theory must be adopted for calculating the conduction bands considering the band distortion which is neglected under moderate stress in this research.

In this work, the isotropic stress-dependent diffusion model for uniaxial stress case has been developed and is sufficient to explain the experimental data. However, even stronger anisotropic stress can be expected in future technologies, and therefore a generalized anisotropic stress-dependent diffusion model for arbitrary stress conditions is necessary.

The impact of stress on interface states has been discussed. However, a quantitatively

analytical model has not been well established yet. It has been reported that the defects strongly depends on the stress states during the oxidation and passivated processes. With well-developed model, the oxide integrity can be controlled by carefully selecting process steps.

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Publication List

Journal and Letter

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