具有低電壓以及良好電荷儲存能力之金屬-氧化層-氮化層-氧化層-矽結構非揮發性記憶體之研究

研究生：楊學人　　　　　　　　　　指導教授：荊鳳德 博士

國立交通大學

電子工程學系暨電子研究所博士班

摘要

在過去十年，由於可攜式電子產品市場的興起，例如手機和數位相機。低功耗以及低成本的記憶體元件已經吸引越來越多的注意，由於這些記憶體元件需擁有至少十年的資料儲存能力，因此非揮發性記憶體的地位日趨重要。

根據 ITRS 技術藍圖，浮停閘(floating-gate)非揮發性記憶體的關鍵技術在於穿遂氧化層的微縮，因為壓力所引起的漏電流(SILC)會造成儲存資料經由單一的缺陷而流失，此問題會在很薄的穿遂氧化層下愈顯嚴重，對於新興的單晶片系統(SoC)積體電路設計來說，由於非揮發性記憶體的編碼電壓必須和低電壓的邏輯電路相容，因此更是一項嚴峻的挑戰。近年來，基於電荷儲存原理所形成的多晶矽或金屬閘極-氧化矽-氮化矽-氧化矽-矽(SONOS/MONOS)記憶體元件和浮停閘記憶體元件相比，具有較低編碼電壓，較小單元尺寸以及較佳耐用度的優點，因此受

到很大的關注。在 SONOS/MONOS 元件中，電荷是儲存於分離性的捕陷區而非浮停閘的連續性，僅有靠近缺陷附近的電荷會流失因此對 SILC 有更好的抵抗能力，另外穿遂氧化層也能更有效的微縮。然而，抹除速度以及資料儲存能力仍然是 SONOS/MONO 元件取代浮停閘元件的主要挑戰。

在此論文中，我們使用全新的高含氮量氮氧化鉿材料作為MONOS元件的捕陷層，此元件具有低的操作電壓，快的速度以及良好的電荷儲存能力。在快速(100毫秒)和低電壓(9伏)的操作條件之下，可得到2.8伏的記憶視窗;在85℃ 和125℃環境下由外插法所得的十年資料儲存能力，其記憶視窗仍有1.8伏和1.5伏，由於我們調整高含氮量氮氧化鉿的捕陷能階深入至靠近矽中間能帶的禁止能帶中，才能在僅2.9奈米穿遂氧化層的MONOS元件中，擁有如此突出的資料儲存能力。為了進一步提升高溫下的資料儲存能力，我們提出了一種具有雙重量子井結構的MONOS元件，在快速(100毫秒)和低電壓(9伏)的操作條件之下，可得到3.2伏的記憶視窗，在150℃的環境下，其十年的資料儲存能力，仍然可維持在2.7伏，僅百分之二十五的視窗衰減，主要歸功於雙重量子井將被捕陷的載子侷限在高含氮量氮氧化鉿材料之中。以上兩種MONOS元件，只要設計一簡單的電路將記憶體元件之操作電壓減少一半便可以達到單一片系統的應用。

Research of MONOS Non-Volatile Memory with Low Voltage and Good Retention

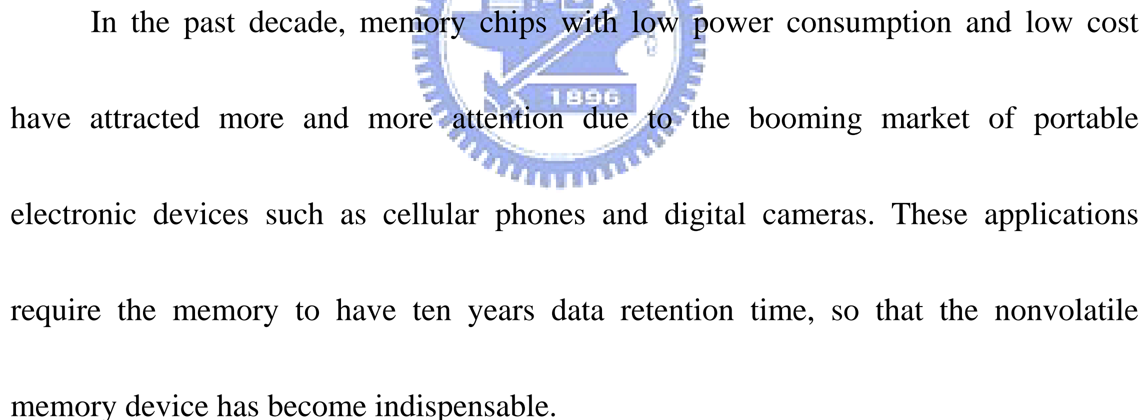
Student: Hsueh-Jen Yang **Advisor: Dr. Albert Chin**

Department of Electronics Engineering

& Institute of Electronics

National Chiao Tung University

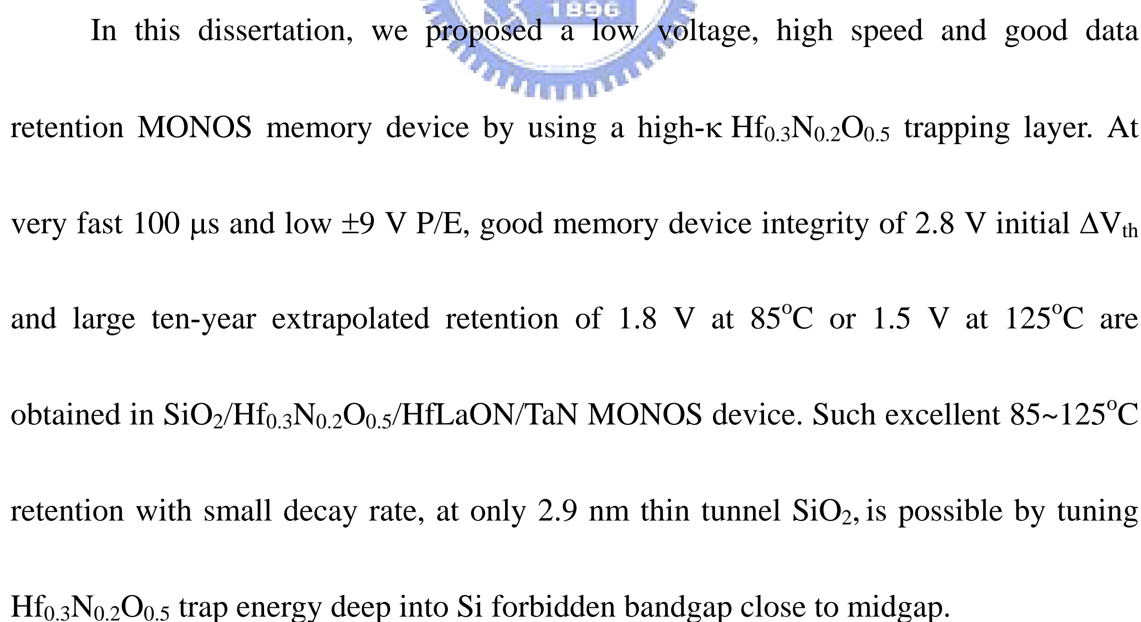
ABSTRACT



In the past decade, memory chips with low power consumption and low cost have attracted more and more attention due to the booming market of portable electronic devices such as cellular phones and digital cameras. These applications require the memory to have ten years data retention time, so that the nonvolatile memory device has become indispensable.

According to ITRS roadmap, the key issue for floating-gate nonvolatile semiconductor memory (NVM) is the scaling of the tunneling oxide because the stress-induced leakage current (SILC), which can discharge the whole floating-gate memory with even one single defect, becomes a severe problem at very thin tunneling oxide thickness. This scaling issue is a formidable challenge especially for the

emerging system-on-chip (SoC) integrated circuit designs in which programming voltage must be scaled for the NVM to be compatible with the low voltage logic circuit. Recently, silicon/metal-oxide-nitride-oxide-silicon (SONOS/MONOS) charge trapping based NVM has received considerable interest due to its advantage of lower programming voltage, smaller cell size and better endurance over the floating-gate devices. In SONOS devices charges are stored in discrete traps instead of continuous floating gate. As a result, such devices are more robust to SILC since only charges near the defect site can be discharged and the tunneling oxide layer can be scaled more aggressively than floating-gate devices. However, retention and erase speed remain as the major challenges for SONOS/MONOS devices to replace floating-gate devices.



In this dissertation, we proposed a low voltage, high speed and good data retention MONOS memory device by using a high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer. At very fast 100 μs and low ±9 V P/E, good memory device integrity of 2.8 V initial ΔV_{th} and large ten-year extrapolated retention of 1.8 V at 85°C or 1.5 V at 125°C are obtained in $SiO_2/Hf_{0.3}N_{0.2}O_{0.5}$/HfLaON/TaN MONOS device. Such excellent 85~125°C retention with small decay rate, at only 2.9 nm thin tunnel SiO_2, is possible by tuning $Hf_{0.3}N_{0.2}O_{0.5}$ trap energy deep into Si forbidden bandgap close to midgap.

To address the high temperature retention issue, we further provide the [TaN-Ir_3Si]-[HfAlO-$LaAlO_3$]-$Hf_{0.3}N_{0.2}O_{0.5}$-[HfAlO-SiO_2]-Si device. At 150°C under

very fast 100 μs low ± 9 V program/erase, this device shows good memory device integrity of a 3.2 V initial ΔV_{th} and 2.7 V ten-year extrapolated retention. This only 25% retention decay at 150°C was achieved by double quantum-barriers confining the deep-trapping-energy $Hf_{0.3}O_{0.5}N_{0.2}$ well. Both above devices are useful for embedded SoC under a single 5 V voltage source by using a simple voltage inverter circuit.

Acknowledgements

First of all, I would like to thank my advisor Prof. Albert Chin for his guidance and support throughout my graduate studies at National Chiao-Tung University. This work would not have been possible without the most insoiring discussions we have had in the past four years.

I am also grateful to all members in ED633 group, including those seniors, C. H. Cheng, C. F. Cheng, H. L. Kao, C. H. Lai, C. H. Wu and B. F. Hung, for their help in my study; especially S. H. Lin, W. B. Chen, K. Y. Jhou and W. L. Huang for their assistance in experiments.

Moreover, I am appreciative of the financial and equipment supports from National Science Council, Nano Facility Center of NCTU and National Nano Device Laboratory. I am also grateful to those who ever assisted this work.

Finally, I greatly appreciate the endless encouragement and spiritual support of my family and my dear girl friend Elisa Chen. Without them, I can't finish this dissertation.

Contents

Abstract (in Chinese)....i

Abstract (in English)....iii

Acknowledgement....vi

Contents....vii

Table Captions....x

Figure Captions....xi

Chapter 1 Introduction

1.1. Motivation to study MONOS Flash memory....**1**

1.2. Motivation to use High-κ materials for MONOS Flash memory....**4**

1.3. The measurement of the devices....**6**

1.4. Overview of Dissertation....**6**

Chapter 2 A Program-Erasable High-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS Capacitor with Good Retention

2.1. Introduction....**15**

2.2. Experimental Details....**16**

2.3. Result and Discussion....**17**

2.4. Conclusions....**19**

Chapter 3 Comparison of MONOS Memory Device Integrity when Using $Hf_{1-x-y}N_xO_y$ Trapping Layers with different N Compositions

3.1. Introduction……………………………………………………………...24

3.2. Experimental Details…………………………………………………….25

3.3. Result and Discussion…………………………………………………...26

3.4. Conclusions……………………………………………………………...32

Chapter 4 Improved Data Retention for Charge-Trapping Memory by Using Double Quantum Barriers

4.1. Introduction……………………………………………………………46

4.2. Experimental Details…………………………………………………...47

4.3. Result and Discussion………………………………………………….48

4.4. Conclusions…………………………………………………………….50

Chapter 5 Compare the Performance of Charge-Trapping Memory with Different Single and Double Quantum Barriers

5.1. Introduction……………………………………………………………...55

5.2. Experimental Details…………………………………………………….56

5.3. Result and Discussion……………………………………………………58

5.4. Conclusions………………………………………………………………62

Chapter 6 Conclusions……………………………………………...71

Reference…………………………………………………………...73

Vita……………………………………………………………….91

Publication Lists………………………………………………….92

Table Captions

Chapter 3 Comparison of MONOS Memory Device Integrity when Using $Hf_{1-x-y}N_xO_y$ Trapping Layers with different N Compositions

Table 3-1. Comparison of memory characteristics for the $Hf_{0.3}N_{0.2}O_{0.5}$, $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layer MONOS device with other state-of-the-art devices.

Chapter 4 Improved Data Retention for Charge-Trapping Memory by Using Double Quantum Barriers

Table 4-1. Comparison of important memory device characteristics among double quantum-barriers charge-trapping device (this work) and other MONOS and TANOS devices.

Figure Captions:

Chapter 1 Introduction

Fig. 1-1 The electrical products of nonvolatile Flash memory application.

Fig. 1-2 Schematic cross-section of a floating gate memory device. It is essentially a MOSFET, except that a floating gate is sandwiched between a tunnel oxide and an inter-poly oxide.

Fig. 1-3 The cross section of [Metal gate/poly-Si]-SiO_2-Si_3N_4-SiO_2-Si memory.

Fig. 1-4 The requirements for SONOS memory (the international technology roadmap for semiconductors:2006 update).

Fig. 1-5 When the tunnel oxide is scaled, the voltage drop across it is reduced for the same programming voltage. This increases the nitride tunnel barrier, as shown by the light gray area. The benefit from tunnel oxide scaling is significantly reduced due to the nitride barrier.

Fig. 1-6 The band offset of popular high-κ materials.

Chapter 2 A Program-Erasable High-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS Capacitor with Good Retention

Fig. 2-1 The *C-V* characteristics of an $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor after applying a ± 5 V program/erase (P/E) voltage for various periods from 0.1 to 100 ms. (b).

The *C-V,* for various P/E voltages from ± 3 to ± 5 V, as a function of the P/E time. The insert shows the V_{fb}-*P/E time* plot.

Fig. 2-2 (a) Retention characteristics at 25 and 100°C of an $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor, measured to 10000 s, after a 1 ms, ± 5 V P/E writing pulse; (b) cycling characteristics of the $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor. Data for an AlN MIS capacitor are shown for comparison in (a). The insert in (b) shows the variation of V_{fb} with cycling.

Fig. 2-3 A ln(*J*)-$E^{1/2}$ plot, using the measured *J-V* of a TaN/$Hf_{0.3}N_{0.2}O_{0.5}$/Si MIS device, where the electron injection is from the Si. Calculated data using both Schottky Emission (*SE*) and Frenkel-Poole (*FP*) conduction models are included. The inserted figure shows the band diagram of the $Hf_{0.3}N_{0.2}O_{0.5}$ MIS devices, where the barrier height and trap energy were obtained from *SE* and *FP* fits to the measured data.

Chapter 3 Comparison of MONOS Memory Device Integrity when Using $Hf_{1-x-y}N_xO_y$ Trapping Layers with different N Compositions

Fig. 3-1 (a) Schematic band diagram of a SiN trapping layer MONOS device and (b) the band alignment of various metal-oxide trapping layers to the oxide barrier and Si channel.

Fig. 3-2 XPS spectra of $Hf_{1-x-y}N_xO_y$, where the composition of $Hf_{0.30}N_{0.20}O_{0.50}$ and $Hf_{0.35}N_{0.10}O_{0.55}$ was determined from the data.

Fig. 3-3 *C-V* hysteresis curves for a TaN-HfLaON-$Hf_{1-x-y}N_xO_y$-SiO_2-Si MONOS device with (a) $Hf_{0.35}N_{0.10}O_{0.55}$ and (b) a $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer.

Fig. 3-4 The measured (a) program and (b) erase characteristics of TaN-HfLaON-$Hf_{0.35}N_{0.10}O_{0.55}$-$SiO_2$-Si MONOS transistors, where the device structure is shown in (c).

Fig. 3-5 The measured (a) program and (b) erase characteristics of TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si MONOS transistors.

Fig. 3-6 The retention characteristics of TaN-HfLaON-$Hf_{0.35}N_{0.10}O_{0.55}$-$SiO_2$-Si devices at 25 and 85°C.

Fig. 3-7 The retention characteristics of TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si devices at (a) 25°C and (b) 85 and 125°C.

Fig. 3-8 Endurance characteristics of TaN-HfLaON-$Hf_{1-x-y}N_xO_y$-SiO_2-Si MONOS devices with different $Hf_{0.3}N_{0.2}O_{0.5}$ and $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layers.

Fig. 3-9 Gate stress disturbance of TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si device.

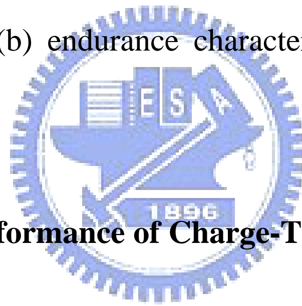
Fig. 3-10 (a) Retention and (b) endurance characteristics of TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si devices at 10 V and 100 μs P/E.

Chapter 4 Improved Data Retention for Charge-Trapping Memory by Using Double Quantum Barriers

Fig. 4-1 Band diagram of of [Metal-gate]-[High-κ top barrier 1]-[High-κ top barrier 2]-[Trapping Layer]-[High-κ bottom barrier 2]-SiO_2-Si double quantum-barriers charge-trapping NVM.

Fig. 4-2 (a) Device program characteristics for different voltages & times. (b) Device erase characteristics at different voltages & times. The device was initially programmed at 8 V for 100 μs.

Fig. 4-3 (a) Retention and (b) endurance characteristics of devices at 25, 85, and 125°C.



Chapter 5 Compare the Performance of Charge-Trapping Memory with Different Single and Double Quantum Barriers

Fig. 5-1. Band diagram of (a) [Metal-gate]-[High-κ barrier]-[Trapping Layer]-SiO_2-Si MONOS non volatile memory device and (b) [Metal-gate]-[High-κ top barrier 1-High-κ top barrier 2]-[Trapping Layer]-[High-κ bottom barrier 2-SiO_2]-Si double-quantum-barrier charge-trapping NVM.

Fig. 5-2. *C-V* hysteresis for double-quantum-barrier device, showing a large V_{th} shift.

Fig. 5-3. Comparison of (a) program and (b) erase characteristics between single- and double-quantum-barrier devices under different voltages & times. For the

erase both devices were initially programmed at 9 V for 100 μs

Fig. 5-4. Device retention characteristics (a) single- and (b) double-quantum-barrier charge-trapping devices at different temperature.

Fig. 5-5. Comparison of (a) endurance characteristics and (b) retention characteristics after 10^3 P/E cycling of single- and double-quantum-barrier devices.

Fig. 5-6. I_d-V_g characteristics of (a) single- and (b) double-quantum-barrier devices after cycling.

Fig. 5-7. Comparison of the interface trap density (D_{it}) for single- and double-barrier devices after P/E cycling.