Chapter 1

Introduction

1.1 Motivation to study MONOS Flash memory

Semiconductor memory is an indispensable component of modern electronic systems. It is used in personal computers, cellular phones, digital cameras, smart-media, networks, automotive systems, global positioning systems. Static Random Access Memory (SRAM) is used as a cache memory in personal computers since it offers the fastest write/read (8ns) speed among all memories. However, a single SRAM cell consists of 6 transistors (6T), so SRAM chip density is very low, although 4T SRAM cells have been demonstrated [1.1]. SRAM memory can retain the stored information as long as the power is on, drawing very little current. However, the information will be lost when the power is turned off, so SRAM is not a nonvolatile memory.

A Dynamic Random Access Memory (DRAM) cell consists of one transistor and one capacitor (1T1C). It is superior to SRAM in many aspects except that the write speed is slower in the DRAM (50ns) than in the SRAM. However, its cell size is much smaller than that of SRAM and thus it is a low cost commodity memory device. Compared to flash memory, DRAM has much faster program/read speed with very

low operating voltage, while flash memory needs 1us to 1ms programming time and high programming voltage. Unfortunately, DRAM is a volatile memory. The data retention time is about 100ms in DRAM while it is 10 years in flash memory: a DRAM cell needs refreshing frequently to maintain its data, so its power consumption is significant. Furthermore, the size of a DRAM cell is larger than that of a flash memory cell. Scaling the DRAM cell size down is difficult due to the large capacitor required to store data.

In the past decade, memory chips with low power consumption and low cost have attracted more and more attention due to the booming market of portable electronic devices such as cellular phones and digital cameras (Fig.1-1). These applications require the memory to have ten years data retention time, so that the nonvolatile memory device has become indispensable. Especially the poly-Si floating gate Flash memory devices its fabrication process is compatible with the current CMOS process and is a suitable solution for embedded memory applications. All other nonvolatile memories such as Ferro-electric Random Access Memory (FeRAM), Magnetic Random Access Memory (MRAM) and phase change memory require integration of new materials that are not as compatible with a conventional CMOS process. It is easier and more reliable to integrate flash memory than other nonvolatile memories with logic and analog devices in order to achieve better chip performance

for wireless communication and wireless computation [1.2].

For conventional poly-Si floating gate Flash memory devices (Fig. 1-2), the key issue is the scaling of tunnel oxide since the storage charges will discharge at very thin tunnel oxide due to the electrical-conductive poly-Si. The scaling of the gate stack and operation voltages are often related to each other. A tunnel oxide thickness of more than 8nm is currently used in the commercial flash memory chip to meet the ten years data retention time requirement. This causes the Flash memories need to operate at higher program and erase voltage (the electric field is more than 6 MV/cm). In order to solve these problems and realize vertical scaling, the conductive poly-Si floating gate is replaced by Si_3N_4 to form the [poly-Si/metal]-SiO_2-Si_3N_4-SiO_2-Si structure; we call the SONOS or MONOS memory devices (the structure is shown in Fig. 1-3). The SONOS/MONOS device is a potentially important non-volatile memory suitable for downscaling below 20 nm [1.3]-[1.7] since the discrete traps in the silicon nitride can prevent complete charge leakage out through single oxide defects, which gives better data retention and useful for 2 bits/cell. Thus a thinner tunnel oxide (<5 nm) can be used in a SONOS/MONOS memory compared with that in a conventional poly-Si floating gate device. This yields lower voltage and faster speed for operation. According to International Technology Roadmap for Semiconductors (ITRS) [1.8], at 2020, the SONOS non-volatile memory will continue

down-scaling the thickness of tunnel oxide to 2 nm and program/erase (P/E) voltage to 4.0-4.5 V (the table is shown in Fig. 1-4) with faster speed while maintaining good data retention at elevated temperature. Such low voltage operation under 5 V is also important for embedded system-on-chip (SoC).

1.2 Motivation to use High-κ materials for MONOS Flash memory

The SONOS/MONOS memory device still faces some challenges for further improvement. The tunnel oxide needs to be scaled more aggressively to improve the program/erase speeds. However, the tunnel oxide thickness cannot be reduced below 2nm to improve the programming speed, if ten years retention time must be guaranteed. The tunnel oxide scaling may not help the programming speed significantly, as shown in Fig. 1-5. The programming speed enhancement from the tunnel oxide scaling is limited since electrons must tunnel through a significant portion of the nitride (shown in the dark gray area) before becoming trapped, especially for low programming voltages. This programming mechanism is called the modified Fowler-Nordheim tunneling process [1.9]. If the tunnel oxide is scaled to improve the programming speed, less voltage will be dropped across the tunnel oxide (see the energy band diagram shown with the dashed line in Fig. 1-5), assuming the same electric field is maintained during programming. As shown by the light gray area in the figure, there will be a larger tunnel barrier within the nitride charge trap

layer for the scaled device. This larger barrier reduces the electron tunneling probability and hence the electron injection current during programming. Therefore the advantage of using a thin tunnel oxide to improve the programming speed is offset by the existence of the nitride tunnel barrier. To mitigate this effect, a larger conduction band offset ϕ_0 between the tunnel oxide and the charge trap layer is desirable to reduce (or eliminate) the extra tunnel barrier from the charge trap layer during programming. The offset ϕ_0 between the tunnel oxide and the nitride charge trap layer is only 1.1 eV.

A larger ϕ_0 is also desirable to mitigate the trapped electron leakage during retention. There are two charge-loss mechanisms: (1) direct tunneling, with an associated barrier height; and (2) thermally assisted de-trapping into the nitride conduction band and subsequent tunneling through the tunnel oxide, with associated barrier height ϕ_0. Thus a larger conduction-band offset ϕ_0 between the charge trap layer and the tunnel oxide is essential for achieving a longer retention time.

Consequently, in order to improve both the programming speed (with a low programming voltage) and the retention time, it is desirable to use a charge trap material with a lower conduction band edge (higher electron affinity) to achieve a larger offset ϕ_0. Recently, high-κ dielectric materials such as HfO_2 and ZrO_2 have been investigated to replace thermal oxide as the MOSFET gate dielectric

[1.10][1.11]. Such materials have a lower conduction band edge than that of silicon nitride. A comparison of some dielectric material properties is given in Fig. 1-6.

1.3 The measurement of the devices

To investigate the electrical characteristics of devices, we measured the I_g-V_g curves for gate leakage current and I_d-V_g for transistor characteristics by using HP 4156A semiconductor parameter analyzer. Besides, HP4284A precision LCR meter was used to evaluate the gate capacitance and the conductance ranging from 100 kHz to 1 MHz. For memory measurement, the fabricated MONOS devices were characterized by program/erase measurements, cycling and retention tests at 85°C , 125°C and 150°C as well as read disturbance and interface trap density generation analysis by charge pumping method using the HP4156A Semiconductor Parameter Analyzer and the HP81110A Pulse Pattern Generator.

1.4 Overview of Dissertation

This dissertation addresses the aforementioned issue of gate stack scaling future generations of semiconductor flash memory, and proposes solutions based on new memory structures and new materials that are compatible with the current CMOS process flow. In Chapter 2, we describe a programmable-erasable MIS capacitor with a single high-κ. $Hf_{0.3}N_{0.2}O_{0.5}$ dielectric layer. This device showed a capacitance density of ~ 6.6 fF/μm^2, low program and erase voltages of +5 and -5 V, and a large V_{fb} memory window of 1.5 V. In addition the 25^{o}C data retention was good, as

indicated by program and erase decay rates of only 2 and 6.2 mV/dec. Such device retention is attributed to the deep trapping level of 1.05 eV in the $Hf_{0.3}N_{0.2}O_{0.5}$.

In Chapter 3, we studied the dependence of different N composition on TaN-HfLaON-$Hf_{1-x-y}N_xO_y$-SiO_2-Si MONOS memory device characteristics. The increasing N composition in the $Hf_{1-x-y}N_xO_y$ trapping layer improves both memory window and high temperature retention. The $Hf_{0.3}N_{0.2}O_{0.5}$ MONOS device displays excellent characteristics in terms of a low ±9 V program/erase (P/E) voltage, fast 100 μs P/E speed, large initial 2.8 V memory window, good 10-year extrapolated retention of 1.8 V at 85°C or 1.5 V at 125°C.

In order to further improve the high temperature data retention with good program/erase speed. In Chapter 4, the HfAlO/SiO_2 double-tunneling and HfAlO/$LaAlO_3$ double-blocking layers are incorporated in a MONOS non-volatile memory device structure with high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ charge storage layer for NAND-type memory application. High program/erase speed and good retention characteristics at high temperature are obtained. At 125°C under very fast 100μs low ± 8V program/erase, the [TaN-Ir_3Si]-HfAlO-$LaAlO_3$-$Hf_{0.3}N_{0.2}O_{0.5}$-HfAlO-SiO_2-Si device shows good memory device integrity of a 2.6V initial ΔV_{th} and 1.9V 10-year extrapolated retention. This only 27% retention decay at 125°C was achieved by double quantum- barriers confining the deep-trapping-energy $Hf_{0.3}N_{0.2}O_{0.5}$ well.

A comparison between single and double quantum barriers charge-trapping MONOS structured memory devices was mentioned in Chapter 5. The [TaN-Ir_3Si]-[HfAlO-$LaAlO_3$]-$Hf_{0.3}N_{0.2}O_{0.5}$-[HfAlO-SiO_2]-Si charge-trapping memory devices display good characteristics in terms of their ±9 V program/erase (P/E) voltage, 100 μs P/E speed, and initial 3.2 V memory window, and a 10-year extrapolated data retention window of 2.4 V at 150^{o}C. The retention decay rate is significantly better than single-barrier MONOS devices, as is the cycled retention data, due to the reduced interface trap generation.

The dissertation is concluded with a summary of the major results in Chapter 6.

Fig. 1-1 The electrical products of nonvolatile Flash memory application.

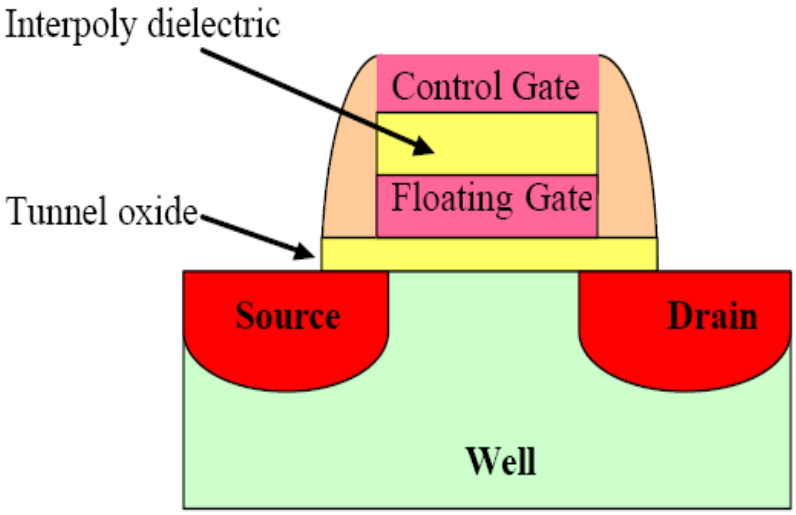


Fig. 1-2 Schematic cross-section of a floating gate memory device. It is essentially a MOSFET, except that a floating gate is sandwiched between a tunnel oxide and an inter-poly oxide.

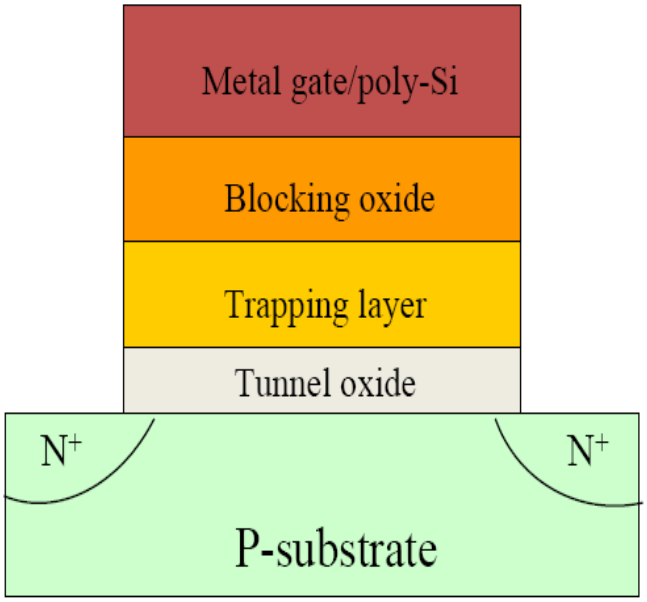


Fig. 1-3 The cross section of [Metal gate/poly-Si]-SiO_2-Si_3N_4-SiO_2-Si memory.

Year of Production	2014	2015	2016	2017	2018	2019	2020
SONOS/NROM technology – F (nm) [34]	32	28	25	23	20	19	18
SONOS/NROM cell size – area factor a in multiples of F^2 [35]	6.5	6.5	7	7	7	7	7
SONOS/NROM typical cell size (μm^2) [36]	0.007	0.005	0.004	0.0037	0.003	0.0025	0.002
SONOS/NROM maximum number of bits per cell ((physical 2-bit/cell) x MLC) [37]	4	4	4	4	4	4	4
SONOS/NROM area per bit (μm^2) [38]	0.0018	0.0013	0.0011	0.0009	0.0007	0.0006	0.0005
SONOS L_g-stack (physical – μm) [39]	0.15	0.15	0.14	0.14	0.14	0.13	0.13
SONOS highest W/E voltage (V) [40]	5.0–5.5	5.0–5.5	4.5–5.0	4.5–5.0	4.0–4.5	4.0–4.5	4.0–4.5
SONOS/NROM I_{read} (μA) [41]	23–33	22–32	21–31	21–31	20–30	20–30	20–30
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
SONOS/NROM tunnel oxide thickness (nm) [42]	3	3	2.5	2.5	2.5	2	2
SONOS/NROM nitride dielectric thickness (nm) [43]	4	4	4	4	4	4	4
SONOS/NROM blocking (top) oxide or dielectric thickness (nm) [44]	6	6	5	5	5	5	5
SONOS/NROM endurance (erase/write cycles) [45]	1.00E+08	1.00E+08	1.00E+09	1.00E+09	1.00E+09	1.00E+09	1.00E+09
SONOS/NROM nonvolatile data retention (years) [46]	10–20	10–20	10–20	10–20	10–20	10–20	10–20

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Fig. 1-4 The requirements for SONOS memory (the international technology roadmap for semiconductors:2006 update).

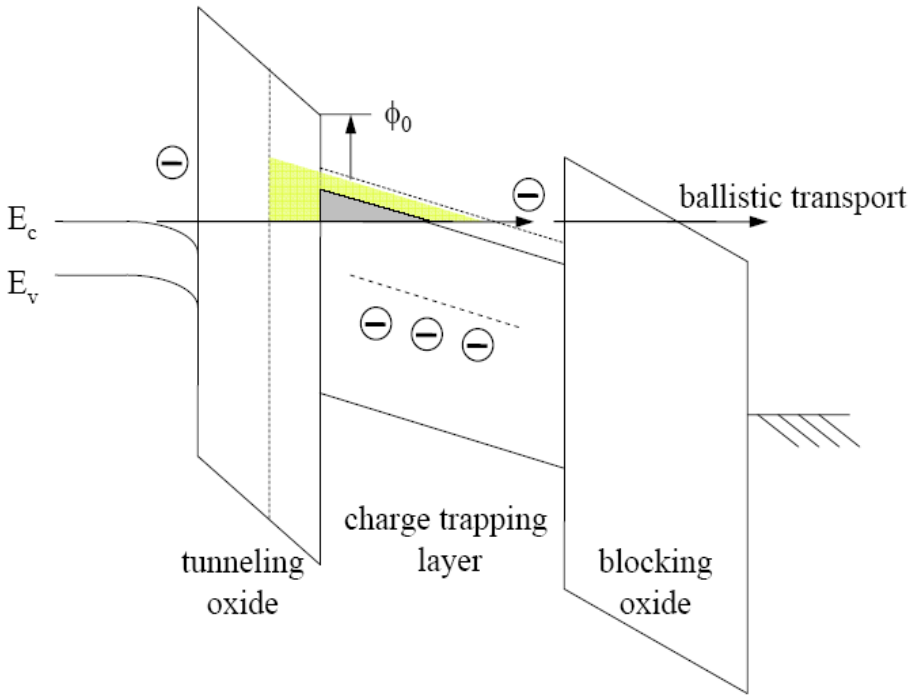


Fig. 1-5 When the tunnel oxide is scaled, the voltage drop across it is reduced for the same programming voltage. This increases the nitride tunnel barrier, as shown by the light gray area. The benefit from tunnel oxide scaling is significantly reduced due to the nitride barrier.

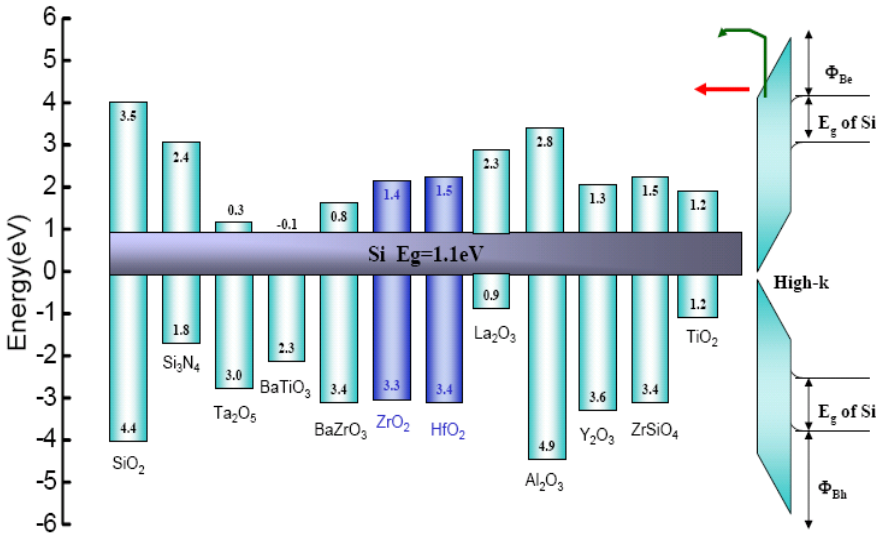


Fig. 1-6 The band offset of popular high-κ materials.

Chapter 2

A Program-Erasable High-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS Capacitor with Good Retention

2.1 Introduction

Capacitors are essential devices for various analog, RF and DRAM functions [2-1]-[2-8] in circuits. It is also desirable to have a program-erasable, non-volatile memory (NVM) function [2-9]-[2-17], in order to integrate low-cost embedded Flash memory into CMOS technology. To address these issues we have previously described a program-erasable AlN Metal-Insulator-Si (MIS) capacitor which used a charge-trapping mechanism [2-9]-[2-11]. Although small degradation was achieved at room temperature and much better than an SiN MIS device [2-17], the data retention at 100^{o}C was poor due to charge de-trapping. Recently, an HfNO MONOS NVM with a lower N content (<10%) has been demonstrated with a record low program/erase (P/E) voltage, at a speed of 100 μs [2-16]. In this paper we describe an improved device which incorporates a high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ with a large N content of 20%, where a deeper trapping energy and/or a smaller band offset are expected from increasing the N% [2-14]-[2-16]. A large memory window, with a flat-band voltage difference (ΔV_{fb}) of 1.5 V, was measured under ± 5 V and 1 ms P/E conditions. Furthermore, the data

retention showed very small P and E decay rates (2 and 6.2 mV/dec) at 25°C and still good at 100°C with small 104 and 116 mV/dec values [2-11]-[2-16]. The better high temperature retention than that of AlN MIS capacitor was due to the deep trapping energy of the $Hf_{0.3}N_{0.2}O_{0.5}$.

2.2 Experimental Details

The MIS devices were formed by sputter-depositing a ~29 nm thick $Hf_{1-x-y}N_xO_y$ dielectric on Si substrate, under mixed O_2 and N_2 with controlled O_2/N_2 flow ratio. After a post-deposition anneal (PDA), a TaN layer was deposited and patterned to form the top electrode. Finally, the devices were given an RTA at 900°C for 30 sec to evaluate the thermal stability. X-ray photoelectron spectroscopy (XPS) was used to determine that the composition was $Hf_{0.3}N_{0.2}O_{0.5}$. The HfNO for NVM [2-16] is different from that used as a CMOS gate dielectric [2-18]-[2-19]: the former is optimized for large charge-trapping, with a high N content, while the latter requires a small N% to improve the high-temperature stability to give a low trap density. The HfNO with N=20% is chosen by considering the increasing trapping energy with N% increase, but low enough to prevent metallic conduction. The formed HfNO shows good reproducibility by controlling the O_2/N_2 flows during reactive sputtering from an Hf target [2-16]. Even better reproducibility can be reached by Atomic Layer Deposition (ALD). The fabricated 100-μm×100-μm devices were characterized by

C-V and *J-V* measurements. A pulse generator was used for the P/E study.

2.3 Result and Discussion

Figures 2-1(a) and 2-1(b) show the *C-V* characteristics and ΔV_{fb}-time dependences of the high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitors, respectively. The devices showed a capacitance density of 6.6 fF/μm^2 and a κ value of ~22. The $|V_{fb}|$ increases with P/E time, as does ΔV_{fb} with increasing P/E voltage. This suggests that the V_{th} shift mechanism is caused by charge-trapping. We found a switching speed of ~ 1 ms, due to the rapid increase of ΔV_{fb} between 0.1 to 1 ms and the approximate saturation for times from 1 to 100 ms. From the ΔV_{fb} shift for P/E conditions of ± 5 V for 1ms, a memory window of 1.5 V was measured - which is larger than that of an AlN device [2-9] and is comparable with certain SONOS NVM [2-13] data. Note that both the 6.6 fF/μm^2 capacitance density and the 9X tunability are larger than those for current varactors made in IC foundries [2-20] (typical only 1.3 fF/μm^2 density and 2.1X tunability), and are comparable with values for advanced varactors [2-21]-[2-22]. The 5 V operation voltage is also useful for certain I/O circuits and is suitable for RF IC.

Figures 2-2(a) and 2-2(b) show the retention and cycling characteristics. The retention data indicates P and E decay rates of only 2 and 6.2 mV/dec, at 25^{o}C. At 100^{o}C, still good P and E decay rates of 104 and 116 mV/dec are obtained [2-11]-[2-13]. Moreover, the retention of this $Hf_{0.3}N_{0.2}O_{0.5}$ device is significantly

better than that of an AlN MIS capacitor, which had a closed memory window at 10000s at 100°C. A memory window of 1.3 or 0.9 V was preserved under ±5 or ±4 V 1 ms P/E for 10^3 cycles respectively, indicating the good device characteristics. Note that the use of a higher N% in HfNO did not degrade the erase speed and reliability. From previous T-Supreme and Medici simulation, the erase mechanism is primary due to hole injection from the Si-channel [2-15]. Therefore, the cycling stress reliability is comparable with our results for AlN. We note that the cycling characteristics can be improved by adding a thin tunnel oxide at the HfNO/Si interface, similar to MONOS [2-14]-[2-17] and double tunneling TANOS cases [2-25].

To understand the good retention we plot the $ln(J)$-$E^{1/2}$ relation in Fig. 2-3, using the measured *J-V* data. The linear $ln(J)$-$E^{1/2}$ relations fit a Schottky emission (*SE*) or Frenkel-Poole (*FP*) conduction [2-8] model at 25, 45, 65 and 85°C. In the expression

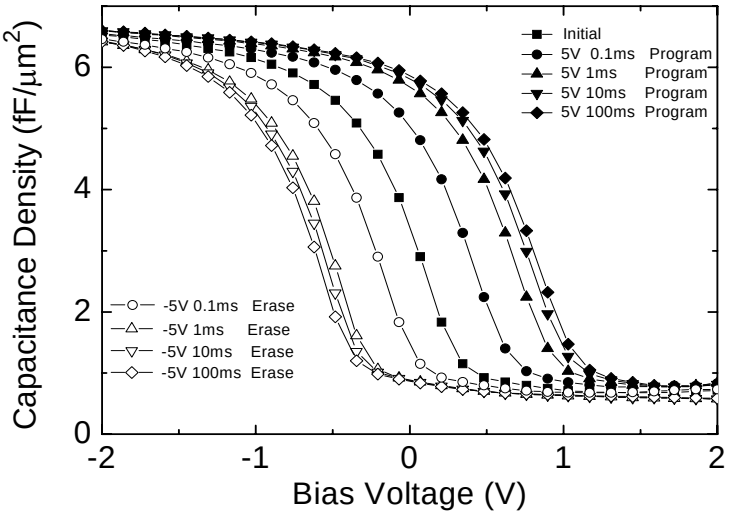
$$J \propto \exp[(\gamma E^{1/2} - q\varphi_{b,t}) / kT]; \qquad \gamma = (q^3 / \eta\pi\varepsilon_0\kappa_\infty)^{1/2} \tag{1}$$

$\eta = 1$ for the *FP* case and 4 for the *SE* case respectively, implying different slopes (γ) in a $ln(J)$-$E^{1/2}$ plot. The extracted low-field *SE* barrier height $q\varphi_b$ and high-field *FP* trap energy $q\varphi_t$ are plotted in the inserted figure. The data give a small *SE* barrier height of 0.7 eV and a dominant *FP* trap energy of 1.05 eV. The small barrier height, deep trap energy, and the corresponding better retention data suggest that the trap

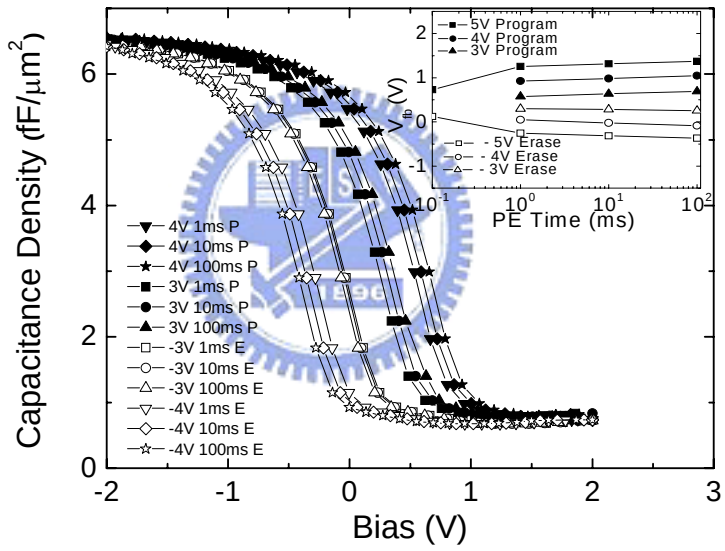
energy is deeper than that in our previous AlN MONOS [2-14]-[2-15]. The merit of using the $ln(J)$-$E^{1/2}$ relation for extracting the trap energy and barrier height is its accuracy (<6~12% error for changing dielectric thickness by more than 2X [2-23]) and a simple experimental setup, compared with methods requiring both high resolution x-ray spectroscopy (XPS) and reflection electron energy loss spectroscopy (REELS) [2-24].

2.4 Conclusions

We have demonstrated a program-erasable $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor with good 100°C data retention and high 6.6 fF/μm^2 density. This new capacitor should find wide application for analog, RF, DRAM and low-cost embedded Flash memory.

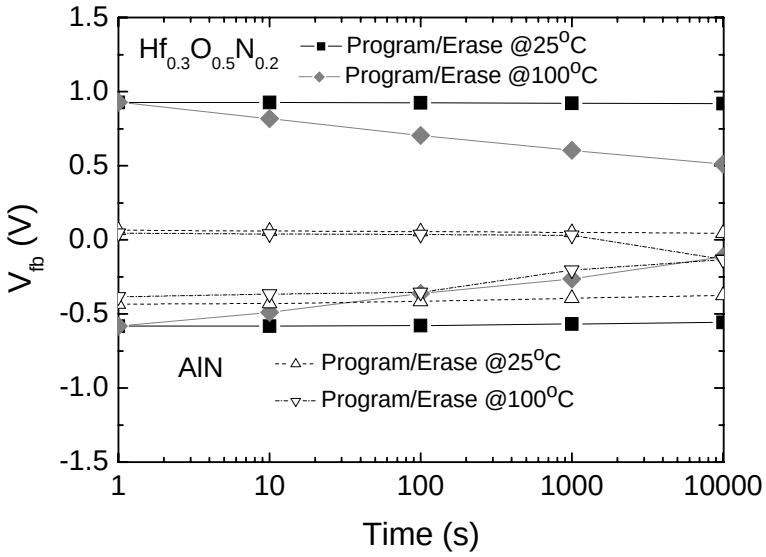


(a)

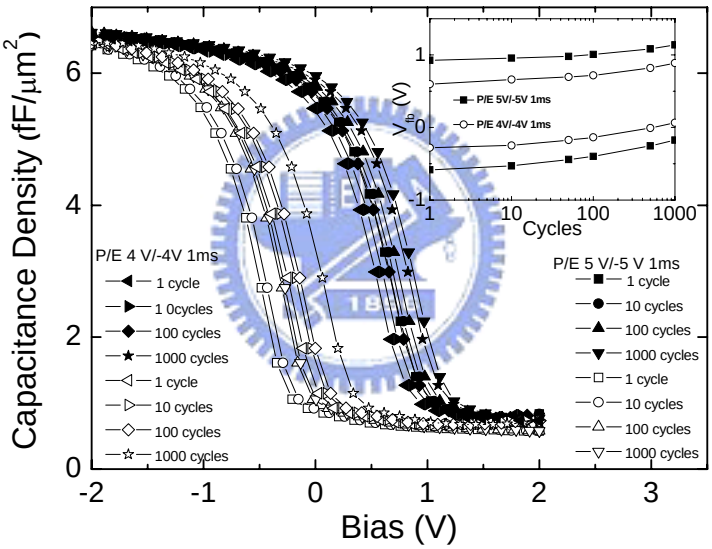


(b)

Fig. 2-1. (a). The *C-V* characteristics of an $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor after applying a ± 5 V program/erase (P/E) voltage for various periods from 0.1 to 100 ms. (b). The *C-V,* for various P/E voltages from ± 3 to ± 5 V, as a function of the P/E time. The insert shows the V_{fb}-*P/E time* plot.



(a)



(b)

Fig. 2-2. (a) Retention characteristics at 25 and 100°C of an $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor, measured to 10000 s, after a 1 ms, ± 5 V P/E writing pulse; (b) cycling characteristics of the $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor. Data for an AlN

MIS capacitor are shown for comparison in (a). The insert in (b) shows the variation of V_{fb} with cycling.

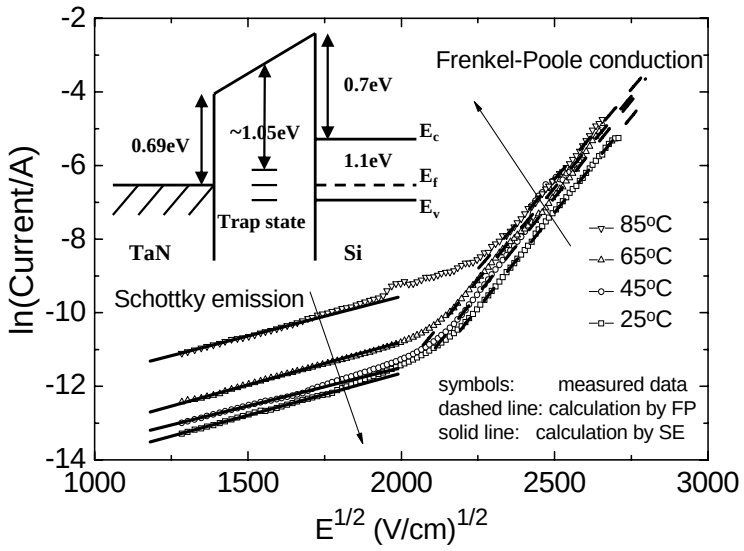


Fig. 2-3. A ln(*J*)-$E^{1/2}$ plot, using the measured *J-V* of a TaN/$Hf_{0.3}N_{0.2}O_{0.5}$/Si MIS device, where the electron injection is from the Si. Calculated data using both Schottky Emission (*SE*) and Frenkel-Poole (*FP*) conduction models are included. The inserted figure shows the band diagram of the $Hf_{0.3}N_{0.2}O_{0.5}$ MIS devices, where the barrier height and trap energy were obtained from *SE* and *FP* fits to the measured data.

Chapter 3

Comparison of MONOS Memory Device Integrity when Using $Hf_{1-x-y}N_xO_y$ Trapping Layers with different N Compositions

3.1 Introduction

Poly-Si/SiO_2/Si_3N_4/SiO_2/Si (SONOS) devices [3-1]-[3-13] are promising for non-volatile memory applications as scaling decreases below 50 nm. This is because of the merit of charge storage in discrete traps within the Si_3N_4, which prevents charge leakage through a single oxide defect, as compared with the conventional poly-Si floating gate memory case. By replacing the poly-Si in SONOS with a high work-function metal-gate (MONOS), further improvements of the erase performance can be achieved by decreasing the electron injection over the gate. However, one difficulty in SONOS or MONOS is the small conduction band discontinuity (ΔE_C) of only 1.1 eV at the Si_3N_4/SiO_2 interface [3-14], which causes charge leak out from shallow trap levels near E_C of Si_3N_4. In contract, a conventional poly-Si floating gate device has a much deeper energy of ~3.15 eV for storage of charge. Therefore, the high temperature retention is a serious concern for a shallow trap energy MONOS device that uses a Si_3N_4. To address this requires the use of a thick SiO_2 tunnel layer to improve the charge storage, but unfortunately this leads to a performance

degradation of increased program/erase (P/E) voltage and write speed. This is contrary to the scaling trend indicated in the International Technology Roadmap for Semiconductors (ITRS) [3-1]. To over come this problem, we have previously proposed using an Al(Ga)N [3-11]-[3-12] storage layer which has deeper ΔE_C than Si_3N_4. This improved the P/E voltage, and write speeds in such deep-trap MONOS devices. Unfortunately, further improvement beyond Al(Ga)N [3-12] is limited since most of the Metal-Nitrides are metallic. To avert this problem, we used a higher κ $Hf_{1-x-y}N_xO_y$ dielectric for MONOS applications, where even lower P/E voltages and better high temperature retention can be achieved [3-13]. Here we increase the nitride composition in the $Hf_{1-x-y}N_xO_y$ beyond that of our previous work [3-13] and investigate how this alters the characteristics. Our TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si MONOS device showed a large initial memory window of 2.8 V at 100 μs and a low ±9 V P/E. The 10-year extrapolated retention of 1.8 V at 85°C or 1.5 V at 125°C compare well with other published data [3-1]-[3-13].

3.2 Experimental Details

The fabrication process of the TaN-HfLaON-$Hf_{1-x-y}N_xO_y$-SiO_2-Si MONOS devices was similar to previous work [3-11]-[3-13]. First, a 2.9 nm thick thermal SiO_2 was grown on a standard p-Si substrate. Then a 9 nm $Hf_{1-x-y}N_xO_y$ layer was deposited by reactive sputtering, under a mixed O_2 and N_2 conditions [3-13] with different

O_2/N_2 ratios - to study the N% dependence of the MONOS device integrity. (The detailed composition of N and O in the $Hf_{1-x-y}N_xO_y$ was measured by X-ray photoelectron spectroscopy (XPS)). A 15 nm HfLaON [3-15] blocking oxynitride was included because of its good thermal stability at 1000°C and its higher κ than the previous-used HfAlO. Finally, a 150 nm TaN layer was added by sputtering. After standard processing, the MONOS devices were made by self-aligned As^+ ion implantation and given a 950°C rapid thermal annealing (RTA) activation to form the S/D regions. The memory devices were characterized by different P/E tests, retention experiments and cycling endurance at 25, 85 and 125°C.

3.3 Result and Discussion

A. Engineering the trap energy:

Figure 3-1(a) shows a schematic energy band diagram of a conventional SiN trapping layer MONOS device. The SiN trapping layer has a small ΔE_C with respect to the barrier oxide of only 1.1 eV, and many traps in deep as well as in shallow energy levels. Since the trap energy is distributed statistically, it is difficult to tune the trap energy to involve only deep energy levels. Thus, the SiN MONOS devices are expected to have poor retention properties because of the small ΔE_C and charge loss from shallow energy levels, unless a very thick barrier oxide is used to trade-off the poor P/E voltage and speed. However, this is not consistent with scaling trends and system-on-chip (SoC) requirements, where lower P/E voltages and faster

P/E speeds are needed. These are the fundamental challenges for conventional SiN charge-trapping MONOS devices.

To address these issues, we previously proposed and demonstrated the use of a deep trapping metal-oxide instead of a nitride. Figure 3-1(b) shows the band alignment with respect to the barrier oxide and Si channel [3-12]-[3-13], [3-16]. Although the trap energy is distributed statistically from levels which are shallow to ones that are deep, the ΔE_C in AlN and Al(Ga)N is improved when compared with SiN. Since the electron injection through the oxide follows an exponential dependence with barrier height, a large ΔE_C with deeper trapping energy is the key factor in improving the retention in charge-trapping MONOS devices. This is confirmed by the >5 times better retention when using GaN instead of SiN, as suggested by the data from Samsung [3-16] and also verified by previously-reported SiO_2/AlN/HfAlO/TaN [3-11] and SiO_2/AlGaN /$AlLaO_3$/TaN [3-12] MONOS memory devices. However, the P/E voltage is still relatively high compared with the target of 4.0-4.5 V for MONOS devices by the year 2018, according to the ITRS roadmap [3-1]. Such low voltage operation (under 5 V) is also important for embedded SoC. To continue the improvement of memory device characteristics - in terms of lower P/E voltage and increased speed - we have proposed using HfNO instead of Al(Ga)N. This is because of the twice as high κ value compared with Al(Ga)N, which reduces the P/E voltage

and improves the speed. This is demonstrated experimentally by the low 8 V P/E voltage over the gate-channel (or half that, ±4 V, by using an inverter circuit and applying the different polarity voltages to the gate and the channel) and the < 100 μs P/E speed [3-13]. Improved retention can be achieved by lowering the ΔE_C, which may be accomplished by increasing the N content in the HfNO [3-17]. This has been confirmed by recent measurements of the conduction band offset of 0.7 eV for $Hf_{0.3}N_{0.2}O_{0.5}$ [3-18] – which is significantly lower than the 1.5 eV value for HfO_2.

B: P/E characteristics:

We first determined the N composition in the $Hf_{1-x-y}N_xO_y$. Figure 3-2 shows the XPS spectra of $Hf_{1-x-y}N_xO_y$ with two different N_2/O_2 flow rates. The existence of Hf, N and O are clear in the XPS spectra, where the compositions were determined to be $Hf_{0.35}N_{0.10}O_{0.55}$ and $Hf_{0.30}N_{0.20}O_{0.50}$ ($Hf_{0.3}N_{0.2}O_{0.5}$ in short). This was done by performing a Compass software calculation on the measured XPS data. These two compositions of the $Hf_{1-x-y}N_xO_y$ trapping layer MONOS devices were used in the following studies.

Figures 3-3(a) and 3-3(b) show the *C-V* hysteresis characteristics of the MONOS capacitor with different trapping layers of $Hf_{0.35}N_{0.10}O_{0.55}$ and $Hf_{0.3}N_{0.2}O_{0.5}$, respectively. The *C-V* hysteresis window increases with increasing voltage, indicating the good charge storage. The *C-V* hysteresis window of 2.4 and 6.5 V was measured

under swept voltages of ±10 V in $Hf_{0.35}N_{0.10}O_{0.55}$ and $Hf_{0.3}N_{0.2}O_{0.5}$ respectively. A similar capacitance density of ~4.2 fF/μm^2, found in both devices, ensures that the large hysteresis window was not due to process variations in the MONOS structure. Hence the large increase in hysteresis window must be due to the different $Hf_{1-x-y}N_xO_y$ trapping layer in the MONOS, which then suggests a higher trap density and/or deeper trap energy in $Hf_{1-x-y}N_xO_y$ with increasing N/O ratio [3-11]-[3-13].

The P/E characteristics at various gate voltages are shown in Figs. 3-4 and 3-5 for $Hf_{0.35}N_{0.10}O_{0.55}$ and $Hf_{0.3}N_{0.2}O_{0.5}$trapping layer MONOS devices, respectively. The program or erase functions were achieved through a Fowler-Nordheim (FN) tunneling mechanism, where a positive or negative voltage pulse, with various pulse widths, was applied between the gate and the channel. During programming an electron inversion channel was formed by biasing the source-drain electrodes, where the positive gate-channel bias voltage permitted inversion electron injection into the trapping layer.

In both cases the threshold voltage (V_{th}) increases with increasing P/E voltage and time - this is typical for MONOS memory devices. For the $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layer MONOS device, a memory window of 2.1 V was obtained at ±9 V for only 100μs P/E. For comparison, the $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer MONOS device showed a larger ΔV_{th} memory window of 2.6 V at a lower P/E voltage of ±8 V under

1-ms/100-μs speed, which increases to 2.8 V at ±9 V 100 μs P/E. The larger memory window suggests a higher trap density in the $Hf_{1-x-y}N_xO_y$ with the higher N composition. This result compares well with our previous TaN-AlHfO-HfON-SiO_2-Si devices that had a thicker trapping layer [3-13]. The low P/E voltage indicates a small voltage drop in the HfLaON(κ=22)-$Hf_{0.3}N_{0.2}O_{0.5}$(κ~22), leading to fast P/E functions due to the large electric field over the SiO_2 tunnel layer. Such a low P/E voltage is valuable for under 5 V embedded SoC operation, where an inverter circuit with opposite polarities of 4~4.5 V can be used between the gate and the channel [3-13].

C: Data retention and endurance:

Data retention is one of the most important parameters for nonvolatile memory. Figure 3-6 shows the retention behavior of the $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layer MONOS device. The initial ΔV_{th} was 2.1 V under 100 μs and ±9 V P/E, and the extrapolated 10-year memory windows 1.2 V and 1.0 V at 25 and 85°C, respectively. The good retention is due to the small decay rate of 98 and 42 mV/dec at 85°C for the high and low states, respectively.

For comparison, in Figs. 3-7(a) and 3-7(b) we show the retention data of a $Hf_{0.3}N_{0.2}O_{0.5}$ MONOS device at 25 and 85~125°C, respectively. The extrapolated 10-year memory window at 25°C increased from 1.7 to 2.1 V with increasing P/E conditions from ±8 V 500 μs/100 μs to ±9 V 100 μs/100 μs. At 85°C, the 10-year

window was still large at 1.8 V under 100 μs ±9 V P/E. Even at 125°C, a 1.5 V 10-year window was obtained. Therefore, not only the room temperature but also the high temperature retention characteristics can be improved by using a higher N% $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer in a MONOS device than one with a $Hf_{0.35}N_{0.10}O_{0.55}$ composition. The decay rates were 52, 92 and 110 mV/dec for the high state and 27, 36 or 55 mV/dec for the low state, under 100μs ±9 V P/E at 25, 85, and 125, respectively. This is an improvement compared with other devices having a thin tunnel SiO_2, as detailed in Table 1 [3-5]-[3-7], [3-11]-[3-13]. The 85 and 125°C retention decay rate are also better than previous deep-trap AlGaN and HfNO data [3-11]-[3-13]. Improved retention characteristics could thus be expected.

We have also measured the endurance characteristics of the TaN-HfLaON-$Hf_{1-x-y}N_xO_y$-SiO_2-Si MONOS devices with the different trapping layers. As shown in Fig. 3-8, good endurance was obtained – as is evident from the still large memory window of 2.4 and 1.7 V after 10^5 cycles at ±9 V 100 μs P/E for $Hf_{0.3}N_{0.2}O_{0.5}$ and $Hf_{0.35}N_{0.10}O_{0.55}$ MONOS devices, respectively. The stress-induced degradation of the non-volatile memory devices is normally related to interface trap generation at the tunnel oxide-Si interface. We suggest that the good cycling characteristics are due to the fast 100 μs P/E functions where less stress is applied to the thin SiO_2 tunnel layer.

To study the possible read disturbance [3-19]-[3-20], we have measured the

device following the gate stress disturbance condition at the current density of 100-nA/(15-nm)^2 [3-19]. This is because similar low voltage P/E at 10 V/-9 V was also reported in reference [3-20] and close to our 9 V/-9 V P/E condition. Figure 3-9 shows charge retention in gate stress conditions of our memory device, where the P/E voltage is increased to higher 10 V/-10 V. The stored charges were not lost largely as evident from the small V_{th} change even after 1000 seconds gate stresses. Therefore, similar to previous conclusion [3-19], the read disturbance is not a severe concern. The retention and endurance characteristics of TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si devices at worse 10 V and 100 μs P/E were shown in Figs. 3-10(a) and 3-10(b) respectively.

Table 3-1 compares the memory device data. The SiO_2/$Hf_{0.3}N_{0.2}O_{0.5}$/HfLaON/TaN device shows good integrity in terms of its 100 μs P/E speed, low ±9 V P/E voltage, large 2.8 V initial ΔV_{th} and good 10-year memory window of 1.8 V at 85^{o}C or 1.5 V at 125^{o}C. The 36%~46% retention decay rates at 85~125^{o}C are among the best in Table 3-1 [3-5]-[3-7], [3-11]-[3-13].

3.4 Conclusions

Improved memory performance in a MONOS device has been obtained by using a high N/O ratio $Hf_{0.3}N_{0.2}O_{0.5}$ dielectric as the trapping layer. Compared with devices using a low N/O ratio $Hf_{0.35}N_{0.10}O_{0.55}$ layer, the $Hf_{0.3}N_{0.2}O_{0.5}$ MONOS devices

showed a wider memory window and a smaller high temperature decay rate. Our TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si MONOS device has potential for nonvolatile memory applications.

Table 3-1. Comparison of memory characteristics for the $Hf_{0.3}N_{0.2}O_{0.5}$, $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layer MONOS device with other state-of-the-art devices.

	P/E condition for retention & cycling	Initial ΔV_{th} (V)	ΔV_{th} (V) for 10-years @ 85°C	P/E decay after 10-years @ 85°C	P/E decay after 10-years @ 125°C
This Work $SiO_2/Hf_{0.3}N_{0.2}O_{0.5}$/ HfLaON/TaN	**9V 100μs/ -9V 100μs**	**2.8**	**1.8**	**36%**	**46%**
	10V 100μs/ -10V 100μs	**3.0**	**1.9**	**37%**	**47%**
This Work $SiO_2/Hf_{0.35}N_{0.10}O_{0.55}$/ HfLaON/TaN	**9V 100μs/ -9V 100μs**	**2.1**	**1.0**	**52%**	**-**
$SiO_2/Si_3N_4/Al_2O_3$/TaN TANOS [5]	13.5V 100μs/ -13V 10ms	4.4	2.07	53%	-
SiO_2/ Si_3N_4/ SiO_2 FinFET SONOS [6]	13V 10μs/ -12V 1ms	4.5	2.4	47%	-
$SiO_2/Si_3N_4/SiO_2$ Tri-gate MONOS [7]	11.5V 3ms/ -11.5V 100ms	1.2	1.1 (@25°C)	8% (@25°C)	-
SiO_2/AlN/AlHfO/IrO_2 [11]	13V 100μs/ -13V 100μs	3.7	1.9	48%	-
SiO_2/AlGaN/$AlLaO_3$ [12]	11V100μs/ -11V 100μs	3.0	1.6	46%	-
SiO_2/HfON/AlHfO/TaN [13]	8V 100μs/ -8V 100μs	2.5	1.45	42%	60%

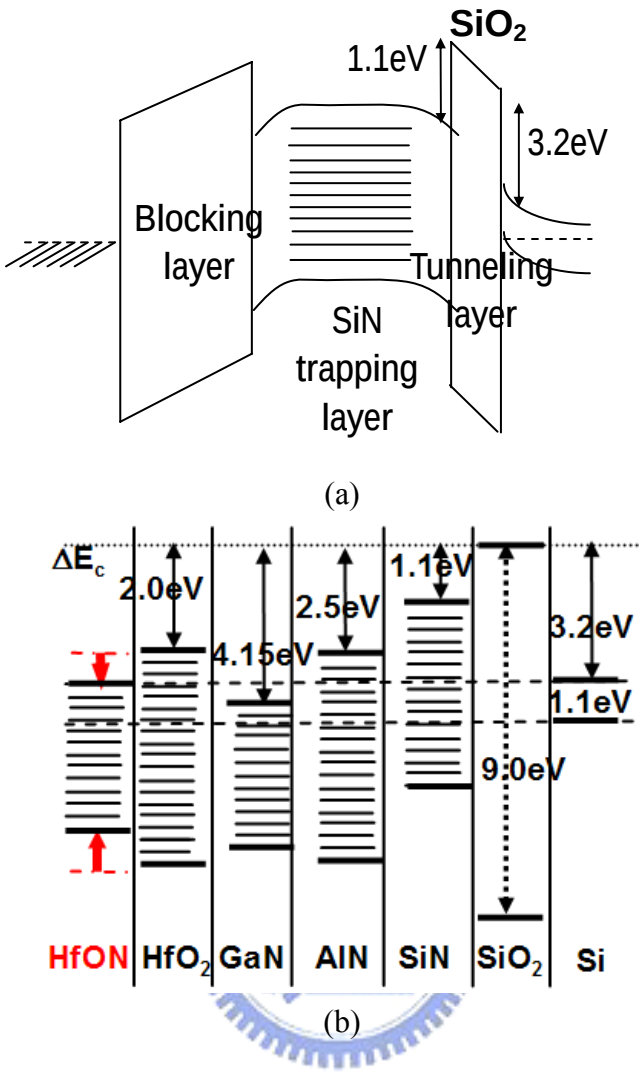


Fig. 3-1. (a) Schematic band diagram of a SiN trapping layer MONOS device and (b) the band alignment of various metal-oxide trapping layers to the oxide barrier and Si channel.

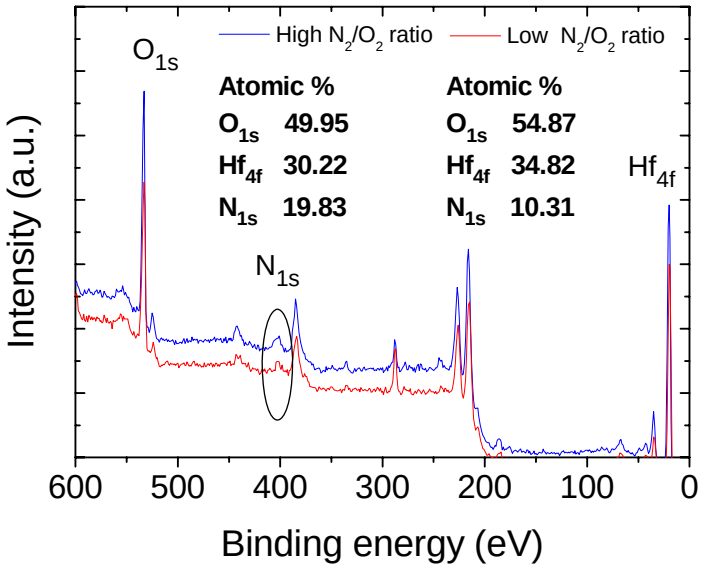
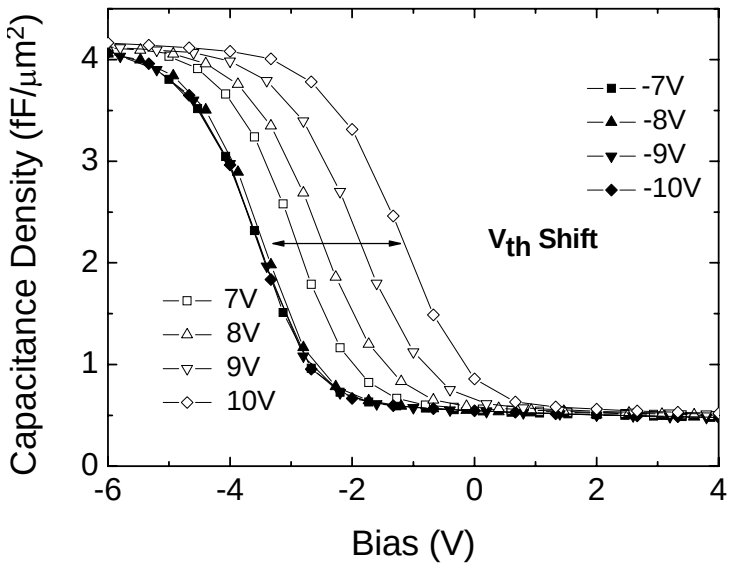
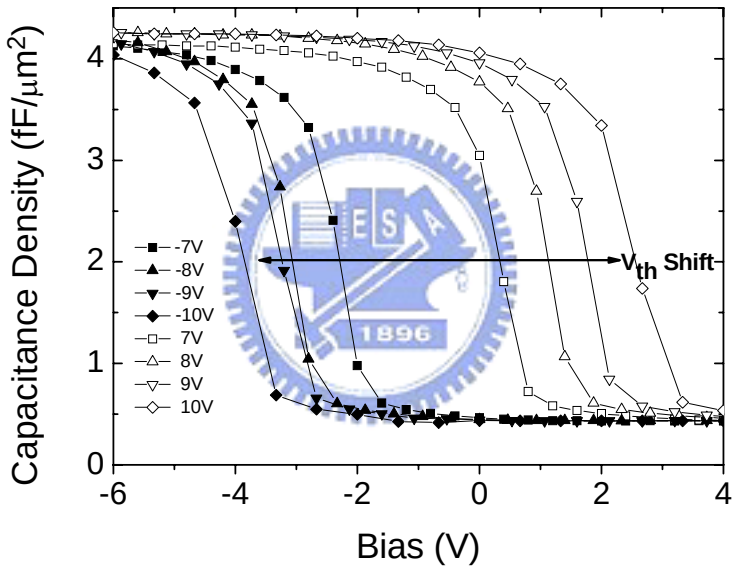


Fig. 3-2. XPS spectra of $Hf_{1-x-y}N_xO_y$, where the composition of $Hf_{0.30}N_{0.20}O_{0.50}$ and $Hf_{0.35}N_{0.10}O_{0.55}$ was determined from the data.

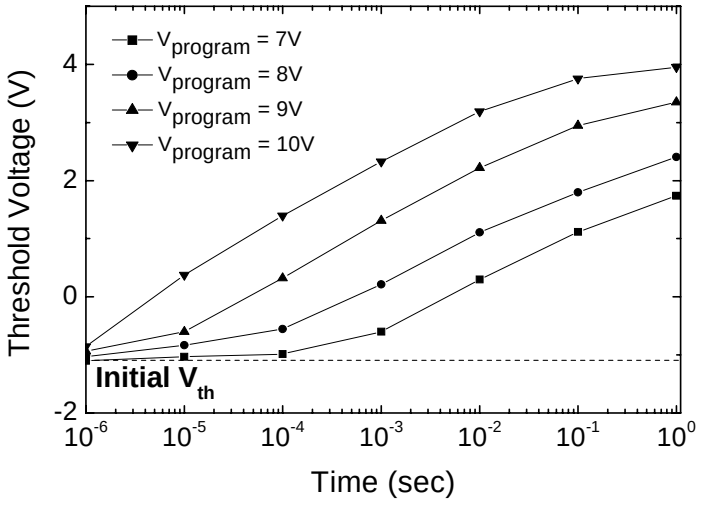


(a)

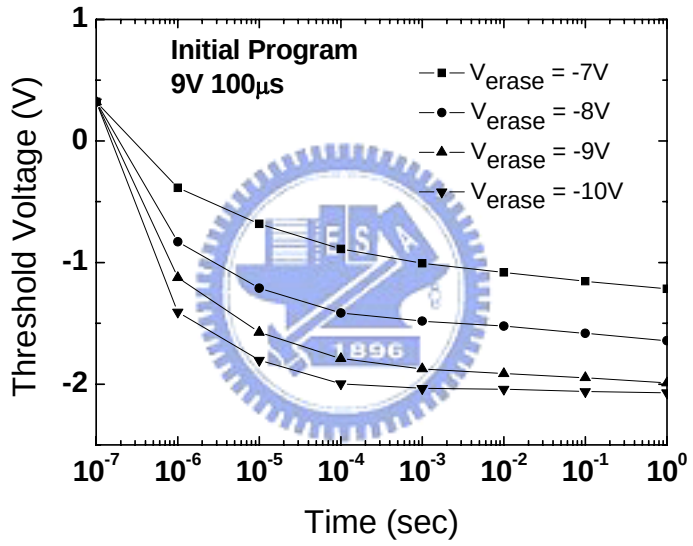


(b)

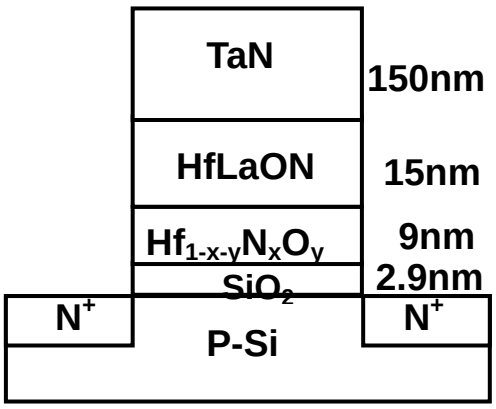
Fig. 3-3. *C-V* hysteresis curves for a TaN-HfLaON-$Hf_{1-x-y}N_xO_y$-SiO_2-Si MONOS device with (a) $Hf_{0.35}N_{0.10}O_{0.55}$ and (b) a $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer.


Threshold Voltage (V)
Time (sec)
V_program = 7V
V_program = 8V
V_program = 9V
V_program = 10V
Initial V_th

(a)

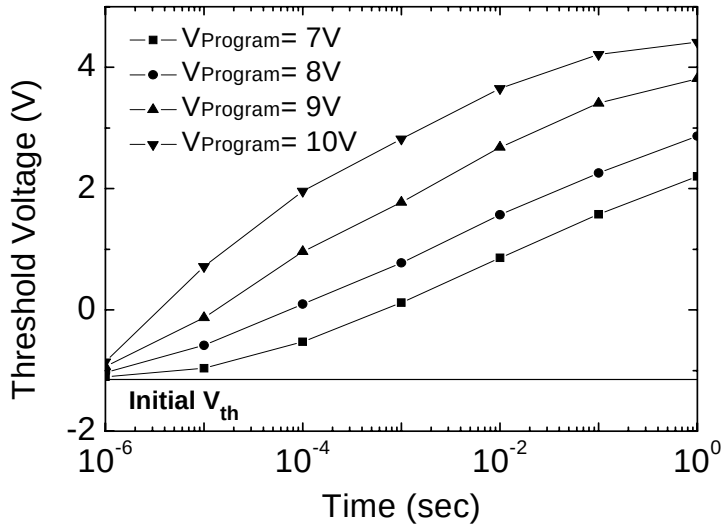

Threshold Voltage (V)
Time (sec)
Initial Program
9V 100μs
V_erase = -7V
V_erase = -8V
V_erase = -9V
V_erase = -10V

(b)

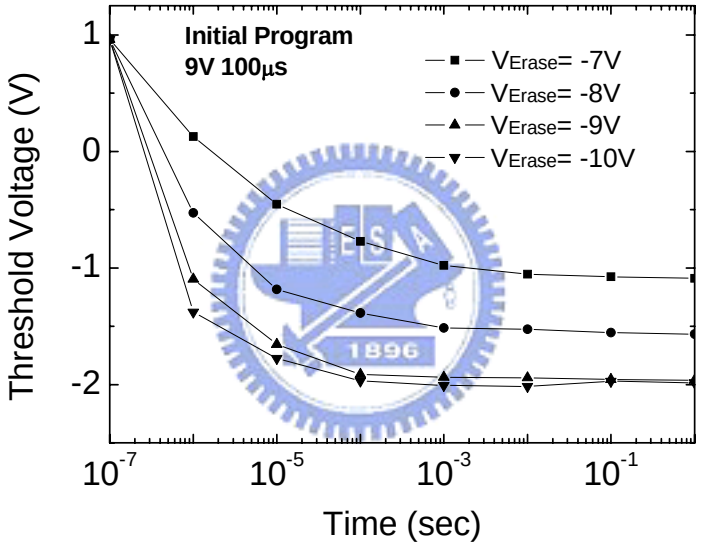

TaN
150nm
HfLaON
15nm
Hf1-x-yNxOy
9nm
SiO2
2.9nm
N+
N+
P-Si

(c)

Fig. 3-4. The measured (a) program and (b) erase characteristics of TaN-HfLaON-$Hf_{0.35}N_{0.10}O_{0.55}$-$SiO_2$-Si MONOS transistors, where the device structure is shown in (c).



(a)



(b)

Fig. 3-5. The measured (a) program and (b) erase characteristics of TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si MONOS transistors.

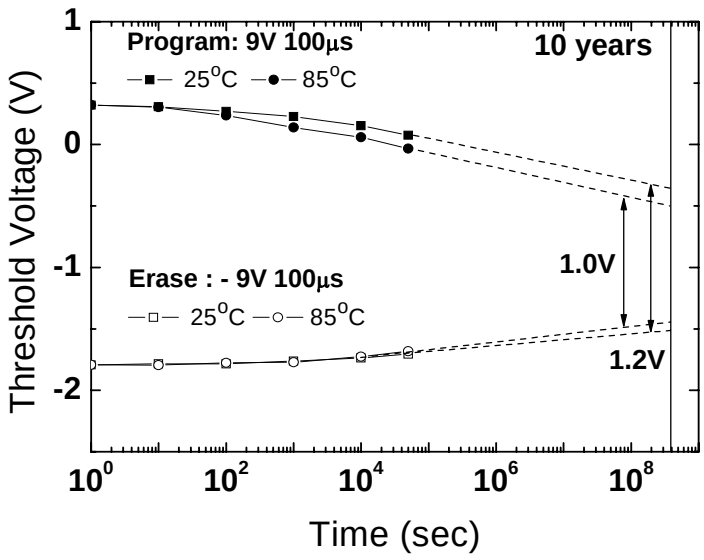
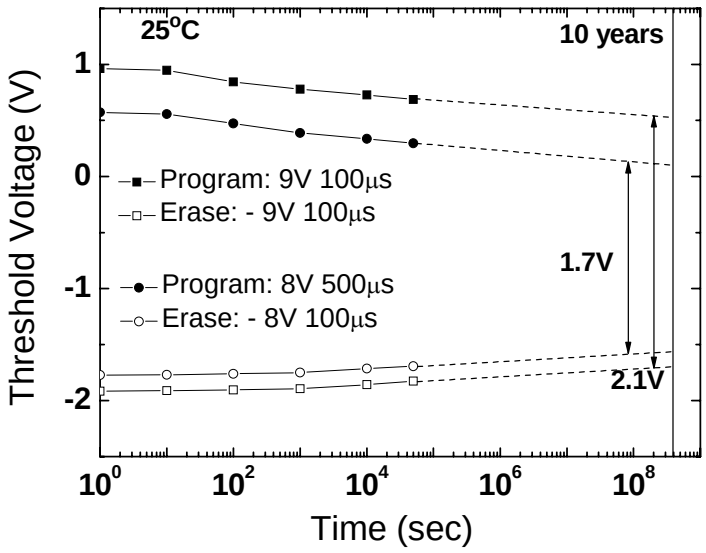
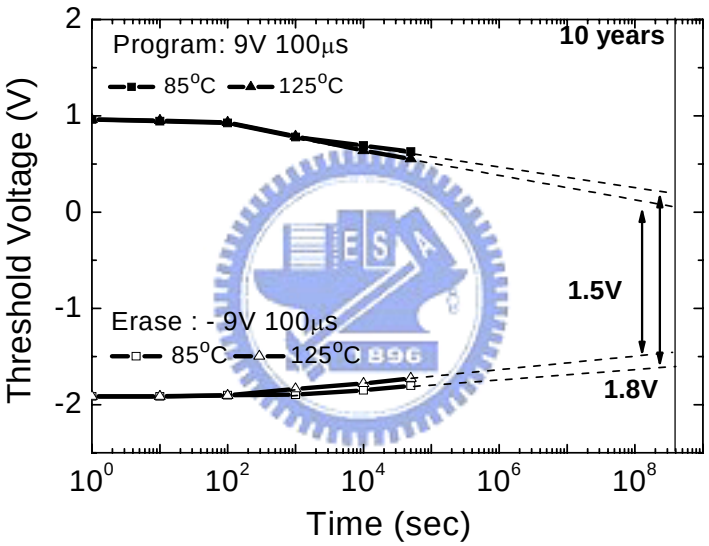


Fig. 3-6. The retention characteristics of TaN-HfLaON-$Hf_{0.35}N_{0.10}O_{0.55}$-$SiO_2$-Si devices at 25 and 85°C.



(a)



(b)

Fig. 3-7. The retention characteristics of TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si devices at (a) 25°C and (b) 85 and 125°C.

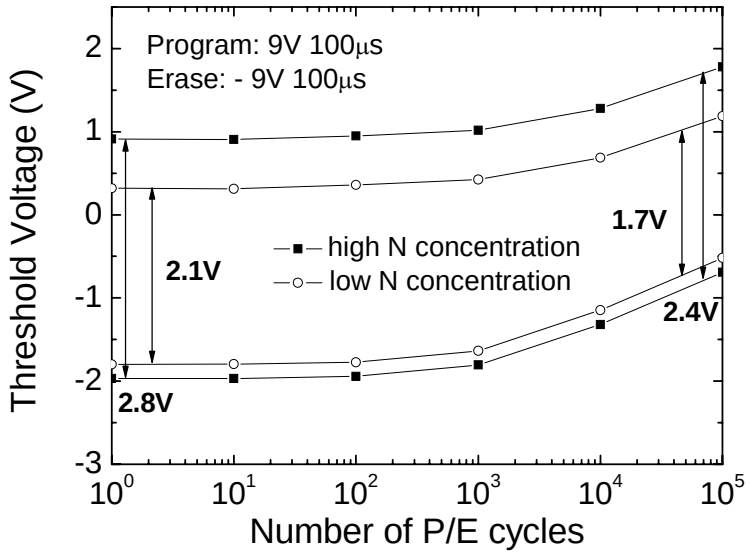


Fig. 3-8. Endurance characteristics of TaN-HfLaON-$Hf_{1-x-y}N_xO_y$-SiO_2-Si MONOS devices with different $Hf_{0.3}N_{0.2}O_{0.5}$ and $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layers.

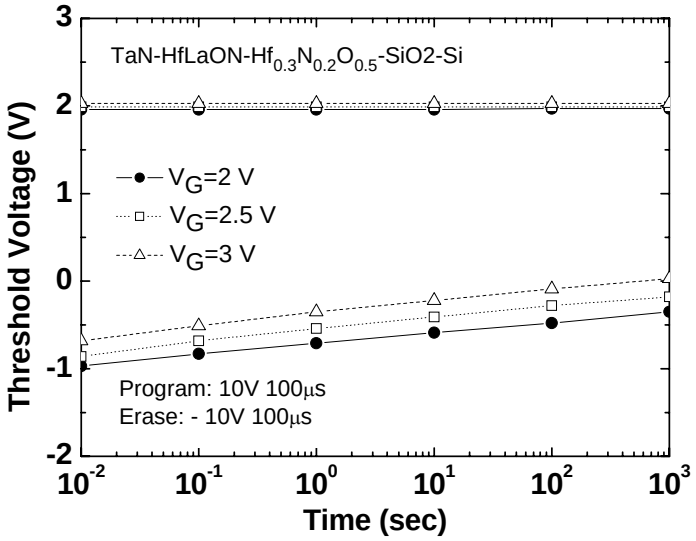
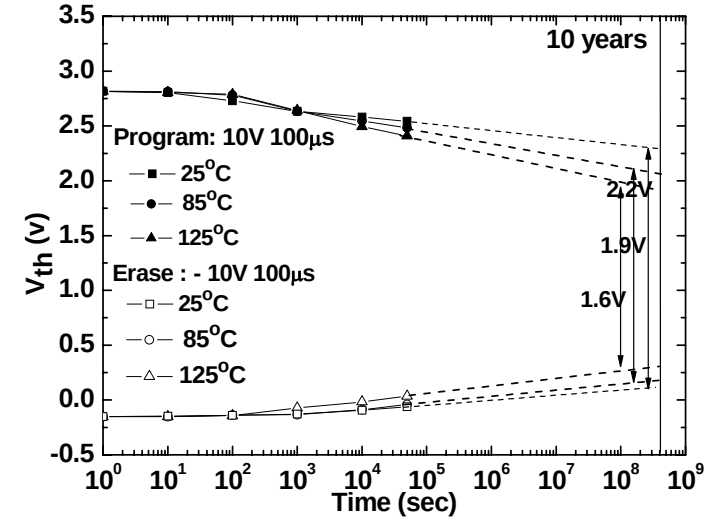
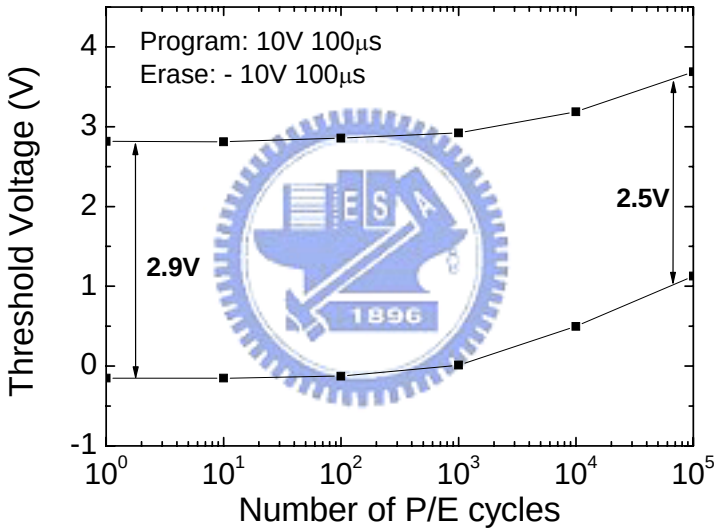


Fig. 3-9. Gate stress disturbance of TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si device.



(a)



(b)

Fig. 3-10. (a) Retention and (b) endurance characteristics of TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si devices at 10 V and 100 μs P/E.

Chapter 4

Improved Data Retention for Charge-Trapping Memory by Using Double Quantum Barriers

4.1 Introduction

Metal-oxide-nitride-oxide-Si (MONOS) type Flash memory devices have been used in the next generation of nonvolatile memory in preference to conventional poly-Si floating-gate memory [4-1]-[4-14]. However, a major challenge for such devices is improving simultaneously both program/erase (P/E) and retention characteristics, because the tunneling current through ultra-thin tunneling oxide layer critically influences both properties [4-12]-[4-14]. The retention becomes even worse at elevated temperature, because the trap energy in Si_3N_4 [4-11] is much lower than that of the conventional deep-energy poly-Si floating gate memory (3.15 eV). To overcome this problem, this letter presents a new charge-trapping memory device. At a low 8 V and fast 100 μs P/E, an extrapolated ten-year retention of 1.9 V was obtained at 125^{o}C, from an initial memory window of 2.6 V. Small retention decays of 64/22 mV/dec at 125^{o}C were measured - better than that of single-barrier HfON and GaAlN MONOS devices [4-12]-[4-14], because the double quantum-barriers in the [TaN-Ir_3Si]-HfAlO-$LaAlO_3$-$Hf_{0.3}O_{0.5}N_{0.2}$-HfAlO-SiO_2-Si charge-trapping device

confines the carriers that are trapped in deep energy $Hf_{0.3}O_{0.5}N_{0.2}$ well. Good 10^5 cycling data are also measured, because the fast 100μs P/E gives less stresses to 3nm effective oxide thickness (EOT) combined tunnel oxides. The data herein are the best ever reported for 125°C at the lowest 8 V P/E voltage and a fast 100 μs speed [4-2]-[4-14].

4.2 Experimental Details

[TaN-Ir_3Si]-HfAlO-$LaAlO_3$-$Hf_{0.3}O_{0.5}N_{0.2}$-HfAlO-SiO_2-Si devices were made by growing 2.5 nm thermal SiO_2 on standard p-Si substrate. Then 2 nm HfAlO was deposited by physical vapor deposition (PVD); 10 nm $Hf_{0.3}O_{0.5}N_{0.2}$ was grown by reactive PVD; 8 nm $LaAlO_3$ and 7 nm HfAlO were deposited by PVD. The $Hf_{0.3}O_{0.5}N_{0.2}$ composition was measured by X-ray photoelectron spectroscopy (XPS). Finally, 15 nm Ir_3Si and 100 nm TaN were fabricated by PVD, before gate definition, self-aligned 25 keV As^+ implantation at 5×10^{15} cm^{-2} dose and 900°C 30 s rapid thermal annealing (RTA) for dopant activation. The gate length of this device is 10 μm. The high work-function Ir_3Si gate was used to reduce the gate erase leakage current that is used for metal-gate/high-κ p-MOS [4-15]. The double HfAlO-$LaAlO_3$ top barrier is also used to lower the leakage current using higher-κ $LaAlO_3$ and larger energy-barrier HfAlO gate dielectrics that have low trapping property [4-16]-[4-17]. A pulse generator was used to program and erase.

4.3 Result and Discussion

Figure 4-1 schematically depicts the double quantum-barriers devices. In conventional MONOS memory, the use of a deep trapping energy layer, such as Al(Ga)N and HfON with a large conduction band discontinuity (ΔE_C) with barrier oxides, can improve the retention of charge-trapping memory [4-12]-[4-14]. However, the trapped carriers can still escape by Schottky emission and tunneling in the MONOS device at high temperatures. To address the issue of retention at high temperature, the double quantum-barrier structure is used to confine more effectively the carriers within the $Hf_{0.3}O_{0.5}N_{0.2}$ quantum well with a deeper trapping energy of 2.5 eV , based on previous work [4-18].

Figures 4-2(a) and 4-2(b) present the program and erase characteristics. During programming, an electron inversion channel was formed by biasing the source-drain electrodes, where the positive gate-channel bias voltage enabled inversion electron injection into the trapping layer. At low a ±8 V P/E voltage and at a fast 100 μs speed, a large ΔV_{th} memory window of 2.6 V was obtained, increasing to 3.2 V at ±9 V 100 μs P/E. The large memory window suggests a high trap density in the $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer. The low P/E voltage is caused by the small voltage drop and electric field (E) in high-κ HfAlO (κ=17) and $LaAlO_3$ (κ~25) barriers, as well as the high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ (κ~22) trapping well. This leads to the fast P/E speed due to large E-field

over the combined tunneling layers of HfAlO-SiO_2. The merit of HfAlO-SiO_2 tunneling layers is the additional conduction band discontinuity (ΔE_C) of HfAlO to SiO_2 which improves charge injection during programming. Such a low P/E voltage is important in realizing the 5 V embedded SoC, where an inverter circuit can be used to generate an opposite polarity of 4~4.5 V between the gate and the channel [4-14].

Figure 4-3 shows the retention and cycled retention characteristics. At ±8 V and a 100 μs P/E, an initial memory window of 2.6 V is obtained, which decreases to 2.3, 2.1and 1.9 V for an extrapolated ten-year memory window at 25, 85 and 125°C, respectively. At these temperatures, the measured decay rates are 36, 60 and 64 mV/dec in the high state and 6, 14 or 22 mV/dec in the low state, respectively, which values are significantly better than those of previous TaN-HfAlO-HfON-SiO_2-Si single barrier MONOS device [4-14]. Such good retention data suggest the charge-trapping mechanism is primary in $Hf_{0.3}N_{0.2}O_{0.5}$ rather than barriers, because the hot electrons injected from the inversion Si channel by Fowler-Nordheim tunneling with a high potential energy to E_c of HfON will be relaxed by fast phonon scattering [4-19] and trapped in a deep amorphous $Hf_{0.3}N_{0.2}O_{0.5}$ well. The tunnel HfAlO layer may trap electrons but also relax to the lower-energy $Hf_{0.3}N_{0.2}O_{0.5}$ well by quantum-mechanical tunneling though a very small thickness of 2 nm. The ten-year retention window is expected to increase with P/E voltage because the P/E

decay rates are small. A large cycled ten-year retention window of 2.0 V is obtained after 10^3 P/E cycles at ±8 V and 100 μs P/E. The good cycling retention is due the fast 100 μs P/E speed with less electrons and holes injection through thin double-tunneling HfAlO-SiO_2 layers.

Table 4-1 compares the memory device characteristics. The presented device has the best retention decay rates at 85 and 125°C, as well as the fast 100 μs P/E, and low 8 V P/E voltage [4-2]-[4-14]. The self-aligned and gate-first processes in this device are compatible with the advanced metal-gate/high-κ CMOS process [4-15], in which 2.5 nm tunnel SiO_2 is useful for logical CMOS integration.

4.4 Conclusions

For a fast 100 μs and low P/E of ±8 V, a large 2.6 V initial memory window and a good 125°C ten-year extrapolated retention of 1.9 V are obtained with only small decay rates of 64/22 mV/dec. This device is promising for low-voltage SoC.

Table 4-1. Comparison of important memory device characteristics among double quantum-barriers charge-trapping device (this work) and other MONOS and TANOS devices.

	P/E condition for retention & cycling	Initial ΔV_{th} (V)	ΔV_{th} (V) for 10-year retention @ 85°C	P/E decay after 10 years @ 85°C (mV/dec)	P/E decay after 10 years @ 125°C (mV/dec)	ΔV_{th} (V) @Cycles
This Work	8V 100μs/ -8V 100μs	2.6	2.1	55 / 19	64 / 22	2.2@10^5
SiO_2/HfON/ AlHfO/TaN [2]	8V 100μs/ -8V 100μs	2.5	1.45	111 / 47	132 / 63	2.1@10^5
SiO2/AlGaN/ $AlLaO_3$ [3]	11V100μs/ -11V 100μs	3.0	1.6	108 / 58	No data	2.3@10^5
TANOS SiO_2/Si_3N_4/ Al_2O_3/TaN [4]	13.5V 100μs/ -13V 10ms	4.4	2.07	140 / 75	No data	4@10^5
SiO_2/Si_3N_4/SiO_2 [5]	11.5V 3ms/ -11.5V 100ms	1.2	1.1 (@25°C)	No data	No data	1.5@10^4
SiO_2/Si_3N_4/SiO_2 [6]	13V 10μs/ -12V 1ms	4.5	2.4	60 / 50	No data	3.5@10^4

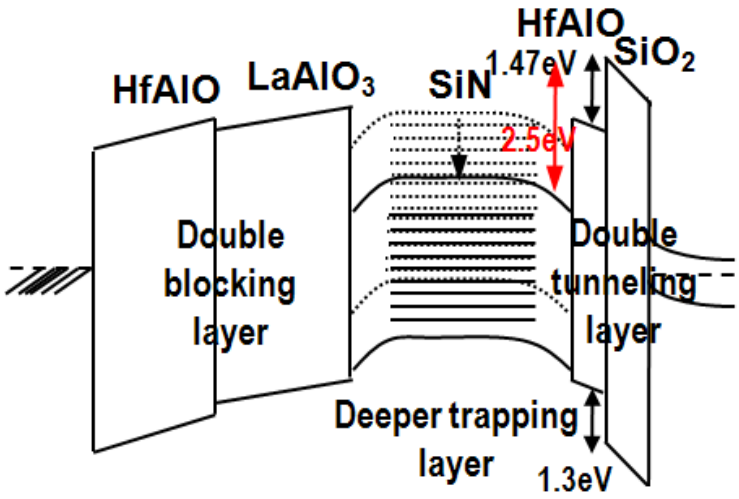
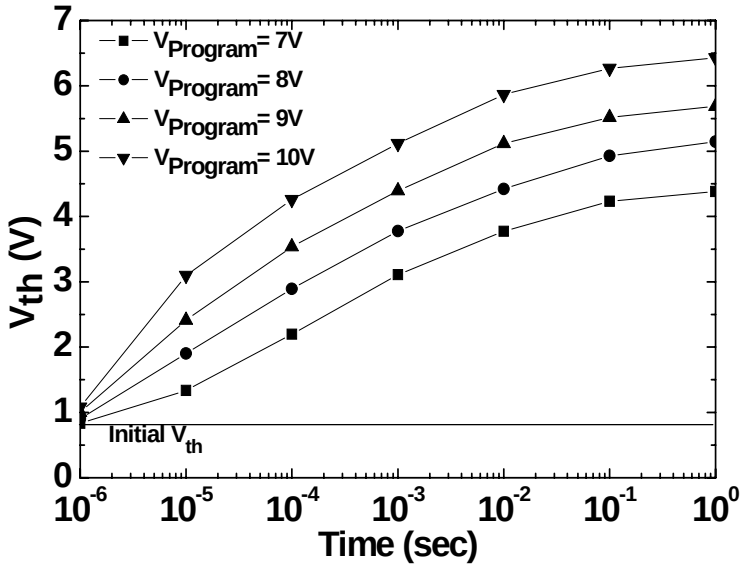
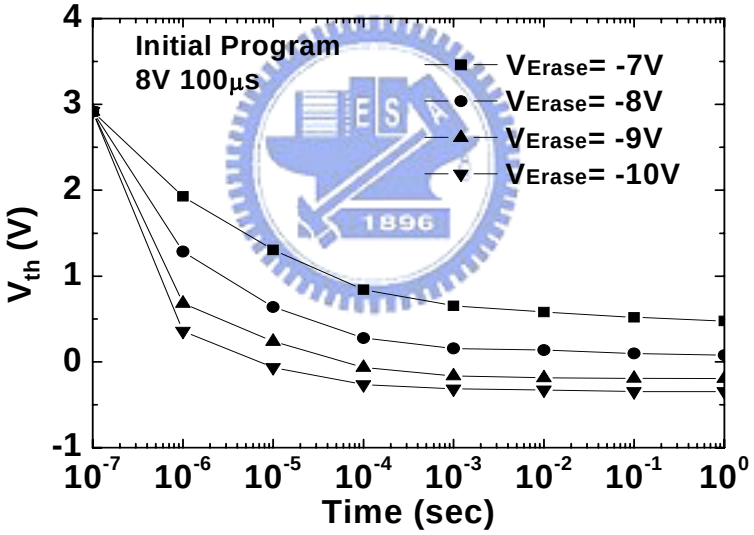


Fig. 4-1. Band diagram of of [Metal-gate]-[High-κ top barrier 1]-[High-κ top barrier 2]-[Trapping Layer]-[High-κ bottom barrier 2]-SiO_2-Si double quantum-barriers charge-trapping NVM.

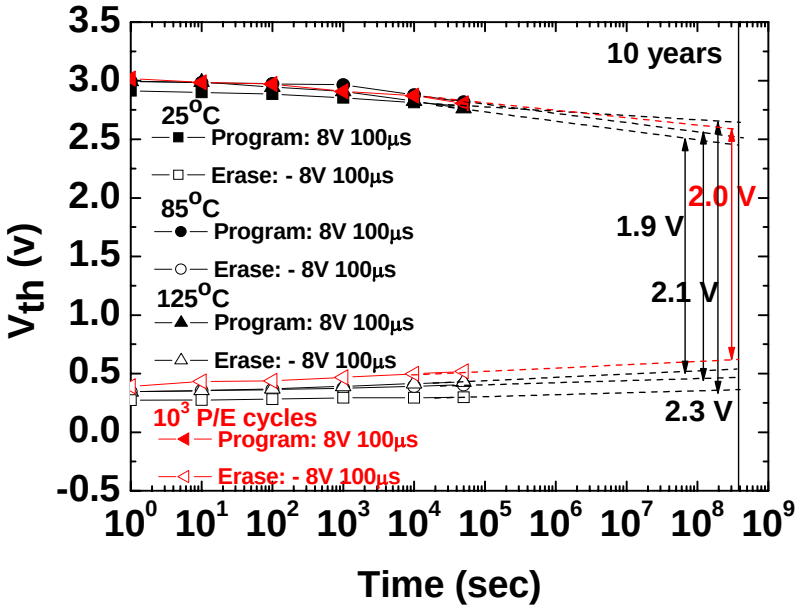


(a)

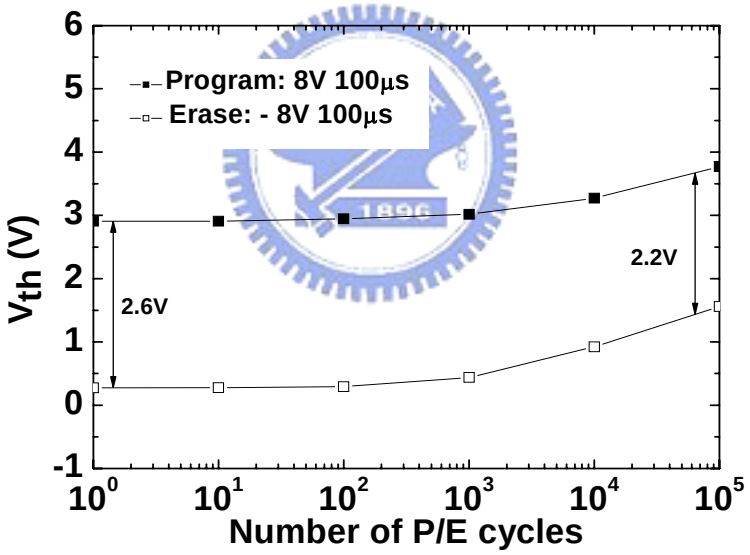


(b)

Fig. 4-2. (a) Device program characteristics for different voltages & times. (b) Device erase characteristics at different voltages & times. The device was initially programmed at 8 V for 100 μs.



(a)



(b)

Fig. 4-3. (a) Retention and (b) endurance characteristics of devices at 25, 85, and 125°C.

Chapter 5

Compare the Performance of Charge-Trapping Memory with Different Single and Double Quantum Barriers.

5.1 Introduction

Metal-Oxide-Nitride-Oxide-Si (MONOS) devices [5-1]-[5-13] are attractive candidates for highly-scaled sub-50nm non-volatile memory (NVM). This is due to their discrete charge-trapping property which can avoid stored charge leakage via a single oxide defect, when compared with conventional conductive poly-Si floating-gate memory devices. However, good data retention at high temperatures is difficult in MONOS memory - this is due to the shallower trap energy in Si_3N_4 [5-14] when compared with poly-Si floating-gate memory, which displays a 3.2 eV trap energy. To address this issue, we previously used deep trap-energy Al(Ga)N and HfON to replace the Si_3N_4 in MONOS devices [5-10]-[5-12], leading to improved retention when compared with Si_3N_4 [5-13]. Unfortunately, the 85^{o}C retention showed a charge decay (at 42~46% of the initial memory window) that was relatively high and unacceptable. The high temperature retention can be improved via bandgap engineered SONOS (BE-SONOS) [5-9], but the erase speed is low (10~100 ms) and the program/erase (P/E) voltages high (18~20 V), contrary to the requirements of the

ITRS scaling roadmap.

In this chapter we report a new double-quantum-barrier charge-trapping NVM device with good high temperature retention, low P/E voltages and high speed. For instance, for a 9V P/E voltage applied between the gate and Si channel at 100 μs the extrapolated 10-year retention window was 2.4 V at 150^{o}C, where the initial value was 3.2 V. The observed retention P/E decay at this temperature was only 82/26 mV/decade (or 25% of the initial memory window) which is better than that of Ga(Al)N [5-10]-[5-11] and HfON [5-12] MONOS devices. This is due to the double quantum barriers, comprising the lower [HfAlO-SiO_2] and the upper [HfAlO-$LaAlO_3$], which confine the carriers trapped in the deep energy $Hf_{0.3}O_{0.5}N_{0.2}$ quantum well. The high electric field across the HfAlO-SiO_2 tunnel oxide leads to the 100μs P/E speed. For the double-barrier devices we have found good 10^5 cycling and cycled retention characteristics, which arise from the rapid 100μs P/E - this produces less stress to the tunnel oxide and thus less interfacial trap generation than in the single-barrier devices. By using ±4.5 V and ∓4.5 V P/E voltages applied between the gate and channel, these devices are promising candidates for embedded SoC applications using a 5 V voltage source [5-12].

5.2 Experimental Details

The [TaN-Ir_3Si]-[HfAlO-$LaAlO_3$]-$Hf_{0.3}N_{0.2}O_{0.5}$-[HfAlO-SiO_2]-Si NVM device

design involved choices of the oxide barrier height and its thickness. First, a 2.5 nm thick thermal SiO_2 layer was grown on a standard p-Si substrate, and a 2 nm layer of HfAlO deposited by PVD to form the double tunneling layers. Then a 10 nm $Hf_{0.3}N_{0.2}O_{0.5}$ layer was deposited by reactive sputtering, under mixed O_2 and N_2 conditions [5-12], [5-15]. (The composition of N and O in the $Hf_{1-x-y}N_xO_y$ was measured by X-ray photoelectron spectroscopy (XPS)). An 8 nm $LaAlO_3$ layer and then 7 nm HfAlO were deposited to form the double blocking layers. Finally, 15nm Ir_3Si and a 150 nm TaN layer was added by PVD. The high work-function Ir_3Si gate was used to make metal-gate/high-κ *p*- MOSFETs [5-16]. After standard processing, the MONOS devices were fabricated using self-aligned As^+ ion implantation and given a 950^{o}C 30sec rapid thermal anneal (RTA) activation to form the source-drain regions. For comparison, we also fabricated TaN-HfLaON-$Hf_{0.3}N_{0.2}O_{0.5}$-SiO_2-Si single barrier MONOS devices. This device had a 2.9 nm thick thermal SiO_2, a 9 nm $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer and a 15 nm HfLaON blocking oxy-nitride layer. Other procedures were the same as for the double-barrier device. The equivalent-oxide-thickness (EOT) of the [HfAlO-SiO_2] tunnel oxide in the double-quantum-barrier device is 3.0 nm, which is close to the 2.9 nm SiO_2 tunnel oxide used in the single barrier MONOS device. The EOT of the [HfAlO-$LaAlO_3$] blocking oxide in the double-barrier device is 3.0 nm - the same as the single-barrier

HfLaON MONOS device. Hence the EOT of both the top blocking oxide and bottom tunnel oxide are almost the same for both the double- and single-barrier charge-trapping memory. The memory devices were characterized by different P/E tests, retention experiments and cycling endurance at 25, 85 and 125^{o}C.

5.3 Result and Discussion

A. Band diagram and P/E characteristics

In Figures 5-1(a) and (b) we compare the schematic band diagrams of the single- and double-quantum-barrier devices, respectively. The conventional SiN trapping layer has a small conduction band discontinuity (ΔE_C) with respect to the barrier oxide of only 1.1 eV [5-14], where the stored charges in shallow trap energy levels can leak out at elevated temperatures. The other ΔE_C and valence band discontinuity (ΔE_C) value are from published literature [5-16]-[5-18]. Thus the SiN MONOS devices are expected to have poor retention properties. The retention in charge-trapping memory can be improved by increasing ΔE_C with respect to the barrier oxide, for instance by using Al(Ga)N and HfON when compared with SiN [5-10]-[5-12]. The use of $Hf_{0.3}N_{0.2}O_{0.5}$ gives a deeper ΔE_C of 2.5 eV [5-16] compared with SiN [5-14], Al(Ga)N [5-10]-[5-11] and our previously-reported HfNO with N~10% [5-12]. However, the trapped carriers can still escape via sequential Schottky emission and tunneling at higher temperatures in the 85~150^{o}C range. For NVM devices good 85~150^{o}C retention is required because of the increasing chip

temperatures arising from the higher power dissipation and larger density of future ICs. As a result the double-quantum-barrier structure is useful to improve the trapped carrier confinement within the $Hf_{0.3}N_{0.2}O_{0.5}$ quantum well, with its deep trapping energy.

Figure 5-2 shows the *C-V* hysteresis characteristics of the double-quantum-barrier charge-trapping device with its $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer. The hysteresis window increases with increasing voltage, indicating good charge storage. A large hysteresis window of 7.3 V was measured under swept voltages of ±10 V in this device, which suggests a high trap density and/or deep trap energy in the $Hf_{0.3}N_{0.2}O_{0.5}$ [5-10]-[5-12].

In Figures 5-3(a) and (b) the P/E characteristics are displayed for various gate voltages, for single- and double-quantum-barrier devices respectively. The devices had the same $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer and almost the same EOT for the barrier oxides. The threshold voltage change (ΔV_{th}) increases with increasing P/E voltage and time, due to the increased number of trapped charges. For the single-quantum-barrier MONOS device, a memory window of 2.8 V was obtained at ±9 V and at 100 μs P/E. For comparison, the double-quantum-barrier charge-trapping device showed a larger ΔV_{th} memory window of 3.2 V for the same testing conditions. It is noticed that the ΔVth for both program and erase are improved compared with single-barrier device.

The combined [HfAlO-SiO2] tunnel oxide, with its EOT close to that for the single-barrier MONOS device, gives a lower energy barrier for electrons to tunnel through, and leads to a larger memory window. The better erase characteristics are due to the higher work-function of Ir_3Si gate electrode than that of TaN in single-barrier device. In both cases, the low P/E voltage arises from the small voltage drop and electric field (E) in the high-κ barriers and the high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ (κ=22) trapping well. This also gives a high E in the tunnel oxide to produce the high P/E speed using tunneling mechanism. Since an inverter circuit can be used to generate the opposite polarities of ±4.5 V and ∓4.5 V applied between the gate and channel [5-12], this low P/E voltage is important for embedded SoC applications using a 5 V voltage source.

B: Retention and endurance:

Good data retention is a challenge for MONOS charge-trapping memory. Figure 5-4(a) shows the retention characteristics of the single-quantum-barrier MONOS device. The initial ΔV_{th} was 2.8 V under 100 μs and ±9 V P/E, and the extrapolated 10-year memory windows were 2.1 V, 1.8 V and 1.5 V at 25, 85 and 125°C, respectively. The decay rates at 85 and 125°C were 92 and 110 mV/dec for the high state or 36 and 55 mV/dec for the low state. For comparison, in Figs. 5-4(b) we show the retention data of a double-quantum-barrier charge-trapping device at 25, 85 and

150°C. The initial ΔV_{th} was 3.2 V under 100 μs and ±9 V P/E, and the extrapolated 10-year memory windows were 3.0 V, 2.7 V and 2.4 V under 25, 85 and 150°C, respectively. The retention P/E decay rates at 85 and 150°C were only 62 and 82 mV/dec for the high state, and 15 and 26 mV/dec for the low state (16% and 25% of initial memory window). This improvement in the high temperature data retentions, compared with a single-barrier MONOS device, indicates the advantage of using double quantum barriers to confine the trapped charges. Since the EOT is close for both single- and double-barrier devices, the using physically thicker high-κ tunnel layer can improve retention in double-barrier devices. The using double blocking layer may also improve the retention due to the slightly higher ΔE_C and misaligned trap energies similar to ONO blocking oxide case. The read disturbance may be a concern in this low voltage operated device to cause charge loss. Similar low voltage P/E at 10 V/-9 V was also reported, where the stored charges were not lost largely as evident from the small V_{th} change even after 1000 seconds gate stresses [19].

Endurance is another important factor for NVM. In Fig. 5-5(a) we compare endurance data for single- and double-barrier charge-trapping devices. A window of 2.4 V and 2.9 V (after 10^5cycles) were obtained for the single- and double-barrier devices, respectively. This arises from the rapid 100μs P/E at 9 V, which causes reduced electric field stress to the tunnel oxide. The degradation after 10^5 cycles is

better for the double-barrier device than that for the single-barrier device, with ΔV_{th} degradations of 0.3 V and 0.4 V or 9% and 14%, respectively. The effect of long-term cycling on the retention appears in Figs. 5-5(b), where the 10^3-cycle 10-year retention windows of 1.7 V and 2.5 V are shown for the single- and double-quantum-barrier devices, which were initially 2.8 V and 3.2 V, respectively. Here again, the double-barrier devices are superior.

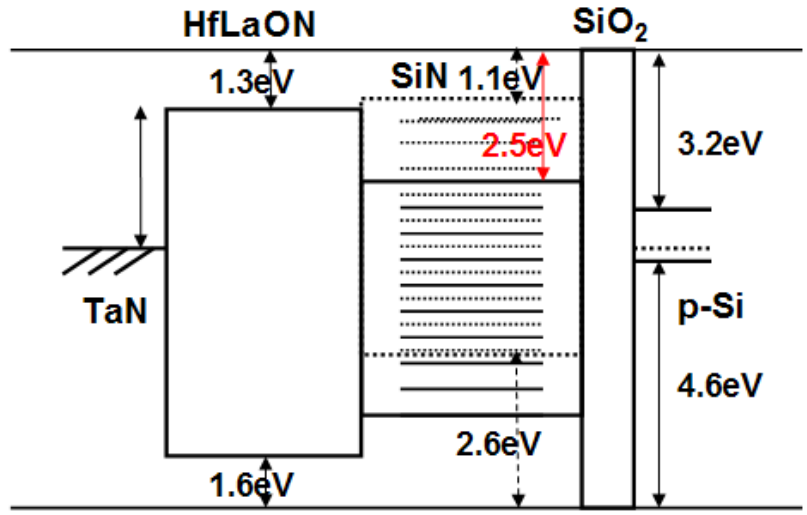
To understand such improvement, we also measured the I_d-V_g characteristics of the devices, before and after cycling. As shown in Figs. 5-6, the single-barrier MONOS device shows an increase of sub-threshold swing (SS) with increasing cycling stress, which suggests generation of SiO_2/Si interface traps. In contrast, the double-barrier device shows the same SS after cycling. Besides the SS change, a shift of I_d-V_g curves was also found for both devices after cycling. The cycling induced linear I_d-V_g shift or ΔV_{th} in Fig. 5(a) is also slightly larger for single-barrier device than double-barrier one, indicating a slightly larger amount of oxide charges generation. The generation of SiO_2/Si interface traps in the single-barrier MONOS device from degraded SS also explains the relative poor retention after cycling, as shown in Fig. 5-5(b), since the trapped carriers may tunnel out via these low energy interface traps within the Si bandgap.

We examined the interface trap generation is by charge pumping methods [20].

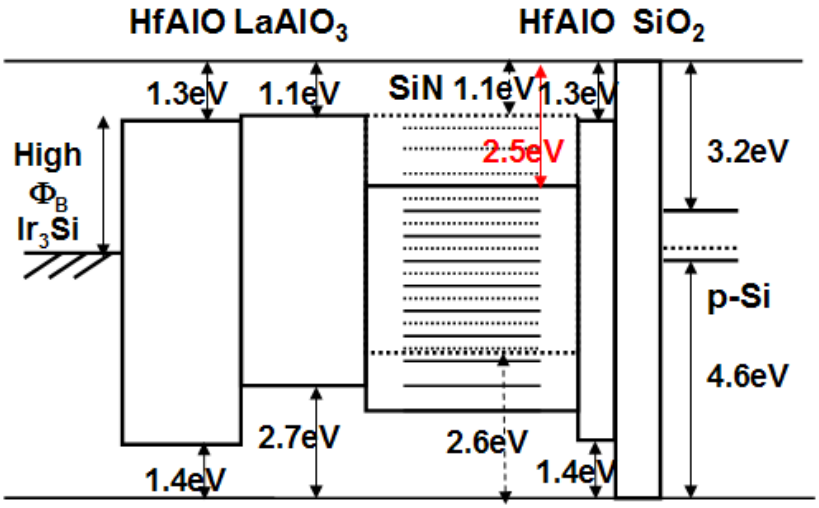
Figure 5-7 compares the interface trap density (D_{it}) of single- and double-quantum barrier devices after P/E cycling. The initial D_{it} is nearly the same for both devices. However, under extensive P/E cycling, more interface traps are created for the single- than for the double-barrier device. This improved D_{it} generation in the double-barrier device leads to better retention after cycling, which is a key factor for achieving good device integrity for NVM.

5.4 Conclusions

At 150°C under a fast 100 μs and low ±9 V P/E voltage, we show that a double-quantum-barrier [TaN-Ir_3Si]-HfAlO-$LaAlO_3$-$Hf_{0.3}O_{0.5}N_{0.2}$-HfAlO-SiO_2-Si charge-trapping device has good NVM integrity in terms of a 3.2 V initial ΔV_{th} and 2.4 V ten-year extrapolated retention. Compared with its single-quantum-barrier MONOS counterpart, the double-quantum-barrier device showed significantly better high temperature retention and cycled retention data, due to better carrier confinement and lower interface trap generation after the P/E cycling.



(b)



(a)

Fig. 5-1. Band diagram of (a) [Metal-gate]-[High-κ barrier]-[Trapping Layer]-SiO_2-Si MONOS non volatile memory device and (b) [Metal-gate]-[High-κ top barrier 1-High-κ top barrier 2]-[Trapping Layer]-[High-κ bottom barrier 2-SiO_2]-Si double-quantum-barrier charge-trapping NVM.

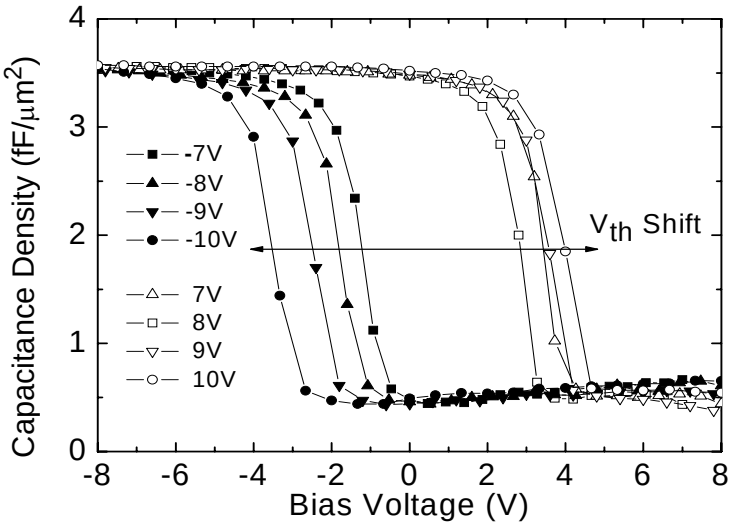
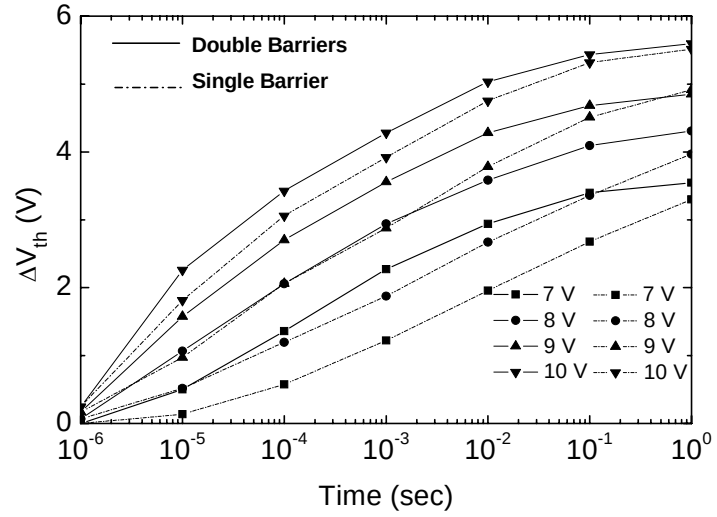
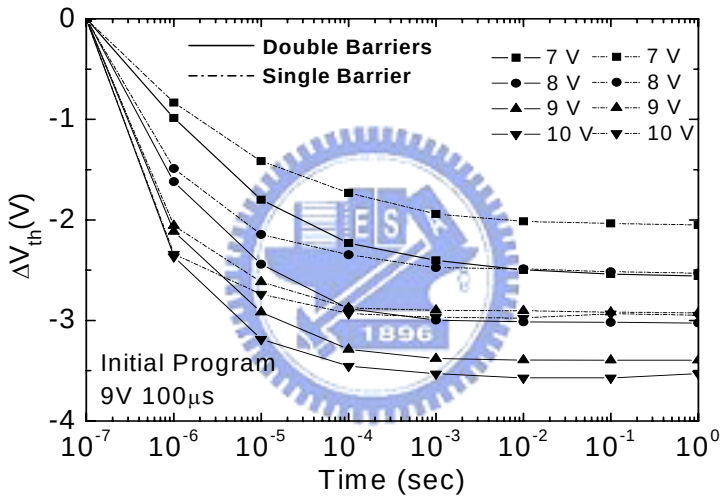


Fig. 5-2. *C-V* hysteresis for double-quantum-barrier device, showing a large V_{th} shift.

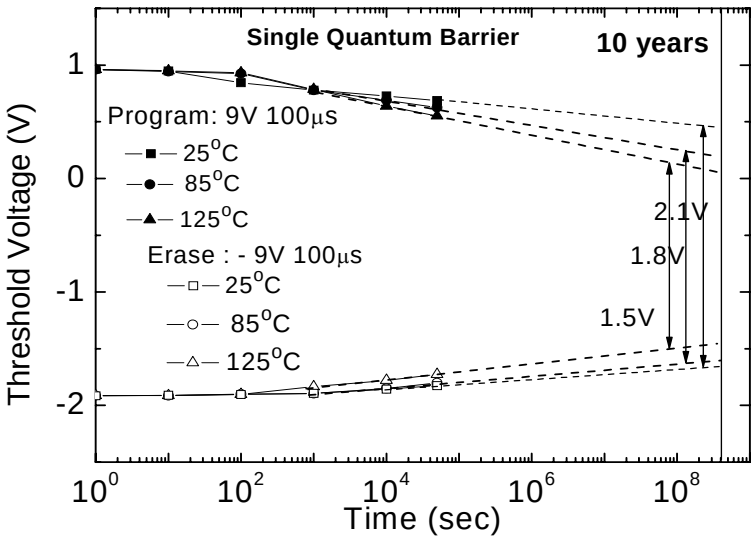


(a)

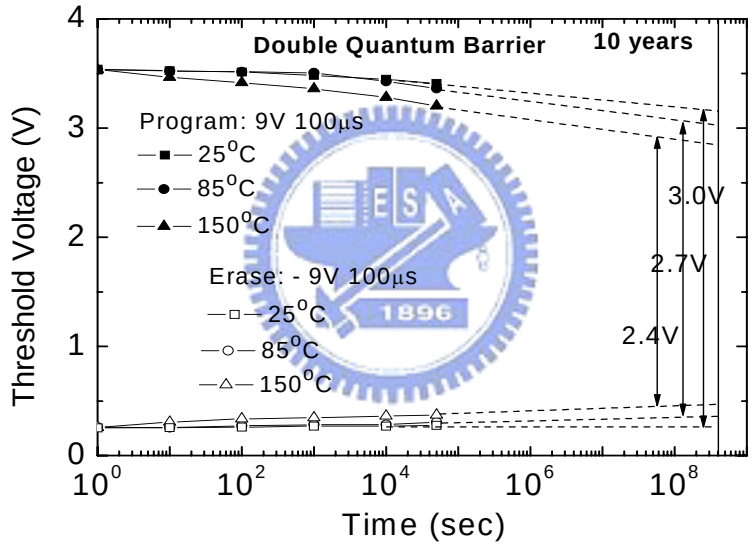


(b)

Fig. 5-3. Comparison of (a) program and (b) erase characteristics between single- and double-quantum-barrier devices under different voltages & times. For the erase both devices were initially programmed at 9 V for 100 μs

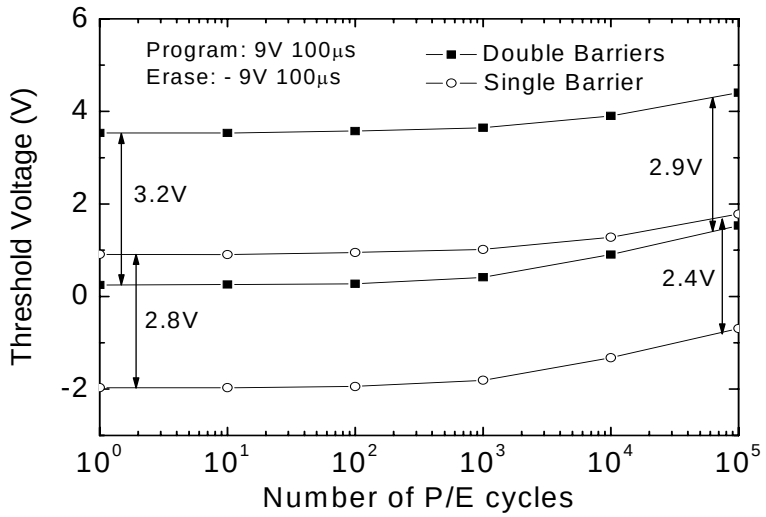


(a)

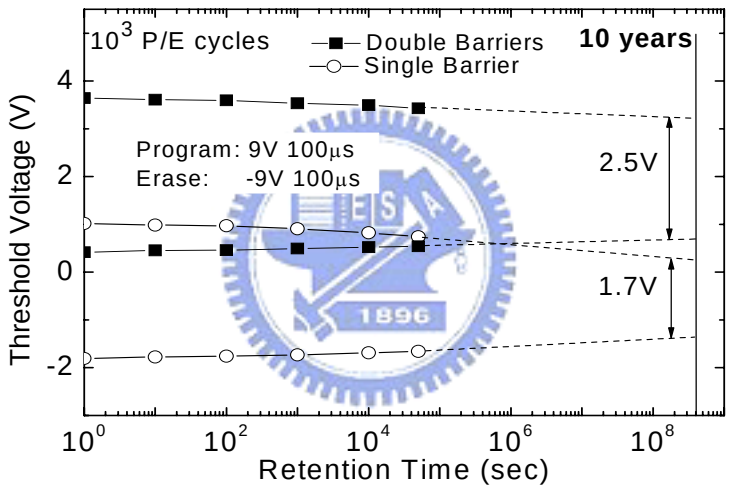


(b)

Fig. 5-4. Device retention characteristics (a) single- and (b) double-quantum-barrier charge-trapping devices at different temperature.

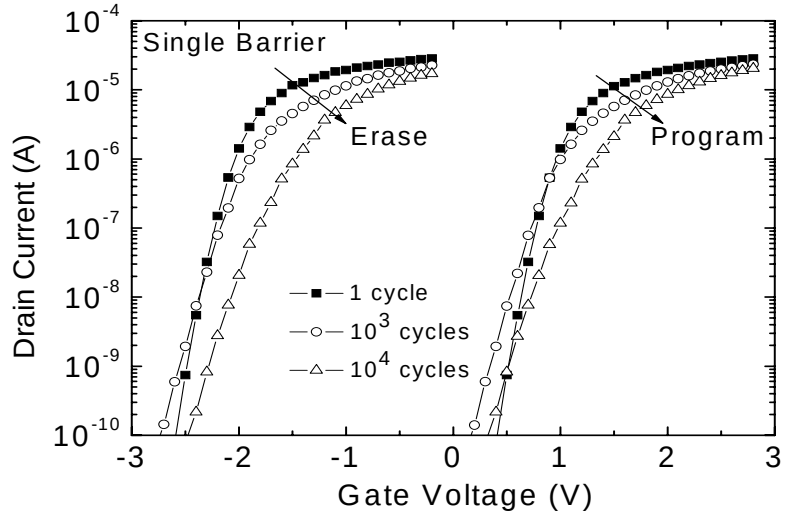


(a)

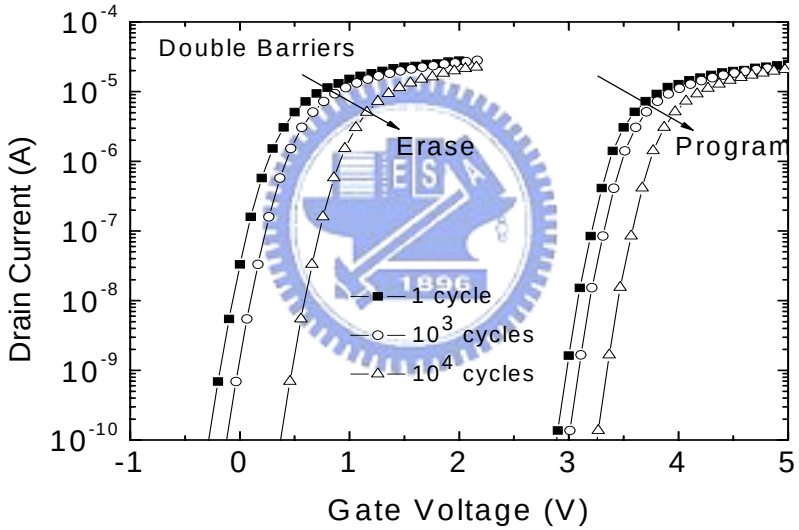


(b)

Fig. 5-5. Comparison of (a) endurance characteristics and (b) retention characteristics after 10^3 P/E cycling of single- and double-quantum-barrier devices.



(a)



(b)

Fig. 5-6. I_d-V_g characteristics of (a) single- and (b) double-quantum-barrier devices after cycling.

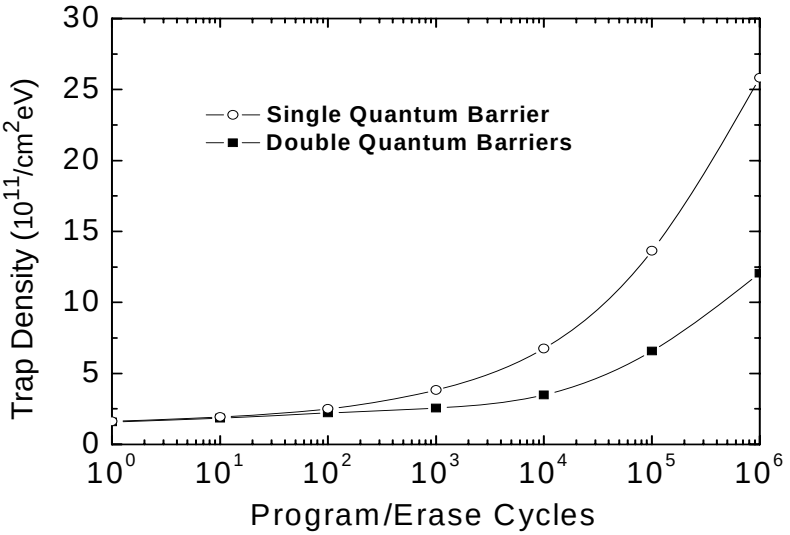


Fig. 5-7. Comparison of the interface trap density (D_{it}) for single- and double-barrier devices after P/E cycling.

Chapter 6

Conclusions

In this dissertation, we describe an improved device which incorporates a high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ with a large N content of 20%, where a deeper trapping energy and/or a smaller band offset are expected from increasing the N%. A large memory window, with a flat-band voltage difference (ΔV_{fb}) of 1.5 V, was measured under ± 5 V and 1 ms P/E conditions. Furthermore, the data retention showed very small P and E decay rates (2 and 6.2 mV/dec) at 25°C and still good at 100°C with small 104 and 116 mV/dec values. The better high temperature retention than that of AlN MIS capacitor was due to the deep trapping energy of the $Hf_{0.3}N_{0.2}O_{0.5}$. This new capacitor with high 6.6 fF/μm^2 density should find wide application for analog, RF, DRAM and low-cost embedded Flash memory.

We first compare the MONOS memory device integrity when using $Hf_{1-x-y}N_xO_y$ trapping layers with different N compositions. We found the extrapolated 10-year memory windows 1.2 V and 1.0 V at 25 and 85°C at initial ΔV_{th} 2.1 V under 100 μs and ±9 V P/E for the $Hf_{0.35}N_{0.10}O_{0.55}$ trapping layer MONOS device. For compared $Hf_{0.3}N_{0.2}O_{0.5}$ MONOS device, the extrapolated 10-year memory window at 25°C increased from 1.7 to 2.1 V with increasing P/E conditions from ±8 V 500 μs/100 μs

to ±9 V 100 μs/100 μs. At 85°C, the 10-year window was still large at 1.8 V under 100 μs ±9 V P/E. Even at 125°C, a 1.5 V 10-year window was obtained. Therefore, not only the room temperature but also the high temperature retention characteristics can be improved by using a higher N% $Hf_{0.3}N_{0.2}O_{0.5}$ trapping layer in a MONOS device than one with a $Hf_{0.35}N_{0.10}O_{0.55}$ composition.

Moreover, we further provide the [TaN-Ir_3Si]-HfAlO-$LaAlO_3$-$Hf_{0.3}N_{0.2}O_{0.5}$-HfAlO-SiO_2-Si charge-trapping memory device. At a low 8 V and fast 100 μs P/E with less read disturbance, an extrapolated ten-year retention of 1.9 V was obtained at 125°C, from an initial memory window of 2.6 V. Small retention decays of 64/22 mV/dec at 125°C were measured - better than that of single-barrier HfNO and GaAlN MONOS devices because the double quantum-barriers in the [TaN-Ir_3Si]-HfAlO-$LaAlO_3$-$Hf_{0.3}N_{0.2}O_{0.5}$-HfAlO-SiO_2-Si charge-trapping device confines the carriers that are trapped in deep energy $Hf_{0.3}N_{0.2}O_{0.5}$ well. Good 10^5 cycling data are also measured, because the fast 100μs P/E gives less stresses to 3nm effective oxide thickness (EOT) combined tunnel oxides. The data herein are the best ever reported for 125°C at the lowest 8 V P/E voltage and a fast 100 μs speed. It is very important for embedded SoC application under a low voltage operation.

References

Chapter1 Introduction

[1.1] "Advanced Memory Technology and Architecture", short course, *IEDM* 2001.

[1.2] Fazio, "0.13um Logic+Flash: Technology and Applications", *Non-Volatile Semiconductor Memory Workshop*, Monterey, CA 2000.

[1.3] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *IEEE Circuits & Devices Magazine,* vol. 16, pp. 22-31, 2000.

[1.4] M. Specht, R. Kommling, L. Dreeskornfeld, W. Weber, F. Hofmann, D. Alvarez, J. Kretz, R.J. Luyken, W. Rosner, H. Reisinger, E. Landgraf, T. Schulz, J. Hartwich, M. Stadele, V. Klandievski, E. Hartmann, and L. Risch, "Sub-40 nm tri-gate charge trapping nonvolatile memory cells for high-density applications," in *Symp. on VLSI Tech. Dig.*, pp. 244-245, 2004.

[1.5] J. Walker, S. Nallamothu, E.-H. Chen, M. Mahajani, S. B. Herner, M. Clark, J. M. Cleeves, S.V. Dunton, V. L. Eckert, J. Gu, S. Hu, J. Knall, M. Konevecki, C. Petti, S. Radigan, U. Raghuram, J. Vienna, and M. A. Vyvoda, "3D FT-SONOS memory cell for ultra-high density file storage applications," in *Symp. on VLSI Tech. Dig.*, pp. 29-30, 2003.

[1.6] T. Sugizaki, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, "Novel multi-bit SONOS

type flash memory using a high-κ charge trapping layer," in *Symp. on VLSI Tech. Dig.*, pp. 27-28, 2003.

[1.7] S.-H. Oh, S.-K. Hong, K.-H. Noh, S.-Y. Kweon, N.-K. Kim, Y.-H. Yang, J.-G. Kim, J.-Y. Seong, I.-W. Jang, S.-H. Park, K.-H. Bang, K.-N. Lee, H.-J. Jeong, J.-H. Son, S.-S. Lee, E.-S. Choi, H.-J. Sun, S.-J. Yeom, K.-D. Ban, J.-W. Park, G.-D. Park, S.-Y. Song, J.-H. Shin, S.-I. Lee, and Y.-J. Park," Noble FeRAM technologies with MTP cell structure and BLT ferroelectric capacitors," in *IEDM Tech. Dig.*, pp. 835-838, 2003.

[1.8] International Technology Roadmap for Semiconductor, 2006 update.

[1.9] White, M.H.; Yang Yang; Ansha Purwar; French, M.L., **"**A low voltage SONOS nonvolatile semiconductor memory technology"**,** *IEEE Transactions on Components, Packaging and Manufacturing Technology Part A*, Vol. 20, pp.190-195, 1997.

[1.10] Zhu, W.; Ma, T.P.; Tamagawa, T.; Di, Y.; Kim, J.; Carruthers, R.; Gibson, M.; Furukawa, T.; **"**HfO_2 and HfAlO for CMOS: thermal stability and current transport ", International Electron Devices Meeting Technical Digest, pp. 20.4.1 -20.4.4, 2001.

[1.11] T. Yamaguchi, H. Satake, N. Fukushima and A. Toriumi, " Band Diagram and Carrier Conduction Mechanism in ZrO_2/Zr-silicate/Si MIS Structure

Fabricated by Pulsed-laser-ablation Deposition", *IEDM Technical Digest*, pp.19-22, 2000.

Chapter2 A Program-Erasable High-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS Capacitor with Good Retention

[2-1] C.-M. Hung, Y.-C. Ho, I.-C. Wu, and K. O, "High-Q capacitors implemented in a CMOS process for low-power wireless applications," *in IEEE MTT-S Int. Microwave Symp. Dig.*, 1998, pp. 505-511.

[2-2] J. A. Babcock, S. G. Balster, A. Pinto, C. Dirnecker, P. Steinmann, R. Jumpertz, and B. El-Kareh, "Analog characteristics of metal-insulator-metal capacitors using PECVD nitride dielectrics," *IEEE Electron Device Lett.*, vol. 22, pp. 230-232, May 2001.

[2-3] C. H. Ng, K. W. Chew, J. X. Li, T. T. Tioa, L. N. Goh, and S. F. Chu," Characterization and comparison of two metal-insulator-metal capacitor schemes in 0.13μm copper dual damascene metallization process for mixed-mode and RF application", in *IEDM Tech. Dig.*, 2002, pp.241-244.

[2-4] T. Ishikawa, D. Kodama, Y. Matsui, M. Hiratani, T. Furusawa, and D. Hisamoto," High-capacitance $Cu/Ta_2O_5/Cu$ MIM structure for SoC applications featuring a single-mask add-on process, in *IEDM Tech. Dig.*, 2002, p. 940-942.

[2-5] H. Hu, S. J. Ding, H. F. Lim, C. Zhu, M.F. Li, S.J. Kim, X. F. Yu, J. H. Chen, Y. F. Yong, B. J. Cho, D.S.H. Chan, S. C. Rustagi, M. B. Yu, C. H. Tung, A. Du, D. My, P. D. Fu, A. Chin, and D. L. Kwong, "High performance HfO_2-Al_2O_3 laminate MIM capacitors by ALD for RF and mixed signal IC applications," in *IEDM Tech. Dig.*, 2003, pp. 379-382.

[2-6] K. C. Chiang, Albert Chin, C. H. Lai, W. J. Chen, C. F. Cheng, B. F. Hung, and C. C. Liao, "Very high-κ and high density TiTaO MIM capacitors for analog and RF applications," in *Symp. on VLSI Tech. Dig.*, 2005, pp. 62-63.

[2-7] K. C. Chiang, C. C. Huang, Albert Chin, W. J. Chen, H. L. Kao, M. Hong, and J. Kwo, "High performance micro-crystallized TaN/$SrTiO_3$/TaN capacitors for analog and RF applications," in *Symp. on VLSI Tech. Dig.*, 2006, pp. 126-127.

[2-8] K. C. Chiang, C. C. Huang, Albert Chin, G. L. Chen, W. J. Chen, Y. H. Wu, Albert Chin, S. P. McAlister, "High performance $SrTiO_3$ metal-insulator-metal capacitors for analog applications," *IEEE Trans. Electron Devices*, vol. 53, pp. 2312-2319, September 2006.

[2-9] C. H. Lai, B. F. Hung, A. Chin, W. J. Yoo, M. F. Li, C. Zhu, S. P. McAlister, and D. L. Kwong, "A novel program-erasable high-κ AlN capacitor," *IEEE Electron Device Lett.*, vol. 26, pp. 148-150, March 2005.

[2-10] C. H. Lai, C. F. Lee, A. Chin, C. H. Wu, C. Zhu, M. F. Li, S. P. McAlister, and

D. L. Kwong, “A tunable and program-erasable capacitor on Si with long tuning memory,” in *IEEE RF-IC Symp. Dig.*, 2004, pp. 259-262.

[2-11] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, “A novel SONOS structure of $SiO_2/SiN/Al_2O_3$ with TaN metal gate for multi-giga bit flash memories,” in *IEDM Tech. Dig.*, 2003, pp. 613-616.

[2-12] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, “A novel SONOS structure of $SiO_2/SiN/Al_2O_3$ with TaN metal gate for multi-Giga bit Flash memeries,” in *IEDM Tech. Dig.*, 2003, pp. 613-616.

[2-13] M. Specht, R. Kommling, L. Dreeskornfeld, W. Weber, F. Hofmann, D. Alvarez, J. Kretz, R.J. Luyken, W. Rosner, H. Reisinger, E. Landgraf, T. Schulz, J. Hartwich, M. Stadele, V. Klandievski, E. Hartmann, and L. Risch, “Sub-40nm tri-gate charge trapping nonvolatile memory cells for high-density applications,” in *Symp. on VLSI Tech. Dig.*, 2004, pp. 244-245.

[2-14] C. H. Lai, Albert Chin, K. C. Chiang, W. J. Yoo, C. F. Cheng, S. P. McAlister, C. C. Chi and P. Wu, “Novel $SiO_2/AlN/HfAlO/IrO_2$ memory with fast erase, large ΔV_{th} and good retention,” in *Symp. on VLSI Tech. Dig.*, 2005, pp. 210-211.

[2-15] Albert Chin, C. C. Laio, K. C. Chiang, D. S. Yu, W. J. Yoo, G. S. Samudra, S. P. McAlister, and C. C. Chi, “Low voltage high speed $SiO_2/AlGaN/AlLaO_3/TaN$

memory with good retention," in *IEDM Tech. Dig.*, 2005, pp. 165-168.

[2-16] C. H. Lai, Albert Chin, H. L. Kao, K. M. Chen, M. Hong, J. Kwo and C. C. Chi, "Very Low voltage SiO_2/HfON/HfAlO/TaN memory with fast speed and good retention," in *Symp. on VLSI Tech. Dig.*, 2006, pp. 54-55.

[2-17] C. H. Lai, C. H. Wu, Albert Chin, S. J. Wang, and S. P. McAlister, "A quantum trap MONOS memory device using AlN" *J. Electrochem. Soc.*, vol. 153, pp. G738-G741, Aug. 2006.

[2-18] C. S. Kang, H-J Cho, R Choi, Y-H Kim, C. Y. Kang, S. J. Rhee, C. Choi, M. S. Akbar, and J. C. Lee "The electrical and material characterization of Hafnium Oxynitride gate dielectrics with TaN-gate electrode" *IEEE Trans. Electron Devices*, vol. 51, pp. 220-227, February 2004.

[2-19] C. H. Wu, B. F. Hung, Albert Chin, S. J. Wang, X. P. Wang, M.-F. Li, C. Zhu, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang "High temperature stable [Ir_3Si-TaN]/HfLaON CMOS with large work-function difference," in *IEDM Tech. Dig.*, 2006, pp. 617-620.

[2-20] H. L. Kao, D. Y. Yang, Albert Chin, and S. P. McAlister, "A 2.4/5 GHz dual-band VCO using a variable inductor and switched resonator," in *IEEE Int. Microwave Symp. Dig.*, 2007, pp. 1533-1536.

[2-21] K. A. Jenkins, and H. Ainspan, "Characteristics of submicron MOS varactors"

in *Si Monolithic IC Dig*., 2006, pp. 123-126.

[2-22] C. S. Chu, Y. Zhou, K. J. Chen, and K. M. Lau, "A novel RF high-Q metal-semiconductor-metal planar inter-digitated varactor based on double-channel AlGaN/GaN HEMT structure" in *Symp. on VLSI Circuit Dig.*, 2005, pp. 402-405.

[2-23] C. L. Yuan, P. Darmawan, M. Y. Chan and P. S. Lee, "Leakage conduction mechanism of amorphous Lu_2O_3 high-κ dielectric films fabricated by pulsed laser ablation" *Euro Phys. Lett.*, vol 77, pp. 67001-1~67001-5, 2007.

[2-24] T. Ino, Y. Kamimuta, M. Suzuki, M. Koyama and A. Nishiyama "Dielectric constant behavior of Hf-O-N System" *Jpn J. Appl. Phys.*, vol. 45, no. 4B, pp. 2908-2913, 2006.

[2-25] Y. Q. Wang, D. Y. Gao, W. S. Hwang, C. Shen, G. Zhang, G. Samudra, Y. C. Yeo, and W. J. Yeo, "Fast erasing and highly reliable MONOS type memory with HfO_2 high-κ trapping layer and Si_3N_4/SiO_2 tunneling stack ," in *IEDM Tech. Dig.,* 2006, pp. 971-974.

Chapter3 Comparison of MONOS Memory Device Integrity when Using $Hf_{1-x-y}N_xO_y$ Trapping Layers with different N Compositions

[3-1] *International Technology Roadmap for Semiconductors (ITRS)*, 2005. [Online]. Available: www.itrs.net

[3-2] S.-I. Minami and Y. Kamigaki, “A novel MONOS nonvolatile memory device ensuring 10-year data retention after 10 erase/write cycles, ”*IEEE Trans. Electron Devices*, vol. 40, pp. 2011–2017, Nov. 1993.

[3-3] M. H. White, Y. Yang, A. Purwar, and M. L. French, “A low voltage SONOS nonvolatile semiconductor memory technology,” *IEEE Trans. Compon., Packag., Manufact. Technol. A*, vol. 20, no. 2, pp. 190–195, Jun. 1997.

[3-4] M. She, H. Takeuchi, and T.-J. King, “Improved SONOS-type flash memory using HfO as trapping layer,” in *Proc. IEEE Nonvolatile Semi. Memory Workshop*, 2003, pp. 53–55.

[3-5] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, “A novel SONOS structure of SiO_2/SiN/Al_2O_3 with TaN metal gate for multi-giga bit flash memeries,” in *IEDM Tech. Dig.*, 2003, pp. 613-616.

[3-6] C. W. Oh, S. D. Suk, Y. K. Lee, S. K. Sung, J.-D. Choe, S.-Y. Lee, D. U. Choi, K. H. Yeo, M. S. Kim, S.-M. Kim, M. Li, S. H. Kim, E.-J. Yoon, D.-W. Kim, D. Park, K. Kim, and B.-I. Ryu, “Damascence gate FinFET SONOS memory implemented on bulk silicon wafer,” in *IEDM Tech. Dig.*, 2004, pp. 893-896.

[3-7] M. Specht, R. Kommling, L. Dreeskornfeld, W. Weber, F. Hofmann, D. Alvarez, J. Kretz, R.J. Luyken, W. Rosner, H. Reisinger, E. Landgraf, T. Schulz, J. Hartwich, M. Stadele, V. Klandievski, E. Hartmann, and L. Risch,

"Sub-40nm tri-gate charge trapping nonvolatile memory cells for high-density applications," in *Symp. on VLSI Tech. Dig.*, 2004, pp. 244-245.

[3-8] X. Wang, J. Liu, W. Bai, and D.-L. Kwong, "A novel MONOS-type nonvolatile memory using high-κ dielectrics for improved data retention and programming speed," *IEEE Trans. Electron Devices*, vol. 51, pp. 597-602, April 2004.

[3-9] Y. N. Tan, W. K. Chim, W. K. Choi, M. S. Joo, T. H. Ng, and B. J. Cho, "High-κ HfAlO charge trapping layer in SONOS-type nonvolatile memory device for high speed operation," in *IEDM Tech. Dig.*, pp. 889-892, 2004.

[3-10] X. Wang and D.-L. Kwong, "A novel high-κ SONOS memory using $TaN/Al_2O_3/Ta_2O_5/HfO_2/Si$ structure for fast speed and long retention operation," *IEEE Trans. Electron Devices*, vol. 53, pp. 78-82, January 2006.

[3-11] C. H. Lai, Albert Chin, K. C. Chiang, W. J. Yoo, C. F. Cheng, S. P. McAlister, C. C. Chi, and P. Wu, "Novel $SiO_2/AlN/HfAlO/IrO_2$ memory with fast erase, large ΔV_{th} and good retention," in *Symp. on VLSI Tech. Dig.*, 2005, pp. 210-211.

[3-12] Albert Chin, C. C. Laio, K. C. Chiang, D. S. Yu, W. J. Yoo, G. S. Samudra, S. P. McAlister, and C. C. Chi, "Low voltage high speed $SiO_2/AlGaN/AlLaO_3/TaN$ memory with good retention," in *IEDM Tech. Dig.*, 2005, pp. 165-168.

[3-13] C. H. Lai, Albert Chin, H. L. Kao, K. M. Chen, M. Hong, J. Kwo, and C. C. Chi, "Very Low voltage SiO_2/HfON/HfAlO/TaN memory with fast speed and good retention," in *Symp. on VLSI Tech. Dig.*, 2006, pp. 54-55.

[3-14] S. H. Gu, T. Wang, W. P. Lu, Y. H. Ku, and C. Y. Lu, "Extraction of nitride trap density from stress induced leakage current in silicon-oxide-nitride-oxide-silicon flash memory," *Appl. Phys. Lett.,* vol. 89, pp. 163514-163516, 2006.

[3-15] C. H. Wu, B. F. Hung, Albert Chin, S. J. Wang, X. P. Wang, M.-F. Li, C. Zhu, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang "High temperature stable [Ir_3Si-TaN]/HfLaON CMOS with large work-function difference," in *IEDM Tech. Dig.*, 2006, pp. 617-620.

[3-16] K. H. Joo, C. R. Moon, S. N. Lee, X. Wang, J. K. Yang, I. S. Yeo, D. Lee, O. Nam, U. I. Chung, J. T. Moon, and B. I. Ryu, "Novel charge trap devices with NCBO trap layers for NVM or image sensor," in *IEDM Tech. Dig.*, 2006, pp. 979-982.

[3-17] T. Ino, Y. Kamimuta, M. Suzuki, M. Koyama and A. Nishiyama "Dielectric constant behavior of Hf-O-N System" *Jpn J. Appl. Phys.*, vol. 45, no. 4B, pp. 2908-2913, 2006.

[3-18] H. J. Yang, Albert Chin, W. J. Chen, C. F. Cheng, W. L. Huang, I. J. Hsieh, and

S. P. McAlister, “A program-erasable high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor with good retention,” *IEEE Electron Device Lett.*, vol. 28, pp. 913-915, Oct. 2007.

[3-19] R. Ohba, Y. Mitani, N. Sugiyama and S. Fujita, “15 nm Planar Bulk SONOS-type Memory with Double Junction Tunnel Layers using Sub-threshold Slope Control,” in *IEDM. Tech. Dig.*, 2007, pp. 75-78.

[3-20] C. H. Lee, C. Kang, J. Sim, J. S. Lee, J. Kim, Y. Shin, K. T. Park, S. Jeon, J. Sel, Y. Jeong, B. Choi, V. Kim, W. Jung, C. I. Hyun, J. Choi and K. Kim, “Charge trapping memory cell of TANOS (Si-Oxide-SiN-Al_2O_3-TaN) structure compatible to conventional NAND flash memory,” in *Non-Volatile Semiconductor Memory Workshop*, 2006, pp. 54-55.

Chapter4 Improved Data Retention for Charge-Trapping Memory by Using Double Quantum Barriers

[4-1] *International Technology Roadmap for Semiconductors (ITRS)*, 2005. [Online]. Available: www.itrs.net

[4-2] S.-I. Minami and Y. Kamigaki, “A novel MONOS nonvolatile memory device ensuring 10-year data retention after 107 erase/write cycles,”*IEEE Trans. Electron Devices*, vol. 40, no. 11, pp. 2011–2017, Nov. 1993.

[4-3] M. H. White, Y. Yang, A. Purwar, and M. L. French, “A low voltage SONOS nonvolatile semiconductor memory technology,” *IEEE Trans. Compon.,*

Packag., Manuf. Technol. A, vol. 20, no. 2, pp. 190–195, Jun. 1997.

[4-4] M. She, H. Takeuchi, and T.-J. King, "Improved SONOS-type Flash memory using HfO as trapping layer," in *Proc. IEEE Nonvolatile Semicond. Memory Workshop*, 2003, pp. 53–55.

[4-5] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, "A novel SONOS structure of SiO2/SiN/Al2O3 with TaN metal gate for multi-gigabit Flash memories," in *IEDM Tech. Dig.*, 2003, pp. 613–616.

[4-6] C. W. Oh, S. D. Suk, Y. K. Lee, S. K. Sung, J.-D. Choe, S.-Y. Lee, D. U. Choi, K. H. Yeo, M. S. Kim, S.-M. Kim, M. Li, S. H. Kim, E.-J. Yoon, D.-W. Kim, D. Park, K. Kim, and B.-I. Ryu, "Damascence gate FinFET SONOS memory implemented on bulk silicon wafer," in *IEDM Tech. Dig.*, 2004, pp. 893–896.

[4-7] M. Specht, R. Kommling, L. Dreeskornfeld, W. Weber, F. Hofmann, D. Alvarez, J. Kretz, R. J. Luyken, W. Rosner, H. Reisinger, E. Landgraf, T. Schulz, J. Hartwich, M. Stadele, V. Klandievski, E. Hartmann, and L. Risch, "Sub-40 nm tri-gate charge trapping nonvolatile memory cells for high-density applications," in *VLSI Symp. Tech. Dig.*, 2004, pp. 244-245.

[4-8] X. Wang, J. Liu, W. Bai, and D.-L. Kwong, "A novel MONOS-type nonvolatile memory using high-κ dielectrics for improved data retention and programming speed," *IEEE Trans. Electron Devices*, vol. 51, no. 4, pp.

597–602, Apr. 2004.

[4-9] Y. N. Tan, W. K. Chim, W. K. Choi, M. S. Joo, T. H. Ng, and B. J. Cho, "High-κ HfAlO charge trapping layer in SONOS-type nonvolatile memory device for high speed operation," in *IEDM Tech. Dig.*, 2004, pp. 889–892.

[4-10] X. Wang and D.-L. Kwong, "A novel high-κ SONOS memory using TaN/Al2O3/Ta2O5/HfO2/Si structure for fast speed and long retention operation," *IEEE Trans. Electron Devices*, vol. 53, no. 1, pp. 78–82, Jan. 2006.

[4-11] S. H. Gu, T. Wang, W. P. Lu, Y. H. Ku, and C. Y. Lu, "Extraction of nitride trap density from stress induced leakage current in silicon–oxide–nitride–oxide–silicon Flash memory," *Appl. Phys. Lett.*, vol. 89, no. 16, pp. 163 514–163 516, 2006.

[4-12] C. H. Lai, A. Chin, K. C. Chiang,W. J. Yoo, C. F. Cheng, S. P. McAlister, C. C. Chi, and P. Wu, "Novel SiO2/AlN/HfAlO/IrO2 memory with fast erase, large ΔVth and good retention," in *VLSI Symp. Tech. Dig.*, 2005, pp. 210–211.

[4-13] A. Chin, C. C. Laio, K. C. Chiang, D. S. Yu, W. J. Yoo, G. S. Samudra, S. P. McAlister, and C. C. Chi, "Low voltage high speed SiO2/AlGaN/AlLaO3/TaN memory with good retention," in *IEDM Tech. Dig.*, 2005, pp. 165–168.

[4-14] C. H. Lai, A. Chin, H. L. Kao, K. M. Chen, M. Hong, J. Kwo, and C. C. Chi, "Very low voltage SiO2/HfON/HfAlO/TaN memory with fast speed and good

retention," in *VLSI Symp. Tech. Dig.*, 2006, pp. 54–55.

[4-15] C. H. Wu, B. F. Hung, A. Chin, S. J. Wang, X. P. Wang, M.-F. Li, C. Zhu, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang, "High temperature stable [Ir3Si-TaN]/HfLaON CMOS with large work-function difference," in *IEDM Tech. Dig.*, 2006, pp. 617–620.

[4-16] C. H. Wu, B. F. Hung, A. Chin, S. J. Wang, F. Y. Yen, Y. T. Hou, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang, "HfAlON n-MOSFETs incorporating low work function gate using ytterbium-silicide," *IEEE Electron Device Lett.*, vol. 27, no. 6, pp. 454–456, Jun. 2006.

[4-17] D. S. Yu, C. C. Liao, C. F. Cheng, A. Chin, M. F. Li, and S. P. McAlister, "The effect of IrO2-IrO2/Hf/LaAlO3 gate dielectric on the bias-temperature instability of 3D GOI CMOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 6, pp. 407–409, Jun. 2005.

[4-18] H. J. Yang, A. Chin, W. J. Chen, C. F. Cheng, W. L. Huang, I. J. Hsieh, and S. P. McAlister, "A program-erasable high-κ Hf0.3N0.2O0.5 MIS capacitor with good retention," *IEEE Electron Device Lett.*, vol. 28, no. 10, pp. 913–915, Oct. 2007.

[4-19] E. Cartier and F. R. McFeely, "Hot-electron dynamics in SiO2 studied by soft-X-ray-induced core-level photoemission," *Phys. Rev. B, Condens. Matter*,

vol. 44, no. 19, pp. 10 689–10 705, Nov. 1991.

Chapter5 Compare the Performance of Charge-Trapping Memory with Different Single and Double Quantum Barriers

[5-1] S.-I. Minami and Y. Kamigaki, “A novel MONOS nonvolatile memory device ensuring 10-year data retention after 10 erase/write cycles, ”*IEEE Trans. Electron Devices*, vol. 40, pp. 2011–2017, Nov. 1993.

[5-2] M. H. White, Y. Yang, A. Purwar, and M. L. French, “A low voltage SONOS nonvolatile semiconductor memory technology,” *IEEE Trans. Compon., Packag., Manufact. Technol. A*, vol. 20, no. 2, pp. 190–195, Jun. 1997.

[5-3] M. She, H. Takeuchi, and T.-J. King, “Improved SONOS-type flash memory using HfO as trapping layer,” in *Proc. IEEE Nonvolatile Semi. Memory Workshop*, 2003, pp. 53–55.

[5-4] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, “A novel SONOS structure of SiO_2/SiN/Al_2O_3 with TaN metal gate for multi-giga bit flash memories,” in *IEDM Tech. Dig.*, 2003, pp. 613-616.

[5-5] C. W. Oh, S. D. Suk, Y. K. Lee, S. K. Sung, J.-D. Choe, S.-Y. Lee, D. U. Choi, K. H. Yeo, M. S. Kim, S.-M. Kim, M. Li, S. H. Kim, E.-J. Yoon, D.-W. Kim, D. Park, K. Kim, and B.-I. Ryu, “Damascence gate FinFET SONOS memory implemented on bulk silicon wafer,” in *IEDM Tech. Dig.*, 2004, pp. 893-896.

[5-6] M. Specht, R. Kommling, L. Dreeskornfeld, W. Weber, F. Hofmann, D. Alvarez, J. Kretz, R.J. Luyken, W. Rosner, H. Reisinger, E. Landgraf, T. Schulz, J. Hartwich, M. Stadele, V. Klandievski, E. Hartmann, and L. Risch, "Sub-40nm tri-gate charge trapping nonvolatile memory cells for high-density applications," in *Symp. on VLSI Tech. Dig.*, 2004, pp. 244-245.

[5-7] X. Wang, J. Liu, W. Bai, and D.-L. Kwong, "A novel MONOS-type nonvolatile memory using high-κ dielectrics for improved data retention and programming speed," *IEEE Trans. Electron Devices*, vol. 51, pp. 597-602, April 2004.

[5-8] Y. N. Tan, W. K. Chim, W. K. Choi, M. S. Joo, T. H. Ng, and B. J. Cho, "High-κ HfAlO charge trapping layer in SONOS-type nonvolatile memory device for high speed operation," in *IEDM Tech. Dig.*, pp. 889-892, 2004.

[5-9] H. T. Lue, S. Y. Wang. E. K. Lai, Y. H. Shih, S. C. Lai, L. W. Yang, K. C. Chen, J. Ku, K. Y. Hsieh, R. Liu, and C. Y. Lu, "A bandgap engineered SONOS with excellent performance and reliability," in *IEDM Tech. Dig.*, 2005, pp. 555-558.

[5-10] C. H. Lai, Albert Chin, K. C. Chiang, W. J. Yoo, C. F. Cheng, S. P. McAlister, C. C. Chi, and P. Wu, "Novel SiO_2/AlN/HfAlO/IrO_2 memory with fast erase, large ΔV_{th} and good retention," in *Symp. on VLSI Tech. Dig.*, 2005, pp.

210-211.

[5-11] Albert Chin, C. C. Laio, K. C. Chiang, D. S. Yu, W. J. Yoo, G. S. Samudra, S. P. McAlister, and C. C. Chi, "Low voltage high speed SiO_2/AlGaN/$AlLaO_3$/TaN memory with good retention," in *IEDM Tech. Dig.*, 2005, pp. 165-168.

[5-12] C. H. Lai, Albert Chin, H. L. Kao, K. M. Chen, M. Hong, J. Kwo, and C. C. Chi, "Very Low voltage SiO_2/HfON/HfAlO/TaN memory with fast speed and good retention," in *Symp. on VLSI Tech. Dig.*, 2006, pp. 54-55.

[5-13] K. H. Joo, C. R. Moon, S. N. Lee, X. Wang, J. K. Yang, I. S. Yeo, D. Lee, O. Nam, U. I. Chung, J. T. Moon, and B. I. Ryu, "Novel charge trap devices with NCBO trap layers for NVM or image sensor," in *IEDM Tech. Dig.*, 2006, pp. 979-982.

[5-14] S. H. Gu, T. Wang, W. P. Lu, Y. H. Ku, and C. Y. Lu, "Extraction of nitride trap density from stress induced leakage current in silicon-oxide-nitride-oxide-silicon flash memory," *Appl. Phys. Lett.,* vol. 89, pp. 163514, 2006.

[5-15] H. J. Yang, Albert Chin, W. J. Chen, C. F. Chen, W. L. Huang, I. J. Hsieh, and S. P. McAlister "A program-erasable high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor with good retention" *IEEE Electron Devices Lett.*, vol. 28, pp. 913-915, Oct. 2007.

[5-16] C. H. Wu, B. F. Hung, Albert Chin, S. J. Wang, X. P. Wang, M.-F. Li, C. Zhu, Y.

Jin, H. J. Tao, S. C. Chen, and M. S. Liang "High temperature stable [Ir_3Si-TaN]/HfLaON CMOS with large work-function difference," in *IEDM Tech. Dig.*, 2006, pp. 617-620.

[5-17] J Robertson, "Band offsets of wide-band-gap oxides and implications for future electron devices," *J Vac Sci Technol B*, vol. 18, pp. 1785-1791, May 2000.

[5-18] H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo and M. S. Joo, "Energy gap and band alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si," *Appl. Phys. Lett.,* vol. 81, pp. 376-378, July 2002.

[5-19] R. Ohba, Y. Mitani, N. Sugiyama and S. Fujita, "15 nm Planar bulk SONOS-type memory with double junction tunnel layers using sub-threshold slope control," in *IEDM. Tech. Dig.*, 2007, pp. 75-78.

[5-20] Y. Y. Liao, S. F. Horng, Y. W. Chang, T. C. Lu, K. C. Chen, T. Wang, C. Y. Lu, "Profiling of nitride-trap-energy distribution in SONOS flash memory by using a variable-amplitude low-frequency charge-pumping technique," *IEEE Electron Devices Lett.*, vol. 28, pp. 828-830, Sept. 2007.

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論文題目：

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Research of MONOS Non-Volatile Memory with Low Voltage and Good Retention

Publication Lists:

(A) International Journal:

[1] **H. J. Yang** C. F. Cheng, W. B. Cheng, S. H. Lin, F. S. Yeh, Sean P. McAlister and Albert. Chin, "Comparison of MONOS Memory Device Integrity When Using $Hf_{1-x-y}N_xO_y$ Trapping Layers With Different N Compositions," IEEE Trans. Electron Devices, 55, no. 6, pp. 1417-1423, June 2008.

[2] **H. J. Yang**, Albert. Chin, S. H. Lin, F. S. Yeh, and S. P. McAlister, **"**Improved High Temperature Retention for Charge-Trapping Memory by Using Double Quantum Barriers," IEEE Electron Device Lett. 29, no. 4, pp. 386-388, 2008.

[3] **H. J. Yang**, Albert. Chin, W. J. Chen, C. F. Cheng, W. L. Huang, I. J. Hsieh, and S. P. McAlister, **"**A Program-Erasable High-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS Capacitor With Good Retention," IEEE Electron Device Lett. 28, no. 10, pp. 913-915, 2007.

[4] S. H. Lin, **H. J. Yang**, W. B. Cheng, F. S. Yeh, Sean P. McAlister and Albert. Chin, "Improving the Retention and Endurance Characteristics of Charge-Trapping Memory by Using Double Quantum Barriers," IEEE Trans. Electron Devices, accepted to be published on July 2008.

(B) Conferences & Proceeding

[1] Albert Chin, **H. J. Yang**, S. H. Lin, F. S. Yeh, "Improved High Temperature Retention and Endurance in HfON Trapping Memory with Double Quantum Barriers," *8th Int'l Conf. on Solid-State and Integrated-Circuit Technology (ICSICT)*, October, 2008. **(Invited)**

[2] S. H. Lin, **H. J. Yang**, H. L. Kao, F. S. Yeh, and Albert Chin, "Improved 150°C Retention in $Hf_{0.3}N_{0.2}O_{0.5}$ Memory Device with Low Voltage and Fast Writing," *IEEE 66th Device Research Conference (DRC)*, 2008.

[3] Albert Chin, C. H. Lai, **H. J. Yang**, W. J. Chen, Y. H. Wu, and H. L. Hwang, "Extremely Low Voltage and High Speed Deep Trapping MONOS Memory with Good Retention," *ICSICT*, 2006 (***Invited***)