應用於行動視訊的 MPEG-2 及 H.264 解碼器之研究

學生：劉子明　　指導教授：李鎮宜 教授

國立交通大學

電子工程學系電子研究所

摘要

視訊壓縮標準的演進將以不利的角度，衝擊著視訊訊號在行動通訊中的硬體實現。這些衝擊，首當其衝的包含有硬體的成本、功率的消耗，以及視訊傳輸的雜訊干擾。因此，本論文提出一個低功率的雙模視訊解碼器來改善其面積、功率的硬體性能。本研究實現了，在一顆單晶片上面同時支援 MPEG-2 SP@ML 和 H.264/AVC BL@L4 兩種視訊解碼標準。並且具有架構可調整之特色，使其能夠降低整合的成本以及實體的運算功率消耗。除此之外，為了抵抗在行動之視訊傳輸過程中的雜訊干擾，此一視訊解碼器也將對於傳輸的通道做一個通盤的考量，以改善傳輸當中所造成的畫質損失。

細部來說，我們整合了 MPEG-2 和 H.264/AVC 當中不同的演算模組。而在這兩個不同的標準當中，我們針對反向餘弦轉換(IDCT)、去區塊雜訊率波器(Deblocking Filter)以及熵解碼器(Entropy Decoder)來作硬體的共享和合併，以試圖降低晶片的成本負擔。另外還有許多的低功率技術在本論文中詳加探討。第一，我們使用區域管線化調整(DPS)技巧以依照處裡的週期來最佳化管線化的結構。第二，我們利用三層級的記憶體階層和行像素預測(LPL)模組來實現頻寬可調式架構。如此可以改善外部的記憶體頻

寬，而且也能夠減低內部記憶體的使用需求量。這樣的做法能夠比傳統設計減少 51% 的記憶體功率消耗。第三，一個新穎式的解碼程序可用來改善一個宏模區塊(Macroblock)的存取性能。低功率的移動補償和去區塊雜訊率波器則被提出，在不損失系統性能的情況下，能夠大大降低所需的操作頻率，以達到低功率的需求。而考慮在行動通訊系統中的視訊傳輸方面，本論文亦提出一個錯誤偵測方式，以提早並正確的偵測出錯誤的宏模區塊並且加以修補隱藏，以改善視訊的觀賞品質。實驗結果也說明在錯誤率為 2.7×10^{-3} 的情況下，我們尚能夠改善 1dB 的畫面 PSNR 值。除此之外，本論文提出一個幀重新壓縮的機制。它不但能夠降低外部的幀記憶體容量，同時亦能夠支援當傳輸的視訊有錯時具有抗錯誤的特色。

最後，本論文利用 0.18μm 1P6M 製程技術實作了一顆測試晶片，面積為 15.21mm^2 並且在測試機台上進行量測。而測試的結果顯示，在符合行動視訊的環境之下，以 QCIF 為畫面大小、每秒進行 15 幀畫面的即時 H.264/AVC 以及 MPEG-2 的視訊解碼過程中，晶片的所需速度為 1.15MHz、所外接的電壓為 1-V 情況下，其消耗的功率分別僅有 125μW 以及 108μW。而此一低成本、低功耗以及抗雜訊的視訊解碼設計也正隱含，本研究結果非常適合於未來視訊訊號傳輸於行動通訊的系統當中。

Study of MPEG-2 and H.264 Video Decoder for Mobile Applications

Student : Tsu-Ming Liu Advisor : Dr. Chen-Yi Lee

Department of Electronics Engineering

Institute of Electronics

National Chiao Tung University

ABSTRACT

Advances of video coding made an adverse impact on VLSI implementation over mobile communication systems. Those impacts mainly include area, power, and channel deterioration in the video decoding side. Therefore, this dissertation presents a low-power dual-standard video decoder to improve the area/power efficiency. It supports MPEG-2 SP@ML and H.264/AVC BL@L4 video decoding in a single chip and features a scalable architecture to reduce the required silicon area as well as power dissipation. Moreover, to combat transmission errors of video streams, this design is robust to the channel behavior for improving the subjective and objective visual quality.

Specifically, we integrate diverse algorithms of MPEG-2 and H.264/AVC to reduce silicon area. Among different standards, IDCT, deblocking filter and entropy decoder are tightly combined at algorithmic and architectural levels. Several low-power techniques are proposed. First, a domain-pipelined scalability (DPS) technique is used to optimize the pipelined structure according to the number of processing cycles. Second, bandwidth

scalability is implemented via three-level memory hierarchy and line-pixel-lookahead (LPL) schemes to improve the external bandwidth and reduce the internal memory size, leading to 51% of memory power reduction compared to a conventional design. Third, a novel decoding ordering is utilized to improve the access efficiency in one macroblock. Low-power motion compensation and deblocking filter are designed to reduce the operating frequency without degrading system performance. Considering the video transmission over the mobile environments, the proposal exploits an error detection to early detect and thereby conceal corrupted macroblocks. It greatly improves the visual quality by 1dB of PSNR under the 2.7×10^{-3} of bit error rate. Moreover, a frame re-compression method is presented to not only lower the required memory capacity but also support error-robustness features when the corrupted portion of one frame is detected.

Finally, a test chip is fabricated in a 0.18μm 1P6M CMOS process with an area of 15.21mm^2 and measured via a VLSI tester. For mobile applications, H.264/AVC and MPEG-2 video decoding of quarter-common intermediate format (QCIF) sequences at 15 frames per second are achieved at 1.15MHz clock frequency with power dissipation of 125μW and 108μW respectively at 1-V supply voltage. This area-efficient, low-power and error-robust design also reveals its strong suitability for mobile communication systems.