

Contents

CHAPTER 1 INTRODUCTION 17

1.1	VIDEO STANDARD INTRODUCTION	17
1.1.1	<i>MPEG-2</i>	19
1.1.2	<i>H.264/AVC</i>	20
1.1.3	<i>Motivation of Implementation Methods</i>	25
1.2	ORGANIZATION AND CONTRIBUTION	26
1.2.1	<i>Low-Cost Design Issue</i>	26
1.2.2	<i>Low-Power Design Issue</i>	27
1.2.3	<i>Error-Robust Design Issue</i>	29

CHAPTER 2 JOINT MPEG-2 AND H.264/AVC DECODER..... 31

2.1	BACKGROUND.....	31
2.2	OVERVIEW	32
2.3	SYNTAX PARSER.....	34
2.4	CONTEXT-ADAPTIVE VARIABLE LENGTH DECODER.....	35
2.4.1	<i>Table-Merging Method</i>	36
2.5	INTRA PREDICTION	38
2.5.1	<i>Combined Intra/Inter Prediction</i>	39
2.6	INVERSE DISCRETE COSINE TRANSFORM	40
2.6.1	<i>Recursive Algorithm</i>	42
2.6.2	<i>Multiple Constant Multiplication</i>	43
2.7	MOTION COMPENSATION	43

2.7.1	<i>Hybrid MPEG-2/H.264 Interpolator Design.....</i>	44
2.8	DEBLOCKING FILTER	46
2.8.1	<i>Background.....</i>	46
2.8.2	<i>Algorithmic Preview</i>	48
2.8.3	<i>In/Post-loop Algorithm</i>	50
2.8.3.1	<i>Triple-mode decision</i>	50
2.8.3.2	<i>Triple pixel-in-pixel-out edge filter.....</i>	52
2.8.4	<i>Performance Evaluation.....</i>	54
2.9	SUMMARY	57
CHAPTER 3 LOW-POWER DESIGN APPROACH.....		59
3.1	OVERVIEW	59
3.2	REDUCING PIPELINE REGISTERS	60
3.2.1	<i>Pipeline Methodology.....</i>	60
3.2.2	<i>Domain-Pipelined Scalability</i>	62
3.3	IMPROVING THE MEMORY HIERARCHY	66
3.3.1	<i>Background.....</i>	66
3.3.2	<i>Content Memory</i>	68
3.3.3	<i>Slice Memory</i>	69
3.3.4	<i>Synchronous DRAM.....</i>	72
3.3.5	<i>Line-Pixel-Lookahead Method</i>	74
3.3.6	<i>Performance Evaluation.....</i>	77
3.3.6.1	<i>Miss rate analysis</i>	77
3.3.6.2	<i>Memory power modeling.....</i>	79
3.4	ELIMINATING MEMORY ACCESS TIMES.....	83
3.4.1	<i>1×4 and 4×1 Decoding Ordering</i>	83

3.4.2	<i>Motion Compensation</i>	85
3.4.2.1	<i>Horizontal-switch technique</i>	85
3.4.2.2	<i>Efficient Memory Interface</i>	87
3.4.3	<i>Deblocking Filter</i>	88
3.4.3.1	<i>Hybrid Filtering Schedule</i>	89
3.4.3.2	<i>Cycle Analysis</i>	93
3.4.4	<i>Performance Evaluation</i>	97
3.5	SUMMARY	98

CHAPTER 4 ERROR-ROBUST DESIGN APPROACH 100

4.1	BACKGROUND	100
4.2	DESIGN CHALLENGES	101
4.2.1	<i>System Highlights</i>	102
4.3	SOFT CAVLC DECODER	104
4.3.1	<i>Soft Decoding Concept</i>	104
4.3.2	<i>Soft VLC Decoding with Error Detection</i>	104
4.3.3	<i>Decoding Architecture</i>	108
4.3.3.1	<i>Code-Word Partitioning</i>	111
4.3.3.2	<i>Fully-Parallel Design</i>	112
4.3.4	<i>Performance Evaluation</i>	114
4.4	ERROR-CONCEALED DEBLOCKING FILTER	117
4.4.1	<i>Design Background</i>	117
4.4.2	<i>Error-Concealed Deblocking Filter (ECDF)</i>	119
4.4.2.1	<i>Edge Detection</i>	120
4.4.2.2	<i>Replacement</i>	120
4.4.2.3	<i>Concealed Strength</i>	121

4.4.3	<i>Performance Evaluations</i>	122
4.5	EMBEDDED COMPRESSOR/DE-COMPRESSOR	123
4.5.1	<i>Literature Reviews</i>	123
4.5.2	<i>Power-Aware and Error-Robust Features</i>	125
4.5.2.1	<i>Power Awareness by Least Significant Bit (LSB) Truncation/Insertion</i>	126
4.5.2.2	<i>Error Robustness by Erroneous Skipping/Padding</i>	128
4.5.3	<i>New Compressor/De-compressor for H.264/AVC</i>	130
4.5.3.1	<i>DPCM and Scanning Pattern Control</i>	131
4.5.3.2	<i>Truncated Huffman Tables</i>	133
4.5.4	<i>Virtual-to-Physical Address Mapping Technique</i>	134
4.5.5	<i>Performance Evaluation</i>	135
4.6	SUMMARY	139



CHAPTER 5 IMPLEMENTATION RESULTS		141
5.1	DESIGN FLOW	141
5.2	CHIP SPECIFICATION	144
5.2.1	<i>Supply Voltage Scaling</i>	147
5.3	COMPARISON WITH RELATED WORKS	149

CHAPTER 6 CONCLUSIONS AND FUTURE WORKS		152
6.1	CONCLUSIONS	152
6.1.1	<i>Dual-Mode Video Decoder for Multi-Standard Requirements</i>	152
6.1.2	<i>Low-Power Implementation for Portable Devices</i>	153
6.1.3	<i>Improved Visual Quality over Mobile Environments</i>	153
6.2	FUTURE WORKS	154
6.2.1	<i>Frame Re-compression Algorithm</i>	154
6.2.2	<i>Joint Source and Channel Design (JSCD)</i>	155

6.2.3	<i>Scalable Video Coding (SVC)</i>	157
6.2.4	<i>Multi-view Video Coding (MVC)</i>	157
6.2.4.1	<i>View Interpolation Prediction</i>	160
6.2.4.2	<i>Illumination Compensation</i>	161
	BIBLIOGRAPHY	162



List of Figures

FIGURE 1.1: BLOCK DIAGRAM OF A BASIC HYBRID DCT/MC CODING INFRASTRUCTURE.....	18
FIGURE 1.2: CORE POWER DISSIPATION IN DIFFERENT TYPES OF VIDEO DECODERS.....	29
FIGURE 2.1: SYSTEM BLOCK DIAGRAM.....	33
FIGURE 2.2: (A)(B) VLC TABLES IN CAVLC AND (C) THE MERGED TABLE.....	38
FIGURE 2.3: OVERVIEW OF COMBINED INTRA AND INTER PREDICTIONS.....	40
FIGURE 2.4: TWO INVERSE KERNELS FOR (A) MPEG-2 AND (B) H.264/AVC.....	41
FIGURE 2.5: $4 \times 4 / 8 \times 8$ IDCT CORE BLOCK DIAGRAM.....	42
FIGURE 2.6: SHARED LOCAL REGISTERS AND BILINEAR FILTERS FOR MPEG-2 AND H.264/AVC.	
.....	45
FIGURE 2.7: COMBINED LUMA/CHROMA INTERPOLATOR DESIGN IN H.264/AVC.....	46
FIGURE 2.8: VARIOUS TYPES OF DE-BLOCKING FILTERS	47
FIGURE 2.9: THE MODIFIED AND RELATED PIXELS IN THE PROCESS OF EDGE FILTER.....	49
FIGURE 2.10: A TRIPLE-MODE DECISION OF THE IN/POST-LOOP FILTER.....	51
FIGURE 2.11: TRIPLE P-I-P-O EDGE FILTER IN WEAK MODE.....	53
FIGURE 2.12: THE (A) DATA FLOW AND (B) PSEUDO CODE OF THE IN/POST-LOOP ALGORITHM.....	54
FIGURE 2.13: THE SUBJECTIVE QUALITY COMPARISON.....	56
FIGURE 2.14: A COST SUMMARY OF DUAL MPEG-2/H.264/AVC VIDEO DECODER.....	58
FIGURE 3.1: POWER PROFILING AND MEMORY USAGE IN [43].....	60
FIGURE 3.2: PIPELINED PATH BETWEEN STREAM INPUTS AND RESIDUAL PIXELS.....	62
FIGURE 3.3: (A) TRADITIONAL PIPELINED METHOD AND (B) TWO PIPELINED DOMAINS BY USING	

THE DPS METHOD	64
FIGURE 3.4: A DATA-PATH DIAGRAM OF RESIDUAL PATH BY DPS	65
FIGURE 3.5: THE (A) CONVENTIONAL [43] AND (B) PROPOSED MEMORY HIERARCHY	67
FIGURE 3.6: VL-FIFO AND PING-PONG SRAM IN THE CONTENT MEMORY	68
FIGURE 3.7: THE (A) SLICE MEMORY IN (B) INTRA PREDICTION AND (C) DEBLOCKING FILTER ...	71
FIGURE 3.8: (A) SIMPLIFIED ARCHITECTURE AND (B) CONFIGURATION OF A 4-BANK SDRAM .	73
FIGURE 3.9: THE (A) DATA FLOW AND (B) RELATED PSEUDO CODE IN THE LPL SCHEME	75
FIGURE 3.10: THE PROPOSED PREDICTION CIRCUIT FOR TAG PREDICTION	76
FIGURE 3.11: DATA ORGANIZATION BETWEEN SLICE PIXEL SRAM AND TAG PREDICTION	77
FIGURE 3.12: MISS RATE ANALYSIS WITH DIFFERENT SCALING FACTORS F	79
FIGURE 3.13: ANALYSIS OF POWER DISSIPATION ON EXTERNAL SDRAM AND INTERNAL SRAM.	
.....	81
FIGURE 3.14: (A) POWER SAVING ON MEMORY HIERARCHY AND (B) DRAM POWER PROFILING.	83
FIGURE 3.15: DIFFERENT DATA ORDERS IN (A) 4×1 AND (B) 1×4 DECODING ORDERS.....	85
FIGURE 3.16: DIFFERENT SCAN ORDERS IN MOTION COMPENSATION: (A) 2×2 RASTER SCAN; (B)	
4×4 RASTER SCAN; (C) EXTENDED 2×2 RASTER SCAN.....	87
FIGURE 3.17: A BLOCK DIAGRAM OF THE PROPOSED MEMORY CONTROLLER	88
FIGURE 3.18: FILTERING ORDERS IN (A) STANDARD-DEFINED AND (B) PROPOSED FILTERING	
SCHEDULE	90
FIGURE 3.19: THE (A) PARTITIONED MB AND (B) EACH TIME INDEX FOR HYBRID FILTERING	
SCHEDULE	91
FIGURE 3.20: THE (A) BLOCK DIAGRAM AND (B) ARCHITECTURE FOR THE PROPOSED	
DEBLOCKING FILTER.....	93
FIGURE 3.21: PROCESSING CYCLE BREAKDOWN IN EACH ARCHITECTURAL DESIGN PHASE	97
FIGURE 3.22: POWER REDUCTION OF PROPOSED MPEG-2/H.264/AVC VIDEO DECODER	99
FIGURE 4.1: SOFT-INPUT H.264/AVC DECODING BLOCK DIAGRAM	103

FIGURE 4.2: SOFT VLC ALGORITHM USING GRAPH REPRESENTATION.....	106
FIGURE 4.3: SOFT VLC DECODING PATH W/T AND W/O ERRORS.....	108
FIGURE 4.4: THE (A) HANDSHAKE STRUCTURE AND (B) ENTROPY DECODER IN H.264/AVC.....	109
FIGURE 4.5: SOFT CAVLD BLOCK DIAGRAM.....	110
FIGURE 4.6: THE (A) CODEWORD PARTITIONING AND (B) PARTIAL <i>COEFF_TOKEN</i> CODING TABLE [1].....	112
FIGURE 4.7: (A) SOFT VLC DECODER BLOCK DIAGRAM AND (B) ASSOCIATED <i>BM</i> ARCHITECTURE.....	113
FIGURE 4.10: A HISTOGRAM OF PM/B IN TERMS OF MACROBLOCKS (MB).	116
FIGURE 4.11: THE BLOCK DIAGRAM OF THE PROPOSED ECDF.....	119
FIGURE 4.12: FOUR KINDS OF REPLACING MODES: (A) 90° , (B) 0° , (C) 45° , (D) 135°	121
FIGURE 4.13: A CORRUPTED FRAME WHEN USING FMO WITH CHECKER-BOARD TYPE.....	122
FIGURE 4.14: SUBJECTIVE QUALITY COMPARISON BETWEEN THE (A) PROPOSED ALGORITHM AND (B) BI.....	123
FIGURE 4.15: SYSTEM BLOCK DIAGRAM OF COMPRESSOR/DE-COMPRESSOR.....	126
FIGURE 4.16: (A) A CORRUPTED FRAME AND ERROR-ROBUST (B) COMPRESSOR AND (C) DE-COMPRESSOR.....	129
FIGURE 4.17: PROPOSED (A) COMPRESSOR AND (B) DE-COMPRESSOR.....	131
FIGURE 4.18: THE HORIZONTAL AND VERTICAL SCANNING CONTROL.....	132
FIGURE 4.19: (A) SDRAM ORGANIZATION AND (B) DATA PACKING IN 4x4 PIXELS.....	134
FIGURE 4.20: A VIRTUAL TO PHYSICAL ADDRESS MAPPING.....	135
FIGURE 4.21: OBJECTIVE VISUAL QUALITY FOR POST-UPGRADE EQUATION.....	136
FIGURE 5.1: A (A) DESIGN FLOW AND (B) POWER REDUCTION OF THIS VIDEO DECODER.	144
FIGURE 5.2: VERIFICATION ENVIRONMENT.....	144
FIGURE 5.3: CHIP MICROGRAPH.....	145
FIGURE 5.4: SHMOO PLOT.....	148

FIGURE 5.5: POWER DISSIPATION COMPARISON.....	151
FIGURE 6.1: (A) CAPTURING AND PROCESSING PARTS OF FTV SYSTEM. (B) FREE VIEWPOINT IMAGES GENERATED IN REAL TIME.	158
FIGURE 6.2: EXAMPLE OF A 3D-TV SYSTEM.	159
FIGURE 6.3: VIEW MORPHING: INTERPOLATING BEHAVIOR IN DIFFERENT VIEWS.	160



List of Tables

TABLE 1.1: ALL PROFILES IN MPEG-2 VIDEO STANDARD.	19
TABLE 1.2: ALL LEVELS DEFINED IN MPEG-2.	20
TABLE 1.3: EXISTING APPLICATIONS FOR H.264/AVC.	21
TABLE 1.4: ALL PROFILES AND CODING TOOLS IN H.264/AVC.	22
TABLE 1.5: ALL LEVELS DEFINED IN H.264/AVC.	24
TABLE 1.6: ERROR CHARACTERISTICS IN DIFFERENT APPLICATIONS [72].	30
TABLE 2.1: THE SIMILARITY ANALYSIS OF EACH KEY MODULE.	34
TABLE 2.2: NUMBER OF REGISTER NEEDED FOR MPEG-2/H.264 SYNTAX PARSER.....	35
TABLE 2.3: FEATURES OF DEBLOCKING FILTER IN DIFFERENT STANDARDS.	48
TABLE 2.4: A COMPOUND METHOD FOR THE STRENGTH DECISION.....	52
TABLE 2.5: VALUES OF T_{T2} WITH A FUNCTION OF QP.	55
TABLE 2.6: THE POST-LOOP FILTERING PERFORMANCE IN TERMS OF LUMA PSNR.....	55
TABLE 3.1: VARIOUS PIPELINED GRANULARITIES.	62
TABLE 3.2: DIFFERENT PIPELINE LEVELS IN EACH MODULE.....	65
TABLE 3.3: DATA ORGANIZATION IN SLICE MEMORY.	71
TABLE 3.4: THE CYCLE ANALYSIS OF THE DE-BLOCKING FILTER.....	95
TABLE 3.5: A HARDWARE SUMMARY FOR THE DEBLOCKING FILTER.....	96
TABLE 4.1: SUBJECTIVE AND OBJECTIVE VISUAL COMPARISON.	117
TABLE 4.2: PERFORMANCE MEASUREMENT OF DETECTION CAPABILITIES.	117
TABLE 4.3: W_{PSNR} FOR LSB TRUNCATION [103].	127

TABLE 4.4: HORIZONTAL AND VERTICAL SCANNING PATTERNS	132
TABLE 4.5: TRUNCATED HUFFMAN TABLES	133
TABLE 4.6: COMPRESSION PERFORMANCE FOR VARIOUS SEQUENCES	136
TABLE 4.7: THE SUBJECTIVE QUALITY COMPARISON	137
TABLE 4.8: HARDWARE SUMMARY	137
TABLE 4.9: PERFORMANCE COMPARISON	139
TABLE 5.1: CHIP FEATURES	146
TABLE 5.2: A DETAILED COMPARISON WITH OTHER LEADING-EDGE APPROACHES.	150

