使用於全球定位系統接收器之頻率合成器設計

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摘要

本論文實現了使用於全球定位系統接收器之全差動頻率合成器。此頻率合成器必須能夠承受外來的雜訊, 尤其是共模雜訊造成的影響, 對於本地振盪器的劇跳特性影響更是嚴重。

本論文以 TSMC 0.35μm SiGe BiCMOS 3P3M 製程, 我們提出使用全差動控制之頻率合成器, 此架構能有效的避免共模雜訊所造成的頻率漂移。其中, 所提出的新型差動式輸出電荷幫浦, 能夠提供高擺幅控制電壓, 亦能有效的降低輸出波形的劇動。然而, 此新型電荷幫浦電路提供了較低的動態消耗功率, 但付出了所需之面積增加之缺點, 輸出控制電壓擺幅可達±2.3V, 其中±1V爲線性充放電區段。整體的總消耗功率爲22mW, 劇跳之均方根值爲22.5ps, 總晶片面積爲1.008X1.008mm^2。

關鍵詞: 電荷幫浦、差動控制、共模雜訊。

Design of Frequency Synthesizer for GPS Applications

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Abstract

A fully differential frequency synthesizer is realized applied to global positioning system (GPS) receivers in this thesis. The frequency synthesizer must be able to restrain the external noise, especially the common mode noise seriously affects the jitter performance of the local oscillator (LO).

The frequency synthesizer is fabricated in a TSMC 0.35μm BiCMOS 3P3M process. We propose a fully differential frequency synthesizer which effectively prevents the frequency drifting due to the common mode noise and reference spurs. The proposed novel differential output charge pump presents a large output swing and improves the jitter performance of the system. However, the smaller dynamic power dissipation in the novel charge pump but larger layout area are shown. This charge pump could provide a high output control swing as ± 2.3V consisting ± 1.5V linearity. The whole power dissipation is 22mW, the peak-to-peak long-term jitter is 22.5ps and the chip area including PADs is 1.008X1.008mm^2.

Keywords: Charge Pump, Differential Control, Common-Mode Noise

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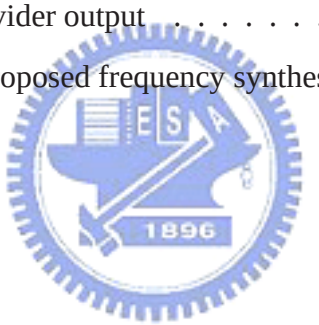

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Chapter 1

Introduction

Global positioning system applications are popularly used today. One of the key components of the GPS receiver requires a local oscillator. The Phase-Locked-Loop-based (PLL-based) frequency synthesizer is generally used for LO [14]. The frequency synthesizer must generate a stable output frequency signal quickly in order to receive the correct signal from the satellites while the power is applied. The frequency synthesizer normally includes five parts of devices: phase and frequency detector (PFD), divider, voltage controlled oscillator (VCO), charge pump and loop filter. However, the control voltage of the conventional single-ended VCO usually suffers the critical various due to noises and spurs which causes a large phase-various on the output signal of LO.

A fully differential frequency synthesizer is presented in this thesis. The characteristics of differential form eliminate the common noise on the control voltage. It effectively takes away the spur from the reference signal of the quartz crystal oscillator. A wide output swing charge pump is presented to reduce the gain of the VCO. The fully differential frequency synthesizer exhibits a better jitter performance compared to the single-ended control voltage form.

Chapter 2 reviews an overview and modeling of PLLs. The phase noises and spurs sources and effects are discussed in this chapter. Chapter 3 demonstrates the design theory, implementations and simulations results. The last chapter is the conclusion of the fully differential frequency synthesizer.

Chapter 2

An Overview and Modeling of PLLs

Frequency synthesizer is an essential part of nearly all multi frequency wireless transceivers. PLL-based frequency synthesizers are most frequently used as local oscillators in wireless receivers to down-converter the carrier frequency to a lower, intermediate frequency. Sometimes, PLLs are also used to perform frequency or phase modulation and demodulation, clock recovery, jitter suppression in communication, frequency synthesis, skew suppression, edge detection, etc [1]. In this chapter, the operation of basic PLL and its transfer function model are demonstrated, then different implementation methods for frequency synthesizers including the PLL-based frequency synthesizers are discussed and compared in terms of their phase noise, frequency locking speed, and manufacturing cost. Some of the implementation methods which discussed in the next few sections are currently in wide used.

2.1 Introduction of PLL

A majority of frequency synthesizers use a PLL [2]. A PLL is a feedback system that operates on the excess phase of periodic signals. As shown in Figure 2.1, a simple PLL consists of a phase detector (PD), a low-pass filter (LPF), and VCO.

Figure 2.2 shows the signals at various points of a typical PLL that has only a small phase difference between the input and output signals. At first, the PD generates pulses whose widths are equal to the time difference between zero crossings of the input and output. Next, these pulses are low-pass filtered to produce the DC value that sustains the

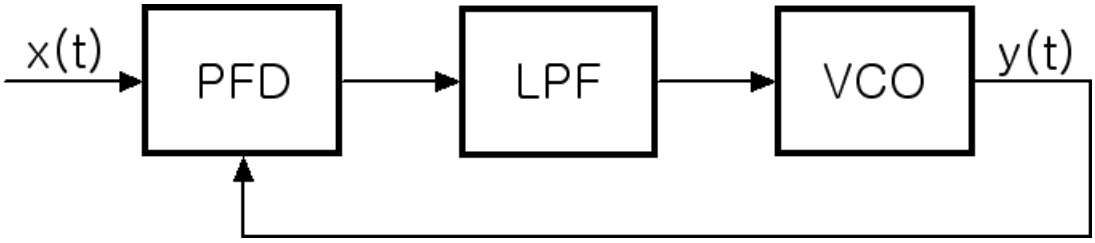


Figure 2.1: A basic phase-locked loop

VCO oscillation at the required frequency.

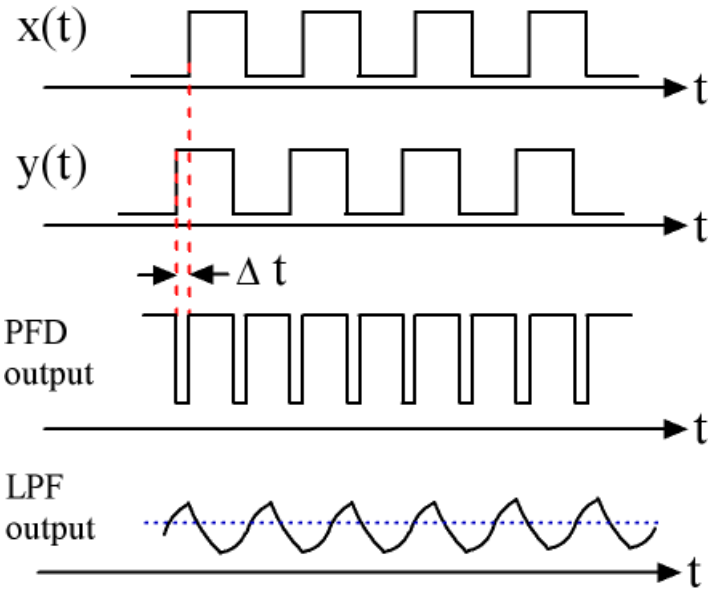


Figure 2.2: Waveforms in a PLL

In Figure 2.3, the overall response of the PLL that was in a locked status before ($t = t_0$) but which enforced a small frequency shift as its input ($t = t_0$) is shown. The phase detector generates increasingly wider pulses because the input frequency is temporarily faster than VCO output frequency. Each of these wider pulses creates an increasingly higher DC voltage at the output of the LPF.

Then, the higher DC output voltage of LPF increases the VCO output frequency. As the difference between the input and output frequencies is diminished by the negative feedback function, the width of the phase comparison pulses decreases. Eventually, the DC output voltage of the LPF becomes slightly greater than its value before ($t = t_0$) [4].

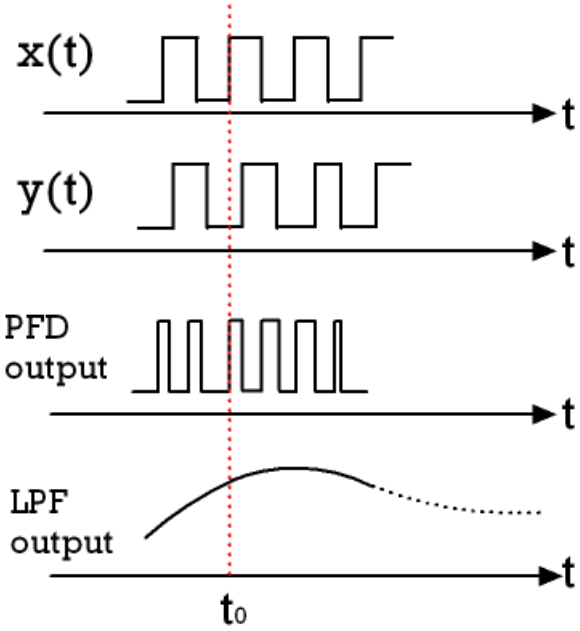


Figure 2.3: Response of a PLL to a small frequency step

2.2 Modeling and Analysis of PLL

Although a PLL is normally a non-linear device because of phase and frequency detector (PFD), divider, and prescaler, it can be accurately analyzed using a linear device model when the loop is in a locked status.

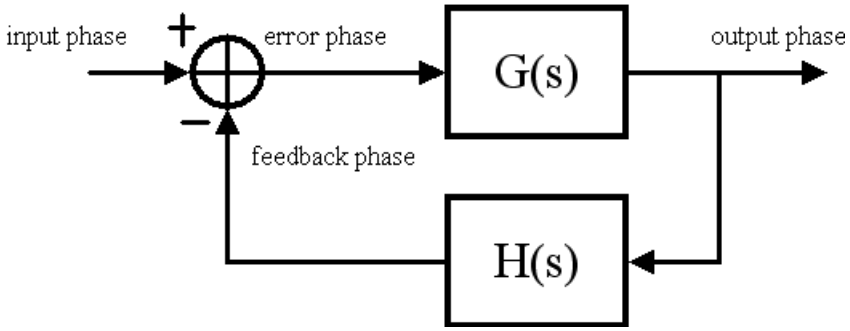


Figure 2.4: A single loop feedback control system

A basic linear feedback control system is shown in Figure 2.4. This control system

model will be used to derive and analyze the transfer functions of a PLL. In this system model, the closed-loop transfer function is given as a function of feed-forward gain, G(s), and feedback gain, $H(s)$, like $G(s)/[1 + G(s)H(s)]$, where s is a complex frequency. Another important feature of the system model is the steady-state error transfer function $1/[1 + G(s)H(s)]$[5], which indicates the remaining error after all transients have died out.

If the system loop-bandwidth is less than 20 times the reference input frequency and the system is in a locked status, then the digital PLL which consists of a divider with modulus N, a PFD with gain K_{PD} (V/rad), a LPF with transfer function $F(s)$, and a VCO with gain K_{VCO} (rad/sec·V) can also be analyzed using a continuous single-loop feedback control system model. The small-signal block diagram of the simple digital PLL where input signal with a frequency of f_i and a phase θ_i is applied is shown in Figure 2.5. In this figure, the closed-loop transfer function can be given by

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{f_o(s)}{f_i(s)} = \frac{G(s)}{1 + G(s)H(s)} \tag{2.1}$$

where

$$G(s) = \frac{K_{PD}K_{VCO}F(s)}{s} \tag{2.2}$$

and

$$H(s) = \frac{1}{N} \tag{2.3}$$

The steady-state error transfer function can be also given by

$$E(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{1}{1 + \frac{K_{PD}K_{VCO}F(s)}{Ns}} \tag{2.4}$$

where θ_e is the phase error between input phase and feedback phase

As shown in Figure 2.6, if a simple lag RC filter is used as a loop filter whose transfer function is $F(s) = 1/(1 + \tau s)$ when $\tau = RC$, then the closed-loop transfer function becomes

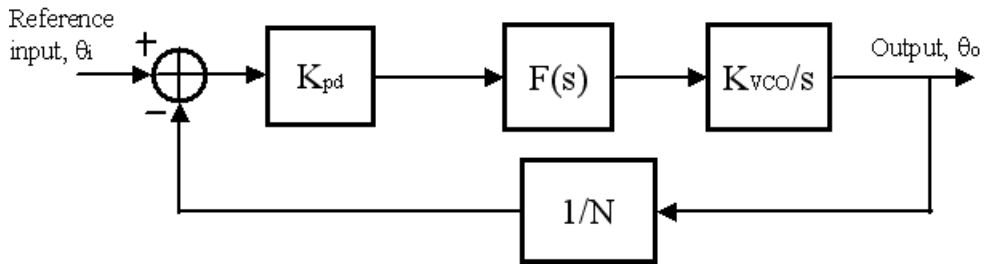


Figure 2.5: Small signal block diagram of the PLL

$$B(s) = \frac{NK_{PD}K_{VCO}}{N\tau s^2 + Ns + K_{PD}K_{VCO}} \tag{2.5}$$

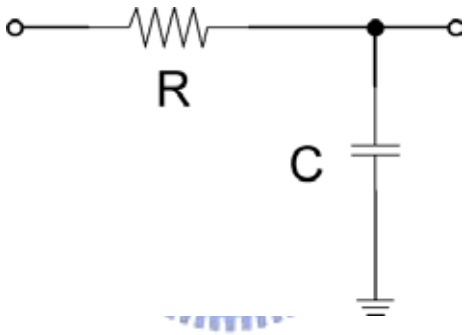


Figure 2.6: A lag RC filter

The open-loop transfer function of this system has one pole at the origin and the highest degree of this PLL system is two. So, this system is described as a type-one, second-order system. The type-one, second-order system can be mapped to a standard second-order control system form using standard parameter definitions. After the mapping, the equation (2.5) becomes

$$B(s) = \frac{N\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.6}$$

where

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N\tau}} \tag{2.7}$$

and

$$\zeta = \frac{1}{2}\sqrt{\frac{N}{K_{PD}K_{VCO}\tau}} \tag{2.8}$$

In the proceeding equations, the natural frequency, ω_n, provides the settling-time measurement of the loop bandwidth, whereas the damping factor, ζ, gives information about the degree of the loop stability.

The PLL using a simple lag RC filter (See Figure 2.6) has a disadvantage. From euqation (2.7) and (2.8), ω_n/ζ is fixed as $2K_{PD}K_{VCO}$ [6]. Thus, the natural frequency, ω_n and the damping factor, ζ cannot be selected independently. Therefore, a PLL design using the simple lag RC loop filter will be constrained by a compromise between n and . However, if a resistor is added in series with the capacitor like shown in Figure 2.7, then the loop filter transfer function $F(s)$ becomes

$$\zeta = \frac{1+\tau_2 s}{1+\tau_1 s} \tag{2.9}$$

where $\tau_1 = (R_1 + R_2)C$ and $\tau_2 = R_2 C$

The presence of a zero located at $s = -(1/\tau_2)$ in the loop filter changes the closed-loop transfer function of the type-one, second-order PLL to

$$B(s) = \frac{s\omega_n(2\zeta - \frac{N^2\omega_n}{K_{PD}K_{VCO}}) + N\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.10}$$

where

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}} \tag{2.11}$$

and

$$\zeta = \frac{1}{2}\sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}(\tau_2 + \frac{N}{K_{PD}K_{VCO}})} \tag{2.12}$$

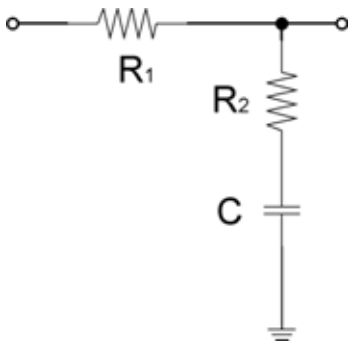


Figure 2.7: A passive lag-lead low-pass filter

In the above equations, the coupling between the parameters has been greatly relaxed since the two flexible design variables τ_1 and τ_2 determine loop parameters. However, the type-one, second-order loop has a finite DC gain that produces a large, static phase error, which increases the noise susceptibility of the system. Therefore, the finite, static phase error is not desirable.

If having a zero phase error in relations to step changes in the input frequency is necessary, the DC gain of a loop filter must be infinite. The infinite gain can be accomplished by including a pole at the origin of $F(s)$. The pole at the origin can be obtained by implementing an active loop filter using a large open-loop gain operational amplifier. The transfer function of Figure 2.8 is given by

$$F(s) = -\frac{1+\tau_2}{2\tau_1} \tag{2.13}$$

with $\tau_1 = R_1C$, and $\tau_2 = R_2C$.
The closed-loop transfer function is given by

$$B(s) = \frac{N\omega_n(2\zeta s + \omega_n)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.14}$$

where

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}} \tag{2.15}$$

and

$$\zeta = -\frac{\tau_2\omega_n}{2} \tag{2.16}$$

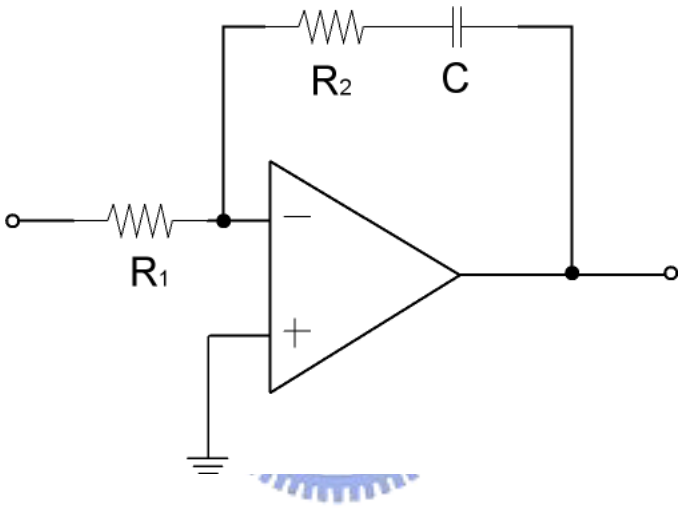


Figure 2.8: An active low-pass filter

The advantage of the active filter such as shown in Figure 2.8 over its passive counterpart like a lag RC filter or a passive lag-lead low-pass filter comes from the presence of a very high DC gain amplifier, which allows a nearly ideal integration in the loop filter. A filter with a pole at its origin helps to reduce the static phase error to a very small, residual value. Using an active filter, the static phase error of PLL can be reduced. However, an operational amplifier in the loop filter produces a significant amount of noise power within the PLL bandwidth. Therefore, the noise power contributes to the offset, which in turn causes unwanted sidebands in the output signal.

A simple way to achieve the same performance result as the active filter with a pole as its origin without using the noisy, offset-susceptible active operational amplifier is use a charge-pump circuit [7]. When compared with the previously discussed PLLs, the

charge-pump PLL offers two important advantages in addition to reducing static phase error. First, the capture range of a charge-pump PLL is only limited by the VCO output frequency range. Second, the static phase error is zero if mismatches and offsets of charge-pump are negligible [8].

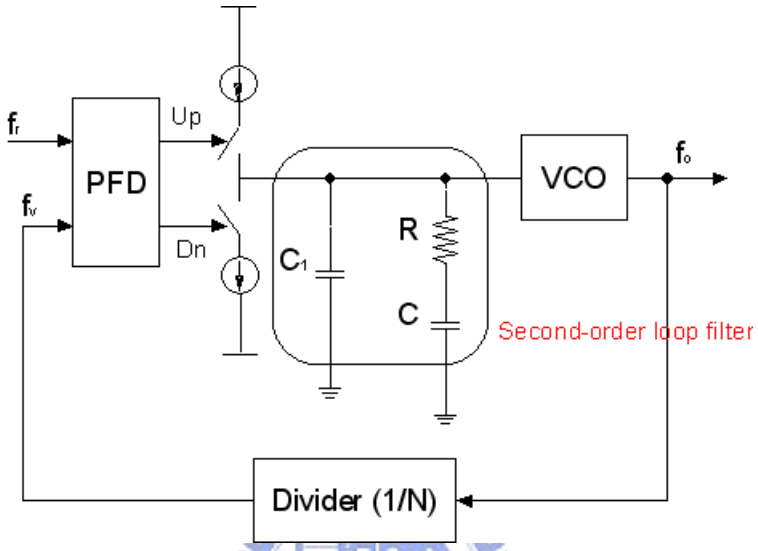


Figure 2.9: A charge-pump PLL

As in Figure 2.9, the charge-pump PLL includes a PFD, a charge pump, a LPF that composed of several capacitors and resistors, a VCO and a variable frequency divider. The signals from the PFD, Up and Dn, are used to control the charge-pump circuit. The purpose of the charge-pump circuit is to charge the VCO control voltage by applying positive or negative charges to the low-pass filter. The electric current magnitude of the charge-pump PLL is an important factor in the overall loop behavior because it determines the transfer function of the charge-pump circuit that is given by

$$\frac{I_d(s)}{\theta_e(s)} = \frac{I_p}{2\pi} \tag{2.17}$$

where

$I_d(s) =$ the Laplace transform of the average current over a cycle

$I_p =$ the pump current

$\theta_e(s) =$ is the Laplace transform of the phase difference at the PFD output

As shown in Figure 2.9, a simple, second-order passive low-pass filter is composed

of a resistor, R and two capacitors, C and C_1. The transfer function of this filter is given by

$$F(s) = \frac{1 + sRC}{s^2RCC_1 + s(C + C_1)} = \frac{1 + s\tau_2}{s(C + C_1(1 + s\tau_1))} \tag{2.18}$$

where $\tau_1 = \frac{CC_1}{C+C_1}$, and $\tau_2 = RC$.
Then, the closed-loop transfer function is found to be

$$B(s) = \frac{K_{PD}K_{VCO}(\frac{1+s\tau_2}{C+C_1})}{s^3 + (\frac{1}{\tau_1})s^2 + (\frac{K_{PD}K_{VCO}\tau_2}{N(C+C_1)s+(\frac{K_{PD}K_{VCO}}{N(C+C_1)\tau_1})})} \tag{2.19}$$

And open-loop transfer function $G(s)H(s)$ is

$$G(s)H(s) = (\frac{K_{PD}K_{VCO}}{N(C + C_1)})(\frac{1 + s\tau_2}{s^2(1 + s\tau_1)}) \tag{2.20}$$

According to the definition of type and order, this type is two, third-order PLL system. In this system, the pole created by capacitor C_1 that is needed to suppress the control voltage ripple coming from the resistor connected in a series must be lower than the reference input frequency in order to attenuate the spurs. But the pole must also be higher than the loop bandwidth; otherwise, the loop will become unstable [9].

The equation (2.19) can be approximated by a second-order expression to derive outcomes that give an intuitive feel of the transient response. The higher order terms are assumed to be small relative to the lower order terms. The simplified second order expression is given by

$$B(s) \cong \frac{\frac{K_{PD}K_{VCO}}{N(C+C_1)}(1 + sNCR)}{s^2 + s(\frac{K_{PD}K_{VCO}RC}{N(C+C_1)})} \tag{2.21}$$

Therefore, natural frequency and damping factor are given by

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N(C + C_1)}} \tag{2.22}$$

and

$$\zeta = (\frac{RC}{2})\omega_n \tag{2.23}$$

So, the poles are located at

$$-\zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2} \tag{2.24}$$

In the equation (2.21), the first term in the numerator has primary effects on time frequency response and the second expression has secondary effects because of the zero.

The time frequency response can be obtained using inverse Laplace transformation as in the equation (2.25) where the PLL is initially locked at frequency f_1 and its oscillation output frequency jumps to f_2 when the counter's modulus value is changed from N to N'.

$$F(t) = f_2 + (f_1 - f_2)e^{-\zeta\omega_n t}(cos(\omega_n\sqrt{1-\zeta^2}t) + \frac{\zeta - RC\omega_n}{\sqrt{1-\zeta^2}}sin(\omega_n\sqrt{1-\zeta^2}t)) \tag{2.25}$$

Since the expression in the large bracket has a maximum value of

$$\frac{1 - 2RC\zeta\omega_n + R^2C^2\omega_n^2}{\sqrt{1-\zeta^2}}$$

The lock time is given by

$$\text{Lock Time} = \frac{-\ln((\frac{\text{tol}}{f_2-f_1})(\frac{\sqrt{1-\zeta^2}}{1-2RC\zeta\omega_n+R^2C^2\omega_n^2}))}{\zeta\omega_n} \tag{2.26}$$

Where tol = tolerance of lock-time measurements
And the equation (2.26) can be approximated by

$$\text{Lock Time} = \frac{-\ln((\frac{\text{tol}}{f_2-f_1})\sqrt{1-\zeta^2})}{\zeta\omega_n} \tag{2.27}$$

Figure 2.10 shows the classical second order model for the transient response derived in the equation (2.26). The relationship between phase margin, damping factor, and natural frequency is shown in Table 2.1.

In general, theoretical and measured lock times has a difference that is caused by VCO and charge pump non-linearity, VCO input capacitance, and bad capacitor dielectrics that lead to longer lock time, discrete phase detector sampling effects, charge pump mismatch and leakage, board parasitic factor, and component leakages.

The second order filter in charge-pump PLL has the least thermal noise compared to other filter is appropriate. However, if the spur is larger than 10 times the loop bandwidth, then a higher order filter is required [9].

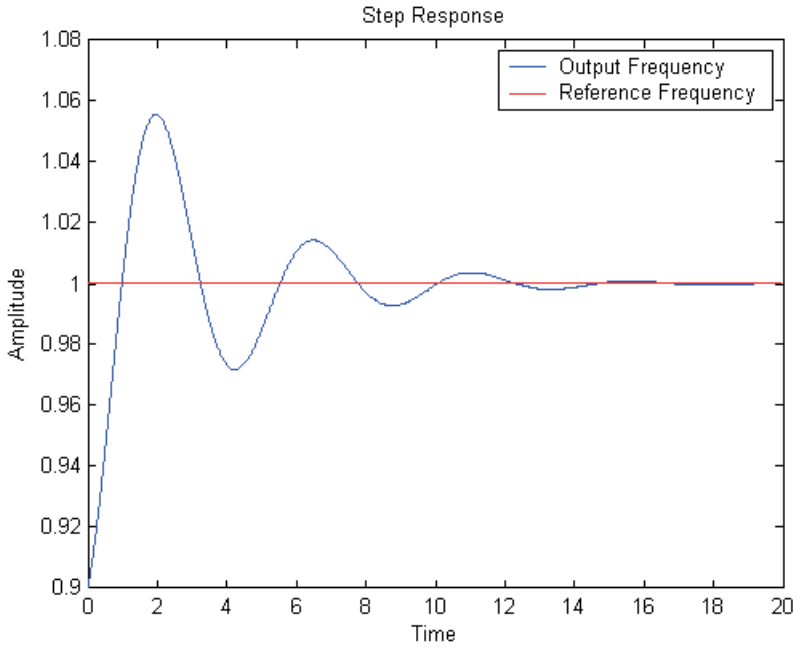


Figure 2.10: Classical models for the transient response of a PLL

The third order filter in charge pump PLL is shown in Figure 2.11.
The impedance of the third order filter is given by

$$F(s) = \frac{1 + sRC}{s(s^2 RR_2 CC_1 C_2 + s(RC(C_1 + C_2) + C_2 R_2(C + C_1)) + (C + C_1 + C_2))} \tag{2.28}$$

Then, the closed-loop transfer function is found to be

$$B(s) = \frac{1 + sRC}{a(s)} \tag{2.29}$$

Phase Margin, ϕ	Damping Factor, ζ	Natural Frequency ω_n
$30°$	0.6580	$0.7599\omega_c$
$35°$	0.6930	$0.7215\omega_c$
$40°$	0.7322	$0.6829\omega_c$
$45°$	0.7769	$0.6436\omega_c$
$50°$	0.8288	$0.6033\omega_c$
$55°$	0.8904	$0.5615\omega_c$
$60°$	0.9659	$0.5177\omega_c$
$65°$	1.0619	$0.4709\omega_c$
$70°$	1.1907	$0.4199\omega_c$

Table 2.1: Relationship between phase margin, damping factor, and natural frequency

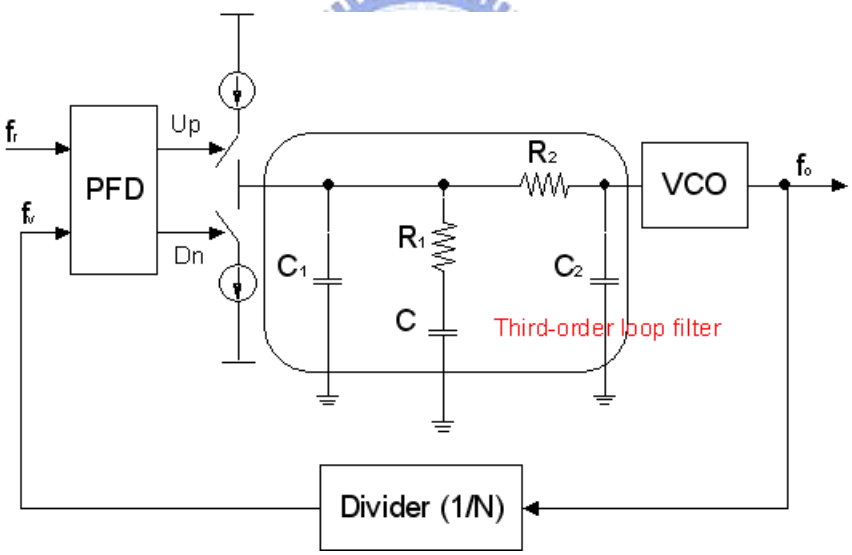


Figure 2.11: A charge-pump PLL with third-order filter

where $a(s) = (\frac{NC}{K_{PD}K_{VCO}})RC_1R_2C_2s^4 + ((\frac{N(C+C_1)}{K_{PD}K_{VCO}})R_2C_2 + (\frac{NC}{K_{PD}K_{VCO}})R(C_1+C_2))s^3 + (\frac{N(C+C_1+C_2)}{K_{PD}K_{VCO}})s^2 + RCs + 1$ With the third order filter, the additional pole must be lower than the reference input frequency to suppress the spurs effectively. However, the pole frequency has to be higher than the loop bandwidth in order to resolve the PLL's stability problem.

Fourth and higher order filter are most practical when the offset frequency spurs to be filtered is at least 20 times the loop bandwidth. However, the higher order filters are often unrealistic because the required capacitor values becomes too small relative to the VCO input capacitance and cause the filters to become unnecessarily complex.

Passive loop filters are generally preferred over active filter as a low-pass filter in a charge-pump PLL because of their low cost, simplicity, and low in-band phase noise. An additional in-band phase noise comes from the active device that is used in the loop filter. However, under circumstances where the VCO requires a higher tuning voltage than the PLL charge-pump can handle, active filters are used as a low-pass filter. In broadband tuning applications such as those required in cable TV tuners, VCOs commonly require a high tuning voltage. A high tuning voltage is also required for low-noise or high-power VCOs. Many design concepts used in active loop filter charge-pump PLL are analogous to those used in passive loop filter. However, a typical recommendation is to use at least a third order filter to suppress the phase noise coming from the active device.

The following two types of basic active filters exist: the first type uses the differential charge pump output and the other one uses the single charge pump output pin. In Figure 2.12, the charge pump active filter that uses a simple gain block is shown as an example of active filter that uses the single charge pump output pin.

The particular architecture involves placing an operational amplifier in front of the VCO. In this architecture, a third or higher order filter should be used to reduce the operational amplifier noise even though spurs are not reduced must as a result. The gain block, -A, in Figure 2.12 is used to invert the charge pump output, which can be negated by reversing the charge pump polarity. The gain block is also used to isolate input/output signals and to place a larger capacitor next to the VCO, thereby reducing the impact of the VCO input capacitance and loop filter resistor noise. Sometimes, the architecture in Figure 2.13 is used to center the charge-pump output voltage at half the charge-pump supply and to lower the spur level by predicting its patterns more accurately.

In general, an architecture that uses the differential charge-pump output is not recommended because it requires an operational amplifier and most PLLs do not have differential output pins.

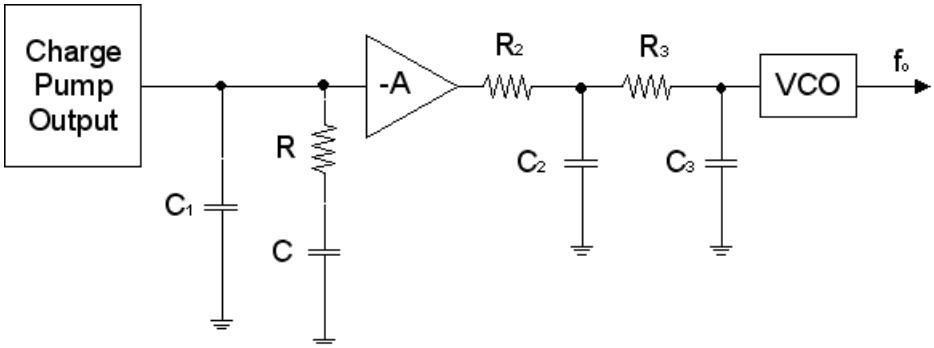


Figure 2.12: An active filter using the simple gain approach

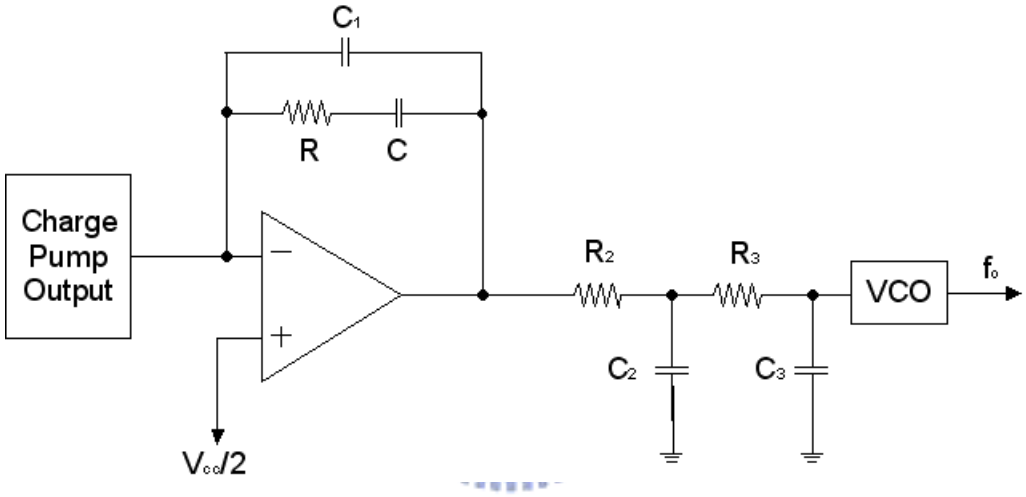


Figure 2.13: An active filter using the standard feedback approach

2.3 Phase Noise and Spurious Response

A purity of synthesized output signal is the most important requirement in all wireless communication applications. Ideally, this means the frequency synthesizer output should be a pure tone. However, in Figure 2.14, two different factors negatively affect the signal purity at the RF output in a PLL-based frequency synthesizer. The first factor is the phase noise associated with physical devices in the PLL. The phase noise limits the quality of the synthesized signal. The noises in the reference, PFD, loop filter, VCO and frequency divider all contribute in degrading the synthesized signal from an ideal pure sin wave. The other factor manifests itself as relatively high-energy, spurious sidebands. The sidebands have a systematic origin that makes them easier to handle than a fundamental,

random noise [1, 4].

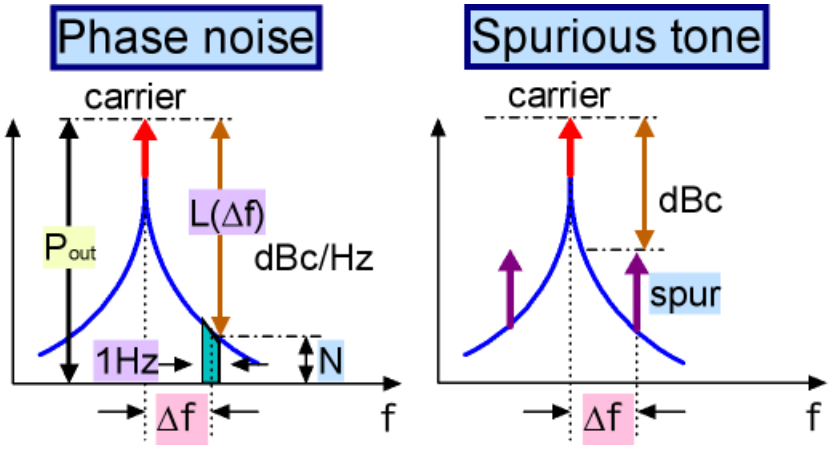


Figure 2.14: Phase noise and spurs in the frequency domain

When an electric current with a fixed frequency gets into the loop filter, the resulting spurs become a design issue. The spurs can be grouped into different categories depending on their causes.

The most common type spur is the reference spur that appears at multiples of the comparison frequency. Usually, spurs are caused by either a leakage or a charge pump mismatch. Depending on their cause, reference spur may behave differently when the comparison frequency or the loop filter is changed.

At lower comparison frequencies, a dominant cause of reference spur is a leakage effect. When the PLL is in a locked status, the charge pump will generate short, alternating electric current pulses with long time intervals where the charge pump is tri-stated. When the charge pump is in a tri-state, it has to be high impedance. However, some parasitic leakage will exist through the charge pump, VCO, and loop-filter capacitors. Among these different leakage sources, the charge pump tends to be the dominant one. The charge pump leakage causes FM modulation on the VCO tuning line and produces spurs.

The older PLLs have a large amount of electric current leakage and such leakage used to be the main reason for spurs. Nowadays, the electric current leakage inside PLLs is quite small. Therefore, other factors dominate in creating spurs expect at low comparison frequencies. The characteristics of spurs created by factors other than the electric current leakage are determined by the charge-pump turn-on-time for short, alternative pulses. Several factors affect the width of alternating pulses including charge pump mis-

match, unequal transistor turn-on-time, dead-zone elimination circuitry, and inaccuracies in the fractional calibration circuitry [10, 11].

The charge pump mismatch comes from the mismatching of its sink and source electric currents. If the mismatch is big, then a wider correction pulse is necessary and larger spurs are generated. The unequal turn-on-time is caused by the mobility difference between P-type and N-type transistors. The elimination circuitry used to keep the PLL out of the dead zone causes an additional gate delay at zero-phase error. All theses factors make the width of the charge pump correction pulse wider and increase spurs.

To reduce spurs, a high-order loop filter can be utilized to suppress the reference frequency spurs and a much smaller loop bandwidth than the reference frequency can be used. The electric current leakage arising from the charge-pump circuit, loop filter, varactor diodes and other components should be reduced in order to achieve low spurs signal. Another method for reducing spurs is to use a higher reference frequency adapted in the fractional-N synthesis technique.

Spurs in a frequency synthesizer can be evaluated using the following analysis. Because spurs are caused by the PLL when a signal with an AC component exists in the tuning line of the VCO, the VCO tuning voltage can be described as

$$V_{tune} = V_{DC} + V_{AC}(t) \tag{2.30}$$

where

V_{tune} = VCO tuning voltage

V_{DC} = DC component of tuning voltage in the VCO

V_{AC} = AC component of tuning voltage in the VCO = $V_m sin(\omega_m t)$

ω_m = modulating frequency = comparison frequency

So, the VCO output is given by

$$V(t) = Acos(\omega_0 t + \beta sin(\omega_m t)) \tag{2.31}$$

where

ω_0 = carrier frequency

β = modulated index

Finally, using the Fourier Series to determine the terms of Bessel function [4], the

VCO output can be expressed as

$$V(t) = Acos(\omega_0 t + \beta sin(\omega_m t)) \tag{2.32}$$

$$= A \sum_{m=-\infty}^{\infty} J_m(\beta) cos(\omega_0 t + m\omega_m t) \tag{2.33}$$

From the equation (2.33), the sideband levels can be defined as $J_0(\beta) \approx 1$, $J_1(\beta) \approx \beta/2$, and $J_2(\beta) \approx \beta^2/8$

The phase noise can be analyzed using a linear, small-signal model of the PLL loop that is shown in Figure 2.15.

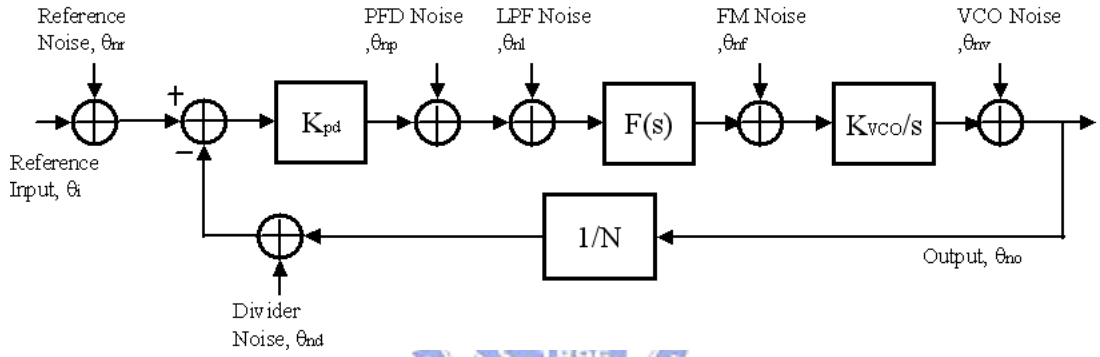


Figure 2.15: Small signal block diagram of the PLL with noise sources

A PLL that is composed of a phase and frequency detector, a low-pass filter as a loop filter, a VCO, and a divider has many noise sources such as reference noise, VCO noise, loop filter noise, and divider noise etc. The reference noise (θ_{nr}) is the noise on the reference signal. The PFD noise (θ_{np}) is the noise generated by the Phase and Frequency Detector. The phase difference signal gets corrupted due to the PFD noise. When a pure electric current switching charge-pump circuit is used, the loop-filter noise (θ_{nl}) arises from the equivalent input noise sources of the amplifier that is used for an active loop filter, logic circuits and electric current source noises. The FM noise (θ_{nf}) represents a total noise coming from the pick-up noise at the VCO tuning input node and the VCO power supply noise. The VCO introduces the VCO noise (θ_{nv}) and most of the noise energy is around the oscillator frequency. The divider noise, θ_{nd} is created by the frequency divider [12].

In Figure 2.15, the feed-forward gain G(s), feedback gain H(s), and open-loop gain

L(s) are given by

$$G(s) = \frac{K_{PD}K_{VCO}F(S)}{s} \tag{2.34}$$

$$H(s) = \frac{1}{N} \tag{2.35}$$

$$L(s) = G(s)H(s) = \frac{K_{PD}K_{VCO}F(s)}{Ns} \tag{2.36}$$

And the transfer functions for various noise sources can be expressed as

$$\text{Crystal-reference} = \frac{\theta_{no}}{\theta_{nr}} = \frac{\frac{K_{PD}K_{VCO}}{s}}{1+\frac{K_{PD}K_{VCO}F(s)}{Ns}} = \frac{NL(s)}{1+L(s)} \tag{2.37}$$

$$\text{PFD} = \text{Loop filter} = \frac{\theta_{no}}{\theta_{np}} = \frac{\theta_{no}}{\theta_{nl}} = \frac{\frac{K_{VCO}F(s)}{s}}{1+\frac{K_{PD}K_{VCO}F(s)}{Ns}} = \frac{NL(s)}{K_{PD}(1+L(s))} \tag{2.38}$$

$$\text{FM} = \frac{\theta_{no}}{\theta_{nf}} = \frac{\frac{K_{VCO}}{s}}{1+\frac{K_{PD}K_{VCO}F(s)}{Ns}} = \frac{NL(s)}{K_{PD}F(s)(1+L(s))} \tag{2.39}$$

$$\text{N divider} = \frac{\theta_{no}}{\theta_{nd}} = \frac{\frac{K_{PD}K_{VCO}F(s)}{s}}{1+\frac{K_{PD}K_{VCO}F(s)}{Ns}} = \frac{NL(s)}{1+L(s)} \tag{2.40}$$

$$\text{VCO} = \frac{\theta_{no}}{\theta_{nv}} = \frac{1}{1+\frac{K_{PD}K_{VCO}F(s)}{Ns}} = \frac{1}{1+L(s)} \tag{2.41}$$

If a reference divider, 1/R, generates various reference frequencies, that is also creates a noise that is given by

$$\text{R divider} = \frac{\theta_{no}}{\theta_{n}\text{R divider}} = \frac{\frac{K_{PD}K_{VCO}}{s}}{1+\frac{K_{PD}K_{VCO}F(s)}{Ns}} = \frac{NL(s)}{1+L(s)} \tag{2.42}$$

And the noise from the reference signal changes to

$$\text{Crystal reference} = \frac{\theta_{no}}{\theta_{nr}} = \frac{1}{R}\frac{\frac{K_{PD}K_{VCO}}{s}}{1+\frac{K_{PD}K_{VCO}F(s)}{Ns}} = \frac{1}{R}\frac{NL(s)}{1+L(s)} \tag{2.43}$$

Using the equation (2.36) through equation (2.41), the total output phase noise contributed by each noise source can be expressed by

$$\theta_{no}^2 = N^2(\theta_{nr}^2 + \theta_{neq}^2)(\frac{L(s)}{1+L(s)})^2 + \theta_{nv}^2(\frac{1}{1+L(s)})^2 \tag{2.44}$$

Where θ_{neq} is the equivalent input noise that is given by

$$\theta_{neq}^2 = \frac{1}{K_d^2}(\theta_{np}^2 + \theta_{nl}^2) + \frac{1}{K_d^2 F(s)^2}\theta_{nf}^2 + \theta_{nd}^2 \tag{2.45}$$

In equation (2.44), the crystal reference noise, PFD noise, N divider noise, FM noise, and loop-filter noise all contain a common factor in their transfer functions. The common factor is given by

$$\frac{L(s)}{1+L(s)} = \frac{1}{N}\frac{G(s)}{1+G(s)H(s)} \tag{2.46}$$

All of these noise sources are referred to as in-band noise sources. If the loop bandwidth ω_c and phase margin ϕ are define as [4]

$$\|G(j\omega_c)H\| = 1 \tag{2.47}$$

$$180 - \angle G(j\omega_c)H = \phi \tag{2.48}$$

Then, equation (2.46) can be approximated by

$$\frac{L(s)}{1+L(s)} = \frac{1}{N}\frac{G(s)}{1+G(s)H(s)} = \begin{cases} 1 & \text{For} \quad \omega << \omega_c \\ \frac{G(s)}{N} & \text{For} \quad \omega >> \omega_c \end{cases} \tag{2.49}$$

Therefore, this term (2.49) has a low-pass transfer function. So, the PLL functions as a low-pass filter for phase noise arising in the crystal reference noise, PFD noise, N divider noise, FM noise, and loop-filter noise. However, the VCO noise is multiplied by a different transfer function is given by

$$\frac{1}{1+L(s)} = \frac{1}{1+G(s)H(s)} \tag{2.50}$$

And this transfer function can be approximated by

$$\frac{1}{1+L(s)} = \frac{1}{1+G(s)H(s)} = \begin{cases} \frac{N}{G(s)} & \text{For} \quad \omega << \omega_c \\ 1 & \text{For} \quad \omega >> \omega_c \end{cases} \tag{2.51}$$

So, the equation (2.51) represents a high-pass filter for phase noise generated from the VCO. The transfer function of equation (2.49) is shown in Figure 2.16 and the transfer function of equation (2.51) is shown in Figure 2.17.

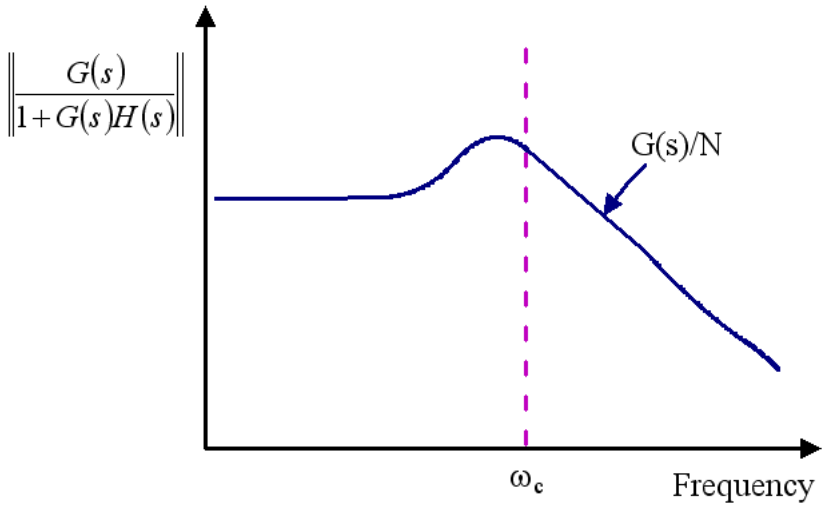


Figure 2.16: Transfer function multiplying all in-band noise sources

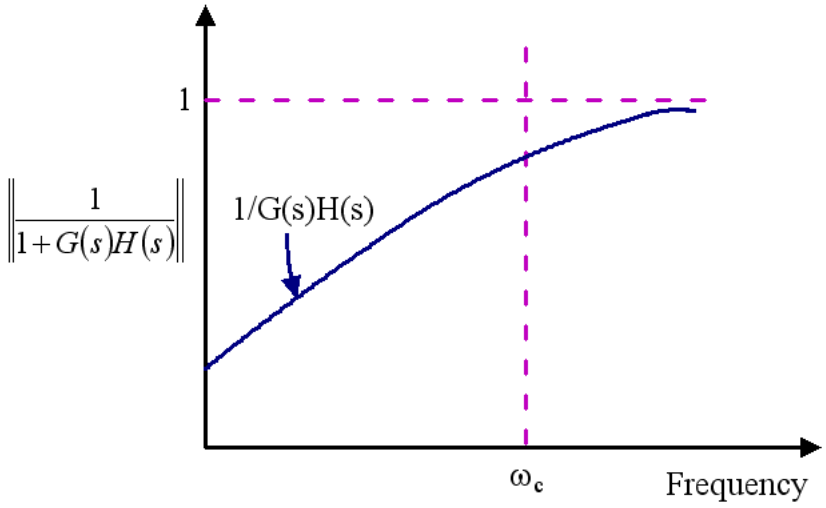


Figure 2.17: Transfer function multiplying the VCO noise

The results in the preceding sections come from the fact that the VCO is an emulated integrator with respect to the phase information that functions as a low-pass filter. Therefore, the loop bandwidth should be wide as possible in order to minimize the output phase noise caused by the VCO inherent phase noise θ_{nv}. However, in order to achieve

a minimum phase noise from the in-band noise sources, the loop bandwidth should be as narrow as possible while minimizing the in-band noise contributed by the other loop components. In addition to the conflict between the in-band noise sources and the VCO inherent noise, the loop bandwidth is further confined by the fact that the loop bandwidth needs to be less than the reference input frequency to keep the loop stable and to suppress spurs at the output. Therefore, to attain a minimal phase noise performance from in-band noise sources and the VCO inherent noise, the best place to put the loop bandwidth is where the VCO phase noise crosses the reference phase noise times N.

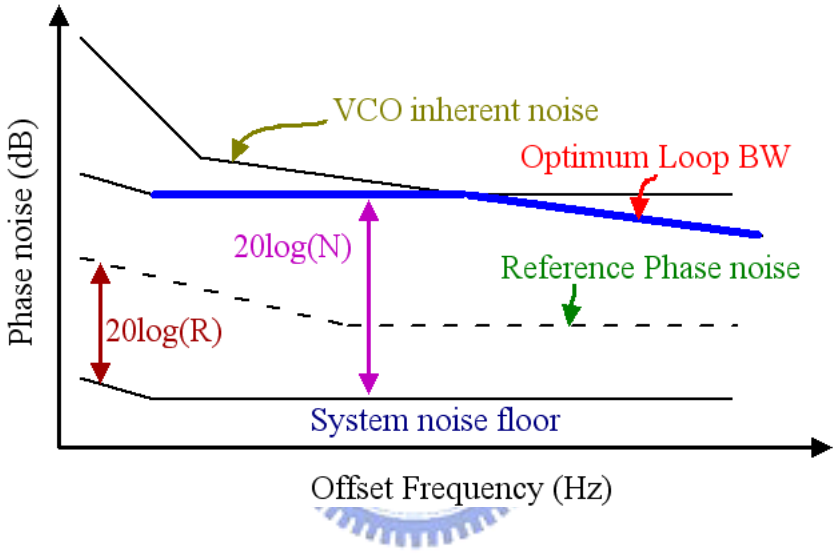


Figure 2.18: Optimal loop bandwidth of a PLL

The graphical estimation of the PLL's optimal loop bandwidth for achieving a minimum phase noise is shown in Figure 2.18. The optimal loop bandwidth is determined based on the following considerations: the phase noise inside the loop bandwidth should not be less than the in-band noise multiplied by N and the phase noise outside the loop bandwidth should not be less than the VCO inherent noise [13].

A several other factors such as the following could have an impact on the phase noise; in-band VCO phase noise contribution, lower charge pump gain phase noise adjustment, dual PLL adjustment, noisy crystal reference consideration, resister noise, and input insensitivity violation problem. For example, the VCO actually does contribute noise within the loop bandwidth in Figure 2.17. Specifically, the VCO tends to produce more noise within the loop bandwidth in case of a narrow bandwidth or a noisy VCO.

In Figure 2.19, the details of a PLL synthesizer's phase noise transfer functions based

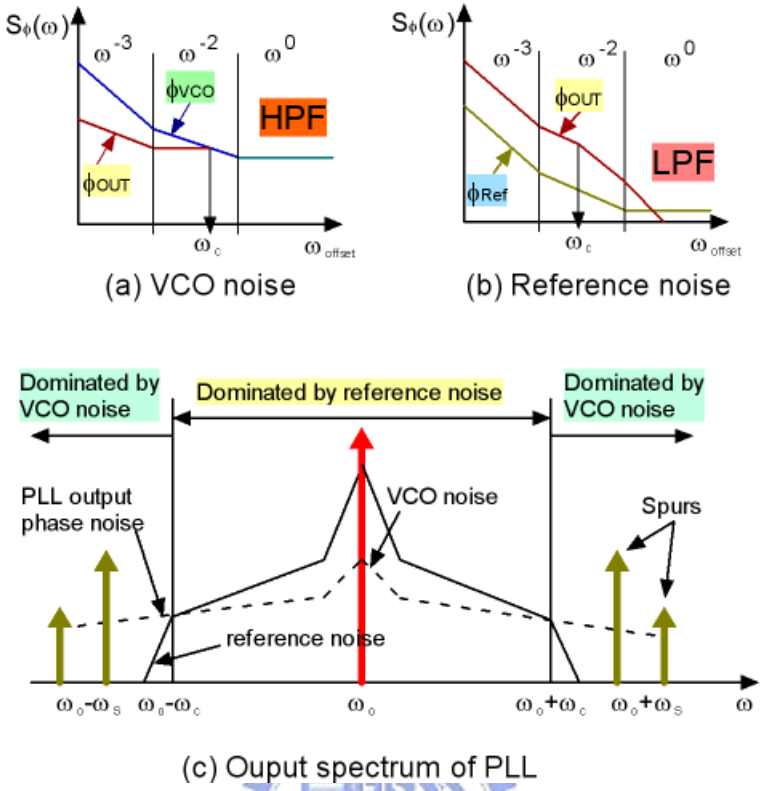


Figure 2.19: (a, b) Phase noise transfer functions in a PLL synthesizer (c) Typical phase noise and spurs spectral plot

on Lesson's equation, and its typical phase noise and spurs spectral waveforms are shown.

2.4 Summary

In this chapter, an overview and modeling of PLLs have been presented. A PLL composed of a PFD, a loop filter, a divider and a VCO is a negative feedback system that operates on the excess phase of periodic signals. The signals at various points of a typical PLL that has only a small phase difference between the input and output signal have been discussed.

Generally, a PLL is a non-linear device because of the divide-by-N divider, PFD, and prescaler. However, the PLL can be assumed to be a linear device if the loop is in a locked status when the reference frequency is at least 10 times larger than the loop

bandwidth. With this linear approximation, a several transfer functions including open loop and closed loop transfer functions, natural frequency, and damping factor have been derived using a simple servo control theory.

The effects of loop filters on the PLL performance have been considered. A simple way to reduce static phase error without an increased noise from the active device is a charge-pump PLL with passive loop filter. So, the charge-pump PLL architecture and its functional characteristics have been analyzed.

The optimal points of the loop bandwidth where the overall noise from in-band and VCO inherent noise is minimum has been discussed based on the characteristics of several phase noise and spur sources.

Chapter 3

Design of Frequency Synthesizer

3.1 An Overview of GPS Receiver Structure

The simplified GPS receiver structure is shown in Figure 3.1. The GPS receiver is applied to GPS L1-band receiver. The antenna receives the 1575.42MHz GPS carrier frequency, which contains the C/A code, P-code, and navigation messages used to commercial GPS receivers. The signal is amplified and mixed down to the intermediate frequency (IF) of 3.996MHz with sine and cosine wave quadrature mixers. The complex signal becomes real with the addition of real and imaginary components. Out of band images of the IF mixing is removed with the band pass filter (BPF). The real signal is then amplified one last time and transferred to digital base-band processing unit.

In the Figure 3.1, local oscillator is implemented as a PLL-based frequency synthesizer. It includes five parts of devices: PFD, divider, VCO, charge pump and loop filter. The whole frequency synthesizer is implemented in a fully differential form circuit. The fully differential synthesizer could effectively reduce the spurs due to the common mode noises. A wide output swing charge pump is presented to enhance the jitter performance by reducing the gain of VCO. A differential-voltage controlled oscillator is shown which provides the quadrature signal consisting of two sine wave 90 degrees of phase. The current mode logic technique is applied to the digital circuits as PFD and divider. It is proved to use the less dynamic power while operating in the high frequency status. The reference frequency of the quartz crystal oscillator in this thesis is 24.5535MHz. The frequency synthesizer generates a stable 1571.424MHz-clock applied to the mixer. The details of

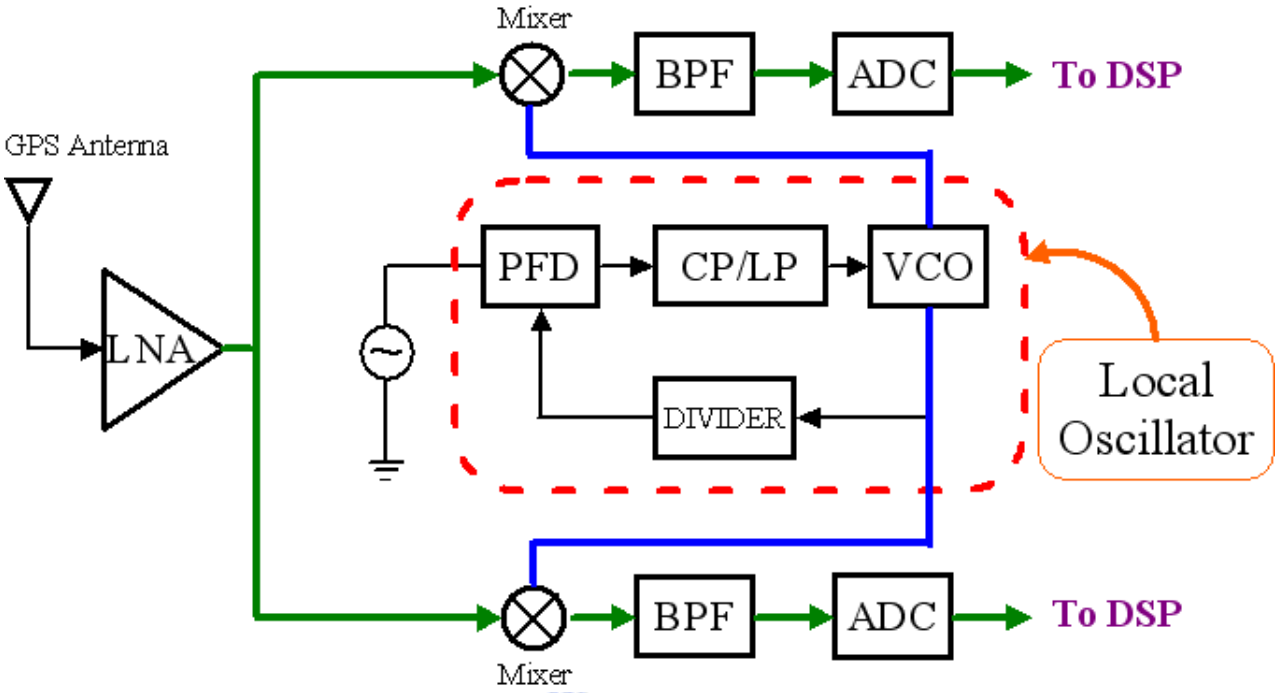


Figure 3.1: Simplified GPS receiver structure

each part are illustrated in the following sections.

3.2 Phase and Frequency Detector

3.2.1 Theory

Ideally, PD outputs the signal which is proportional to the difference of inputs as shown in Figure 3.2, where $V_1(t)$ and $V_2(t)$ are the input signals of PD. While there is a phase error between these signals, PD activates.

The simplified PD is implemented by exclusive-or gate (XOR) is shown in Figure 3.3. The pulse width of output changes according to the phase difference ($\Delta\phi$) of the input signals. This simplified PD generates the proportional pulse width based on the phase difference between input signals whether the positive or negative edges.

The conventional three-state PFD is shown in Figure 3.4 which including two resettable D flip-flops (DFFs) and a NAND gate. It generates Up and Dn signals to control

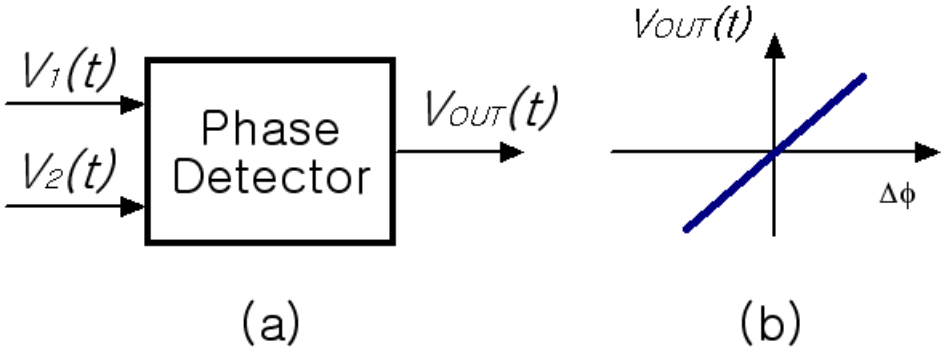


Figure 3.2: Phase Detector activates diagram

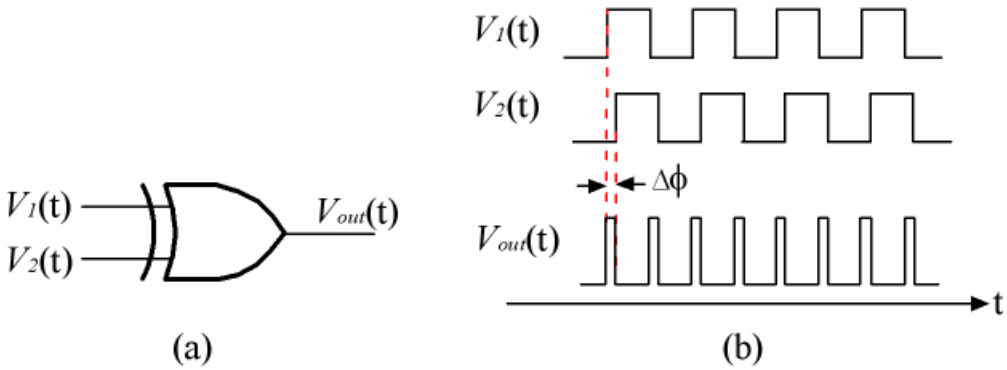


Figure 3.3: XOR gate PD

charging and discharging of the charge pump. The status diagram is shown in Figure 3.5. Up and Dn both are '0' state when initial state. Either of the input signals (CK_{ref} or CK_{VCO}) rises, the relative output node will be '1' state (Up='1' or Dn='1'). The status keeps on and recovers until the other state arises. This kind of PFD detects both of the phase and the frequency and delivers the error phase signal to the charge pump circuit.

The ideal characteristic curve of three-state PFD is shown in Figure 3.6. While the frequencies of the input signals are different, the phase error during each period is equal to $2\pi[(TCK_{ref} - TCK_{VCO})/\max(TCK_{ref}, TCK_{VCO})]$. Thus, the three-state PFD produces the proportional outputs in the range $0 \pm 2\pi$ according the phase difference during each frequency acquisition cycle. The proportional outputs pass through the charge pump to charge or discharge the loop filter. Finally, it tunes the output frequency of VCO to reach frequency-locked state by the loop [15].

MOS Current Mode Logic (MCML) circuits are useful. It has been investigated for

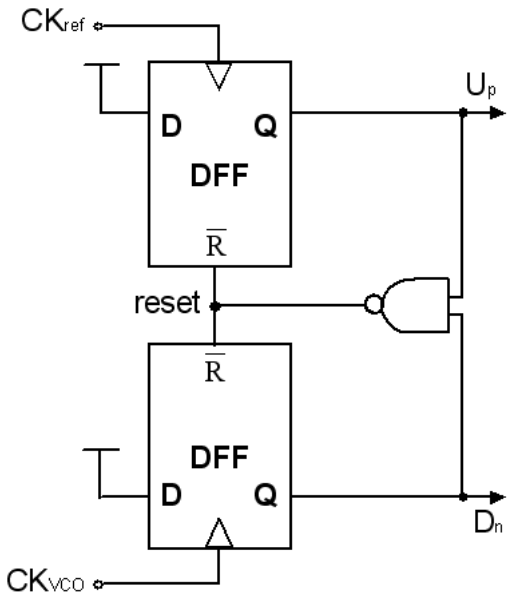


Figure 3.4: Conventional three-state PFD

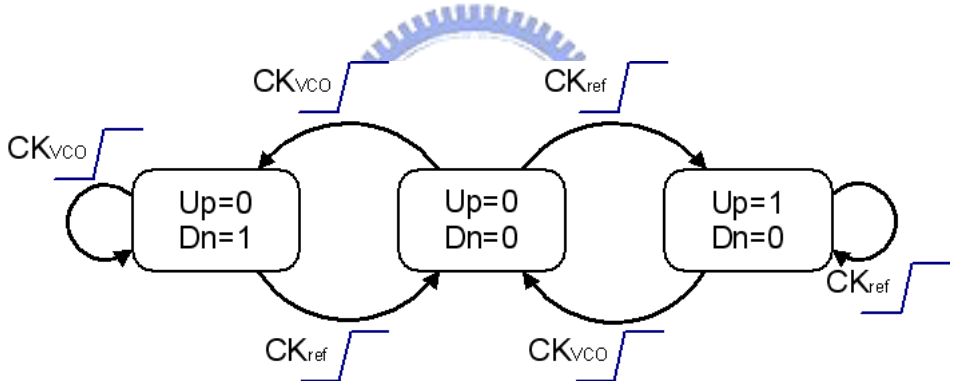


Figure 3.5: Status diagram of three-state PFD

use in high-speed mixed signal environments due to its reduced switching noise, its lower power dissipation at high frequencies compared to standard CMOS logic, and its immunity to common-mode noise [17]. It also could effectively reduce the dynamic power in RF applications. The operated theory is shown in Figure 3.6. The CML circuit could be sub-divided into three main elements. The first one is the sink-current source which determines the maximum operated speed and the static power. The second part is the switching circuits. CML accomplishes the different logic circuits through the distinct switch combinations. The last part is the passive or active load. The load determines the voltage difference between the logic level ’0’ and ’1’. The maximum operating frequency

and the required operating power of an MCML gate can be altered by changing the DC bias condition of the gate. This mechanism enables performance versus power trade-offs to be made during circuit operation.

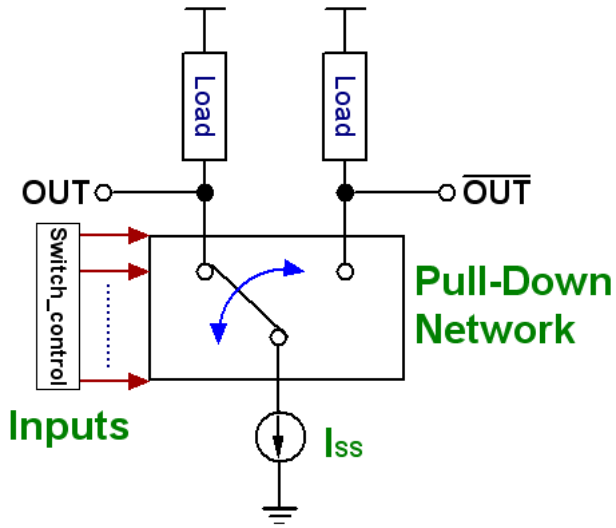


Figure 3.6: Operated Theory of CML

Using the active P-type MOS load could effectively ensure the logic level of '0' and '1'. The example of INVTER gate is shown in Figure 3.7. M1 and M2 perform as the switches, M3 represent a current source I_{SS}, and M4 and M5 are the active loads whose gates are driven by the adaptable MOS CML shown in Figure 3.8 [16]. In the branch where current is flowing, a resistive voltage drop is developed at the output while at the complementary output, no current flows through the load and the output is pulled to VDD. Using the adaptable bias control loop generates the control signal RFP which enforces the logic '0' level to follow a given voltage level V_{LOW}.

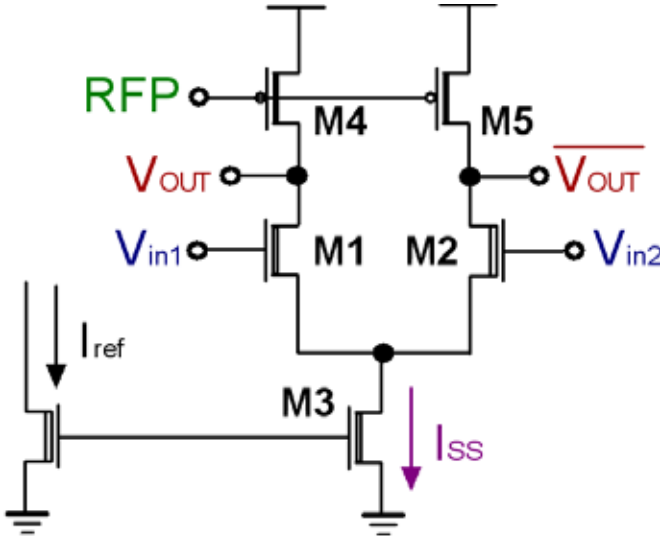


Figure 3.7: Example of CML INVERTER

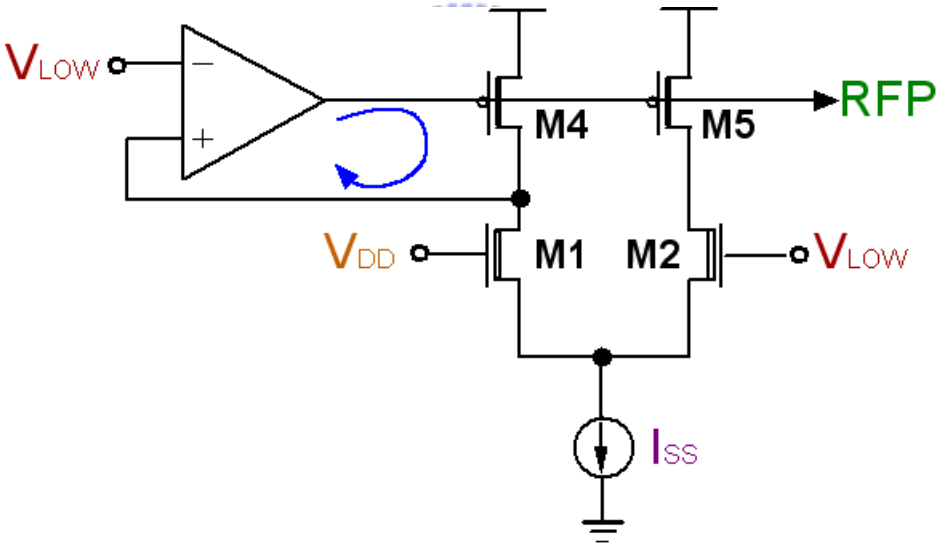


Figure 3.8: Implementation of the bias control loop

3.2.2 Simulation Results

The schematic indicated in 3.4 was simulated in Cadence using HSPICE simulation tool. Figure 3.9 shows the resulting waveforms for the case when the frequencies are equal, but the reference phase ϕ_{ref} leads the feedback phase ϕ_{fb}. Figure 3.10 presents the opposite phase situation. The logic low level V_{LOW} is set to 2.8V, thus the output swing

is ± 0.5V.

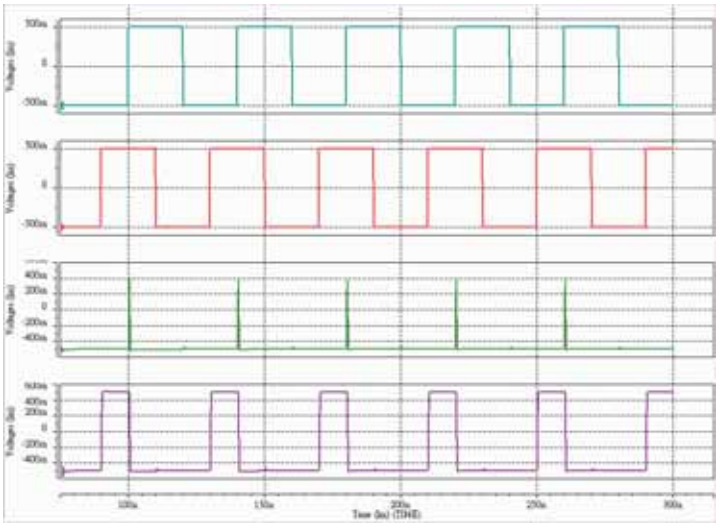


Figure 3.9: Resulting waveforms for ϕ_{ref} leads ϕ_{fb}

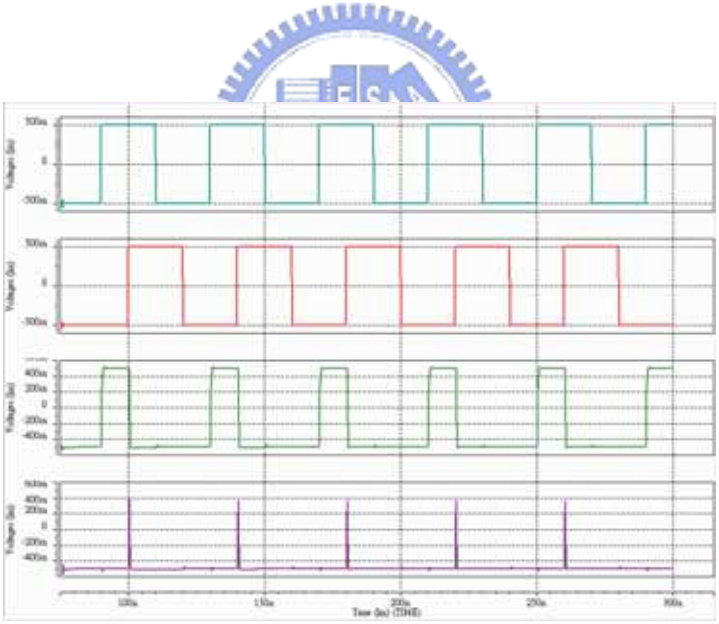


Figure 3.10: Resulting waveforms for ϕ_{ref} lags ϕ_{fb}

3.3 Divide-by-N Divider

3.3.1 Theory

Normally, the most different between PLL and the frequency synthesizer is that the frequency synthesizer has an additional frequency divider. There are commonly two kinds of architectures for divider implementation: synchronous-type and asynchronous-type dividers.

An asynchronous-type divider is shown in Figure 3.11 (a). We implement this type of divider in this thesis. The advantage of this type divider is that the circuit design is simpler. The input clock only enables the first DFF, and then its output signal enables the next DFF. And so on, the output frequency would be divided by 2^N, where N means the numbers of DFFs. Figure 3.11 (b) illustrates a synchronous-type divider with an NAND gate which generates the synchronous signal on purpose to synchronize. This kind of divider would be operated in the higher frequency, but we should notice the clock race problem [18].

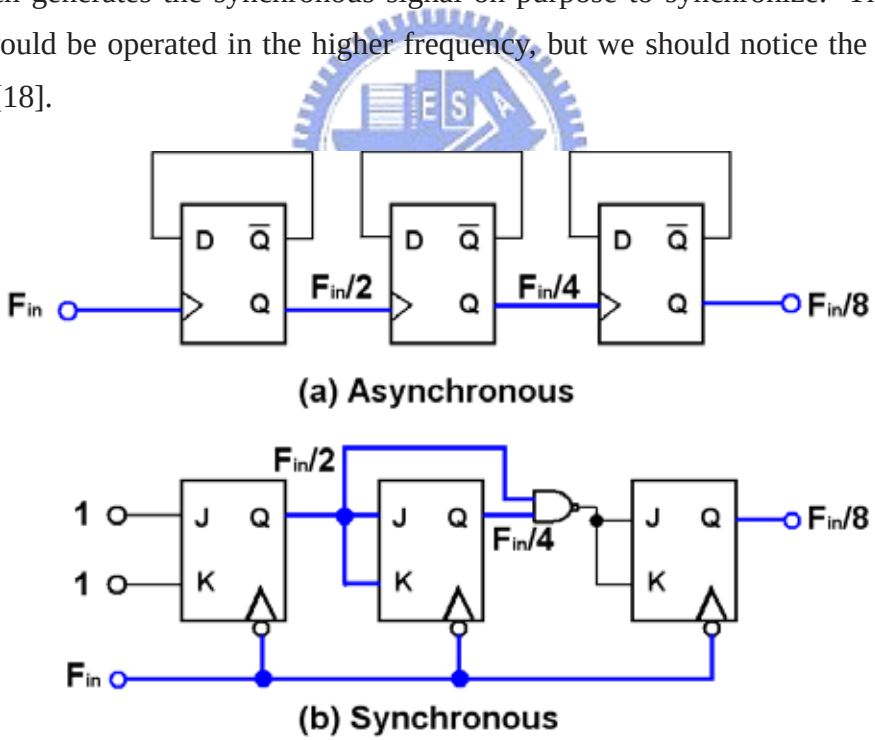


Figure 3.11: (a) Asynchronous-type divider (b) Synchronous-type divider

3.3.2 Implementation and Simulation Results

Figure 3.12 shows the divided waveform while the input frequency is equal to 1.6GHz. As shown in the graph, The output waveform divide the input frequency by 64 exactly. However, In Figure 3.13, the valid input frequency range which would be divided by 64 is 1GHz - 2.25GHz. The range is enough for tracking in the PLL.

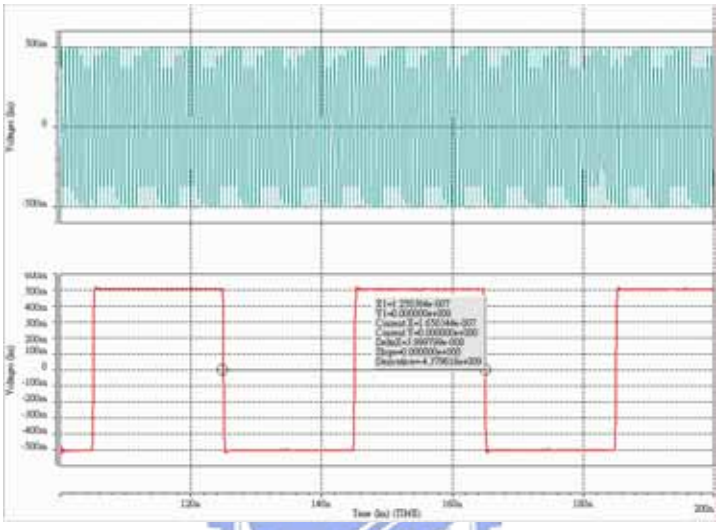


Figure 3.12: Divided output waveform with f_{in}=1.6GHz

3.4 Voltage Controlled Oscillator

3.4.1 Theory

The voltage controlled oscillator is perhaps the most crucial elements of the PLL because it directly provides the output signal of the PLL. A VCO can be built using ring structures, relaxation circuits, or LC resonant circuits. The LC design has the best noise and frequency performance owing to the large quality factor Q achievement with resonant networks [21]. However, adding high-quality inductor increases the cost and complexity of the chip, and also introduces problems such as the control of eddy currents. Ring oscillators, on the other hand, may require less die area than LC designs. The design is straightforward, and ring architectures can be used to provide multiple output phases and wide tuning ranges.

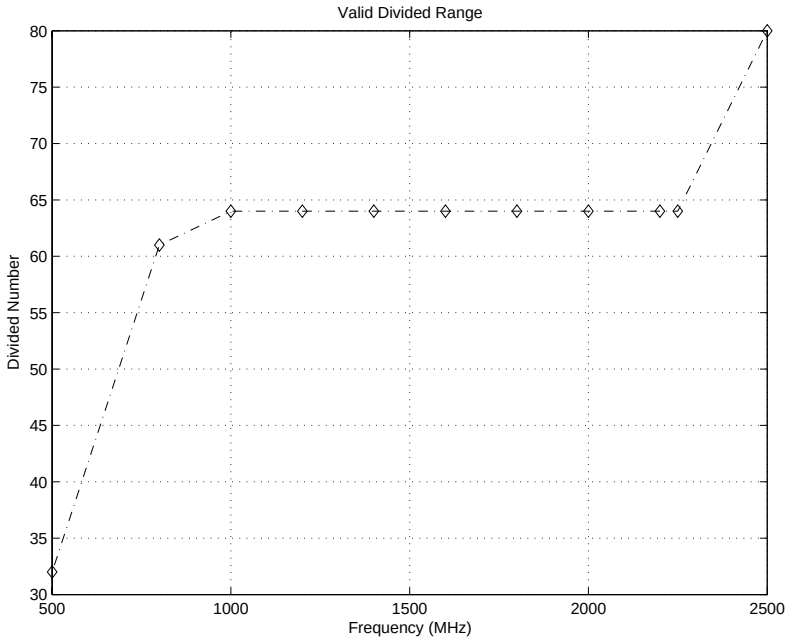


Figure 3.13: Valid input frequency range

The architecture of VCO we use here is the ring oscillator. In the Figure 3.1, the quadrature signal consisting of two sine wave 90 degrees of phase must be generated from VCO. The quadrature signal property could increase SNR 6dB in the received GPS signals. The ring voltage oscillator used in this thesis would produce these output signals without any other extra circuits, but the poor phase noise performance. Even though the phase noise performance is poor compared to the LC resonant circuits, it would be acceptable in GPS applications and save the area cost on the chip.

The ring oscillators consist of delay cells connected in cascade and in a closed loop, which provide enough gain and phase shift to satisfy the Barkhausen's oscillation criteria [22]. A 4-stage differential ring voltage controlled oscillator is shown in the Figure 3.14.

In these topologies, the oscillation frequency is given by

$$f = \frac{1}{2N\tau_d} \tag{3.1}$$

Where N is the number of delay cells in the ring, and τ_d is the delay time in the cell.

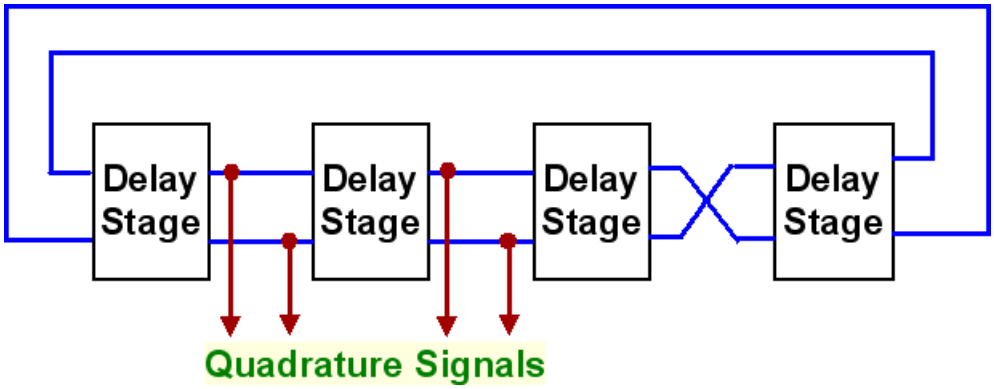


Figure 3.14: Basic structure of ring oscillators

3.4.2 Implementation of Voltage Controlled Oscillator

Each delay stage is implemented with the latch-type circuit in the Figure 3.15 [19]. This oscillator topology is the modified version of that presented in [20]. A single stage is comprised of a core switching pair M1/M2 with a negative resistance synthesized by cross-coupled pair M3/M4 in parallel. The resistor R_{diff} detects the difference voltage between VC1 and VC2 and transfers the difference voltage to the difference current via M7/M8. The VCO is tuned by steering current with M7/M8 between negative-resistance cell and the core switching pair. This structure has the advantage that the oscillation amplitude remains relatively constant even as current is steered through its core in order to change the oscillation frequency. Parasitic poles associated with the differential pair and cross-coupled pairs guarantee that each delay cell generates more than 45° of phase shift, which ensures the reliable oscillation can be realized over process and operating condition. The tuning current $I_{TUNE1,2}$ is sized to be less than the bias current I_{BIAS}, which guarantees that oscillation persists over the entire tuning range.

The effective output resistance is equal to R_D and cross-coupled pair M3/M4 in parallel. The cross-coupled pair forms a negative resistance shown in Figure 3.16. The effective negative resistance approximately equal to $-2/g_{m3,4}$, the transconductance of M3/M4, is related with the bias current I_{TUNE2}. Thus, the effective output resistance can be expressed as

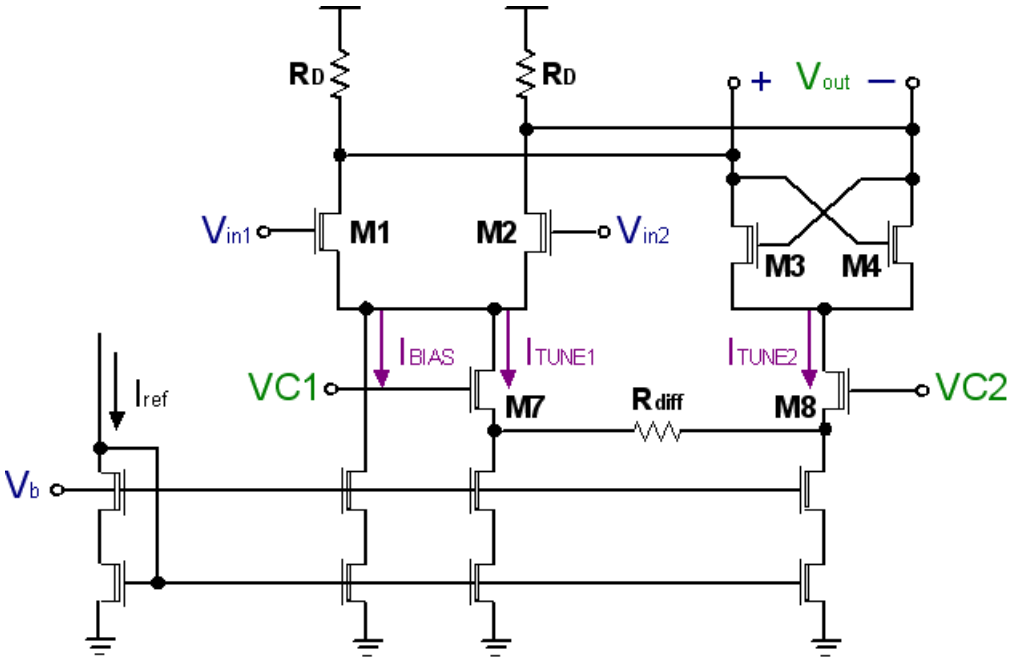


Figure 3.15: Delay cell of the VCO

$$R_{eff} = R_o//(-2/g_{m3,4}) = \frac{-2R_o/g_{m3,4}}{R_D - 2/g_{m3,4}} \tag{3.2}$$

Where R_o is equal to $R_D//r_{o1,2}$. Normally, The design value of $-2/g_{m3,4}$ must be greater than R_D.

Howeveer, VC1 and VC2 tunes the current amounts of T_{TUNE1} and T_{TUNE2} to control the effective output resistance of the delay stage. We define a tuning parameter $\Delta V = VC1 - VC2$ and $V_{CM} = (VC1 + VC2)/2$ determines the center frequency of VCO. The VCO tuning status can be sub-divided into three parts:

$$\begin{cases} I_{TUNE1} = I_{TUNE2} & \text{if } \Delta V = 0 \\ I_{TUNE1} > I_{TUNE2} & \text{if } \Delta V > 0 \\ I_{TUNE1} < I_{TUNE2} & \text{otherwise} \end{cases}$$

The oscillation frequency depends on the time constant $\tau = R_{eff}C_{eff}$. The effective capacitor value could be regarded as a fixed value. Thus, R_{eff} determines the oscillation frequency directly. However, (3.2) shows that the oscillation frequency arises while $g_{m3,4}$ decreases and R_o is given. The transconductance $g_{m3,4}$ is proportional to $\sqrt{I_{TUNE2}}$. While

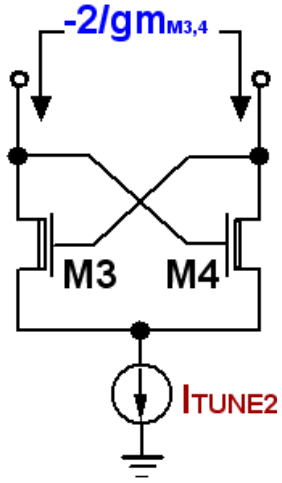


Figure 3.16: Cross-coupled pair forms the negative resistance

M7/8 are operated at the saturation region, the relationship between ΔV and I_{TUNE2} almost maintains linearity. As well as the tuning current I_{TUNE2} decreases, the other tuning current I_{TUNE1} enters to improve the linearity between ΔV and R_{eff}. This technique makes sure of the VCO gain K_{VCO} being invariable while M7/8 operated in the saturation region.

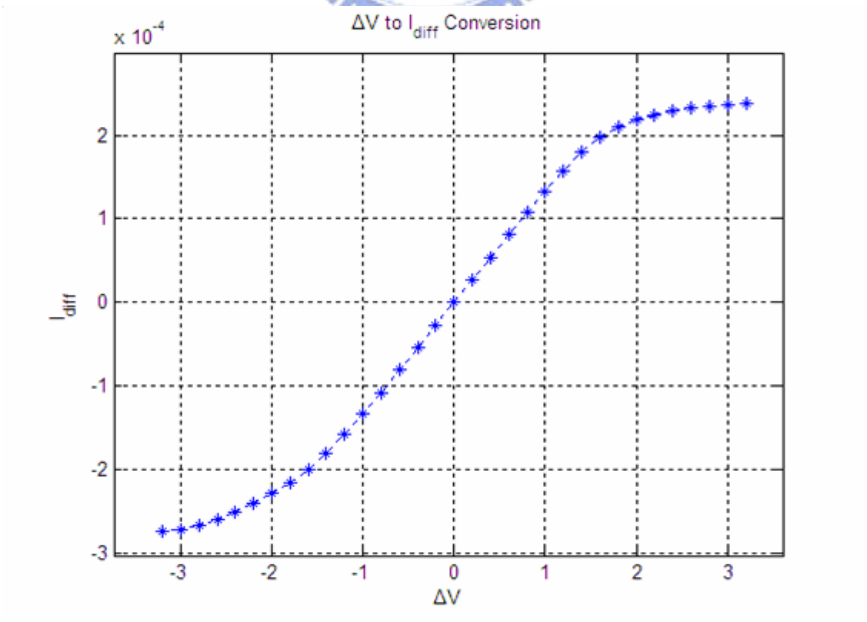


Figure 3.17: Relationship between I_{diff} and ΔV

3.4.3 Simulation Results

Figure 3.17 illustrates the relationship between the current flow I_{diff} on the sensible resistaor R_{diff} and the differential control voltage ΔV. The destrict among $\Delta V = \pm 1.0$V presents a high linear result. However, either the transistor M7 or M8 goes into the triode region while ΔV exceeding 1V. The results of relationship between the oscillation frequency f_{OSC} and ΔV are shown in Figure 3.18 to 3.20. As expect in result, we could observe that the result is linear among $\Delta V = \pm 1.0$ in three different corners (TT, FF, SS).

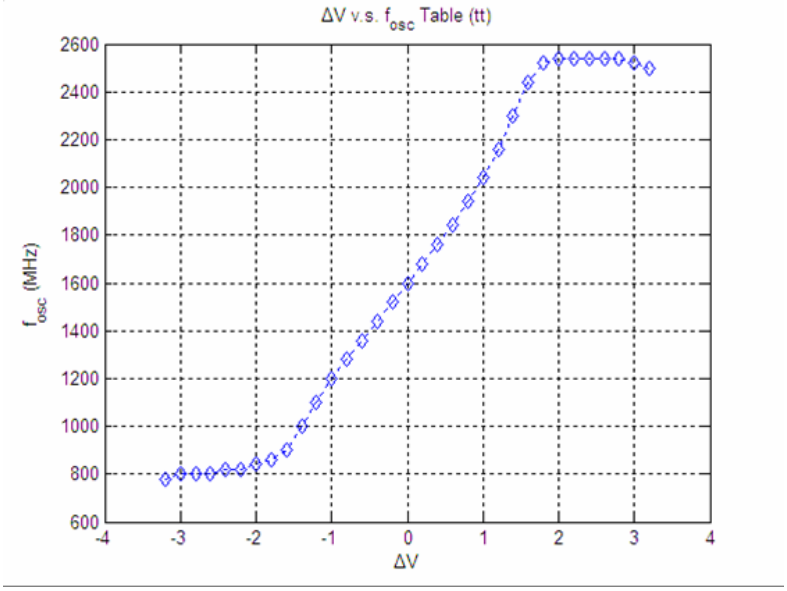


Figure 3.18: Relationship between f_{OSC} and ΔV (TT corner)

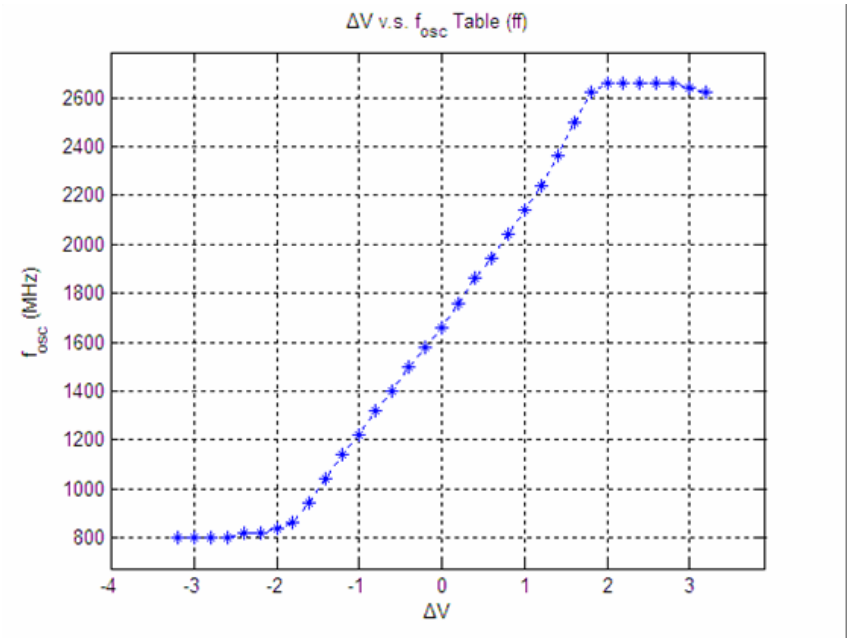


Figure 3.19: Relationship between f_{OSC} and ΔV (FF corner)

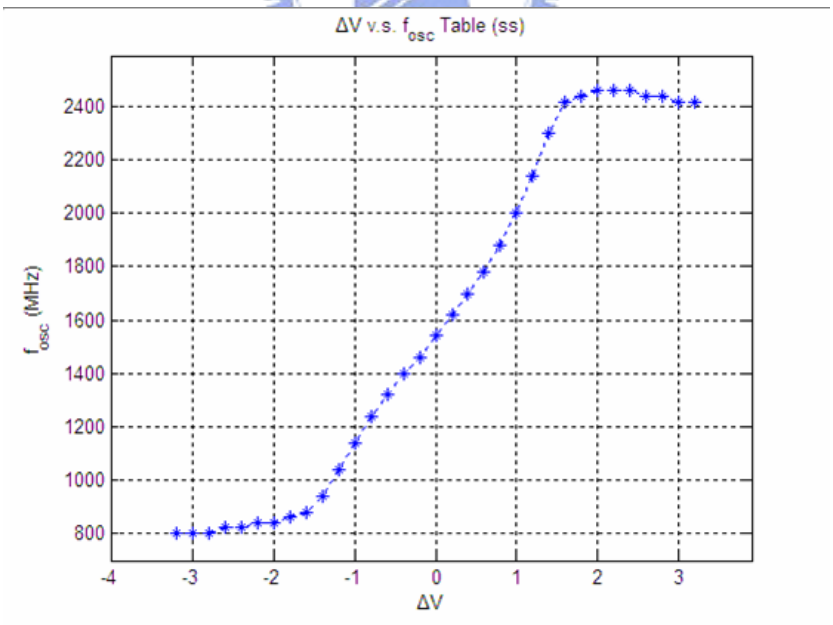


Figure 3.20: Relationship between f_{OSC} and ΔV (SS corner)

3.5 Fully Differential Charge Pump/Loop Filter

3.5.1 Theory and Implementation of Fully Differential Charge Pump

The conventional charge-pump PLL is usually implemented as a single-ended control voltage. The control voltage often suffers the noise coupled from the reference clock shown in Figure 3.21. The reference spurs affects the oscillation frequency of VCO directly. In practice, we hope that the jitter of the PLL only relates to VCO itself. The other phase noise sources must be constrained as well as possible. The differential technique provides a reference spurs-free on the control voltage of VCO. However, the differential-to-single converter or the differential control VCO is needed to collocate the differential control voltage.

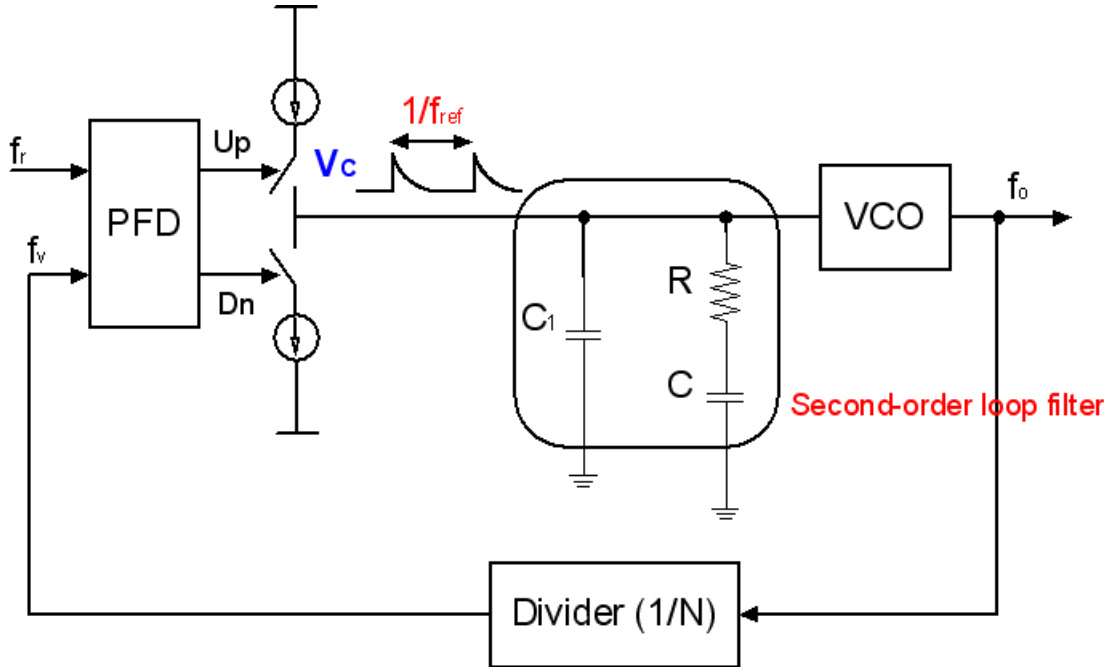


Figure 3.21: Reference spurs occurs on the control voltage

The charge pump and the loop filter provide a conversion between the phase error and the control voltage of VCO. The differential control voltage is used in this thesis, so the charge pump must generate a differential control signal to the loop filter. The fully differential charge pump implemented in [19] is shown in Figure 3.22. The coming Up and Dn pulses from the PFD control two independent current steering pairs, Q1/Q2

and Q3/Q4, whose output current are summed at the load resistors R. A -2R negative-resistance cell cancels out the pull-up resistors to increase the dc gain during differential operation. The negative-resistance cell is implemented with a cross-coupled differential pair. When Up and Dn signals are both low state, the charge pump is a tri-state mode where ideally no current flows in or out of the loop filter. Thus, the loop filter holds the VCO control voltage constant during this time. When Up and Dn are different states, the loop filter is charged or discharged. The explanatory chart of [19] is shown in Figure 3.23. Note that the common-mode voltage of output control voltages is approximately equal to $VDD - I_{CP}R$.

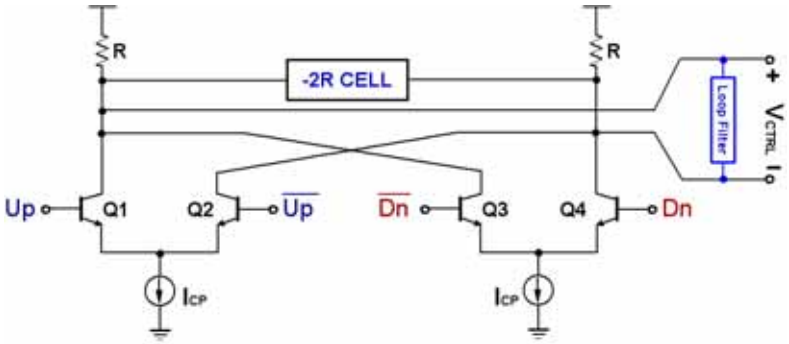


Figure 3.22: Fully differential charge pump [19]

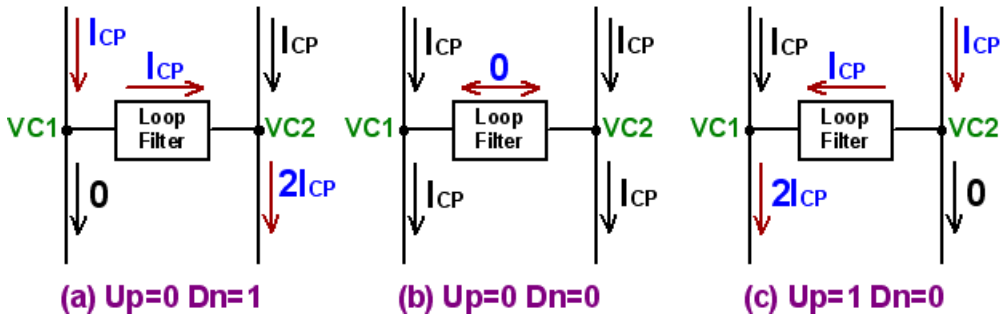


Figure 3.23: Explanation chart of circuit in Figure 3.22

The proposed fully differential charge pump in this thesis is shown in the Figure 3.24. The circuit could be sub-divide into three part elements: the symmetric charge pump pair which is composed of pump-up, pump-down circuits and weak pull-up circuits, wide-swing current mirrors, and the common-mode feedback circuit. The most

difference between [19] and the proposed one is that when Up and Dn signals are both low state, the proposed charge pump has no current on the path A to D shown in Figure 3.24. However, the common-mode feedback circuit is required due to the voltage is unknown while Up and Dn signals are both low state. In order to accomplish the control voltage to the maximum range, the common-mode voltage must cooperate with the VCO. The explanatory chart of the propused pully differential charge pump is shown in Figure 3.25.

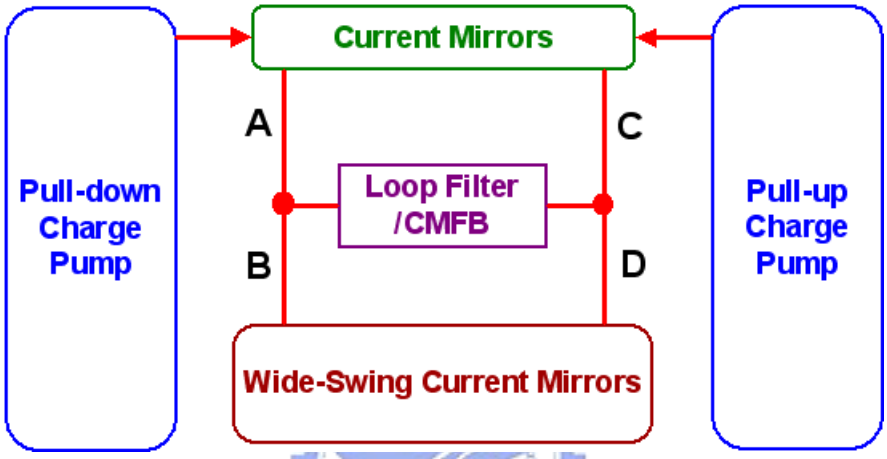


Figure 3.24: The proposed fully differential charge pump circuit

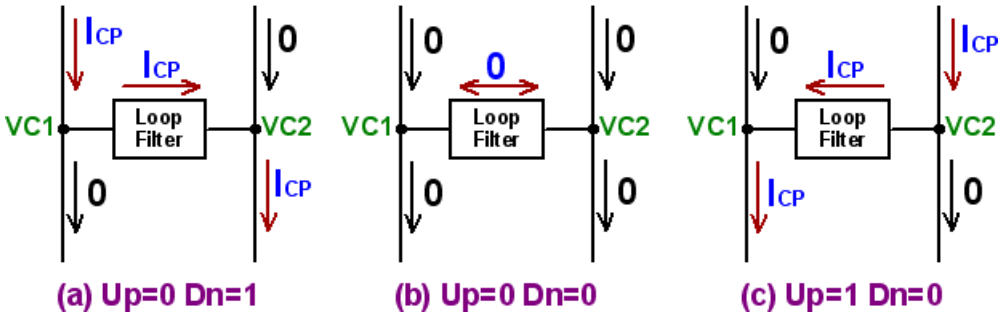


Figure 3.25: Explanatory chart of the proposed fully differential charge pump

The pump-up charge pump circuit is shown in the Figure 3.26. Either pump-up or pump-down circuits [23] consists of a differential input pair M1-M2, current mirror load M3, dummy current mirror load M4, bias current sources I_B and I_{small}, and weak pull-up current mirror M5-M6. The symmetric charge pump inputs are driven by PFD. The

pump-up circuit receives the differential input signals from PFD to control the production of charge current. On the other hand, the pump-down circuit controls the production of the discharge current. When Up^+ is high, the bias current I_B is steered through M1. The differential between I_B and I_{small} flows through M3 and is mirrored to M7. When Up^+ is low, the current in M3 begins to go to zero. If the charge pump circuit has no weak pull-up circuit M5-M6, there will be a long time-constant conducted current in the transistor M3 that we don't have well-controlled. To overcome this problem, the weak pull-up circuit M5-M6 and I_{small} are inserted. Thus, when Up^+ is low, M5 mirrors Ismall to M6 and M6 pulls up the gate of M3 to VDD so that M3 could be turned off within a short period of time. Therefore, we can quickly shut off the current source M7. This technique avoids the transient current occurred due to too longer switching time and restrains the glitches.

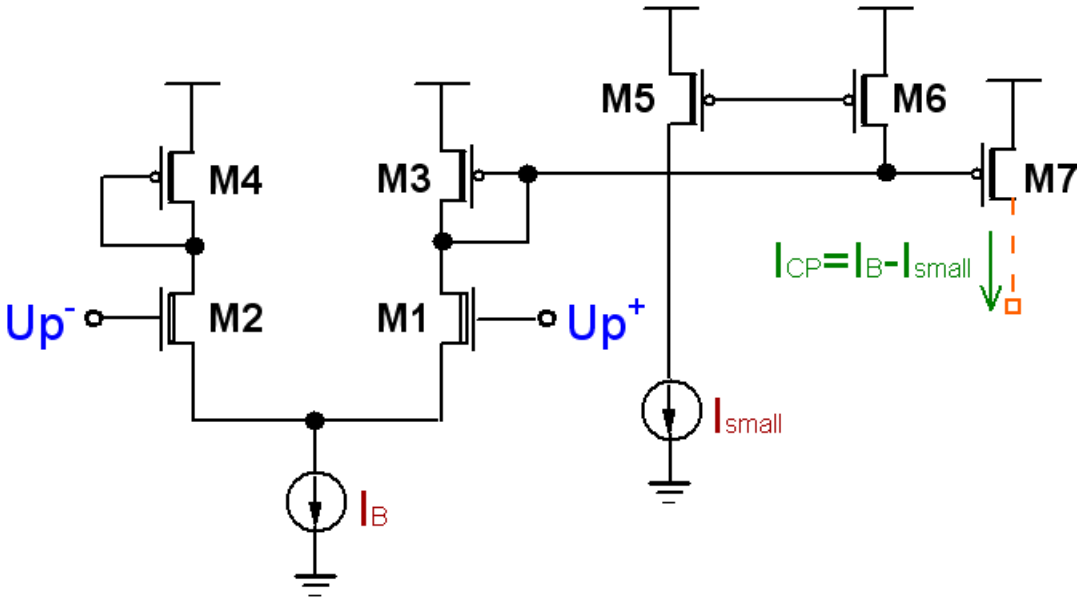


Figure 3.26: Pull-up charge pump circuit

However, the output control voltage are the differential type, so the symmetric loop filter are needed. Figure 3.27 shows a symmetric second-order filter.

The common-mode feedback (CMFB) circuit is shown in Figure 3.28 [22]. The CMFB block sets the dc level and counteracts common-mode noise variations on the differential lines of the floating loop filter. It consists of p-type and n-type sub-circuits. If the common-mode component of VC1 and VC2 goes up, the current in N transistors increases, which in turn discharges the two line similarly and pulls down their voltage level.

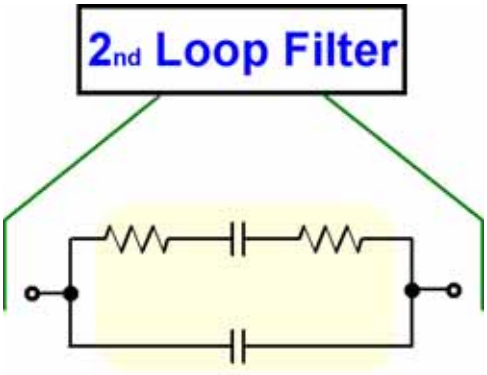


Figure 3.27: Symmetric second-order filter

If the common-mode component of VC1 and VC2 goes down, the P transistors counteract accordingly to pull up the voltage levels of the two lines. The operation of the CMFB defines the dc levels on VC1 and VC2 and prevents transients from creating steady-state components on parasitic line capacitors. The differential signal (VC1-VC2) controls the oscillation frequency of the VCO without converters. Differential signals larger than normal linear operating range can affect the bias points in the CMFB and cause nonlinearities and large transients in the PLL. To avoid such situation at start-up, an auxiliary reset circuit discharges the loop filter capacitor, creating an initial condition VC1-VC2=0.

It must be known that the CMFB circuit could not restrict the output swing of the charge pump. However, the maximum output swing are ranged between V_{THN} and $VDD - |V_{THP}|$. The body potential of the transistors MP1/MP2 are connected to the respectively source to improve the output swing slightly.

The wide-swing current mirror circuit is shown in Figure 3.29. It mirrors the pump-down current to charge node VC1. Using this structure, we can accurately mirror the pump-down current. To design the current mirror, it's important not to make M3-M4 go into triode region. The reason for including M2 is to decrease the drain-source voltage and lower the channel-length modulation effect of M4 so that it is matched to the drain-source voltage of M3. Therefore, the output current I_{out} is more accurately match the input current I_{in}.

To determine the bias voltages for this circuit, set the effective gate-source voltage of M3 and M4 be V_{eff} and assume all of the drain currents are equal [24].

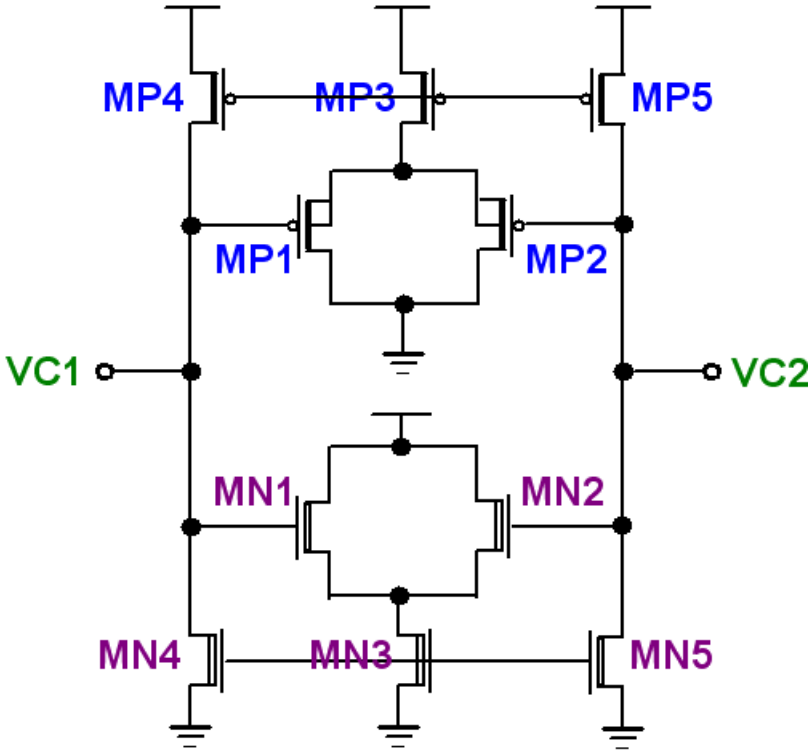


Figure 3.28: Common-mode feedback circuit

$$V_{eff} = V_{eff2} = V_{eff3} = \sqrt{\frac{2I_{D2}}{\mu_n c_{ox}(W/L)_2}} \tag{3.3}$$

Furthermore, let M5 has the same drain current equal to the others but its size is $(\alpha+1)^2$ times smaller than M3(4), then we have

$$V_{eff5} = (\alpha+1)V_{eff} \tag{3.4}$$

Similarly, the effective gate-source voltages of M1 and M2 are given by

$$V_{eff1(2)} = \alpha V_{eff} \tag{3.5}$$

Thus,

$$V_{G5} = V_{G1(2)} = (\alpha{+}1)V_{eff} + V_{TN} \tag{3.6}$$

$$V_{DS3(4)} = V_{G5} - V_{GS1} = V_{G5} - (\alpha V_{eff} + V_{TN}) = V_{eff} \tag{3.7}$$

To ensure both of M3 and M4 maintain in the saturation region right at the edge of the triode region, the minimum allowable output voltage should be

$$V_{OUT} > V_{eff1} + V_{eff3} = (\alpha + 1)V_{eff} \tag{3.8}$$

In practice, we adjust the M1 and M2 to have longer gate length to help eliminate the short-channel effects, but the gate lengths of M3 and M4 are chosen just a little larger than the minimum allowable gate length which is 0.35μm.

Since there may be errors during the fabrication process, the wide-swing current mirror doesn't accurately mirror the pump-up and pump-down current during an operation of Up^+ and Dn^+ being high simultaneously. To take the above situation into consideration, we avoid Up^+ and Dn^+ signals of PFD to be high at the same time. Thus, the three-state PFD is used in this thesis to avoid the above situation occur.

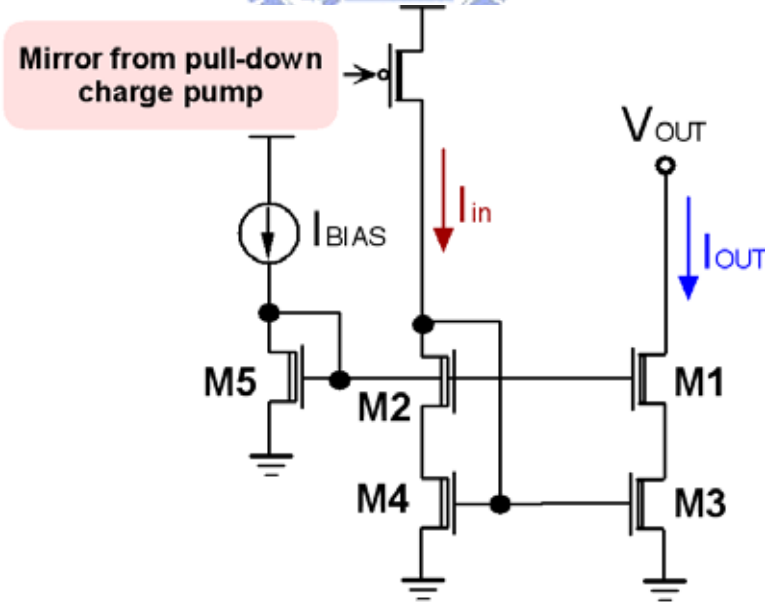


Figure 3.29: Wide-swing current mirror circuit

3.5.2 Simulation Results

Figure 3.30 shows the differential control waveform of the proposed charge pump while the phase error, $\theta_e = \theta_{ref} - \theta_{fb}$, is given and fixed (positive or negative). As shown in Figure 3.30, the maximum output swing range reaches to almost ± 2.4V. However, the useful range among ± 1.5V is chosen in order to ensure the linearity between the charge current I_{CP} and Δ_V. The output swing range in [19] is limited by the static current I_{CP}. The linear swing-range is approximately ± 0.5V when VDD is applied to 3.3V.

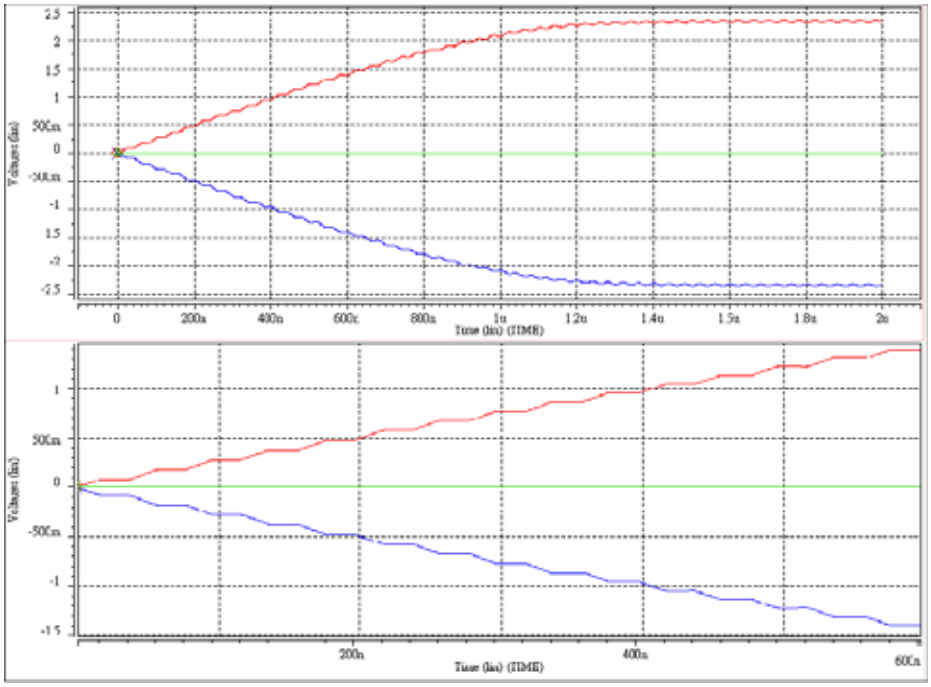


Figure 3.30: ΔV=VC1-VC2 versus θ_e

The CMFB circuit shown in Figure 3.28 sets the common mode voltage between VC1 and VC2. As described in the previous section, either VC1 or VC2 is charged, the CMFB circuit tries to keep the common-mode voltage invariable. This phenomenon makes the output swing wider compared to [19]. Figure 3.31 illustrates the control outputs VC1 and VC2 while the loop filter is charged. The initial common-mode voltage is set to VDD/2. VC1 and VC2 vary with the different trends due to the CMFB actives. Although the common-mode voltage doesn't keep constant due to the different mobilities between NMOS and PMOS, the CMFB circuit relaxes the rising rate of the common-mode voltage and makes the control voltage ΔV wider. The common-mode voltage variation is shown

in Figure 3.32.

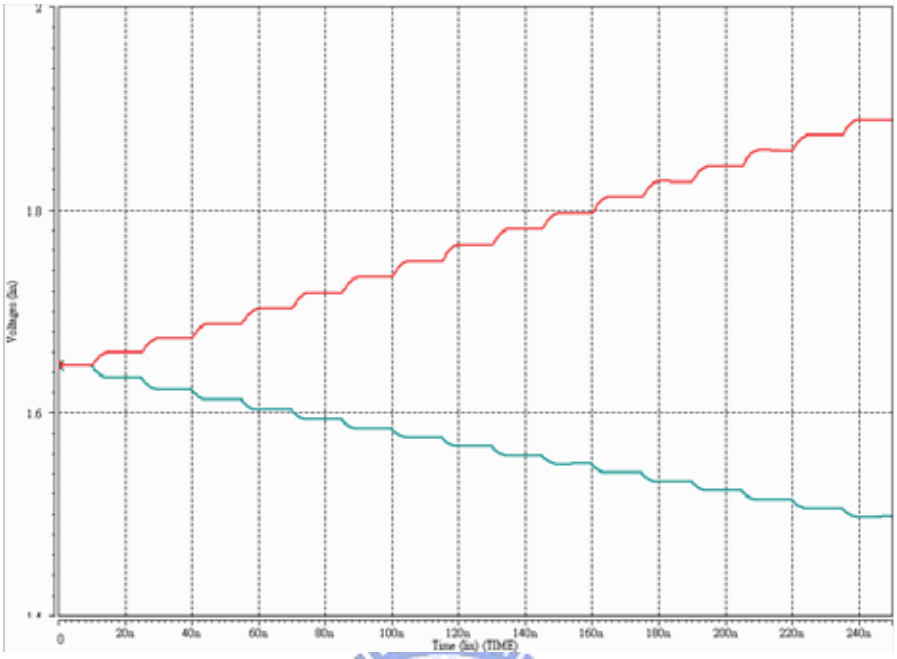


Figure 3.31: CMFB keeps the common-mode voltage fixed

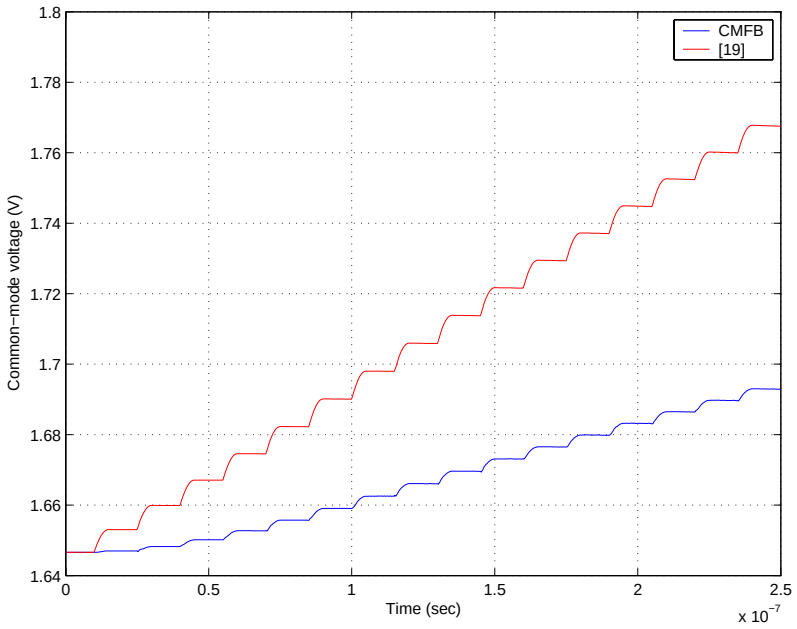


Figure 3.32: Common-mode voltage variation

The matches between charge and discharge current is important for the PLL. It af-

fects the parameter values of the loop filter discussed in next section. Figure 3.33 shows the average charge and discharge currents versus the different phase errors. The resulting curve is quite linear both phase lead or lag. There just occurs a little difference between the average charge and discharge currents. The maximum current difference occurs at $\phi_{err} = \pi/4$ is only 1.7nA shown in Figure 3.34. Figure 3.34 also indicates that the current mirrored from the wide-swing current mirror and the original current are matching exactly.

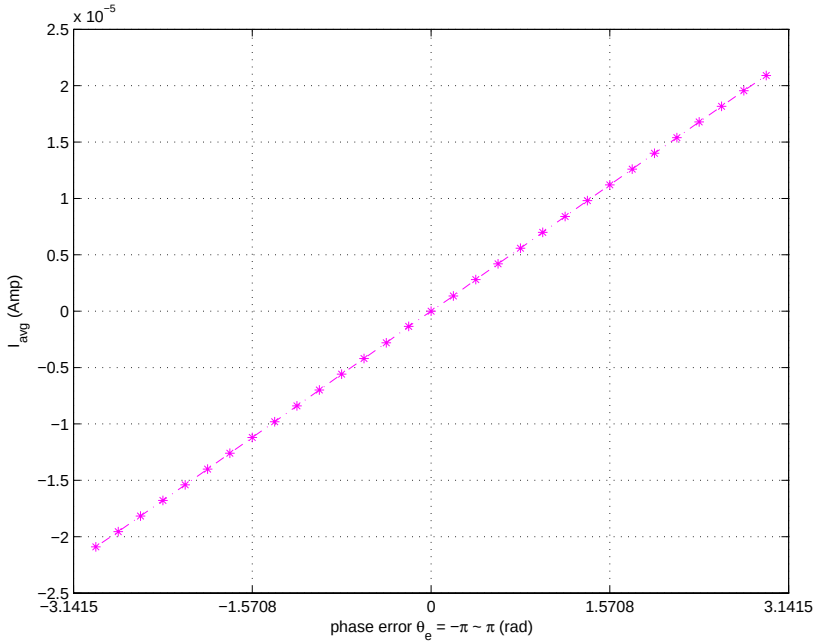


Figure 3.33: I_{avg} versus ϕ_e

The proposed fully differential charge pump could effectively restrain the reference spur. Figure 3.35 and 3.36 show the Fourier series plot without DC components respectively. As the resulting plots, the reference spurs (25MHz) dominate the variation at each control voltage node. However, the differential technique reduce the reference frequency component from 33dB to -66dB without normalized.

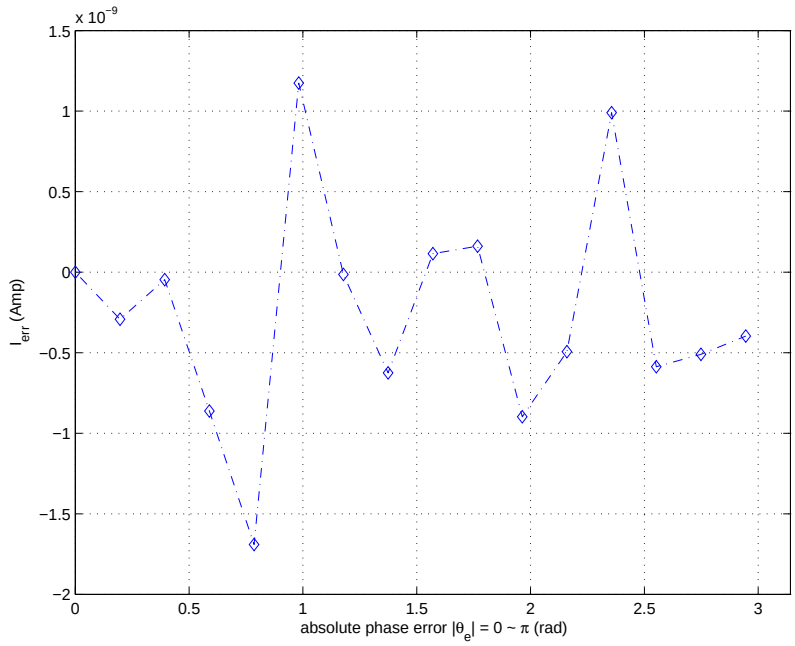


Figure 3.34: Common-mode voltage variation

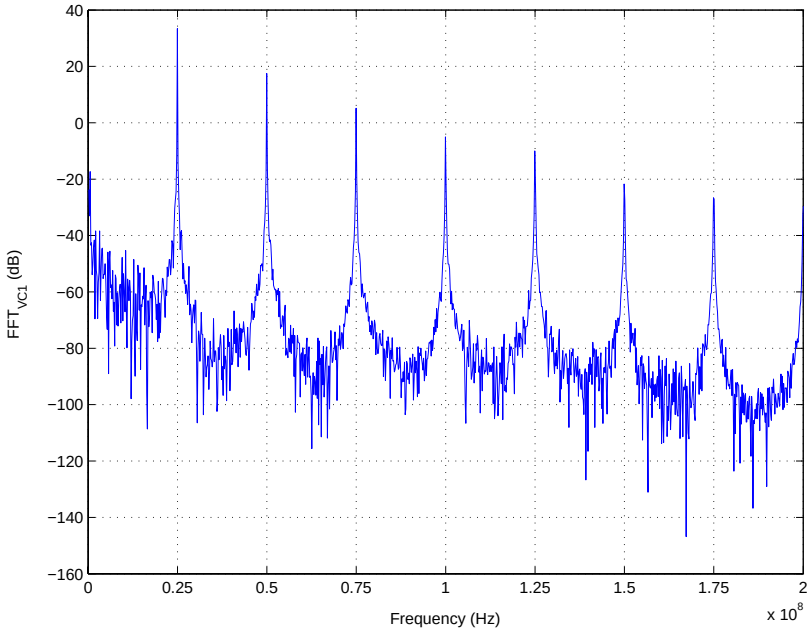


Figure 3.35: Fourier series plot of single-side control voltage

3.6 Component Parameters Decision of Loop Filter

The loop filter used in the frequency synthesizer either restrains the high frequency noise or reduce the modulation effects of the spurs from VCO. Besides, the loop filter af-

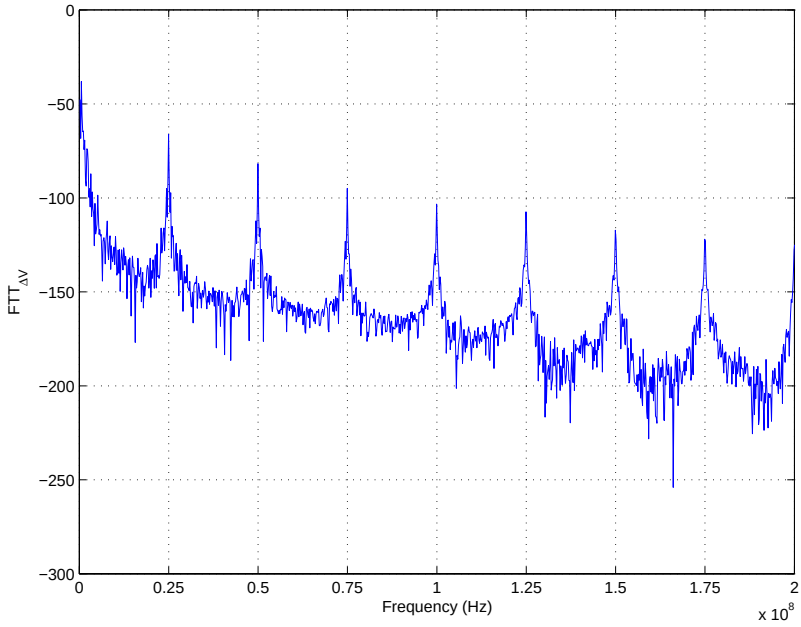


Figure 3.36: Fourier series plot of the differential control voltage

fects the transient response of the frequency synthesizer for the whole loop. For instance, the trade-off between the loop bandwidth, settling time, and the immunity of noise are the specifications varied by the loop filter. Consider a PLL linear model shown in the Figure 3.37. We set the output current of the charge pump is equal to I_{CP}. The charge or discharge time to the load capacitor in a period is equal to $T(\theta_e/2\pi)$, where θ_e is the difference between θ_{ref} and θ_{div}. Thus, the average output current of the charge pump is given by

$$I_{avg} = I_{CP}(\theta_e/2\pi) \tag{3.9}$$

We define a constant value K_ϕ given as

$$K_\phi = I_{avg}/\theta_e = I_{CP}/2\pi \tag{3.10}$$

The open-loop gain of the PLL linear model is

$$G(s)H(s) = \frac{\theta_i}{\theta_o} = \frac{I_{CP}Z(s)K_{VCO}}{Ns} \tag{3.11}$$

Where Z(s) is the transfer function of the loop filter

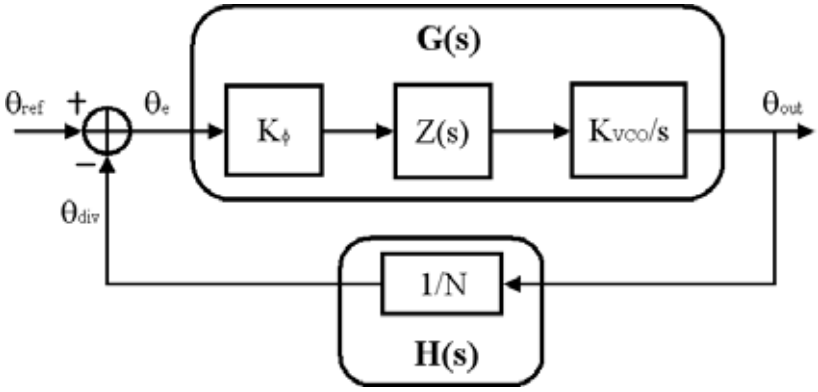


Figure 3.37: A PLL linear model

Suppose that Z(s) is the first order loop filter whose transfer function is given by

$$Z_{1st}(s) = R_p + \frac{1}{sC_p} \tag{3.12}$$

Replacing $Z_{1st}(s)$ into the equation (3.11), we have

$$G(s)H(s) \mid_{1st} = \frac{sI_{CP}K_{VCO}R_pC_p + I_{CP}K_{VCO}}{s^2C_pN} \tag{3.13}$$

Plotting the Bode plot with MATLAB is shown in Figure 3.38. The resistor R_p series to the capacitor Cp would improve the stability in the loop.

The transfer function of the second order loop filter applied to the system is

$$Z_{2nd}(s) = (R_p + \frac{1}{sC_p})//\frac{1}{sC_2} \tag{3.14}$$

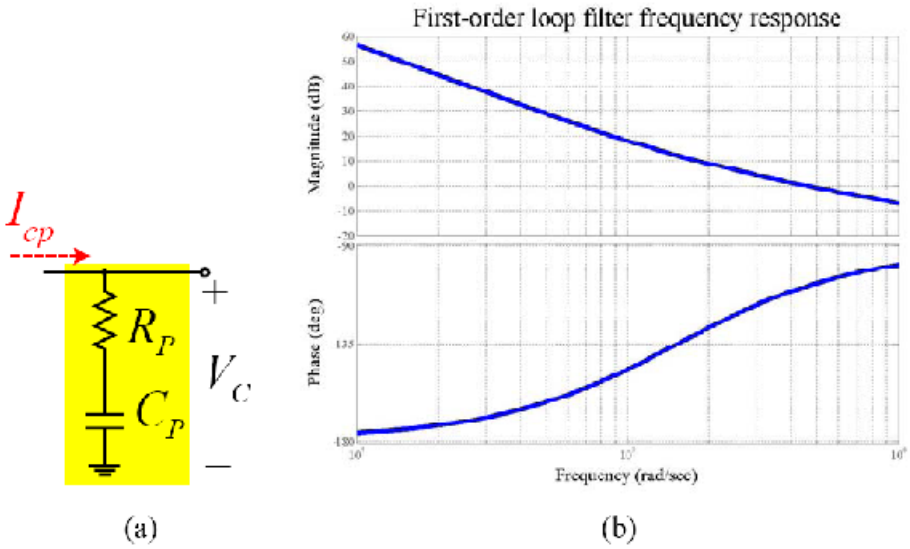


Figure 3.38: First order loop filter (a) Schematic (b) Open-loop frequency response

Replacing $Z_{2nd}(s)$ into equation (3.11), we have

$$G(s)H(s) \mid_{2nd} = \frac{sICPK_{VCO}R_pC_p + I_{CP}K_{VCO}}{s^3C_2C_pR_pN + s^2N(C_2 + C_p)} \tag{3.15}$$

Plotting the Bode plot with MATLAB is shown in Figure 3.39. The advantage of the second order loop filter compared to the first one is that the effective control voltage range of VCO will not be reduced due to the granular effect.

In the second order loop filter design, we define that

$$T_1 = R_p\frac{C_2C_p}{C_2 + C_p} \text{ and } T_2 = C_pR_p \tag{3.16}$$

Let $s = j\omega$, and replacing equation (3.16) into equation (3.15), we have

$$G(s)H(s)|_{s=j\omega} = \frac{I_{CP}V_{VCO}(1 + j\omega T_2)}{-\omega^2C_2N(1 + j\omega T_1)}\frac{T_1}{T_2} \tag{3.17}$$

We can derive the phase margin ϕ_p from equation (3.17)

$$\phi_p = \frac{\omega}{T_2} - \frac{\omega}{T_1} + 180^\circ \tag{3.18}$$

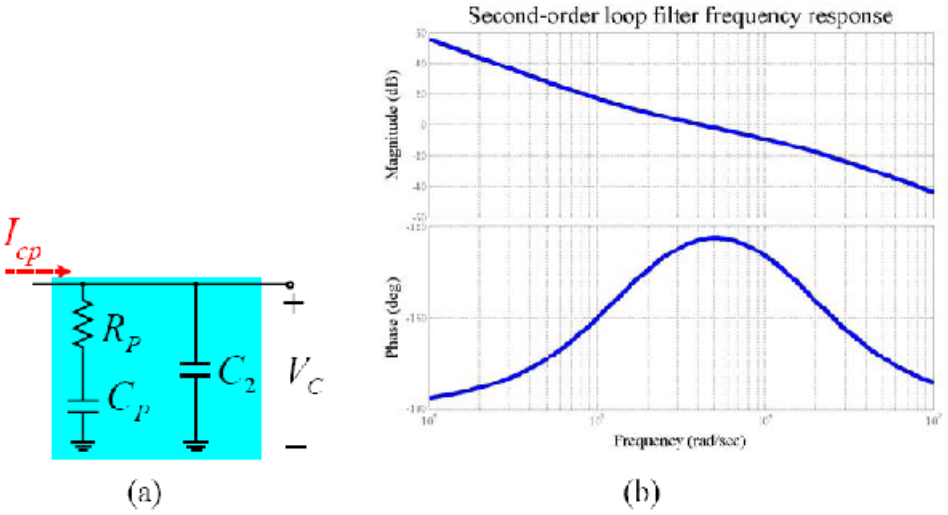


Figure 3.39: Second order loop filter (a) Schematic (b) Open-loop frequency response

The first consideration in designing the loop filter is the stability problem in the loop. While the open-loop gain $|G(j\omega = j\omega_p)H(j\omega = j\omega_p)| = 1$, the phase margin can be obtained from equation (3.18). The differential for ϕ_p is shown in equation (3.20) that stands for the maximum phase margin condition, where ϕ_p is the loop bandwidth of the PLL.

$$\frac{d\phi_p}{d\omega} = \frac{T_2}{1+(\omega T_1)^2} - \frac{T_1}{1+(\omega T_2)^2} = 0 \tag{3.19}$$

$$\omega_p = 1/\sqrt{T_1 T_2} \tag{3.20}$$

While ω_p and ϕ_p are given, we can obtain

$$T_1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \tag{3.21}$$

$$T_2 = \frac{1}{\omega_p^2 T_1} \tag{3.22}$$

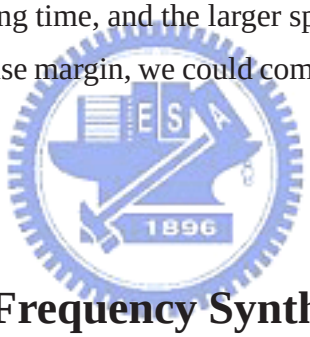
Thus, we obtain

$$C_2 = \frac{I_{CP}K_{VCO}}{\omega_p^2 N}\frac{T_1}{T_2}\sqrt{\frac{1+(\omega T_2)^2}{1+(\omega T_1)^2}} \tag{3.23}$$

$$C_p = C_2(\frac{T_2}{T_1} - 1) \tag{3.24}$$

$$R_p = \frac{T_2}{C_p} \tag{3.25}$$

Thus, we could estimate the component values of the second order loop filter. Note that the loop filter of the frequency synthesizer in this thesis is off-chip. Normally, the loop bandwidth will be set ten times less than the reference frequency of the frequency synthesizer. The wider loop bandwidth causes the shorter settling time, but larger spurs effect and overshooting. In the consideration of the phase margin, the bigger one makes the higher stability, longer settling time, and the larger spurs effect. Determining the suitable loop bandwidth and the phase margin, we could compute the values of the parameters of the loop filter.



3.7 Simulations of Frequency Synthesizer

In this section, we exhibit the PLL characteistic results which are the post simulations. In the simulation, the reference clock is applied to a 25MHz square wave. The reference clock is equal to 24.5535MHz in practice, but the simulation result is hard to observed due to the timing resolution problem in SPICE.

PFD, Divider, VCO, Charge Pump and the common bias circuits are implemented on chip. However, the loop filter is achieved as off-chip type in order to fine-tuning the specifications as described in Chapter 2. The conditions and the parameters of PLL are given as following

VDD=3.3V TEMP=25°C

Reference frequency $f_{ref} = 25$MHz

Stages of Divider $N = 64$

$I_{CP} = 45\mu$A

Tuning Voltage Range: $\pm 1V$ and V_{CM} =VDD/2

$K_{VCO} = 400$MHz/V

Phase margin $\phi_p = 60°$

There are three cases bandwidth considered in this frequency synthesizer. Thus, we could calculate the parameter values of the loop filter as

$$\begin{cases} \omega_n = 200\text{KHz} & \Rightarrow R = 4.7\text{K}\Omega,\ C = 685.6\text{pF},\ C_1 = 56pF \\ \omega_n = 300\text{KHz} & \Rightarrow R = 6.8\text{K}\Omega,\ C = 303\text{pF},\ C_1 = 22pF \\ \omega_n = 400\text{KHz} & \Rightarrow R = 8.2\text{K}\Omega,\ C = 172\text{pF},\ C_1 = 12pF \end{cases}$$

Figure 3.40 shows the transient response of PLL with three different bandwidths. All of three different bandwidth could lock the phase and frequency between V_{ref} and V_{fback}. The larger loop bandwidth fomrs the shorter settling time, but worse jitter performance. However, there is a trade-off between speed and jitter.

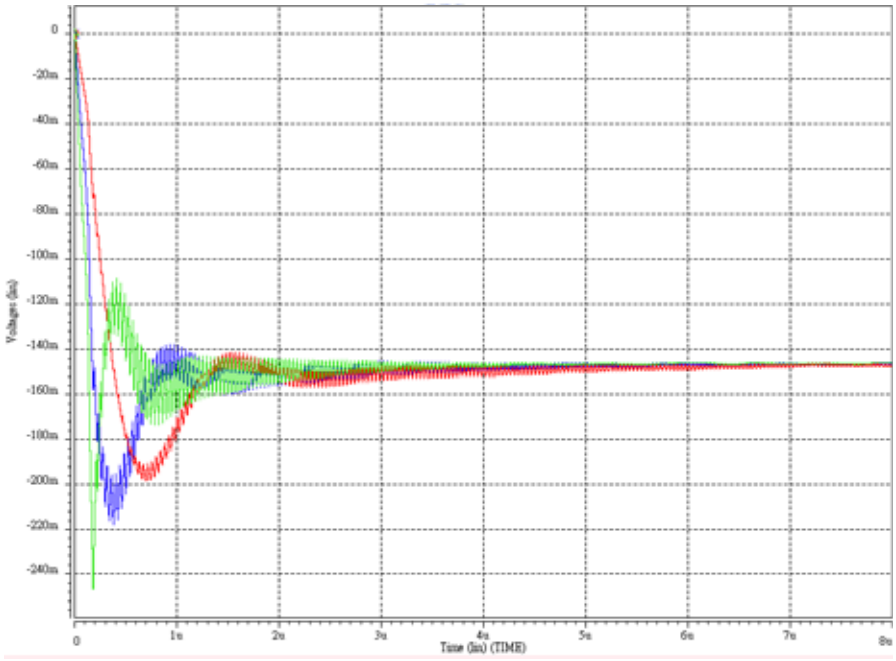


Figure 3.40: Transient Response while ω_n=200, 300, 400KHz

The following simulation result plots are based on ω_n=300KHz. Figure 3.41 shows the eye pattern plot. The calculated peak-to-peak jitter and the jitter$_{rms}$ of VCO output are 22.5ps and 7.2ps respectively. We use the ring type oscillator in order to generate the quadrature output waveforms. However, it is necessary to observe the jitter performance

of the divider output due to measurement considerations. Figure 3.42 shows the eye diagram of the divider output with peak-to-peak jitter is 201.5ps and the jitter$_{rms}$ is 47.8ps.

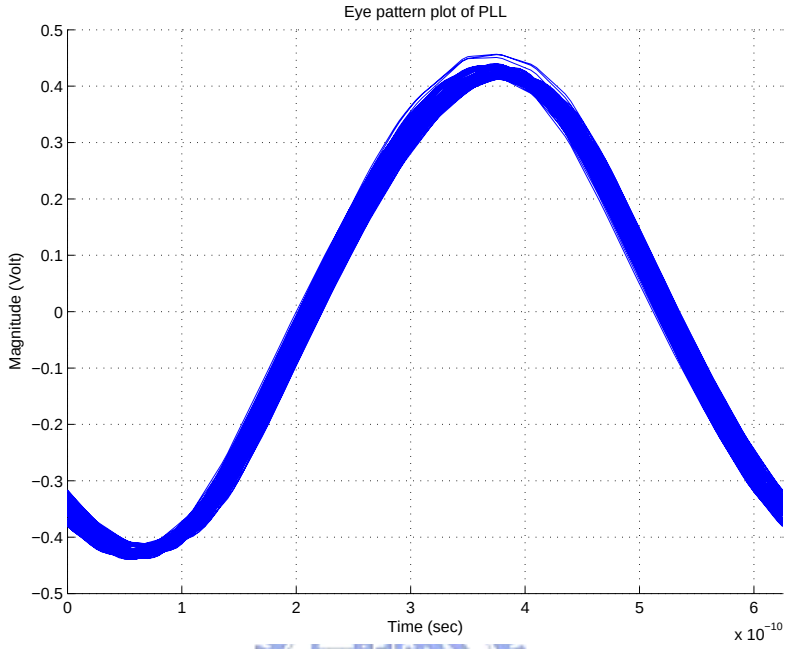


Figure 3.41: Eye pattern plot of PLL

Figure 3.43 shows the layout photo of the proposed frequency synthesizer. The whole chip area including bondpad is 1.008 X 1.008 mm^2. Table 3.1 states the specifications of the frequency synthesizer.

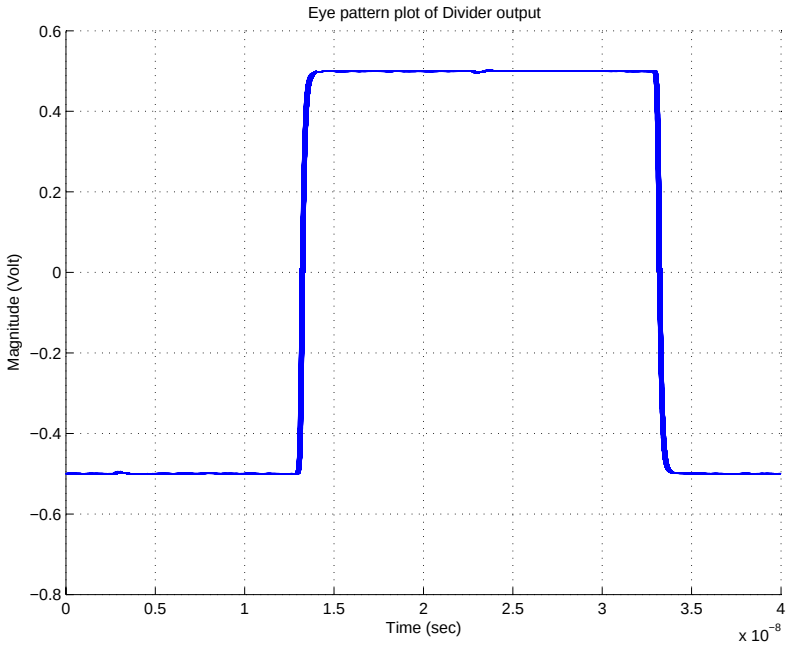


Figure 3.42: Eye pattern plot of Divider output

Items	Result	Unit	Comment
VDD	$3.0 - 3.6$	Volt	
Power dissipation	22	mW	Whole chip
Settling time	4.1	μsec	$\omega_n = 300$KHz
Jitter	22.5	psec	VCO output:peak-to-peak
Jitter	7.2	psec	VCO output:rms
Jitter	201.5	psec	Divider output:peak-to-peak
Jitter	47.8	psec	Divider output:rms
Die area	1.008 X 1.008	mm^2	Whole chip (PAD)
Reference spur	negligible	$-$	Charge pump spec.
Locked-frequency range	$1.2 - 2.0$	GHz	VCO spec.
Tuning-voltage range	± 1.0	Volt	Charge pump spec.

Table 3.1: Specifications of the frequency synthesizer

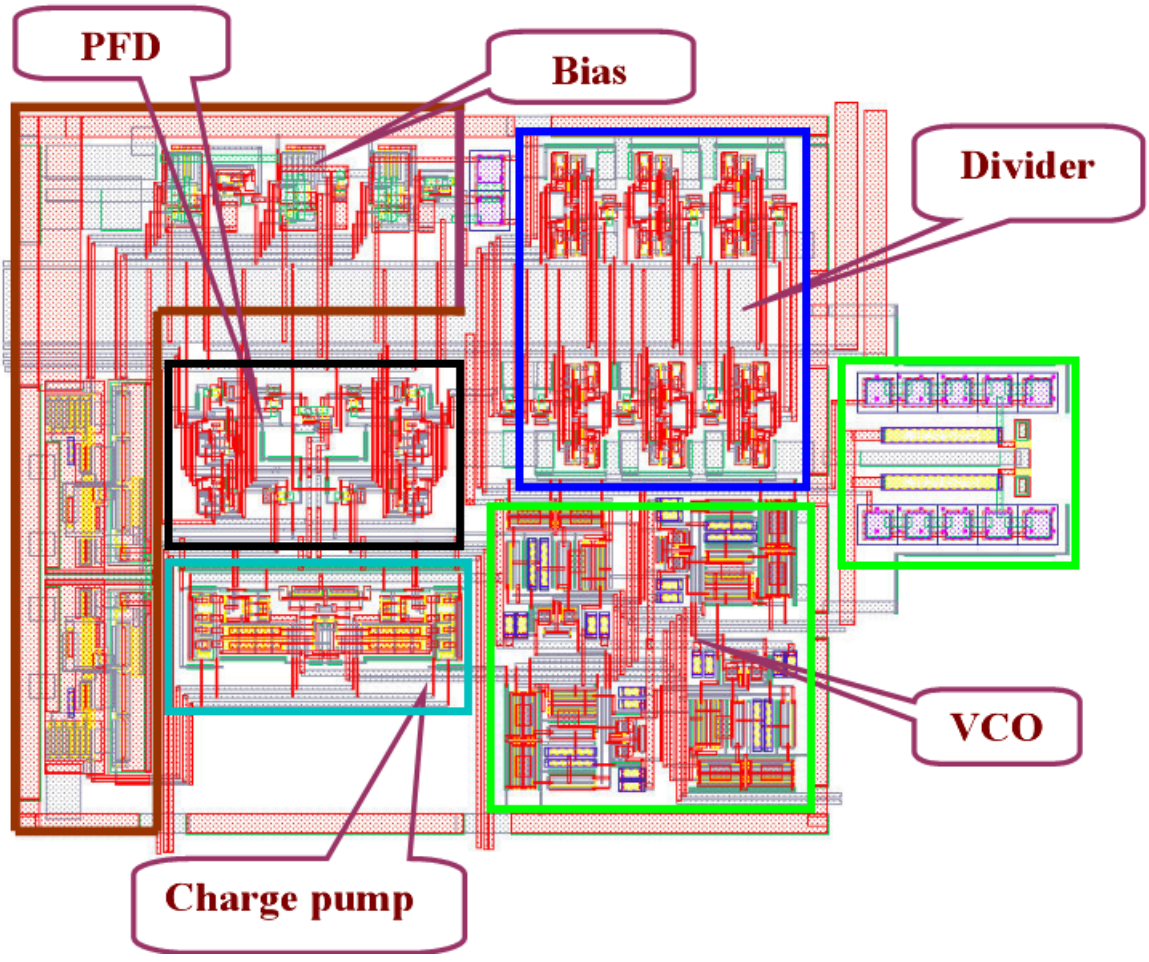


Figure 3.43: Layout photo of the proposed frequency synthesizer

Chapter 4

Conclusion

The fully differential frequency synthesizer is realized and implemented in this thesis. The differential technique provides a way to eliminate the common-mode noise and the reference spurs. A novel differential charge pump is proposed which servos a wider control voltage range, matching charge and discharge currents and lower dynamic power dissipation. The frequency synthesizer dissipates less than 22mW in whole chip including the bias circuits. The peak-to-peak jitter is 22.5ps and the root-mean-square jitter is 7.2ps. The refeurence spurs are effectly cancelled due to the differential properties. The high-linearity control voltage is about $\pm$1V with tunging frequency range 1.2 to 2.0 GHz. Finally, the chip area of the proposed frequency synthesizer is 1.008X1.008mm^2 consisting PADs.

However, the final jitter is not so good since the ring-type oscillator is used. The better way to solve this problem is using LC-tank oscillator with differential control signals. It could be expected to greatly lower the phase noises and spurs effects.

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