國 立 交 通 大 學

電 機 與 控 制 工 程 研 究 所

碩 士 論 文

一個適用於多級類比數位轉換器的嶄新數位背景校正方法

A Novel Digital Background Calibration Scheme for Multistage ADCs

研 究 生：吳孟軒

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中 華 民 國 九十五 年 七 月

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誌謝

在這兩年的研究生生涯中，我學到了很多。我一直覺得我是一個很幸運的人，在每一個階段的學習過程，我都遇到了對我幫助很多的好老師。一樣的，在就讀研究所的階段裡，我依然遇到了一個對我幫助很多，甚至更多的好老師。我要感謝我的指導教授，洪浩喬教授。在每一次我們討論到對於新的方法裡的問題時，他都能以他豐富的經驗與學識提供我一個可行的方向。除了研究的本身，老師也教導了我許多研究所應該要有的態度，這對我幫助很大。並且，老師也常以他的經驗，指導我做人處事的方向。不啻是學術或是人生旅程上，我真的很慶幸能遇到洪老師。

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一個適用於類比數位轉換器的嶄新數位背景校正方法

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摘要

當 CMOS 的製程朝向尺寸越來越小演進時，由於低電壓以及低基本增益的關係，設計類比電路如管線式類比數位轉換器中的殘餘量放大器是一項相當具有挑戰性的工作。信號不再線性的被放大而開始有了失真。因而在本篇論文裡，我們提出了一個嶄新的數位背景校正方法，可以精準的量測與修正殘餘量放大器中的線性與非線性增益誤差。我們所提出的方法 multi-correlation estimation (MCE) technique，利用加入不同振幅的隨機序列，而得以得知有關於誤差的訊息。除此之外，利用此種方法的數位校正電路可以被大幅的簡化。

此外，本篇論文探討了類比數位轉換器被校正過後的精準度與其在校正電路裡校正參數之間的關係，同時建立了一個對於電路實現的設計流程。

應用所提出的方法，模擬結果展示出一個 12-bit 200MSample/s 管線式類比數位轉換器在校正之前 ENOB=6，SNDR=38dB，DNL=2.6/-0.7 LSB，INL=27/-27，校正後的ENOB=11.7，SNDR=72.3，DNL=0.43/-1，INL=0.66/-0.6。 從以上結果可以驗證我們所提出的方法是可行的。

A Novel Digital Background Calibration Scheme for Multistage ADCs

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Abstract

As the trend for the CMOS process scaling continues advancing, the design of analog circuits such as the residue amplifier in the pipelined ADCs has become a much challenging work due to the lowed intrinsic gain and the voltage swing. The signal amplification by the residue amplifier is no longer linear but has distortions. This thesis presents a novel digital background calibration that accurately estimate and correct the linear and the nonlinear gain errors arising from the residue amplifier. The proposed estimation technique, called the multi-correlation estimation (MCE) technique, estimates residue gain errors by injecting random sequence alternatively, allowing extractions of linear and nonlinear gain errors orthogonally. In addition, the circuits enabling background estimation is largely simplified.

This thesis also discusses the relationship between the recovered ADC resolution and the correction parameters associated with the calibration function. Therefore, a design strategy related to the practical implementation as well as the design consideration is built in this thesis.

Employing the proposed scheme, the simulation result shows that a 12-bit 200 MSample/s pipelined ADC before calibration only has an effective number of bit (ENOB) of 6 bits, an SNDR of 38.4 dB, a DNL of $2.55/-0.75$ LSB, and an INL of $27/-27$ LSB. After calibration, its ENOB and SNDR are improved to be 11.7 bits and 72.3 dB respectively, and its DNL and INL are $0.43/-1$ and 0.66/-0.6 LSB respectively. These results verify the proposed technique does work well.

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Chapter 1

INTRODUCTION

1.1 Motivation

As the fabrication technology continues to scale down, digital circuits have much superiority over analog ones. Digital circuits benefit from the scaled CMOS technology, making them smaller, consuming less power, and capable of operating at high speed. That is, more digital signal processing (DSP) capability is available for the same area at a reduced power consumption. On the other hand, the analog circuits suffer from reduced voltage headroom and intrinsic gain of the scaled devices. Both add design challenges in high-gain feedback loops [10–12]. Meanwhile, the reduced supply voltage limits the usage of traditional gain-enhancement design techniques such as cascode and gain-boosting. It also lowers the ratio of useful signal range, leading to increased power dissipation in the noise-limited circuits to keep the same Signal-to-Noise Ration (SNR).

In modern SoC (System-on-Chip) devices, the analog-to-digital converter (ADC) is a fundamental building block for connecting the real world to the digital processors. The demands for high performance ADCs with high resolution, high speed, and low power keep increasing in various applications such as audio, portable, and telecommunication. High performance ADCs, however, are usually power inefficient and difficult to design using the advanced process. Based on above observations, a new design scenario, digital-assist analog design, is getting more and more popular [3] and digital processing of analog signals has become more attractive [13] in communication systems. Circuit designers now tend to use fast-but-imprecise analog functional blocks, while employing DSP to compensate for the errors due analog circuits. Such ADCs composed of digital calibration circuits therefore have the ability to facilitate compensation in digital domain to sustain their performance even under the scaled technology.

1.2 Overview

This thesis is concerned with improving the ADC performance under scaled process. For this reason, we employ DSP techniques to overcome the analog circuits

limitations, recovering the degraded ADC accuracy.

The multistage ADC, e.g., the pipelined ADC, has been the most popular ADC architecture because of its versatility. Typical applications include audio, video, ultrasound, base station, and telecommunications. Flexible and suitable for a wide range of specification, the pipelined ADC has the potential of achieving high resolution, high speed, and low power. Because of its advantages, the pipelined ADC is used to demonstrate and validate the effectiveness of our scheme described in this thesis.

Among the key building blocks in the pipelined ADC are the residue amplifiers in each stages. In general, we require the residue amplifier providing precise amplification and operating at high speed. Hence, both features need high open-loop gain and large unity-gain bandwidth at the same time. However, large open-loop gain is difficult to realize without sacrificing bandwidth especially using closed-loop topology. With the closed-loop topology, although robust and highly linear, designers inevitably have to make tradeoff between the precision, speed, and power in an ADC design, making a constraint loop.

To break the constraint loop, numerous researches have been proposed to tackle the technology limitation. The main concept of these algorithms lie in using analog or digital circuits for the calibration of the non-ideal analog functions. Those works can be classified into two scenarios:

- Area Redundancy
- Time Redundancy

The area-redundancy scheme uses an additional slow-but-accurate reference ADC to calibrate the main ADC by comparing the digital raw codes of the main ADC to those of the reference one [14, 15]. This reference ADC may be a $\Sigma\Delta$ ADC or a cyclic ADC. The added ADC just for calibration may consume significant area and power; besides, designing such highly linear ADCs is a challenging task especially under reduced supply voltage.

On the contrary, the time-redundancy scheme takes the ADC digital output codes for calibration rather than the comparison results, leading to less hardware overhead and being easy to implement [3, 7, 16]. Such methodology may employ complex digital circuits (to carry out statistical functions) instead of analog ones; therefore, it is more robust and adaptable to the continuing scaled process. The statistical algorithm enables the ADC itself to estimate the analog errors of the residue amplifier so as to digitally compensate them.

Among previous works, two researches that can calibrate linear and nonlinear gain errors of residue amplifiers have been proposed [3,17]. They have the advantages of performing calibration in digital domain and working in background. However, the calibration algorithm in [3] has large dependence on input signal statistics owing to the way that it estimates the analog errors. Some specified residue values must be toggled such that the information of errors can be obtained. This condition is hard to fulfill since information itself cannot be predicted or assumed having specific distribution. Moreover, redundant stages are required to precisely estimate

the error of analog components. In [17], it is only suitable for weakly nonlinear amplifiers due to its calibration mechanism and not easy-to-implement because of using very complex digital calibration circuits.

Faced with these issues and driven by the trends using calibration to improve ADC accuracy while maintaining high speed, this thesis proposes an alternative scheme. The scheme relaxes the design challenges on precise analog circuits by using open-loop amplifiers exhibiting high speed, low power, and low noise that then can be corrected in digital domain. Assisted by the digital circuits, the proposed scheme can adaptively calibrate the linear and nonlinear gain errors introduced by the residue amplifiers while performed in background without interrupting the normal conversion. In particular, incorporated with statistical functions, it is featured in that the quantization noise of backend ADC does not affect the system identification process as compared with [3, 18]. Therefore, the linearization parameters for the calibration of the ADC can be obtained through an unaffected identification process. In addition, calibrations of multistage ADCs using conventional precision feedback amplifiers is available owing to the characteristics described in the scheme.

A 12-bit 200 MSample/s pipelined ADC with open-loop amplifiers design example using MATLAB [19] is used to demonstrate the effectiveness of the proposed scheme. The simulation results show that before calibration, the pipelined ADC only has an effective number of bit (ENOB) of 6 bits, an SNDR of 38.4 dB, a DNL of 2.55/-0.75 LSB, and an INL of 26.5/−26.4 LSB. After calibration, its ENOB, SNDR, DNL, and INL are improved to be 11.7 bits, 72.3 dB, 0.43/-1 LSB, and 0.66/-0.6 LSB respectively.

1.3 Chapter Organization

This thesis is divided into nine chapters. Chapter 2 reviews the fundamentals of pipelined ADC.

Chapter 3 discusses the error sources relating to pipelined ADCs and the error models for further analysis.

Chapter 4 reviews previously proposed calibration techniques while giving analysis on their applications and limitations in depth.

Chapter 5 describes a digital correction mechanism that assists the proposed estimation technique described in chapter 6 and 7.

Chapter 6 and 7 aim at giving comprehension of the proposed digital background calibration scheme with its implementations and design considerations.

Chapter 8 gives the simulation results that validate the proposed concepts. From the simulation results, we have shown a great improvement on the ADC performance: a nearly ideal digital output is possible even extremely nonlinear stages are used in the front-end stages.

Chapter 9 gives the summary and presents suggestions for future researches.

Chapter 2

PIPELINED ADC OVERVIEW

Resolving engineering issues needs a thorough understanding to the question itself, which helps the engineers find more elegant solutions to the problem and save the design period. This chapter introduces the basis of the pipelined ADC and aims at giving a straightforward insight into the ADC architecture, prepared for the topics in depth of the following chapters. Sec. 2.1 introduces the basic principles of the operation and the structure. Sec. 2.2 describes a technique, digital error correction, that is commonly used in pipelined ADCs to relax the requirement on accurate comparators in the sub-ADC.

2.1 Fundamentals of Pipelined ADC

A pipelined ADC is featured in performing a multi-step amplitude quantization as indicated by Fig. 2.1. Shown in Fig. 2.2 is a pipelined ADC with its conventional transfer function in the stage 2, where V_2 is a function of stage's input voltage V_1. In this stage, it resolves two bits at a time and therefore has four segments in its transfer function. A general pipelined ADC cascades plural similar stages in which each stage resolves a few bits at a time. Within each stage, the analog input signal is first sampled and held. Then, a sub-ADC resolves the held analog signal into a coarse n-bit output. After that, a sub-DAC converts the coarse digital output back to an analog level that is being subtracted from the original input signal, yielding the quantization error. This quantization error is then restored to the original full-scale range by the residue amplifier. As a result, the locally amplified quantization, usually called residue, is further quantized by the remanding stages to resolve each n-bit respectively. Finally, the digital output is obtained by the recombination of digital raw codes of each stages. Hence, the digital output is expressed as

$$D_{out} = D_1 + \frac{D_2}{G_1} + \frac{D_3}{G_1 G_2} + \ldots + \frac{D_N}{G_1 \ldots G_{N-1}}, \tag{2.1}$$

where D_i and G_i are the digital raw codes and the gain of the residue amplifier within each stage, respectively, and N is the ADC resolution. Accordingly, higher resolution can be achieved by cascading more stages with the penalty of about linearly growing area. The number of bits that each stage can resolve depends on the

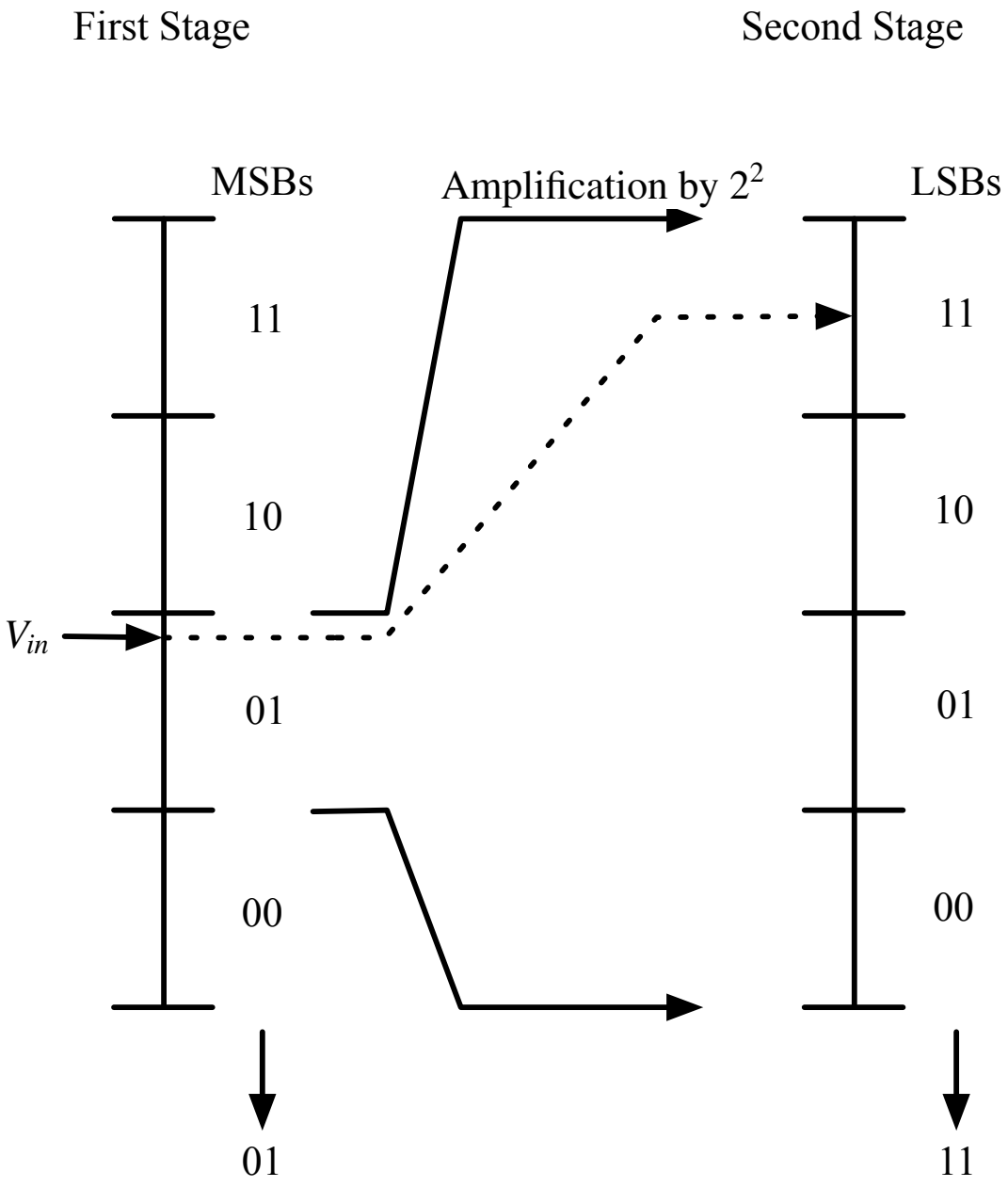

Figure 2.1: Example of the multi-step amplitude quantization.

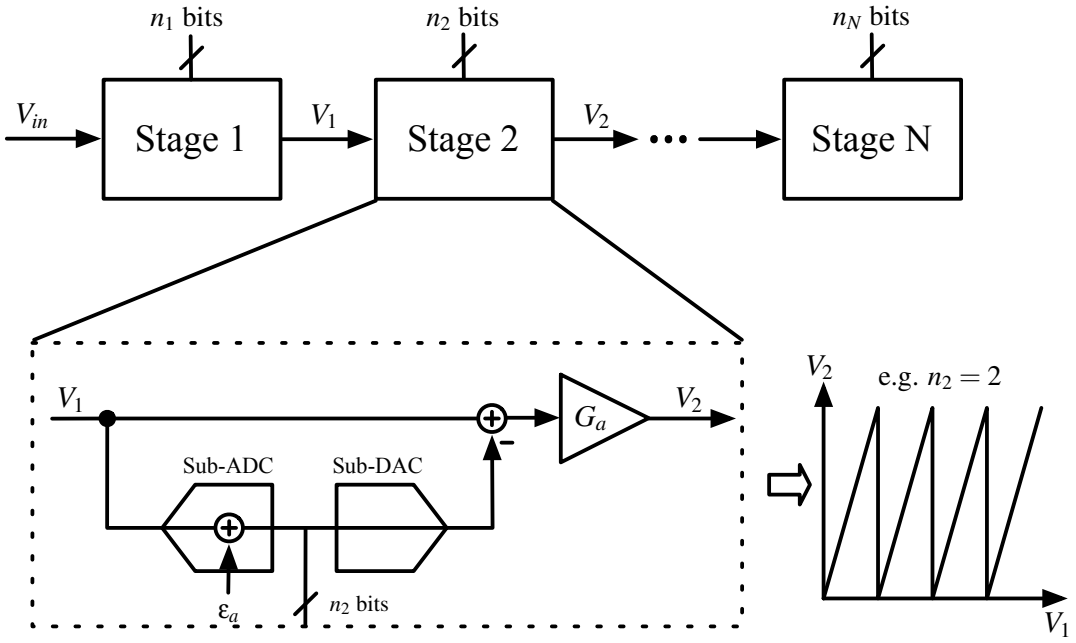

Figure 2.2: Pipelilned ADC diagram [1].

applications. For instance, with conventional architecture, high speed specification favors the architecture with a low number of bits per stage because the interstage gain is lowered, allowing high speed operation due to the fundamental unity-gain bandwidth trade-off of the residue amplifier. On the contrary, low speed, high resolution tends to favor higher number of bits per stage. A detailed analysis can be found in [20].

The concept of the pipeline architecture comes from the digital signal processing. This configuration trades the process latency with the throughput with the aid of inherent sample-and-hold function [21]. Also, since each stage resolves a few bits at a time, this approach increases the throughput and reduces the number of the comparators compared to the flash architecture.

Several attributes of the pipelined ADC architecture can be observed from the introduction above. First, the circuit complexity increases about linearly when each additional bit is added. Because of the involvement of the binary search algorithm, the number of comparators roughly grows linearly, while that of the flash ADC grows exponentially. Second, the ADC throughput is as fast as the flash ADC but the pipelined ADC consumes less power provided their resolutions are greater than 6 bits. Finally, the pipelined ADC has a wide range of specifications since the functional blocks within the stage can be implemented with a variety of topologies. Hence, the ADC fulfills the demands on various applications such as radio, video, instrumentation, imaging, and communication systems.

Within the pipelined stages, the presence of the residue amplifier largely relaxes the accuracy requirements of the comparators. That is, the ADC needs no accurate comparators with very small threshold levels as compared with the two-step ADC.

However, since the opamps have to perform precise amplifications, they usually dominate the power dissipation and limit the maximum speed of the ADC in stead of the comparators. This phenomenon has become an emerging issue especially in advanced process on account for the reduced intrinsic gain and supply voltage.

Although a precise comparator with very small threshold levels is not necessarily required, the inherent offset issue is not resolved. To suppress the effect of offsets, a technique in digital domain, called digital error correction (DEC) [21] technique, is commonly used in almost every pipelined ADC. It largely alleviates the ADC sensitivity to the offsets in the sub-ADC, making the high-speed but low accuracy comparators available in the sub-ADC design. The concept of digital error correction will be described in Sec. 2.2

2.2 Digital Error Correction

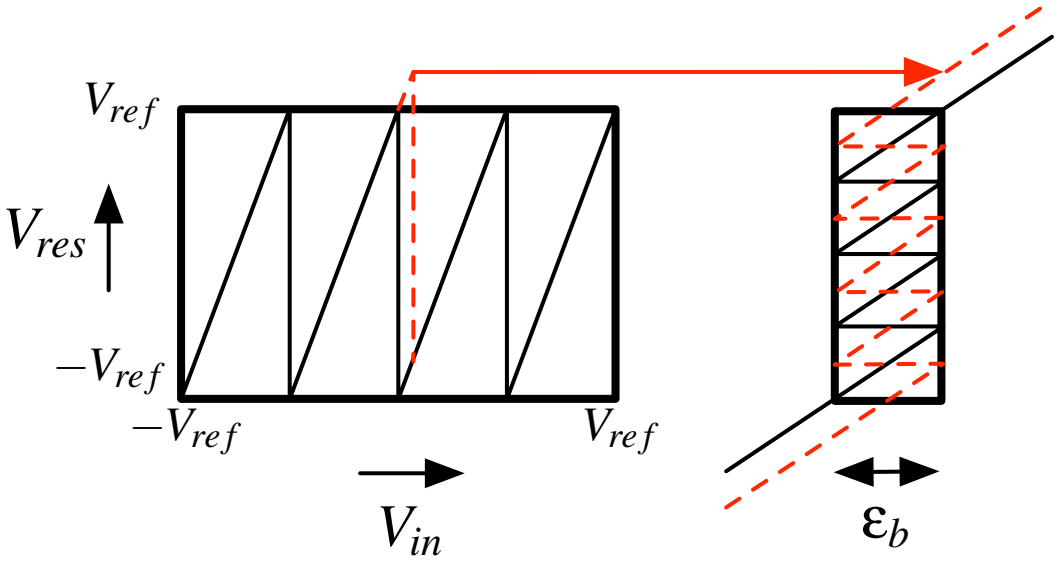

Figure 2.3: Residue plot with sub-ADC offsets.

The digital error correction scheme can tolerate the presence of nonidealities in pipelined ADCs. These nonidealities consists of the offsets of the comparators and opamps, capacitors mismatch, finite opamp gains, and charge injections. They may induce deviations of the transfer curve (dashed line) from the idea one (solid line) as indicated by Fig. 2.3. Thus, the residue may saturate the following stages resulting in missing levels thereby introducing distortion in the spectrum due to the deviation. With the cascaded topology, the errors that saturate next stage's input range can be seen as offsets of the sub-ADC in the next stage. Under this condition, several techniques have been proposed to ease such problem of saturation

by employing digital error corrections. Usual implementations of digital correction schemes include:

- over-range detection, [21]
- reducing residue amplification gain by half. [21–23]

An over-range detection topology detects out-of-range residue signals in the next stage and converts them back to correction bits, which are then added/substracted to the coarse digital output of the previous stage. To make detection, a common approach is to use two extra capacitors in the MDAC or two extra comparators in the sub-ADC of next stage. Fig. 2.4 illustrates this idea.

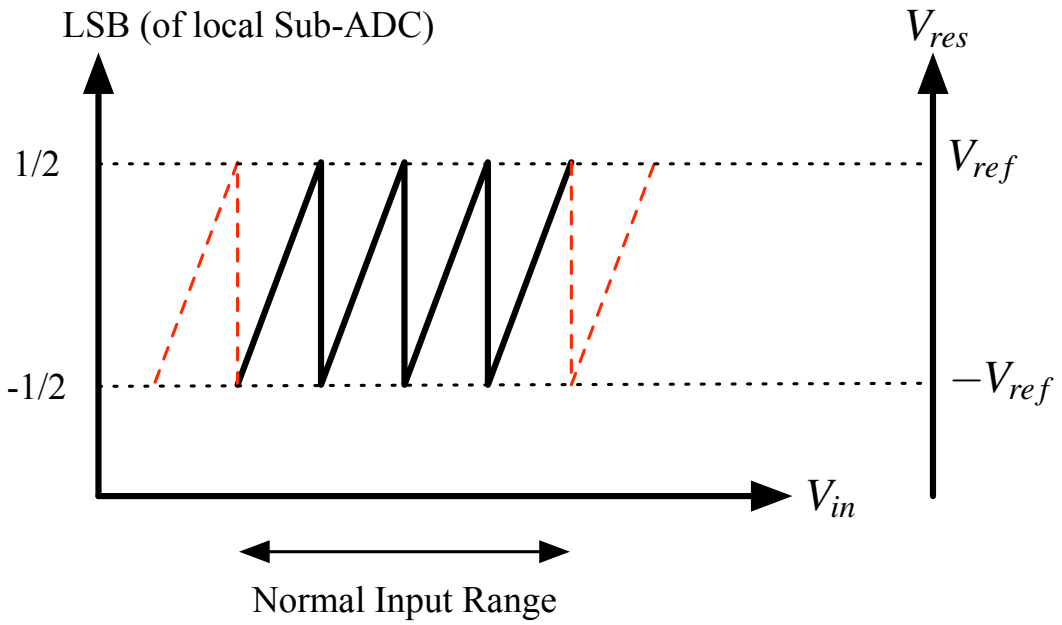

Figure 2.4: Residue plot using extra comparators in next stage.

Compared with the over-range detection scheme, another technique reduces the local stage's gain by half, thereby lowering the next stage's input range. This scheme is commonly used in practical designs. As a result of the lowed output range, large comparator offsets in the local stage can be tolerant as far as they are less than $\pm 1/2$LSB of local sub-ADC's threshold levels. As a result, when the next stage's input falls in the upper/lower half input full-range of next stage, digital error correction is performed by adding/subtracting extra bit to the raw codes of the previous stage. This ideal is shown in Fig. 2.5.

However, both topologies require some encoding logics to recalculate the true digital output. The encoding logic would be greatly simplified if some offsets are added to the transition thresholds of the sub-ADC or sub-DAC. An example of a popular 1.5bit/stage architecture as indicated in Fig. 2.6 demonstrates this concept [2, 24]. Although a single-ended architecture is represented here for simplicity, a

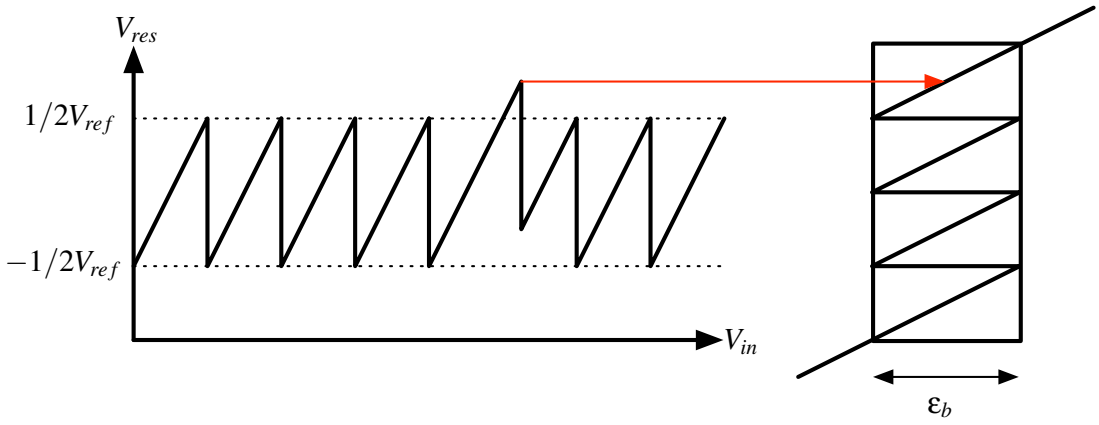

Figure 2.5: Residue plot with reduced half gain.

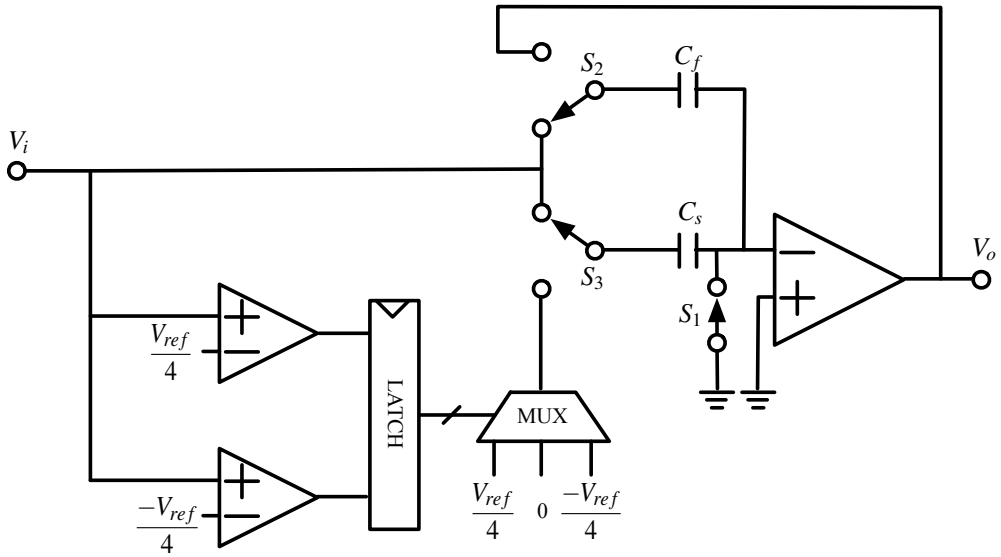

Figure 2.6: Switched-capacitor implementation of a 1.5bit pipline stage [2].

fully differential topology is adopted in many practical designs. In Fig. 2.6, only 2 comparators are needed to resolve 3 levels for a 2bit sub-ADC, while 3 comparators are required for a nominal 2-bit sub-ADC. Thus, the architecture tolerates sub-ADC offsets up to ±1/2LSB in the local stage. As a result, the requirements on precise comparator are greately relaxed. With this concept, the digital output is obtained by shifting bits of each stages and then added together as shown in Fig. 2.7.

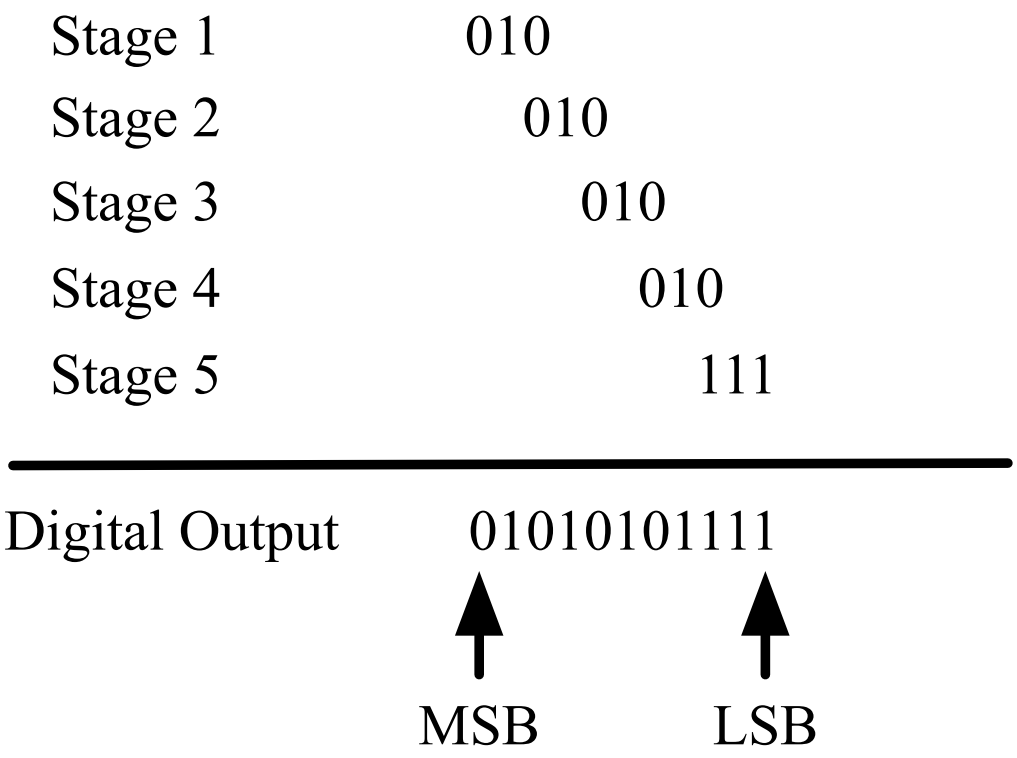

Figure 2.7: Digital output with bit-shifting

Chapter 3

ANALOG ERROR MODELS

This chapter describes the common error sources affecting the performance of the pipelined ADCs and tries to build adequate mathematical models for prior design considerations. First, the error sources commonly encountered in conventional architecture are addressed in Sec. 3.1, 3.2, 3.3, including errors arising from the capacitors mismatch, the residue amplifier.

Then, an alternative residue amplifier approach, i.e., the open-loop residue amplifier topology, is discussed in Sec. 3.4 and demonstrated as a calibrating machine in the proposed calibration scheme in Chapter 6 and 7.

3.1 Introduction

Shown in the Fig. 3.1 is a conventional demonstration-by-concept single-bit/stage architecture intended to be used over Sec. 3.1-3.3 in this chapter. This architecture uses switched-capacitor technique that can be switched between the input, the reference voltages, and ground, realizing the sample-and-hold, DAC, and subtraction functions. It performs two phase operations as following. During the first phase, usually called the sampling phase, the input is connected to the bottom plates of the capacitors while the top plates connected to virtual ground. The charges $Q = (C_s + C_f)V_{in}$ are then stored onto the capacitors. In the second phase, the amplification phase, the bottom plate of C_f is connected to the output of the residue amplifier and that of C_s is connected to positive V_{ref} or negative V_{ref} depending on $D = 1$ or $D = -1$, where D is the local conversion result of the sub-ADC. As a result, total charges of $Q = C_f V_{res} + C_s D V_{ref}$ are stored during that phase. By charge conservation with $C_f = C_s$, the ideal residue transfer function in the amplification phase is given by

$$V_{res} = \begin{cases} (1 + \frac{C_s}{C_f})V_{in} - \frac{C_s}{C_f}V_{ref} = 2V_{in} - V_{ref} & \text{if } V_{in} \geq 0 \quad D = 1 \quad (1)_2 \\ (1 + \frac{C_s}{C_f})V_{in} + \frac{C_s}{C_f}V_{ref} = 2V_{in} + V_{ref} & \text{if } V_{in} < 0 \quad D = -1 \quad (0)_2, \end{cases}$$

therefore we have the ideal transfer curve with ramp input shown in Fig. 3.2.

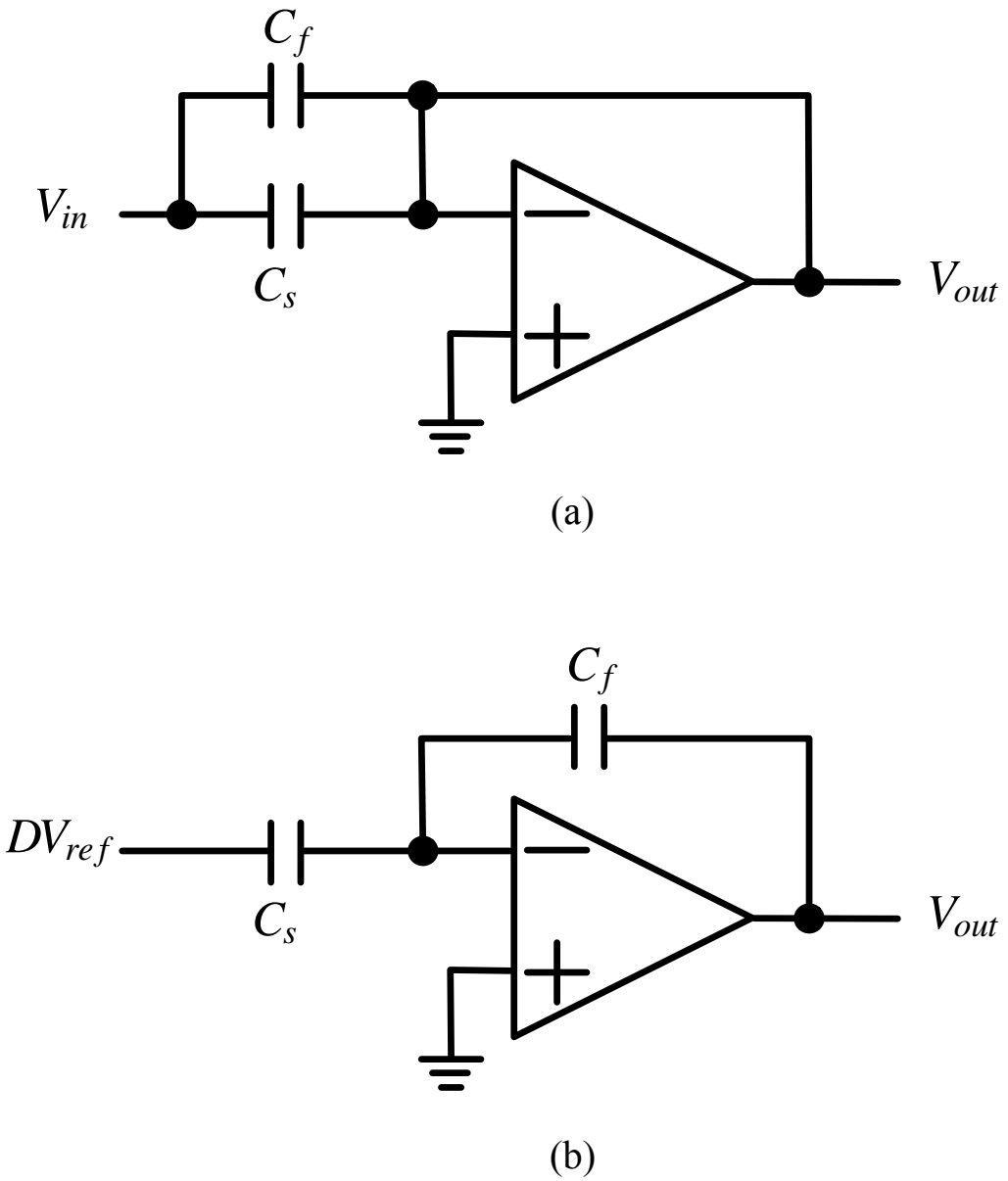

Figure 3.1: Single-bit architecture: (a) sampling phase (b) amplification phase.

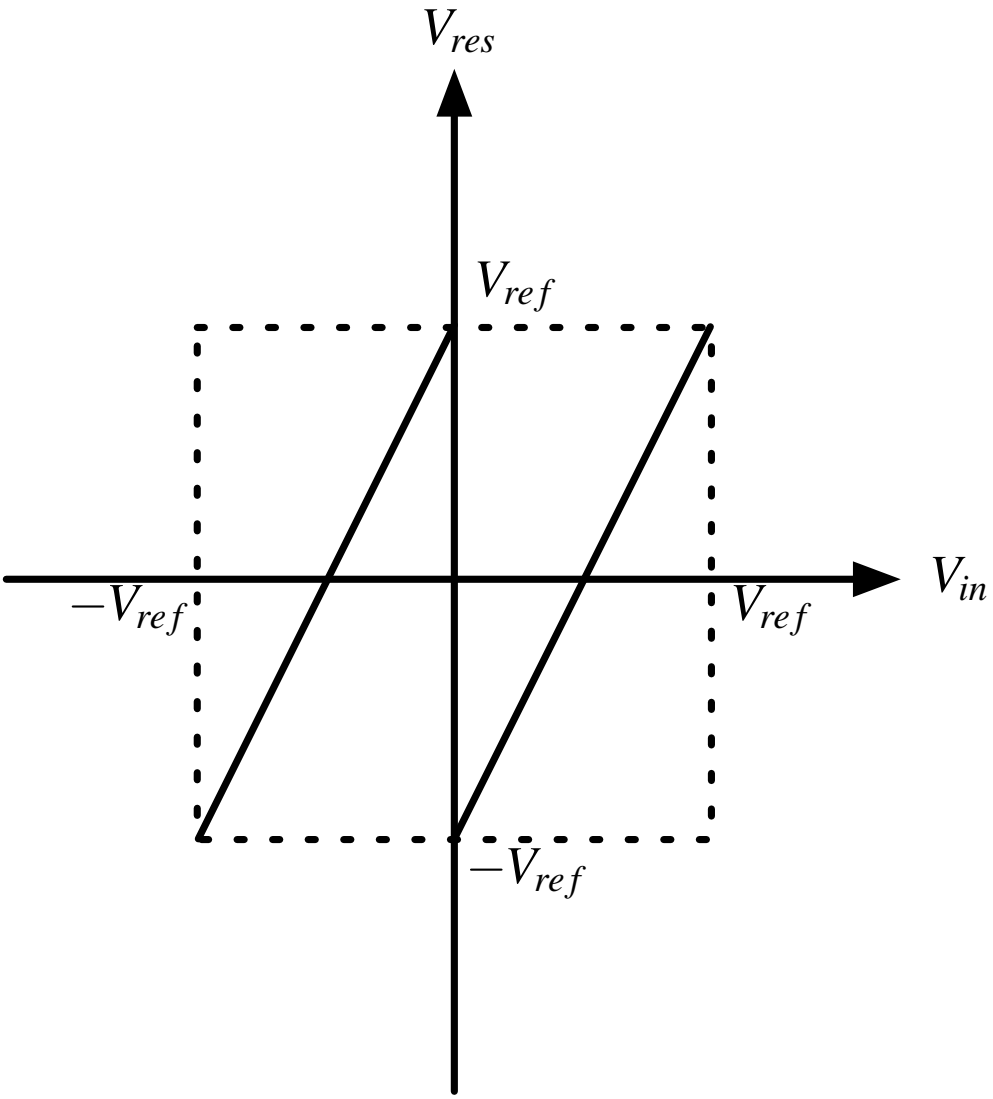

Figure 3.2: Transfer function of single-bit architecture.

3.2 Capacitors Mismatch

Consider the capacitors mismatch only, if $C_s \neq C_f$, an error proportional to the mismatch is generated at the residue output. Defining the difference between the capacitors is ΔC, we have

$$\Delta C = C_s - C_f \tag{3.1}$$

and

$$C = \frac{C_s + C_f}{2}, \tag{3.2}$$

Therefore,

$$C_s = C + \frac{\Delta C}{2}, \tag{3.3}$$

$$C_f = C - \frac{\Delta C}{2}, \tag{3.4}$$

and

$$\frac{C_s}{C_f} = \frac{C + \frac{\Delta C}{2}}{C - \frac{\Delta C}{2}} \approx 1 + \frac{\Delta C}{C}, \tag{3.5}$$

if $\mid \Delta C/C \mid \ll 1$. From (3.5), the transfer function considering the mismatch now becomes

$$V_{res} \approx (2 + \frac{\Delta C}{C})V_{in} \pm (1 + \frac{\Delta C}{C})V_{ref}. \tag{3.6}$$

From (3.6), it is evident the capacitors mismatch result in linear gain error and wrong subtraction of the reference voltages. Both errors are proportional to the difference ΔC provided in the absence of no other circuit imperfections.

Due to the limited fine-line process, the phenomenon of capacitors mismatch mainly stem from variations at the edges of the capacitor plates. Under the statistical manner, capacitors with larger area to perimeter ratios tend to have better matching. However, variations in the oxide thickness between the capacitor plates also affect the matching. This variation is small especially for small, adjacent capacitors. If we only consider the variations of capacitor edges, the standard deviation of the fractional matching error between two adjacent square capacitors can be models as:

$$\sigma_{\Delta C/C} = \frac{A_C}{S}, \tag{3.7}$$

where S is one side of the capacitor in μm. The value of A_C is technology dependent, but can typically vary between $2 - 5\%\mu$m. For instance, if A_C is $5\%\mu$m, then two adjacent, 15μm$\times 15\mu$m capacitors will match to better than 1% with 99.7% probability [2].

3.3 Impairment of Residue Amplifier

Ideally, the residue amplifier produces an output proportional to the input. In practical implementations, the finite open-loop gain and limited unity-gain bandwidth (GBW) make the amplification non-precise or nonlinear. Hence, the finite open-loop

gain and GBW give rise to static and dynamic errors, limiting the ADC achievable resolution and speed as a consequence.

3.3.1 Opamp's Open-Loop Gain

A gain error occurs at the residue signal when the open-loop gain is finite. Assume the actual opamp open-loop gain is A_0, we can derive the transfer function with regard to A_0:

$$V_{res} = (\frac{1}{1+\beta A_0})(2V_{in} \pm V_{ref}), \tag{3.8}$$

where β is the return ratio of the feedback network. Of the feedback network in Fig. 3.1 during the amplification phase, β can be expressed as

$$\beta = \frac{C_f}{C_s + C_f + C_p},$$

where C_p is the parasitic capacitance at the inputs of the opamp.

Taking the first-order Taylor expansion of (3.8), we have the approximation of the transfer function:

$$V_{res} \approx (1 - \frac{1}{\beta A_0})(2V_{in} \pm V_{ref}). \tag{3.9}$$

Observed in (3.9), the relative error $1/\beta A_0$ results in a static error if the residue is fully settled, therefore limiting the ADC resolution. Since β is well-controlled by the capacitor ratios that can achieve about 10-bit in modern technology, high resolution ADCs above 10-bit often require high open-loop gain.

3.3.2 Opamp's Settling

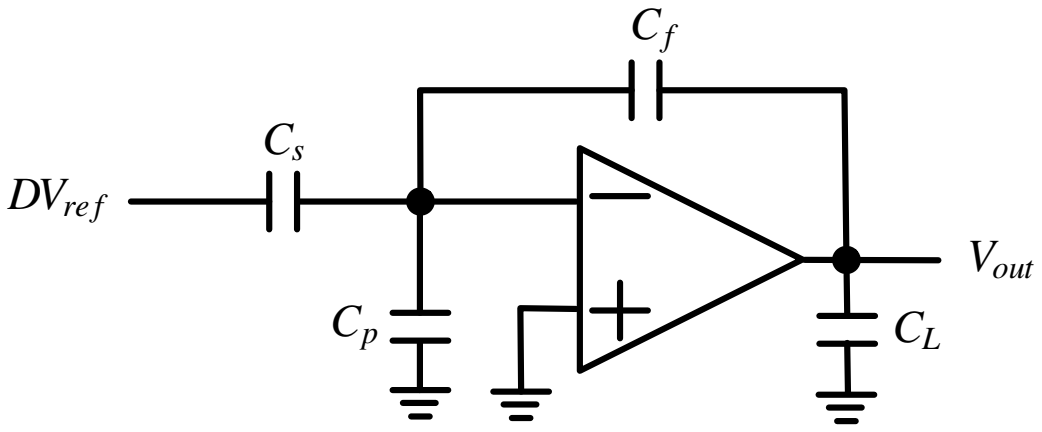

Figure 3.3: MDAC with practical loading during amplification phase.

Because the opamp has finite bandwidth, the output takes time to settle to its final value. As a result, the opamp determines the ADC's speed in most cases. Consider Fig. 3.3, the GBW can be derived as

$$GBW = \frac{g_m}{2\pi[C_L + \frac{C_f(C_s+C_p)}{C_s+C_f+C_p}]}.$$

Hence, the bandwidth (BW) related to the unity-gain bandwidth is obtained by

$$BW = \beta \times GBW = \frac{g_m}{2\pi C_{eff}},$$

where

$$C_{eff} = C_L + C_s + C_p + \frac{C_L(C_s + C_p)}{C_f}.$$

Assume the opamp is a single-pole system with time constant τ, the settling behavior at the end of the amplification phase is given by

$$V_{res} = (1 - \exp^{-t/\tau})(2V_{in} \pm V_{ref}), \tag{3.10}$$

where $|\exp^{-t/\tau}|$ is the relative gain error and $\tau = 1/(2\pi\beta GBW)$.

To make the residue error of the first stage's amplifier tolerable in the following stages, i.e. this error is less than 1/2LSB of the backend ADC, the GBW of the opamp must satisfy the criteria such that

$$GBW > \frac{(N - N_1)\ln(2)}{2\pi\beta(T/2)}, \tag{3.11}$$

where N and N_1 are the resolution of ADC and the first stage accordingly. Therefore, it can be seen GBW will almost increase $2\times$ when each additional bit is added in the first stage. Note that above equations validate when the opamp does not slew.

However, some circuit configurations can hardly meet the condition in (3.11), e.g., the pipelined ADCs with low gain stages [25]. Furthermore, in many applications, slewing is often inevitable under the speed and power constraints. As a consequence, the residue error if slewing occurred now becomes

$$V_{error} = V_{ref} - V_{res}(T/2) = (V_{ref} - \Delta V_{SR}) \exp^{\frac{-T/2-T_{SR}}{\tau}}. \tag{3.12}$$

Given the bias current I_{Bias} of the opamp, we have

$$\Delta V_{SR} = \frac{I_{Bias}}{C_L + \frac{C_f(C_s+C_p)}{C_s+C_f+C_p}} T_{SR}.$$

Fig. 3.4 shows that ΔV_{SR} is linearly proportion to the slewing period T_{SR}.

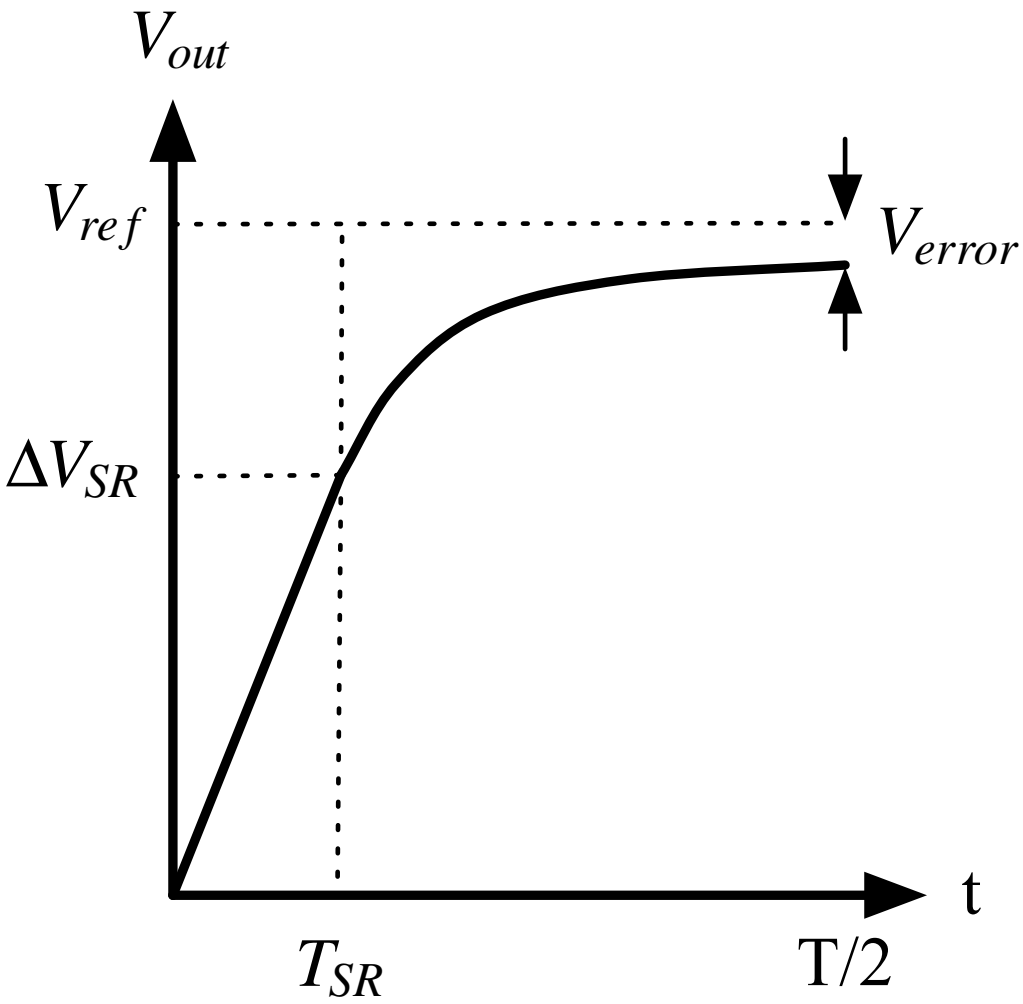

Figure 3.4: Output voltage with slewing during amplification phase.

3.4 Open-Loop Amplifier

3.4.1 Introduction

The function of the opamp in the closed-loop is to provide an output signal proportional to the input. Because feedback topology desensitizes the environment variation, a precise residue amplification is available and the close-loop implementation has been a standard in lots of ADCs. However, an amplifier using open-loop architecture can provide gain in an equivalent manner. Recently, certain ADCs with open-loop structure have shown the availability and capability to achieve both power efficiency and high resolution [3, 26]. Fig. 3.5 shows a conceptual diagram of this kind of topology.

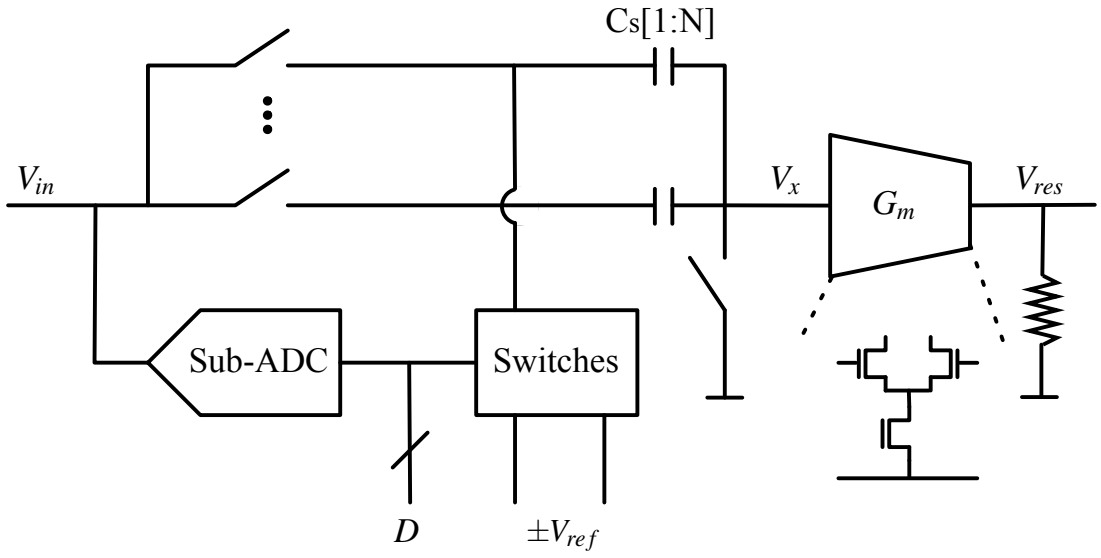

Figure 3.5: ADC with open-loop architecture [3].

The operation of this circuit is similar to the conventional topology except the amplification phase. The charges onto the feedback capacitor are not fed to the output of the residue amplifier, but remained in place to generate a voltage, V_x, at the input of the amplifier. V_x is then amplified to the desired level to be the input of the next stage. With this topology, the demand for high open-loop gain is no longer necessary and the power dissipation drops as well. As a consequence, the amplification function is available using a simple differential pair. These advantageous, however, come at the price of nonlinearities in the signal amplification.

3.4.2 Behavioral Model of the Open-Loop Amplifier

While using open-loop residue amplifiers in pipelined ADCs, the absence of feedback no longer assists desensitizing the environment variations; that is, a linear model is insufficient to describe the amplifier behavior because of increased nonlinearity and

input-dependent amplification. Therefore, a simple but sufficient accurate model is required for prior design considerations.

The nonlinear behavior can be divided into two categories: static and dynamic. Dynamic frequency-dependent distortion, however, becomes significant and dominant when the operating frequency near the dominant pole of the system. Because of a simple differential pair being used as an open-loop amplifier, the assumption of a fully settled system is reasonable for its inherent potential operating at high speed. Thus, the complexity of modeling an open-loop amplifier is quite reduced. Meanwhile, since high performance ADCs often adopt fully differential architecture, this configuration advantages less significant even harmonics. High order harmonics such as fifth or above is negligible with appropriate choice of the overdrive voltage of the input pair of the amplifier according to [3]. If above conditions are satisfied, a simple polynomial model is sufficient to describe the fully differential residue amplifier implementation. As a result, the behavior of the amplifier can be described by a third order polynomial

$$y = a_1 x + a_3 x^3. \tag{3.13}$$

This model is then used in our simulation to validate the effectiveness of our calibration scheme.

Chapter 4

ADC CALIBRATION TECHIQUES

Limited by the process and noise consideration, the resolution of pipelined ADCs without calibration usually may achieve no more than 10 bits. With optimized design and careful layout, some state-of-the-arts ADCs are capable of reaching resolution of 12 bits [27, 28] or above without trimming or calibration. However, to achieve the same performance like these state-of-art ADCs is often paid with large design efforts and periods due to the supply voltage and intrinsic gain constraints as well as the process variations. Therefore, designing high resolution ADCs has become a much challenging work among circuit designers. As a result, many techniques that can calibrate nonlinear errors arising from the inaccurate blocks in the ADC have been proposed in literature [6,18,29–31]. Hence, this chapter gives a brief review of the ADC calibration techniques and relative subjects.

4.1 Introduction

For the past decade, many researches have been proposed to improve the ADC performance and focusing on being compatible with CMOS technology, therefore relaxing the stringent demands on highly linear analog components. Multistage ADCs, e.g. the pipelined ADCs, are well suited for such trends. In the error correction techniques, digital error correction and the use of residue amplifier greatly relax the design of accurate comparators in the sub-ADC and the following stages. However, the ADC linearity is still sensitive to the error arising from the sub-DACs as well as the static and/or dynamic performance of the residue amplifier such as finite dc gain, slew rate, finite GBW, and so on. Hence, a calibration mechanism that is capable of correcting errors arising from the non-perfect MDAC is demanding and promising in recent years. Among the calibration techniques, correcting errors using digital signal processing rather than analog has become an attractive scheme [3, 16, 17, 32, 33]. In these schemes, the analog errors are treated into distortions in the digital domain, therefore we can digitally correct them.

ADC calibrations usually have two steps: error estimation and error correction.

Having understood how bad the ADC is or what/where the error is, we can correct errors according to the estimation results. For example, the digital output of a pipelined ADC is obtained by the recombination of each stage's raw codes. That is, the digital gains must match the analog gains of each stage otherwise the 'noise-leakage' would occur, causing performance loss [34]. Under this condition, if only the linear gain error is concerned, the errors in the digital output is proportional to the difference between the analog and the digital gains. If the accurate estimate of this difference is available, we can adjust the digital gain accordingly, recovering the ADC accuracy.

Based on the error correction/estimation mechanism, the calibration techniques can be categorized into four types: analog/digital and foreground/background calibrations. Foreground calibration techniques estimate the errors when the input is not applied to the converter and then the correction is performed in analog or digital domain; background ones estimate the errors during the normal operation, and then the correction is performed in analog or digital domain. Thanks to the robustness of digital signal processing and their easy-to-implement feature in the CMOS technology, digital background calibrations compare favorably to analog/digital foreground ones. The key concepts of various proposed calibration schemes in literature can be classified into two topologies: area-redundancy and time-redundancy. They will be explained in this chapter in detail.

4.2 Area-Redundancy

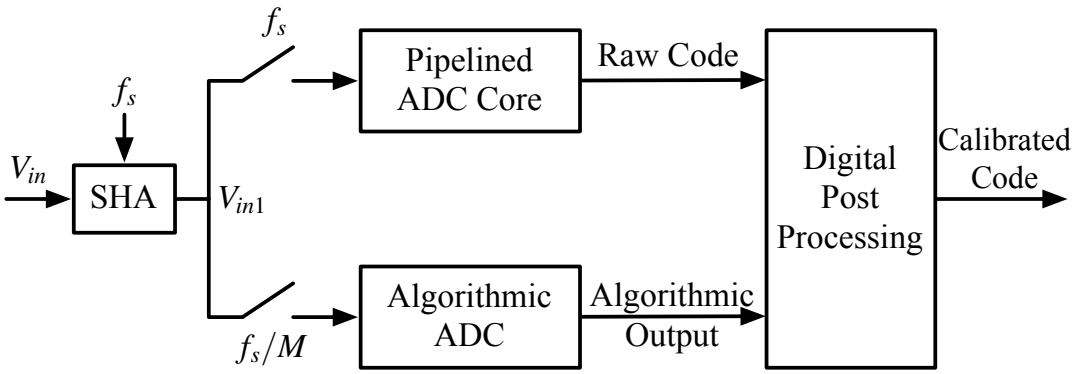

Figure 4.1: Queue-based calibration [4].

An area-redundancy topology uses extra analog circuits such as a slow-but-accurate reference ADC [4, 14, 15], split-ADC architecture [5, 7], or more than one SHA [4, 6], etc., to measure and calibrate the main ADC. In Fig. 4.1, a slow-but-accurate reference ADC takes the same input as the pipelined ADC core and then compares one out of M samples of its output to the corresponding digital output of the ADC core. As a result, the difference between both outputs is used as an information so as to improve the linearity of the main ADC. This scheme has the

advantage of deterministic calibration process since the error information is obtained directly through the outputs instead of statistical manner. Although the reference ADC can achieve very high resolution using a $\Sigma\Delta$ or an algorithmic ADC, the reference ADC usually limits the achievable resolution of the main ADC after calibration. On the other hand, the linearity of the reference ADC is still confined and may not adaptable to the continuing scaled process. Prior calibration of the reference ADC may be necessary before calibrating the main ADC.

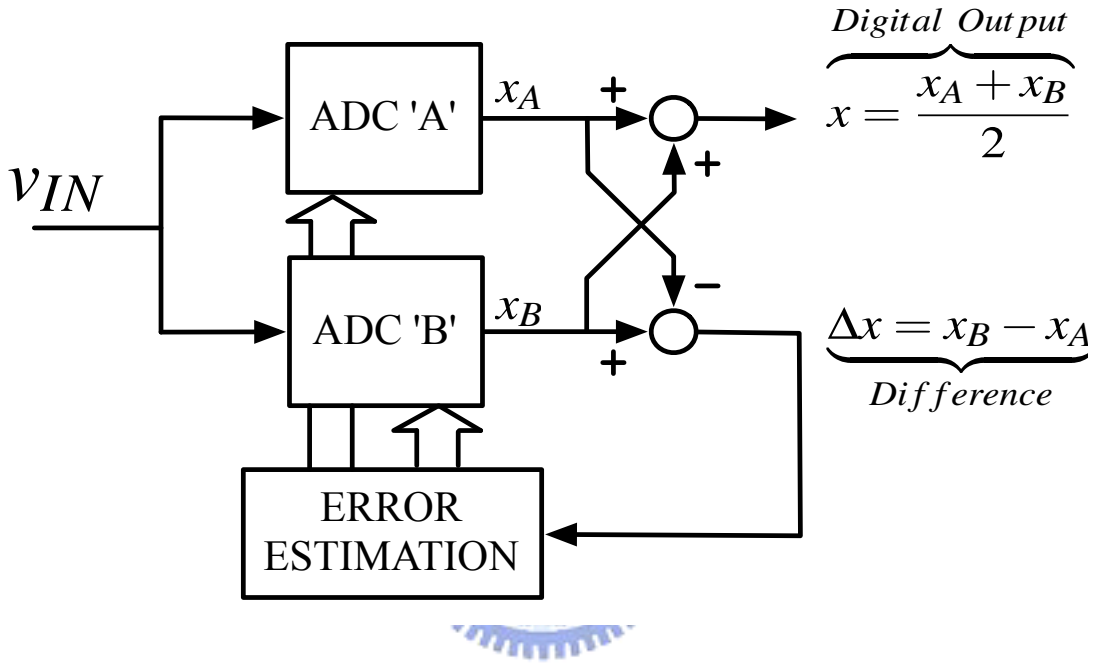

Figure 4.2: "Split ADC" architecture [5].

The split-ADC architecture, as shown in Fig. 4.2, works in the way that the ADC is split into two channels. Each of them takes the same input and produces individual outputs. If both channels are completely calibrated, the average of the individual outputs agrees; otherwise, the difference is served as a calibration signal so as to develop the background calibration. Hence, this technique plays a role analogy to the channel equalization commonly encountered in communications and tries to make the average error power as small as possible. Compared with [3,17,35], this method has the benefit of short calibration time. However, if one of the channels drifts more severe than the other one, the calibration results would be biased, leading to imperfect calibration result.

Shown in Fig. 4.3 is a queue-based architecture [6] with its timing plot illustrated in Fig. 4.4. This architecture uses two or more sample-and-hold circuits in order that some reference signals can be inserted within the same conversion cycle. The inserted signal is then used to calibrate the main ADC due to use of faster clock than the conversion rate. However, the faster clock may lead to large over-design, leading to large area overhead; it is because all the components must be able to operate at the high clock rate rather than the conversion rate. Another drawback

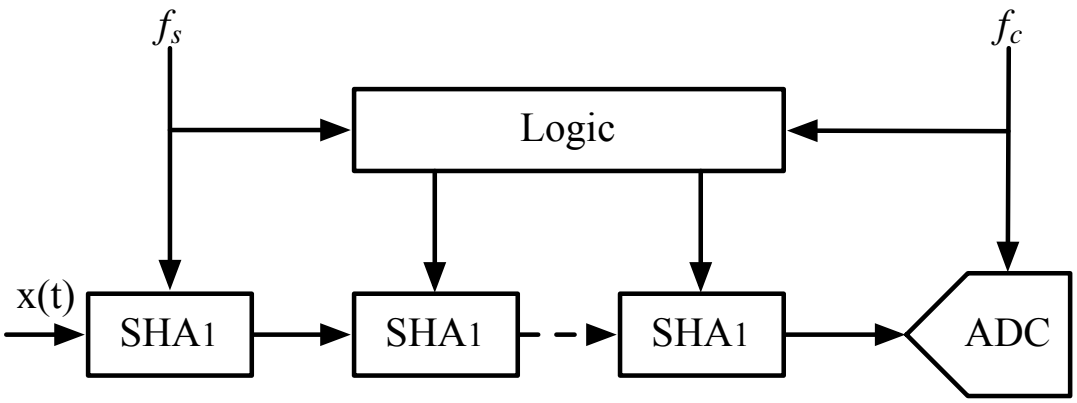

Figure 4.3: Queue-based calibration [6].

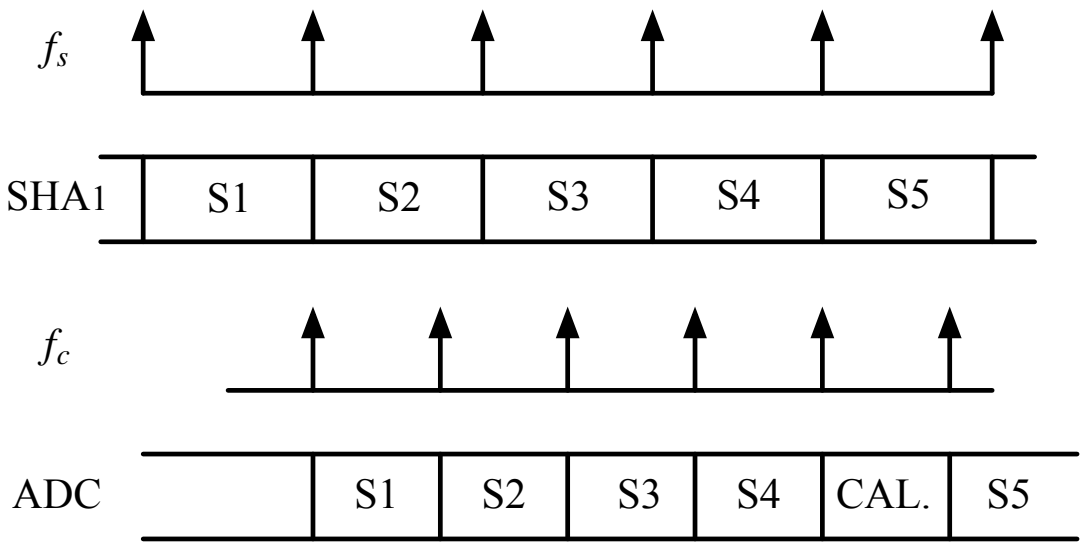

Figure 4.4: Timing scheme [6].

is the limitation on the available acquisition time that is often shorter than half the clock period.

4.3 Time-Redundancy

A time-redundancy topology estimates the nonlinear information for a period of time, and then the statistical result is processed or fed into an iterative function so as to calibrate the ADC. Recently, one such kind of technique called correlation-based [35] calibration becomes more and more popular. This technique features negligible hardware overhead for calibration and the capability to work concurrently during the normal operation. The basic concept lies in modulating the input signal with a pseudo-random sequence that is uncorrelated with the input, then the digital outputs are demodulated in order to extract the modulated error information. Since the modulated errors take same analog path as the input, demodulated information thus contains the characteristic of the ADC. Then the information is applied to the calibration circuits for the ADC calibration. A conceptual diagram is depicted in Fig. 4.5. Generally, the insertion of pseudorandom sequences is realized by changing the threshold levels in the sub-ADC [3, 7] or abstractly adding scaled references to the sub-DAC [17, 35]. Whichever is used, both result in the residue shifting up or down, leading to different distribution. By observing the distribution, we can extract the nonlinear information.

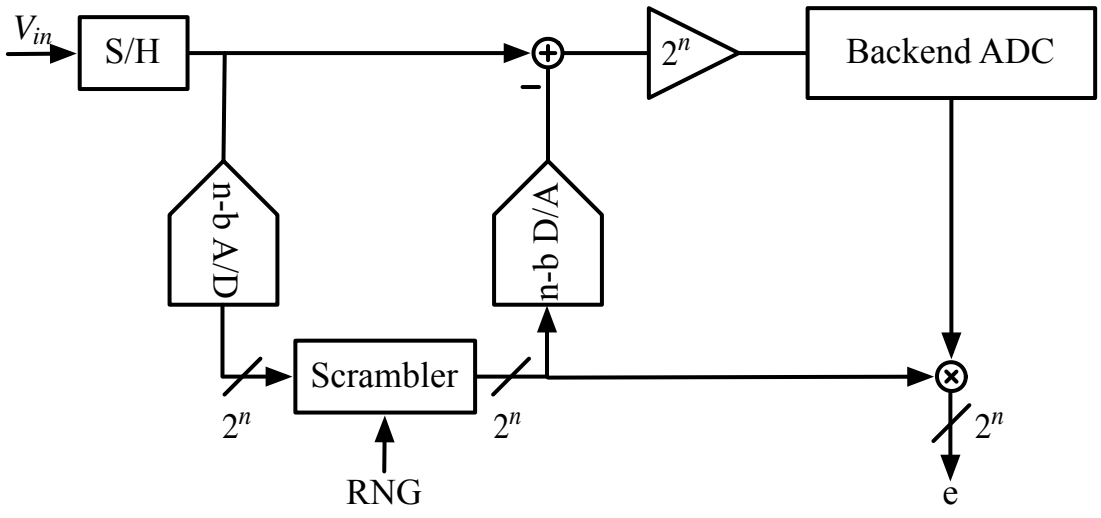

Figure 4.5: Correlation based estimation [7].

Chapter 5

DIGITAL CALIBRATION

5.1 Introduction

Digital calibration performs the task of digitally correcting the gain errors of imprecise residue amplifiers due to the finite open-loop gain, slewing, and capacitors mismatch. Some techniques can correct errors by means of carrying out digital signal processing on the ADC output codes and therefore remain the residue amplifier inaccurate. This implies the need of calibrating error by using analog circuits is reduced. Also, high order harmonics such as third, fifth order nonlinearities of the residue amplifier can be corrected through the use of more complex digital circuits. This feature is desirable since the cost/function of digital circuits decreases by 29% each year [36].

Generally, all calibration techniques are built based on their analog error models; that is to say, only the errors capable of being modeled as an equation or any other analytical problems can be calibrated. Therefore, only the deterministic errors can be corrected. As a result, model-based error estimation and calibration turn to be the key concept among the self-calibration techniques.

Many digital calibration techniques have been proposed to tackle the non-perfect analog functional blocks. Those blocks include the imprecise capacitors ratio in the sub-DAC or the non-ideal residue amplifier, including the finite open-loop gain and incomplete settling, etc. Sine the errors arising from these blocks can be modeled as deterministic representations, equations that include error terms, the basic calibration concept among these techniques is quite similar. The ADCs are self-calibrated in the manner: the residues of each stage are individually observed using their remaining stages of the pipeline ADC. Then based on the observed results, the weighting of the gain within each stage can be recalculated, therefore obtaining the accurate outputs. For example, since the contribution of each stage to the origianl digital output can be represented as its weight [18, 37], we can adjust the estimated

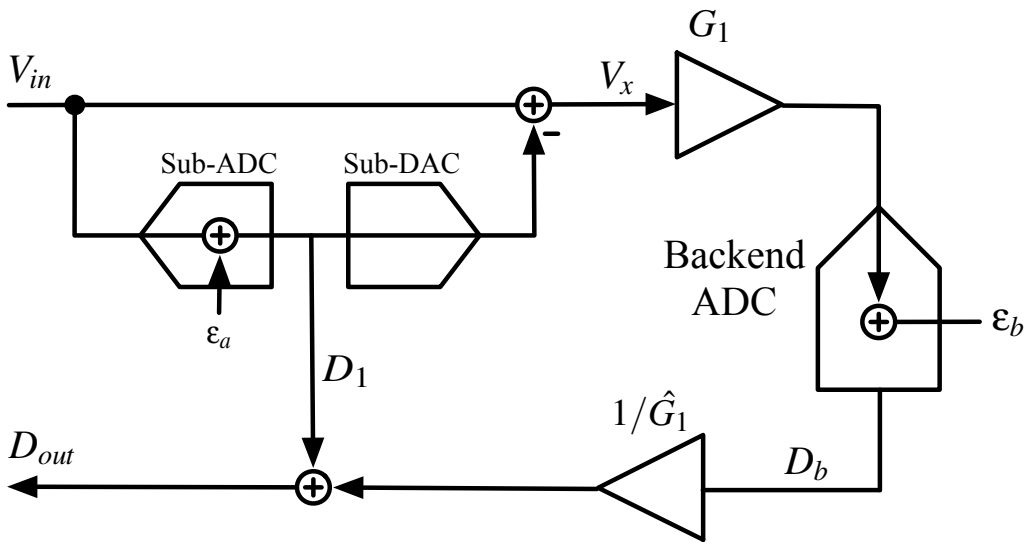

Figure 5.1: Pipelined ADC stage macro model [8].

gain in the digital domain to match the analog gain. Considering Fig. 5.1, we have

$$\begin{aligned} D_{out} &= D_1 + \frac{D_b}{\hat{G}_1} \\ &= (V_{in} + \varepsilon_a) + \frac{G_1(-\varepsilon_a) + \varepsilon_b}{\hat{G}_1}, \end{aligned} \tag{5.1}$$

where $D_1 (= V_{in} + \varepsilon_a)$ is the conversion result of the first stage and and D_b the digitized residue of first stage. ε_a and ε_b represent the quantization noises in the sub-ADC and the backend ADC accordingly, and $\hat{G}_1$ is the estimate of G_1 of the residue amplifier in the first stage. If G_1 is linear and invertible such that $\hat{G}_1 = G_1$, (5.1) becomes

$$D_{out} = V_{in} + \frac{\varepsilon_b}{\hat{G}_1}. \tag{5.2}$$

As a consequence, the output can be represented as the original input plus the total ADC quantization noise. In general, G_1 is intentionally designed to the power of 2 and therefore the digital output is obtained just by shifting bits and then adding together. In fact G_1 deviates from its ideal value, shifting bits results in the quantization noise of the sub-ADC leaking to the next stage. Odd harmonics thus arise in the spectrum due to the quantization noise of the sub-ADC correlating with the input, leading to performance degradation. Therefore, calibration is required to find out the digital gain $\hat{G}_1$ that match the analog gain G_1 of the residue amplifier.

5.2 Overview

In the following sections, we will describe a fully digital background calibration technique that is capable of correcting the errors arising from the non-perfect residue

amplifiers [3]. Then this technique is used and combined with the proposed estimation technique to highlight the proposed calibration scheme in this thesis.

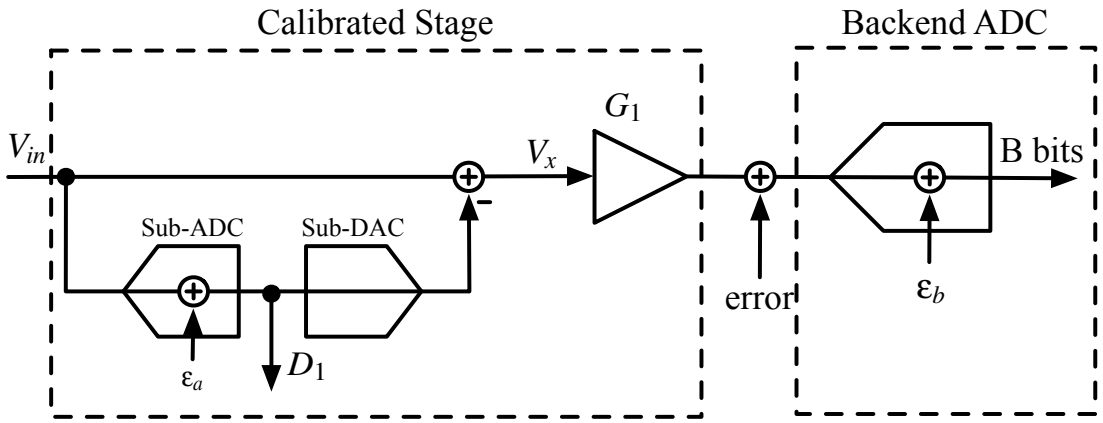

Figure 5.2: Precision requirements

Shown in Fig. 5.2 is the precision requirement after calibration. It indicates errors from the stage to be calibrated can be modeled as an additive term at the input of the backend ADC. To make the error have no impact on the ADC performance, its value must be within 1/2 LSB (the quantization noise ε_b) of the backend ADC.

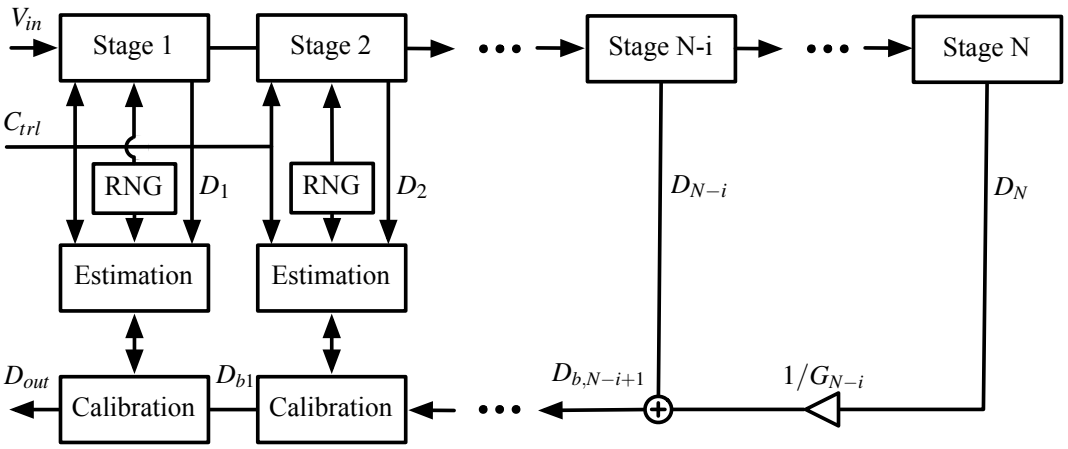

Figure 5.3: ADC block diagram

Fig. 5.3 shows the block diagram of the proposed calibration scheme including three main digital calibration functions: the pseudorandom sequence generator (labeled as 'RNG'), the calibration (labeled as 'calibration') block, and the estimation (labeled as 'estimation') block. The pseudorandom sequence generator injects multiple uniform distributed noise sequences (dithers) at the sub-DAC input. The estimation block performs the task of system identification so as to blindly find the optimal calibration parameters based on the dithered and digitized outputs of the backend ADC. The estimation block will be described in detail in chapter 6. In

Fig. 5.3, the backend ADC does not need to be calibrated since the resolution of the backend ADC is low (usually 6-8 bits); therefore, it is less significant compared with the front-end stage.

The calibration processes in the way that the least significant stage (e.g., stage i-1) is calibrated using the backend ADC (the remaining stages). Once the calibration of that stage is done, the calibration proceeds toward its front stage (e.g., stage i), and therefore the total resolution grows linearly with the calibration process, which shows similarity to the 'accuracy bootstrapping' [37]. Although the completion of the calibration within each stage is done once at a time, calibrations of each stage can work concurrently. That is, the calibration of each stage comes about simultaneously and ends after the calibration of the most significant stage is done.

To simplify the analysis, all stages are assumed to be ideal except for the first stage as represented in Fig. 5.1. Since the fully differential architecture is often adopted all over the high resolution ADCs, the even harmonics are much less significant as a consequence. Under this condition, the fundamental tone and the third harmonic will dominate the overall performance [3, 17]. If those above conditions are satisfied, the object to be calibrated, the open-loop residue amplifier in the first stage, can be approximated as a third-order polynomial:

$$G_1(V_x) = V_{res} = a_1(V_x) + a_3(V_x)^3, \tag{5.3}$$

where $V_x = -\varepsilon_a$. Alternative models can be found in [38].

5.3 Calibration Mechanism

Nonlinear gain error of the residue amplifier are first calibrated since it will affect the estimation of the linear gain error. In order to correct the nonlinear errors, one possible solution is finding the nonlinear term $a_3(V_x)^3$ in (5.3) then being subtracted from the original residue, which can be realized by using an inverse function described in [3].

After the nonlinear term $a_3(V_x)^3$ is corrected, linear gain error can be calibrated by recalculating the digital gain with respect to each stage, thus obtaining a linearized output.

5.3.1 Nonlinear Gain Error Calibration

Rearranging (5.1) in a more general form, we have

$$\begin{aligned} D_{out} &= D_1 + G_1^{-1}(D_b) \\ &= (V_{in} + \varepsilon_a) + G_1^{-1}[G_1(-\varepsilon_a) + \varepsilon_b], \end{aligned} \tag{5.4}$$

where G_1^{-1} is the inverse of G_1 provided that G_1 is invertible.

Taking the first order Taylor expansion of the last term in (5.4) gives

$$D_{out} \cong V_{in} + \varepsilon_a + G_1^{-1}[G_1(-\varepsilon_a)] + \varepsilon_b \frac{dG_1^{-1}}{dD_b} = V_{in} + \varepsilon_b \frac{dG_1^{-1}}{dD_b} = V_{in} + \varepsilon_b \left[\frac{dG_1}{d(-\varepsilon_a)}\right]^{-1}. \tag{5.5}$$

According to (5.5), the output can be represented as an input and an output-referred inverse function. To make the residue linear, the nonlinear term $a_3(V_x)^3$ needs to be removed; therefore a linearized residue can be obtained by

$$V_{res,linear} = G_1(V_x) - e(V_x). \tag{5.6}$$

Observing this equation, we can represent $e(V_x)$ as

$$e(V_x) = G_1(V_x) - a_1 G_1^{-1}(V_{res}). \tag{5.7}$$

Using the fact $V_x = -\varepsilon_a = G_1^{-1}(V_{res})$, $V_{res} = D_b - \varepsilon_a$ and substituting them into (5.7), we obtain $e(D_b)$ represented in digital domain [39]:

$$\begin{aligned} e(D_b) &\cong D_b - a_1 G_1^{-1}(D_b) - \varepsilon_b \left[1 - a_1 \left(\frac{dG_1}{dV_x}\right)^{-1}\right] \\ &\cong D_b - a_1 G_1^{-1}(D_b). \end{aligned} \tag{5.8}$$

As a result, (5.8) is used to correct the nonlinear error. Observing the neglected term $\varepsilon_b[1 - a_1(\frac{dG_1}{dV_x})^{-1}]$, how much will it affect the precision of the calibration? Considering $\varepsilon_b[1-a_1(\frac{dG_1}{dV_x})^{-1}]$ in (5.8) while taking the differential of G_1 with respect to V_x, we can further expand it as

$$\varepsilon_b[1 - a_1(\frac{dG_1}{dV_x})^{-1}] = \varepsilon_b \cdot \left[1 - a_1 \left(\frac{dG_1}{dV_x}\right)^{-1}\right] = \varepsilon_b \left[1 - a_1 \left(\frac{1}{a_1 + 3a_3\varepsilon_a^2}\right)\right]. \tag{5.9}$$

If dividing both sides by ε_b, we obtain a relative error with respect to the backend quantization error in LSB such that

$$error = \varepsilon_b/\varepsilon_b \left[1 - \left(\frac{a_1}{a_1 + 3a_3\varepsilon_a^2}\right)\right] \approx 1 - \left(1 - \frac{3a_3}{a_1}\varepsilon_a^2\right) = \frac{3a_3}{a_1}\varepsilon_a^2. \tag{5.10}$$

Indicated by (5.10), it implies a multi-bit architecture is preferred because of a_1 in the denominator, resulting in less harm to DNL; however even with a single-bit architecture, the redundancy topology makes ε_a a relatively small value when compared to ε_b. Thus, the neglected term makes an relatively small error on DNL and the accuracy consequently.

To find $G_1^{-1}(D_b)$ in (5.8), a trigonometric approximation is used [3]

$$e(D_b) = D_b - 2\sqrt{\frac{-a_1^3}{3a_3}} \cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{D_b}{2\sqrt{\frac{-a_1^3}{27a_3}}}\right)\right]. \tag{5.11}$$

The above equation points out $e(D_b)$ only depends on the digitized residue D_b and the ratio a_3/a_1^3; that is, once this ratio is found, the linear residue can be recovered by subtracting $e(D_b)$ to the original nonlinear residue. Another approaches can be found in [17] .

5.3.2 Linear Gain Error Calibration

Considering Fig. 5.1 and rearranging (5.1), we have

$$\hat{G}_1 \cdot D_{out} = \hat{G}_1 \cdot D_1 + D_b.$$

The digital output D_{out} thus becomes

$$D_{out} = \hat{G}_1 D_1 + D_b. \tag{5.12}$$

Observing this equation, the local conversion result D_1 has become $\hat{G}_1 D_1$, which results in a global gain error of the whole ADC; however, this global gain error is tolerable in most applications such as digital communication in which the ADC is preceded by an automatic gain control (AGC) amplifier. As a result, the linear gain calibration is accomplished by recalculating the digital gain that matches the analog gain.

5.4 Summary

Fig. 5.4 summarizes the digital calibration mechanism. Two arguments p_1 and p_3 depicted in Fig. 5.4 are the correction parameters to compensate for the linear and nonlinear gain errors respectively. According to the description above, their optimum values are expressed as

$$\begin{aligned} p_{1,opt} &= a_1 \\ p_{3,opt} &= \frac{a_3}{a_1^3}, \end{aligned} \tag{5.13}$$

where they correspond to a_1 and the ratio in (5.11).

In practice, the characteristics of the residue amplifier may drift due to temperature, time, process, etc, resulting in varying p_1 and p_3. For open-loop amplifier implementation, these variations become even sever in the absence of feedback. As a result, in next chapter we propose a novel digital calibration scheme that can accurately estimate the real amplifier operating condition and adaptively update p_1 and p_3.

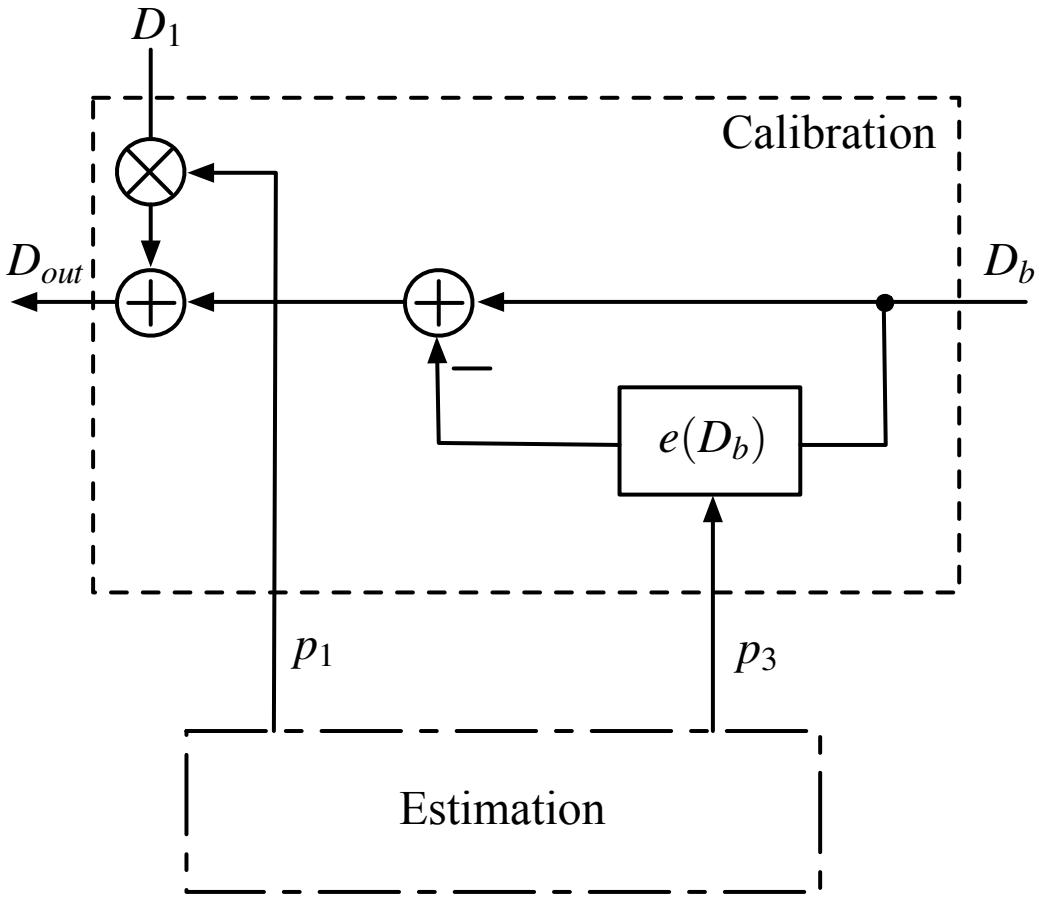

Figure 5.4: Complete digital correction [3].

Chapter 6

MULTI-CORRELATION ESTIMATION (MCE) TECHNIQUE

6.1 Introduction

In the following sections, we propose a novel calibration scheme that can accurately estimate and correct errors arising from the residue amplifiers and continuously track and update the correction parameters against environmental variations. Because using the open-loop amplifier rather than closed-loop one in the pipeline stages, the amplifier may substantially changes its transfer function due to the absence of feedback. This condition dictates the need of fast updating the correction parameters. Under this condition, the proposed scheme enables fast and continuous estimation for the varying amplifier in short time intervals as compared to [35]. Meanwhile, the scheme operates during the normal ADC conversion with no scheduled calibration cycles or use of redundant hardware [15] or slots queues [4, 40] to enable the background feature.

To estimate the error information about the MDAC or the amplifier, many calibration techniques have been proposed. Some techniques need additional stages [3, 18, 37] to reduced the backend ADC quantization noise, enabling precise estimation of the transition heights that relate to amplifier's gain. Fig. 6.1 indicates that the transition height of the residue is proportional to the amplifier's gain [41–43]. However, some of such techniques need to stop the input then a calibration signal can be applied as in [18], which is not allowed in many applications. Other approaches acquire the nonlinear information by using a parallel ADC to compare the difference of an ideal output (from the parallel ADC) and a real one (from the main ADC) [1, 44]. Fig. 6.2 demonstrates this idea.

For instance, the split-ADC architecture extracts the nonlinear information using separated ADC channels [5, 7]. If these channels were non-perfect, the unbalanced channels generate different outputs that can be used for nonlinearity correction as shown by Fig. 6.3 and 6.4. While such techniques have the advantages of deterministic error extraction therefore reducing the calibration time, they increases

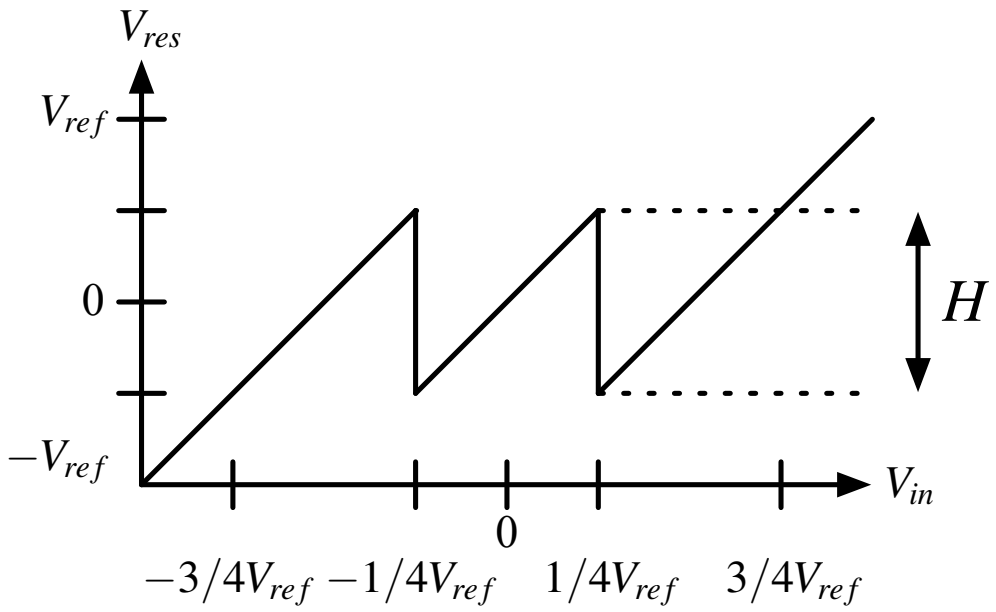

Figure 6.1: Transition height of digitized residue.

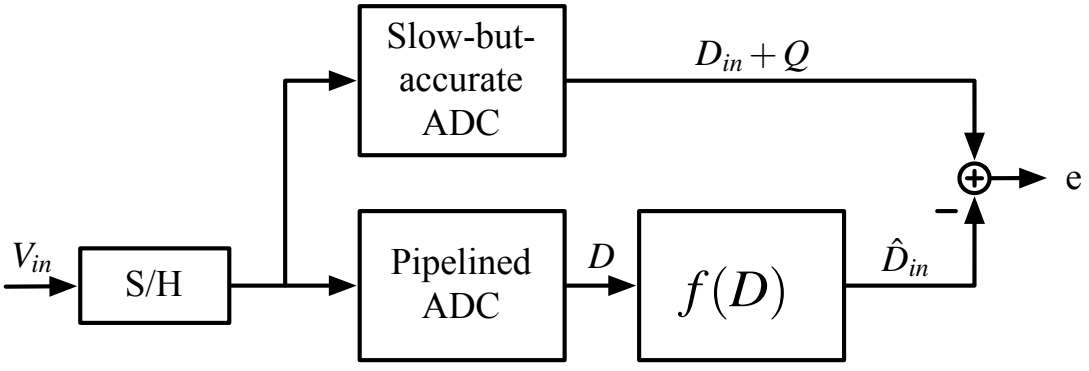

Figure 6.2: Error correction of pipelined ADC [1].

analog circuits' complexity, imposing penalties of larger die area, power, and bandwidth [45].

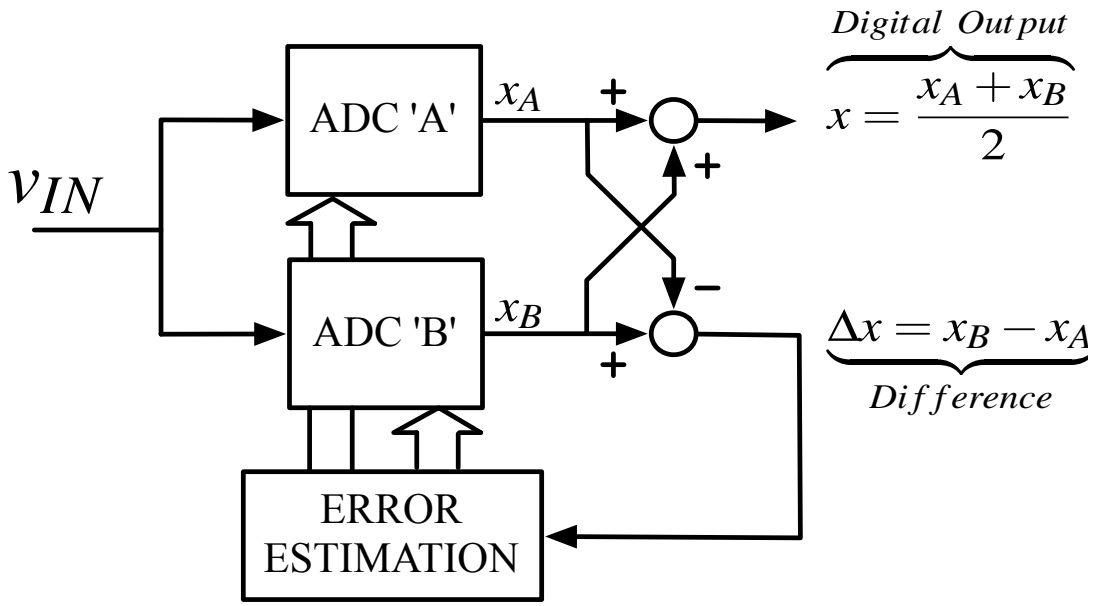

Figure 6.3: "Split" ADC architecture [5].

Some calibration techniques, called the correlation-based technique, use statistical functions to estimate errors therefore being able to correct gain errors have been presented in literature [17,35,44]. In these techniques, the analog error is modulated using a pseudo-random noise sequence and then the digital output is processed in order to extract the error information useful to calibrate the ADC.

Having described the features of above techniques, we propose a technique that has the following superiorities:

- *No limitation on the input amplitude:*
  The benefit of the proposed technique relative to that presented in [3] is that it works for any input signal, and the benefits relative to that presented in [17] are that it does not have restrictions on dc input and it is not sensitive to amplifier offsets.

- *Reduced circuit complexity:*
  The proposed calibration scheme cooperated with statistics-based estimation enables the use of a low resolution backend ADC. Unlike the work in [3], the resolution of the backend ADC is no longer limited by the target resolution minus one. Therefore, employing simple circuits yields the potential toward high speed and/or low power. To facilitate the estimation, the required pseudorandom noise sequences (RNGs) only needs negligible modifications on the sub-DAC.

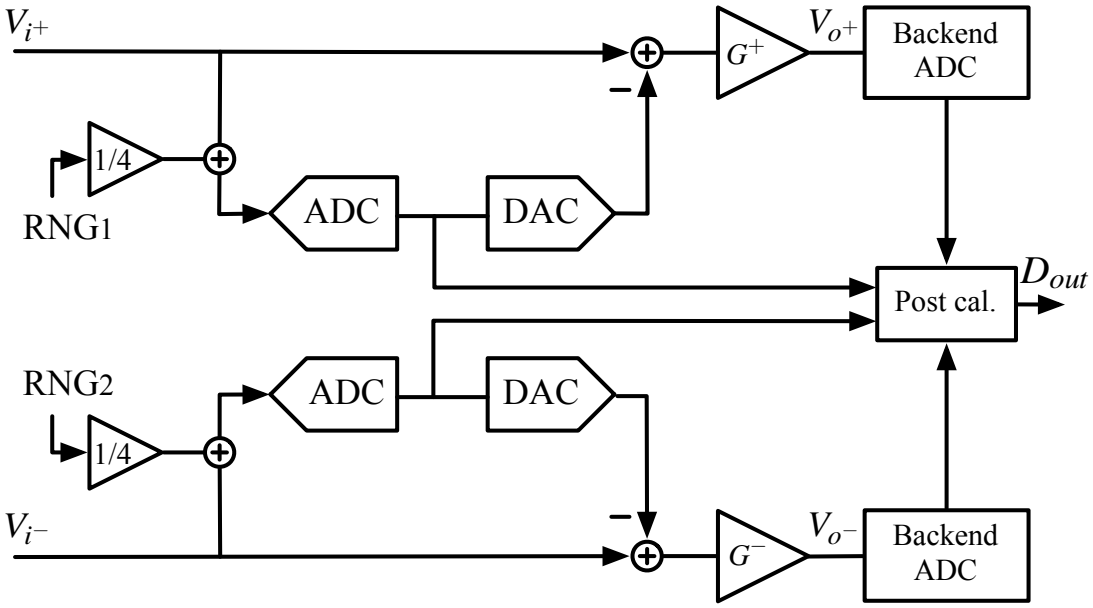

Figure 6.4: Two channel ADC architecture [7].

- *Digital background calibration:*
  All the calibration circuits are built using digital circuitry. Given that the input acts as a stimulus and is modulated with the RNGs, the scheme performs error estimation and calibration during the normal operation of the ADC.

- *Unbiased gain error information extraction:*
  With the simple statistical function (mean function) and the estimation procedure, the linear and nonlinear gain error information of the amplifier can be extracted independently. Notably, error information of high order nonlinearities, e.g., 5th order, is possible if more RNGs are merged.

In the following sections, we will describe the technique with the associated functions in detail.

6.2 Modulation Approach

The proposed scheme makes use of the fact that the offsets in the sub-ADC does not affect the ADC conversion results based on the digital redundancy [21]. As a result, the scaled random noise sequences whose values no more than the tolerable offsets can be applied using either the sub-ADC or the sub-DAC. Because of the added random sequence, the residue moves up/down. Fig. 6.5 shows one possible residue plot when the RNG is added. It shows that one input signal may have two different residues. However, their conversion results agree provided that the gain errors are perfectly corrected. Similar approaches can be found in [3, 7, 17, 35, 44]. The modulation approach implementation will be explained in chapter 7.

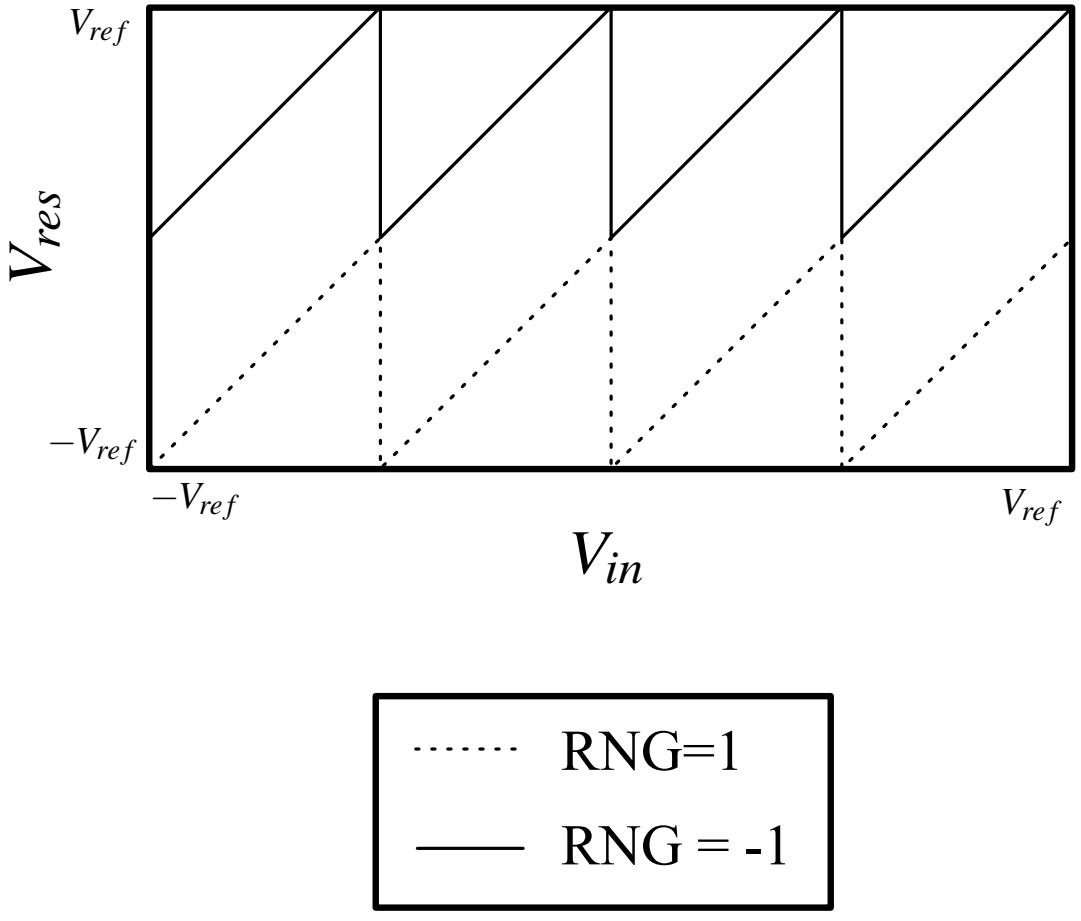

Figure 6.5: Residue plot when adding RNGs.

In order to unbiasedly estimate the correction parameters, the RNG is designed as a uniformly distributed pseudorandom binary number sequence, i.e., ($RNG \in \{1, -1\}$) and is uncorrelated with the input. As a result, the RNG is continuously applied to the stage being calibrated to continuously estimate and update the correction parameters.

In the remainder of this chapter, we propose a multi-correlation estimation (MCE) technique using the modulation approach, allowing continuous background estimation of the correction parameters p_1 and p_3 described in the previous chapter.

6.3 Multi-Correlation Estimation (MCE) Technique

In this section we will describe a technique based on statistics that can estimate the correction parameters. Using two different modulated sequences, this approach results in the residue having different distributions. Then the statistical results associated with the residues are used to find the nonlinearities, i.e., the error information. With the help of this information, we can approach the optimum values of p_1 and p_3 using Least Mean Square (LMS) algorithm [46].

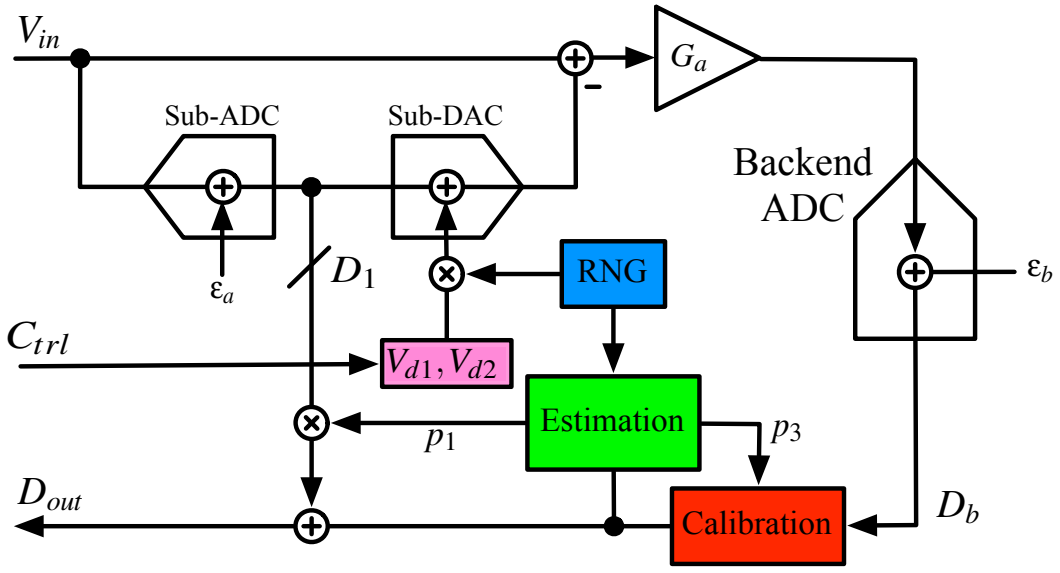

Figure 6.6: Reduced model with proposed calibration scheme.

Considering Fig. 6.6, the digitized residue D_b when the random sequences are applied is

$$\begin{aligned} D_{bi} &= a_1(V_x) + a_3(V_x)^3 + \varepsilon_b \\ &= a_1(-\varepsilon_a + R_i \cdot V_{di}) + (-\varepsilon_a + R_i \cdot V_{di})^3 + \varepsilon_b, \ i \in \{1, 2\} \end{aligned} \tag{6.1}$$

where R_i are the pseudo-random number sequences that are uniformly distributed and uncorrelated with the input and $R_i \in \{1, -1\}$. V_{di} represent the amplitudes.

Therefore, R_i times V_{di}, i.e., R_iV_{di} add offsets of $\pm V_{d1}$ or $\pm V_{d2}$ LSB (of local sub-ADC) to the sub-DAC. They are

$$R_1V_{d1} \in \{+V_{d1}, -V_{d1}\},$$

$$R_2V_{d2} \in \{+V_{d2}, -V_{d2}\}.$$

Taking the correlations of D_{bi} and R_i, we have

$$E[R_iD_{bi}] = E\left[a_1(-R_i\varepsilon_a - V_{di}) + a_3(-R_i\varepsilon_a^3 - 3\varepsilon_a^2V_{di} - 3R_i\varepsilon_aV_{di}^2 - V_{di}^3) + R_i\varepsilon_b\right]. \tag{6.2}$$

Because R_i are uncorrelated with the input, correlations of R_i and the quantization errors ε_a, ε_b will be zero. Under this circumstance, (6.2) is further reduced to

$$E[R_iD_{bi}] = a_1(-V_{di}) + a_3(-3\varepsilon_a^2V_{di} - V_{di}^3). \tag{6.3}$$

This finding reveals the quantization noise of backend ADC has no effect on the estimation accuracy as compared with [3].

Considering the terms $a_1(-V_{di})$ and $a_3(-3\varepsilon_a^2V_{di})$ in (6.3), if they can be eliminated, the result is proportional to a_3. For such a reason, we propose a technique called "multi-correlation estimation technique" that can accurately estimate the error information.

Using (6.3) and $V_{d2} = V_{d1}/2 = LSB/4$ gives

$$\varepsilon_3 = E[R_1D_{b1}] - 2E[R_2D_{b2}] = -\frac{3}{4}a_3V_{d1}^3. \tag{6.4}$$

In this equation, ε_3 represents the sum of correlations $E[R_1V_{d1}]$, $E[R_2V_{d2}]$ and is directly proportional to a_3, leading to an unbiased estimation. If the correction function (5.11) is applied, we obtain

$$\varepsilon_3 = -\frac{3}{4}a_3V_{d1}^3 = -\frac{3}{4}a_1^3V_{d1}^3 \cdot (p_{3,opt} - p_3). \tag{6.5}$$

This result indicates the deviation of parameter p_3 from its ideal value is directly proportional to ε_3. According to this result, we can use iterative functions, e.g., LMS algorithm, trying to minimize the deviation so as to obtain the ideal value of p_3.

As can be seen from the derivation of ε_3, it only represents the degree of nonlinear term a_3. Hence, we need another error information related to the linear gain a_1. Indicated by (6.3), the resulting correlation is proportional to a_1 when $a_3 = 0$. That is, when the nonlinear gain error has been corrected, we define (6.3) as

$$\varepsilon_1 = E[R_1D_{b1}] = a_1(-V_{d1}), \tag{6.6}$$

where ε_1 represents the linear gain error information. In addition, correlation of R_2 and D_{b2} can be used as well. Since $p_{1,opt} = a_1$ as indicated in (5.11), it is straightforward that dividing ε_1 by V_{d1} is $p_{1,opt}$. However, this procedure takes large number of samples for reducing the variance of p_1. For an N-bit ADC, roughly 2^{2N}

samples are required to obtain sufficiently accurate estimate of a_1 [5]. Above results suggest that fast updates of p_1 and p_3 is desirable. As a result, we employ LMS algorithm to achieve this goal. Although making use of LMS still needs an amount of time to converge the corrections parameters to a sufficient accuracy, once they have converged, each update is fast enough to track the environment variations. In order to be merged in the LMS loop, ε_1 is modified as

$$\varepsilon_1' = \frac{\varepsilon_1}{p_1} + V_{d1} = -\frac{a_1 V_{d1}}{p_1} + V_{d1}. \tag{6.7}$$

In this modification, p_1 will approaches $p_{1,opt}$ when $\varepsilon_1' = 0$ by using LMS.

6.4 Adaptive Signal Processing

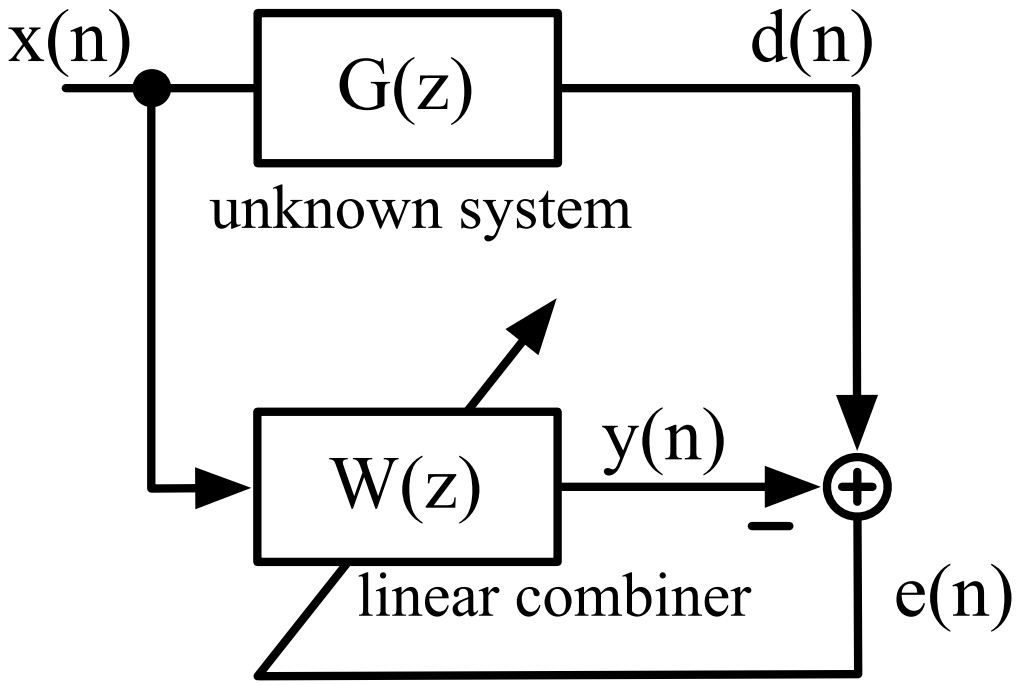

Figure 6.7: Adaptive system performing system identification.

Adaptive signal processing performs the task of identifying the "model" of an unknown "system" based on the knowledge of a certain input $x(n)$ and its corresponding output $d(n)$ to the system [46]. Fig. 6.7 shows a typical block diagram of an adaptive system. The error signal $e(n)$ is made by subtracting the adaptive linear combiner's output $y(n)$ from the desired output $d(n)$. Then $e(n)$ is fed back to $W(z)$ in order to update parameters of the combiner; as a result, $W(z)$ tries to act like $G(z)$. Under this condition, the optimum parameters of a linear combiner (linear filter) are obtained by minimizing its *mean square error* (MSE). When

the unknown system changes, $W(z)$ tracks it accordingly. Therefore, this kind of searching methodology is suitable for the varying open-loop amplifier.

Based on the concept of adaptive systems, the same idea of minimizing the MSE can be applied to minimizing the ε_1' and ε_3. A practical implementation of the adaptive system is using the LMS algorithm for the blind search of $p_{1,opt}$ and $p_{3,opt}$. Using LMS algorithm has many advantages: 1) easy-to-implement, 2) stable and robust against the environment disturbance. Based on the LMS algorithm, two recursions are constructed with respect to ε_1' and ε_3. They are

$$p_1(k+1) = p_1(k) - \mu_1 \varepsilon_1', \tag{6.8}$$

$$p_3(k+1) = p_3(k) - \mu_3 \varepsilon_3. \tag{6.9}$$

Observed from the equations, each contains a simple register and a summing node, which can be represented by Fig. 6.8, where μ_i are the step sizes that control the convergence speed.

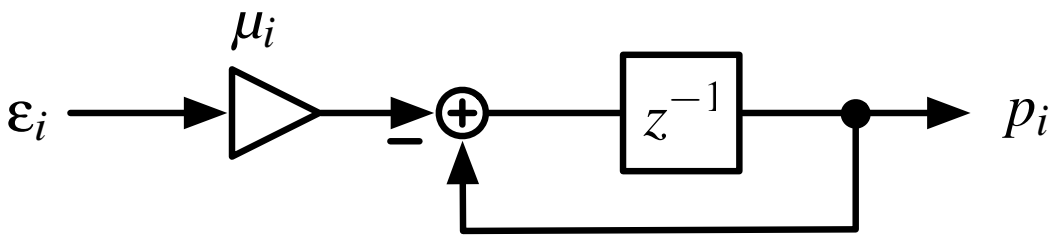

Figure 6.8: Recursive iteration using LMS.

Chapter 7

PRACTICAL CONSIDERATIONS ON IMPLEMENTATION

7.1 Introduction

In this chapter, we will describe the technique in depth, including its practical implementation and design consideration. Therefore, we will explain the required circuit modifications involved in this scheme in realizing the estimation and the calibration procedures. The estimation procedure enabling the background calibration process will be explained in Sec. 7.2.3.

7.2 Circuit Modifications

To realize the estimation and the LMS loop introduced in chapter 6, some circuit modifications in the conventional ADC architecture are required. These modifications consist of the analog and digital circuits.

7.2.1 Analog Part

In a conventional sub-DAC implementation of a pipelined ADC, the capacitor array often employs the thermometer encoding, which results in unity elements. For example, a stage resolving 2-bit has 4 unity capacitors. The configuration during the sampling phase in an open-loop architecture remains; however, during the amplification phase, we connect the grounded capacitor to the voltage references instead, resulting in $\pm V_{d1}$ offsets at the sub-DAC output. If a smaller offsets $\pm V_{d2}$ were being injected, we can divide the grounded capacitor by two while keeping same capacitance. By charge conservation, connecting the voltage reference to one of the smaller capacitor while keeping the other grounded results in offsets of $\pm V_{d2}$ at the sub-DAC output. By doing so, this modification avoid using additional voltage

references, thereby making the design simpler. The modified sub-DAC is shown in Fig. 7.1.

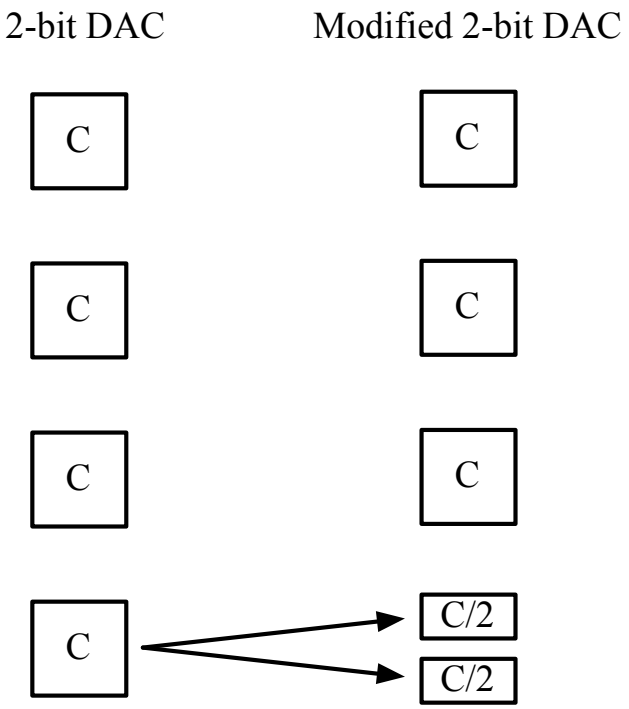

Figure 7.1: Modified capacitor array.

7.2.2 Digital Part

The correlation performing multiplication and expectation can be realized by simple accumulators, bit-shifting, and adders. Fig. 7.2 depicts its implementation, where the Low pass filter (LPF) is realized with a simple accumulator. Of the product $R_i D_{bi}$ in (6.2), since the RNGs have only two values, 1 or -1, the multiplication is realized just by changing the sign of D_b then being integrated. Meanwhile the discrete time integrator in the LMS loop can be realized with simple accumulators as well.

To correct the nonlinear gain error, a two-dimension loop-up table implementing $e(D_b)$ can be precomputed and stored in a ROM [3]. Then the linear gain error can be corrected either by multiplying D_1 by p_1 or D_b being divided by p_1.

7.2.3 Alternative Injection of RNGs

To enable the background calibration, the two offsets $\pm V_{d1}$ and $\pm V_{d2}$ are applied alternatively; that is to say, $\pm V_{d1}$ are injected and then the $\pm V_{d2}$ or vice versa, while either they are positive or negative depends on the RNGs.

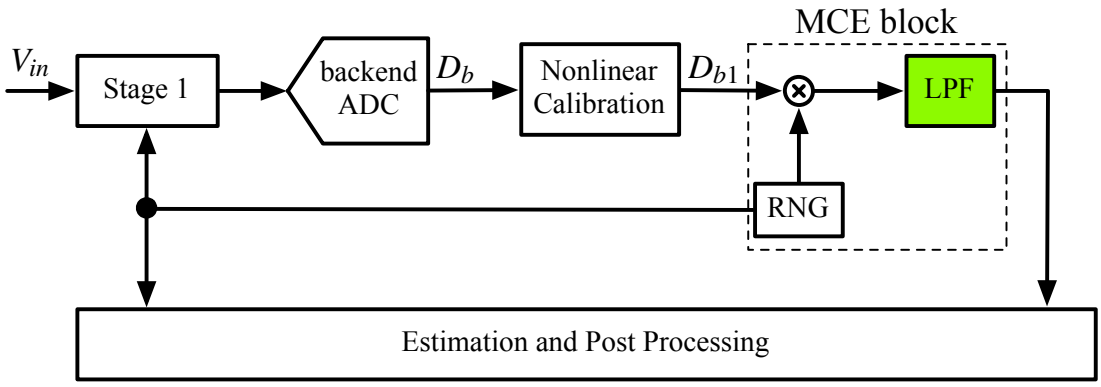

Figure 7.2: Block diagram of the background calibration scheme.

According to (6.4), two RNGs are theoretically necessary. However, each stage can use the same random sequences generated from only one generator; therefore one RNG is sufficient in reality.

7.3 Complete Calibration Scheme

Combined with the concepts explained in the previous chapter and above sections, the estimation block using the LMS loop is shown in Fig. 7.3. The MCE block in the estimation block calculates the correlation of D_b and RNG, thus finding out ε_1 and ε_3. Fig. 7.2 shows the detailed content of the MCE block. In the LMS loop, the discrete time integrator forces the mean values of ε_1' and ε_3 to zero, leading to p_1 and a_3 approaching a_1 and zero, respectively. This can be further explained by rewriting p_3 and p_1 in (6.4) and (6.6) as

$$\varepsilon_3 = -\frac{3}{4}a_1^3 V_{d1}^3 \cdot (p_{3,opt} - p_3), \tag{7.1}$$

and

$$\varepsilon_1' = -\frac{p_{1,opt}V_{d1}}{p_1} + V_{d1}. \tag{7.2}$$

ε_1' and ε_3 equal zero provided that p_1, p_3 approach $p_{1,opt}$, $p_{3,opt}$.

7.4 Estimation Confidence Level

Due to the statistical variations in the estimation of ε_1 and ε_3, large samples of D_b are required. Ideally, infinite samples make unbiased ε_1 and ε_3; however, it is not practical since improving the accuracy by $\sqrt{2}\times$ costs double samples to be taken, therefore doubling the calibration time. For such a reason, how many samples should be taken is important in reaching an accessible balance between the estimation accuracy and the tracking time.

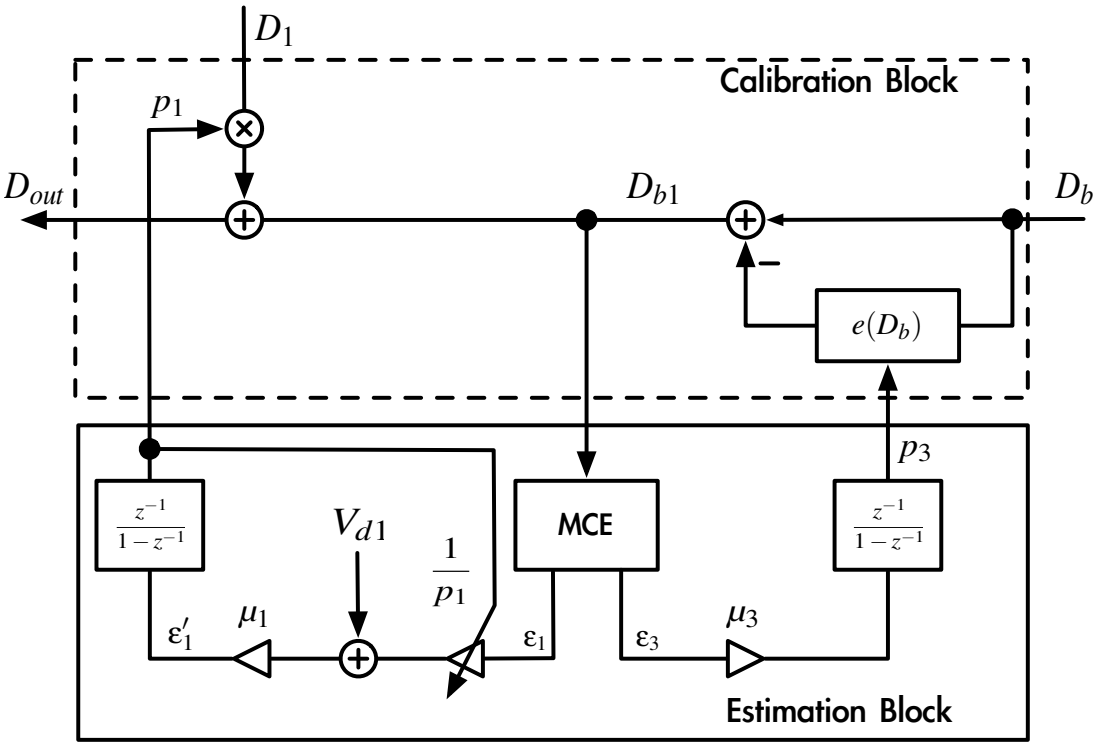

Figure 7.3: Complete background calibration scheme using LMS algorithm.

Using the theorem *Law of Large Numbers* [47, 48] gives

$$var[m_X] = \frac{1}{N} var[X], \tag{7.3}$$

where m_X is the *N-sample* mean (expectation) of an infinite-long random variable X. This equation tells that the variance between each N-sample average of X is governed by the number of samples being taken, i.e., N. Using this property while representing $m_{X1} = E[R_1 D_{b1}]$ and $m_{X2} = E[R_2 D_{b2}]$ gives the variance of ε_3:

$$var[\varepsilon_3] = var\left[E[R_1 D_{b1}] - 2E[R_2 D_{b2}]\right] \cong var[m_{X1}] + 4var[m_{X2}]. \tag{7.4}$$

Let D_{bi} be the random variable in (7.3) and normalized with respect to V_{ref}, which results in D_{bi} uniformly distributed within $\pm 1/2V_{ref}$. Under this condition, (7.4) now relates to the number of samples N, and we have

$$var[\varepsilon_3] \cong \frac{1}{N_a}\frac{V_{ref}^2}{12} + 4 \cdot \frac{1}{N_b}\frac{V_{ref}^2}{12}, \tag{7.5}$$

where N_a and N_b represent the number of samples when $\pm V_{d1}$ and $\pm V_{d2}$ are injected respectively. This finding suggests that more samples we take, more accuracy we get. In order to build the confidence level, we introduce a parameter γ_3 into (7.5) and let $N_a = N_b = N_3$, giving

$$\gamma_3^2 var[\varepsilon_3] = \frac{5\gamma_3^2 V_{ref}^2}{12N_3} \leq (\varepsilon_3^2). \tag{7.6}$$

Using the same approach with respect to ε_1, we obtain

$$var[\varepsilon_1] = \frac{1}{N_1}\frac{V_{ref}^2}{12}. \tag{7.7}$$

And the introduced parameter γ_1 that controls the confidence level of ε_1 in (7.7) gives the confidence level:

$$\gamma_1^2 var[\varepsilon_1] = \frac{\gamma_1^2 V_{ref}^2}{12N_1} \leq (\varepsilon_1^2). \tag{7.8}$$

Above equation suggests that 99.7% of the estimate of ε_1 falls in the range of $\varepsilon_1 \pm \varepsilon_1/3$ if we choose $\gamma_1 = 9$. This result can also be applied to ε_3. In light of above developments, (7.6) and (7.8) as well as the controlling parameters γ_3 and γ_1 help us determine how many samples we should take with satisfied confidence levels.

7.5 LMS Loop Analysis

7.5.1 Convergence

In the feedback loop in Fig. 6.7, the step sizes μ_i determine the convergence conditions of the loop.

Substituting (7.1) into (6.9) gives

$$\begin{aligned} p_3(k+1) &= p_3(k) - \mu_3 \left[-\frac{3}{4} a_1^3 V_{d1}^3 (p_{3,opt} - p_3(k)) \right] \\ &= p_3(k) \left(1 - \mu_3 \frac{3}{4} a_1^3 V_{d1}^3 \right) + \mu_3 \frac{3}{4} a_1^3 V_{d1}^3 p_{3,opt}, \end{aligned} \tag{7.9}$$

and then subtracting $p_{3,opt}$ from both sides results in

$$\begin{aligned} p_3(k+1) - p_{3,opt} &= p_3(k) \left(1 - \mu_3 \frac{3}{4} a_1^3 V_{d1}^3 \right) + \mu_3 \frac{3}{4} a_1^3 p_{3,opt} - p_{3,opt} \\ &= (p_3(k) - p_{3,opt}) \left(1 - \mu_3 \frac{3}{4} a_1^3 V_{d1}^3 \right). \end{aligned} \tag{7.10}$$

Making $V_3(k) = p_3(k) - p_{3,opt}$, the difference between p_3 and $p_{3,opt}$, we therefore can rewrite (7.10) as

$$V_3(k) = V_3(0) \left(1 - \mu_3 \frac{3}{4} a_1^3 V_{d1}^3 \right)^k, \tag{7.11}$$

where $V(0)$ is the initial condition. Based on this result, the requirement for (7.11) to be convergent is

$$\left| 1 - \mu_3 \frac{3}{4} a_1^3 V_{d1}^3 \right| < 1. \tag{7.12}$$

Therefore,

$$\frac{8}{3a_1^3 V_{d1}^3} > \mu_3 > 0. \tag{7.13}$$

It is worthy noting that (7.13) is a necessary condition rather than a sufficient one. Since $e(D_b)$ has a usable region, large μ_3, therefore large p_3, may causes $e(D_b)$ a multiple-to-one function. As a result, the inverse does not exist. In reality, the ADC resolution determines the maximum value of μ_3; in most cases, μ_3 is far smaller than the upper bond in (7.13), preventing $e(D_b)$ from not existing as a consequence.

Using the same approach to find the upper bond of μ_1, we have

$$\begin{aligned} p_1(k+1) &= p_1(k) - \mu_1 \varepsilon_1' \\ &= p_1(k) - \mu_1 \left(\frac{a_1(-V_{d1})}{p_1(k)} + V_{d1} \right) \\ &= p_1(k) - \mu_1 \left(\frac{a_1(-V_{d1}) + p_1(k)V_{d1})}{p_1(k)} \right) \\ &= p_1(k) - \mu_1 V_{d1} \left(\frac{p_1(k) - a_1}{p_1(k)} \right). \end{aligned} \tag{7.14}$$

Again, subtracting $p_{1,opt}(= a_1)$ from both sides, and making $V_1(k) = p_1(k) - p_{1,opt}$ the difference between p_1 and the ideal value $p_{1,opt}$, we obtain

$$V_1(k) = V_1(0) \left(1 - \frac{\mu_1 V_{d1}}{p_1'} \right)^k. \tag{7.15}$$

The term p_1' in the denominator of (7.15) starts from 2^N in initial, and then converges to its optimum value. Under this condition, we assume it has a fixed value if it falls between the initial and the optimum value and therefore the equation may be convergent. If the above conditions were satisfied, it is possible to represent

$$\left| 1 - \frac{\mu_1 V_{d1}}{p_1'} \right| < 1. \tag{7.16}$$

Thus, the convergence criteria of μ_1 is

$$\frac{2p_1'}{V_{d1}} > \mu_1 > 0. \tag{7.17}$$

7.5.2 Time Constant

The *time constant* in an LMS loop indicates how fast the loop will approach its optimum value. Hence, the time constant influences the calibration period. A definition of time constant is that *"the time at which the initial condition has decayed to a value of 1/e times initial value"* [46]. With the definition, we thus can find the time constant τ_3 by using (7.11), therefore

$$\frac{1}{e} V_3(0) = V_3(0) \left(1 - \mu_3 \frac{3}{4} a_1^3 V_{d1}^3 \right)^{\tau_3}. \tag{7.18}$$

Taking the natural log on both sides and using the first order Taylor expansion

$$\ln(1 - x) \cong -x,$$

we obtain

$$\tau_3 \cong \frac{4}{3a_1^3 V_{d1}^3 \mu_3}. \tag{7.19}$$

Applying the same approach to (7.15) gives

$$\tau_1 \cong \frac{p_1'}{\mu_1 V_{d1}}. \tag{7.20}$$

7.5.3 Correction Parameter Variance

The estimated p_1 and p_3 variances are largely affected by the variance of the estimated ε_1 and ε_3 due to the statistical estimating process. The phenomenon of keeping varied p_1, p_3 occurs even the LMS loop under steady-state. To analyze this issue then incorporated in the proposed scheme, we construct an expression representing this condition using (6.9). When the loop is in steady-state, we have

$$p_3(k) = p_3(0) - \mu_3 \sum_{j=1}^{k-1} \varepsilon_{3,j}. \tag{7.21}$$

Taking the variances on both sides, we obtain

$$var[p_3(k)] = \mu_3^2 var[\varepsilon_3]. \tag{7.22}$$

Substituting (7.6) into (7.22), we have

$$var[p_3(k)] = \frac{9\mu_3^2 a_3^2 V_{d1}^6}{16\gamma_3^2}. \tag{7.23}$$

Hence, (7.23) indicates the variance of p_3 in steady-state.

Applying the same approach to p_1 while using (6.8) gives

$$p_1(k) = p_1(0) - \mu_1 \sum_{j=0}^{k-1} \varepsilon_{1,j}'. \tag{7.24}$$

Also, taking variances on both sides gives

$$var[p_1(k)] = \mu_1^2 var[\varepsilon_1'] = \mu_1^2 \frac{1}{a_1^2} var[\varepsilon_1]. \tag{7.25}$$

Therefore, we have the expression

$$\begin{aligned} var[p_1(k)] &= \frac{1}{a_1^2 \gamma_1^2} \mu_1^2 a_1^2 V_{d1}^2 \\ &= \frac{\mu_1^2 V_{d1}^2}{\gamma_1^2}. \end{aligned} \tag{7.26}$$

Both (7.23) and (7.26) give the variances of the correction parameter when the loops have converged. Understanding them is important since the calibrated ADC output depends on the correction parameters. Even small disturbances in those parameter could result in large performance degradation.

7.5.4 Digital Output Resolution

In this section, we will establish the relationship between the ADC resolution and the correction parameters. Based on the relationship, we can find the upper bonds of the variances of p_1 and p_3 so as to select the corresponding μ_1 and μ_3, achieving an optimum balance in the ADC output accuracy and the calibration time. With the accuracy requirement of the ADC, i.e., the errors arising from the residue amplifier must be within 1/2 LSB of the backend ADC, we have the following requirement

$$\sigma_{p_3}\frac{\partial e}{\partial p_3} \leq \frac{1}{2}L_3 LSB_{backendADC}, \tag{7.27}$$

where e represents the digital inverse function described by (5.11) and L_3 is the allocated error budged of the nonlinear gain error correction. Observing the $e(D_b)$ in (7.27), the worst case occurs when $D_b \cong 1/2V_{ref}$ in (5.11) during steady-state because $e(D_b)$ needs to compensate for large errors at this moment. Under this condition, taking the partial derivative of p_3 gives

$$\begin{aligned}\frac{\partial e}{\partial p_3} = &\frac{-1}{\sqrt{\frac{-3}{p_3}}}\cos\left[\frac{\pi}{3}+\frac{1}{3}\cos^{-1}\left(\frac{9}{4\sqrt{\frac{-3}{p_3}}}\right)\right]\frac{1}{p_3^2}\\ &-\frac{1}{p_3}\sin\left[\frac{\pi}{3}+\frac{1}{3}\cos^{-1}\left(\frac{9}{4\sqrt{\frac{-3}{p_3}}}\right)\right]\frac{1}{\sqrt{16+27p_3}}.\end{aligned} \tag{7.28}$$

Eq. (7.28) is still a nonlinear function of p_3 and D_b. Hence, we use a numerical approach as shown by Fig. 7.4, where $L_3 = 1$, rather than an analytical one. This avoids solving complex nonlinear equations. A further derivation of this nonlinear equation is beyond the scope this thesis. The intersection of the sensitivity line and the quantization level of backend ADC sets the upper bond of σ_{p_3} for the required resolution. If D_1 is multiplied by p_1 instead of D_b being divided by p_1 in the recombination logic, the accuracy requirement of the ADC becomes

$$\sigma_{p_1}\delta \leq \frac{1}{2}L_1 LSB_{totalADC}, \tag{7.29}$$

where δ is the quantization level of the sub-ADC in the first stage and L_1 the allocated error budged of the linear gain compensation. According to (7.27) and (7.29), we can obtain the upper bonds of μ_1 and μ_3 according to the allocated tolerable σ_{p_1} and σ_{p_3}.

7.5.5 Analog Circuit Imperfection

Above equations are built in the absence of circuit imperfections such as mismatched capacitor array in the sub-DAC, offsets in the sub-ADC, etc. Among these non-idealities, capacitors mismatch in the sub-DAC may largely affect the calibration results because it results in the mismatches between V_{d1} and V_{d2}.

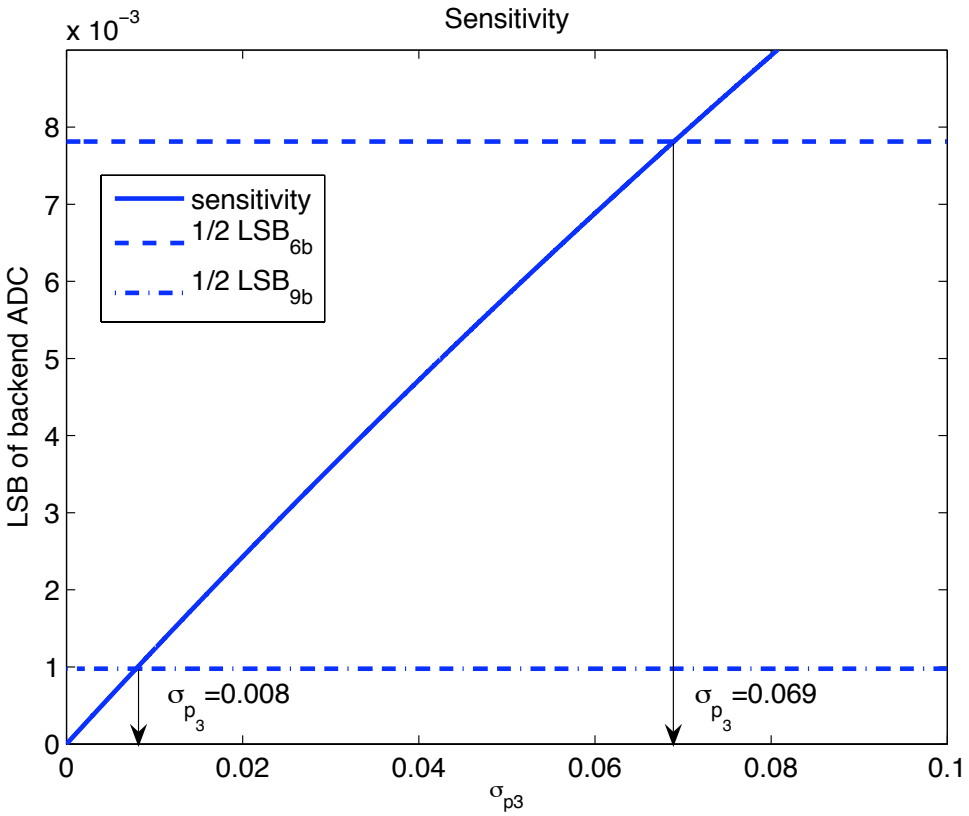

Figure 7.4: Sensitivity of σ_{p_3}.

Let α stand for the mismatch with respect to V_{d2}, that is, $V'_{d2} = V_{d2} + \alpha$. Substituting V'_{d2} into (6.1) while keeping V_{d1} ideal, then

$$\begin{aligned} D_{b2} = {} & a_1(-\varepsilon_a - R_2V_{d2} - R_2\alpha) \\ & + a_3(-\varepsilon_a^3 - 3\varepsilon_a^2R_2V_{d2} - 3\varepsilon_a^2R_2\alpha - 3\varepsilon_aV_{d2}^2 \\ & - 6\varepsilon_a\alpha V_{d2} - 3\varepsilon_a\alpha^2 - R_2V_{d2}^3 - 3R_2V_{d2}^2\alpha - 3R_2V_{d2}\alpha^2 - R_2\alpha^3). \end{aligned} \tag{7.30}$$

Multiplying D_{b2} by R_2 gives

$$\begin{aligned} R_2D_{b2} = {} & a_1(-R_2\varepsilon_a - V_{d2} - \alpha) \\ & + a_3(-R_2\varepsilon_a^3 - 3\varepsilon_a^2V_{d2} - 3\varepsilon_a^2\alpha - 3R_2\varepsilon_aV_{d2}^2 \\ & - 6R_2\varepsilon_a\alpha V_{d2} - 3R_2\varepsilon_a\alpha^2 - V_{d2}^3 - 3V_{d2}^2\alpha - 3V_{d2}\alpha^2 - \alpha^3). \end{aligned} \tag{7.31}$$

According to the above equation, the correlation of R_2 and D_{b2} becomes

$$\begin{aligned} E[R_2D_{b2}] = {} & \underbrace{a_1(-V_{d2}) + a_3(-3\varepsilon_a^2V_{d2} - V_{d2}^3)}_{\text{original term}} \\ & \underbrace{+a_1(-\alpha) + a_3(-3\varepsilon_a^2\alpha - 3V_{d2}^2\alpha - 3V_{d2}\alpha^2 - \alpha^3)}_{\text{error term}}. \end{aligned} \tag{7.32}$$

In the second line of (7.32), $a_1(-\alpha)$ is much larger than the second term such that it dominates the total error. Since $\varepsilon_3 = E[R_1D_{b1}] - E[R_2D_{b2}]$ and (6.5), the deviation Δp_3 is approximated as

$$\Delta p_3 \cong -\frac{2a_1\alpha}{\varepsilon_{3,ideal}} = -\frac{2a_1\alpha}{3/4a_1^3V_{d1}^3} \tag{7.33}$$

As a result, the correction parameter due to the mismatch now converges to

$$p'_3 = p_3 + \Delta p_3,$$

where p_3 is the original optimum value.

Fig 7.5 depicts the SNDR versus the mismatch of V_{d2}, where 1% in the x-axis stands for $\alpha = 0.01V_{d2}$. In the simulation, the parameter setting are describe in Table 8.1.

As can be seen, the SNDR remains above 70dB when the mismatch falls in $\pm 0.1\%$. This finding infers that the calibration still behave well if the matching is well controlled within $\pm 0.1\%$ relative error. In today's technology, this requirement is available with careful layout.

However, we may use alternative solutions to this issue. Since the correlation needs a sufficient large number of samples, dynamic element matching in the sub-DAC such as DWA [9] or others [49–53] can be used. Because the correlation is an average result, those techniques aim to make the long-term average use of each unit element in the sub-DAC the same. If taking sufficient samples, the estimation is virtually unaffected by the matching errors provided that the average error is zero.

In order to apply these techniques, the capacitor array is modified as depicted in Fig. 7.6. In this modification, we double the number of unity capacitors but keep the

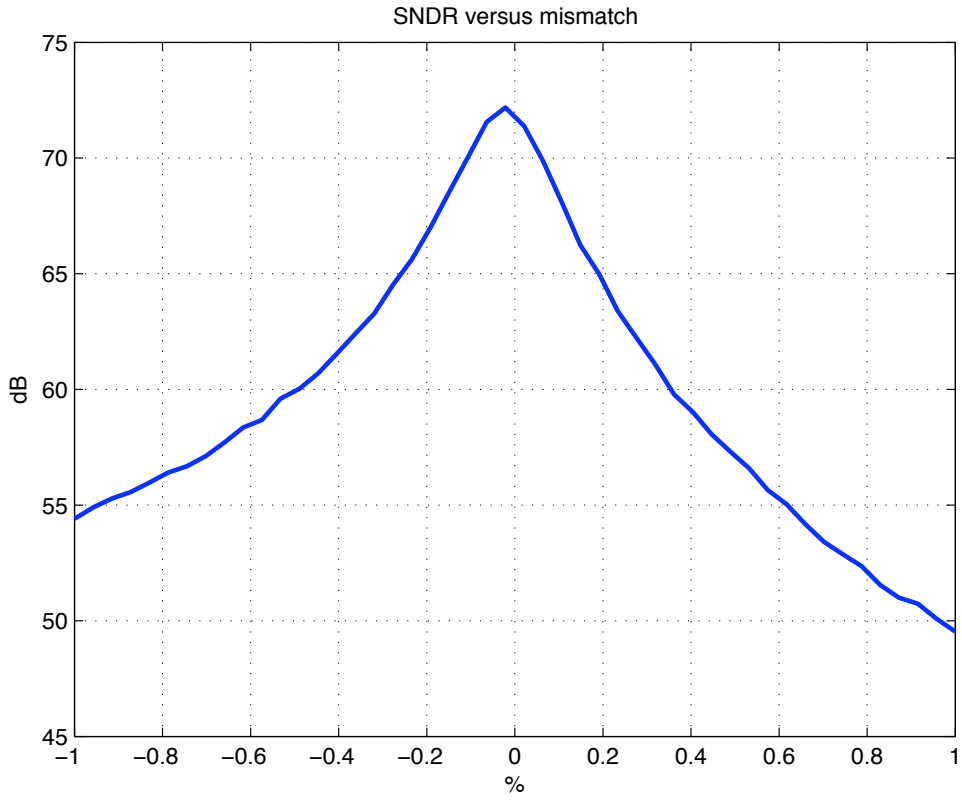

Figure 7.5: SNDR versus mismatch.

total capacitances the same as in the original configuration. Take a 2-bit sub-DAC using DWA for example. If the local conversion result $d = 2$ in cycle 1, then C_1-C_4 are selected and C_5 as well as C_6 or C_5 alone is selected depending on whether V_{d1} or V_{d2} is injected; if $d = 1$ in cycle 2 and V_{d2} is selected by RNG in cycle 1, then C_6 and C_7 are selected while C_8 and C_1 or C_8 is selected with the same reason. Observing the procedure, we select $2 \times d$ capacitors in each cycle and two or one of the following capacitors depending on the injected V_{d1} or V_{d2}. The circular selection acts as the DWA technique.

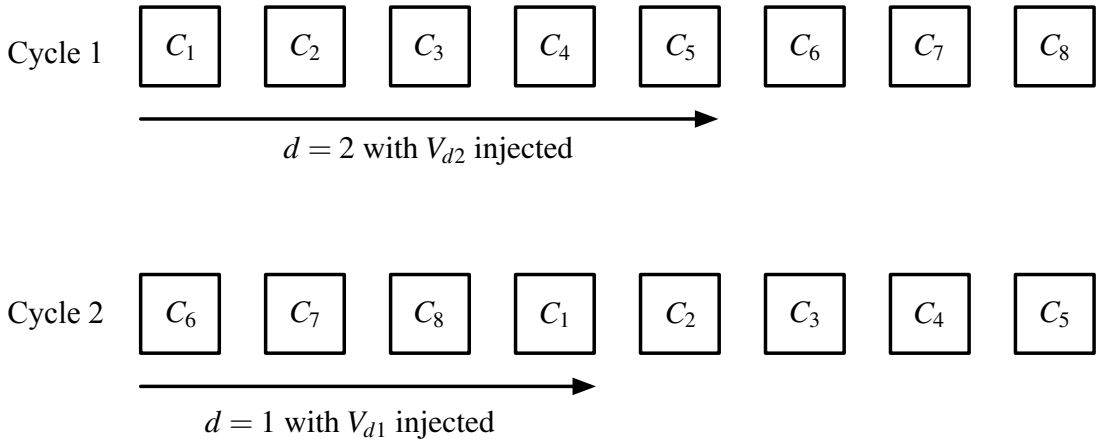

Figure 7.6: Modified capacitor using DWA [9].

Chapter 8

SIMULATION RESULTS

8.1 Simulation Setup

In this chapter, we use a behavioral model that closely resembles the pipelined ADC to validate the proposed scheme. This model uses a fully differential (3+1)-bit/stage in the first stage and then followed by ten 1.5-bit/stage stages that has an effective resolution of 9 bits. Hence, the behavioral model has a total resolution of 12 bits. The configuration in the first stage gives 1bit redundancy for the injection of random sequences. In the simulation setup, only the first stage uses the open-loop residue amplifier thus having non-perfect amplification, while the others are assumed to be ideal. An appropriate model of the residue amplifier is expressed as a third-order polynomial described by (5.3). That is

$$G_1(V_x) = a_1(V_x) + a_3(V_x)^3.$$

Table 8.1 summarizes the associated values of a_1 and a_3 as well as the design parameters.

Table 8.1: Open-looop amplifier parameters.

Parameter	Description	Value
V_{ref}	Converter reference voltage	1V
FS	Full scale range	2V
δ	quantization level in stage 1	$\delta = 1/16 = 0.0625$
a_1	Linear gain term with 5% error	7.6
a_3	Nonlinear gain term with 10% distortion in FS	-204.8

With the values listed in Table. 8.1, the corresponding amplifier model is

$$G_1(V_x) = 7.6V_x - 204.8V_x^3, \tag{8.1}$$

which leads to the correction parameter $p_{1,opt} = 7.6$ and $p_{3,opt} = -0.46654$.

8.2 Simulated ADC Performance

Fig. 8.1 and 8.2 show the converter's DNL and INL without calibration applied. As can be seen from the DNL, the nonlinear amplification results in a large number of missing codes. Its distribution also reveals errors in the non-perfect first stage. The large amount positive and negative INL is caused by these missing codes and also by the cubic error terms.

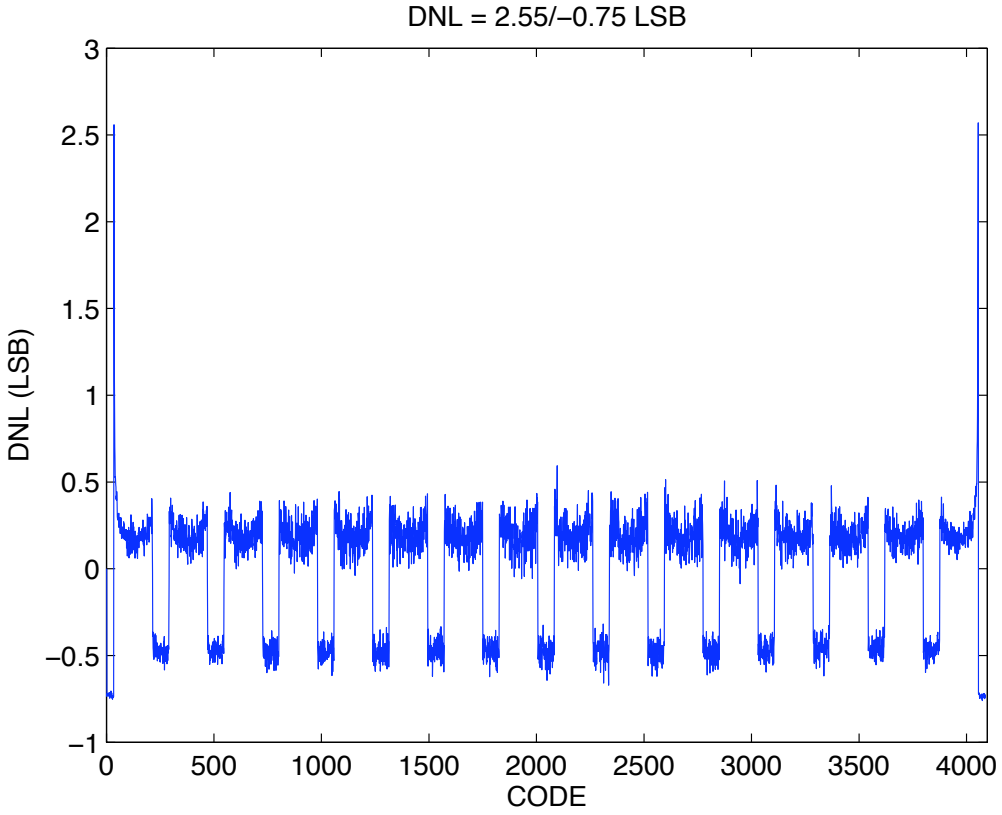

Figure 8.1: DNL without correction.

With the optimum p_1 and p_3 applied in the calibration block, we obtain the corrected DNL and INL shown in Fig 8.3, 8.4. The DNL now has no systematic error in the first stage; however, the DNL still has missing codes. This performance loss is mainly due to the fairly nonlinear amplification as well as the approximated digital inverse function (5.11) in which we have analyzed the effect that brings about to the DNL. The INL after calibration shows a significant improvement in the converter linearity from 26.5LSB to 0.66LSB. This improvement can also be seen in the frequency domain. Fig. 8.5 and 8.6 compare the results of a single tone sinusoidal input test with and without digital correction. With calibration, the ENOB improves from 6.09 to 11.7 bits, which is about 33.83dB in SNDR.

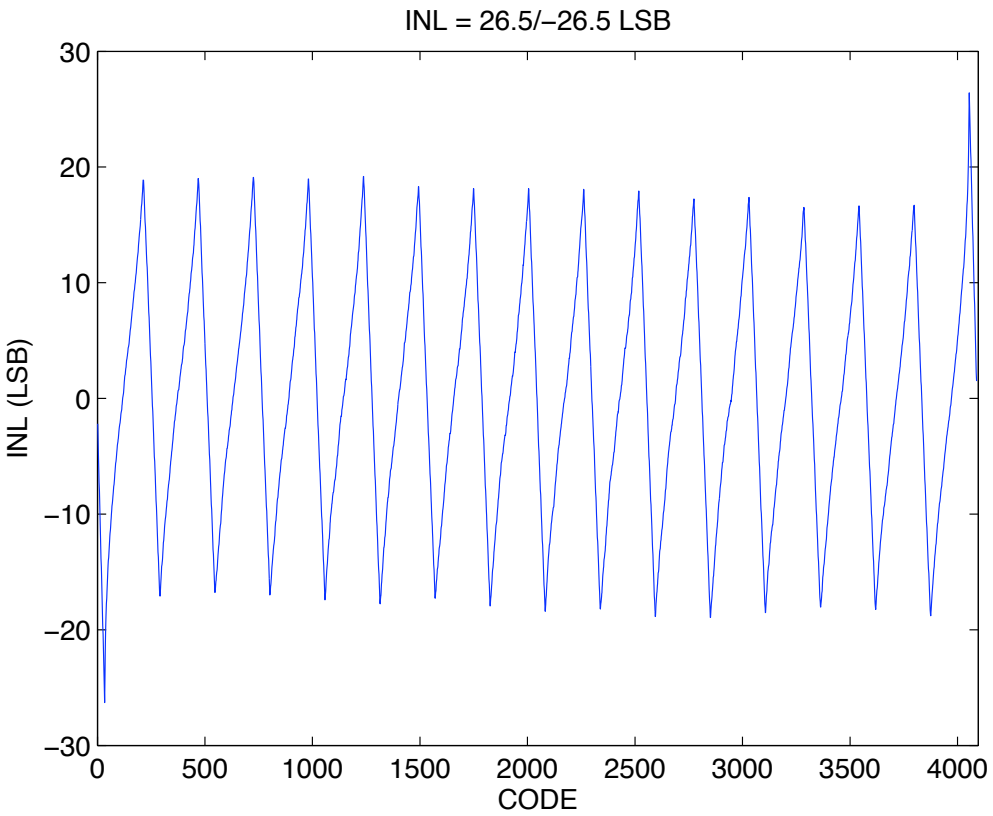

Figure 8.2: INL without correction.

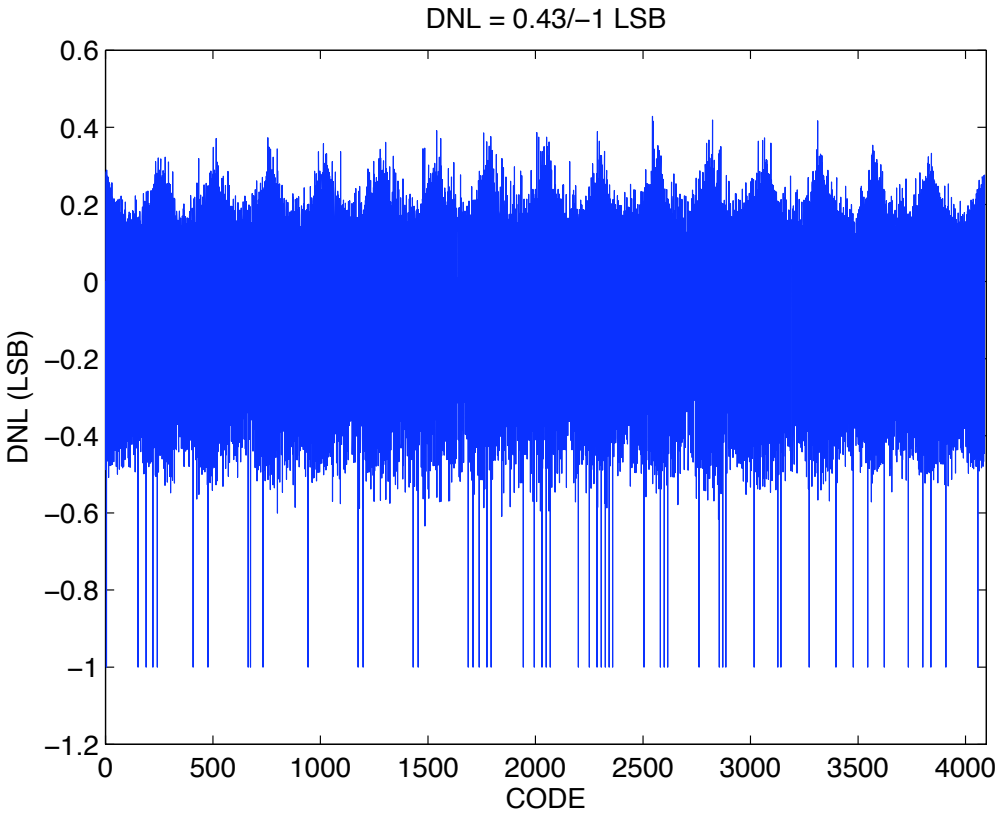

Figure 8.3: DNL with perfect adjust p_1,p_3

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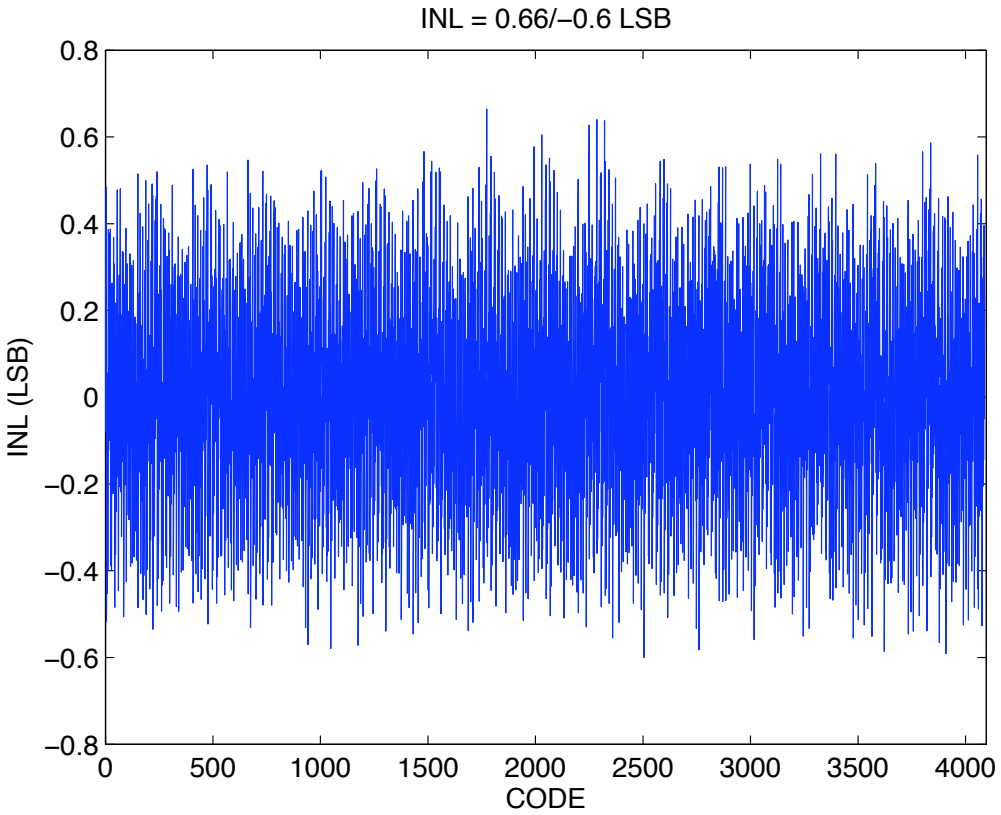

Figure 8.4: INL with perfect adjust p_1,p_3

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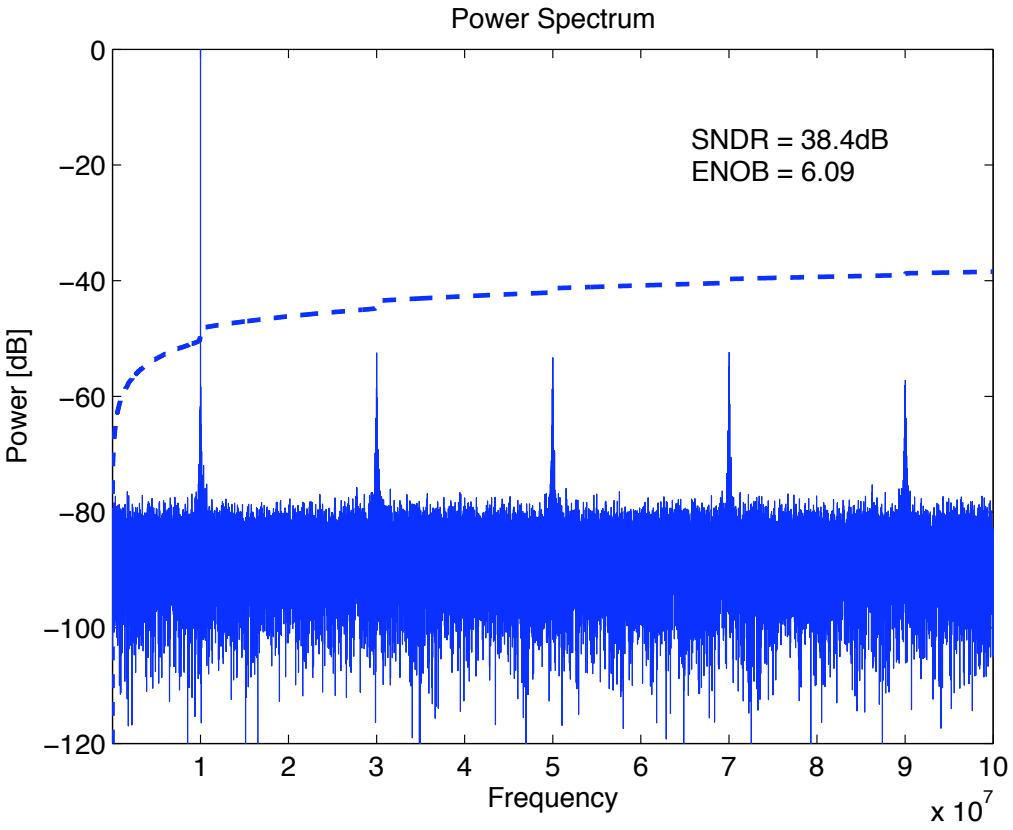

Figure 8.5: FFT without correction.

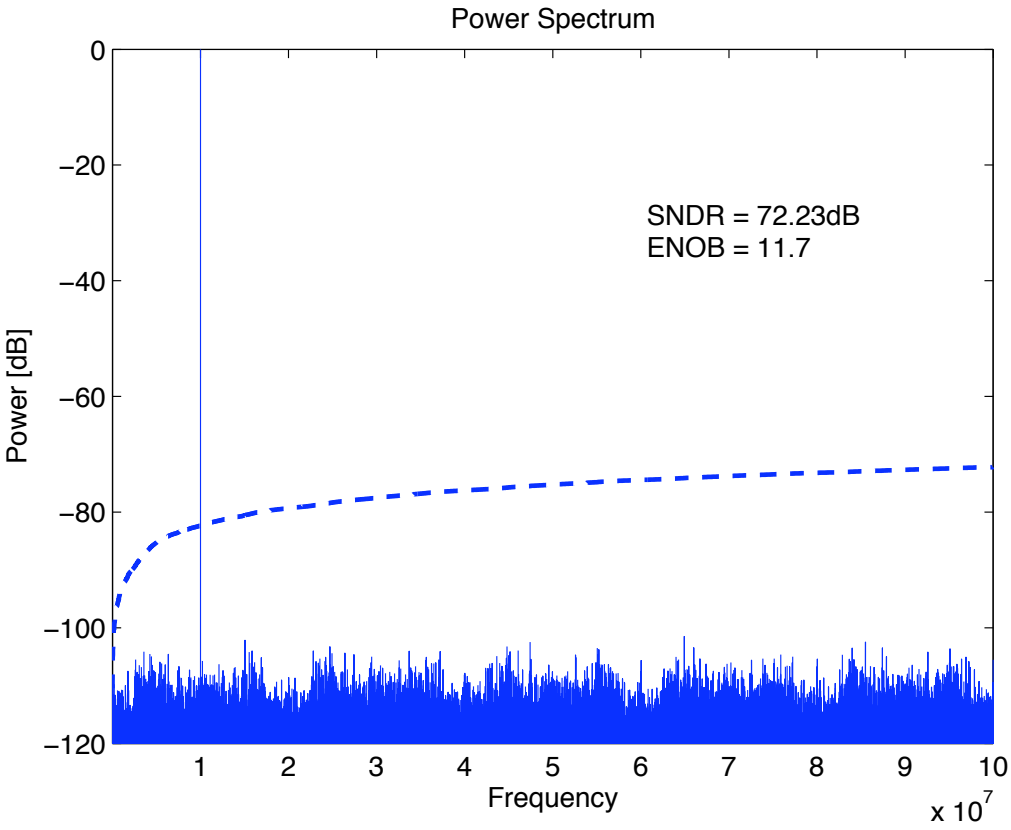

Figure 8.6: FFT with correction.

8.3 LMS Loop Simulation

In this section we include the multi-correlation estimation technique in the simulation. We allocate 50% error budgets for L_1 and 50% for L_3 at first, finding the upper bonds 0.004 for σ_{p_3} and 0.001 for σ_{p_1} according to (7.27) and (7.29). Both values help us determine the upper bonds for μ_1 and μ_3 respectively. Selecting $\gamma_1 = 3$ in (7.8) gives the number of samples for the estimation of ε_1 is 14. It is not reasonable because the ADC accuracy requirement dominates in determining the number of samples for estimating ε_1 in the LMS loop. With the help of chapter 7, we obtain the loop parameters summarized in Table. 8.2.

Table 8.2: LMS Loop Parameters.

Step Size	Time Constants
$\mu_1 = 3.04$	$\tau_1 = 1.02 \cdot 10^6/fs$
$\mu_3 = 0.96$	$\tau_3 = 67 \cdot 10^6/fs$

Based on the values intended for design, we select the cycle length $N = 2^{17}$ for doing each correlation. That is, we take totally 2^{18} samples for each updates of p_1 and p_3. Fig. 8.7 and 8.8 show the parameter convergence upon startup of the converter, with a full-scaled sinusoidal input applied. Both p_1 and p_3 converge to their ideal values. The deviations of the parameters from their expected envelope are caused by the fact the two estimation loop are not orthogonal. An obvious observation is the p_1 convergence, its learning curve is not monotonic just because its learning speed is faster than p_3 while a_3 still exists. And the learning curve of p_1 will follow the envelope if the nonlinearity is totally removed.

Fig. 8.9 shows the ENOB when the parameters have settled.

The distribution of the ENOB in steady state is shown in Fig. 8.10.

8.4 Discussion

8.4.1 Summary

With the proposed scheme, Table. 8.3 summarizes the ADC performance with/without calibration.

Table 8.3: ADC Performance.

	DNL (LSB)	INL (LSB)	ENOB (bit)	SNDR (dB)
Before calibration	$2.55/-0.75$	$26.5/-26.4$	6	38.4
Calibration with the proposed scheme	$0.43/-1$	0.66/-0.6	11.52	71.1

From the table, we see a great improvement in the INL as well as the SNDR.

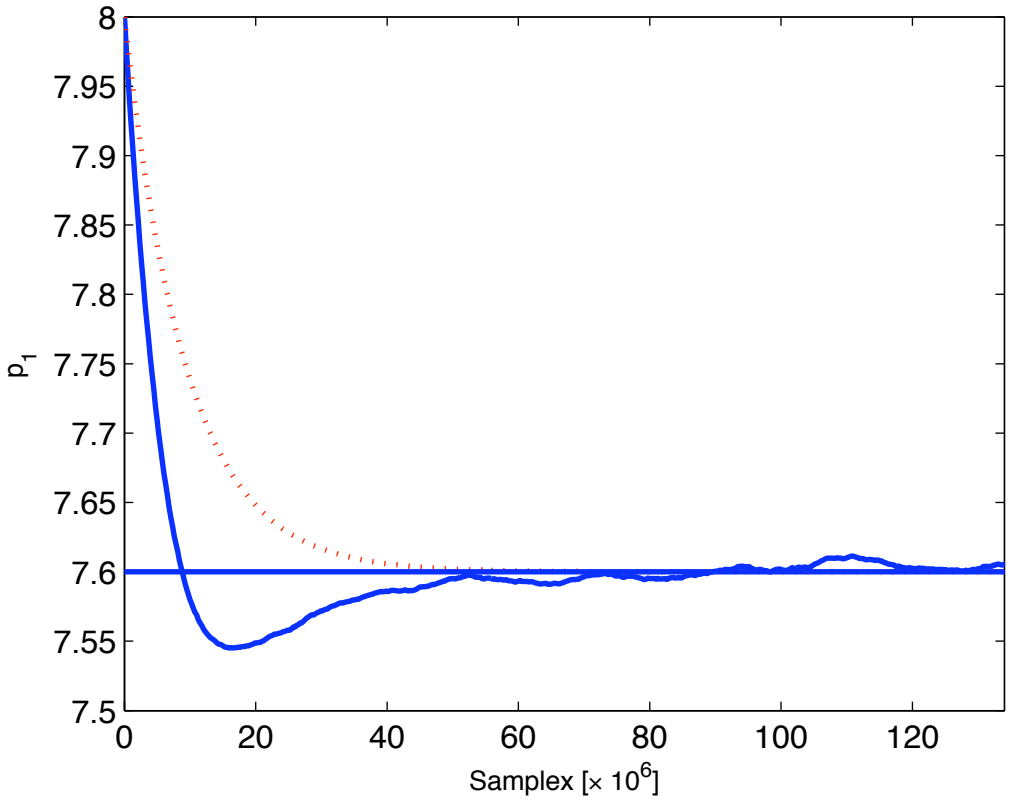

Figure 8.7: p_1 convergence.

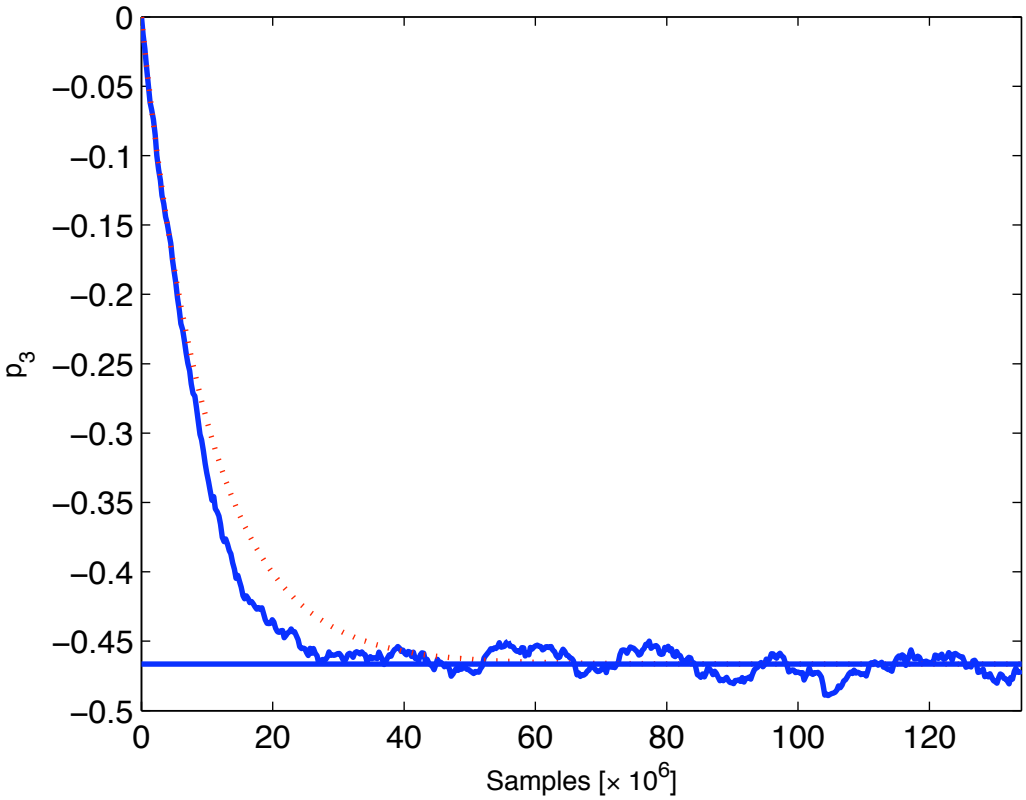

Figure 8.8: p_3 convergence.

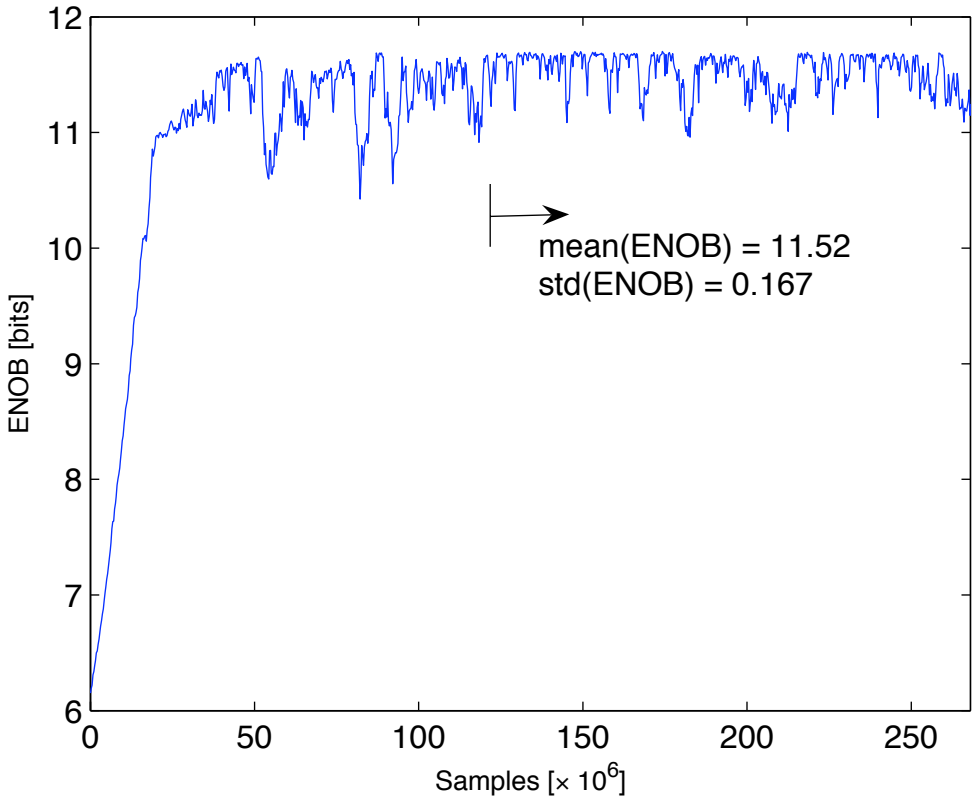

Figure 8.9: ENOB convergence.

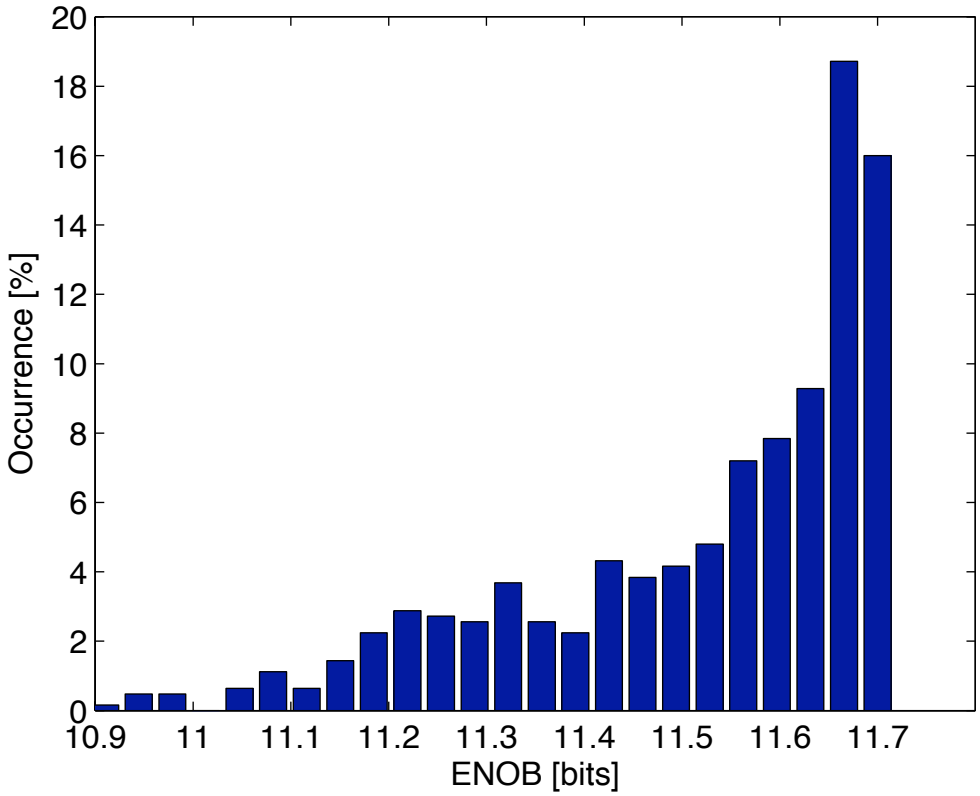

Figure 8.10: ENOB distribution.

8.4.2 Tracking Time Limitations

As we can see from the above simulation results, the statistical nature of the parameter estimation leads to fairly large tracking time. Another reason for this long tracking time is that we have used a fairly nonlinear amplifier model in our simulation. For a conversion rate of 200MS/s in a typical pipelined ADC, the time constants τ_1 and τ_3 translate to 5ms and 335ms on an absolute time scale. In cases where slow adaption cannot be tolerated, an FGEC estimation process [45] could be considered here.

Chapter 9

CONCLUSION

9.1 Summary

A novel digital background calibration scheme for multistage ADCs has been presented. This scheme can accurately estimate and calibrate the linear and nonlinear gain errors of the open-loop residue amplifier. Moreover, correction of high order nonlinear terms is also possible if more RNGs are injected. In addition, using statistical functions achieves precise estimation of the correction parameters in background without additional analog circuit. This feature makes the design of the whole ADC easy-to-implement. Because the input is served as a calibration signal, the proposed algorithm perform calibration without scheduled cycles. Compared with the similar digital background techniques discussed previously [3, 17], the proposed algorithm is favorable in many aspects, where they are summarized in Table. 9.1.

Table 9.1: Comparison

	[3]	[17]	proposed
Stimuli	uniformly distributed	stationary	stationary
Correction range	limited by analog and digital circuits	limited by algorithm	reaching theoretical maximum
Hardware cost	moderate	large	small

9.2 Suggestion on Future Works

In this thesis, we have proposed a digital background calibration scheme for multistage ADCs; as a result, an obvious future work is the pipelined ADC implementation with multi-stage calibration using this technique. Using multiple open-loop stages in the converter front-end will result in larger power saving and high conversion rate.

Other opportunities exist in exploring more efficient estimation that cancels the input signal interference in the estimation. At the same time, an optimization of this work based on the implementation in each stages could be a future research topic.

A third, more aggressive vision, is to extend the digital correction in ADCs to include dynamic, frequency dependent error. The benefits of fully digital dynamic error compensation could be revolutionary.

More generally, a similar estimation concept to analog distortion could be considered in audio, video, and other communication systems that are limited by nonlinear effects.

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