

# 分析離散式單迴路積分三角類比數位轉換器之非線性失真、雜訊與功率，以達到最佳化設計

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## 摘要

在本篇論文中，我們分析了積分三角類比數位轉換器的非線性特性所造成的失真問題，包括趨穩失真(settling distortion)和數位類比轉換器不匹配的失真..等，藉由分析推導出的失真功率以及雜訊功率，我們以訊號對雜訊和失真比(SNDR)來當作我們的設計規格，利用此規格以及功率消耗模型，我們進而可以在指定的系統規格下，做最佳化的設計。此最佳化設計意指在特定系統規格下(如頻寬、訊號對雜訊和失真比)，找到一組最佳化的設計參數，使得類比數位轉換器的功率消耗最小以及訊號對雜訊和失真比最大。我們使用訊號對雜訊和失真比當作設計規格而非訊號雜訊比(SNR)是因為，訊號對雜訊和失真比是訊號雜訊比和總諧波失真(THD)的集合，也是類比數位轉換器動態效能完整的測量。最後我們將針對已發表的設計結果來做驗證的工作。

# Nonlinear Distortion, Noise and Power Analyses of Discrete-time Single-Loop Sigma-Delta ADCs for Design Optimization

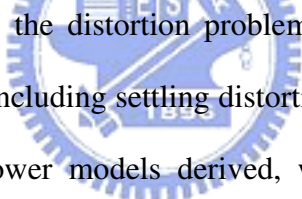
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## ABSTRACT



In this work, we analyse the distortion problems resulting from the nonlinear characteristic of  $\Sigma\Delta$  ADCs, including settling distortion and DAC distortion, etc. By these distortion and noise power models derived, we utilize Signal-to-Noise and Distortion Ratio (SNDR) as our design specification. Utilizing this specification and power consumption model, we can forward to do design optimization under the specific specifications. Design optimization means that under the specific specifications (signal bandwidth, SNDR), we find a set of optimal design parameters such that the power consumption of ADCs is minimum and SNDR is maximum. We use SNDR instead of SNR as our specification because SNDR is a combination of the SNR and the THD specifications and it is an overall measure of ADC dynamic performance. Finally, design optimization is tested against a published design result.

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# List of Symbols

## Symbols

$V_{LSB}$	Quantizer step size
OSR	OverSampling Ratio
$n$	Order of the Sigma-Delta modulator
$B$	Number of bits in the quantizer
$f_s$	Sampling Frequency
$f_B$	Signal Bandwidth
$V_{ref}$	Reference Voltage of the quantizer
$A$	Gain of OTA
$f_{in}$	Frequency of the input signal
$\phi_i$	$i$ th phase of a nonoverlap clock
$A_{in}$	Amplitude of input signal
$\sigma_{jit.}$	standard deviation of clock jitter
$C_s$	Sampling capacitor
$C_I$	Integrating capacitor
$C_L$	Load capacitor of OTA
$V_s$	Input signal plus feedback DAC signal
$\tau_1$	Time constant of input branch
$\sigma_{vs}$	Standard deviation of $V_s$
$\tau_2$	Time constant of integrator output settling
$a_i$	gain coefficient of $i$ th integrator
$\eta$	percentage of the bottom plate parasitic
$T$	Absolute temperature
$R$	Switch ON resistance
$N$	quantizer levels
gm1	Amplifier transconductance
Pr()	Probability of some condition

$\sigma_{cap.}$	Mismatch of unit capacitance
$k$	Boltzmann's constant ( $1.38 \times 10^{-23}$ ) J/K
$\alpha$	OTA noise factor
$Erf[]$	Error Function



# Lists of Tables

Table 4.1	Standard deviations of $V_s$ vs. different quantizer bit numbers	37
	.....	
Table 5.1	Minimum $SR$ and $GBW$ required w. r. t. $OSR$	55
	.....	
Table 5.2	Simulation results of standard deviation of capacitor mismatch vs. unit DAC number with $A_m=1$	64
	.....	
Table 5.3	Theoretical results of standard deviation of capacitor mismatch v.s. unit DAC number with $A_m=0.5$	64
	.....	
Table 5.4	Simulation results corresponding to Table 5.3	65
	.....	
Table 6.1	Summary of noise and distortion power and power-rating when design parameters increase	73
	.....	
Table 7.1	Comparisons of our design results and those in [Gag 03] with different $K$	77
	.....	
Table 7.2	the corresponding noise and distortion powers for the design parameters listed in Table 7.1	79
	.....	
Table 7.3	Listing the details of power consumption.	79
	.....	

# Lists of Figures

Fig. 2.1 (a) Original signal spectrum	6
(b) Sample function when $f_s > 2f_B$	
(c) Signal spectrum that is sampled by (b)	
(d) Sample function when $f_s < 2f_B$	
(e) Signal spectrum that is sampled by (d).....	6
Fig. 2.2 Quantization process .....	7
Fig. 2.3 Quantization error caused by A/D converter .....	7
Fig. 2.4 Quantization error range .....	8
Fig. 2.5 P.D.F of quantization error .....	8
Fig. 2.6 Sampling system .....	10
Fig. 2.7 Noise distribution after sampling .....	10
Fig. 2.8 (a) General $\Sigma\Delta$ modulator	
(b) Linear model with quantization noise .....	11
Fig. 2.9 Noise shaping .....	13
Fig. 3.1 Block diagram of $\Sigma\Delta$ A/D converter. ....	14
Fig. 3.2 First-order $\Sigma\Delta$ modulator .....	15
Fig. 3.3 Single-loop second order $\Sigma\Delta$ modulator .....	17
Fig. 3.4 Comparison of noise shaping techniques .....	18
Fig. 3.5 Single-loop high order $\Sigma\Delta$ modulator .....	19
Fig. 3.6 Four-order interpolative architecture .....	19
Fig. 3.7 2-1 architecture MASH $\Sigma\Delta$ modulator .....	20
Fig. 3.8 SNR vs. OSR with different quantizer bit number .....	22
Fig. 3.9 Multi-bit architecture .....	23
Fig. 3.10 A B-bit DAC with DEM technique .....	24

Fig. 3.11 Operation principle of the DWA algorithm .....	25
Fig. 3.12 Output spectrum with three kinds of DAC .....	26
Fig. 3.13 Comparison of $\Sigma\Delta$ modulator architectures .....	27
Fig. 3.14 Performance characteristic of a $\Sigma\Delta$ converter .....	29
Fig. 4.1 Integrator and the DAC branches.....	30
Fig. 4.2 Equivalent circuits of sampling and integration phases.....	33
Fig. 4.3 A bandgap voltage reference circuit.....	34
Fig. 4.4 Equivalent circuit while considering reference voltage noise.....	34
Fig. 4.5 Switched capacitor integrator diagram	
(a) Sampling phase	
(b) Integration phase .....	35
Fig. 4.6 Simulated results of $V_s$ distribution .....	36
Fig. 4.7 Three types of settling conditions in integration phase.....	38
Fig. 4.8 Comparison of our theoretical result with behavior simulation result .....	40
Fig. 4.9 Main nonidealities sources in the $\Sigma\Delta$ modulator .....	44
Fig. 5.1 3D plot of (5.5) .....	49
Fig. 5.2 Spectrum of $V_s$ with different quantizer bit number .....	52
Fig. 5.3 Output spectrum of a second-order $\Sigma\Delta$ modulator with harmonic distortion.....	53
Fig. 5.4 $20\log \alpha_3 $ vs. $SR$ .....	54
Fig. 5.5 $20\log \alpha_3 $ vs. $GBW$ .....	55
Fig. 5.6 PSD of second-order $\Sigma\Delta$ modulator with 5 quantization levels .....	57
Fig. 5.7 A block diagram of a B-bit flash DAC .....	58
Fig. 5.8 (a) Ideal DAC	
(b) DAC with mismatch .....	59
Fig. 5.9 DAC transfer curve:	
(a) DAC with larger DAC output error	



(b) DAC with smaller DAC output error .....	60
Fig. 5.10 DAC transfer curve:	
(a) DAC with smaller output level	
(b) DAC with larger output level .....	60
Fig. 5.11 Simulation results of DAC harmonic distortion.....	63
Fig. 5.12 HD2 vs. std. of mismatch with 3 Bit DAC and $A_m = 0.2$ .....	65
Fig. 5.13 HD2 vs. DAC output level with std. = 0.04% and $A_m = 0.2$ .....	66
Fig. 5.14 Switched-capacitor integrator .....	69
Fig. 6.1 Proposed design optimization for the $\Sigma\Delta$ modulator design .....	74



# Contents

中文摘要 .....	I
English Abstract .....	II
List of Symbols .....	IV
Lists of Tables .....	VI
Lists of Figures .....	VII
Contents .....	X
Chapter 1 Introduction .....	1
1.1 Current Status and Background .....	1
1.2 Motivation and Aims .....	1
1.3 Organization .....	3
Chapter 2 Fundamental Theorems of Sigma-Delta Modulators .....	5
2.1 Nyquist Sampling Theorem .....	5
2.2 Quantization Noise and Peak SNR .....	7
2.3 Techniques of Sigma-Delta Modulator .....	9
2.3.1 Oversampling Technique .....	9
2.3.2 Noise shaping .....	11
Chapter 3 Architectures of Sigma-Delta Modulator .....	14
3.1 First-Order Sigma-Delta Modulator .....	15
3.2 Single-Loop Second-Order Sigma-Delta Modulator .....	17
3.3 Single-Loop High Order Sigma-Delta Modulator .....	18
3.4 Interpolative Sigma-Delta Modulator .....	19
3.5 MASH Architecture .....	20
3.6 Multi-bit Quantizer Sigma-Delta Modulator .....	21
3.7 Multi-bit Sigma-Delta Modulator use DEM Technique .....	23

3.7.1 Randomization Technique .....	24
3.7.2 Data Weighted Averaging (DWA) .....	25
3.8 Decimator .....	27
3.9 Performance Metrics for a $\Sigma\Delta$ Modulator .....	28
Chapter 4 Models of Sigma-Delta Modulator Noises and Power .....	30
4.1 Finite OTA Gain Error .....	31
4.2 Thermal noise (Switch, OTA, Reference circuits) .....	31
4.3 Settling Problem .....	34
4.4 Multi-bit DAC noise .....	41
4.5 Clock Jitter Effects .....	43
4.6 Relative Power Model .....	44
Chapter 5 Models of Sigma-Delta Modulator Nonlinear Distortion .....	47
5.1 Settling Distortion .....	47
5.2 Quantizer Nonlinearity Distortion .....	56
5.3 Multi-bit DAC Distortion .....	57
5.4 Nonlinear Op-amp Gain Distortion .....	66
5.5 Nonlinear Capacitances Distortion .....	67
5.6 Nonlinear Switch Resistance Distortion .....	68
Chapter 6 Design Optimization of Sigma-Delta ADCs Design .....	71
6.1 Design Parameters Discussions .....	71
6.2 Design Optimization .....	73
Chapter 7 Simulation Results .....	76
Chapter 8 Conclusions and Future Works .....	80
References .....	81