1
Introduction

1.1 Current Status and Background

Sigma-Delta A/D converters have become popular for high-resolution medium-to-low-speed applications such as digital audio [Bos 88][Nor 89], voice codec, and DSP chip. Recently, ΣΔ ADCs have been applied to higher bandwidth signals, and low power designs are frequently emphasized. For example, in ×DSL [Gag 03][Rio 04] applications, signals up to several MHz must be handled. Since significantly increasing the sampling rate is difficult, designers either seek to increase the order or the cascade stages [Oli 02][Vle 01], or employ multi-bit quantization [Gri 02][Mil 03], or both, in order to achieve the required dynamic range. DAC linearity can be improved due to process technology advances, making the multi-bit architecture more popular. The ΣΔ modulator design is a complex and time consuming process because many coupled design parameters must be determined. Coming up with an acceptable design is very challenging with increasing design specification demands, previously described. Even an acceptable design may not be the best one. We propose an optimization approach to increase automation and reduce complexity in the single-loop ΣΔ ADCs design.

1.2 Motivation and Aims

To propose the design optimization for single-loop ΣΔ modulators, we need a complete set of important nonideality models and the power consumption model. Some issues concerning ΣΔ modulator noise and error modeling appeared in [Bos 88][Nor 89][Mal 03]. The performance of the ΣΔ ADCs is usually expressed in

terms of SNR and SNDR. Circuit designers must take into consideration the nonidealities and decide the circuit and system parameters to meet the desired specifications. A design optimization procedure is proposed in [Chu 05] to meet design specifications while minimizing power consumption. However, it didn't consider the nonlinear distortions, so that the effectiveness of the proposed design optimization is limited. In this work, we discuss all the important nonlinear distortions, and incorporate relevant distortion powers into the optimization process in order to achieve more realistic designs.

In a $\Sigma\Delta$ modulator, common causes for harmonic distortions are nonlinear op-amp gain, settling error, nonlinear capacitances, quantizer nonlinearity, nonlinear switch resistance and unit-DAC mismatch. Operational amplifiers (op-amps) are the critical part of the $\Sigma\Delta$ modulators and its nonidealities such as nonlinear op-amp gain and settling error may produce distortions significantly. Some analyses of the distortions resulting from nonlinear op-amp gain and settling error are given in [Med 94][Dia 94]. In [Med 94], the settling distortion has been modeled. However, the model provides little insight on how settling distortion are related to circuit and system parameters and it had a mistake. In this work, we correct this mistake and discuss the harmonic distortion how to vary with circuit and system parameters and what condition it can be ignored. Then we will apply the model and discuss to our design optimization.

Recently, with the advanced technology, multi-bit modulators are used often because it offers many advantages. However, multi-bit modulators can introduce significant distortion into the modulator loop due to the unit-DAC mismatch. Any error in the DAC response will be directly subtracted from the input signal and hence it appears at the output without the benefit of noise shaping. Therefore any nonlinearity of the DAC will introduce a corresponding nonlinear signal distortion into the overall ADC response. Some analyses about DAC nonlinearity appeared in

[Stu 01][Bru 99]. The derived distortion models in [Stu 01][Bru 99] are not expressed in harmonic power forms, and the relations between circuit parameters and distortion powers are not clear. In this work, we derive the harmonic distortions in terms of quantization level and standard deviation of capacitor mismatch, and the distortion model can help us do design optimization to determine the quantizer output level.

One straightforward approach to improve the accuracy of the internal DAC is to improve the matching of the individual elements. The most common approach for improving the accuracy of a DAC is dynamic element matching (DEM). Many dynamic element matching algorithms have been proposed to convert the static error into a wide-band noise signal [Bai 01][Kuo 95][Car 89]. ΣΔ modulators using DEM can reduce the distortion but it increases the extra hardware and consumes more power. In this work, the effects of DEM on distortion and power consumption are also considered for our design optimization.

These nonidealities described above are important when the specifications of the modulator are demanding because they can become the dominant error sources. In this work, we have the noise and distortion models of all important nonidealities and power consumption model for design optimization. The design of ΣΔ modulators is a complex and time consuming process. With these models for design optimization, we can increase the automation and reduce complexity in the single-loop ΣΔ ADCs design.

1.3 Organization

This work is organized as follows. In Chapter 2 and Chapter 3, systematic studies of fundamental theory and various architectures of ΣΔ modulator are presented first. In Chapter 4, analyses of several errors which may degrade system performance are proposed, and the power consumption model is derived. In Chapter 5, analyses of

several distortions are proposed. A design optimization scheme is proposed in Chapter 6. It essentially combines system and circuit level designs, and optimizes all design parameters at the same time. The optimization scheme is verified in Chapter 7, and various issues are discussed. Conclusions and future works are presented in Chapter 8.

2
Fundamental Theorems of Sigma-Delta Modulators

Before we establish the error models of ΣΔ modulators, several important theorems and concepts must be known, such as Nyquist sampling theorem, quantization error and the two most critical techniques in a ΣΔ modulator: oversampling and noise shaping. All topologies of ΣΔ modulators are based on these two techniques. There also have some parameters we must to understand, such as OSR, SNR, and SNDR …etc. This chapter starts from fundamental theorems, and introduces several topologies of ΣΔ modulators.

We will illustrate quantization error and analyze quantization noise in an ideal A/D converter and then derives the peak signal-to-noise ratio. The resolution of an A/D converter is determined by signal-to-noise ratio, which is a very important specification in an A/D converter.

2.1 Nyquist Sampling Theorem

In an analog-to-digital converter, the analog signal from external environment must be converted to discrete-time signal by sampling. However, the sampling rate (fs) and signal bandwidth (f_B) must follow the Nyquist sampling theorem in (2.1):

$$f_S \geqq 2f_B \qquad (2.1)$$

The sampling rate must be higher or equal to twice of signal bandwidth in order to prevent from aliasing. We will illustrate the phenomenon of aliasing by Fig. 2.1. Fig. 2.1(a) and (b) are the spectrums of signal and sample function respectively; from fig. 2.1(c), when sampling rate is twice higher than signal bandwidth, the signal after

sampling has no aliasing and it can be perfectly reconstructed by using low pass filters. However, in Fig. 2.1(d), when the sampling rate is lower than twice of signal bandwidth, aliasing will appear in the signal after sampling. The signal having aliasing is difficult to reconstruct to original signal [Mach 96], like Fig. 2.1(e).

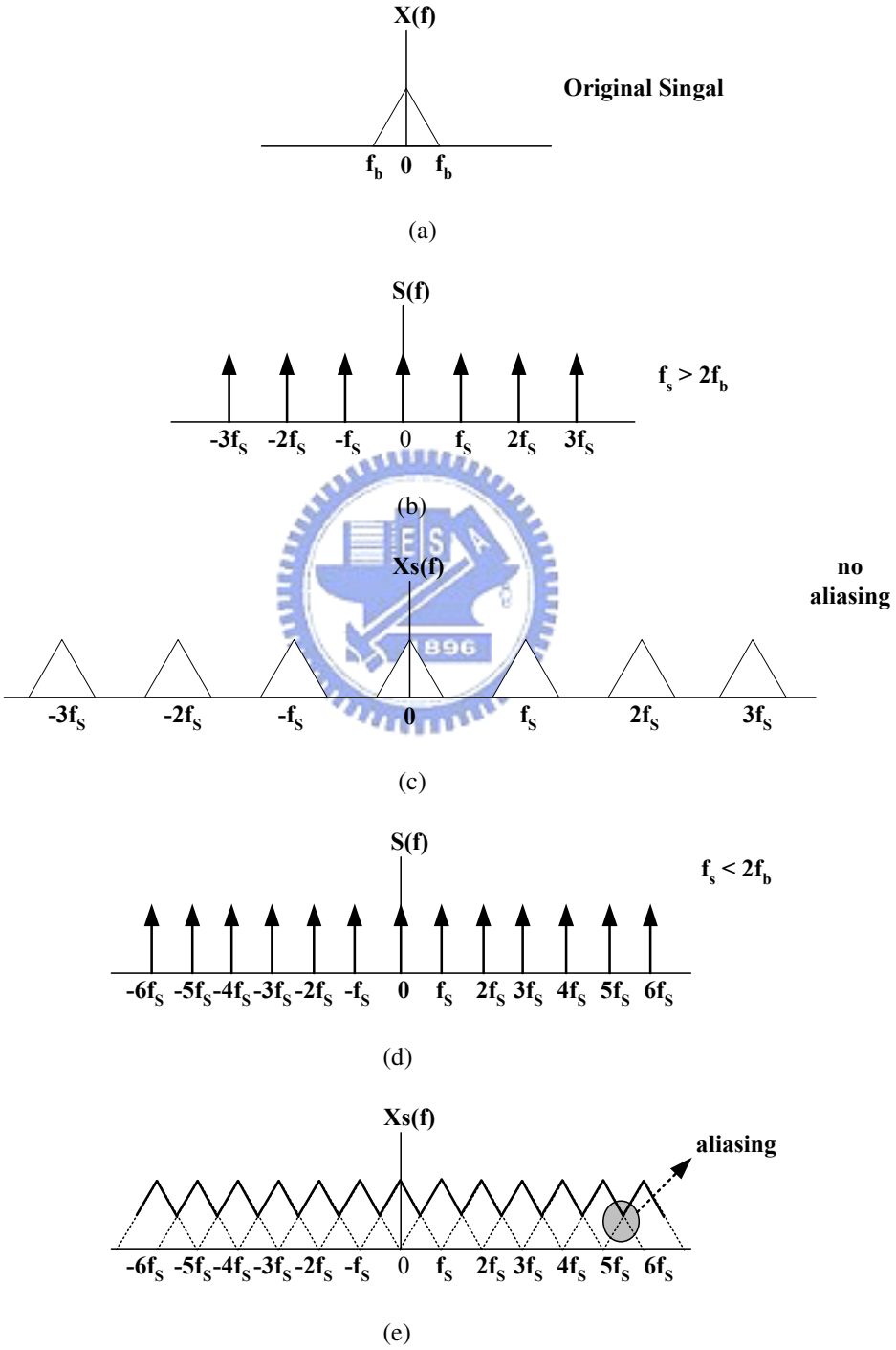


Fig. 2.1（a）Original signal spectrum（b）Sample function when fs > 2fB（c）Signal spectrum that' sampled by (b)（d）Sample function when fs < 2fB（e）Signal spectrum that sampled by (d)

2.2 Quantization noise and Peak SNR

We can get a discrete-time signal by sampling a continuous-time signal, and this sampled signal can be converted to digital signal. Quantization will appear in this process, the basic concept of quantization is to classify the original signal to different levels according to its level to determine the bit number of this signal, as shown in Fig. 2.2.

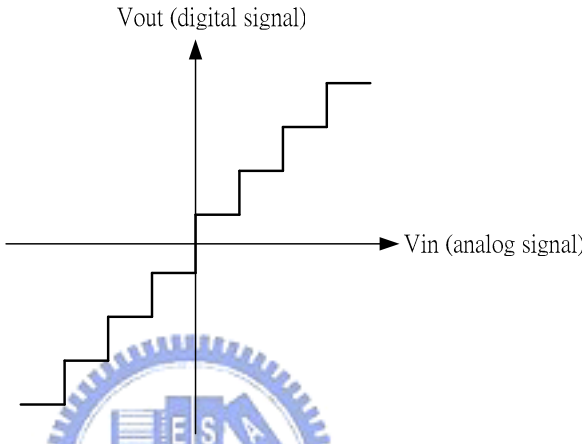
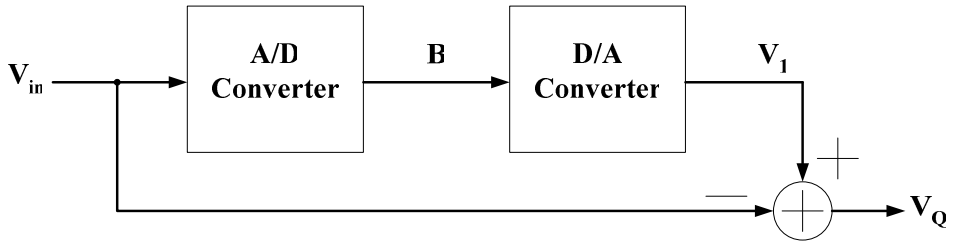


Fig. 2.2 Quantization process

It will have quantization error even in an ideal analog-to-digital converter. As shown in Fig .2.3, we convert the digital signal B to analog signal V_1 by a D/A converter, and then the signal V_1 is subtracted by input signal Vin. The result is the quantization error V_Q, as in (2.2) [Joh 97].

$$V_Q = V_{in} - V_1 \qquad (2.2)$$



Quantization noise $V_Q = V_{in} - V_1$

Fig. 2.3 Quantization error caused by A/D converter

The range of quantization error is limited in $\pm V_{LSB}/2$ (as in Fig. 2.4), and we assume the probability density function of quantization error is uniformly distributed between $\pm V_{LSB}/2$ and its mean is zero, as shown in Fig. 2.5. From this assumption, we can easily get the quantization noise power $V_{Q(rms)}^2$ in (2.3).

$$V_{Q(rms)}^2 = \int_{-\infty}^{\infty} x^2 \cdot f_Q(x) \cdot dx = \frac{1}{V_{LSB}} \int_{-VLSB/2}^{VLSB/2} x^2 \cdot dx = \frac{V_{LSB}^2}{12} \qquad (2.3)$$

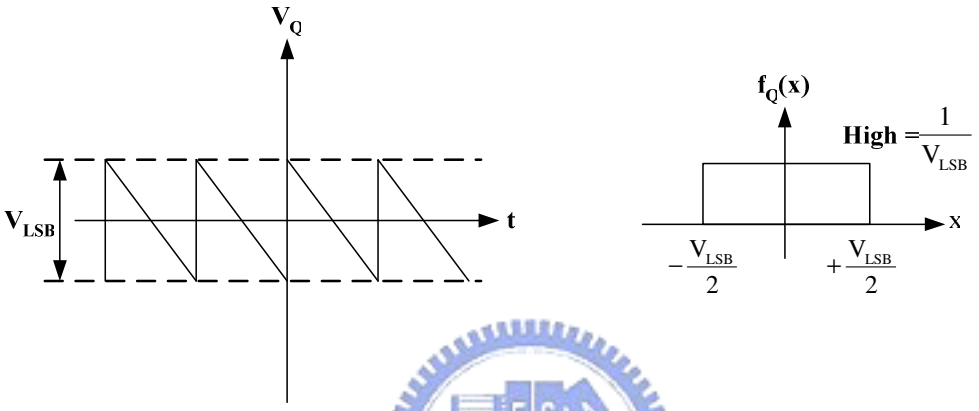


Fig. 2.4 Quantization error range　　Fig. 2.5 P.D.F of quantization error

From (2.3) we can know the quantization noise power is proportional to square of V_{LSB}, and V_{LSB} can be represented as in (2.4). Therefore, we can say that the quatization noise will reduce by increasing quantization bit number.

$$V_{LSB} = \frac{FS}{2^B} \qquad (2.4)$$

FS=Full scale = $V_{ref+} - V_{ref-}$　　B：Quantization bit number

Assume that input signal is sinusoidal, expressed as $V_{in}(t) = A \sin\omega t$, so the input signal power $V_{in(rms)}^2$ is as （2.5）. In （2.5）, we define the amplitude of input signal is the full scale of reference voltage, and from (2.3), (2.4) and (2.5), the peak SNR(Peak Signal-to-Noise Ratio) can be derived as in (2.6).

$$V_{in(rms)}^2 = \frac{1}{T} \int_{-T/2}^{T/2} (A \cdot \sin \omega t)^2 \cdot dt = \frac{A^2}{2} = \frac{(2A)^2}{8} = \frac{FS^2}{8} \qquad (2.5)$$

$$PSNR = 10 \log \left(\frac{V_{in(rms)}^2}{V_{Q(rms)}^2} \right) = 6.02B + 1.76 \text{ dB} \qquad (2.6)$$

(2.6) is the result obtained by Nyquist sampling rate. From (2.6), we can know that each additional bit number in quantizer increases 6dB in SNR. In Nyquist A/D converters, increasing the resolution of quantizer (decrease V_{LSB}) while reducing the quantization noise is a general method to reach higher SNR, but this method is sensitive to mismatches of analog device. Therefore, the general Nyquist A/D converter is not easily to implement with high resolution.

2.3 Techniques of Sigma-Delta Modulator

ΣΔ A/D converters are based on oversampling and noise shaping to reach high resolution. Oversampling means the sampling rate is much higher than Nyquist rate, about 8~512 times in general applications. The goal of oversampling is to expand quantization noise to wider range. It can reduce the quantization noise in signal bandwidth and increase the DR (Dynamic range) of input signal. Noise shaping is a technique that moves noise to high frequency, which is done by using discrete time filter and feedback technique. After noise shaping, the noise in high frequency can be filtered out by a digital filter [Nor 97].

2.3.1 Oversampling Technique

First, we made the assumption that quantization noise is a uniform distribution in sampling spectrum so its mean is zero and is a white noise [Raz 01]. The system in Fig. 2.6 just has oversampling function and does not have noise shaping effect. If a A/D converter is sampled in Nyquist rate, then the quantization noise is uniform distributed between $\pm f_B$; if it is sampled by oversampling technique, then quantization noise is uniform distributed between$\pm$ $f_{S2}/2_s$, which is much larger than f_B. As shown in Fig. 2.7, if the signal bandwidth is between $\pm f_B$, then quantization noise in this bandwidth will be reduced by using oversampling technique, which will raise PSNR

significantly.

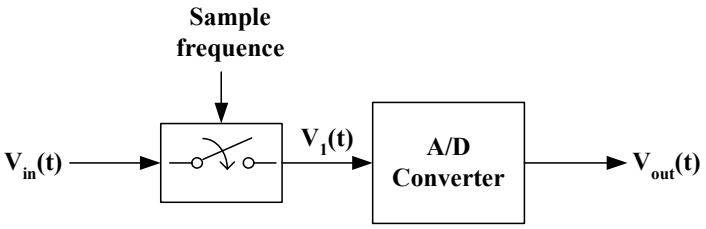


Fig. 2.6 Sampling system

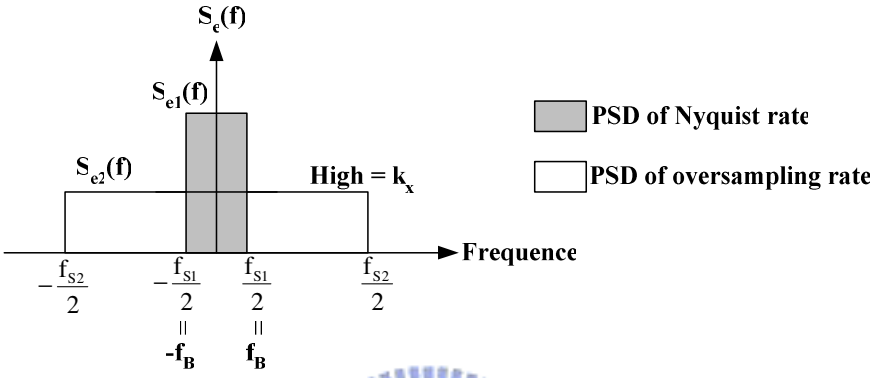


Fig. 2.7 Noise distribution after sampling

In the condition of oversampling, the PSD (Power Spectrum Density) of quantization noise is as $S_{e2}(f)$ in Fig. 2.7 and can be represented as:

$$k_X^2 = \frac{V_{LSB}^2}{12 \cdot f_s} = S_{e2}^2(f) \qquad (2.7)$$

From (2.7) we can estimate the quantization noise in $2f_B$ after oversampling

$$P_Q = \int_{-f_B}^{f_B} k_x^2 \cdot df = \frac{2f_B}{f_s} \cdot \frac{V_{LSB}^2}{12} = \frac{FS^2}{12 \cdot 2^{2B} \cdot OSR} \qquad (2.8)$$

In (2.8), we define a parameter OSR (Oversampling Ratio) as

$$OSR = \frac{f_s}{2f_B} \qquad (2.9)$$

Finally, we can get PSNR from (2.5) and (2.8)

$$PSNR = 10 \log \left(\frac{P_{signal}}{P_Q} \right) = 6.02B + 1.76 + 10 \log (OSR) \qquad (2.10)$$

From (2.10), we can find that doubling OSR will increase 3dB in PSNR, which is

about 0.5 bit increase in resolution. Although oversampling can reduce quantization noise, it is difficult to reach high SNR when using a low bit quantizer. For example, if we need a 16bit A/D converter, then SNR must be equal to 98dB, if the signal bandwidth is 20KHz, then the sampling rate must equal to $2 \times 10^9 \times 20\text{KHz}$, it is impossible to implement. Because at such high frequency, quantization noise is no longer a white noise, it is correlated with input signal. So there is not only oversampling technique, we must add noise shaping technique also, if we want to achieve high resolution.

2.3.2 Noise Shaping

We can model a general ΣΔ modulator and its linear model as shown in Fig. 2.8.

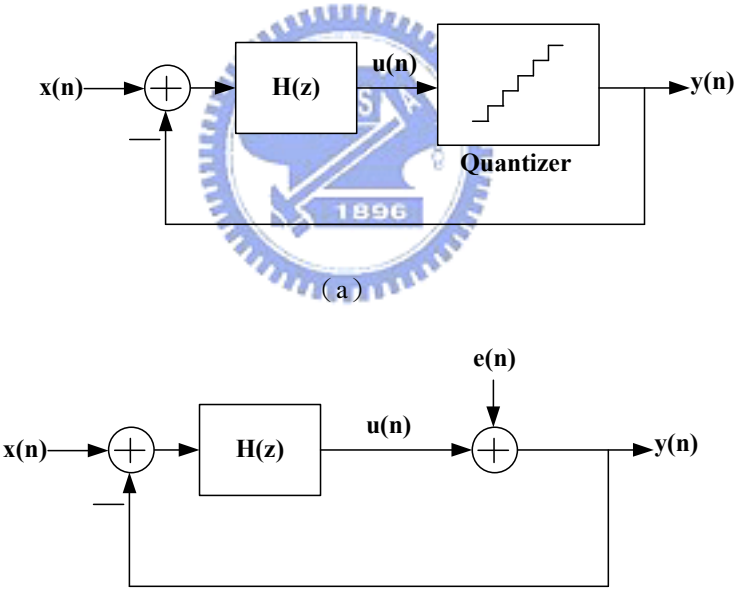


Fig. 2.8 (a) General ΣΔ modulator (b) Linear model with quantization noise

From Fig. 2.8(a), we can derive output Y(z) as (2.11)

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} E(z) \qquad (2.11)$$

and define Signal Transfer Function S_{TF} and Noise transfer function N_{TF} as

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \quad (2.12)$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \quad (2.13)$$

where H(z) is the transfer function of a discrete time filter. There have two important meanings in (2.12), (2.13). If we want to obtain highest SNR, S_{TF} must be equal to 1, that means the input signal can transfer to output without attenuating; and N_{TF} (z) must be equal to 0, because the quantization noise will not affect output SNR.

In order to make N_{TF} (z) be a high pass filter, so at DC(z = 1), N_{TF} must be 0, and z = 1 is a pole of H(z), so the transfer function H(z) of the discrete filter is as

$$H(z) = \frac{1}{Z-1} = \frac{Z^{-1}}{1-Z^{-1}} \quad (2.14)$$

Substitute (2.14) into (2.12) and (2.13), we can get

$$S_{TF}(z) = \frac{1}{z} \quad (2.15)$$

$$N_{TF}(z) = 1-\frac{1}{z} \quad (2.16)$$

And we substitute z with $e^{j\frac{2\pi f}{fs}}$, then we can plot $|S_{TF}(f)|^2$ and $|N_{TF}(f)|^2$ in frequency domain, as Fig. 2.9. We can find $|N_{TF}(f)|^2$ also increases with frequency, and $|S_{TF}(f)|^2$ is always equal to 1, if we choose signal bandwidth in low frequency, then we can get highest signal power and lowest noise power, from this figure we see that quantization noise is moved to higher frequency significantly, this is the noise shaping effect.

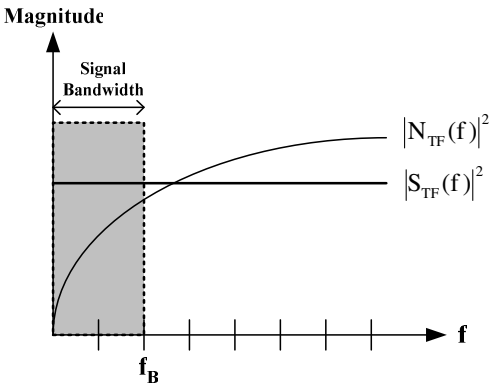


Fig. 2.9 Noise shaping

After noise shaping, we can filter out the noise in high frequency by using digital filter, and we will illustrate its architecture more detail in the next chapter.

3
Architectures of Sigma-Delta Modulator

Before we introduce various architectures of ΣΔ modulators, we must to realize the basic architecture of a general ΣΔ A/D converter. Fig. 3.1 is a complete block diagram of a ΣΔ A/D converter [Joh 97], and we can divide it into two different parts. First part is the ΣΔ modulator. The main function of this part is doing oversampling and noise shaping to the input analog signal. Second part is the decimation filter. The main function of this part is to remove noise in high frequency and down sampling the sampling frequency to base band frequency.

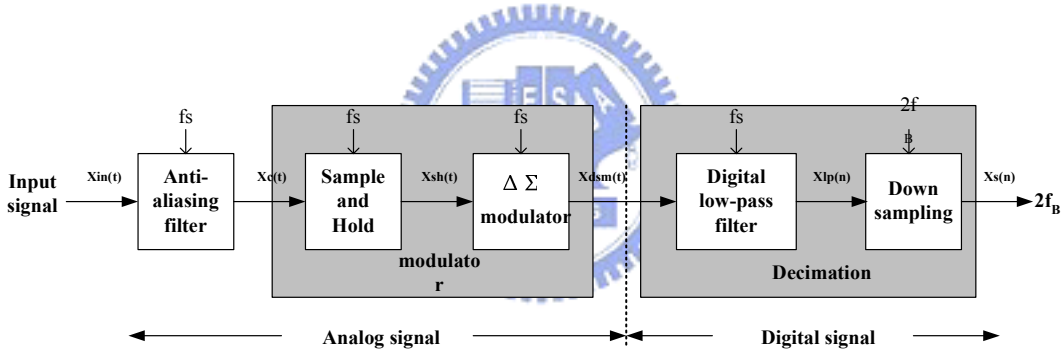


Fig. 3.1 Block diagram of ΣΔ A/D converter

First, the input signal Xin(t) pass an Anti-aliasing filter, the 3dB frequency of this filter is about few times of Nyquist frequency, so signal and noise out of Nyquist frequency is filtered roughly, and this signal goes into the ΣΔ modulator after goes through a S/H circuit. However, in the circuits implement situation, the sample and hold function is included in the circuits of ΣΔ modulator, so the signal Xc(t) will pass this modulator and produces a high speed data code Xdsm(n), because of noise shaping, the quantization noise will appear in high frequency. Finally, we must filter the noise in high frequency and reduce the sampling frequency to Nyquist frequency

by a decimator, and passes the digital signal to the output [Joh 97].

In this chapter, we will focus on the architectures of ΣΔ modulator, because that the noise model and optimal method is focus on this part, we must understand the theorem, benefits and drawbacks of each kinds of ΣΔ modulators. In addition, the implement of decimator is very typical [Ner 02][Mok 94]. In today's technology, DSP processors are also used to replace decimators, so we will introduce this part roughly.

3.1 First-Order Sigma-Delta Modulator

We recall that H(z) in (2.14) is $\frac{Z^{-1}}{1-Z^{-1}}$, substitute it into Fig. 2.8, then we can get a first-order ΣΔ modulator; Analyze transfer function H(z) from time-domain, it indicates that output signal m(t) is obtained by adding the delayed input signal n(t-1) and the delayed output signal m(t-1), so we can express a complete first-order ΣΔ modulator as Fig. 3.2.

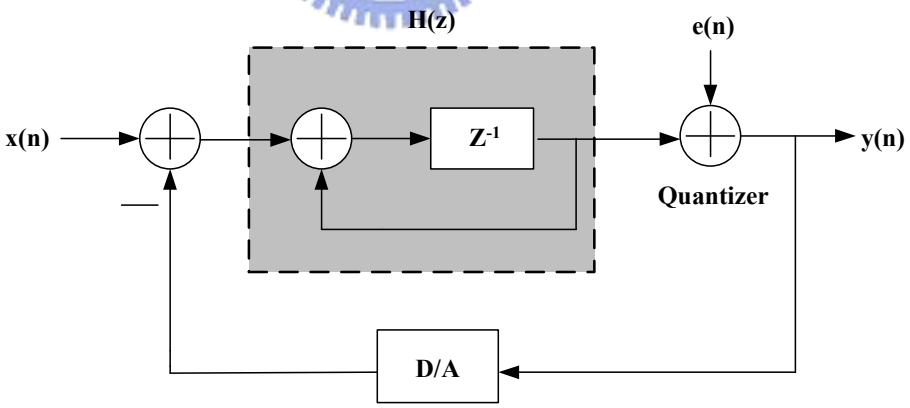


Fig. 3.2 First-order ΣΔ modulator

H(z) in Fig. 3.2 is indicated the effects of delay and accumulation, this is equivalent with an integrator in circuit design, so the three circuits components of ΣΔ modulator are integrator, quantizer and DAC in the feedback path.

A first order ΣΔ modulator's output can represent as

$$Y(z) = z^{-1}X(z) + (1-z^{-1})E(z) \qquad (3.1)$$

From (3.1) we can find the signal transfer function is as a delay function, and noise transfer function is as a high pass filter, moves the noise to high frequency. In order to derive PSNR of first order ΣΔ modulator, we must get the magnitude of $N_{TF}(z)$ and $S_{TF}(z)$ in the frequency domain, so we substitute z with $e^{j2\pi \cdot f/f_s}$, and get $|S_{TF}(f)|$ and $|N_{TF}(f)|$ respectively as:

$$|S_{TF}(f)| = |z^{-1}| = |e^{-j2\pi \cdot f/f_s}| = 1 \qquad (3.2)$$

$$N_{TF}(f) = 1 - e^{-j2\pi \cdot f/f_s} = \sin(\frac{\pi f}{f_s}) \times 2j \times e^{-j\pi \cdot f/f_s}$$

$$\Rightarrow \quad |N_{TF}(f)| = 2 \cdot \sin(\frac{\pi f}{f_s}) \qquad (3.3)$$

So the quantization noise in base band $\pm f_B$ can obtain by (2.7) and (3.3)

$$P_Q = \int_{-f_B}^{f_B} S_e^{\,2}(f) \cdot |N_{TF}(f)|^2 df = \int_{-f_B}^{f_B} \frac{V_{LSB}^{\,2}}{12 \cdot f_s} \cdot \left[2\sin\left(\frac{\pi f}{f_s} \right) \right]^2 \cdot df \qquad (3.4)$$

Because that f_B is much lower than f_s, so $\sin(\pi f/f_s)$ is approximate equal to $(\pi f/f_s)$, and P_Q is as

$$P_Q = \frac{V_{LSB}^{\,2}\pi^2}{36} \cdot (\frac{1}{OSR})^3 = \frac{FS^2 \cdot \pi^2}{36 \cdot 2^{2B} \cdot OSR^3} \qquad (3.5)$$

From (2.5) and (3.5), if we have the maximum signal power, then PSNR is as (3.6)

$$PSNR = 10\log(\frac{P_{signal}}{P_Q}) = 10\log(\frac{3}{2}2^{2B}) + 10\log[\frac{3}{\pi^2}(OSR)^3]$$

$$= 6.02B + 1.76 - 5.17 + 30\log(OSR) \qquad (3.6)$$

From (3.6), we find that each octave of OSR, PSNR will increase 9dB, increase 1.5 bit in resolution. Compare (3.6) with (2.10) that only has oversampling effect; we can find that 1st order noise shaping increases the performance of ΣΔ modulator.

3.2 Single-Loop Second-Order Sigma-Delta Modulator

When the discrete time filter in Fig. 2.8 is replaced by two cascade integrator, then it is a second order ΣΔ modulator, output of the first integrator is only connecting with the input of the second integrator, it is shown in Fig. 3.3

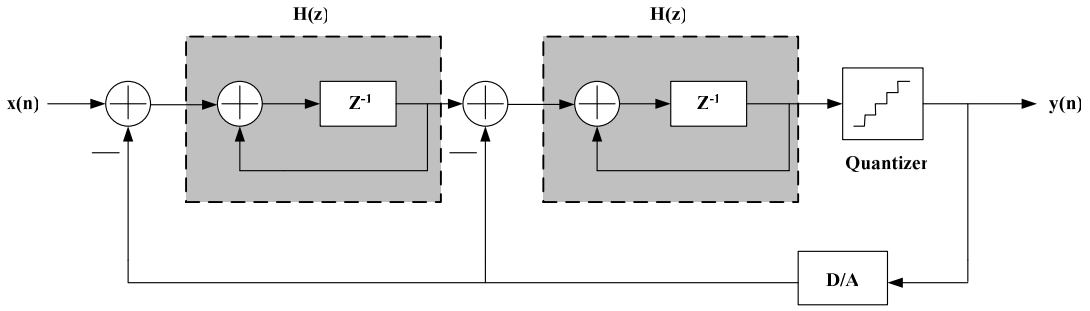


Fig. 3.3 Single loop second order ΣΔ modulator

Then the output of it can easily be derived as

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2E(z) \qquad (3.7)$$

where S_{TF} and N_{TF} is as

$$S_{TF}(z) = z^{-2} \qquad (3.8)$$

$$N_{TF}(z) = (1- z^{-1})^2 \qquad (3.9)$$

Using the same method in (3.3) (3.4), we can obtain

$$\left|S_{TF}(f)\right| = 1 \qquad (3.10)$$

$$\left|N_{TF}(f)\right| = \left[2 \cdot \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \qquad (3.11)$$

$$P_Q = \frac{{V_{LSB}}^2 \cdot \pi^4}{60 \cdot OSR^5} = \frac{FS^2 \cdot \pi^4}{2^{2B} \cdot 60 \cdot OSR^5} \qquad (3.12)$$

So finally, PSNR of the second order ΣΔ modulator is as

$$PSNR = 10\log\left(\frac{P_{signal}}{P_Q}\right) = 10\log\left(\frac{3}{2}2^{2B}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

$$= 6.02B + 1.76 - 12.9 + 50\log(OSR) \qquad (3.13)$$

In the single loop second order architecture, each octave of OSR can increase PSNR by 15 dB, it is equivalent to 2.5 bit in resolution. If we compare (3.13), (3.11) with $|NTF(f)|=1$ that without noise shaping, as Fig. 3.4, we can find that in our needed signal bandwidth, the quantization noise is highest when $|NTF(f)|=1$, and that with second order noise shaping is smallest among this figure [Joh 97].

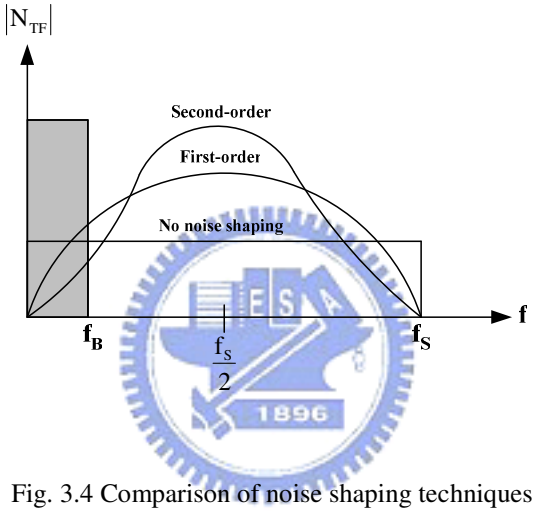


Fig. 3.4 Comparison of noise shaping techniques

3.3 Single-Loop High Order Sigma-Delta Modulator

Fig. 3.5 is a single loop high order ΣΔ modulator, from the derivation in Section 3.1 and Section 3.2, we can get the quantization noise P_Q in signal bandwidth is as

$$P_Q = \frac{V_{LSB}^{\ 2}}{12} \cdot \frac{\pi^{2L}}{2L+1} \cdot \left(\frac{1}{OSR}\right)^{2L+1} \quad , L: \text{order} \qquad (3.14)$$

and its PSNR is

$$PSNR = 6.02B + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \qquad (3.15)$$

In the application of high order ΣΔ modulator, (6L+3)dB increases in SNR when OSR is octave, so PSNR can be raised by increasing the order of the system, especially at large oversampling ratio. But sometimes in high order architecture, the

performance will be worsen than result predicted by (3.13), because of the stability problem, it will make less effective noise shaping function, so the quantization noise will not be suppressed completely.

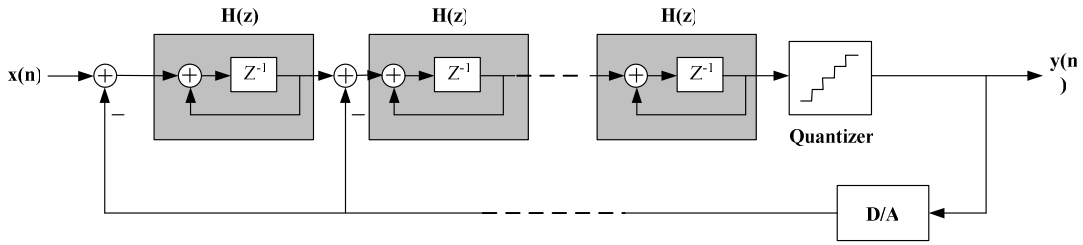


Fig 3.5 Single-loop high order ΣΔ modulator

3.4 Interpolative Sigma-Delta Modulator

Interpolative is a kind of high order ΣΔ modulator, it changes connection of some stages, adds some feedforward paths and feedback paths in order to suppose more aggressive noise shaping effect, Fig. 3.6 is a four-order interpolative architecture ΣΔ modulator [Cha 90].

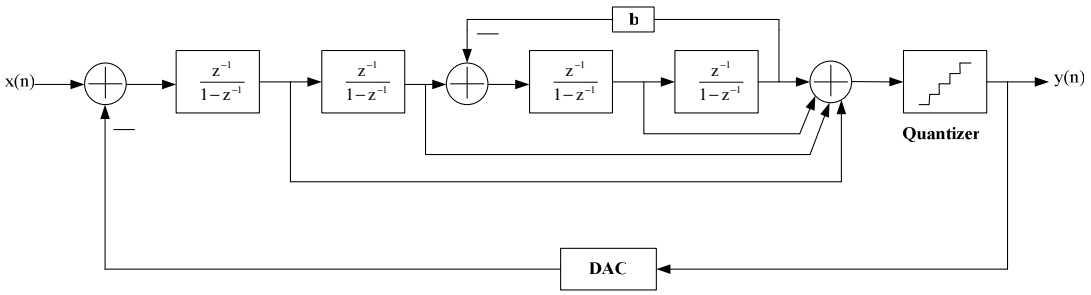


Fig. 3.6 Four-order interpolative architecture

This architecture also has stability problem, when the order L increases, each integrator produces one pole, and when the order is higher, poles of this system will also increase, and it will cause unstable situation, so the range of integrator gain will be limited; if the range of integrator gain is small, oscillation will appear in the

circuits. Another is the considerations of clock control, when we use SC (switched-capacitor) to implement the integrator, each integrator needs two clocks to control its operation, and we will need more clock to control the integrator when the order of system increases, it will produce more problems.

3.5 MASH Architecture

MASH (Multi-stage noise shaping) architecture is also called cascade architecture, which is a method that cascades several low order loops modulator in order to get high order noise shaping effect. The fundamental ideal of MASH is delivering quantization noise of front stage to input of next stage, and combining the digital outputs of all the stages with proper transfer function in digital domain, only the quantization noise of last stage will appear at the output, and the orders of N_{TF} is the same with total orders in the cascade ΣΔ modulator. Fig 3.7 is a three-order cascade ΣΔ modulator, its is the combination of a second-order and first-order ΣΔ modulator, so also called 2-1 cascade architecture [Wil 94].

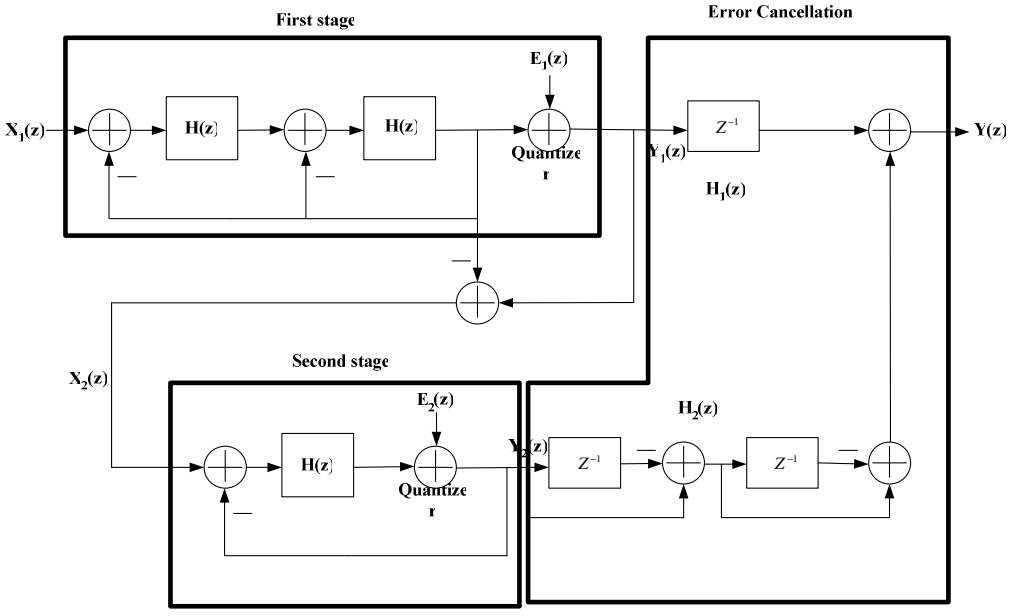


Fig. 3.7 2-1 architecture MASH ΣΔ modulator

From Fig. 3.7, we can derive the first stage output $Y_1(z)$ can be represented as

$$Y_1(z) = z^{-2}X_1(z) + (1-z^{-1})^2E_1(z) \quad (3.16)$$

Output of second stage $Y_2(z)$ is as

$$Y_2(z) = z^{-1}X_2(z) + (1-z^{-1})E_2(z) \quad (3.17)$$

and overall output of MASH Y(z) is as

$$Y(z) = H_1(z)Y_1(z) + H_2(z)Y_2(z) \quad (3.18)$$

and we can say that second stage input $X_2(z)$ is almost the same with $E_1(z)$, in order to eliminate first stage quantization noise $E_1(z)$, from (3.16) ~ (3.18), we can define the error cancellation functions $H_1(z)$ and $H_2(z)$ as

$$H_1(z) = z^{-1} \quad (3.19)$$

$$H_2(z) = (1-z^{-1})^2 \quad (3.20)$$

From (3.16)~(3.20), $E_1(z)$ can be eliminated, and second stage quantization noise $E_2(z)$ is shaped by third-order noise shaping function, and the MASH output Y(z) is as

$$Y(z) = z^{-3}X_1(z) + (1-z^{-1})^3E_2(z) \quad (3.21)$$

The most significant advantage of this architecture is that stability is not an issue, because it is composed by several low-order systems, and the quantization noise will not be amplified stage by stage, so its stability is good. Most important, the noise shaping function is equivalent as high order ΣΔ modulator, so it is popular in recent publications [Rio 04][Vle 01]. However, there also have some drawbacks of this topology; it is sensitive to the circuits' imperfections, such as finite DC gain of OTA, variance of integrator gain due to capacitor mismatch and non-zero switch resistance. These are all practical considerations when we design a MASH architecture ΣΔ modulator [Gag 03].

3.6 Multi-bit Quantizer Sigma-Delta Modulator

The demands of high resolution and high bandwidth ADC are more and more in

recent years. In a high signal bandwidth, OSR of ΣΔ ADC can't be too high, and the peak SNR of a ΣΔ modulator with such limited OSR can't satisfy of high resolution applications, if we use higher order architecture, then the performance will degrade due to instability. So the most general method to increase performance is to use multibit quantizer. The most obvious advantage of using multibit quantizer is that the distance between quantizer level V_{LSB} in (2.4) is much smaller due to increasing of B, and according to (2.3), the power of quantization noise is attenuated. Fig. 3.8 is the results of theoretical peak SNR of ΣΔ modulator versus oversampling ratio, with different order and quantizer bits, it is noted that peak SNR of the same OSR is increase 6 dB with each additional bit number in quantizer, and at low OSR, low order higher bit number architecture has equivalent performance as high order architecture. This result is usable for high bandwidth applications, and the power consumption of digital circuit in ΣΔ modulator is reduced due to lower sampling rate [Pel 99].

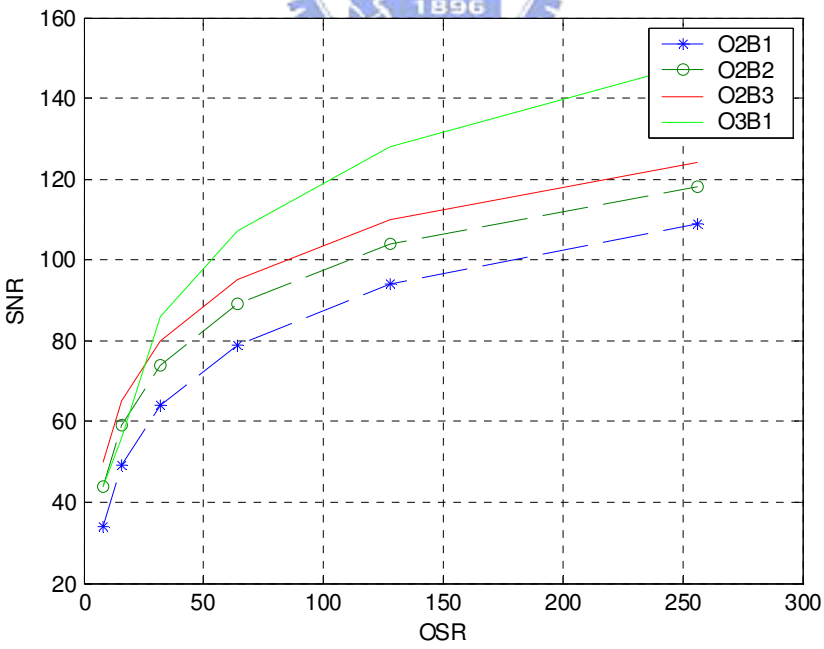


Fig. 3.8 SNR vs. OSR with different quantizer bit number

Because of using multi-bit quantizer, so we also need to use multi-bit DAC(Digital-to Analog Converter) to transfer the digital output to analog signal, and feed it back to

integrator. The most significant disadvantage is the non-linearities introduced by multi-bit DAC can degrade the performance of ΣΔ converter, like Fig. 3.9. It is a linear model of multi-bit ΣΔ modulator, where E(Q) and E(D) represent the quantization noise and feedback DAC noise respectively. The values of these capacitor elements in DAC will not equal to ideal values that we need, it is due to process variation, typical value of mismatch in modern CMOS technology is about 0.05% ~ 0.5%. In recent years, so many researches are make efforts on reduce DAC noise due to mismatch, such as trimming [Nor97], Dynamic element matching(DEM)[Mil 03][Reb 90], although trimming is effective, but it has a expensive production step. So, DEM becomes more and more popular because of its efficiency and cheaper cost.

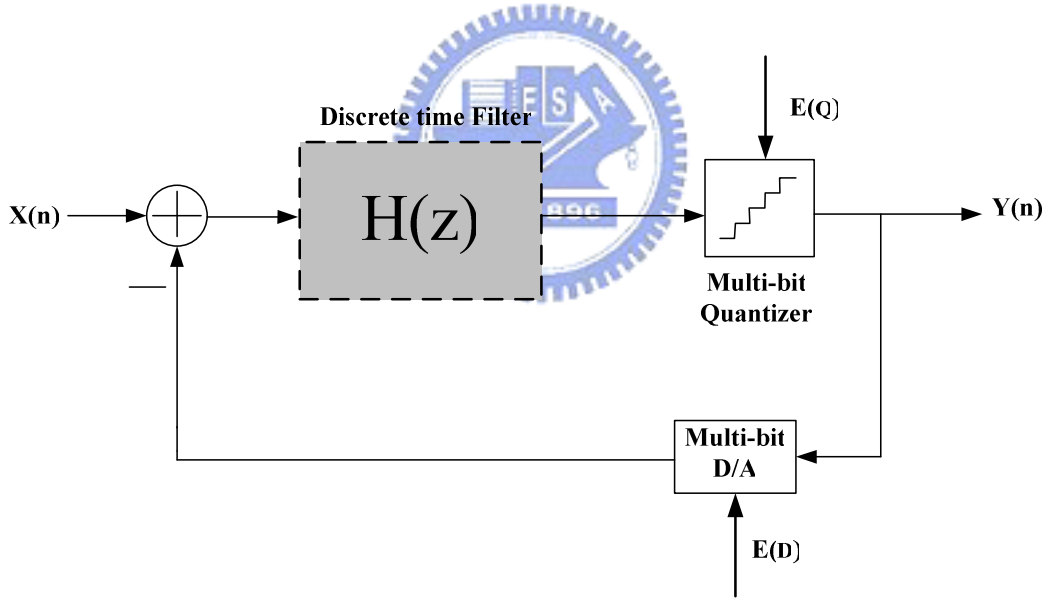


Fig. 3.9 Multi-bit architecture

3.7 Multi-bit Sigma-Delta Modulator use DEM Technique

Dynamic element matching is a different approach to decrease the DAC noise, it is used to improve the linearity of pure DACs [Pla 79], but now it is most used in inner DAC of multi-bit ΣΔ modulator. A DAC with DEM technique is illustrated in

Fig. 3.10, 2^B bits thermometer code is put into the element selection logic block, and the function of element selection logic is try to select DAC elements in such way let the errors introduced by DAC average to zero for several operation periods. Because the DEM block is located in feedback loop, so its delay must be very small prevent to degrade the performance of $\Sigma\Delta$ converter, therefore the algorithm used in the DEM block must be simple. There are several techniques of DEM, such as Randomization [Car 89], Clocked Averaging (CLA) [Pla 79], Individual Level Averaging (ILA) [Che 95], Data Weighted Averaging (DWA) [Bai 95], Randomization is the first approach to use DEM technique in $\Sigma\Delta$ ADC, and DWA offers a good performance to reduce DAC error, in this section, an overview introduction of these two algorithms will be presented, and the operation principle of them will be explained.

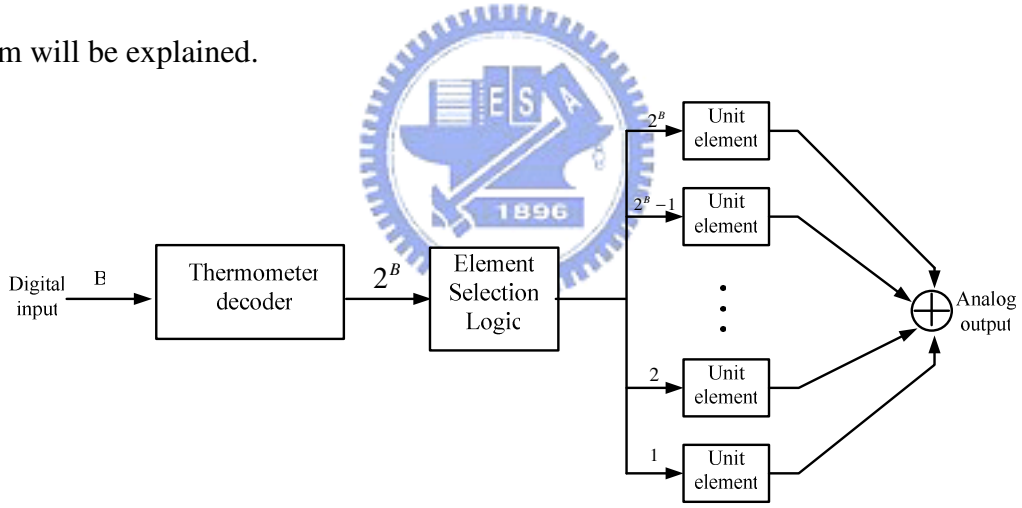


Fig. 3.10 A B-bit DAC with DEM technique

3.7.1 Randomization Technique

The main operation principle of randomization is that the element selection logic performs as a randomizer. In each clock period, the randomizer selects DAC elements randomly to generate the output of DAC. If the randomizer is ideal, then the DAC noise will become uncorrelated with each other. Simulation results show that randomization DEM technique reduces the noise floor from DAC error by several dB,

but it still be a white noise in low frequency. Fig. 3.12 is the output spectrum of a second-order ΣΔ modulator with a 0.1% capacitor mismatch, it is notable that the noise floor of randomization DEM is lower than that without any calibration technique in the feedback DAC.

3.7.2 Data Weighted Averaging (DWA)

DWA is a efficiently method to reduce DAC mismatch noise, it uses one register to remember the capacitor last time used, and always points to the first unused unit capacitor in this clock, so DWA rotates through all the unit capacitors such that all capacitors are used at the maximum possible rate. From this algorithm, each elements is used the same number of times in long interval, this ensures that the errors caused by the DAC average to zero quickly. In Fig. 3.11, it is a 4-bit DAC and the shaded boxes are the number of 1's in the thermometer code. Assumes that the input codes sequence is 8, 8, 10, 9, 10, 10, 11, 11, 12, 11, 14, 11, 14, 13, 12, 15... Fig. 3.12 is the simulation results of a third order ΣΔ modulator, we can see that without DEM has highest noise floor and DWA works as a first order noise shaping function of DAC noise, ideal DAC only with quantization noise has third-order noise shaping.

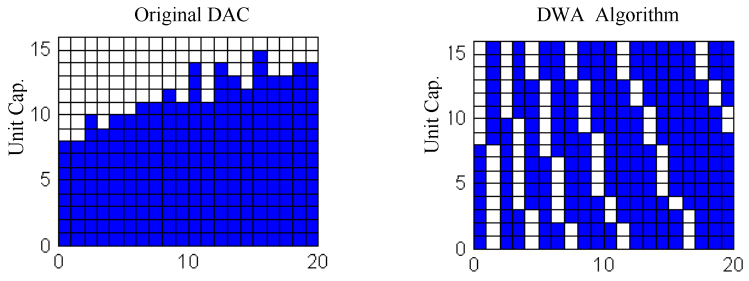


Fig. 3.11 Operation principle of the DWA algorithm

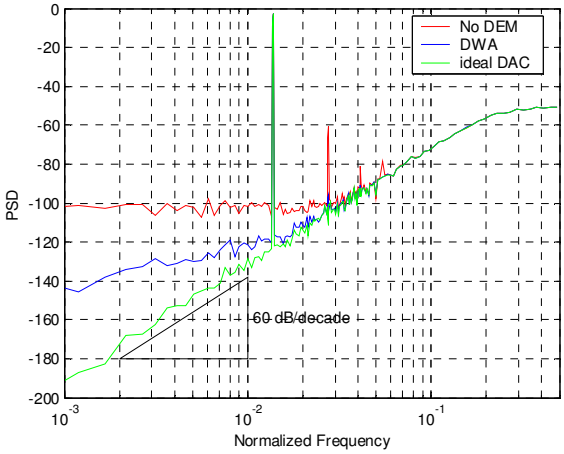


Fig. 3.12 Output spectrum with three kinds of DAC

Another consideration is the sub-ADC(quantizer) of the ΣΔ modulator, we usually use Flash A/D as the multi-bit quantizer because of its high speed, but Flash A/D has a significant disadvantage is that the number of comparators of it is proportional to 2^B. That means a 6 bit quantizer needs 64 comparators, the occupied area of comparator may not much, but in modern SOC applications, the problems of power and area are important, so it becomes one limitation of multi-bit quantization.

ΣΔ A/D converter is attractive for high resolution application, for higher signal bandwidth, we increase system order to raise SNR, but it still have stability problem. So people develop MASH and multi-bit architecture to improve its performance. Finally, we classify they into low order, high order, MASH and multi-bit four kinds of architecture, and compare their advantage and disadvantage as Fig. 3.13 [Med 99]

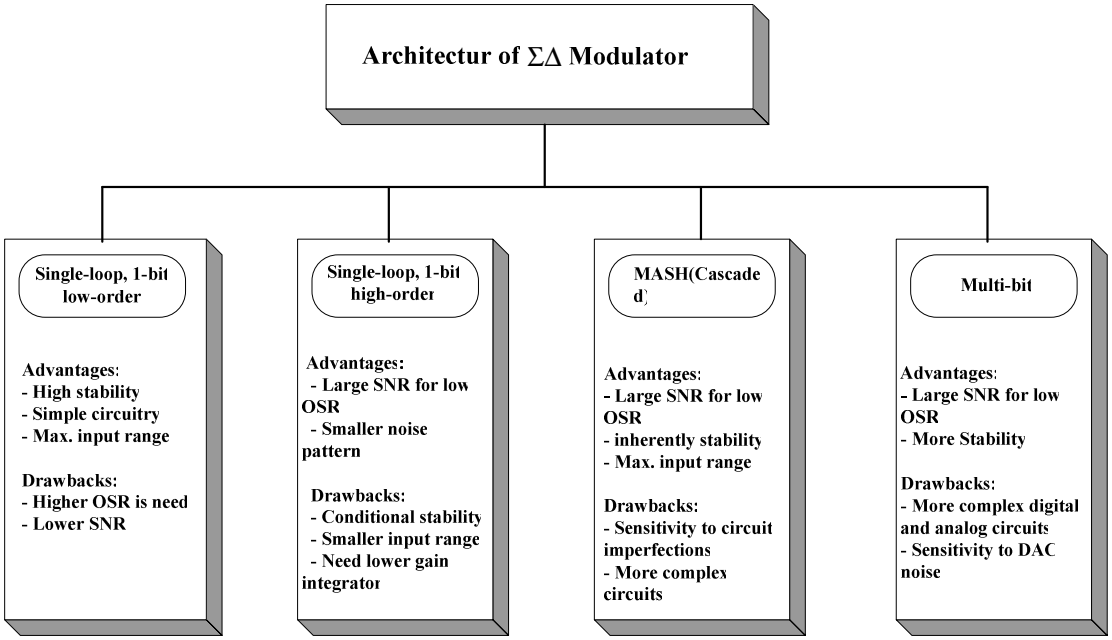


Fig. 3.13 Comparison of ΣΔ modulator architectures

3.8 Decimator

In ΣΔ A/D converter, digital decimator is used to process digital signal of the quantizer output, the high speed data word after oversampling modulation can't be used directly. Because there have original signal and quantization noise among it, so the main function of decimator is to convert the oversampled B-bit output words of the quantizer at a sampling rate of fs to N-bit words at Nyquist rate of input, and removes the noise out of signal band. In order to prevent the noise introduced by other frequency, the decimator filter must have very flat signal pass-band, and sharp transition region and enough signal attenuation in stop band. Two-stage decimator is used in a general situation, because that single stage decimator is difficult to convert sampling rate to Nyquist rate in 1 time and without degrading SNR. In the first stage, we can down-sample the sample frequency to 2~4 times of Nyquist frequency, and in the second stage, we can use IIR or FIR filter that have high linearity [Nor 97]. For a large OSR, multi-stage decimator is used.

3.9 Performance Metrics for a ΣΔ Modulator

In order to understand the performance merits used to specify the behavior of ΣΔ modulator, several specifications concerning the performance are discussed [Gee 02].

- **Signal to Noise Ratio:** The SNR of a data converter is the ratio of the signal power to the noise power, measured at the output of the converter for a certain input amplitude. The maximum SNR that a converter can achieve is called the peak SNR.
- **Signal to Noise and Distortion Ratio:** The SNDR of a converter is the ratio of the signal power to the power of the noise and the distortion components, measured at the output of the converter for a certain input amplitude. The maximum SNDR that a converter can achieve is called the peak SNDR.
- **Dynamic Range at the input:** The DRi is the ratio between the power of the largest input signal that can be applied without significantly degrading the performance of the converter, and the power of the smallest detectable input signal. The level of significantly degrading the performance is defined as the point where the SNDR is 6 dB bellow the peak SNDR. The smallest detectable input signal is determined by the noise floor of the converter.
- **Dynamic Range at the output:** The dynamic range can also be considered at the output of the converter. The ratio between maximum and minimum output power is the dynamic range at the output DR_o, which is exactly equal to peak SNR.
- **Effective Number of Bits:** ENOB gives an indication of how many bits would be required in an ideal quantizer to get the same performance as the converter. This numbers also includes the distortion components and can be calculated from (2.6) as

$$\text{ENOB} = \frac{SNR - 1.76}{6.02} \tag{3.22}$$

- **Overload Level:** OL is defined as the relative input amplitude where the SNDR is decreased by 6dB compared to peak SNDR

Typically, these specifications are reported using plots like Fig. 3.14. This figure shows the SNR and SNDR of the ΣΔ converter versus the amplitude of the sinusoidal wave applied to the input of the converter. For small input levels, the distortion components are submerged in the noise floor of the converter. Consequently, the SNDR and SNR curves coincide for small input levels. When the input level increases, the distortion components start to degrade the modulator performance. Therefore, the SNDR will be smaller than the SNR for large input signals. Note that these specifications are dependent on the frequency of the input signal and the clock frequency of the converter. Fig. 3.14 also shows that SNDR curves drop very fast once the overload point is achieved. This is due to the overloading effect of the quantizer which results in instabilities.

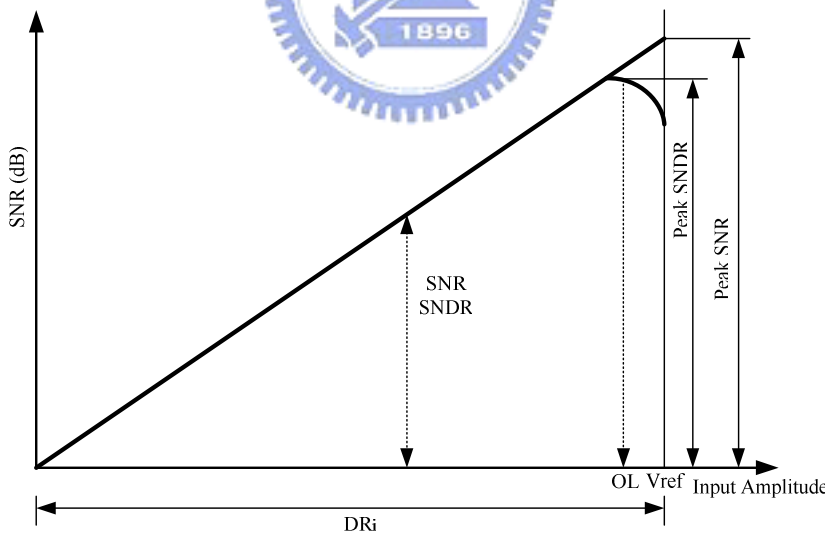


Fig. 3.14 Performance characteristic of a ΣΔ converter

4

Models of Sigma-Delta Modulator Noises and Power

Proposing an optimization algorithm for searching design parameters which maximize ΣΔ ADC SNR while minimize power consumption, is one of the primary purposes of this paper. Related model completeness determines success of this goal. The ΣΔ modulator nonidealities are categorized into five parts in this chapter; finite OTA gain error, thermal noise, settling error, multi-bit DAC noise, and jitter noise. All nonideality models are expressed in noise power form, which can directly add to ideal quantization noise power. All noise power models discussed in the following are based on the integrator scheme, as shown in Fig. 4.1. In Fig. 4.1, C_u is the unit capacitor whose capacitance value is $\frac{C_S}{2^B}$. The power consumption model is presented as the last part of this chapter.

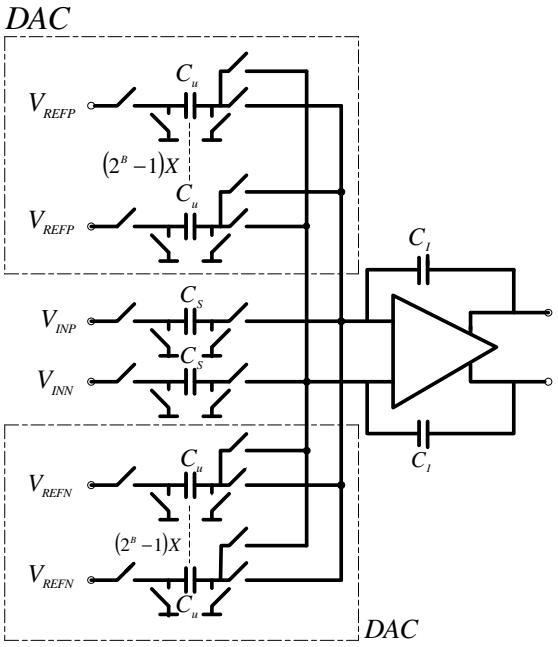


Fig. 4.1 Integrator and the DAC branches

4.1 Finite OTA Gain Error

Finite OTA Gain is an important error when we analyze a real integrator. Typical value of OTA gain is about 50 ~ 80 dB in modern CMOS technology. For a general single-loop n th order ΣΔ modulator with finite OTA gain A, the modified quantization noise is expressed as [Med 99]:

$$P_{Q(\text{mod.})} \cong \frac{\Delta^2}{12} \cdot \left[\frac{\pi^{2n}}{(2n+1) \cdot OSR^{2n+1}} + \left(\frac{a_1}{A} \right)^2 \cdot \frac{\pi^{2n-2} \cdot n}{(2n-1) \cdot OSR^{2n-1}} \right]$$

$$= P_Q + P_{AV} \qquad (4.1)$$

where P_Q is the original quantization noise, and Δ is the quantizer step size. The P_{AV} in (4.1) is due to finite OTA gain, and can be considered as an additive quantization noise power. It can be verified using (4.1) that, for a single-loop topology, $A = 50$ dB is sufficient to avoid SNR degrades, in the sense that a higher A would not significantly reduce $P_{Q(\text{mod.})}$.

4.2 Thermal noise (Switch, OTA, Reference circuits)

There are three thermal noise sources in the ΣΔ modulator, in MOS switches, OTAs and reference voltage. We will analyze them separately as follows.

For a fully differential implementation, the in band switch thermal noise during the sampling phase results in output noise power [Med 99]

$$P_{sw1} = \frac{1}{OSR} \cdot \left(\frac{4\text{kT}}{\text{C}_\text{S}} \right) \qquad (4.2)$$

where k is Boltzman constant and T is the absolute temperature. Additional thermal noise is introduced by the switches during the integration phase, resulting in the output noise power [Gee 02]

$$P_{sw2} \cong \frac{1}{OSR} \cdot \left(\frac{4\mathrm{kT}}{\mathrm{C_S}} \right) \tag{4.3}$$

Since the thermal noise voltages introduced during these two phases are uncorrelated, the total output switches thermal noise power from the switched capacitor integrator is

$$P_{sw} = P_{sw1} + P_{sw2} \cong \frac{1}{OSR} \cdot \left(\frac{8\mathrm{kT}}{\mathrm{C_S}} \right) \tag{4.4}$$

Half of P_{sw} is from the input branch, and the other half is from the DAC branch.

The OTA transistor thermal noise can be modeled as an equivalent noise source $\mathrm{V_{no}}$ at OTA input shown in Fig. 4.2. In deep submicron process $\mathrm{V_{no}} \cong \frac{\alpha \cdot 10\mathrm{kT}}{\mathrm{gm1}}\ \mathrm{V^2/Hz}$ [Gra 01], where α is a noise factor depending on OTA topology. In a two-stage OTA, $\alpha \approx 2$. During the sampling phase (Fig. 4.2(a)), the circuit looks like a voltage follower. However, due to OTA finite gain bandwidth, noise at $\mathrm{V_O}$ has an equivalent bandwidth, so thermal noise power at integrator output in the sampling phase is

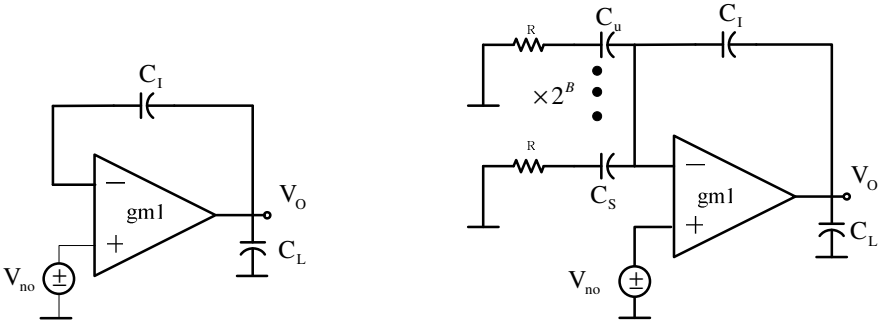
$$P_{OTA}(samp) \cong \mathrm{V_{no}} \cdot \frac{\mathrm{GBW_{samp}}}{A \cdot 2\pi} \cdot \frac{\pi}{2} = \frac{10\alpha \cdot \mathrm{kT}}{4AC_L} \tag{4.5}$$

During the integration phase (Fig. 4.2(b)), the circuit looks like a non-inverting amplifier, with

$$\frac{\mathrm{V_O}}{\mathrm{V_{no}}}(s) \cong \left(\frac{2a_1 + 1 + 2sC_S R}{1 + 2sC_S R} \right) \Big/ \left(1 + \frac{s}{GBW/A} \right) \tag{4.6}$$

where GBW/A is the 3dB frequency of the non-inverting amplifier. Then the OTA noise power at the first integrator output can be expressed as

$$P_{OTA}(\mathrm{int}) \cong \int_0^\infty \mathrm{V_{no}} \cdot \left| \frac{\mathrm{V_O}}{\mathrm{V_{no}}}(f) \right|^2 df \tag{4.7}$$



(a) sampling phase (b) Integration phase

Fig. 4.2 Equivalent circuits of sampling and integration phases

Finally, the total OTA thermal noise power at the ΣΔ ADC output can be obtained as

$$P_{OTA} = \frac{1}{OSR}\cdot\left(\frac{1}{a_1}\right)^2\cdot(P_{OTA}(samp)+P_{OTA}(\text{int}))$$

$$=\frac{1}{OSR\cdot a_1^{\,2}}\cdot\left(\frac{10\alpha\cdot \text{kT}}{4AC_L}+\int_0^{\infty}\text{V}_{\text{no}}\cdot\left|\frac{\text{V}_{\text{O}}}{\text{V}_{\text{no}}}(f)\right|^2 df\right) \qquad (4.8)$$

The reference voltage circuit is implemented by transistors, so the thermal noise device will appear at the reference circuit output and influence the system directly. Consider the bandgap reference circuit in Fig. 4.3 [Raz 01]. Reference output noise is nearly equivalent to OTA input referred noise [Raz 01], so we can express it as $\overline{V_{ref}^{\,2}} \approx \text{V}_{\text{no}} = \frac{10\text{kT}\cdot\alpha}{\text{gm1}}$. Different integrator schemes can introduce reference noise in different ways [Gag 03][Mil 03][Gee 00]. We consider the case shown in Fig. 4.4, where this noise is introduced only in the sampling phase. If the reference noise is unbuffered, its noise power at the ΣΔ ADC output can be derived as

$$P_{ref} = \frac{1}{OSR}\cdot\int_0^{\infty}\frac{\overline{V_{ref}^{\,2}}}{1+4\pi^2\text{R}^2\text{C}_\text{S}^2 f^2}df = \frac{\overline{V_{ref}^{\,2}}}{OSR\cdot 4\text{RC}_\text{S}} \qquad (4.9)$$

We usually add buffers between the bandgap circuits [Pie 02] and the DAC paths.

Denote the 3dB buffer bandwidth as BW_b. If BW_b is smaller than $\frac{1}{4RC_S}$, the P_{ref} in （4.9）is changed to be

$$P_{ref} = \overline{V_{ref}^2} \cdot \frac{\pi \cdot BW_b}{2OSR} \qquad (4.10)$$

If BW_b is larger than $\frac{1}{4RC_S}$, the P_{ref} in（4.9）is applied.

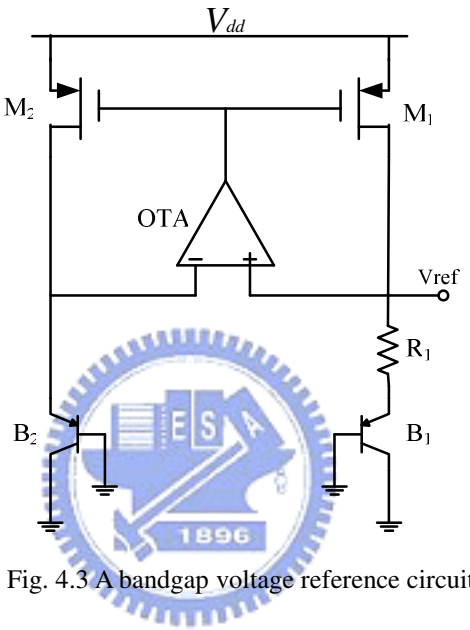


Fig. 4.3 A bandgap voltage reference circuit

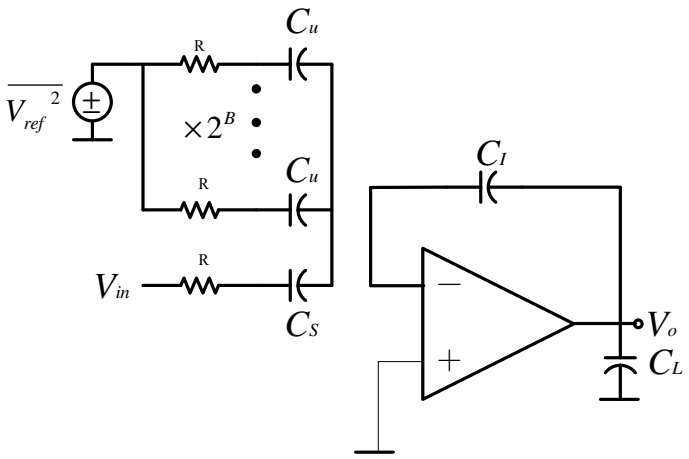


Fig. 4.4 Equivalent circuit while considering reference voltage noise

4.3 Settling Problem

As ΣΔ modulator sampling frequency increases, and multi-bit quantization

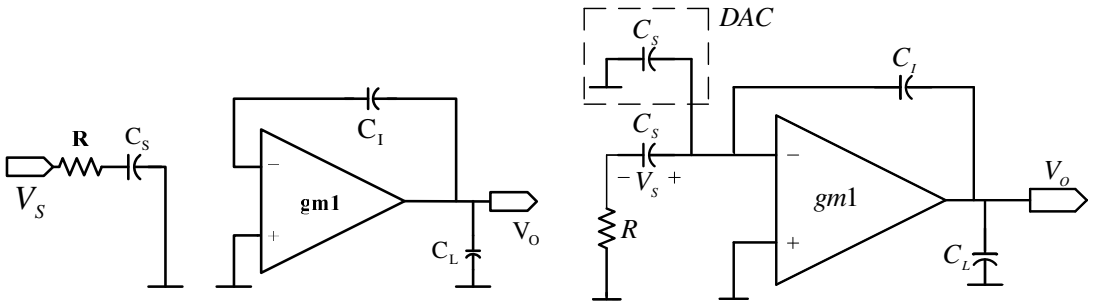
becomes a high resolution and high-speed application trend, the dynamic settling problem of switched capacitor integrator becomes a more dominant factor. Previous articles have mentioned the settling error [Mal 03][Gri 02][Rio 00]. References [Mal 03] and [Rio 00] provide behavior models, which are tedious and integrate poorly with noise-power models of other noises or errors. The noise-power model of [Gri 02] is very primitive since it assumes the pdf (probability density function) settling error is uniformly distributed, and does not consider multi-bit quantization. We only consider the integrator at the first stage. Settling errors at later stages are less influential due to noise shaping.

Now consider a switched capacitor integrator in Fig. 4.5. Assume the MOS switch has an on-resistance *R*, and gm1 is the transconductance of OTA. Let the output parasitic capacitor $C_L \cong \eta \cdot C_I$, where η is the percentage of bottom plate parasitic, assumed to be 20% [Rab 99]. In Fig. 4.5(a), the voltage V_S represents the difference between the sinusoid input signal and the feedback signal from DAC. It is sampled by C_S, so C_S is charged in the half clock period $\frac{T}{2}$ to the voltage V_{CS}:

$$V_{CS} = V_S \cdot [1 - \exp(-\frac{T}{2 \cdot \tau_1})] \qquad (4.11)$$

where $\tau_1 = R \cdot C_S$ is the time constant in the input branch. So the setting error during the sampling phase is:

$$\varepsilon_1 = V_S \cdot \exp(-\frac{T}{2 \cdot \tau_1}) \qquad (4.12)$$



(a) Sampling phase (b) Integration phase

Fig. 4.5 Switched capacitor integrator diagrams

In order to obtain settling noise power during the sampling phase from（4.12）, we need to find the V_S statistical property. Simulations results (using SIMULINK) on a second-order $\Sigma\Delta$ modulator with $a_1 = 0.5$, $a_2 = 2$, 10-level quantization, reference voltage $V_{ref} = \pm 1$, and a full scale sinusoidal input signal, are shown in Fig. 4.6. The result is close to a Gaussian distribution. Therefore, we assume V_S is Gaussian distributed with a zero mean. The standard deviations σ_{VS} of V_S under different quantizer levels are tabulated in Table 4.1. We observed that when the quantizer level N increases, σ_{VS} decreases. From this table, the relation between standard deviation σ_{VS} and quantizer levels 2^B can be approximated by

$$2^B \cdot \sigma_{vs} \approx 1.4 \cdot |V_{ref}| \qquad (4.13)$$

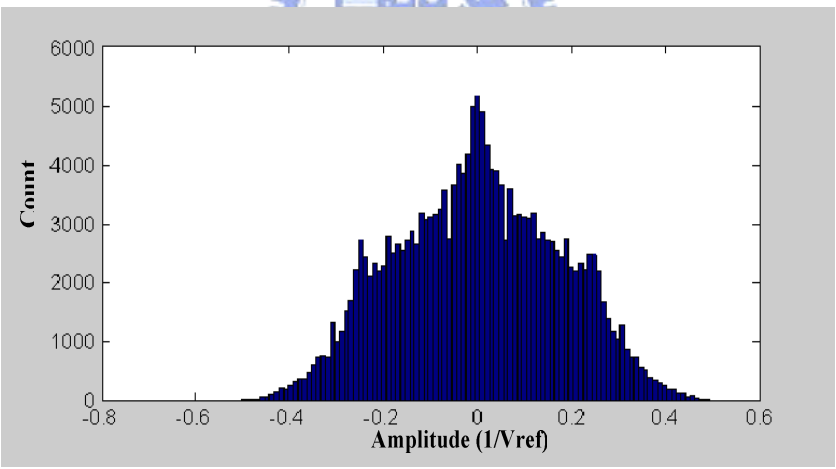


Fig. 4.6 Simulated results of V_S distribution

Std. deviation (σ_{VS})	Variance	Quantizer level (N)	Bit number (B)
0.706	0.498	2	1
0.476	0.227	3	1.585
0.282	0.080	5	2.322
0.198	0.040	7	2.808
0.152	0.023	9	3.17
0.124	0.016	11	3.46
0.047	0.002	31	4.95

TABLE 4.1 Standard deviations of V_S vs. different quantizer bit numbers

The settling noise can reasonably assumed to be white, and its power spectral density constant and distributed over $(-f_S/2, f_S/2)$ as:

$$S_{\varepsilon 1} = \frac{1}{f_S} \cdot \left(\frac{1.4 \cdot \mathrm{V_{ref}}}{2^B} \right)^2 \cdot \exp(\frac{-T}{\tau_1}) \qquad (4.14)$$

Due to oversampling, noise power can be obtained by integrating (4.14) in the signal band $(-f_B, f_B)$, which is:

$$P_{\varepsilon 1} = \frac{1}{OSR} \cdot \left(\frac{1.4 \cdot \mathrm{V_{ref}}}{2^B} \right)^2 \cdot \exp(\frac{-T}{\tau_1}) \qquad (4.15)$$

Next, we consider the integration phase shown in Fig 4.5(b), where the 2^B unit capacitors are combined into C_S, and the 2^B DAC switches are neglected. The charge stored in sampling capacitor will be added to the integration capacitor and this charge current is supplied by OTA. So when the slew rate and gain bandwidth are not large enough, the settling error ε_2 will be produced. The statistical properties of V_S have been summarized in Table I. Then, according to Fig. 4.7, three types of settling conditions can happen in the integrator output during this phase, and the corresponding voltage errors of these three conditions are [Mal 03]:

1. Linear settling: When the initial change rate of the integrator output voltage ($\mathrm{V_O}$) is smaller than the OTA slew rate (SR).

$$\varepsilon_2 = a_1 \cdot |V_S| \cdot \exp(-\frac{T}{2 \cdot \tau_2}), \text{ when } \ 0 < |V_S| < \frac{1}{a_1} \cdot SR \cdot \tau_2 \qquad (4.16)$$

2. Partial slewing: The initial change rate of V_O is larger than SR, but it gradually decreases until it is below the slew rate.

$$\varepsilon_2 = SR \cdot \tau_2 \cdot \exp(\frac{a_1 \cdot |V_S|}{SR \cdot \tau_2} - \frac{T}{2\tau_2} - 1), \text{ when } \ \frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S| < (\frac{T}{2} + \tau_2)\frac{SR}{a_1} \qquad (4.17)$$

3. Fully slewing: The initial change rate of V_O is larger than SR, and it maintains above SR in the $T/2$ interval.

$$\varepsilon_2 = a_1 \cdot |V_S| - SR \cdot \frac{T}{2}, \text{ when } \ |V_S| > \frac{SR}{a_1}(\frac{T}{2} + \tau_2) \qquad (4.18)$$

where SR is the slew rate of OTA, and $\tau_2 = \frac{1 + 2\pi \cdot GBW \cdot R \cdot Cs}{2\pi \cdot GBW}$ [Gee 99a] is the time constant in the integration phase, with GBW being the equivalent gain bandwidth in the integration phase. The capacitor loading in OTA output during this phase is heavier than in the sampling phase, and is [Gee 02]

$$C_{L2} = 2C_S + C_L \cdot \frac{C_I + (2C_S)}{C_I} \qquad (4.19)$$

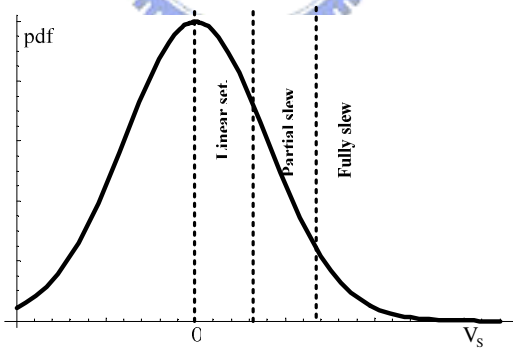


Fig. 4.7 Three types of settling conditions in integration phase

The GBW is given by

$$GBW = \frac{\text{gm1}}{C_{L2} \cdot 2\pi} \qquad (4.20)$$

In order to estimate settling noise in this phase, we must analyze the occurrence probability for each of the three conditions defined by(4.16)-(4.18). The probability

of V_S in the linear settling region is

$$\Pr_{lin} = \int_0^{\frac{1}{a_1}SR\cdot\tau_2} \frac{2}{\sqrt{2\pi}\cdot\sigma_{VS}} \exp(\frac{-V_S{}^2}{2\cdot\sigma_{VS}{}^2})\, dV_S = Erf[\frac{SR\tau_2}{\sqrt{2}a_1\sigma_{VS}}] \quad (4.21)$$

Let $\varepsilon_{2\max}$ be the maximum linear settling error, and it can be obtained by substituting $|V_S| = \frac{1}{a_1}\cdot SR\cdot\tau_2$ into (4.16). Since V_S is approximately Gaussian, it is reasonable to assume that the linear settling error in (4.16) also has a Gaussian distribution in $(-\varepsilon_{2\max}, \varepsilon_{2\max})$. So the average linear settling noise power in the integration phase is approximately

$$P_{lin} \approx \frac{\varepsilon_{2\max}{}^2}{9} = \frac{1}{9}\left(SR\cdot\tau_2 \exp(\frac{-T}{2\tau_2}) \right)^2 \quad (4.22)$$

Before calculating the partial settling probability, we must check the possibility of this condition. If $\frac{1}{a_1}\cdot SR\cdot\tau_2 \geq 2\mathrm{V_{ref}}$, a partial and fully slewing condition does not need to be considered. If $\frac{1}{a_1}SR\tau_2 < 2\mathrm{V_{ref}}$, partial slewing probability is

$$\Pr_{par} = Erf[\frac{SR(T+2\tau_2)}{2\sqrt{2}a_1\sigma_{VS}}] - Erf[\frac{SR\tau_2}{\sqrt{2}a_1\sigma_{VS}}] \quad (4.23)$$

Now we calculate noise power under the partial slewing condition. The pdf of V_S when $\frac{1}{a_1}\cdot SR\cdot\tau_2 < |V_S| < (\frac{T}{2}+\tau_2)\frac{SR}{a_1}$ is

$$f_{par}(V_S) = \frac{1}{\Pr_{par}} \cdot \frac{2}{\sqrt{2\pi}\cdot\sigma_{VS}} \exp(\frac{-V_S{}^2}{2\cdot\sigma_{VS}{}^2}) \quad (4.24)$$

The ε_2 here is no longer Gaussian distributed, and its pdf can be computed from

$$f_{par}(\varepsilon_2) = f_{par}(V_S)\cdot\frac{dV_S}{d\varepsilon_2} \quad (4.25)$$

where $\frac{dV_S}{d\varepsilon_2}$ can be obtained by (4.17), and its value is $\frac{SR\tau_2}{a_1\varepsilon_2}$. Then the average noise power of partial slewing is

$$P_{par} = \int_{\varepsilon_2|V_S=\frac{1}{a_1}SR\tau_2}^{\varepsilon_2|V_S=(\tau_2+\frac{T}{2})\frac{SR}{a_1}} f_{par}(\varepsilon)\cdot\varepsilon^2 d\varepsilon = \int_{V_S=\frac{SR\tau_2}{a_1}}^{V_S=\left(\tau_2+\frac{T}{2}\right)\frac{SR}{a_1}} f_{par}(V_S)\cdot\varepsilon_2{}^2 dV_S \quad (4.26)$$

Finally, we analyze the settling noise in a fully slewing condition using the same procedure. First, if $(\tau_2+\frac{T}{2})\frac{SR}{a_1}>2\mathrm{V}_{\mathrm{ref}}$, this condition will never occur. If $(\tau_2+\frac{T}{2})\frac{SR}{a_1}<2\mathrm{V}_{\mathrm{ref}}$, then the fully slewing probability is

$$\Pr_{ful}=Erf[\frac{2\mathrm{V}_{\mathrm{ref}}}{\sigma_{VS}}]-Erf[\frac{SR(T+2\tau_2)}{2\sqrt{2}a_1\sigma_{VS}}] \quad (4.27)$$

The p.d.f of V_S when $|V_S|>(\tau_2+\frac{T}{2})\frac{SR}{a_1}$ is

$$f_{ful}(V_S)=\frac{1}{\Pr_{ful}}\cdot\frac{2}{\sqrt{2\pi}\cdot\sigma_{VS}}\exp(\frac{-V_S{}^2}{2\cdot\sigma_{VS}{}^2}) \quad (4.28)$$

The p.d.f of ε_2 is

$$f_{ful}(\varepsilon_2)=f_{Vs}(V_S)\cdot\frac{dV_S}{d\varepsilon_2} \quad (4.29)$$

So, the average noise power of fully slewing is

$$P_{ful}=\int_{\varepsilon_2|V_S=(\tau_2+\frac{T}{2})\frac{SR}{a_1}}^{\varepsilon_2|V_S=2\mathrm{V}_{\mathrm{ref}}}f_{ful}(\varepsilon)\cdot\varepsilon^2d\varepsilon=\int_{V_S=(\tau_2+\frac{T}{2})\frac{SR}{a_1}}^{V_S=2V_{ref}}f_{ful}(V_S)\cdot\varepsilon_2{}^2dV_S \quad (4.30)$$

The total average settling noise in the integration phase can be obtained by (4.21), (4.22), (4.23), (4.26), (4.27) and (4.30) as

$$P_{\varepsilon_2}=\frac{P_{lin}\cdot\Pr_{lin}+P_{par}\cdot\Pr_{par}+P_{ful}\cdot\Pr_{ful}}{OSR} \quad (4.31)$$

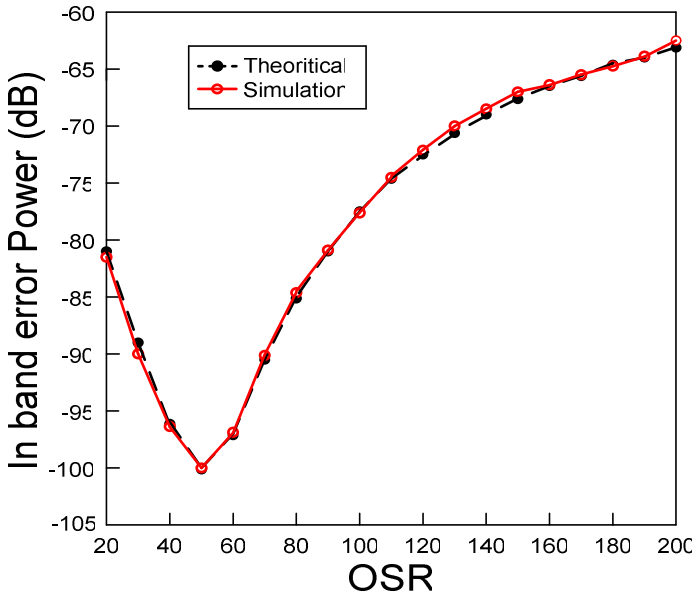


Fig. 4.8 Comparison of our theoretical result with behavior simulation result

In order to verify the result in（4.31）, we use SIMULINK to build a second-order ΣΔ modulator with a 4-bit quantizer. The behavioral settling model in [Mal 03] is used. We assume that $a_1 = 0.5$, $R = 300\Omega$, $C_S = 1.7$ pF, $GBW = 100$ MHz, $f_B = 300$ kHz and *SR* = 100V/μs, and use a 300 kHz sinusoidal input signal. In an ideal behavior simulation with a sinusoidal input, the error ε_2 can not be observed at modulator output, because ε_2 is highly correlated with V_S, so that ε_2 is compensated in the steady state by the integrator. However, adding a small noise to the input signal can eliminate the effects of feedback and integration. The Gaussian white noise added to the input has a small variance 0.04. After performing FFT to the ΣΔ modulator output data which exclude the input signal and Gaussian noise, we obtain simulated noise power, which is a combination of quantization noise and settling noise. The theoretical noise power is obtained by adding the theoretical settling noise power from（4.31）to the theoretical quantization noise power. The simulated and theoretical noise powers are both shown in Fig. 4.8 v.s. *OSR*. The two lines are closely related. When *OSR*<50, quantization noise dominates. When *OSR*>50, settling noise dominates. Notice that increasing *SR* and *GBW* will reduce settling noise and increase *SNR*, but will also increase analog power consumption and the design challenges. On the other hand, multi-bit quantizers can reduce the slew rate requirement, since a multi-bit structure makes the output feedback signal closer to the input signal.

4.4 Multi-bit DAC noise

There are several advantages in using a multi-bit structure. One is that when the quantization step Δ decreases, quantization and settling noise reduce. Another is that a multi-bit structure improves stability and provides a higher overload level and

more aggressive noise shaping function. However, due to CMOS process variations, there can be mismatches in the 2^B unit capacitors C_u of a *B*-bit DAC shown in Fig. 4.4. Assume that each unit capacitor distribution is Gaussian [Pel 89] around a nominal value. Let the normalized capacitance be

$$c_i = \frac{C_i}{\sum_{k=1}^{2^B} C_k}, \qquad 1 \le i \le 2^B \tag{4.32}$$

where C_i is the capacitance of the ith unit capacitor. Define the deviation of c_i as $e_i = c_i - c_m$, where

$$c_m = \frac{\sum_{i=1}^{2^B} c_i}{2^B} \tag{4.33}$$

Then voltage error caused by unit capacitor mismatches is given by [Gee 02]

$$e_{dac}(k) = V_{ref}\left(\sum_{i=1}^{x(k)} e_i - \sum_{i=x(k)+1}^{2^B} e_i\right) \tag{4.34}$$

where $x(k)$ represents the number of 1's in the feedback thermometer code at the time step k. The $e_{dac}(k)$ can be treated as an additive Gaussian noise in the ΣΔ modulator feedback path, the variance of which is

$$\begin{aligned}\sigma^2[e_{dac}] &= V_{ref}^{\ 2}\left(x(k)\cdot\sigma^2[e_i] + (2^B - x(k))\cdot\sigma^2[e_i]\right) \\ &= V_{ref}^{\ 2}\cdot 2^B\cdot\sigma^2[e_i] = V_{ref}^{\ 2}\cdot 2^B\cdot\sigma_{cap}^{\ 2}\end{aligned} \tag{4.35}$$

where σ_{cap} is the standard deviation of unit capacitor. Assuming the $e_{dac}(k)$ is also white, the average DAC noise power at the modulator output becomes

$$P_{dac} = \frac{1}{OSR}\cdot V_{ref}^{\ 2}\cdot 2^B\cdot\sigma_{cap}^{\ 2} \tag{4.36}$$

Apparently the dominating factor is *B*, since P_{dac} increases exponentially with respect to *B*. In order to reduce DAC error due to unit capacitor mismatch, several techniques have been proposed. The most efficient among these is the Data Weighted

Averaging (DWA) [Bai 95], and it is shown in [Nys 96] that the DWA effect is a first-order noise shaping of the DAC noise. If the DWA is employed, the average DAC noise power at the modulator output is modified to be

$$P_{dac}(DWA) \cong \mathrm{V_{ref}}^2 \cdot 2^B \cdot {\sigma_{cap}}^2 \cdot \frac{\pi^2}{3 \cdot OSR^3} \qquad (4.37)$$

Equations (4.36) and (4.37) will be used to estimate the DAC noise power in the optimization process.

4.5 Clock Jitter Effects

As both the signal bandwidth and the required output SNR increase, clock jitter problems become more obvious. Jitter is usually defined as a random variation in clock signal period around the ideal value, and the value of jitter can be reasonably assumed as a Gaussian random variable with zero mean and standard deviation σ_{jit}. If there is some variation in clock high time, the input signal will be sampled at the wrong instant and receive a consequent voltage error. For a sinusoidal input signal with maximum amplitude A_i and frequency f_{in}, if it is sampled by a clock which has a jitter variation, then the voltage error is [Bos 88]:

$$\Delta V \cong 2\pi \cdot f_{in} \cdot A_i \cos(2\pi \cdot f_{in} \cdot t)\Delta T \qquad (4.38)$$

where ΔT is the variation of clock period with standard deviation σ_{jit}. Then the jitter noise power becomes:

$$P_{jitter} = \frac{(2\pi \cdot f_{in} \cdot A_i)^2}{2} \cdot \frac{{\sigma_{jit}}^2}{OSR} \qquad (4.39)$$

We consider the worst case in this work. That is, f_{in} and A_i are replaced by f_B and V_{ref} respectively.

Before discussing power consumption modeling, we summarize the nonideality

modeling as follows. The leakage noise due to finite OTA gain can be considered as an additional quantization noise, so the total quantization noise will be higher than theoretical quantization noise, appearing at D2 in Fig. 4.9. All other nonidealities are modeled at D1 in Fig. 4.9, because we have modeled them as input-referred noise in the integrator input.

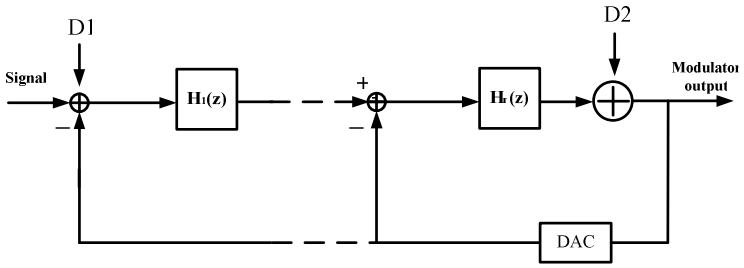


Fig. 4.9 Main nonidealities sources in the $\Sigma\Delta$ modulator

4.6 Relative Power Model

In order to understand how $\Sigma\Delta$ modulator power consumption is related to different circuit parameters, we must derive the power dissipation equation. Some derivations of this are based on the results presented in [Gee 02][Mar 98a][Lau 02]. It is difficult to estimate real system level power consumption, so our goal is not to estimate the absolute value of the power, but to find how power changes with circuit parameters; it is called the relative power consumption. Typically, $\Sigma\Delta$ ADC power consumption is categorized according to analog and the digital parts. In recent years, multi-bit quantization becomes popular, so the power dissipation in the quantizer has to be considered too. We analyze the analog part first. The analog power dissipation in a $\Sigma\Delta$ modulator is mainly from OTA, and is proportional to the product of several parameters:

$$POW_{OTA} \sim k_{OTA} \cdot V_{DD} \cdot \pi \cdot C_{L2} \cdot GBW \qquad (4.40)$$

where k_{OTA} is the number of current branches of OTA and V_{DD} is the power supply. The k_{OTA} depends on the topology of OTA. The first integrator is the most important

in terms of noise. Hence, all succeeding integrators are normally scaled down progressively to reduce the power consumption and die area. Consider that the sum of the relative scaling factors used in all the integrators of the $\Sigma\Delta$ is $k_{\Sigma\Delta}$. Then the analog power consumption equals $k_{\Sigma\Delta} \cdot POW_{OTA}$, where $k_{\Sigma\Delta}$ is proportional to the order n of the $\Sigma\Delta$ modulator. Assuming that the scaling factor is 0.5, then from （4.40）, the total analog power consumption is :

$$POW_{analog} \cong k_{\Sigma\Delta} \cdot POW_{OTA}$$

$$\sim \left(\sum_{i=0}^{n-1} (0.5)^i \right) \cdot k_{OTA} \cdot V_{DD} \cdot \pi \cdot C_{L2} \cdot GBW \qquad (4.41)$$

Since the analog power consumption is related to n, V_{DD}, C_{L2} and GBW, are important circuit parameters to be determined in the design flow.

Next, we discuss digital power consumption. Digital power consumption is mainly from MOS switch operation, and is proportional to the product of another set of parameters:

$$POW_{SW} \sim n \cdot 2^B \cdot C_{Switch} \cdot V_{DD}{}^2 \cdot 2 \cdot f_B \cdot OSR \qquad (4.42)$$

where $2 \cdot f_B \cdot OSR$ is equal to the sampling frequency, and C_{Switch} is the total gate capacitance of switches. The value of C_{Switch} is inversely proportional to the switch-on resistance *R* [Wes 94], so we define the relative digital power as

$$POW_{digital} \sim n \cdot 2^B \cdot \frac{1}{R} \cdot V_{DD}{}^2 \cdot f_S \qquad (4.43)$$

Next we discuss quantizer power consumption. For 1-bit $\Sigma\Delta$ modulators, a comparator is used as the quantizer, so its power consumption can be neglected compared to the integrator power. In the multi-bit ADC, this is not true. A simple power estimation formula of Nyquist ADC [Lau 02] is

$$P_{quantizer} = \frac{V_{DD}{}^2 \times L_{\min} \times (fs + f_B)}{10^{(-0.1525 \times B + 4.838)}} \qquad (4.44)$$

where $L_{\min}$ is the minimum channel length of the technology associated, which in our case is $0.18\times10^{-6}m$.

According to the above discussion, the total relative power is defined as

$$Power = K_1 \times POW_{ana\log} + K_2 \times POW_{digital} + P_{quantizer} \qquad (4.45)$$

where K_1 and K_2 are adjusted to make Power (in mW) comparable in magnitude with real power dissipations. After comparing with power measurements reported in [Gag 03][Mil 03], we set $K_1 = 0.03651$ and $K_2 = 3.6877\times10^{-10}$. Both [Gag 03] and [Mil 03] are based on 0.18-μm CMOS technology. For other CMOS technologies, the K_1 and K_2 may be set to other appropriate values.

Dynamic element matching (DEM) [Bai 95][Nys 96] is based on scrambling the use of the unit elements in a multi-bit DAC to average out nonlinearity and turn distortion into noise. There are many DEM algorithms and the most common DEM algorithms are based on first order noise-shaping, with DWA being the most popular of these. One of the main advantages of the DWA algorithm is its simplicity. In some designs, the logic in the quantizer, the DEM algorithm and the decimation filter run at a lower supply voltage to reduce the digital power consumption. Also, the DEM logic grows exponentially in complexity, size, and power dissipation as the internal quantizer bit increases. And the power consumption of DEM depends on CMOS technology. Therefore, we do not try to calculate the power consumption for any specific type of DEM scheme. Instead, picking a medium value, we assume DEM power is 0.6×Power if DEM is employed.

5

Models of Sigma-Delta Modulator Nonlinear Distortion

5.1 Settling Distortion

We analyze incomplete transfer of charge in a SC integrator to obtain analytical models to represent harmonic distortion as function of the operational amplifier finite gain-bandwidth (*GBW*), slew-rate (*SR*). The model developed here assumes the effect of the *SR* in a SC integrator may be interpreted as a nonlinear gain. Consider the integrator operates in the integration phase. As discussed in Chapter 4, there are three settling conditions depending on the absolute value of V_S [Mal 03].

1. Linear settling $\left(|V_S| < \frac{1}{a_1} \cdot SR \cdot \tau_2\right)$:

We can represent integrator output voltage during the *n*th integration interval as

$$V_O(t) = V_O(nT - T) + a_1 V_S\left(1 - e^{\frac{-(t - nT + \frac{T}{2})}{\tau_2}}\right) \quad , \quad nT - \frac{T}{2} < t < nT \qquad (5.1)$$

2. Partial slewing $\left(\frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S|\right)$:

$$V_O(t) = V_O(nT - T) + SR \cdot (t_0 - nT + \frac{T}{2}) + \left[a_1 V_S - SR \cdot (t_0 - nT + \frac{T}{2})\right]\left(1 - e^{\frac{-(t - t_0)}{\tau_2}}\right)$$

$$t > t_0 \qquad (5.2)$$

where t_0 is the time instant when V_O rate becomes less than *SR*. The full slewing case is not considered here because it is not significant. Note that (5.1) and (5.2) at end of each integration interval can be rewritten as

$$V_O(nT) = V_O(nT - T) + a_1 V_S\left(1 - e^{-\left(\frac{T}{2\tau_2} + 1\right)} \cdot e\right) = V_O(nT - T) + a_1 V_S(1 - \beta \cdot e) \quad , \quad |V_S| \le V_L$$

$$V_O(nT) = V_O(nT-T) + a_1 V_S\left[1 - \frac{SR\tau_2}{a_1 V_S}\cdot e^{-\left(\frac{T}{2\tau_2}-\frac{a_1 V_S}{SR\tau_2}+1\right)}\right]$$

$$= V_O(nT-T) + a_1 V_S\left[1 - \frac{V_L}{V_S}\cdot \beta e^{|V_S|/V_L}\right] \quad , \qquad |V_S| > V_L \tag{5.3}$$

where $\beta = e^{-(T/(2\tau_2)+1)}$; $V_L = SR\tau_2 / a_1$

Let $$g_i(V_S) = \begin{cases} a_1(1-\beta e) \ ; & |V_S| \le V_L \\ a_1\left(1 - \frac{V_L}{V_S}\beta e^{|V_S|/V_L}\right) ; & |V_S| > V_L \end{cases} \tag{5.4}$$

which is the integrator gain. Harmonic distortions are produced at the modulator output when op-amps operate in the partial slewing region, because in the partial slewing region the integrator gain is a function of input V_S. In order not to produce harmonic distortion, op-amps should always operate in the linear region. From (5.4), we can see that if $|V_S| \le V_L$ is satisfied all the time, the modulator always operates in linear region and harmonic distortion would not be produced. $|V_S| \le V_L$ can be further derived as:

$$|V_S| \le V_L$$

$$\Rightarrow 2A\omega T \le \frac{SR\tau}{0.5}$$

$$\Rightarrow 2A\cdot 2\pi\cdot f_{in}\cdot\frac{1}{2\times BW\times OSR} \le \frac{SR}{0.5}\cdot\frac{1+2\pi\cdot GBW\cdot RC_S}{2\pi\cdot GBW}$$

Assuming $f_{in} = BW$, $R = 300\Omega$, $C_S = 2\times 10^{-12} F$, it leads to the following equation:

$$OSR \ge \frac{\pi}{SR\left(\frac{1}{2\pi\cdot GBW} + 6\times 10^{-10}\right)} \tag{5.5}$$

We then plot (5.5) as shown in Fig. 5.1 which shows that *OSR* is inverse proportional to *SR* and is almost independent to *GBW*.

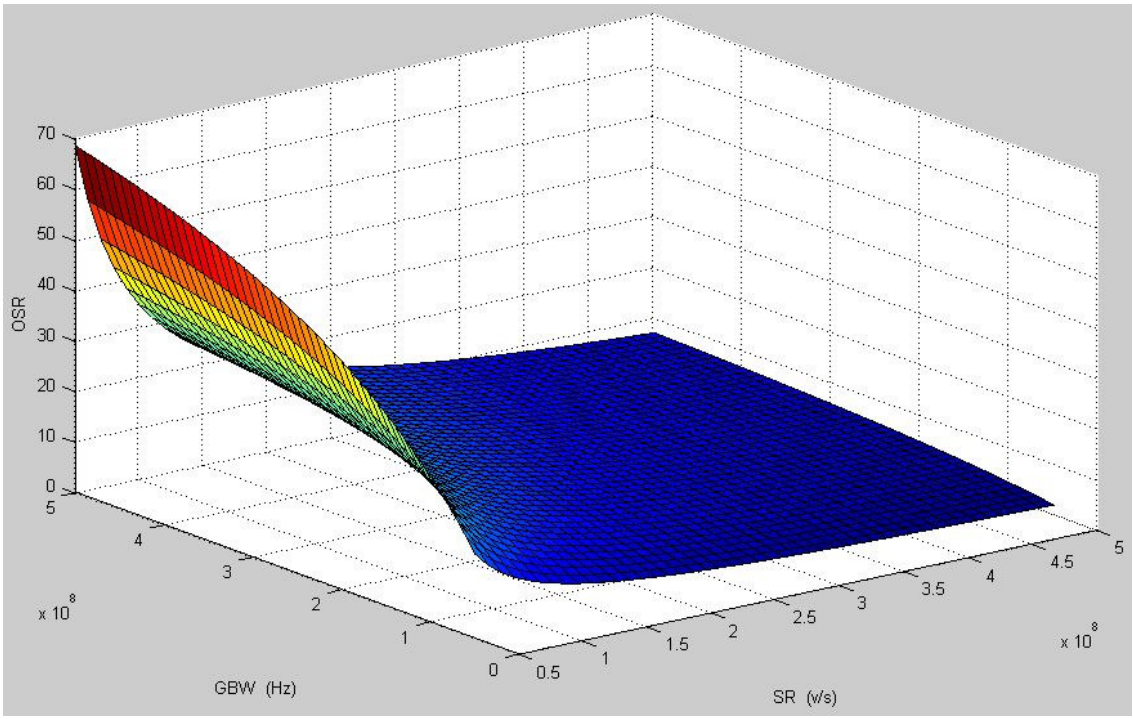


Fig. 5.1 3D plot of（5.5）

Fig. 5.1 indicates that if we design *SR* and *GBW* above the curve with desired *OSR*, the modulator would have no harmonic distortion. It shows that the op-amp slew rate needs to be at least 200V/us, then the modulator can have no harmonic distortions with *OSR* larger than 15. Although op-amps operate in linear region can have no harmonic distortion, it may consume more power dissipation (because large slew rate). Therefore, there has a trade off between power consumption and harmonic distortion. In general, one can choose smaller slew rate to let power consumption lower and have negligible harmonic distortions. In the following, we analyses the influences of slew rate on harmonic distortion when op-amps operate in partial slewing region.

Assume that $g_i(v)$ can be approximated by

$$p_i(v) = a_1 \cdot (\alpha_1 + \alpha_3 v^2 + \alpha_5 v^4) \qquad (5.6)$$

In this point, the problem of estimating harmonic distortion consists of searching for the curve with the form shown in（5.6）which best fits（5.4）for a specific interval.

We will use the least square method to determine the coefficient α_1, α_3 and α_5 to fit（5.4）. The $p_i(v)$ should be fitted through all the points in that specific interval so that the sum of the squares of the distances of those points from the $p_i(v)$ is minimum. The sum of the squares is

$$q = \sum_{j=1}^{n} \left[g_i(x_j) - p(x_j) \right]^2$$

$$= \sum_{j=1}^{n} \left[g_i(x_i) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right]^2$$

q depends on α_1, α_3 and α_5. A necessary condition for q to be minimum is

$$\begin{cases} \dfrac{\partial q}{\partial \alpha_1} = \sum_{j=1}^{n} 2\left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](-a_1) = 0 \\ \dfrac{\partial q}{\partial \alpha_3} = \sum_{j=1}^{n} 2\left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](-a_1 x_j^2) = 0 \\ \dfrac{\partial q}{\partial \alpha_5} = \sum_{j=1}^{n} 2\left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](-a_1 x_j^4) = 0 \end{cases}$$

With this method, the calculation of the coefficients in（5.6）becomes the solution of the following system of linear equations:

$$\begin{cases} \sum_{j=1}^{n} \left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right] = 0 \\ \sum_{j=1}^{n} \left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](x_j^2) = 0 \\ \sum_{j=1}^{n} \left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4} \right](x_j^4) = 0 \end{cases}$$

$$\Rightarrow \begin{cases} a_1\left(\sum_{j=1}^{n} \alpha_1 + \sum_{j=1}^{n} \alpha_3 x_j^2 + \sum_{j=1}^{n} \alpha_5 x_j^4 \right) = \sum_{j=1}^{n} g_i(x_j) \\ a_1\left(\sum_{j=1}^{n} \alpha_1 x_j^2 + \sum_{j=1}^{n} \alpha_3 x_j^4 + \sum_{j=1}^{n} \alpha_5 x_j^6 \right) = \sum_{j=1}^{n} g_i(x_j) \cdot x_j^2 \\ a_1\left(\sum_{j=1}^{n} \alpha_1 x_j^4 + \sum_{j=1}^{n} \alpha_3 x_j^6 + \sum_{j=1}^{n} \alpha_5 x_j^8 \right) = \sum_{j=1}^{n} g_i(x_j) \cdot x_j^4 \end{cases}$$

$$\Rightarrow \begin{cases} a_1\left(\int_0^{Vh}\alpha_1+\int_0^{Vh}\alpha_3 x_j^2+\int_0^{Vh}\alpha_5 x_j^4\right)=\int_0^{Vh} g_i(x_j) \\ a_1\left(\int_0^{Vh}\alpha_1 x_j^2+\int_0^{Vh}\alpha_3 x_j^4+\int_0^{Vh}\alpha_5 x_j^6\right)=\int_0^{Vh} g_i(x_j)x_j^2 \\ a_1\left(\int_0^{Vh}\alpha_1 x_j^4+\int_0^{Vh}\alpha_3 x_j^6+\int_0^{Vh}\alpha_5 x_j^8\right)=\int_0^{Vh} g_i(x_j)x_j^4 \end{cases}$$

where V_h is the distribution range of the first integrator input V_S.

$$\Rightarrow \begin{cases} a_1\left(\int_0^{Vh}\alpha_1+\int_0^{Vh}\alpha_3 x_j^2+\int_0^{Vh}\alpha_5 x_j^4\right)=\int_0^{VL} a_1(1-\beta e)\,dV_S+\int_{VL}^{Vh} a_1(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})\,dV_S \\ a_1\left(\int_0^{Vh}\alpha_1 x_j^2+\int_0^{Vh}\alpha_3 x_j^4+\int_0^{Vh}\alpha_5 x_j^6\right)=\int_0^{VL} a_1(1-\beta e)\cdot V_S^{\,2}\,dV_S+\int_{VL}^{Vh} a_1(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})V_S^{\,2}\,dV_S \\ a_1\left(\int_0^{Vh}\alpha_1 x_j^4+\int_0^{Vh}\alpha_3 x_j^6+\int_0^{Vh}\alpha_5 x_j^8\right)=\int_0^{VL} a_1(1-\beta e)\cdot V_S^{\,4}\,dV_S+\int_{VL}^{Vh} a_1(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})V_S^{\,4}\,dV_S \end{cases}$$

$$\begin{bmatrix}\alpha_1\\ \alpha_3\\ \alpha_5\end{bmatrix}=\begin{bmatrix} \frac{225}{64\cdot Vh} & \frac{-525}{32\cdot Vh^3} & \frac{945}{64\cdot Vh^5} \\ \frac{-525}{32\cdot Vh^3} & \frac{2205}{16\cdot Vh^5} & \frac{-4725}{32\cdot Vh^7} \\ \frac{945}{64\cdot Vh^5} & \frac{-4725}{32\cdot Vh^7} & \frac{11025}{64\cdot Vh^9}\end{bmatrix}\begin{bmatrix} \int_0^{VL}(1-\beta e)\,dV_S+\int_{VL}^{Vh}(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})\,dV_S \\ \int_0^{VL}(1-\beta e)\cdot V_S^{\,2}\,dV_S+\int_{VL}^{Vh}(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})V_S^{\,2}\,dV_S \\ \int_0^{VL}(1-\beta e)\cdot V_S^{\,4}\,dV_S+\int_{VL}^{Vh}(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})V_S^{\,4}\,dV_S\end{bmatrix} \quad (5.7)$$

The amplitudes of the third and fifth harmonics of the modulator output are:

$$A_3 \cong \frac{|\alpha_3|A_{VS}^3}{4} \quad ; \quad A_5 \cong \frac{|\alpha_5|A_{VS}^5}{16} \qquad (5.8)$$

where A_{VS} is the amplitude of V_S. However, in [Med 94], A_{in} instead of A_{VS} is employed in (5.8), where A_{in} is the amplitude of a sinusoidal modulator input signal. It is intuitively clear that using A_{in} is not correct, and our simulation shows that (5.8) is correct and precise. Next we need to obtain an expression for A_{VS}.

$$V_S(z)=X(z)-Y(z) \qquad (5.9)$$

In a second-order ΣΔ modulator, modulator output signal *Y(z)* is the time delay version of *X(z)* plus high-pass filtered (noise shaped) quantization noise E(z). Therefore,

$$Y(z)=z^{-2}X(z)+(1-z^{-1})^2E(z) \qquad (5.10)$$

Combining（5.9）and（5.10）, $V_S(z)$ can be written as

$$V_S(z) = X(z)\left[1 - z^{-2}\right] - (1 - z^{-1})^2 E(z) \qquad (5.11)$$

Ignoring the quantization noise and taking the inverse z-transform, one obtains

$$\begin{aligned} V_S(t) &= x(t) - x(t-2T)u(t-2T) \\ &= A_{in}\sin(\omega t) - A_{in}\sin(\omega(t-2T)) \cdot u(t-2T) \end{aligned} \qquad (5.12)$$

Then, the amplitude of V_S can be obtained as

$$A_{VS} = V_S(2T) = x(2T) = A_{in}\sin(\omega \cdot 2T) \cong 2A_{in} \cdot \omega \cdot T \qquad (5.13)$$

Note that A_{VS} is not related to quantizer bit number *B* which can only affect the level of noise floor $E(\omega)$. The result(5.13)has been verified by behavior simulation under different *B* values, as shown in Fig. 5.2. From（5.8）(5.13）, we can see that input signal amplitude A_{in}, input signal frequency ω and sampling time *T* are the critical parameters to impact the harmonic distortion.

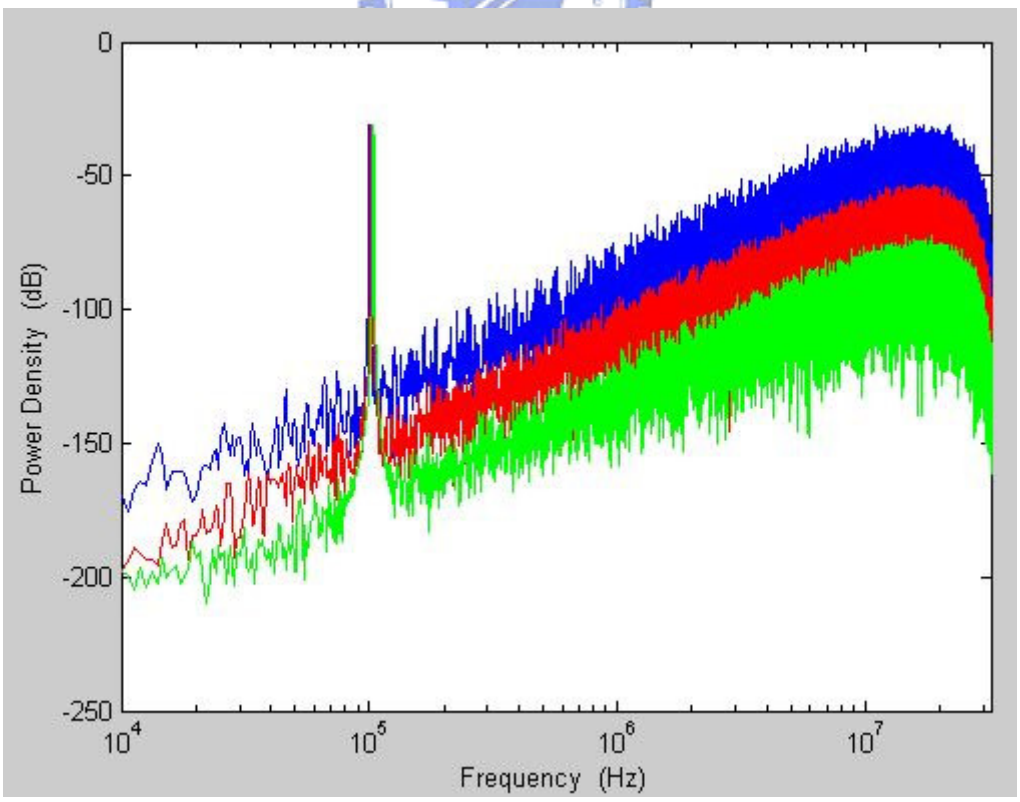


Fig. 5.2 Spectrum of V_S with different quantizer bit number

In order to verify the result in （5.8）, we use SIMULINK to build a second-order ΣΔ modulator with a multi-bit quantizer. The behavioral settling model in [Mal 03] is employed. We assume that $SR = 70V/\mu s$, GBW = 100MHz, $R = 300\Omega$, OSR = 16, f_B = 1MHz and C_S = 2pF, and a 1MHz sinusoidal input signal is used. After performing FFT to the output data of the ΣΔ modulator, we obtain the simulated PSD (Power Spectrum Density) which is shown in Fig. 5.3. It shows that HD3 is -112.5dB and HD5 is -117.5dB. The theoretical harmonic powers calculated from （5.7）and（5.8）are HD3 = -112.4dB and HD5 = -117.3dB. The simulated and theoretical results are very close, and this confirms that our settling distortion model is reasonably precise.

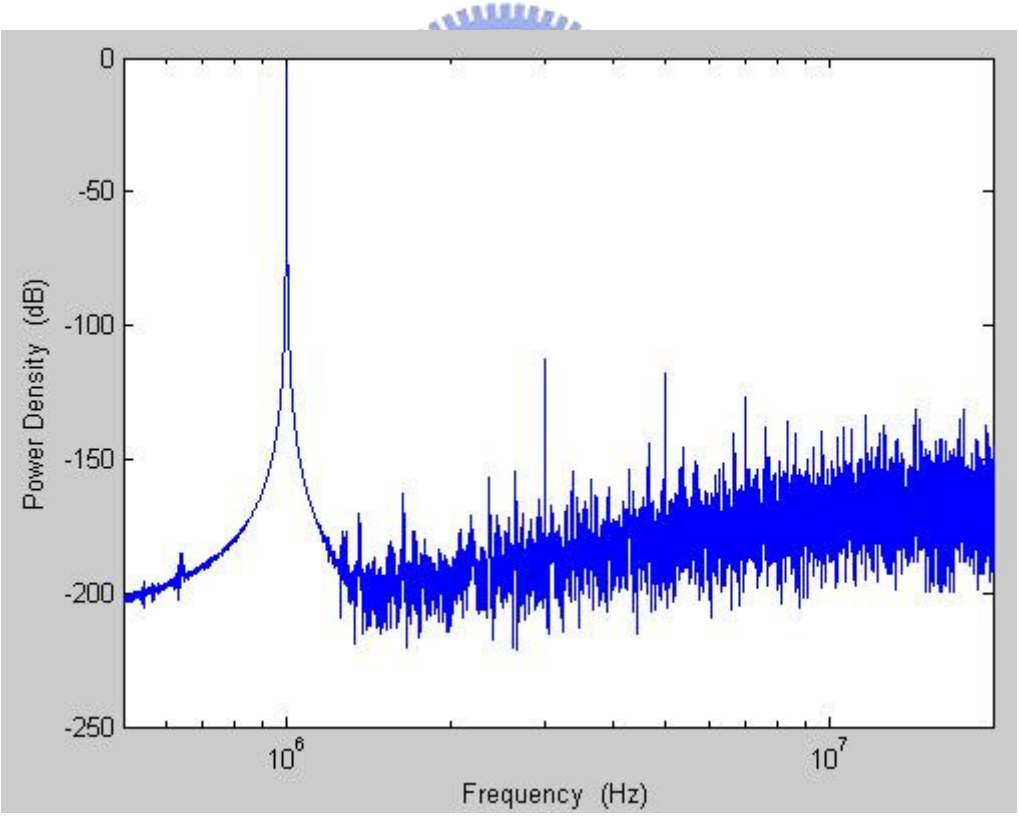


Fig. 5.3 Output spectrum of a second-order ΣΔ modulator with harmonic distortion

In order to provide insight on how settling distortions are related to circuit and

system parameters, we further analyze the 3rd and 5th harmonic powers as follows:

$$HD3(dB) = 20\log\left(\frac{1}{\sqrt{2}}\left(\frac{|\alpha_3|A_{VS}^3}{4}\right)\right)$$

$$= 20\left[\log|\alpha_3| + \log(2A\omega T)^3 - \log 4\sqrt{2}\right]$$

$$= 20\log|\alpha_3| - 60\log OSR + 30.095 \qquad (5.14)$$

$$HD5(dB) = 20\log|\alpha_5| - 100\log OSR + 48.15$$

From (5.14) we can see that *OSR* can effectively influence settling harmonic powers. The(5.7)reveals that α_3 and α_5 are functions of *T*, *GBW*, *R*, C_S and *SR*. Using the parameters designed in Chapter 7 with f_S = 52MHz, *R* = 300ohm, C_S= 1.7pF, and setting *GBW* and *SR* at medium values as *GBW* = 250MHz and *SR* = 250V/μs, we plot $20\log|\alpha_3|$ vs. *SR* in Fig. 5.4 and $20\log|\alpha_3|$ vs. *GBW* in Fig. 5.5.

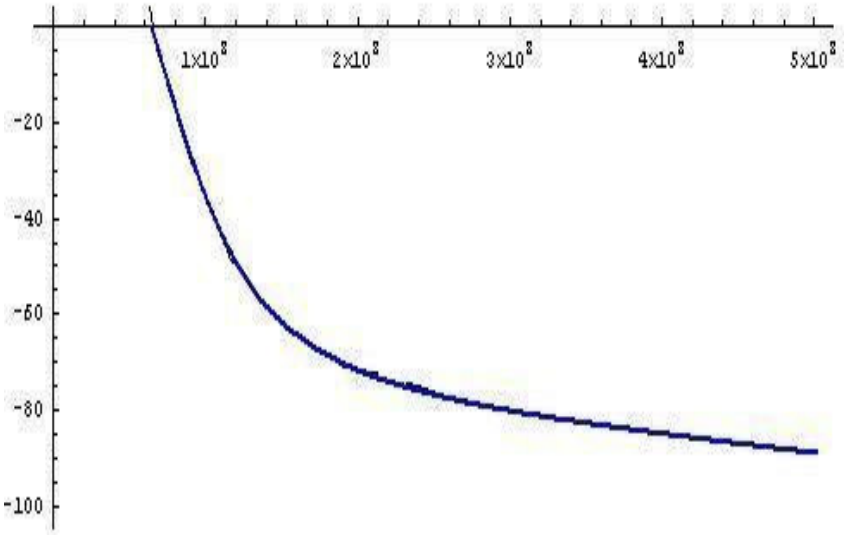


Fig. 5.4 $20\log|\alpha_3|$ vs. *SR*

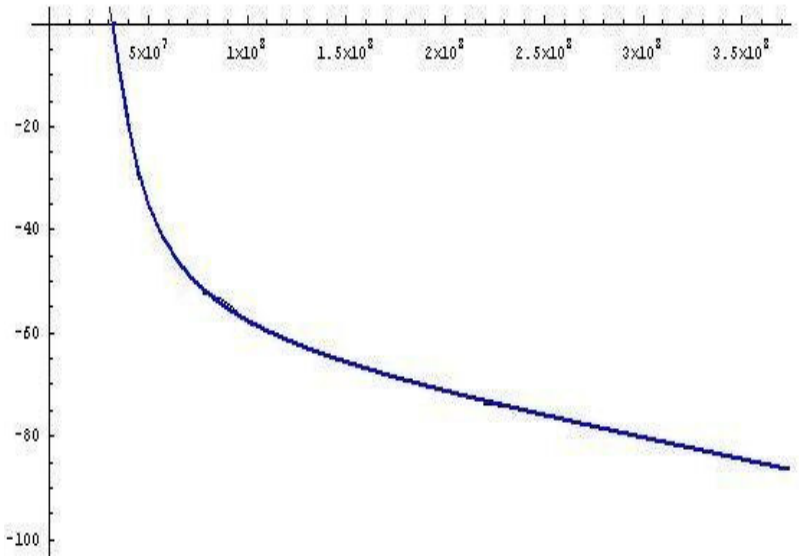


Fig. 5.5 $20\log|\alpha_3|$ vs. *GBW*

In general, harmonic distortion less than -110dB can be ignored because it is below the noise floor of modulator output spectrum. From（5.14）, Fig. 5.4 and Fig. 5.5, we can obtain the minimum required *SR* and *GBW* w. r. t. a specific *OSR*. The results are summarized in Table 5.1.

OSR	**HD3(dB)**	***SR*** $(V/\mu s)$	***GBW*** **(MHz)**
8	$20\log\|\alpha_3\|$ **-24**	≥ 500	≥ 380
16	$20\log\|\alpha_3\|$ **-42**	≥ 200	≥ 180
32	$20\log\|\alpha_3\|$ **-60**	≥ 120	≥ 70
50	$20\log\|\alpha_3\|$ **-72**	≥ 110	≥ 60
64	$20\log\|\alpha_3\|$ **-78**	≥ 100	≥ 50
96	$20\log\|\alpha_3\|$ **-89**	≥ 90	≥ 40

Table 5.1 Minimum *SR* and *GBW* required w. r. t. *OSR*

It is clear from Table 5.1 that as *OSR* decreases, *SR* and *GBW* have to increase dramatically so that the effect of settling distortion can be contained. This can be explained by（5.13）, since *T* increases when *OSR* decreases.

5.2 Quantizer Nonlinearity Distortion

The quantization operation is inherently nonlinear because the quantizer error is determined from the quantizer input signal. For convenience, we usually model the quantizer as a linear model and approximate the quantization noise as a white noise. This approximation is made when the quantization error has the following properties, which we refer to collectively as the "input-independent additive white noise approximation" [Nor 97]:

Property 1. ε_n is statistically independent of the input signal or ε_n is uncorrelated with the input signal.

Property 2. ε_n is uniformly distributed in $[-\Delta/2, \Delta/2]$.

Property 3. ε_n is an independent identically distributed sequence or ε_n has a flat power spectral density.

where ε_n is the error sequence and Δ is the distance between output levels. Therefore, the quantization error from $\Sigma\Delta$ modulators is typically not white. For dc inputs, the quantization error is periodic, generating idle channel tones or pattern noise. For ac inputs, the quantization error is also periodic, containing components harmonically related to the input frequency and amplitude. One can view this effect as a time-domain distortion and therefore argue that the converter actually has less resolution than rms measurements. From the properties described above, one can see that multi-bit quantizers are closer to the linear model than single-bit ones and the time-domain distortions of multi-bit quantizers can be ignored, as shown in Fig. 5.6.

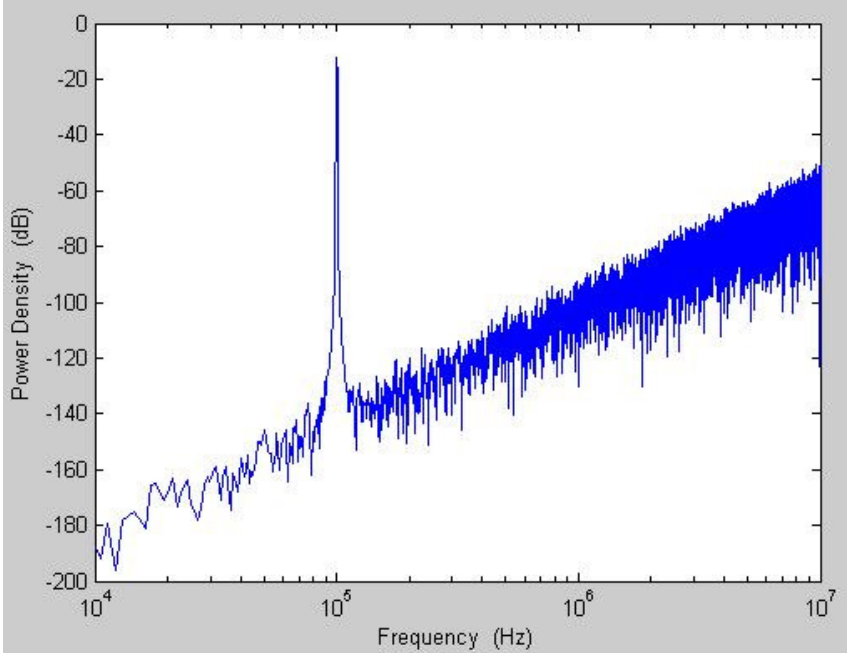


Fig. 5.6 PSD of second-order $\Sigma\Delta$ modulator with 5 quantization levels

From Fig. 5.6, we can see that the quantization noise is almost white and harmonic distortion is unapparent.

5.3 Multi-bit DAC Distortion

Recently, multi-bit modulators are used often because it offers many advantages. However, multi-bit modulators using multi-bit DACs can introduce significant distortion into the modulator loop. Any error in the DAC response will be directly subtracted from the input signal and hence it appears at the output without the benefit of noise shaping. And any nonlinearity of the DAC will introduce a corresponding nonlinear signal distortion into the overall ADC response.

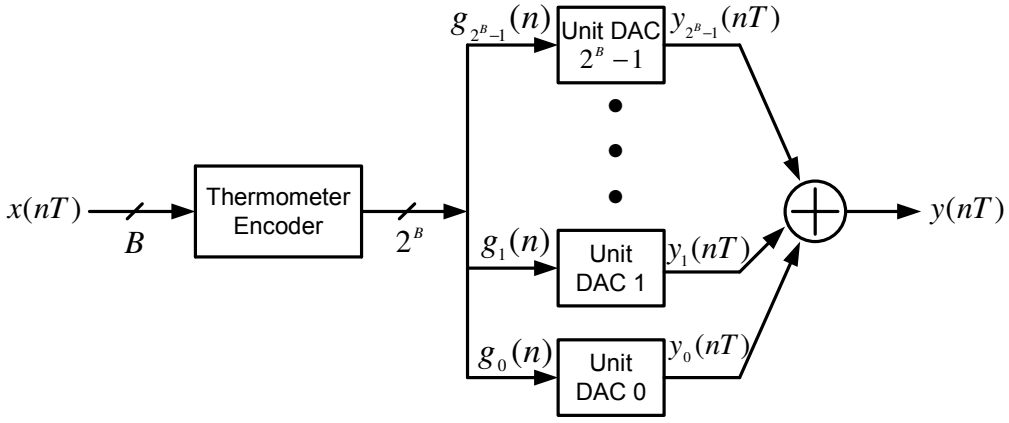


Fig. 5.7 A block diagram of a B-bit flash DAC

Fig. 5.7 shows a block diagram of a common B-bit flash DAC that relies on matched components between the unit DACs [Stu 01]. We define the output $y_k(nT)$ of the *k*th unit DAC as

$$y_k(nT)=\begin{cases} a_k, & g_k(n)=1 \\ d_k, & g_k(n)=0 \end{cases}$$

where a_k and d_k are the values of the activated and deactivated *k*th unit DAC, respectively. If $\bar{a}$ and $\bar{d}$ are defined as the average values of the activated and deactivated unit DACs, respectively, $y_k(nT)$ can also be rewritten as

$$y_k(nT)=\begin{cases} \bar{a}+h_k, & g_k(n)=1 \\ \bar{d}+l_k, & g_k(n)=0 \end{cases}$$

where h_k is the activated mismatch error of the kth unit DAC, and l_k is the deactivated mismatch error of the kth unit DAC. These errors h_k and l_k are random variables and they have the same standard deviations. The DAC's analog output $y(nT)$ can be written as

$$y(nT)=\sum_{k=0}^{2^B-1} y_k(nT) \qquad (5.15)$$

For a particular DAC input level, the DAC output will produce a corresponding value which is the sum of the unit DACs. Therefore, the DAC output value will contain the

sum of the random variables h_k and l_k. Assuming the thermometer encoder activates $\chi(n)$ unit DACs and deactivates the remaining $2^B - \chi(n)$ unit DACs, (5.15)can be written as

$$y(nT) = \chi(n) \cdot \left[\bar{a} + h_k\right] + \left(2^B - \chi(n)\right) \cdot \left[\bar{d} + l_k\right]$$

$$= \chi(n) \cdot \left(\bar{a} - \bar{d}\right) + 2^B \bar{d} + \chi(n) h_k + \left(2^B - \chi(n)\right) l_k \qquad (5.16)$$

Because h_k and l_k are random variables and have the same standard deviations, (5.16) can be written as

$$y(nT) = \chi(n) \cdot \left(\bar{a} - \bar{d}\right) + 2^B \bar{d} + 2^B l_k \qquad (5.17)$$

where $2^B l_k$ is the DAC output error and it is proportional to the unit DAC number 2^B and mismatch error l_k. As shown in Fig. 5.8(a) is an ideal DAC and Fig. 5.8 (b) is a DAC with mismatch. The DAC output level is the DAC unit number plus one. From Fig. 5.8(b) we can see that the DAC output levels are not equally spaced which results in the harmonic distortion, undesirable tones, as well as noise.

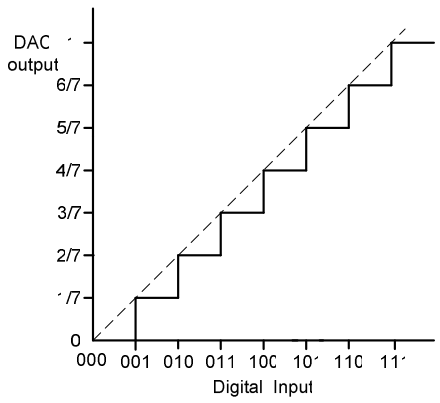


Fig. 5.8(a) Ideal DAC

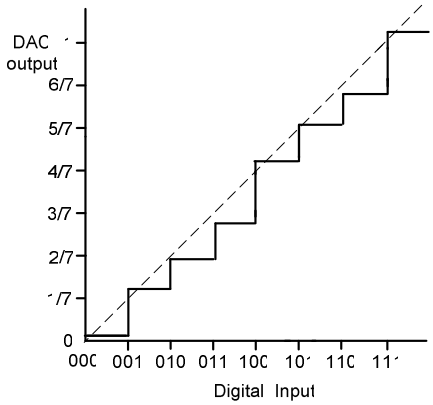
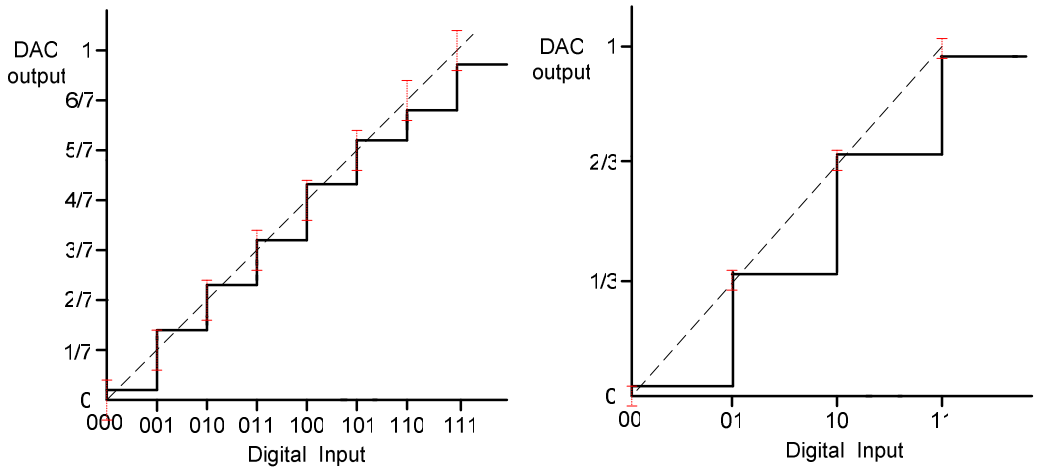
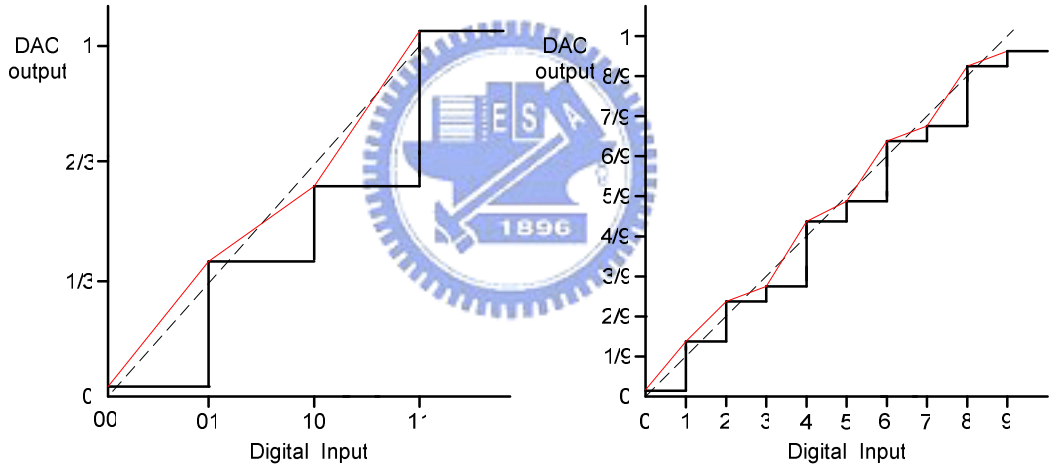


Fig. 5.8(b) DAC with mismatch



(a) (b)

Fig. 5.9 DAC transfer curve: (a) DAC with larger DAC output error, and (b) DAC with smaller DAC output error



(a) (b)

Fig. 5.10 DAC transfer curve: (a) DAC with smaller output level, and (b) DAC with larger output level

Fig. 5.9 describes the DAC transfer curves with different DAC output error $2^B l_k$. From Fig. 5.9 we can see that the deviation of the non-ideal output level from the ideal one is equal to the DAC output error so that the deviation is related to the mismatch error h_k, l_k and unit DAC number 2^B. The larger the DAC output error is, the larger the deviation. Fig. 5.10 describes DAC transfer curves with different output

levels. From Fig. 5.10 we can see that the frequency of levels oscillating up or below the ideal ones is relative to DAC output level. The larger the output level is, the larger the oscillation frequency, but they are independent of the deviations. The discussions in Fig. 5.9 and Fig. 5.10 can provide us the tendency of deviations and frequencies of DAC transfer curves and what parameters they related to.

Therefore, assuming the deviation is A and frequency is a, from the above discussions, we assume the DAC output value can be written as

$$y(nT) = x(nT) + A\sin(a \cdot x(nT) + \theta) \qquad (5.18)$$

where $x(nT)$ is the DAC input, θ is a uniformly distributed random variable in $[0,2\pi]$ and $A\sin(a \cdot x(nT) + \theta)$ represent the effect of random variables h_k and l_k on the transfer curve. In $\Sigma\Delta$ modulator, $x(nT)$ is also the modulator output so it is usually a sinusoid $A_{in}\sin(\omega nT)$. From Fig. 5.8 and the DAC output error $2^B l_k$, we can expect the value of A is a function of the unit DAC number and standard deviation of capacitor mismatch, and the larger the DAC output error is, the larger the A. From Fig. 5.9 we expect a is a function of DAC output level and in a fixed input range the larger the output level is, the larger the radian frequency a.

In (5.18), $A\sin(ax + \theta)$ representing mismatches errors h_k and l_k can be further derived as:

$$\begin{aligned} A\sin(ax + \theta) &= A(\sin ax\cos\theta + \cos ax\sin\theta) \\ &= A\cos\theta\sin ax + A\sin\theta\cos ax \end{aligned} \qquad (5.19)$$

Utilizing Taylor's series, (5.19) can be expanded as follows:

$$A\cos\theta \times \sum_{n=0}^{\infty}(-1)^n \frac{(ax)^{2n+1}}{(2n+1)!} + A\sin\theta \times \sum_{n=0}^{\infty}(-1)^n \frac{(ax)^{2n}}{(2n)!}$$

$$= a_0 + a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4 + a_5 x^5 + \cdots$$

where $a_2 = A\sin\theta\left(-\frac{a^2}{2}\right), a_3 = A\cos\theta\left(-\frac{a^3}{6}\right), a_4 = A\sin\theta\frac{a^4}{24}, \cdots$

Therefore, when a sine-wave is applied to the modulator input such that $x(nT)=A_{in}\sin(\omega nT)$, the modulator output will produce harmonics due to the high order terms. These harmonics are represented in power form below:

$$HD2=\frac{1}{2}\left(\frac{a_2}{2}A_{in}^2+\frac{a_4}{2}A_{in}^4+\frac{15a_6}{32}A_{in}^6+\cdots\right)^2=\frac{1}{2}\left(\frac{a_2'}{2}A_{in}^2+\frac{a_4'}{2}A_{in}^4+\frac{15a_6'}{32}A_{in}^6+\cdots\right)^2\cdot\sin^2\theta$$

$$HD3=\frac{1}{2}\left(\frac{a_3}{4}A_{in}^3+\frac{5a_5}{16}A_{in}^5+\cdots\right)^2=\frac{1}{2}\left(\frac{a_3'}{4}A_{in}^3+\frac{5a_5'}{16}A_{in}^5+\cdots\right)^2\cdot\cos^2\theta$$

$$HD4=\frac{1}{2}\left(\frac{a_4}{8}A_{in}^4+\frac{3a_6}{16}A_{in}^6+\cdots\right)^2=\frac{1}{2}\left(\frac{a_4'}{8}A_{in}^4+\frac{3a_6'}{16}A_{in}^6+\cdots\right)^2\cdot\sin^2\theta$$

where $a_2'=A\left(-\frac{a^2}{2}\right), a_3'=A\left(-\frac{a^3}{6}\right), a_4'=A\cdot\frac{a^4}{24},\cdots$

Because θ is a uniformly distributed random variable in $[0,2\pi]$, the expected value of these harmonic powers can be further represent

$$E[HD2]=\frac{1}{2}\left(\frac{a_2'}{2}A_{in}^2+\frac{a_4'}{2}A_{in}^4+\frac{15}{32}a_6'A_{in}^6+\cdots\right)^2\cdot E[\sin^2\theta]$$

$$E[HD3]=\frac{1}{2}\left(\frac{a_3'}{4}A_{in}^3+\frac{5}{16}a_5A_{in}^5+\cdots\right)^2\cdot E[\cos^2\theta]$$

$$E[HD4]=\frac{1}{2}\left(\frac{a_4'}{8}A_{in}^4+\frac{3}{16}a_6'A_{in}^6+\cdots\right)^2\cdot E[\sin^2\theta]$$

where $E[\sin^2\theta]$, $E[\cos^2\theta]$ is equivalent to 0.5. Finally, we further derive these harmonic distortions as a function of *A* and *a* and express in dB as follows.

$$E[HD2]\cong 20\log A\cdot\left|-0.125a^2A_{in}^2+0.010415a^4A_{in}^4-0.0003255a^6A_{in}^6\right|$$

$$E[HD3]\cong 20\log A\cdot\left|-0.02083a^3A_{in}^3+0.00130208a^5A_{in}^5\right|$$

$$E[HD4]\cong 20\log A\cdot\left|0.002604a^4A_{in}^4-0.00013021a^6A_{in}^6\right| \qquad (5.20)$$

In order to obtain *A* and *a*, we build a behavioral model of DAC including the mismatch of unit-elements and the unit-elements mismatches are assigned a Gaussian distribution with a specific standard deviation. By use of this DAC model and behavior simulation, simulations results on a second-order ΣΔ modulator with input frequency 0.1MHz, input amplitude 1V, 9-level quantization and standard deviation

σ_{cap} = 0.316%, are shown in Fig. 5.11. Simulation results of the standard deviations of capacitance mismatch under different unit DAC number are tabulated in Table 5.2. These harmonic distortions are obtained by averaging ten simulation results in a specific standard deviation and unit DAC number. We observe that when the unit DAC number increases, the harmonic distortions increase. Comparing（5.20）with Table 5.2 and expecting A is a function of the unit DAC number and standard deviation of capacitor mismatch and a is a function of unit DAC number, we conclude the following equations:

$$A = 0.566 \times \sqrt{u} \times \sigma_{cap}$$

$$a = 1.4667 + 0.0625 \cdot u + 0.0021 \cdot u^2 \qquad (5.21)$$

where u is the unit DAC number, σ_{cap} is the standard deviation of capacitor mismatch.

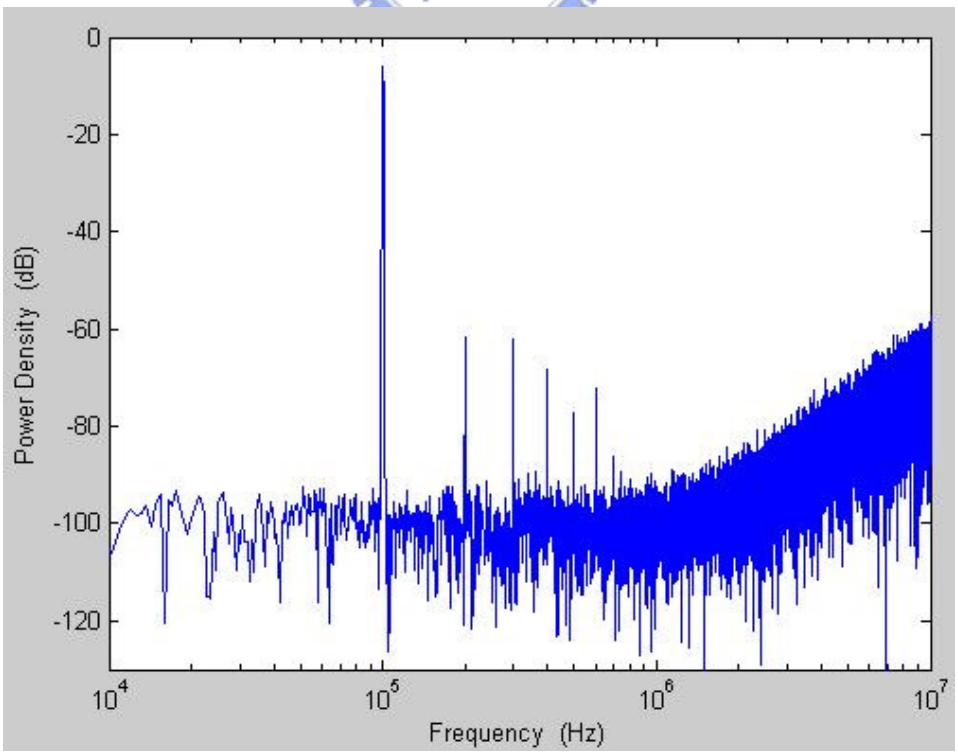


Fig. 5.11 Simulation results of DAC harmonic distortion

Std. deviation (σ_{cap})	**Unit DAC number (*u*)**	**HD2 (dB)**	**HD3 (dB)**	**HD4 (dB)**
0.316%	8	-54.59	-60.315	-67.63
0.316%	10	-53.93	-59.13	-61.69
0.316%	12	-50.3	-58.62	-60.29
0.316%	16	-48.97	-53.82	-61.635
0.1%	8	-65.79	-74.42	-74.48
0.1%	10	-63.39	-70.63	-80.70
0.1%	12	-62.98	-67.26	-73.49
0.1%	16	-59.62	-65.22	-73.44

TABLE 5.2 Simulation results of standard deviation of capacitor mismatch vs. unit DAC number with A_{in}=1

Next, in order to check our model if it is correct in other cases, we calculate our model（5.20）（5.21）and simulate the behavior DAC model to see if they are equal to each other. Theoritical results of harmonic distortion according to our model（5.20）（5.21）are tabulated in Table 5.3 and the corresponding simulation results are tabulated in Table 5.4. From Table 5.3 and Table 5.4, the two results are mostly close and they confirm that our DAC distortion model is reasonably precise.

Std. deviation (σ_{cap})	**Unit DAC number (*u*)**	**HD2 (dB)**	**HD3 (dB)**	**HD4 (dB)**
0.05%	8	-79.945	-94.89	-112.4
0.05%	12	-75.39	-88.69	-104.56
0.05%	16	-71.58	-83.27	-97.51
0.025%	8	-85.97	-100.915	-118.42
0.025%	12	-81.41	-94.71	-110.58
0.025%	16	-77.60	-89.29	-103.53

TABLE 5.3 Theoritical results of standard deviation of capacitor mismatch vs. unit DAC number with A_{in}=0.5

Std. deviation (σ_{cap})	**Unit DAC number** (***u***)	**HD2 (dB)**	**HD3 (dB)**	**HD4 (dB)**
0.05%	8	-77.02	-90.77	-98.80
0.05%	12	-76.34	-86.75	-97.98
0.05%	16	-70.88	-78.53	-77.80
0.025%	8	-89.46	-102.44	-110.64
0.025%	12	-79.88	-89.56	-93.61
0.025%	16	-74.13	-87.48	-91.5

TABLE 5.4 Simulation results corresponding to Table 5.3

From（5.20）（5.21）, we can plot $E[HD]$ vs. standard deviation of capacitance mismatch and DAC output level. It is shown in Fig. 5.12 and Fig. 5.13.

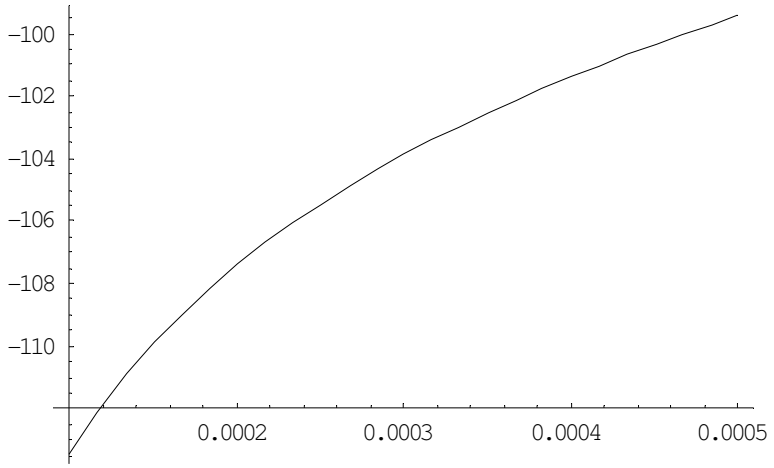


Fig. 5.12 HD2 vs. std. of mismatch with 3 Bit DAC and $A_{in} = 0.2$

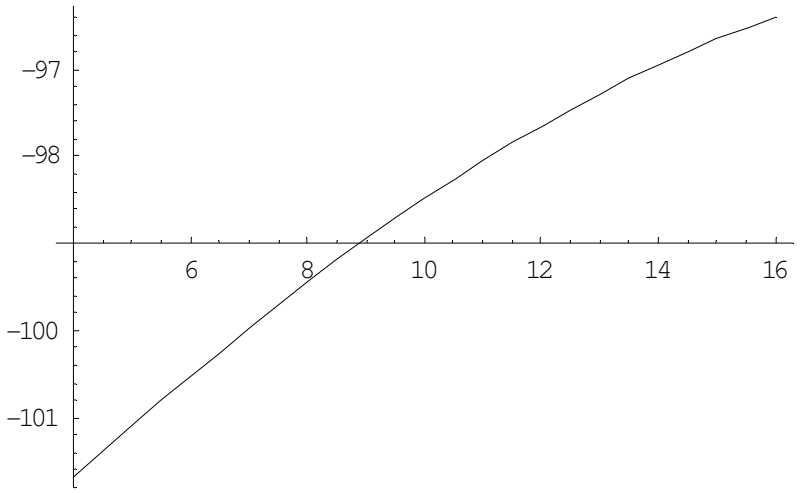


Fig. 5.13 HD2 vs. DAC output level with std. = 0.04% and $A_{in} = 0.2$

From Fig. 5.13, we can see that multi-bit DACs produce significant harmonic distortion when its output level is large.

5.4 Nonlinear Op-amp Gain Distortion [Gee 02][Med 99]

The gain of the operational amplifier depends on its input and output voltages. The dependence on the input voltage can be neglected in a switch-capacitor integrator since the input voltage of the op-amp at the end of a clock phase always settles to the same voltage. However, the output voltage of the op-amp is the integral of the difference between the input and feedback signal of the $\Sigma\Delta$ converter. Therefore, it varies significantly and influences the output conductance of the op-amp. This results in gain variations and distortion of the input signal.

The gain of the op-amp varies with the output voltage. When the output voltage increases, the drain-source voltage v_{DS} of the output transistors decreases so that this results in a reduction of the output impedance and the gain of the op-amp. The nonlinear gain of the op-amp can be modeled by a truncated Taylor expansion as

$$A_V = A_0(1 + \beta_1 v_0 + \beta_2 v_0^2)$$

where v_o is the output voltage of the op-amp. Note that β_2 is a negative value since the gain decreases as the output swing increases. We obtain the following expressions for the amplitude of the second and third harmonics referred to at the modulator output [Med 99],

$$A_2 = \frac{|\beta_1|}{2A_0}A^2 \qquad A_3 = \frac{|\beta_2|}{4A_0}A^3 \tag{5.22}$$

(5.22) shows that the harmonic distortions can be suppressed by increasing the gain of the op-amp. In general, the value of β_1 is about 2.5%/V and β_2 is $10\%/V^2$. Substituting the values of β_1, β_2 and assuming the DC gain A_0 as 60dB, we can estimate the HD2 = -103dB and HD3 = -98 dB. The larger the DC gain A_0, the smaller the harmonic distortions are. The DC gain A_0 60dB can have a negligible harmonic distortion.

5.5 Nonlinear Capacitances Distortion [Gee 02][Med 99]

The dependency of the value of the capacitance on the stored voltage, that is, the presence of nonlinearity, provokes an error in the charge transfer, is a source of distortion at the modulator output. In general, the nonlinear capacitors with a dependency between the capacitance and the stored voltage v can be described by a second-order Taylor series as

$$C(v) = C_0(1 + \alpha v + \beta v^2) \tag{5.23}$$

where C_0 represents the capacitance when the capacitor is uncharged and α, β are the nonlinear coefficients. The values of these coefficients depend on the technique used to implement the capacitor. Typical values for poly-poly capacitors are around 30-50ppm/V for α and 4-7ppm/V^2 for β. In particular, for a capacitor implemented with two polysilicon layers, the first non-linear coefficient dominates clearly [Med 99]. In such a case, we can truncate (5.23) in the linear term, resulting

in:

$$C(v) = C_0(1 + \alpha v)$$

The coefficient α will result in a second order harmonic in the modulator output with amplitude [Med 99]:

$$A_{H,2} = \frac{1}{4}\alpha A_{in}^2 \qquad (5.24)$$

where A_{in} is the input amplitude. Substituting $\alpha = 50\text{ppm/V}$ into (5.24), the second order harmonic distortion is calculated as -103dB. The amplitude of this harmonic is doubled for multi-bit modulators. However, in a differential implementation, this second-order harmonic is removed. Due to mismatches in a practical implementation, some second order harmonic distortion components will still be present, but it will be significantly smaller than for a single-ended implementation [Gee 02].

5.6 Nonlinear Switch Resistance Distortion [Gee 02]

In Chapter 4, the influence of the non-zero resistance of the switches on the settling performance of the $\Sigma\Delta$ converter was discussed. It was assumed that the switches have a constant resistance during the on-phase, independent on the voltages across them. This nonideality introduced a gain and a pole error which degraded the settling performance of the integrators. Note that this model generates no harmonic distortion components.

In reality, the resistance of the MOS switches is nonzero and depends on the voltages across the terminals since switches are generally implemented with nMOS and/or pMOS transistors. Depending on the location of the switch, the variation of the resistance can generate harmonic distortions. The on-resistances of an nMOS and pMOS transistor used as a switch are respectively given by

$$R_{SW,N} = \frac{1}{KP_n \cdot \frac{W}{L} \cdot \left(v_{GS} - V_{Tn} - \frac{v_{DS}}{2} \right)}$$

$$R_{SW,P} = \frac{1}{KP_p \cdot \frac{W}{L} \cdot \left(\frac{v_{DS}}{2} - (v_{GS} - V_{Tp}) \right)} \qquad (5.25)$$

From（5.25）, we can see that the switch resistance is dependent on the source and drain voltages, or, in the case of switch S1, on the input signal, as shown in Fig. 5.14. During the sampling phase, the input signal of the switched-capacitor integrator is sampled through switches S1 and S2 on the sampling capacitance. The resistance of switch S1 depends directly on the input signal and therefore causes harmonic distortion. Switch S2 always has one terminal connected to a fixed voltage. So at the end of the sampling phase, the voltages at the source and drain of that switch are about constant for each clock period. Therefore, the distortion generated by this switch can be neglected compared to the distortion introduced by switch S1.The same applies to switches S3 and S4, which are connected to respectively a fixed reference voltage or the virtual ground of the op-amp at the end of the integration. Furthermore, no time varying input signal is driving the circuit during the integration phase. Instead, a constant charge proportional to the input signal is transferred from the sampling to the integration capacitance. Since this is like applying a dc signal during every clock phase, S3 and S4 generate considerably less distortion.

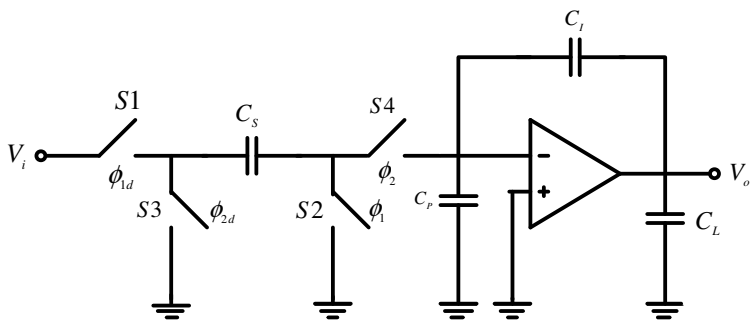


Fig 5.14 Switched-capacitor integrator

There are two ways of reducing the distortion: decreasing the signal amplitude or increasing the switch size. Appropriate design can be obtained to have negligible harmonic distortions. For example, this distortion can be reduced by employing transmission gates with n- and pMOS transistors in parallel.

6

Design Optimization of Sigma-Delta ADCs Design

Power, noise and distortion models derived in Chapter 4, 5 are employed to systematically discuss how each design parameter affects the *SNDR* and power consumption. After identifying critical parameters, we will use them to do design optimization, in order to search for parameter optimal combinations. Before the discussions, we formally define the peak *SNDR* at ΣΔ ADC output as

$$SNDR = \frac{(2A_{in})^2 / 2}{P_Q + P_{AV} + P_{\varepsilon 1} + P_{\varepsilon 2} + P_{dac} + P_{jitter} + P_{sw} + P_{OTA} + P_{ref} + HD_{DAC}} \quad (6.1)$$

6.1 Design Parameters Discussions

Based on models in Chapter 4, 5, the influences of each design parameter to the *SNDR* in（6.1）and *Power* in（4.45）are discussed in the following:

1. ***OSR*** can influence the behavior of all nonidealities and power consumption. Higher OSR is helpful to reduce settling distortion. But, OSR is proportional to the digital power consumption according to（4.42）.
2. ***B*** is an important system parameter. Higher bit number results in smaller quantizer level and relaxes the dynamic requirement of OTA. But, the settling distortion doesn't change with B and higher B will introduce significant DAC distortion. Both the DAC noise power（4.36）and the digital power consumption（4.43）increase exponentially with B.
3. ***n*** is the order of a ΣΔ modulator. Increasing *n* will increase the value of A_{VS}

such that it will increase the settling distortion.

4. ***A*** is the open loop gain of OTA. Finite *A* will cause nonlinear op-amp gain distortion. Simulation shows that a minimum required *A* is about 60 dB.
5. $\boldsymbol{a_1 = C_S / C_I}$ is the gain coefficient of the first integrator, and usually varies from 0.1 to 1.
6. ***R*** is the on-resistance of switches. The on-resistance of switch S1 is dependent on the input signal, so it produces harmonic distortions. Appropriate design can be obtained to have negligible harmonic distortions.
7. ***GBW*** means the effective gain bandwidth of OTA during integration phase. A larger *GBW* can reduce the settling distortion, but increase analog power consumption（4.41）.
8. $\boldsymbol{C_S}$ is the capacitance of sampling capacitor. Its value depends on the stored voltage slightly so it produces little harmonic distortions.
9. ***SR*** is the OTA slew rate and plays an important role in integrator output settling performance. The larger *SR*, the smaller settling noise and distortion is.
10. $\boldsymbol{\sigma_{cap}}$ is the standard deviation of unit capacitor and its value depends on process technology. Recently, double poly and metal-insulator-metal (MIM) capacitor are the two main methods to implement capacitors in analog integrators circuits. These two types of capacitors have high linearity and good matching accuracy, and $\boldsymbol{\sigma_{cap}}$ of them are all below 0.05%. The main influence of $\boldsymbol{\sigma_{cap}}$ on ΣΔ modulators is the multi-bit DAC linearity.

	B ↑	OSR ↑	n ↑	R ↑	GBW ↑	C_S ↑	SR ↑	σ_{cap} ↑
P_Q	↓	↓	↓	—	—	—	—	—
P_{AV}	↓	↓	↓	—	—	—	—	—
$P_{\varepsilon 1}$	↓	↑	—	↑	—	↑	—	—
$P_{\varepsilon 2}$	↓	↑	—	—	↓	↑	↓	—
P_{dac}	↑	↓	—	—	—	—	—	↑
P_{jitter}	—	↓	—	—	—	—	—	—
P_{sw}	—	↓	—	—	—	↓	—	—
P_{OTA}	—	↓	—	—	↑	—	—	—
P_{ref}	—	↓	—	↓	↓	↓	—	—
HD_{SR}	↓	↓	↑	↑	↓	↑	↓	—
HD_{DAC}	↑	—	—	—	—	—	—	↑
$Power$	↑	↑	↑	↓	↑	↑	↑	—

TABLE 6.1 Summary of noise and distortion-power and power-rating when design parameters increase

In Table 6.1, P_Q is the quantization noise. P_{AV} is the leaky quantization noise. P_{ε_1} is the setting error during the sampling phase. P_{ε_2} is the setting error during the integration phase. P_{dac} is the DAC noise. P_{jitter} is the jitter noise. P_{sw} is the switch thermal noise. P_{OTA} is the OTA thermal noise. P_{ref} is the reference circuits thermal noise. HD_{SR} is the settling distortion. HD_{DAC} is the DAC distortion. Table 6.1 summarizes the above discussions. Basically we identify *B*, *OSR*, *n*, *R*, *GBW*, C_S and *SR* as the optimization process design parameters. Table 6.1 shows qualitatively how distortion and power are affected when a particular design parameter increases, and it reveals that the ΣΔ ADC design task is a very complex one.

6.2 Design Optimization

In the following we describe the design optimization approach and it will help designers reach an optimal design quickly. It is based on the noise, distortion and power models described in Chapter 4, 5. The complete flow of the optimization methodology is shown in Fig. 6.1. The input signal bandwidth (Hz) and the output signal *SNDR* (dB) are treated as design specifications. We modify the figure-of-merit (FOM) [Sch 05] function by multiplying a variable *K* to the *SNDR* term of FOM, to become our weighting function.

$$\text{Weighting Function} = K \cdot SNDR_{\text{dB}} + 10\log\left(\frac{f_B}{Power}\right) \qquad (6.2)$$

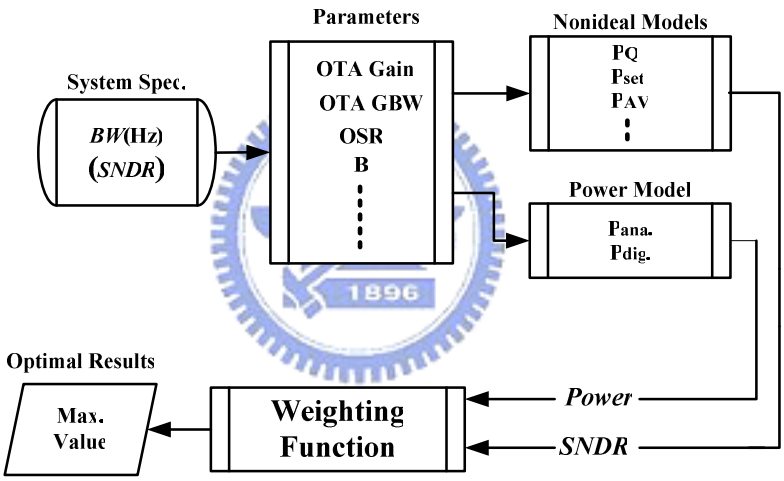


Fig. 6.1 Proposed design optimization for the $\Sigma\Delta$ modulator design

In（6.2）the *SNDR* and the inverse of *Power* are both expressed in log scale. The design optimization approach basically searches through the entire parameter space to find the set of design parameters which maximize the Weighting Function. By maximizing the Weighting Function we can increase *SNDR*（6.1）and reduce *Power*（4.45）at the same time. The constant *K* serves as the relative weighting between *SNDR* and *Power*. A larger *K* would result in a larger *SNDR* and *Power*. Some optimization iterations may be required. Typically, if we prefer high resolution

designs, we set *K* higher and *SNDR* plays a more important role than *Power*; on the other hand, if we prefer low power designs, we can set *K* lower. After an optimization process, the set of design parameters resulting in the largest Weighting Function value is the process outcome and is evaluated. If not acceptable, the *K* is adjusted and the optimization process is repeated. The parameter searching space is specified to be

- OSR : 8 ~ $\dfrac{80\ \text{MHz}}{2 \cdot f_B}$
- B : 1 ~ 6 (if > 3, DEM is required)
- n : 1 ~ 3
- R : 100 Ω ~ 300 Ω
- GBW : 50 MHz ~ 500 MHz
- SR : 50 V/μs ~ 500 V/μs
- C_S : 1 pF ~ 10 pF

The parameters σ_{cap} and V_{ref} depend on the technology, so they are set before the optimization. During the optimization process, the gain coefficients a_i are specified according to the rules provided in [Mar 98b]. The optimization algorithm systematically searches the entire parameter space listed above.

7
Simulation Results

The design optimization described above is implemented by Mathematica®. In order to demonstrate the accuracy and practicability of our models, we apply it to a published design case, which is a $\Sigma\Delta$ modulator in 0.18-um CMOS technology for ADSL-CO application [Gag 03]. Its peak *SNDR* can reach 78dB over 276kHz signal bandwidth.

To compare with the design of [Gag 03], the optimization algorithm uses the same specifications as those in [Gag 03]. They are:

- Peak *SNDR* : 78 dB
- Signal bandwidth : 276 kHz

The OTA gain A is set at 60 dB and the V_{ref} is set at 0.9 V for a 1.8 V power supply in 0.18-μm CMOS technology. The matching of capacitor σ_{cap} is set at 0.04% for the MIM capacitance. The parameter variable ranges are also specified as follows. For the signal bandwidth of 276 kHz, the range of *OSR* is set between 8 ~ 128, and the quantizer bit *B* is between 1 ~ 5. The order n is between 1 ~ 3, since using a n higher than 3 may cause instability. The *R* range is between 100 Ω ~ 300Ω. C_S is between 1 pF and 10 pF. The minimum size of C_S is usually determined by process technology. Finally, *GBW* and *SR* are between 50 MHz ~ 500 MHz and 50 V/μs ~ 500 V/μs respectively. The results published in [Gag 03] and those obtained from our optimization methodology are all listed in Table 7.1, which includes three optimization results corresponding to *K*=0.4, *K*=0.45, and *K*=0.5.

circuit parameters	in [Gag 03]	K =0.4	K =0.45	K =0.5	Unit
OSR	96	40	50	60	-
B	3	2	2	3.17(9level)	-
n	2	2	2	2	-
R	300	300	300	300	Ω
C_S	1.7	1	1	2	pF
GBW	400	70	90	140	MHz
SR	500	120	160	80	V/μs
A_{in}	0.5	0.9	0.9	0.9	V
SNR	82.8	81.5	83.3	96.1	dB
SNDR	76.0	79.0	79.9	96.1	dB
Power	15	3.0	3.7	15.7	mW

TABLE 7.1 Comparisons of our design results and those in [Gag 03] with different *K*

From Table 7.1, we find that when *K* = 0.4, the *SNDR* is 79.0 dB, which just a little higher than the specification. To increase *SNDR*, we need to increase *K*. When *K*=0.45, the result of *SNDR* = 79.9 satisfies the specification, although the *Power* = 3.7 mW is higher than *Power* = 3.0 mW when *K*=0.4. The results from higher *K* are also reported. When *K*=0.5, parameters achieving high *SNDR* are preferred, resulting in level being 9. Since *B* is larger than 3, the DEM algorithm is used. The power consumption is dramatically larger at 15.7 mW, due to the fact that the DEM is employed and *B* is larger. We choose the case *K*=0.45 (with *SNDR*= 79.9) as our design.

The design of [Gag 03] is also listed in Table 7.1. The *SNDR* and *Power* of [Gag 03] listed in Table 7.1 are computed from our models. The *SR* = 500V/μs and *GBW* = 400MHz used in [Gag 03] are considerably larger than those of our design. According to Table 5.1 in the Chapter 5, the values *SR* = 500 V/μs and *GBW* = 400MHz are barely enough for *OSR* = 8, but are more adequate for *OSR* = 16. Since the *OSR* in [Gag 03] is designed to be 96, the *SR* and *GBW* values used in [Gag 03] are too large compared with the minimum required values at *SR*=90V/μs and *GBW*=40MHz listed

in Table 5.1, resulting in power consumption four times of our design (15mW vs. 3.7mW). In contrast, the *SR* and *GBW* values in our design are adequate, with (*SR*, *GBW*) = (160, 90) compared with the minimum required (110, 60) listed in Table 5.1.

Table 7.2 shows the corresponding noise and distortion powers for the four design cases shown in Table 7.1. In the design of [Gag 03], and in our designs for K=0.4, 0.45, the dominating power is P_{dac} and P_{HD}. Our optimization process may help to distribute noise power more evenly among different noise and distortion categories, resulting in a larger gap between P_{dac}, P_{HD} and P_{total}, where P_{total} is the sum of in band noise and distortion powers. The gap between P_{dac}, P_{HD} and P_{total} from [Gag 03] is very small. Our optimization algorithm may also help designers consider less aggressive design parameters first, e. g., settling B = 2 instead of 3. When K=0.5, the optimization algorithm sets B to be 3.17 (level=9), so the DEM technique is employed, and DAC noise is suppressed to -108.5 dB. According the P_{sw} at -95.6 dB becomes the dominating noise power.

Noise	in [Gag 03]	K =0.4	K =0.45	K =0.5
P_Q	- 109.8 dB	- 84.9 dB	- 89.8 dB	-100.8 dB
P_{AV}	-141.1dB	- 123.6 dB	- 126.5 dB	- 135.9 dB
$P_{\varepsilon 1}$	- 196.5 dB	- 681.7 dB	- 551.5 dB	- 253.4 dB
$P_{\varepsilon 2}$	- 119.3dB	- 103.9dB	- 104.5dB	- 111.8 dB
P_{sw}	- 96.9 dB	- 90.8 dB	- 91.8 dB	- 95.6dB
P_{ref}	- 114.7dB	- 101.0dB	- 103.1 dB	- 108.8 dB
P_{OTA}	- 117.0 dB	- 110.9 dB	- 111.9 dB	- 115.7 dB
P_{dac}	- 80.8dB	-81.4dB	- 82.3dB	- 108.5dB
P_{HD}	-79.5	-81.2	-81.2	-
P_{total}	- 77.1dB	- 76.9 dB	-77.8dB	-94.0dB

TABLE 7.2 the corresponding noise and distortion powers for the design parameters listed in Table 7.1

Table 7.3 lists the power consumption details. From (4.41), we can see that the POW_{analog} is proportional to the *GBW* and C_{L2}. The C_{L2} (4.19)is proportional to the sampling capacitance C_S. From Table 7.1, we can see that the *GBW* of [Gag 03] is larger than that of *K*=0.4, *K*=0.45 and *K*=0.5 and C_S of [Gag 03] is larger than that of *K* = 0.4 and *K* = 0.45 (almost the same with *K* = 0.5). Hence, the POW_{analog} of [Gag 03] is the largest among the four cases. From (4.43), we can see that the $POW_{digital}$ is proportional to the 2^B and *OSR*. It is also inversely proportional to the on-resistance *R*. The quantizer power $POW_{quantizer}$ (4.44) is related to *OSR* and *B*. The larger the *OSR* and *B* are, the larger the quantizer power $POW_{quantizer}$. In Table 7.3 the *Power* of [Gag 03] is four times larger compared with that of *K*=0.45. This is due to the design of [Gag 03] employs larger *GBW*, *OSR*, C_S, and *B*, resulting in large POW_{analog}, $POW_{digital}$ and $POW_{quantizer}$.

	Ref [5]	***K*=0.4**	***K*=0.45**	***K*=0.5**	**Unit**
POW_{analog}	64.6	6.65	8.55	26.6	-
$POW_{digital}$	3.1×10^{10}	6.4×10^{9}	8.02×10^{9}	2.16×10^{10}	-
$POW_{quantizer}$	1.29	0.38	0.48	0.86	mW

TABLE 7.3 Listing the details of power consumption.

8
Conclusions and Future Works

The main contributions of this work are described in the following. First, we analyses the settling distortion of the OTA and provide insight on how settling distortions are related to *SR* and *GBW*. Our analyses can explain why the *SR* and *GBW* in [Gag 03] are too large, but the *SR* and *GBW* obtained in our design are adequate. We also derive the DAC distortion model. Additionally, we make modifications to settling error model and consider the effect of the switch on-resistance in the integration phase. The noise models and distortion models are established in Chapter 4 and Chapter 5 respectively. Based on these noise and distortion models, the *SNDR* is defined in （6.1）, and we utilize it and power model to do design optimization. We use *SNDR* instead of SNR as our specification because *SNDR* is a combination of the SNR and the THD specifications and it is an overall measure of ADC dynamic performance.

In the future works, the DAC distortion with DEM and other distortion issues are needed to be analyzed to get a more accurate *SNDR* estimation such that the overall design optimization will be more realistic.

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