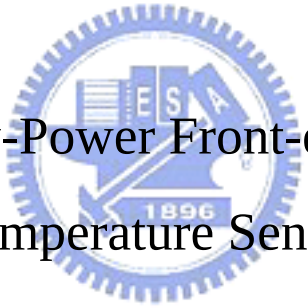
國 立 交 通 大 學

電 機 與 控 制 工 程 研 究 所

碩 士 論 文

超低功率溫度感測器前端電路



An Ultra Low-Power Front-end Circuit for Temperature Sensor

研 究 生：吳宗諭

指導教授：蘇朝琴　教授

中 華 民 國 九十五 年 十 月

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in

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中 華 民 國 九十五 年 十 月

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摘要

近年來，感測器在 IC 市場上有所進步。在一般的積體電路製程中結合感測器為顯著的趨勢。因此，結合電路與感測器不僅僅能降低電路的複雜度更能因此降低成本上的支出。另外，低功率低電壓更是未來的另一個趨勢。如何節省功率的消耗將是一大問題。

在此論文中，提出一個應用於低功率與低電壓的溫度感測器前端電路。為了達到低功率與低電壓，操做在弱反轉區的放大器將會被介紹。在這前端電路中，由於溫度感測器的訊號相當小，截波放大器(chopper amplifier)將在論文中被使用。除此之外，非連續性的低通濾波器也會被介紹。為了降低製程偏移的影響，使用一些電路技巧，用以消除運算放大器的偏移電壓。由於電路中使用到時脈開關，雜訊應此將會產生。因此在論文中藉由多餘的開關(dummy switches)製造反相的雜訊以消除單一開關所產生之雜訊。

在論文中，溫度感測器前端電路在 TSMC CMOS 0.18μM 的製程被實現。此前端電路包括截波放大器、濾波器、後端放大器。其晶片面積為 0.78μm x 0.78μm(不包含 PAD)。取樣頻率在 6.4k，整體功率為 5.6μW，訊號頻率為 50Hz。

索引詞彙—截波放大器、電容切換式低通率、低電壓、低功率、反相器、偏移電壓消除。

An Ultra Low-Power Front-end Circuit for Temperature Sensor

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Abstract

Sensors advanced greatly in the field of semiconductor in recent years. A notable trend is to realize a sensor in a standard CMOS processing. A combination of micro-sensor and circuits decrease the complexity of package and make cost down. On the other hand, low-voltage low-power techniques are necessary to increase the battery life time in the future. How to decrease the power consumption is a serious problem in our design.

In this thesis, a low-power low-voltage front-end circuit of the thermopile is implemented. The amplifier working in weak inversion is introduced in order to reduce the power consumption. Because the output signal of the thermopile is very small, a chopper amplifier is needed in the front-end circuits to improve the SNR. Also, a switch-capacitor lowpass filter will be implemented following the chopper amplifier. To reduce the effects of process variation of amplifiers, a offset-cancellation technique is introduced. Dummy switches are used to reduce the clock feedthrough noise in our design.

In this thesis, the front-end circuit is realized with TSMC CMOS 0.18 μm. It includes chopper amplifier, filter, and post amplifier. The core area is 0.78 μm x 0.78 μm. The clock is 6.4k Hz, the power is 5.6 μW, the signal bandwidth is 50 Hz.

Index Terms – chopper amplifier, switched-capacitor circuits, low-voltage, low-power, offset cancellation

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在此要感謝我的父母，讓我無後顧之憂的完成學業。還有感謝父母在我最失意最灰暗的時候，給我鼓勵讓我能夠安下心繼續努力。不管是在學業上或是其它方面更能專注的學習。

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吳宗諭

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Chapter 1

Introduction

1.1 Motivation

In recent years, IC processing technologies have a great improvement. It not only increases the performance but also scales down the price. In the intelligent sensor, how to scale down the price is important. Therefore, the sensor using standard (CMOS) technology is cheaper than previous system solution. Another advantage in sensor using standard technology is that it can combine with the circuit. The circuit for signal processing, A/D conversion, on-chip calibration can increase the performance in the smart sensor. Therefore, integrating the micro-sensor and circuit is a trend to scale down the price and increase the performance.

The temperature sensor is an important device in smart sensor market. The applications of sensors have many aspects, like ear thermometer and home climate control. Ear thermometers, the temperature measurement are widely used in hospital, Fast and accuracy are the important point. The home climate control is similar to the ear thermometer. It is important to check the temperature in the room then to enhance the comfort level of the room. The thermopile is one of the temperature sensors. The

thermopile can transfer temperature to the heat then transfer the heat to the voltage.

Because the voltage from the thermopile is too small, the thermopile sensor is limited by the offset and noise of the input of the amplifier. Therefore, to remove noise and offset voltage is a main subject. The solutions that can remove offset voltage and low frequency noise are invented. Examples of these are the autozero and chopper technology. The principle of the autozero technique is that the offset cancellation is done in two phase [1]. The principle of the chopper technique is to move the offset voltage to a high frequency and modulate back to the base-band. The offset is only modulated once, so the higher frequency needs to be canceled. Therefore the low frequency noise can be cancelled and the input signal is maintained. The signal noise ratio (SNR) is improved.

In this thesis, the low-voltage, low-power front-end circuit of the thermopile is present. Using the amplifier which works in weak inversion enables the front-end circuits to achieve tens of micro voltage. How to cancel the offset and low frequency noise is included in it.

1.2 Basic Concepts of Thermopile

In recent years, the thermopile techniques are developed and commercialized [26]. The well-known product is the infrared temperature sensor which use in the ear thermometer. Aside from the ear thermometer and pyrometer, the new application that includes the automated climate control and other housed held such as microwave ovens and hair dryers are invented.

In this thesis, the thermopile sensor is introduced. The thermopile is a popular device using the concept of the see-back effect. The principle of the see-back effect is shown in Figure1.1.The mate. A, B, and C have different thermoelectric factor α_A , α_B ,and α_c . The junctions of the metal A and B are at higher temperature T_h (hot point) and the metal C is at lower temperature T_C (cool point). Therefore, the differential voltage is produced. The voltage across A and B is proportional to temperature difference and the metal A and B.

$$V_{AB} = \left(\alpha_A - \alpha_B\right)\left(T_h - T_C\right) \tag{1-1}$$

At thermoelectric sensor consists of several thermocouples connects in series that form a thermopile. In recent years, the thermopile sensors use the silicon and metal as

the thermoelectric material.

According to differential metals, the voltage can be produced. The equation in semiconductor is:

$$\Delta V = \Delta T \cdot \alpha_a \tag{1-2}$$

where the α_a is the see-back coefficient for material and ΔT is the temperature difference between the end of the conductor. According to the principle, the temperature sensor can be design.

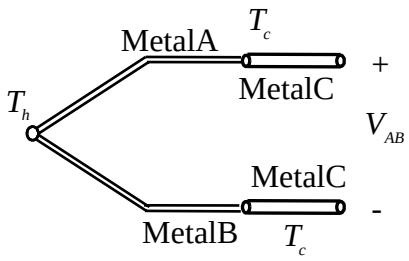

Figure 1.1 The see-back effect

1.3 Thesis Organization

This thesis is organized into five chapters. In Chapter 1, this thesis and the thermopile are briefly introduced. In Chapter 2, the basic concepts of chopper, the MOS working in the weak inversion, and the noise autozero technique are introduced.

In Chapter 3, the noises of the amplifier, and design amplifier, filter architecture and clock generator are outlined. In Chapter 4, the total architecture of the thermopile is presented. The pre-amp, filter and the post-amp are include it. In Chapter 5, the front-end circuits are mentioned and compared.

Chapter 2

Noise and Dynamic Offset Cancellation Technology Analysis

2.1 Introduction

Some of the fundamental issues in the design of amplifier will be reviewed in this chapter. Input signal is influenced by the noise produced by the amplifier. The discussion of the noise source is presented in the Section 2.1. Next, in Section 2.2 to 2.4, the dynamic offset cancellation technologies is introduced. Section 2.2 present the technology named Autozero (AZ) [1]. In Section 2.3 and 2.4, there are two basic techniques that are used to reduce the offset and low frequency of amplifier. Section The Correlation Double Sampling (CDS) is introduced in Section 2.3. Chopper Stabilization (CHS) is introduced in Section 2.4.

2.2 Type of Noise

There are two basic noise sources from the analog circuits. The noises are produced by the electronic device. First, the major source of noise in the resistor is thermal noise. It appears as white noise and can be model as an independent voltage

source. Second, another noise source is flicker noise (1/f noise) [23]. Unlike thermal noise, it just only appears in the low frequency.

2.2.1 Thermal Noise

The thermal noise is the random motion of the electrons in a conductor. Therefore, there is some fluctuation in the voltage measurement even if there is not any voltage source.

The thermal noise in the spectrum is white. It distribute uniformly in the frequency spectrum. Like the thermal noise of a resistor R, it is module as voltage source, shown in Figure 2.1

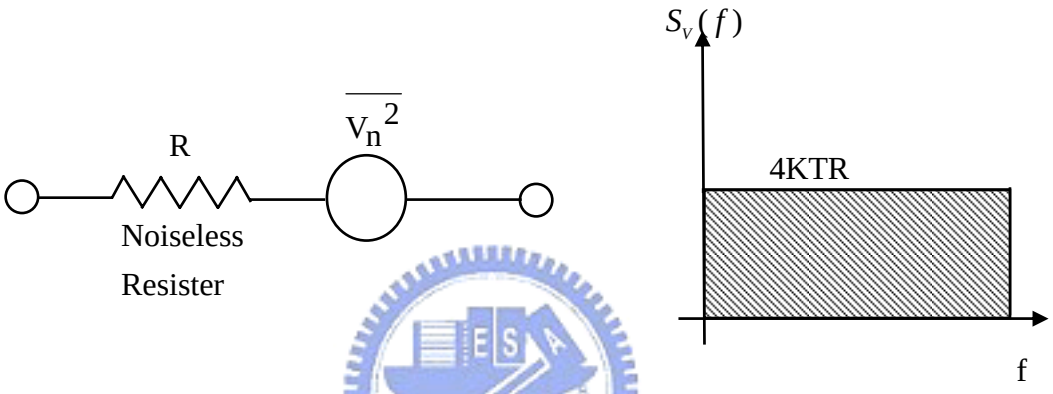

Figure 2.1 (a) Thermal noise in resistor , (b) Power spectrum density

The thermal noise of a resistors R with the one-side spectral density is

$$S_V(f) = 4KTR, \quad f \geq 0 . \tag{2-1}$$

Where k=1.38×10^{-23} J/k is the Boltzmann constant, T is the absolute temperature, and the R is the resistance of the resistor.

In MOSFET, MOS also exhibits the thermal noise. Normally, the thermal noise of the MOS is model by a current source. Its spectral density is:

$$\overline{In^2} = 4KTg_m\gamma . \tag{2-2}$$

Like Fig 2.2. The coefficient γ is derived as 2/3, therefore the spectral density can be written as $\overline{I_n}^2 = 4KT\frac{2}{3}g_m$.

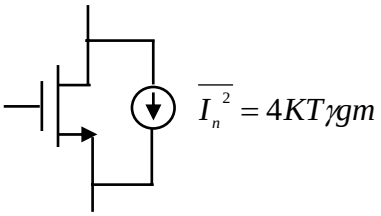

Figure 2.2 The thermal noise in MOSFET

2.2.2 Flicker Noise

Some noises appear in the low frequency is called flicker noise [23]. The reason of the flicker noise is that when silicon crystal reaches the interface, many dandling bonds appear. It takes extra energy and later releases energy. This phenomenon introduces the flicker noise as shown in Figure 2.3. Simultaneously, the flicker noise is also called 1/f noise.

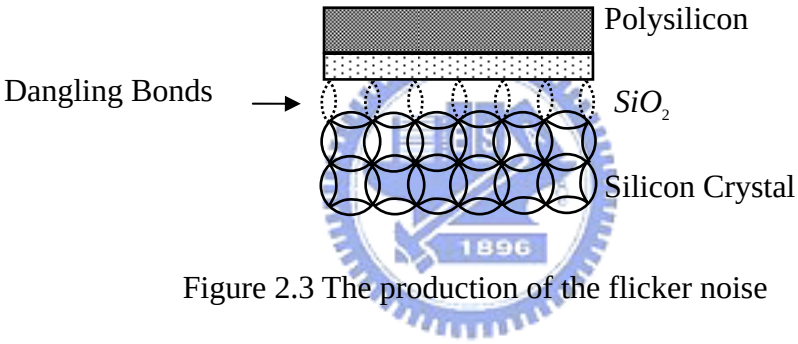

Figure 2.3 The production of the flicker noise

Unlike thermal noise, the flicker noise is not white. The energy of the flicker noise is concentrated at the low frequency. Its spectral density is:

$$\overline{V_n^2} = \frac{K_f}{C_{ox}WL} \cdot \frac{1}{f} \tag{2-3}$$

where K_f is the fabrication parameter, C_{ox} is the gate capacitor per unit area, and W and L are the size of the MOS. The spectral density of the flicker noise is shown in Figure 2.4 and the thermal noise is included [2]. The magnitude of the flicker noise is inversely proportional to the frequency.

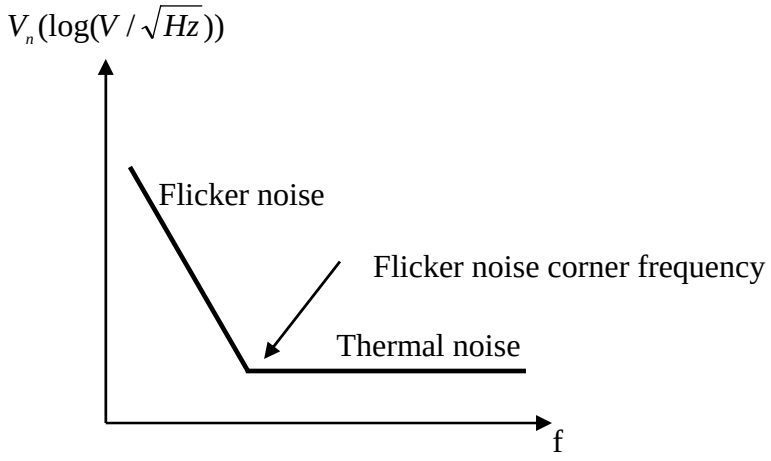

Figure 2.4 Noise spectrum of noise

In Fig 2.4 the intersection between flicker noise and thermal noise is called flicker noise frequency.

2.3 Autozero Technigue

The autozero technique (AZ) [2] is a method of offset voltage cancellations. It can improve the SNR of the system. The correlated double sampling is similar to autozero technique. Next, in Section 2.3.1, the AZ is presented. Then, in Section 2.3.2 the correlated double sampling is outlined latter.

An autozeroing amplifier is shown in Figure 2.5. The principle of autozero technique is to cancel offset voltage in two phases. In first phase ϕ_1, input voltage is set zero, then let offset voltage be sampled on C_{az}. In second phase ϕ_2, when input signal enter to the amplifier, the offset sampling on C_{az} is subtracted than amplified. Through this way, the offset voltage can be cancelled. In the meantime, the low frequency noise is also cancelled. Because, when noise is in low frequency, the characteristic of it belong to DC. So low frequency noise can be regard as DC offset.

In order to remove low frequency and offset voltage, sampling frequency (f_s) must higher than 1/f noise corner frequency. So the noise lower than f_s can be stored on the C_{az}, it will be cancelled in the next phase. However, the noise comes form switched is also sampled on the C_{az}. Therefore, the noise lower than f_s folded back to increase the noise level. Therefore, the noise level must be higher than thermal noise as shown in figure 2.6.

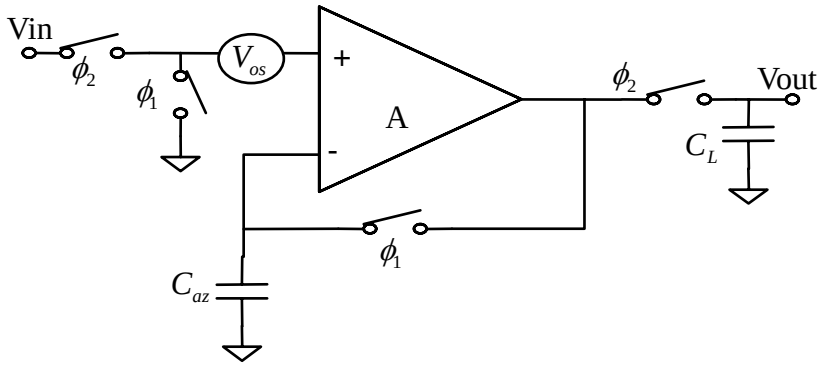

Figure 2.5 Principle of autozero technique

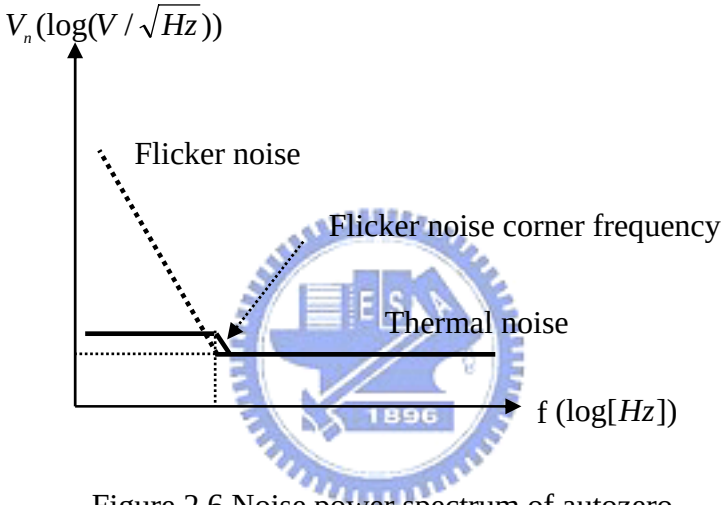

Figure 2.6 Noise power spectrum of autozero

2.3.2 Correlation Double Sampling

The correlation double sampling technique (CDS) [1] is regarded as a special case of the AZ (autozero). As its name indicates, the offset voltage and low frequency noise are sampled at each phase.

In AZ, there are two phases to remove offset voltage. The first one is used to sample the low frequency noise and offset voltage, the second one is used to cancel the offset voltage and amplify the input signal. Therefore, the AZ phase may require one additional phase. The characterization of the CDS like AZ is suitable for SC (switched capacitor) circuit.

Figure 2.7 shows the architecture of the integrator with double sampling. When

ϕ_2 is on, the offset voltage and low frequency noise are sampling in the capacitor. When ϕ_1 is on, the offset voltage can be cancelled. Therefore, only the signal is transferred to the capacitor C_2. We assume the input signal is zero for analysis.

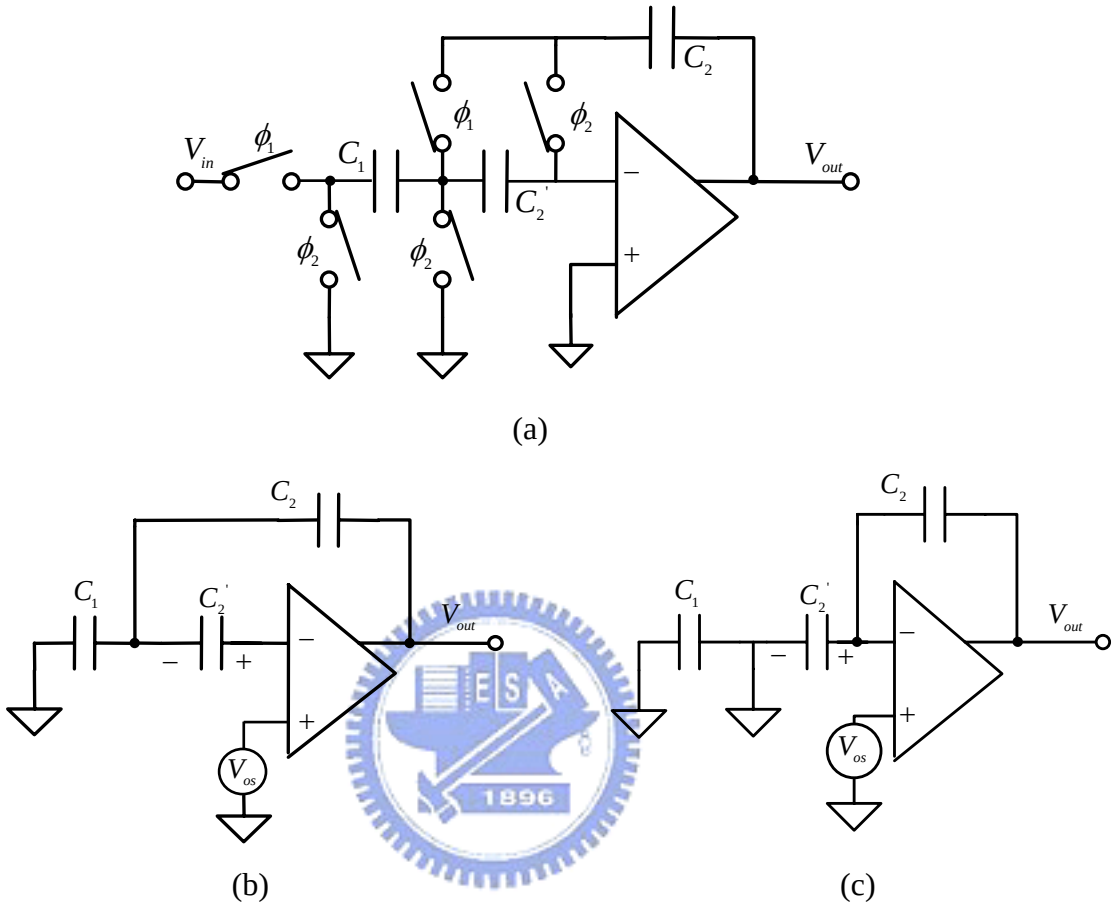

Figure 2.7 The integrator with CDS (a) architecture, (b) during ϕ_1, (c) during ϕ_2

2.4 The Chopper Stabilization Technique

The chopper stabilization technique (CHS) [2] [7] [17] is different from the AZ and CDS. Unlike AZ and CDS, the chopper stabilization technique does not use sampled data to cancel offset voltage. In next section, the principle and the circuit of the chopper stabilization technique are introduced.

2.4.1 Basic Principle

The principle of the chopper stabilization technique is that the input signal is modulated to the higher frequency, amplified and modulated back to the original frequency [17][13]. At the same time, the low frequency noise is modulated to the higher frequency, but only once. Therefore, the filter is followed by the chopper

amplifier, in order to cancel the noise in the higher frequency. This technique is different from AZ (autozero). In AZ, the noise is sampled on clock phase. In CHS, the noise is modulated to the higher frequency then try to cancel it. The principle of the chopper is shown in Figure 2.8.

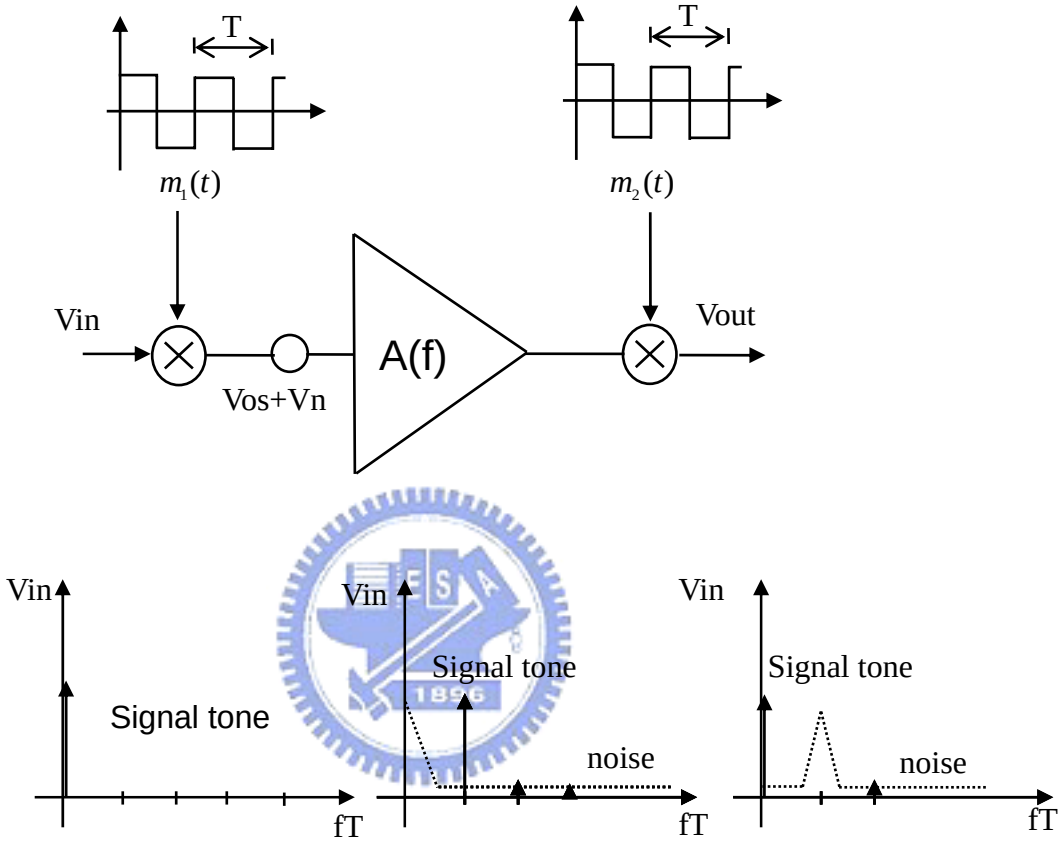

Figure 2.8 The principle of the chopper technique

The input signal is multiplied by the square-wave carrier signal $m_1(t)$. After the modulation, the signal is transposed to the higher frequency. Then the signal in the higher frequency is amplified, at the same time the offset and noise is produced. After amplifying the signal, the signal tone must be modulated to the original spectrum. The noise is modulated to the higher spectrum by $m_2(t)$. Therefore, the low frequency noise can be cancelled since the noise is modulated again.

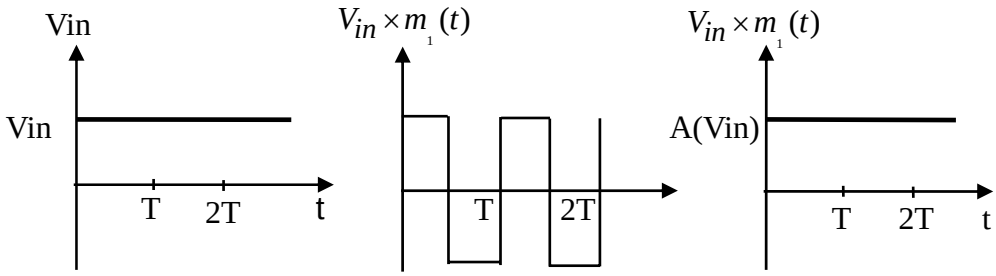

Figure 2.9 The principle of chopper in time domain

In the time domain, the input signal is inverted by the first modulation signal as shown in Figure 2.9. After the second modulation clock, the signal is transferred to the original state. In this case, the amplifier gain is infinite, the bandwidth is infinite, and it does not introduce any delay.

The amplifier has a constant gain A as shown in Figure 2.10. There are some differences in block function. The function of the V_{out} is not the same with square wave, it become a sine-wave. The amplitude of the sine-wave is $(4/\pi)(A \cdot V_{in})$.

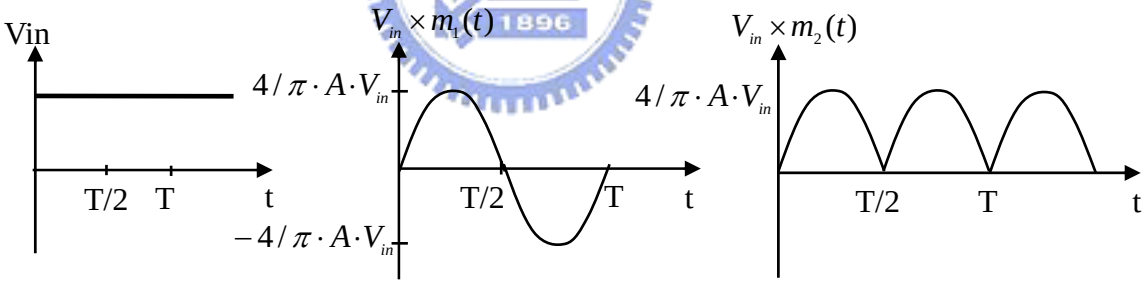

Figure 2.10 The principle in the time domain

The modulation technique of CHS is made up of $m_1(t)$. The $m_1(t)$ is modulation signal. The period of the modulation signal is T ($1/f_{chopper}$) and its magnitude is ± 1 as shown in Figure 2.11. The purpose of the modulation signal is to transpose to other bandwidth [30].

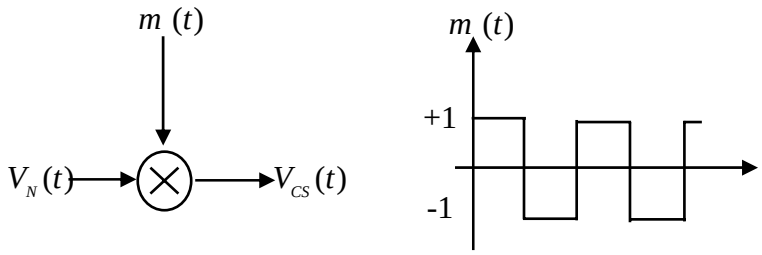

Figure 2.11 Chopper modulation

The Fourier series of the chopper modulation is:

$$f(x) = a_0 + \sum_{n=1}^{n=\infty} \left\{ \; a_n \cos\frac{2n\pi}{T} + b_n \sin\frac{2n\pi}{T} \; \right\} \tag{2-4}$$

$$f(x) = \begin{cases} +1, & 0 < x < \dfrac{T}{2} \\ -1, & \dfrac{T}{2} < x < T \end{cases} \tag{2-5}$$

The coefficient of $a_0,\ a_n,\ b_n$:

$$a_0 = \frac{1}{T}\int_0^T f(x) = 0 \tag{2-6}$$

$$a_n = \frac{1}{T/2}\int_0^T f(x)\cdot\cos\frac{2n\pi}{T}xdx = 0 \tag{2-7}$$

$$b_n = \frac{1}{T/2}\int_0^T f(x)\cdot\sin\frac{2n\pi}{T}xdx = \frac{4}{\pi}\cdot\frac{1}{n} \tag{2-8}$$

Therefore, $f(x)$ is presented:

$$f(x) = \frac{4}{\pi}\sum_{n=1,3,5,\ldots}^{n=\infty}\frac{1}{n}\sin n\omega t = \frac{4}{\pi}\left\{\sin\omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t + .. \; \right\} \tag{2-9}$$

In Equation (2-9), the original signal is modulated to the odd harmonic frequency ($f_{chopper}$).The noise is modulated to the odd harmonic frequency, the noise is filter out. The PSD(Power Spectral Density) of the chopped output signal $V_{cs}(t)$ is obtained by

$$S_{cs}(f) = (\frac{2}{\pi})^2 \sum_{n=-\infty\ \mathrm{n=odd}}^{n=\infty}\frac{1}{n^2}S_N\left(f - \frac{n}{T}\right). \tag{2-10}$$

the low frequency noise and offset voltage are shifted to the odd harmonic.

2.4.2 The architecture of the chopper amplifier

In general, there are a gain amplifier, a low pass filter, and a modulation circuit in

the architecture of the chopper amplifier as show in Figure 2.12. The modulation circuit is made up of the switches as shown in Figure 2.13. The modulation signal is the square wave. Therefore, if the signal passes the switch, the signal is modulated.

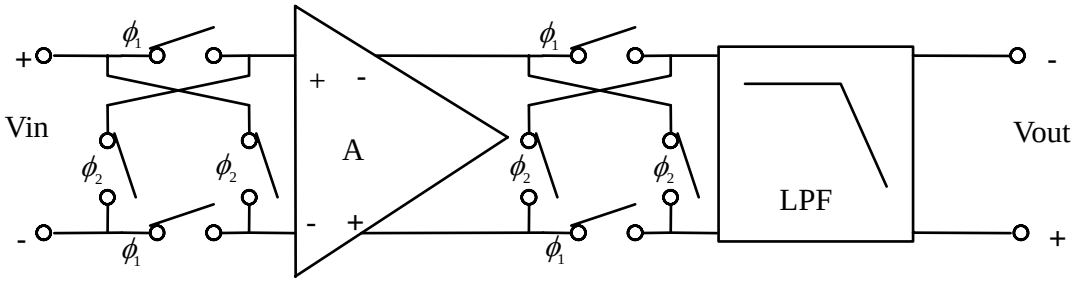

Figure 2.12 The architecture of the chopper

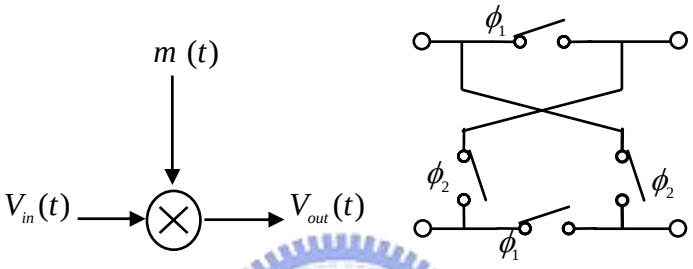

Figure 2.13 The circuit of the modulation signal

If the chopper frequency is higher than the flicker corner frequency, the noise is filtered out through the low pass filter. At the same time, the signal of the baseband is extracted. In the frequency domain, the major noise is the thermal noise as shown in Fig 2.14.

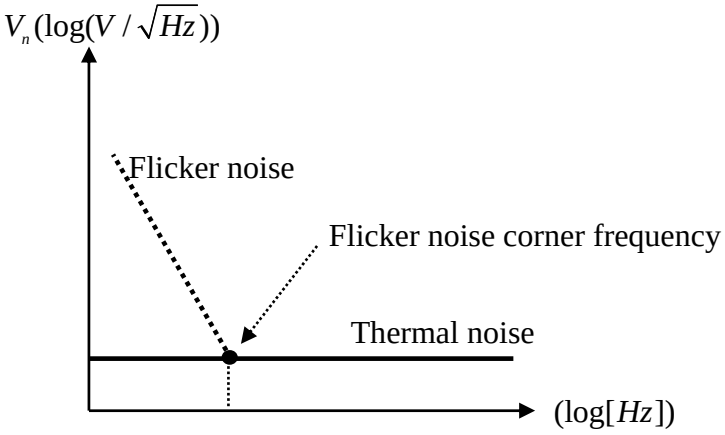

Figure 2.14 The spectrum after filter

2.4.3 Non-ideal effect in circuit

The modulation circuit chopper amplifier is most often realized using MOS switches. Therefore, no-ideal effect is introduced by the switches. In general, there are

two major non-ideal items: clock feedthrough [1], and channel charge injection [1].

When the clock signal is turned off rapidly, the MOS switch couples the noise to the sampling capacitor through its gate-source or gate-drain, as shown in Figure 2.15 [23]. The clock feedthrouth is produced:

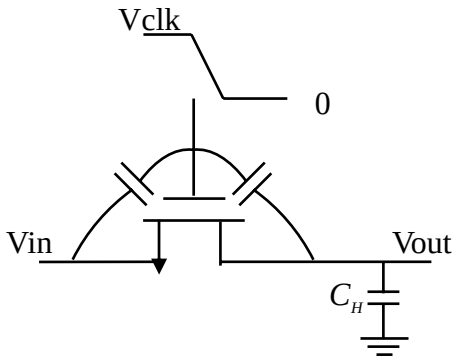

Figure 2.15 Clock feedthrough

where C_H is the sampling capacitor, V_{clk} is the clock signal. The error ΔV is :

$$\Delta V = V_{ck} \frac{C_{ov}W}{C_{ov}W + C_H} \tag{2-11}$$

C_{ov} stands for the overlap capacitance per unit width, V_{ck} is the magnitude of the clock.

Channel charge injection shows in Figure 2.16. When the switch is on, the charge Q_c (2-9) stores in the channel of the switches. When the switch turns off, the charge (Q_c) flows to the terminal point (drain or source). If the charge flows to the drain point with sampling capacitance, the error voltage (ΔV) will appear. In this case, it has an assumption that the quantity of the charge that flow to the drain is only half.

The charge in switch is:

$$Q_c = WlC_{ox}(V_{dd} - V_{in} - V_{th}) \tag{2-12}$$

$$\Delta V = \frac{WlC_{ox}(V_{dd} - V_{in} - V_{th})}{2C_H} \tag{2-13}$$

Therefore the error voltage ΔV is the residual voltage. In the chopper amplifier, this phenomenon causes other offset voltage as shown in Figure 2.17.

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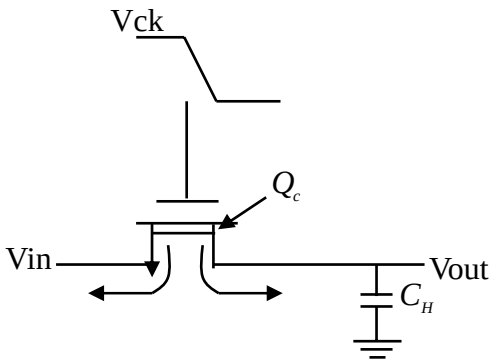


Figure 2.16 Channel charge injection

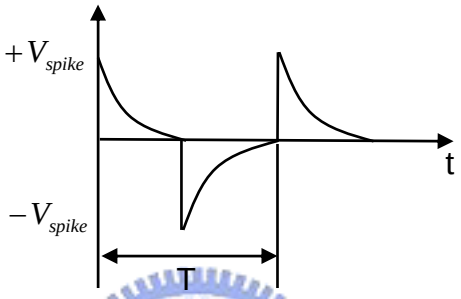


Figure 2.17 Spike signal of the switch

2.4.4 Practical Implementation Issue

In practice, the dummy switch is used to cancel dynamic offset as shown in Figure 2.16. The signal of the switch is accomplished by the clock ϕ_1, and its counter-phase $\overline{\phi_1}$. When ϕ_1 of the major switch (S_m) is turned off, the channel charge splits equally to the drain and source terminals. Therefore, the dummy switches with shorted drain and source place in the drain and source. The size of the dummy switch is half of the major switch. The channel charge splits equally to the source and drain.

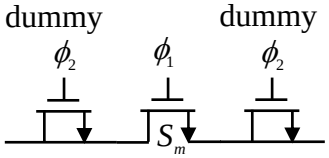


Figure 2.18 The dummy switch

The modulation signal used in differential chopper amplifier is shown in Figure 2.18[3]

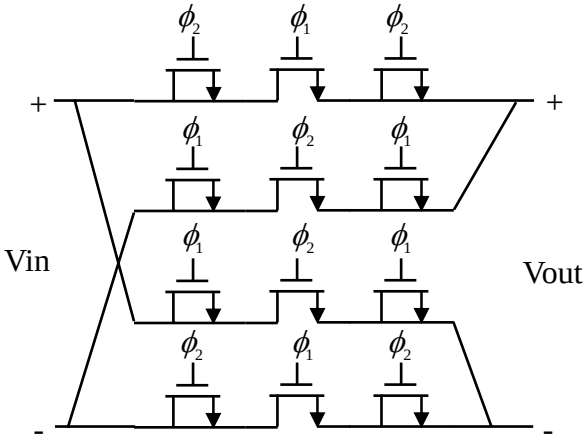


Figure 2.19 The NMOS chopper realization

2.5 Summary

In this section, the dynamic offset cancellation is presented. It includes the autozero, correlated double sampling, and chopper stabilization technique. In contrast to the autozero amplifier, the noise of the chopper amplifier is less than the noise of the autozero amplifier. There are other noises which caused by sampling clock in the autozero amplifier. Therefore, the signal in the order of only few μV is suitable for the chopper amplifier to resist the low frequency and offset voltage.

Chapter 3

Design Considerations for Low-Voltage Low-Power Chopper Amplifier

3.1 Introduction

Design considerations for low-voltage and low-power chopper amplifier will be discussed in this chapter. First, the MOS transistor working in weak inversion is presented in Section 3.2. The circuits working in weak inversion is designed under the low-power and low-voltage environment. In Section 3.3, the architecture of the filter is introduced. At the end, the clock generator is outlined.

3.2 Weak Inversion in the MOS Transistor

In the region of weak inversion [19] [24], the gate-source voltage is less than the threshold voltage V_t. Although the gate-source voltage is small, the voltage is still high enough to create depletion region. In the weak inversion, the channel charge is less than the charge in the depletion region. Therefore, the diffusion current is the

major part of the total current.The drift current is negligible. In contrast to strong inversion, the channel current is the major part of the total current.

Equation (3-1) is the drain current of a MOS in weak inversion [20]:

$$I_D = I_{D0} e^{\frac{V_{GS}-V_t}{nU_T}} \left[1 - \exp(-\frac{V_{DS}}{U_T}) \right] \tag{3-1}$$

Where $U_T = \frac{KT}{q}$ is thermal voltage. K is Boltzmann constant ($1.38\times10^{-23} J/^{\circ}K$). T is the temperature in degrees Kelvin. q is charge of an electron (1.6×10^{-19} C). n is the slope factor of the curve. The n is related to the changes in the surface potential $\Delta\psi_s$. $\Delta\psi_s$ is controlled by the oxide capacitance C_{ox} and the depletion-region capacitance C_{js}. Therefore,

$$\frac{d\psi_s}{dV_{GS}} = \frac{C_{ox}}{C_{ox}+C_{js}} = \frac{1}{n}. \tag{3-2}$$

In Equation (3-1), the characteristic current is:

$$I_{D0} = 2n\beta U_T^{\,2} e^{-(\frac{V_{t0}}{nU_T})} \tag{3-3}$$

Where $\beta = \mu C_{ox} W/L$, μ =electron mobility, and W L are the channel width and channel width.

In Figure 3.1, the weak inversion and strong inversion cure are illustrated. As V_{GS} below the threshold voltage V_t, the device is in the weak inversion. In this range, the curve of the current is exponential (3-1). Above the threshold voltage, the range belongs to the saturation region. In the saturation region, the current is larger than that in the weak inversion. Its current equation is a square function. Therefore, the device in the weak inversion is suitable to low-voltage low-power circuit.

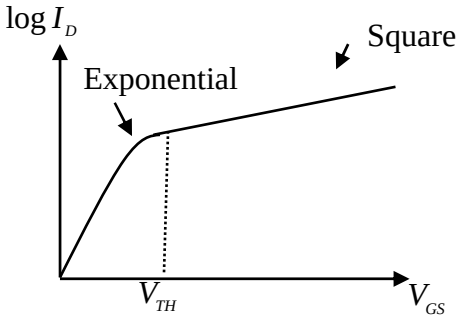


Figure 3.1 MOS weak inversion characteristics

In the weak inversion region, the transconductance can be found by differentiating V_{GS} [24] [5]. This result is

$$g_m = \frac{dI_D}{dV_{GS}} = I_{D0}\frac{W}{L}\frac{1}{nU_T}\exp(\frac{V_{GS}-U_T}{nU_T})\left[1-\exp(-\frac{V_{DS}}{U_T})\right] = \frac{I_D}{nU_T} \tag{3-4}$$

From Equation 3-4, the ratio of the transconductance to the current of an MOS transistor is:

$$\frac{g_m}{I_D} = \frac{1}{nV_T}. \tag{3-5}$$

In Equation 3-5, the ratio is independent of the overdrive. It is related with the n slop factor (n) and thermal voltage (V_t). In contrast to the saturation region, the ratio of the transconductance to the current is related to the overdrive voltage as show in Equation (3-6)

$$\frac{g_m}{I_D} = \frac{\sqrt{2k_nI_D}}{I_D} = \frac{2}{V_{GS}-V_T} = \frac{2}{V_{ov}} \tag{3-6}$$

Under the overdrive voltage in strong inversions, g_m / I_D ration is :

$$V_{ov} = V_{GS} - U_T = 2nU_T \tag{3-7}$$

The value in Equation (3-7) is about 78 mV when n is 1.5. The ratio of the transconductance to the current versus overdrive voltage is illustrated in Figure 3.2.
It is the key point between the strong inversion and the weak inversion.

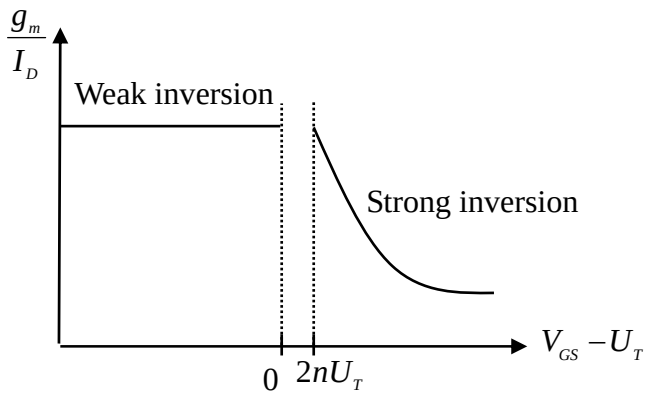


Figure 3.2 Transconductance to current ratio versus overdrive

The other parameter of the small signal model is the resistance variation. For weak inversion and strong inversion, the channel-length modulation effect is the same. Thus the variation of r_{ds} with drain current is inversed current as shown in Equation (3-8)

$$r_{ds} = \frac{1}{\lambda I_{DS}} \tag{3-8}$$

where λ is the channel-length modulation factor. I_{DS} is the drain current. In Figure 3.3 the drain current versus drain-source voltage in weak inversion is illustrated. The size is W=5 μm and L=5 μm in TSMC 0.18 process. The drain current is almost constant when $V_{DS} > 3U_T$. It implies the variation of r_{ds} is small.

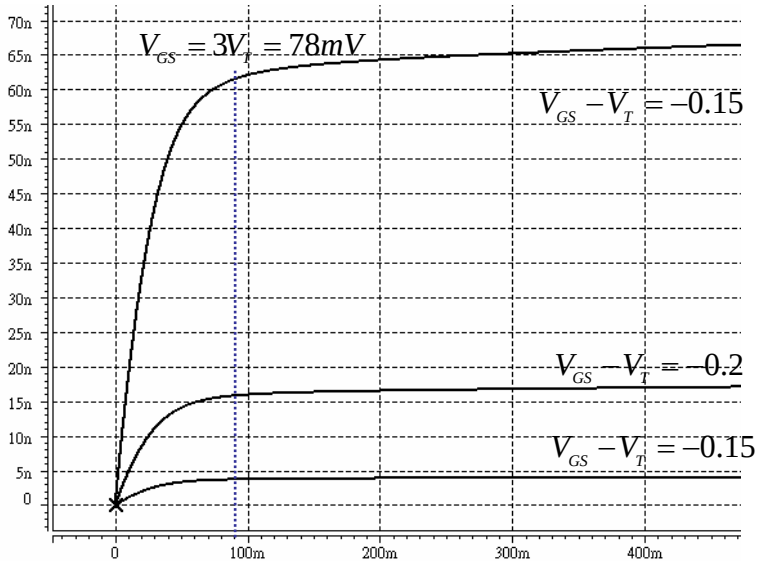


Figure 3.3 Drain current versus drain-source voltage in weak inversion

Next, the mid-band voltage of the common source stage is considered. The mid-band gain is

$$A_{gain} = -g_m r_{ds} \tag{3-9}$$

In the strong inversion, the gain varies with I_D as

$$A_{gain} = \frac{\sqrt{2KI_D}}{I_D} = \sqrt{\frac{2K}{I_D}} \tag{3-10}$$

In the weak inversion, the mid-band gain approaches a constant value. It is independent of drain current I_D as shown in Equation (3-11).

$$A_{gain} = \frac{I_D}{nV_T}\frac{1}{I_D} = \frac{1}{nV_T} \tag{3-11}$$

3.3 Filter in Chopper Amplifier

The filter in the chopper amplifier takes an important role. Its purpose is to cancel the noise out of the bandwidth. Therefore, in order to improve the signal to noise ratio, the filter is an important issue. Switched-capacitor filter is introduced latter.

3.3.1 Fundamental of Switched-capacitor circuit

In switched-capacitor circuit is shown in Figure 3.4 [21]. To analyze this circuit, V_1 and V_2 are the DC voltage. When ϕ_1 is on, C_1 is charged to V_1. When ϕ_2 is on, C_1 is charged to V_2. The ϕ_1 and ϕ_2 are non-overlapping clocks. The charge in capacitor C_1 can be presented with mathematic:

$$\Delta Q = C_1\left(V_1 - V_2\right) \tag{3-12}$$

The average current I_{av} is equal that the charge in the capacitor divides the clock period.

$$I_{av} = \frac{C_1(V_1 - V_2)}{T} \tag{3-13}$$

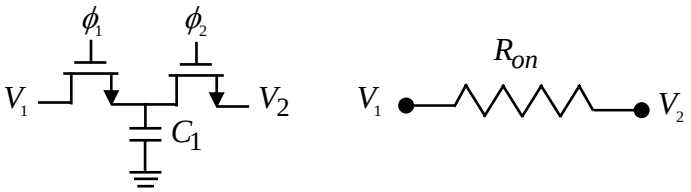


Figure 3.4 Resistor equivalence of the switched-capacitor

At the same time, the equivalent resistor can be shown as:

$$I_{av} = \frac{V_1 - V_2}{R_{eq}} \tag{3-14}$$

Therefore, the equivalent resistor of the switched-capacitor is:

$$R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s} \tag{3-15}$$

Switched capacitor integrator is an important role in discrete time integrator [21]. It uses in the switched-capacitor filter or sigma-delta modulator. Usually, parasitic-sensitive integrator and parasitic-insensitive integrator are introduced.

The parasitic-sensitive integrator is shown in Figure 3.5. At the time $(nT - T)$, the voltage across the capacitor C_2 is $V_{co}(nT - T)$. Therefore, the charge on C_2 is equal to $C_2 V_{co}(nT - T)$. When this time $(nT - T)$, ϕ_1 is just off and ϕ_2 is off. The input signal is sampled on C_1. The charge on C_1 is equal to $C_1 V_{ci}(nT - T)$. When ϕ_2 is on, the charge on C_1 is transfer to the C_2. Therefore, the charge on C_1 is added to the charge on C_2. This causes the voltage across C_2 is negative.

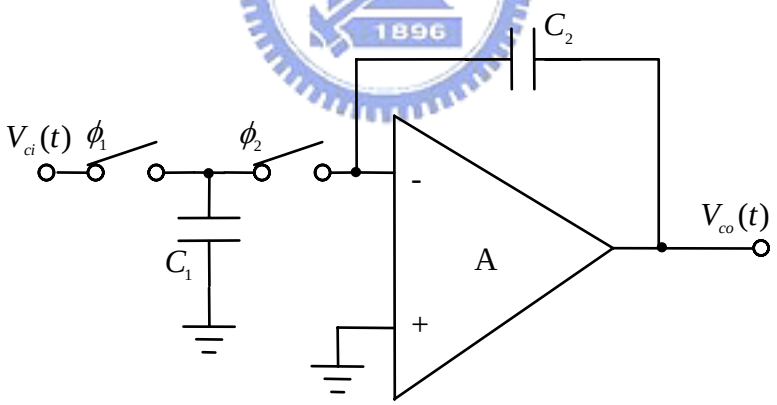


Figure 3.5 Parasitic-insensitive integrator

In Figure 3.6 the behavior during ϕ_1 and ϕ_2 is illustrated.

This phenomenon is presented by mathematical equation:

$$C_2 V_{co}(nT - \frac{T}{2}) = C_2 V_{co}(nT - T) - C_1 V_{ci}(nT - T) \tag{3-16}$$

At the end of the next ϕ_1, the charge on C_2 at time (nT) is equal to the charge at time $\left(nT - \frac{T}{2}\right)$. It can be shown as:

$$C_2V_{co}(nT) = C_2V_{co}(nT-T) - C_1V_{ci}(nT-T) \tag{3-17}$$

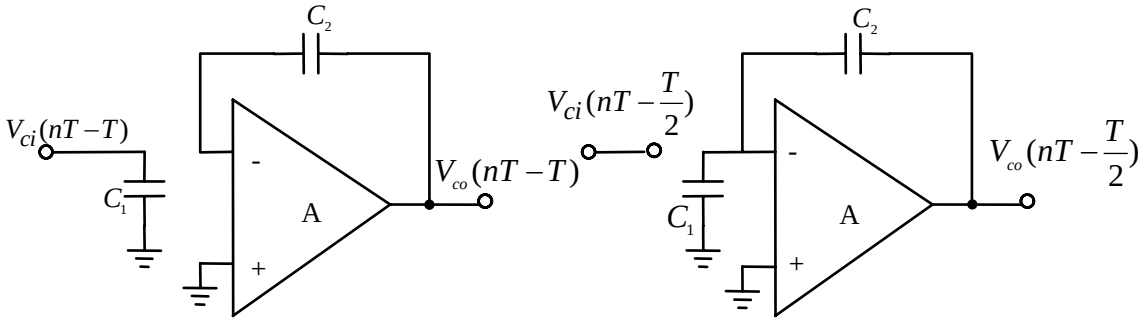


Figure 3.6 The parasitic-sensitive integrator

Equation (3-17) is further presented as:

$$C_2V_{co}(n) = C_2V_{co}(n-1) - C_1V_{ci}(n-1) \tag{3-18}$$

Taking (3-18) z-transform, it obtains:

$$V_{co}(Z) = Z^{-1}V_{co}(Z) - \frac{C_1}{C_2}Z^{-1}V_{ci}(Z) \tag{3-18}$$

$$H(Z) = \frac{V_{co}(Z)}{V_{ci}(Z)} = -(\frac{C_1}{C_2})\frac{Z^{-1}}{1-Z^{-1}} \tag{3-19}$$

The parasitic-insensitive integrator is a critical circuit to develop high-accuracy circuit. As its name, it is insensitive to parasitic capacitor [21]. Therefore, the parasitic-insensitive integrator is usually used for high-order high-resolution circuits,.

The parasitic-insensitive integrator is made up of four switches as shown in Figure 3.7. When ϕ_1 is on, C_1 is charged to $C_1V_{ci}(nT-T)$. Then C_2 turns on, the charge on C_1 discharge to the C_2. At this moment, the output voltage is positive.

In Figure 3.8 it can be presented in mathematical:

$$C_2V_{co}(nT-\frac{T}{2}) = C_2V_{co}(nT-T) + C_1V_{ci}(nT-T) \tag{3-20}$$

At the end of next time (nT), the charge on C_2 is the same at the time ($nT-\frac{T}{2}$). Therefore, the Equation (3-20) is:

$$C_2V_{co}(nT) = C_2V_{co}(nT-T) + C_1V_{ci}(nT-T) \tag{3-21}$$

Its z-transform is presented:

$$V_o(z) = Z^{-1}V_o(z) + \frac{C_1}{C_2} z^{-1}V_i(Z) \tag{3-22}$$

$$H(z) = \left(\frac{C_1}{C_2}\right)\frac{z^{-1}}{1-z^{-1}} \tag{3-23}$$

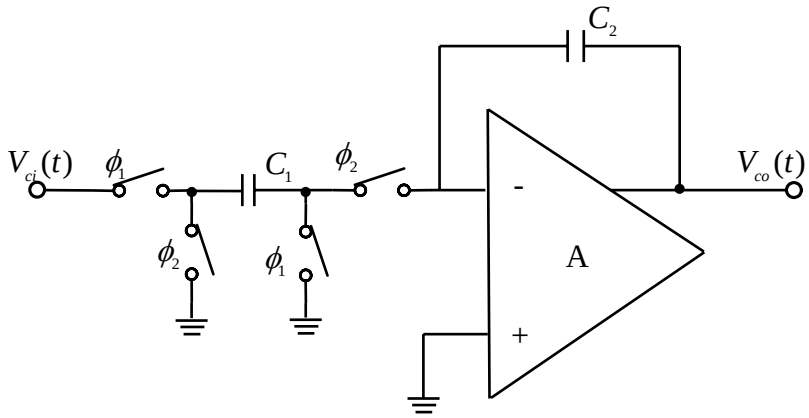


Figure 3.7 A non-inverting delaying integrator

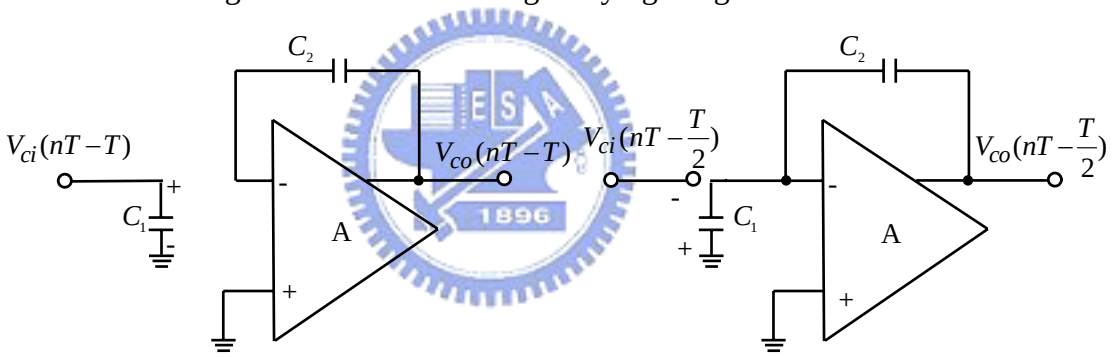


Figure 3.8 Behavior in each clock (a)ϕ_1 ,(b)ϕ_2

There is another parasitic-insensitive integrator as shown in Figure 3.9. It is different from the non-inverting integrator. When clock ϕ_1 is on, the capacitor is charged to $V_{ci}(t)$. Then the charge passes through C_2 to change the amount of the output voltage. In other words, when ϕ_2 turns on, the charge across C_2 is the same as the old charge. It stands for $C_2V_{co}(nT-\frac{T}{2}) = C_2V_{co}(nT-T)$, so its behavior and the z-transform are introduced.

$$C_2V_{co}(nT) = C_2V_{co}(nT-\frac{T}{2}) - C_1V_{ci}(nT) \tag{3-24}$$

$$C_2V_{co}(nT) = C_2V_{co}(nT-T) - C_1V_{ci}(nT) \tag{3-25}$$

$$H(z) = -\left(\frac{C_1}{C_2}\right)\frac{1}{1-z^{-1}} \tag{3-26}$$

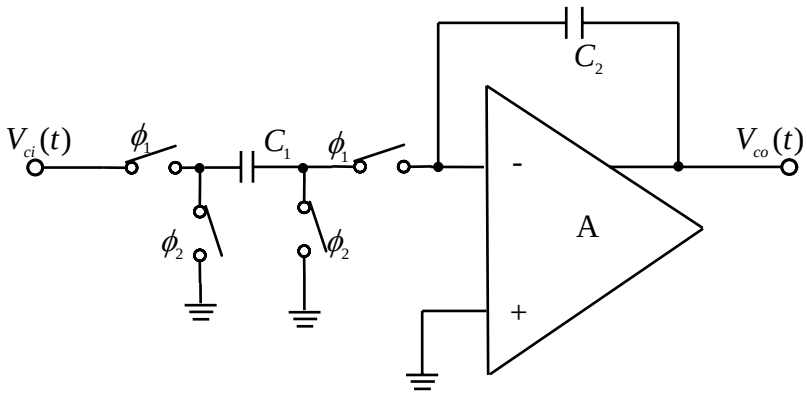


Figure 3.9 Delay-free integrator

3.3.2 The Architecture of Filter

Next, the architectures of the filter are introduced. It includes the first-order and second-order filter .

A first-order active-RC filter is shown in Figure 3.10. The resistors are replaced with delay-free switched capacitors. Therefore, the discrete-time first-order filter is illustrated as shown in Figure 3.11.

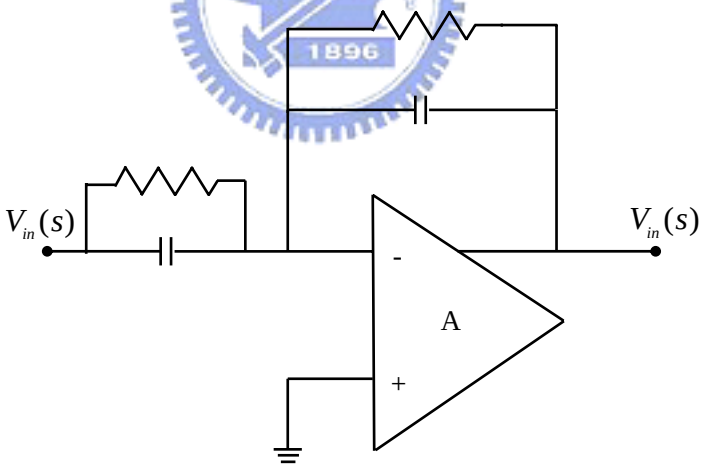


Figure 3.10 A first-order active-RC filter

According to the Figure 3.11 the transfer function is:

$$C_A(1-z^{-1})V_o = -C_3V_o(z) - C_2V_i(z) - C_1(1-z^{-1})V_i(z) \tag{3-27}$$

$$H(z)=\frac{V_o(z)}{V_i(z)}=-\frac{\left(\frac{C_1+C_2}{C_A}\right)z-\frac{C_1}{C_A}}{(1+\frac{C_3}{C_A})z-1} \tag{3-28}$$

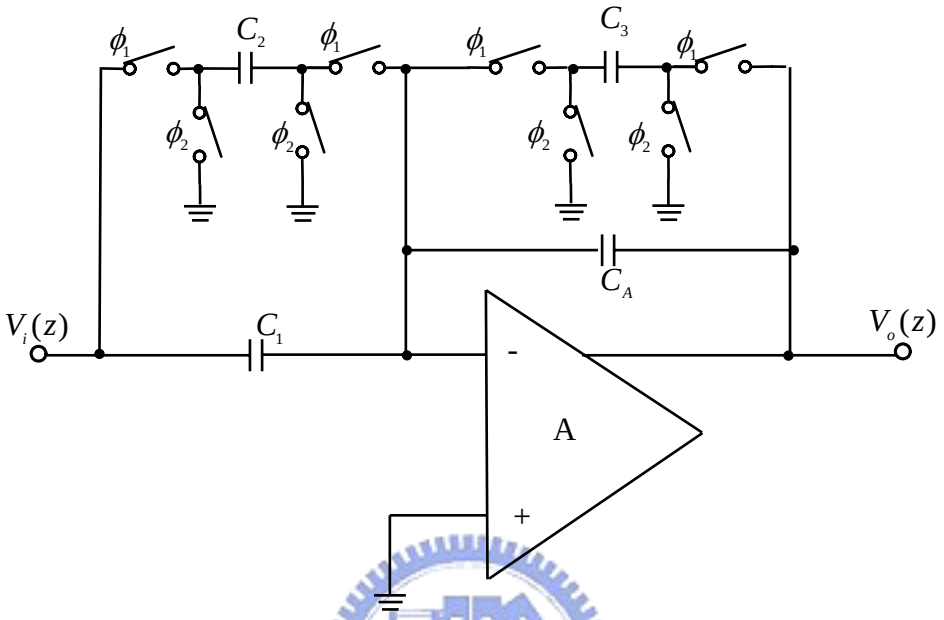


Figure 3.11 Discrete-time form

Next section, the architecture of the second-order filter is introduced. The one is the low-Q biquad filter, the other is high-Q biquad filter. These filters are made up of inverting integrator and non-inverting.

First, the architecture of the low-Q biquad filter is illustrated in Figure 3.12. According to the block diagram, the transform function of the architecture is illustrated. It design the coefficient according to the specification. The discrete-time architecture is illustrated in Figure 3.13. In Figure 3.12 the transfer function is

$$H\ (s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{k_2s^2+k_1s+k_0}{s^2+(\frac{\omega_0}{Q})+{\omega_0}^2} \tag{3-29}$$

The z-transfer function is shown as Figure 3.13:

$$H(z)=-\frac{(k_2+k_3)z^2+(k_1k_5-k_2-2k_3)+k_3}{(1+k_6)+(k_4k_5-k_6-2)+1} \tag{3-30}$$

According to the equations, designing filter is done.

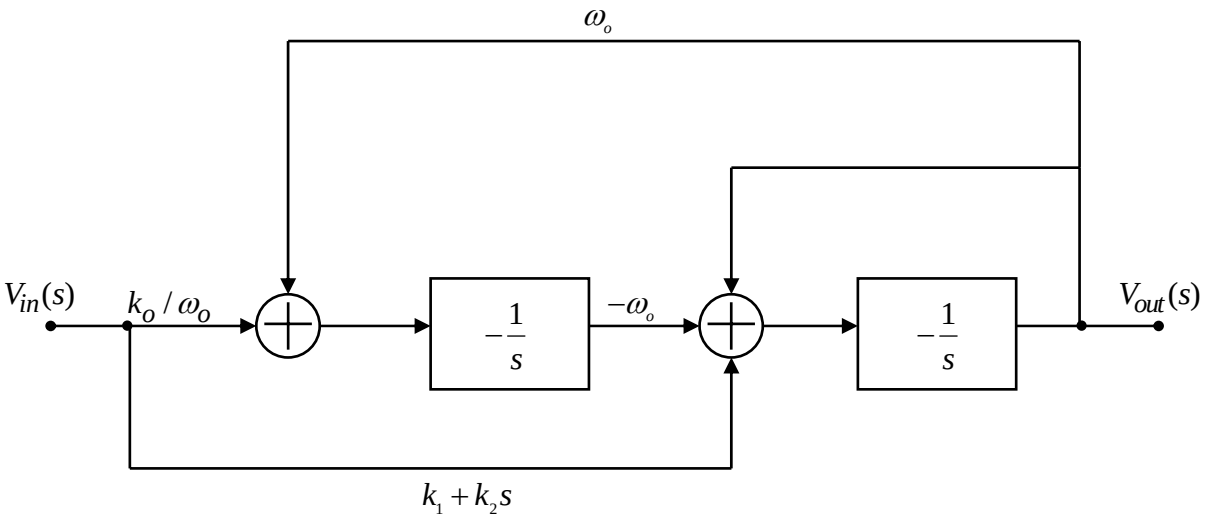


Figure 3.12 The block diagram of the biquad filter

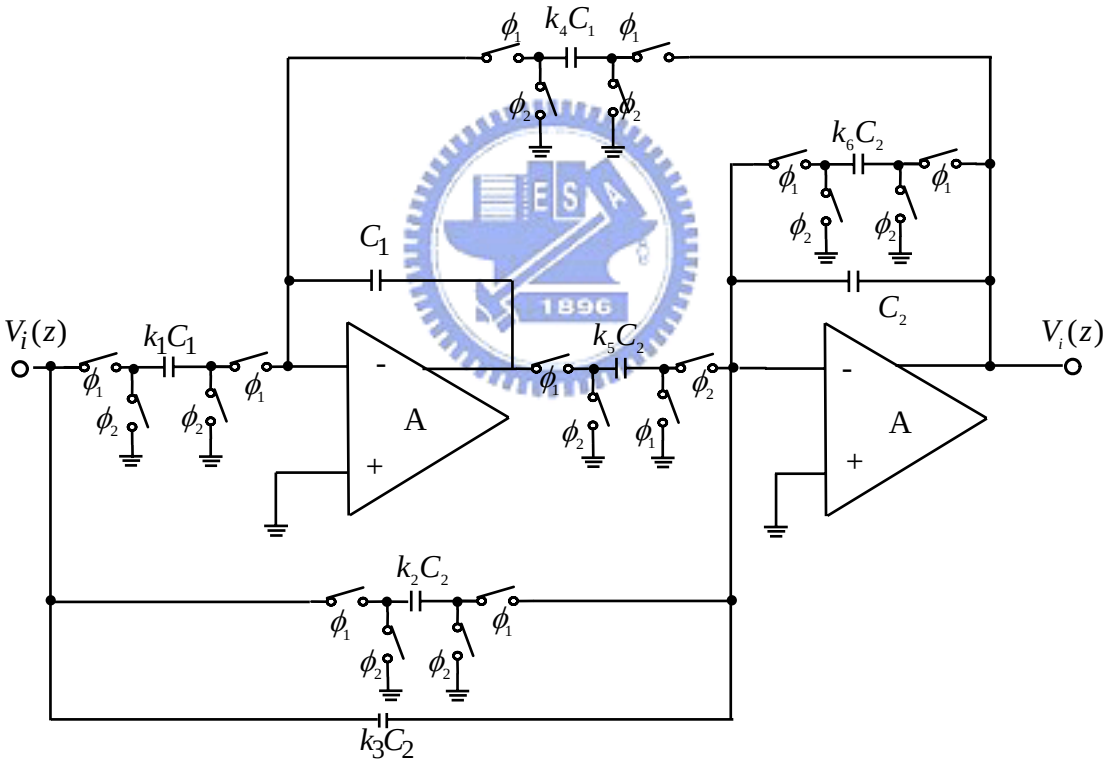


Figure 3.13 A low-Q switched capacitor biquad filter

The other architecture of the filter is high-Q biquad filter as shown in Figure 3.14 This value of Q in this architecture is limited to 5 or less. The elements in high-Q biquad filter is not too large. If the element is too large, it may be not realized. The transfer function of the high-Q biquad filter is shown as Equation (3-29). To replace resistor with switched-capacitor integrator, the architecture of the discrete-time form

is described as shown in Figure 3.15

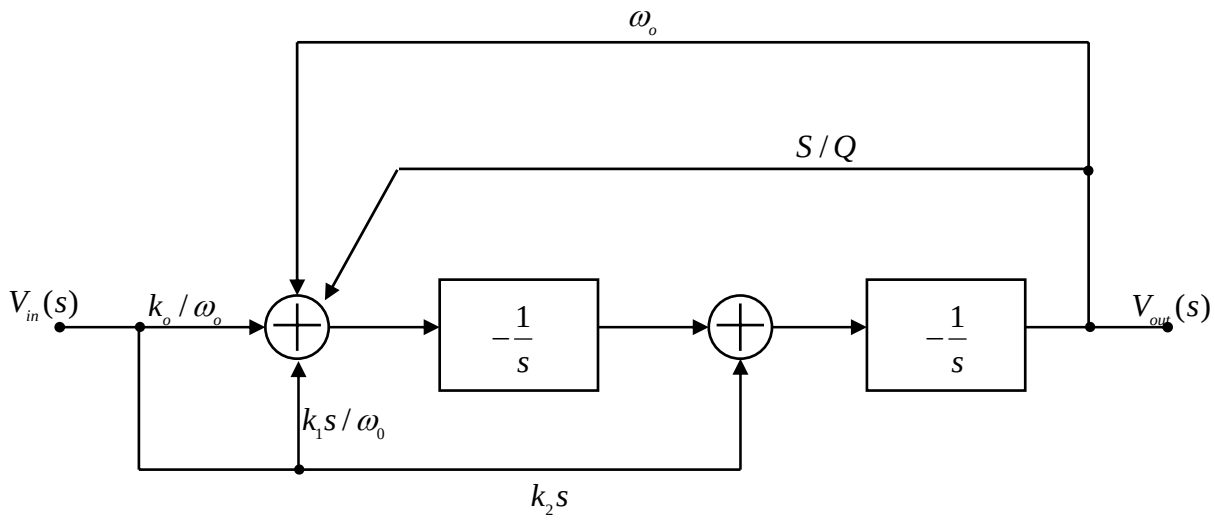


Figure 3.14 The high-Q biauad filter

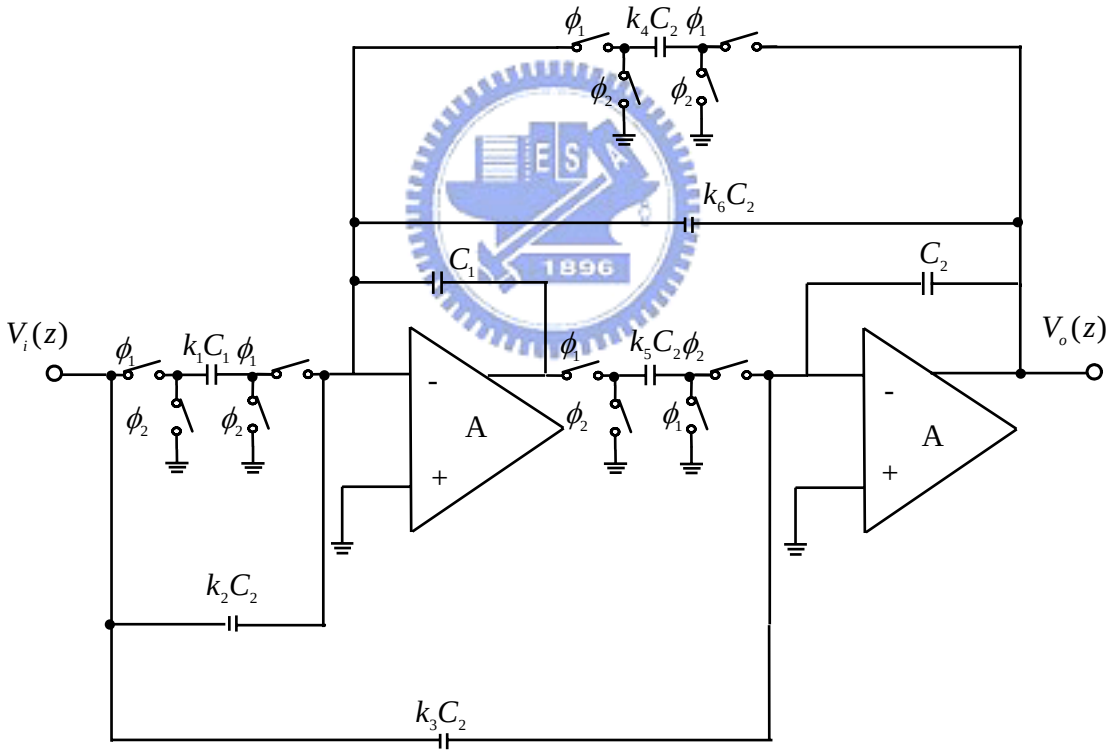


Figure 3.15 High-Q switched-capacitor biquad filter

Taking the z-transform in Figure 3.15, the transform function of the high-Q filter is

$$H(z)=\frac{V_o(z)}{V_i(z)}=-\frac{k_3z^2+\left(k_1k_5+k_2k_5-2k_3\right)z+\left(k_3-k_2k_5\right)}{z^2+\left(k_4k_5+k_5k_6-2\right)+\left(1-k_5k_6\right)} \tag{3-31}$$

According to Equation (3-29) (3-31), the switched-capacitor filter is designed for the specification.

3.4 Low-Voltage Switch

At low supply voltage, it is difficult to drive the switch. Under this condition, the overdrive voltage is lower than threshold voltage. The switch is not open entirely. The signal must have some loss, it is a serious problem in sampling circuit. How to drive the switch at low supply voltage must be solved. The switch conductance for different input depending on supply voltage is illustrated in Figure 3.16. In Figure 3.16 (a) it is at standard voltage, Figure 3.16 (b) at low supply voltage.

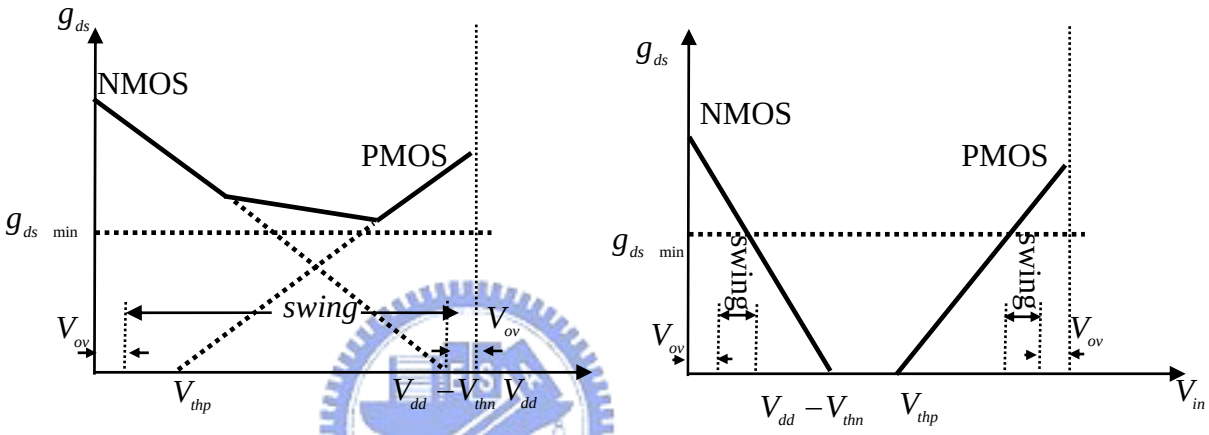


Figure 3.16 Transmission gate conductance at (a) standard, (b)low supply voltage

Low threshold voltage is one of the solution to be solved the switch at low supply voltage. The threshold voltage is given by

$$V_{th} = \phi_{GB} - \frac{Q_{ox}}{C_{ox}} + 2\phi_F + \gamma\sqrt{|2\phi_F| - V_{BS}} \tag{3-32}$$

The above equations show that the V_{th} depends on V_{BS}. The bulk to source junction causes the threshold voltage increase due to the body effect. So in order to drive switches at low supply voltage, the threshold voltage needs to be decreased. Therefore, the body effect reversed, the threshold voltage can be decreased.

However, decreasing the threshold voltage causes another problem. When switch is off, there is leakage current between bulk and source. If this condition happens, the resolution of this circuit must lower. Non-ideal items is hard to be expected.

The voltage multiplier is another technique. It converts the lower voltage to higher voltage. In higher supply voltage, the overdrive voltage is higher enough to

drive the switch. The aliasing phenomenon can be decreased. Figure 3.17 shows a voltage boosted clock driver. Fist, C_1 and C_2 are charged to V_{dd} which passes through cross-coupled NMOS M1 and M2. When clock input signal, goes high, the output voltage must be pushed to $2V_{dd}$. However, the output voltage can not achieve $2V_{dd}$, in transition time charge sharing happens. So the capacitor C_2 must be large enough, charge sharing effect will be decreased little. On the side, latch-up can be avoided; the voltage doubler is used as shown in Figure 3.18. The bulk of the PMOS M3 is tied to a voltage doubler.

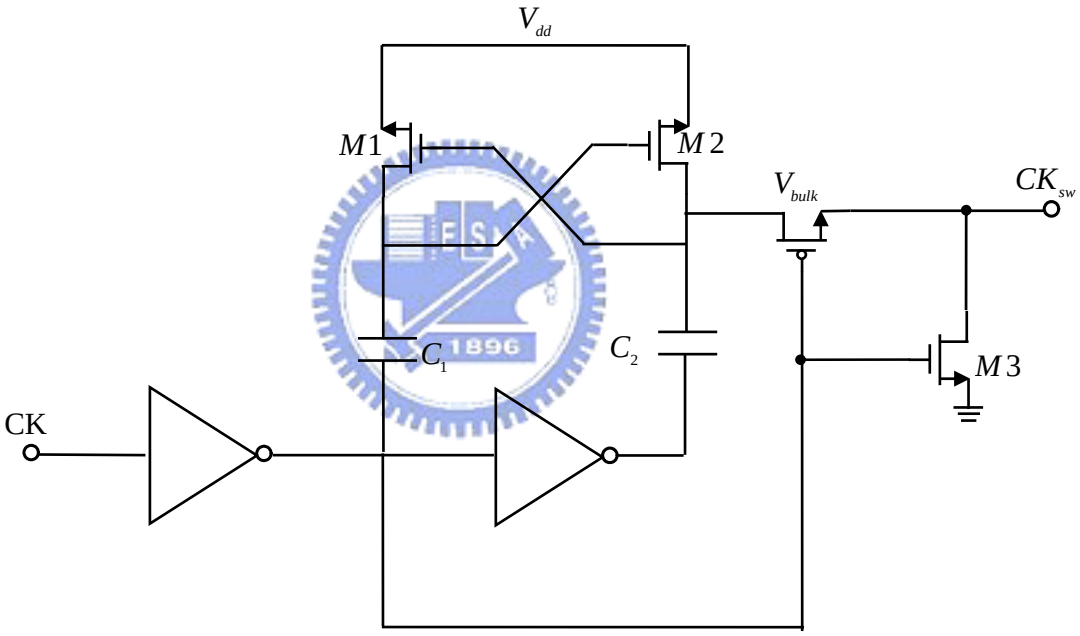


Figure 3.17 Voltage boosted clock driver

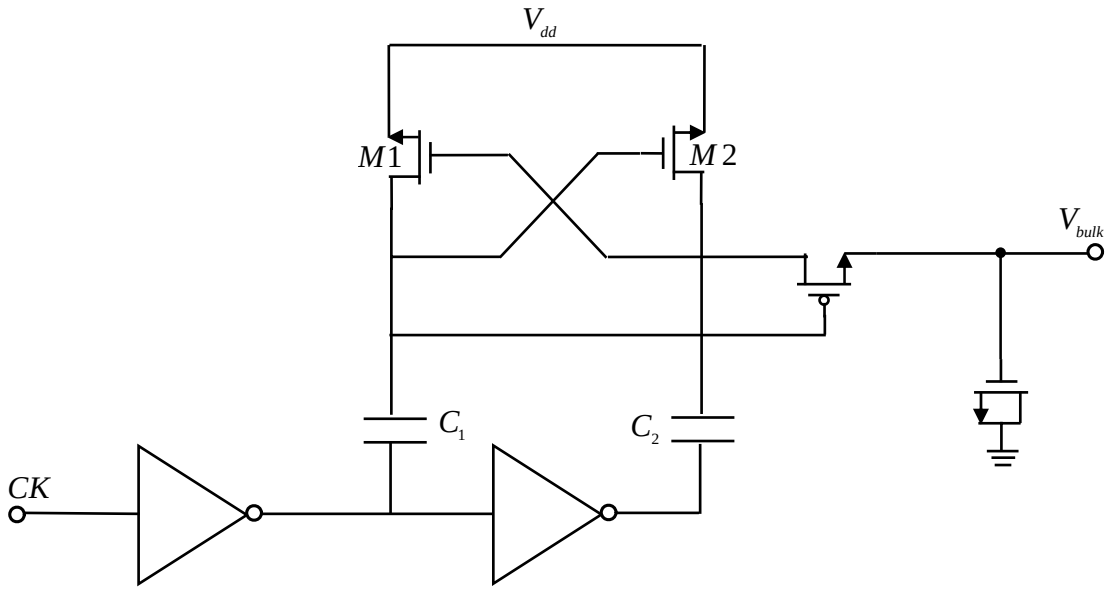


Figure 3.18 Voltage doubler

3.5 Summary

In this chapter, the MOS transistor working in weak inversion, switched-capacitor circuits, and low-voltage switch techniques are introduced. There are the elements in the chopper amplifier. In order to work at low supply voltage, the MOS working in weak inversion is needed. The switch working at low supply voltage is another important issue. Summing up this issue, how to design a low-voltage low-power circuit is a critical thing.

Chapter 4

The Front-end Circuit of the Thermopile

4.1 Introduction

The MOS transistor working in weak inversion, switched-capacitor filter, and switches at low supply voltage are introduced in the previous chapter. Some of them are used in this thesis. The amplifier working in weak inversion is necessary for low supply voltage. The MOS working in strong inversion is not realized under low supply voltage. In contrast to strong inversion, weak inversion is suitable for low supply voltage. The amplifier working in weak inversion is used in switched-capacitor filter, preamplifier, and post-amplifier. On the side, the total architecture is illustrated. The preamplifier, switched-capacitor filter, and post-amplifier are introduced detail. The noise of the preamplifier is also carefully calculated in this chapter. Finally, the front-end circuit of the thermopile sensor (preamplifier, filter, and post-amplifier) is realized in this thesis.

4.2 System Architecture

In Chapter 2, the architecture of the chopper amplifier is introduced. The

preamplifier, filter, and post-amplifier are the parts of architecture. The front of the chopper amplifier is a thermopile sensor. The thermopile sensor detects the temperature to transfer to the voltage. Then the voltage passes through chopper amplifier, filter, and ADC. Finally, the signal is transferred to digital form [3] [14]. The block diagram is shown in Figure 4.1

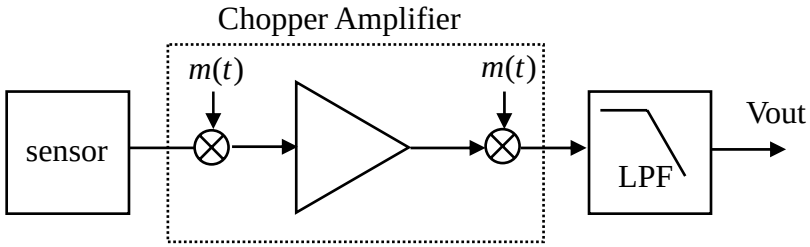


Figure 4.1 Block diagram of the temperature sensor

Sensor Signal In this thermopile sensor, the signal specification is:

Type: voltage

Temperature range: $32^{\circ} \sim 44^{\circ}$

Signal magnitude: $10\mu V / ^{\circ} 0.2C$

Signal bandwidth: 50Hz

The output voltage rang of the thermopile sensor is from $10\,\mu V$ to $600\,\mu V$. This signal magnitude is only a few micro volts. The noise power must not be too large under this condition. In this thesis, the system resolution is 8-bit. When the resolution is 8-bit, the signal to noise ratio is worked out. Its value is approximately 50db. According to signal to noise ratio (SNR) the noise power is calculated as [6]

$$SNR = 20 \times \log \frac{600\mu V}{\sqrt{2} \cdot N_{rms}} = 50db\,. \tag{4-1}$$

The noise root mean square is approximately $1.38\,\mu V$. Therefore, the noise root mean square can not be over $1.38\,\mu V$ in the output of the sensor.

Chopper Amplifier Due to the magnitude of the sensor signal is too small, and the bandwidth is DC value, the signal to noise ratio does not achieve the specification [5]. The chopper amplifier is used to cancel the low frequency noise to increase the signal to noise ratio. Therefore the gain of the system must be another issue. Thinking about

signal to noise ratio, the gain of the system must achieve to 60db. The open loop amplifier is used in this block

Low Pass Filter In this architecture, the purpose of the low pass filter is used to cancel the noise [7] [4]. According to the noise root mean square value, the second-order switched capacitor filter is implemented. In this low pass filter, its pass band frequency is 50hz, and its stop-band frequency is 500hz. Due to this specification, the total noise power is integrated in this spectrum range. The value is the total noise power.

4.3 Implementation of Chopper Amplifier

The chopper amplifier is the first stage. The first stage is an important element in all system. The noise power behind the chopper amplifier can be negligible. Because the gain of the chopper amplifier is large, the input referred noise changes small. So the major noise is produced in the first stage. Therefore the flicker noise and thermal noise comes from the first stage are considered. The chopper amplifier can cancel low frequency noise (flicker noise). Therefore the thermal noise dominants noise power. How to decrease the noise power is important.

4.3.1 Noise Consideration

In order to consider the thermal noise of the amplifier, the noise model must be considered. In Chapter 2, the noise of the MOS transistor is brought out. It includes the thermal noise and flicker noise. The noise model can be shown in Figure 4.2

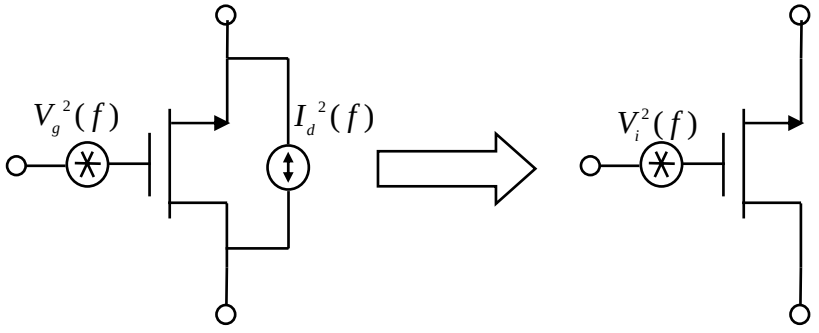


Figure 4.2 Noise model

The equivalent model includes flicker and thermal noise. The noise divides by g_m^2 to the input. Hence, the PSD of an equivalent input noise is calculated as

$$S_{eq}(f) = \frac{8}{3}kT\frac{1}{gm} + \frac{k_f}{WLC_{ox}f} \quad . \tag{4-2}$$

According to the equivalent input noise, the input referred noise in amplifier is illustrated. Each noise of the MOS transistor is independent each other. Therefore, they are uncorrelated. Next, current mirror and telescopic circuit working in weak inversion are discussed. Figure 4.3 shows the total noise source in current mirror amplifier [7].

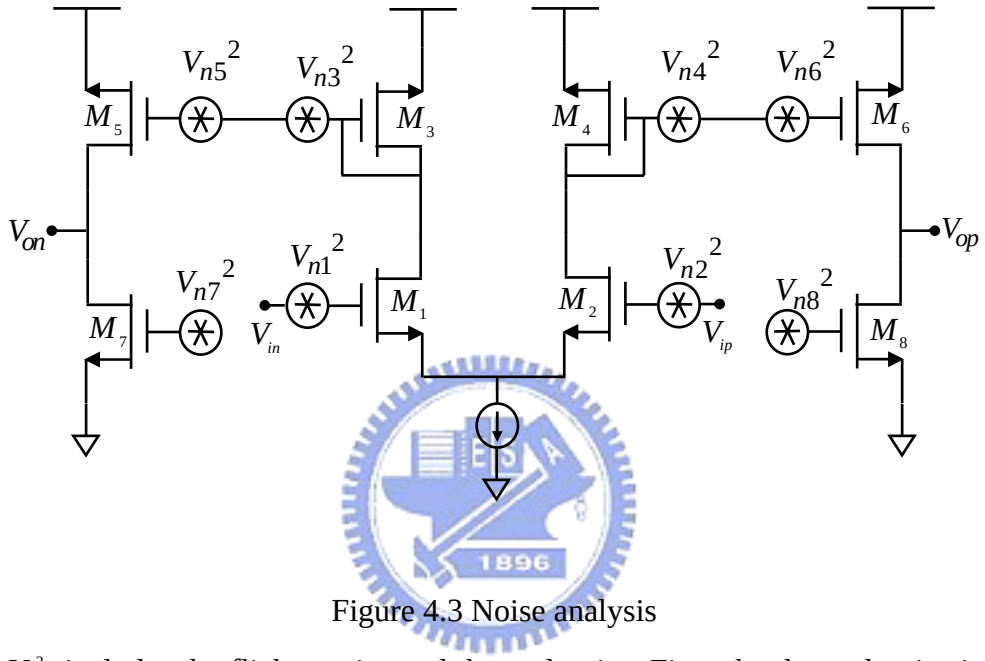


Figure 4.3 Noise analysis

The V_n^2 includes the flicker noise and thermal noise. First, the thermal noise is only calculated. The $\overline{V_n}^2$ is shown as $\frac{8KT}{3g_m}$. The total thermal noise power is presented

$$\overline{V_{o,total}}^2 = V_{n1}^2(g_{m1}r_{out})^2 + V_{n3}^2(g_{m3}r_{out})^2 + V_{n5}^2(g_{m5}r_{out})^2 + V_{n7}^2(g_{m7}r_{out})^2$$

$$+V_{n2}^2(g_{m2}r_{out})^2 + V_{n4}^2(g_{m4}r_{out})^2 + V_{n6}^2(g_{m6}r_{out})^2 + V_{n8}^2(g_{m8}r_{out})^2 \tag{4-2}$$

Because the circuit is symmetry, the total noise power can be presented as

$$\overline{V_{o,total}}^2 = 2(V_{n1}^2(g_{m1}r_{out})^2 + V_{n3}^2(g_{m3}r_{out})^2 + V_{n5}^2(g_{m5}r_{out})^2 + V_{n7}^2(g_{m7}r_{out})^2) \tag{4-3}$$

The $\overline{V_n}^2$ is replaced by $\frac{8KT}{3g_m}$, the Equation (4-3) is shown as:

$$\overline{V_{o,thermal}}^2 = 2(\frac{8kT}{3g_{m1}}(g_{m1}r_{out})^2 + \frac{8kT}{3g_{m3}}(g_{m3}r_{out})^2$$

$$+\frac{8kT}{3g_{m5}}(g_{m5}r_{out})^2+\frac{8kT}{3g_{m7}}(g_{m7}r_{out})^2) \tag{4-4}$$

The Equation (4-4) is divided by $(g_{m1}R_{out})^2$, therefore the total input referred thermal noise spectral density is:

$$\overline{V^2_{i,total}(f)}=\frac{16kT}{3g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}+\frac{g_{m5}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right). \tag{4-5}$$

Second, the flicker noise is considered. The output noise spectral density is

$$\overline{V^2_{o,flicker}}=\frac{k_f}{f\cdot C_{ox}W_1L_1}(g_{m1}r_{out})^2+\frac{k_f}{f\cdot C_{ox}W_3L_3}(g_{m3}r_{out})^2$$
$$+\frac{k_f}{f\cdot C_{ox}W_5L_5}(g_{m5}r_{out})^2+\frac{k_f}{f\cdot C_{ox}W_7L_7}(g_{m7}r_{out})^2 \tag{4-6}$$

The input referred noise can be shown as:

$$\overline{V^2_{i,flicker}}=\frac{k_f}{f\cdot C_{ox}W_1L_1}\cdot 1+\frac{k_f}{f\cdot C_{ox}W_2L_2}\left(\frac{g_{m3}}{g_{m1}}\right)^2$$
$$+\frac{k_f}{f\cdot C_{ox}W_5L_5}\left(\frac{g_{m5}}{g_{m1}}\right)^2+\frac{k_f}{f\cdot C_{ox}W_7L_7}\left(\frac{g_{m7}}{g_{m1}}\right)^2 \tag{4-7}$$

The flicker corner noise frequency is presented, when the flicker noise is equal to the thermal noise as $V^2_{i,theraml}=V^2_{i,flicker}$. According to the Equation (4-5) and (4-7), the flicker noise corner frequency is obtained.

In the telescopic amplifier, the noise is analyzed. The manner is the same with current mirror amplifier. In Figure 4.4, the noise in the telescopic amplifier is shown as

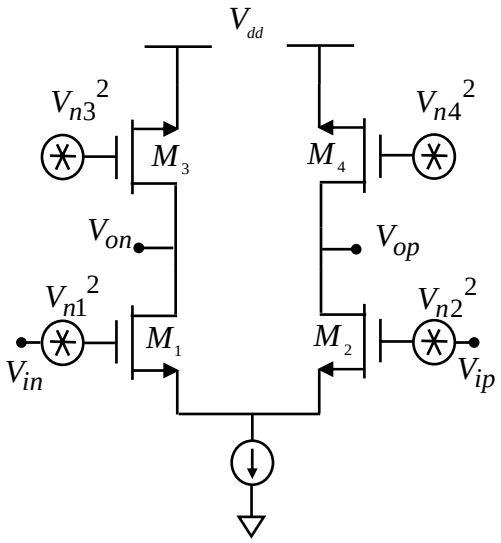


Figure4. 4 Noise analysis in telescopic current

The input referred flicker and thermal noise are shown as

$$\overline{V^2_{i,thermal}(f)} = \frac{16kT}{3g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}\right) \tag{4-8}$$

$$\overline{V^2_{i,flicker}} = \frac{k_f}{f\cdot C_{ox}W_1L_1}\cdot 1+\frac{k_f}{f\cdot C_{ox}W_2L_2}\left(\frac{g_{m3}}{g_{m1}}\right)^2 \tag{4-9}$$

In a word, the thermal and flicker noise are shown in MOS circuit.

In Section 4.2, the noise power is calculated. The filter bandwidth is set. Because the chopper amplifier cancel the flicker noise, the thermal noise dominants the total noise power. The noise bandwidth is known form the filter bandwidth, the thermal noise power is obtained. The current mirror amplifier is taken as example. The g_{m1} is calculated. First, the g_m is equal each other. Second, the thermal noise power spectral density is calculated $80nV/\sqrt{Hz}$ in due to filter bandwidth. Therefore the transconductance g_m can be presented as:

$$\overline{V^2_{i,theraml}(f)} = \frac{16kT}{3g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}+\frac{g_{m5}}{g_{m1}}+\frac{g_{m7}}{g_{m1}}\right) = (80nV)^2 \tag{4-10}$$

According to Equation (4-10), g_m is $13.8\mu A/V$. Therefore the g_m must be less than $13.8\mu A/V$.

4.3.2 Noise Efficient Factor

We are interested in minimizing noise in strict power. They are tradeoff between noise and power. Noise efficient factor is considered. Noise efficient factor is related with noise and power. According to noise efficient factor, we distinguish between differential architectures. The noise efficient factor is introduced in Equation (4-11).

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{total}}{\pi \cdot V_T \cdot 4kT \cdot BW}} . \quad (4\text{-}11)$$

Where $V_{ni,rms}$ is the input-referred rms noise voltage. I_{total} is the total current. BW is the amplifier bandwidth. V_T is the thermal voltage.

The noise efficient factor is an important factor. It is used to designing the chopper amplifier. The value of the NEF is smaller, the chopper amplifier is better.

4.3.3 Figure of Merit

There is another index to design chopper amplifier. The amplifier focused on noise and low supply voltage. Therefore, the figure of merit focused on noise, power and area, the equation is

$$FOM = \frac{1}{N \times S \times P} . \quad (4\text{-}12)$$

Where N is the noise density. P is the power dissipation. S is the chip area. According to the FOM[8], the tradeoff between cost and power dissipation is distinguish. In contrast to the NEF (noise efficient factor), the FOM (figure of merit) focus on area. Therefore the cost is considered.

4.3.4 Summary

In order to design the chopper amplifier efficiently, the factors as NEF, FOM are considered. On the side, the SNR is another issue. Therefore, the signal before ADC must be large to suit to the specification. The signal must be large than 0.5v to achieve SNR. The gain of the system must be large 60db. The gain can be divided as Table 1

	Pre-amplifier	Post-amplifier
Type 1	60db	0db
Type 2	50db	10db
Type 3	40db	20db
Type 4	30db	30db

Table 1 The gain of the block

The best type is chosen. Because the chopper amplifier is modulation signal, the chopper amplifier must be faster than the modulation signal. First, we assume that the modulation signal clock is 10k hz, the chopper amplifier must be faster than the 10k hz.

This key point lists following to design the chopper amplifier

(1) The unity gain frequency,

(2) Thermal noise value,

(3) Flicker noise,

(4) Flicker noise corner frequency,

(5) Slew rate,

(6) Noise efficient factor,

(7) Figure of merit.

Integrating with these rules, the chopper amplifier is designed. The design flow is illustrated as shown in Figure 4.5. First, the unity gain frequency is decided, then the transconductance and current is found. Next, the slew rate of amplifier is checked. If the slew rate is suitable for the specification, the flow can continuous. However the slew rate may be not suitable for the specification. In this condition, the flow must be return to start. When the slew rate is completed, next step decide the MOS transistor size. Finally, the noise efficient factor and figure of merit are calculated. In this flow, the size of the differential pair is considered in the FOM.

The noise efficient factor and figure of merit are the bases of the amplifier comparison. According to the parameter, the gain of the first stage can be distinguished. The parameter of the current mirror and telescopic amplifier are listed in Table 2. In Table 2, the gain of each block is decided and the telescopic amplifier is design in the first stage .

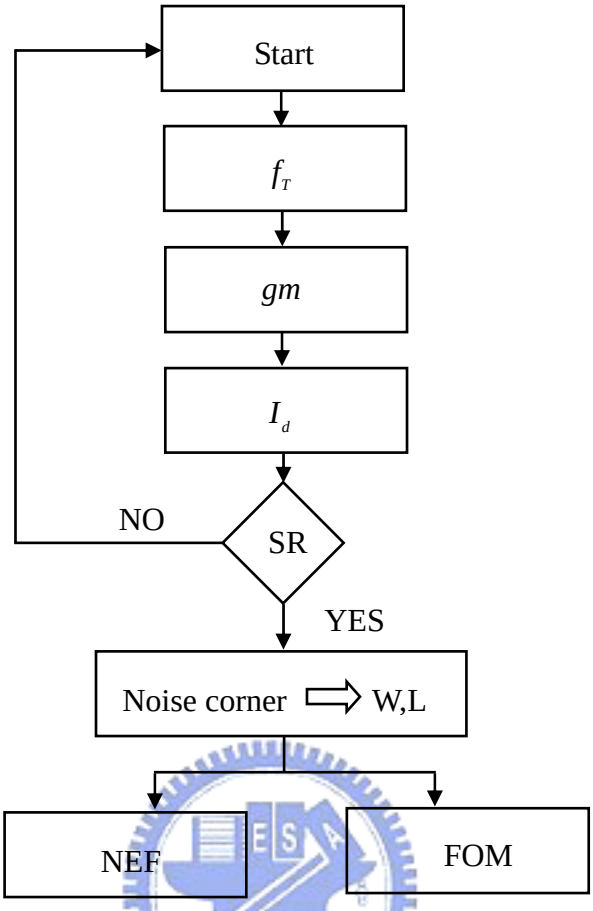


Figure 4.5 The design flow

First Stage	$gm\ (\mu V/A)$	$I_d\ (nA)$	Noise$\left(nV/\sqrt{Hz}\right)$	NEF	FOM
60db	125	4.875	26	4.3	4.598
50db	39	1.521	50	4.6	23
40db	12	0.486	85	4.5	73
35db	89	0.347	99	4.5	232

Table 2 Current mirror type

First Stage	$gm\ (\mu V / A)$	$I_d\ (nA)$	Noise$\left(nV/\sqrt{Hz}\right)$	NEF	FOM
60db	125	4.875	26	2.1	12
50db	39	1.521	33	2.2	73.2
40db	12	0.486	60	2.25	2.9
35db	89	0.347	20	8.2	721

Table 3 The telescopic amplifier type

Table 2 and Table 3 are suitable for the slew rate. Therefore, the solution is suitable for the specification. Last, we choose that the gain is 40db in first stage.

4.4 Filter Design

4.4.1 System Architecture

According to the signal bandwidth, the pass-band frequency is 50 hz. In this thesis the filter type is butterworth. Its characteristic of the butterworth is flat in pass bandwidth and stop bandwidth. The transfer function of the second-order low pass filter is shown as

$$H(s)=\frac{V_o(s)}{V_i(s)}=\frac{98596}{s^2+444s+98596}. \tag{4-13}$$

The Bode Diagram of the transfer function is shown as Figure 4.6

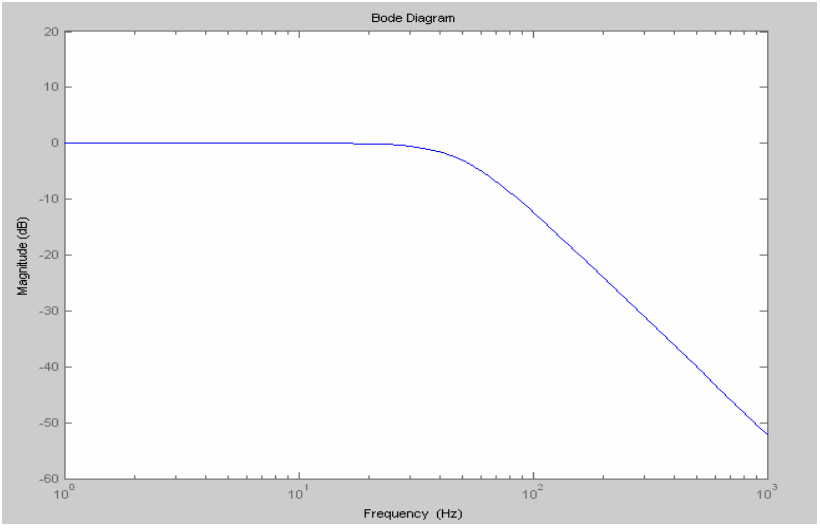


Figure 4.6 The Bode Diagram

4.4.2 Switched Capacitor Low Pass Filter

In Chapter 3, the parameter insensitive integrators and design flow are introduced. The switched capacitor filter is implemented by these items [22]. The transfer function is already known. The parameter of the switched capacitor low pass filter can be decided. The transfer function belongs to the low-Q switched capacitor filter in Figure 3.13. The parameter is shown as Table 4. In the thesis, the clock signal is 6.4k. Therefore, the capacitor value is calculated.

k_1	k_4	k_5	k_6
0.049	0.049	0.049	0.064

Table 4 The parameter of the switched capacitor filter

4.4.3 Filter Noise

In Section 4.3, the input referred noise in the amplifier is introduced. In this section, the noise in the switched capacitor integrator is shown in Figure 3.7[23]. In Figure 4.7, the noise is illustrated when the ϕ_1 is off.

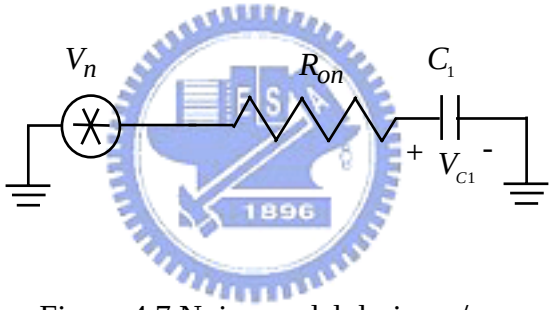


Figure 4.7 Noise model during ϕ_1

Its PSD is shown as

$$S_{n,\phi_1} = 4kTR_{on}. \tag{4-14}$$

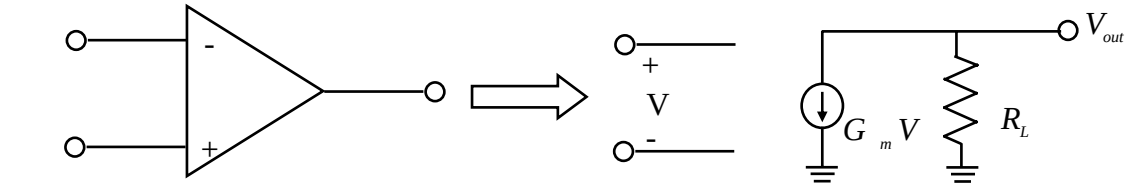
Its transfer function is derived:

$$H(s) = \frac{V_{c1}(s)}{V_n(s)} = \frac{1}{1+s\tau}. \tag{4-15}$$

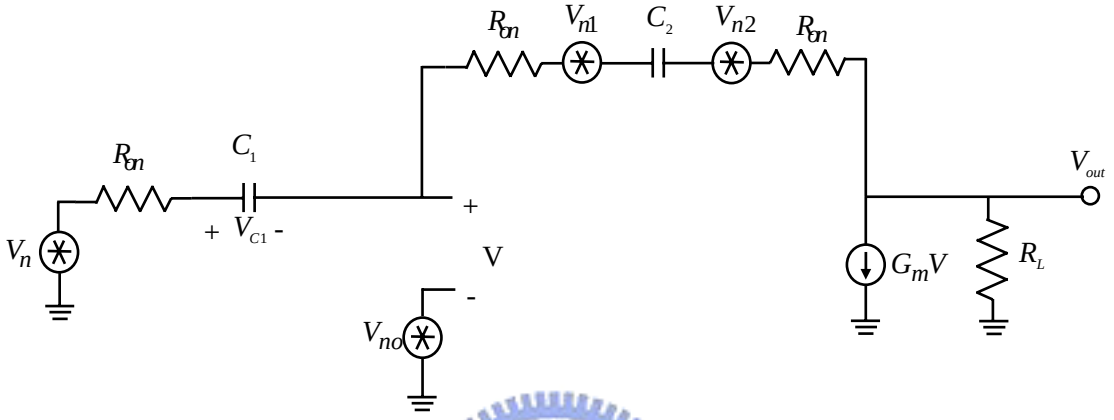
where $\tau = R_{on}C_1$. Hence, the thermal noise in C_1 is calculated.

$$\overline{V_{c1}^2} = \int_0^\infty S_{vt\_\phi 1}(f)\left|H(j2\pi f)\right|^2 df = \frac{4kTR_{on}}{4\tau} = \frac{kT}{C_1} \tag{4-16}$$

In Figure 4.8, the ϕ_2 is high. The total noise is illustrated. In this condition, the amplifier small-signal and the switch noise are analyzed.



(a)



(b)

Figure 4.8 (a) amplifier small-signal, (b) noise model in ϕ_2

In Figure 4.8 (a) $\beta G_m R_L \gg 1$, where $\beta = C_2/C_1 + C_2$ and $R_L \approx 0$ .In Figure 4.8(b) the noise voltage cross C_1 is presented

$$V_{C1} = \frac{V_n(s) - V_{no}(s)}{1 + s\tau} = \frac{V_n(s) - V_{no}(s)}{1 + s(R_{on} + 1/G_m)C_1}. \tag{4-17}$$

The transfer function is $H(s) = 1/1 + s\tau$. The total noise power in switch is calculated

$$\overline{V^2_{c1,sw}} = \int_0^\infty S_v(f)\left|H(j2\pi f)\right|^2 df = \frac{kTR_{on}}{(R_{on} + 1/G_m)C_1}$$

$$= \frac{kT/C_1}{(1 + 1/x)} \tag{4-19}$$

where $x = G_m R_{on}$. The noise power in amplifier is also considered. We assume the transfer function of amplifier is $H(s) = 1/1 + s\tau_{op}$, where $\tau_{op} = 2R_{on} + 1/g_m$. The thermal noise is $(16/3)kT/g_{m1}$ from the Equation (4-8). Therefore, the noise in the integrator is

$$\overline{V^2_{C1,op}} = \int_0^\infty S_{no,op}\left|H(j2\pi f)\right| df = \frac{S_{no,op}}{4\tau} = \frac{(16/3)kT/g_m}{4(2R_{on} + 1/g_m)C_1} = \frac{4}{3}\frac{kT/C_1}{1 + x}. \tag{4-20}$$

The total noise power includes the switch noise during ϕ_1, the switch noise, and the amplifier noise during ϕ_2. The three noise sources are uncorrelated. Therefore the total noise power is

$$\overline{V^2_{c1,total}} = \frac{kT}{C_1}\left(1+\frac{x}{1+x}+\frac{4/3}{1+x}\right) = \frac{kT}{C_1}\left(\frac{7/3+2x}{1+x}\right)$$

$$= \frac{2kT}{C_1}\left(1+\frac{1/6}{1+x}\right) \tag{4-21}$$

where $x = 2R_{on}g_{m1}$. If $x \gg 1$ the total noise power can be approach to be $2kT/C_1$. The noise power in switch capacitor is

$$\overline{V'^2_{c1}} = V^2_{c1}\cdot\frac{f_B}{f_S/2}. \tag{4-22}$$

Where f_B is signal bandwidth. Considering SNR is 50db, the unit value of the switch capacitor is obtained. If the signal is 60mV, the noise power is calculated to achieve the specification. Therefore, the switch capacitor must be over 242f as shown in Equation (4-24).

$$\overline{V'^2_{c1}} \le V^2_{c1}\cdot\frac{f_B}{f_S/2} = \left(\frac{0.06}{\sqrt{2}\cdot 1778}\right)^2 = (23\mu V)^2 . \tag{4-23}$$

According to the noise power, the switch capacitor is shown as:

$$C_1 = \frac{2kTf_s/2}{f_B} = 242\,f \tag{4-24}$$

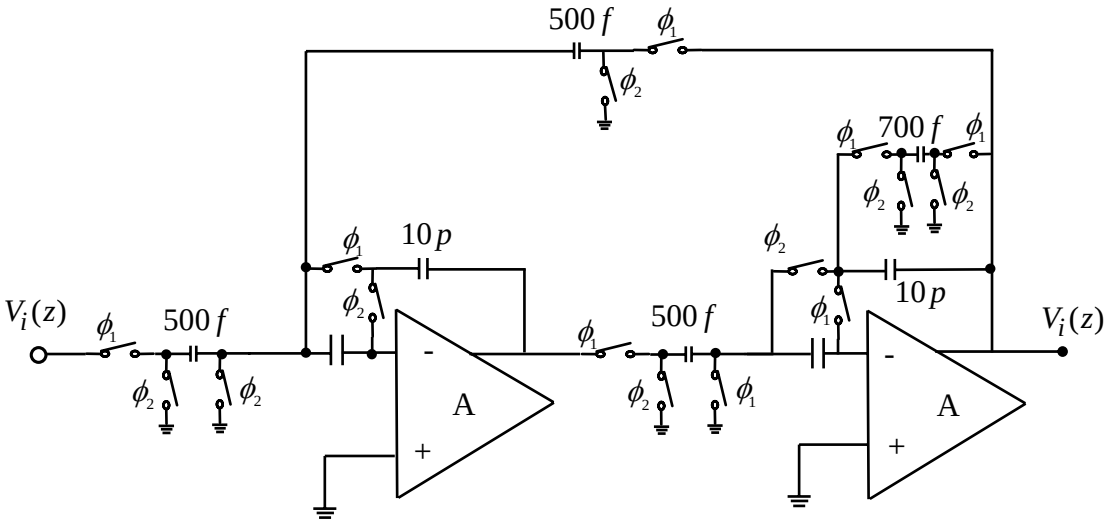


Figure 4.9 The architecture of the low pass filter

In Figure 4.9 the architecture is shown. Its clock signal is 6.4k hertz. This architecture

is implemented with correlated double sampling. Its purpose is to cancel the offset voltage.

4.4.4 The Linearity of the Amplifier

The amplifier in weak inversion is some drawbacks. First, the linearity of the amplifier is bad. Second, the gain is not high enough. Therefore, some circuit techniques are introduced [27]. Because the transconductance is proportional to the current, the linearity is not enough than the circuit in saturation region. Therefore input range is very small. In Figure 4.10 shows the improvement amplifier.

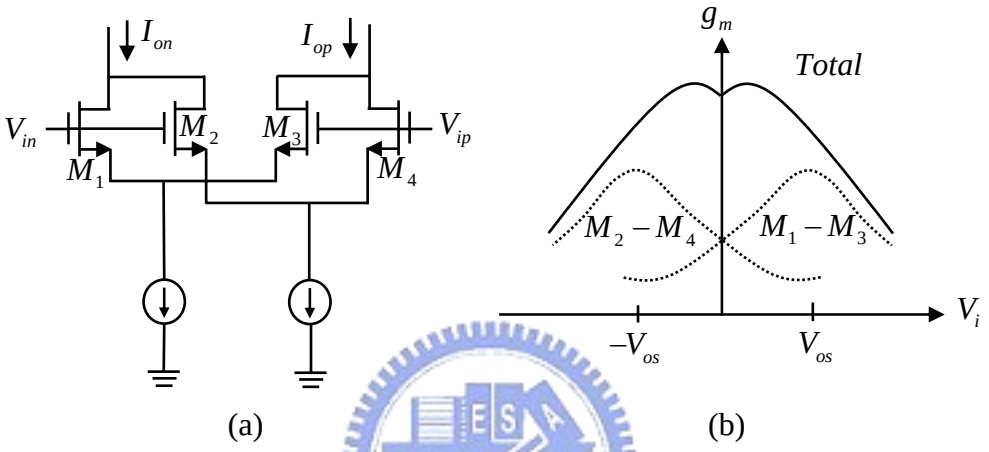


Figure 4.10 (a) the linearity circuit, (b) transconductance

In Figure 4.10, the center of the transconductance is removed to V_{os}. The input range increase in linearity . The V_{os} is

$$V_{os} = V_{be1} - V_{be3} = \frac{kT}{q} \ln \frac{I_{s1}}{I_{s2}} . \tag{4-25}$$

According to the Equation (4-25), we can design the size of the input pair. Due to the linearity, the output voltage can not achieve large. Otherwise, the signal is aliasing.

Another drawback is the gain is not high enough. Therefore, Figure 4.11 shows the technique to enhance the gain [18]. The main characteristic of the circuit is to increase branch in the current (I_9 and I_{10}). Using the bigger ratio (I_5 to I_3) is to increase the gain. If the I_9 is half of the I_1, the current mirror gain is:

$$gain = g_{m1} \cdot r_{out3} \cdot g_{m5} \cdot (r_{out5} // r_{out7}) = g_{m1} \cdot \frac{2}{g_{m3}} \cdot g_{m5} \cdot (r_{out5} // r_{out7})$$

$$= 2 \cdot g_{m1} \cdot (r_{out5} // r_{out7}) . \tag{4-26}$$

According to the Equation (4-26) the gain is increase due to the branch.

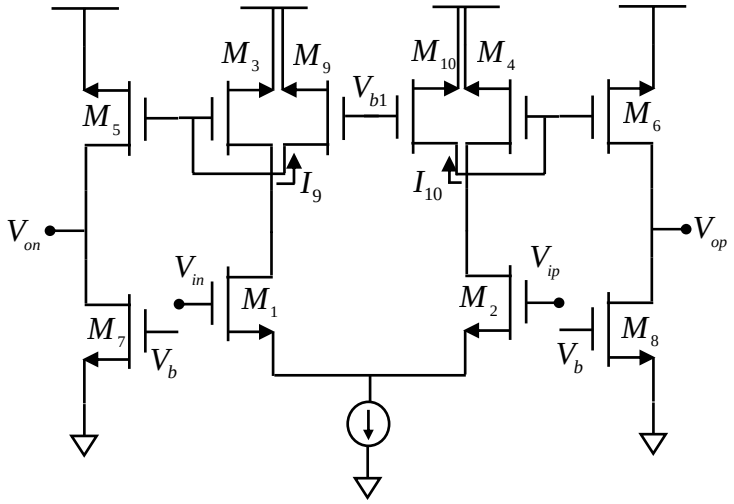


Figure 4.11 The improvement gain circuit

4.5 Post Amplifier

The gain of the first stage is 40db, so the post amplifier is needed [28]. The charge transfer amplifier is used. During ϕ_1, the signal stores the charge on the capacitor C_1. Then next clock is on, the charge on C_1 transfers to the capacitor C_2. According to the capacitor ratio, the signal is amplified [16].

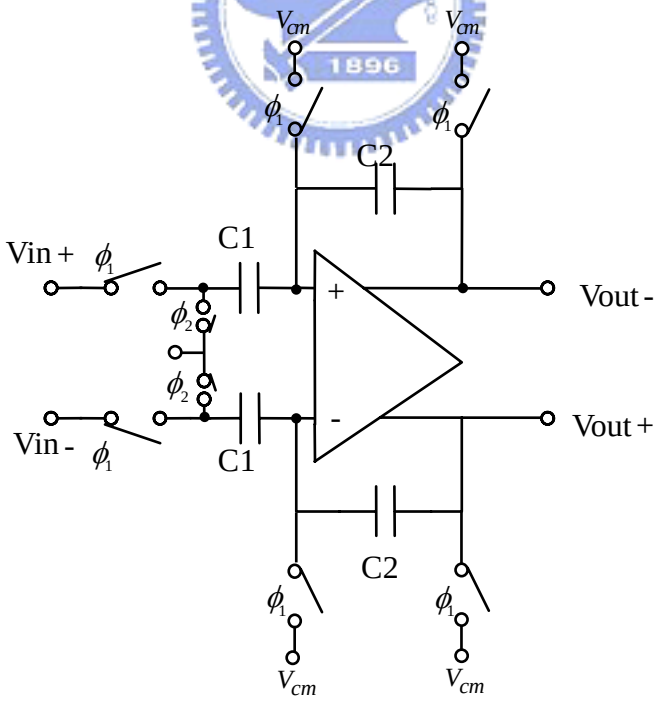


Figure 4.12 The post amplifier

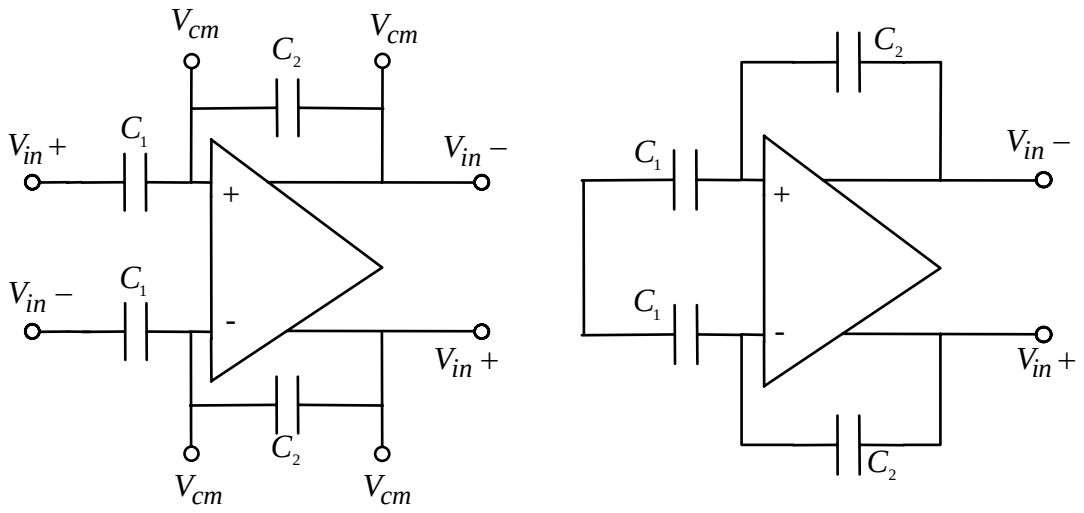


Figure 4.13 Behavior (a) ϕ_1 ,(b) ϕ_2

Figure 4.12 shows the architecture of the post-amplifier. Figure4.13 shows the behavior during clock ϕ_1 and ϕ_2. Because the resistor of the MOS transistor in weak inversion is very large, the capacitor is suitable than resistor feedback.

Another issue is noise in the closed loop amplifier. In Section 4.4.3 the noise is introduced. The main noise source is focused on capacitor C_1. Therefore, there are two noise sources in closed loop amplifier. One is thermal noise on amplifier, the other is switch sampling noise. The noise is

$$\overline{V^2_{c1,sw}} = V^2_{c1,op} + V^2_{c1,sw} = \frac{kT}{C_1}\left(1+\frac{x}{1+x}\right). \quad (4\text{-}27)$$

Where $x = 2R_{on}g_{m1}$. The noise is approximately $\frac{2kT}{C_1}$. According to the Equation (4-27) and the magnitude of the signal is 0.25v, the capacitor C_1 must be large than 200f.

4.6 Clock Generator

Figure 4.22 shows the clock generator in the system. The clock signal is made up of the NOR gate and inverter chain. The clock ϕ_1 and ϕ_2 are non-overlapping signal. The clock signal is delay through the inverter chain and NOR gate. According to the delay time, the inverter and NOR gate is designed. The clock ϕ_{1a} and ϕ_{2a} are slightly advance than the clock ϕ_1 and ϕ_2. The external noise can be separated by DFF. The clock signal is used in low supply voltage. Therefore, the clock boosted

driver must be used to increase the higher voltage. In Chapter 3 Figure 3.17 and Figure 3.18 is implemented in clock boosted.

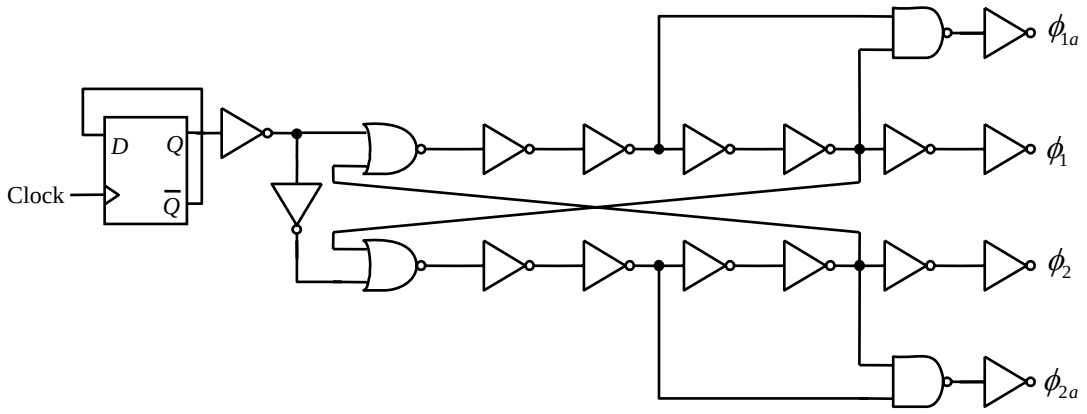


Figure 4.14 The clock generator

4.7 Simulation Result and Circuit

The blocks of the architecture are introduced above sections. According to noise corner, the clock signal is 6.4k hz. In order to design the low-power system, the preamplifier is 40db. Considering the swing of the weak inversion circuit, the post-amplifier is 20db. Next, the total circuit and simulation result are illustrated.

The MOS transistor in weak inversion is sensitive to the temperature. Therefore, in Figure4.23, the bias circuit is shown. The temperature coefficient of the PTAT circuit is positive, and the temperature coefficient of the V_{BE} is negative. So the current I_d is insensitive to the temperature.

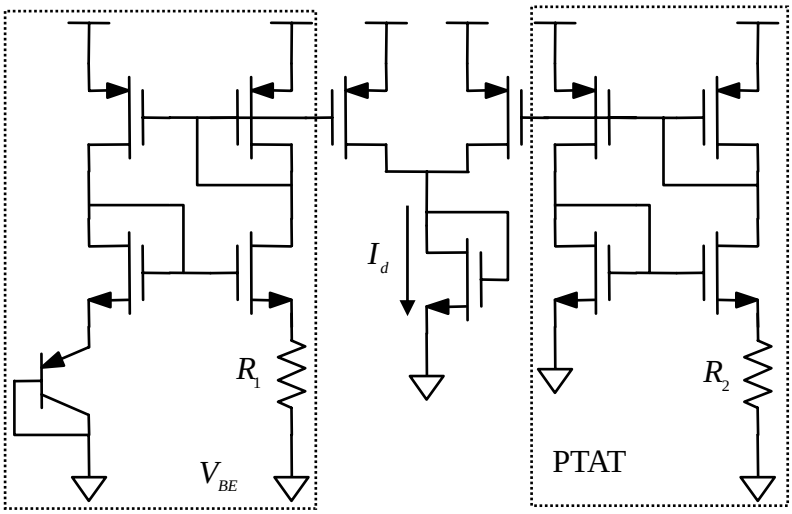


Figure 4.15 Bias circuit

The chopper amplifier uses the linear telescopic amplifier. The linear amplifier is introduced in Section 4.3. In this thesis, the gain of the chopper amplifier is 40db.

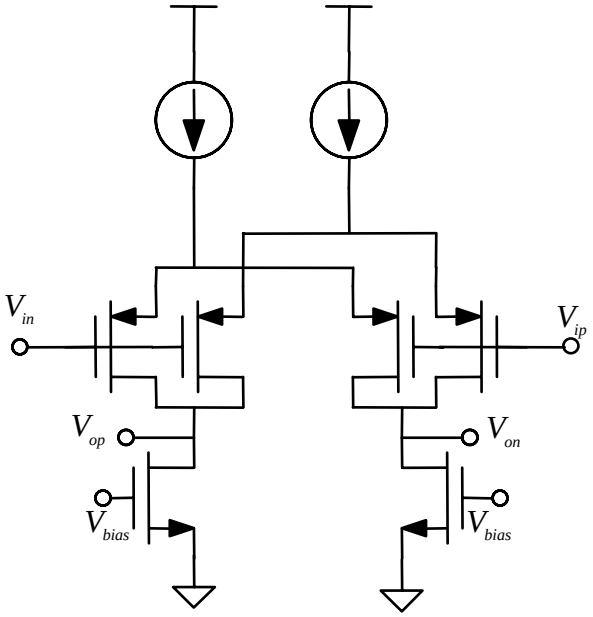


Figure 4.16 The chopper amplifier

Figure 4.25 shows the CMFB. The form of the CMFB is discrete-time. During ϕ_1 the charge samples on capacitor C_1, then during ϕ_2, the charge on capacitor C_1 transfer to the capacitor C_2. Therefore, the common mode feedback voltage is locked [25].

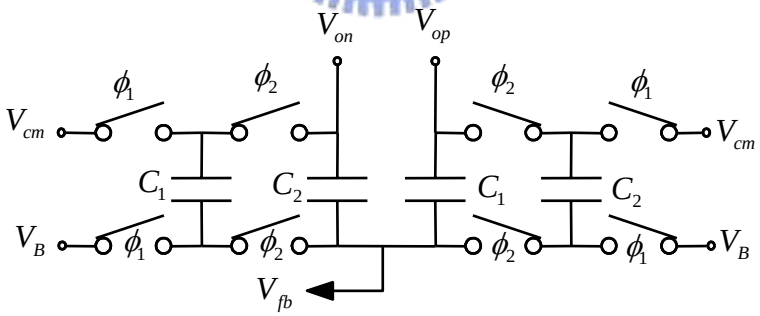


Figure 4.17 CMFB circuit

Figure 4.26 shows the current mirror amplifier. This amplifier is used in the switched capacitor circuit. The gain of the current-mirror amplifier is higher than the telescopic amplifier. The reason is introduced in Section 4.3. In the switch capacitor circuit, the amplifier is usually over 60db. The linearity is needed in the system. Therefore, the developed circuit shows as Figure 4.26.

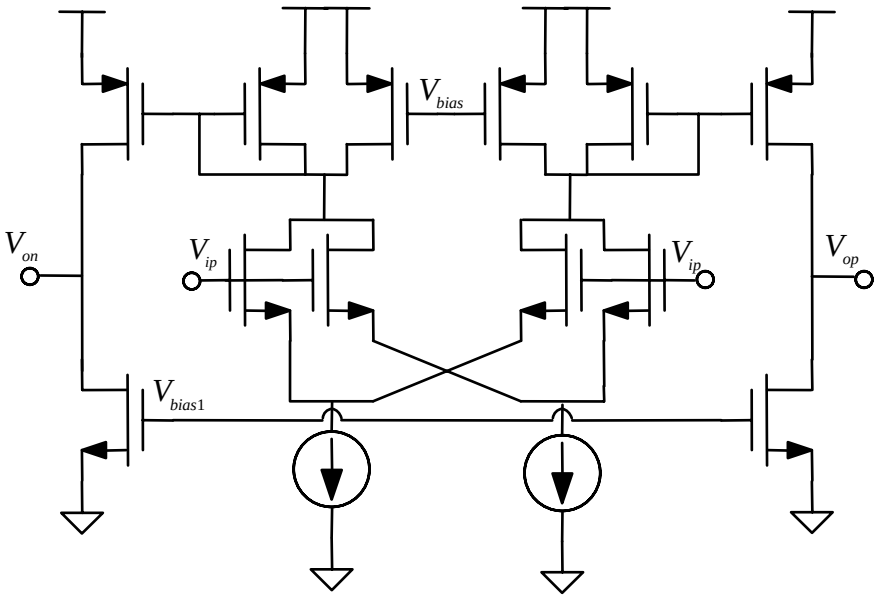


Figure 4.18 The current mirror amplifier

Figure 4.27 shows the signal of the architecture. Figure 4.28(a) shows the signal from the chopper amplifier. Its value is 0.6v .Figure 4.28 (b) shows the signal from filter. Figure 4.28 (c) shows the signal from post-amplifier.

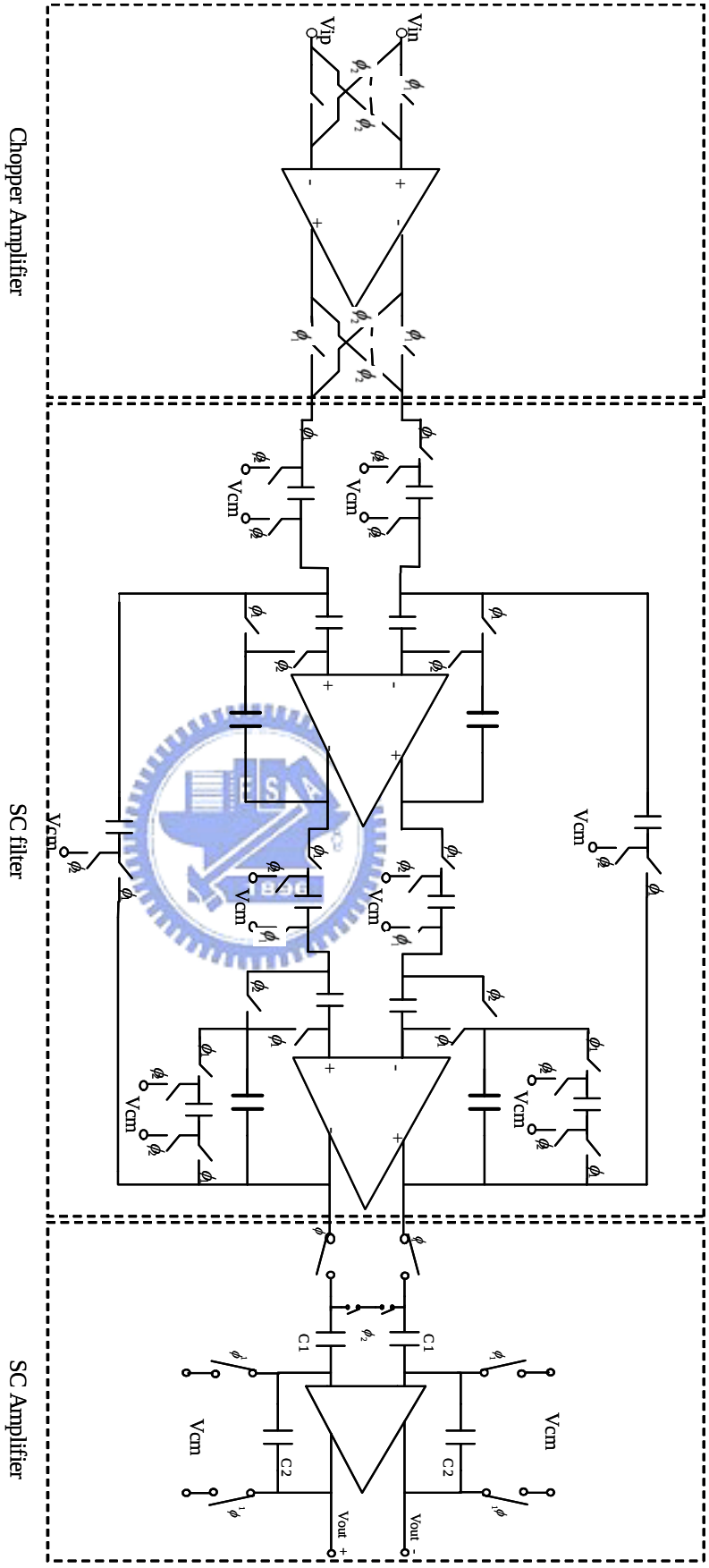
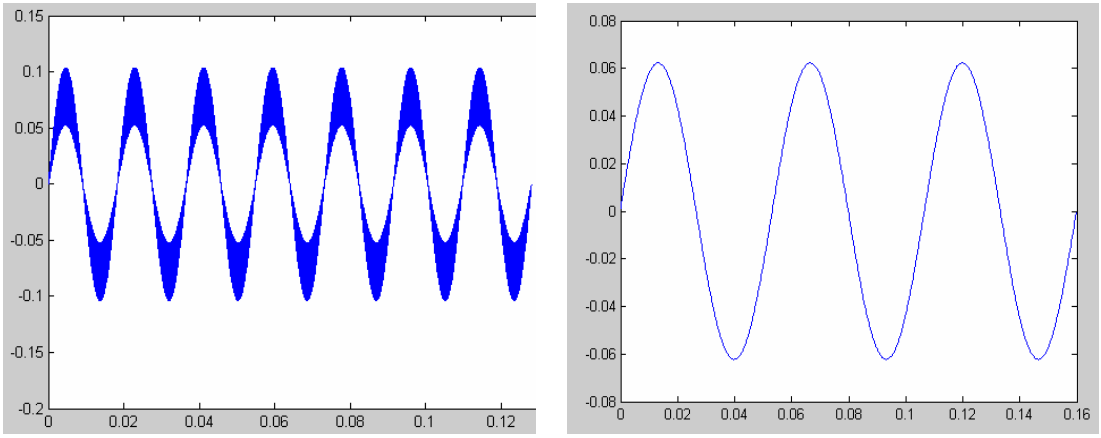
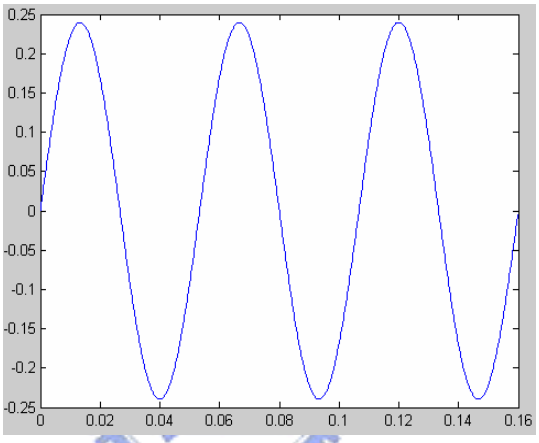


Figure 4.19 The front-end circuit of the thermopile sensor



(a) (b)



(c)

Figure 4.20 The signal output (a) the chopper amplifier, (b) filter ,(c)post-amplifier

The Table 6 shows the specification of the chopper amplifier. The input referred noise is $49nV/\sqrt{Hz}$.

gain	40db
PM	88
PSRR(10k)	46db
CMRR(10k)	86db
Input referred noise(6.4k)	$49\,nV/\sqrt{Hz}$
Power consumption	2.43uW

Table 5 The specification of the chopper amplifier

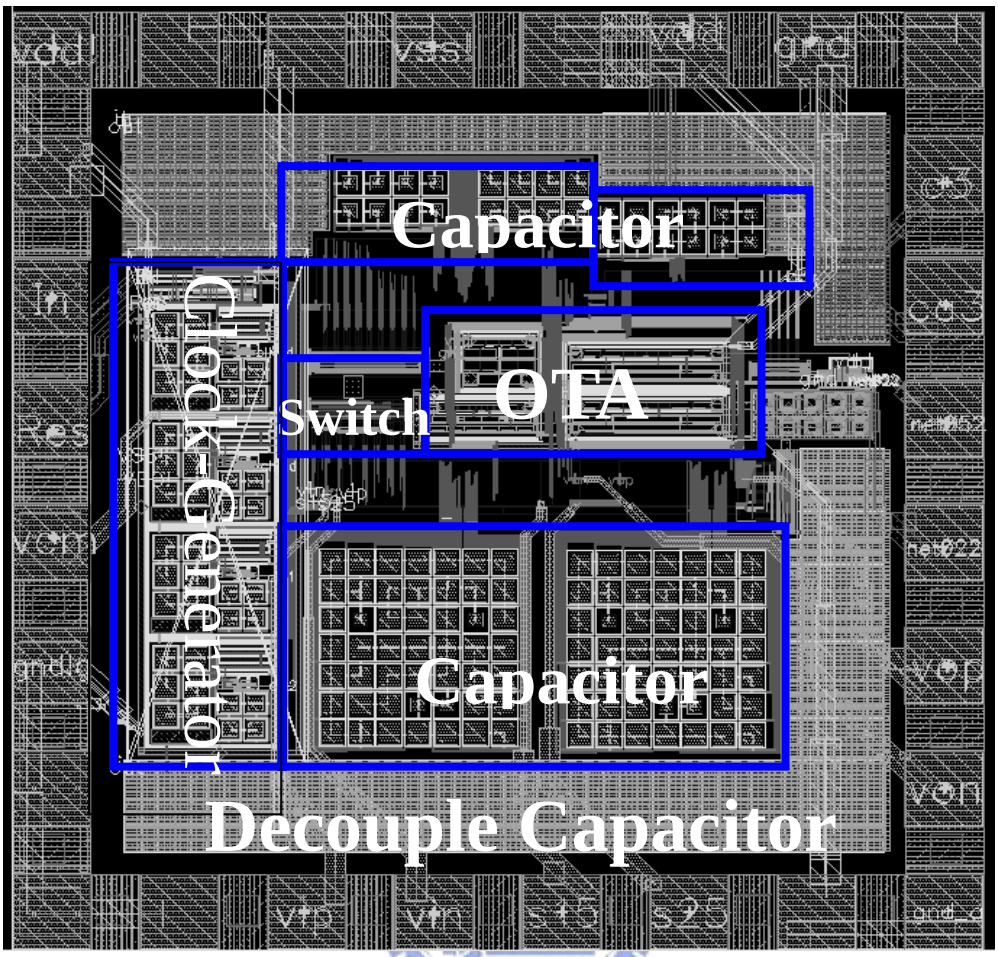


Figure 4.21 The layout of the front-end circuit for temperature sensor

Chapter 5

Conclusions

5.1 The Figure-Of-Merit (FOM)

In order to make a fair comparison, the noise efficient factor (NEF) and figure of merit are introduced in Section 4.3. The noise efficient factor is a criterion in chopper amplifier. The noise efficient is presented in Equation 4.11.It is relative with the total current, signal bandwidth, and noise root mean square value. It is

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{total}}{\pi \cdot V_T \cdot 4kT \cdot BW}}. \tag{4-11}$$

However, the noise efficient is not relative with the total area. Therefore, the figure of merit is introduced following the noise efficient factor. The figure of merit about the chopper amplifier is

$$FOM = \frac{1}{N \times S \times P}. \tag{4-12}$$

The figure of merit is relative with noise, power and area. It provides another criterion to distinguish the chopper amplifier. The Table6 shows the coefficient to distinguish the chopper amplifier.

Name & Year	V_{DD}	BW	Input Noise	NEF	Power	Process
Hammel,2005[3]	1.8v	4k	$7\,nV/\sqrt{Hz}$	3.19	242 μ W	0.18 μ m CMOS
Yoshida,2005[8]	1v	100k	$50\,nV/\sqrt{Hz}$	42	500 μ W	0.18 μ m CMOS
Mustafa, 2004 [9]	5v	1k	$16\,nV/\sqrt{Hz}$	7.4	750 μ W	1.6 μ m CMOS
Uranga,2004 [10]	5v	3k	$6.6\,nV/\sqrt{Hz}$	5.3	1.3mW	0.7 μ m CMOS
Hammel,2003[6]	3v	10k	$4.8\,nV/\sqrt{Hz}$	1.84	275 μ W	0.5 μ m CMOS
Yamu,2002[16]	1.8v	4.5k	$56\,nV/\sqrt{Hz}$	44	775 μ W	0.18 μ m CMOS
Bakker,2000[2]	5v	2k	$27\,nV/\sqrt{Hz}$	14	1mW	1.6 μ m CMOS
This Work	**0.9V**	**50**	**50** $nV/\sqrt{Hz}$	**4.7**	**5.6 μ W**	**0.18 μ m CMOS**

Table 6 The efficient factor for the front-end circuit

Name & Year	V_{DD}	BW	Power	Area	Process	FOM
Hammel,2005[3]	1.8v	4k	242 μ W	1.4 mm^2	0.18 μ m CMOS	81
Yoshida,2005[8]	1v	100k	500 μ W	0.88 mm^2	0.18 μ m CMOS	45
Mustafa, 2004 [9]	5v	1k	750 μ W	---	1.6 μ m CMOS	---
Uranga,2004 [10]	5v	3k	1.3mW	2.7 mm^2	0.7 μ m CMOS	43
Hammel,2003[6]	3v	10k	275 μ W	---	0.5 μ m CMOS	---
Yamu,2002[16]	1.8v	4.5k	775 μ W	0.52 mm^2	0.35 μ m CMOS	44
Bakker,2000[2]	5v	2k	1mW	6 mm^2	1.6 μ m CMOS	6.17
This Work	**1.8**	**50**	**5.6 μ W**	0.684 mm^2	**0.18 μ m CMOS**	**5414**

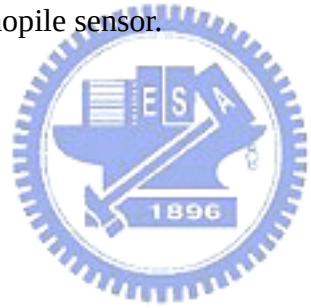
Table 7 The FOM comparison.

5.2 Conclusions

The front-end circuit of the thermopile is implemented in this thesis. The chopper

amplifier removes the offset voltage and low frequency noise to improve the SNR. The low pass filter sets the bandwidth of the total system. In order to achieve low-power low-voltage, the amplifier working in weak inversion is practiced. The offset cancellation technologies are fitted out in switched-capacitor filter. The total system is implemented in discrete time form. The clock signal is 6.4k, and the signal bandwidth is 50 hz under 0.9 supply voltage. Because the amplifier working in weak inversion, the total power consumption is approximately 5.6 μV in this thesis. From the simulation result, the fundamental signal component to the largest distortion component is over 60db. Therefore, the noise dominates the denominator of the signal to noise plus distortion ratio (SNDR). For achieving 8-bit resolution, the noise is only considered under this condition.

However, there are problems in this architecture. Although the amplifier working in weak inversion decreases power consumption, the total area increases. The area is a big problem in weak inversion. Therefore, area and power consumption are tradeoff in designing circuit. Moreover, the low-power front-end circuit extends the battery life. The battery is used efficiently in thermopile sensor.



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