國 立 交 通 大 學

電信工程學系

碩 士 論 文

2.45-GHz 低電壓(0.7V)低功率摺疊切換式混頻器

Design of Low-Voltage (0.7V) Low-Power Folded-Switching Mixer for 2.45-GHz Applications

研究生：賴宏斌

指導教授：周復芳　博士

中 華 民 國 九 十 五 年 六 月

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摘　　要

由於無線通訊市場的蓬勃發展，以及 CMOS 製程技術的快速提升，使得傳統上利用 GaAs 或 SiGe 製程來設計的射頻積體電路也能夠在 CMOS 的製程下實現。此一進步使得無線接收機的射頻前端電路能夠跟基頻電路整合成單一晶片，大大地減少了電路面積以及成本。但是由於隨著製程進步持續降低的供應電壓使得射頻積體電路很難滿足接收機的訊號動態範圍，因此需要研究新的架構使得射頻前端電路能夠操作在低於 1V 的供應電壓環境下，如此才能更進一步的跟基頻電路整合。

因此我們使用一個新型的摺疊切換式混頻器，藉由它能操作在低於 1V的供應電壓下，將此混頻器應用在低電壓低中頻接收機架構中。此混頻器可以提供 8.99dB的轉換電壓增益，以及良好的線性度(P1dB=-9dBm，IIP3=4dBm)，消耗功率為 2.87mW，晶片面積為 1.24 × 1.19 mm^2。本論文中的晶片使用標準的 0.18-μm CMOS製程設計和實作，並且在國家晶片系統設計中心完成量測。

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ABSTRACT

Wireless and mobile communications is one of the fast growing microelectronics applications. Traditionally, the RFICs are implemented in GaAs or SiGe process. With the progress of scaled down CMOS technology, RFICs can be implemented in CMOS process and provide high integration and low cost. Under reduced supply voltages, many circuit topologies of the RF front-end can not meet the stringent dynamic range of wireless receiver. It needs more efforts toward finding out new topology suitable to operate at sub-1V supply voltage.

In this thesis, we analyze the design of low-voltage folded-switching mixer and employee it to the proposed low-IF receiver RF front-end. The new mixer has high voltage gain (8.99dB), moderate noise figure (10.3dB in simulation), moderate linearity (P1dB = -9dBm, IIP3 = 4dBm), and low power consumption (2.87mW). The total chip size is 1.24×1.19 mm^2. This chip is designed and implemented in CMOS 0.18-μm 1P6M technology and measured in National Chip Implementation Center (CIC).

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Chapter 1

Introduction

1.1 Background and Motivation

Wireless and mobile communication is one of the fastest growing microelectronics applications and has an enormous impact in our daily lives. On the hardware frontier, there are persistent demands for low cost, low power consumption and high performance for portable and hand-held terminals. This incited rapid evolution of highly integrated radio frequency (RF) receivers within CMOS technology [1]-[5].

Traditionally, radio frequency integrated circuits (RFICs) were implemented in GaAs or SiGe bipolar technologies, because of their relatively high unity gain cutoff frequencies and superior noise performances. However, CMOS technology scaling continues to improve the f_T of the transistors to the point where it is becoming comparable to those of GaAs and SiGe processes. Contemporaneous with this evolution is the reduction in supply voltage implies that the RF front-end of wireless system will have to operate with low-voltage supplies (ie. $\leqq$ 1V). Under reduced supply voltage, many of the circuit topologies commonly used in RF receivers, such as cascoded low noise amplifiers [6] and Gilbert mixers [7], [8], will not meet the stringent dynamic range requirements of the receiver. These circuits require at least

two transistors stacked between the supply rails, making them unsuitable for low-voltage operation.

The most widely used RF receiver architecture is heterodyne receiver where the RF front-end converts the RF signal to a high intermediate frequency signal (IF) which is up to several tens or hundreds of MHz. This type of architectures requires off-chip image-reject filters which are bulky and often made of discrete components. Recently, as the demand for higher integration increases, the low-IF architecture which converts the RF signal to tens of KHz or a few of MHz IF signal has gained more popularity, due to its ease of integration. Therefore, no image reject filter is required after the first amplification stage, and the LNA does not to drive off-chip high quality filters.

Fig. 1-1 shows the complete proposed RF front-end architecture for low-IF receiver.

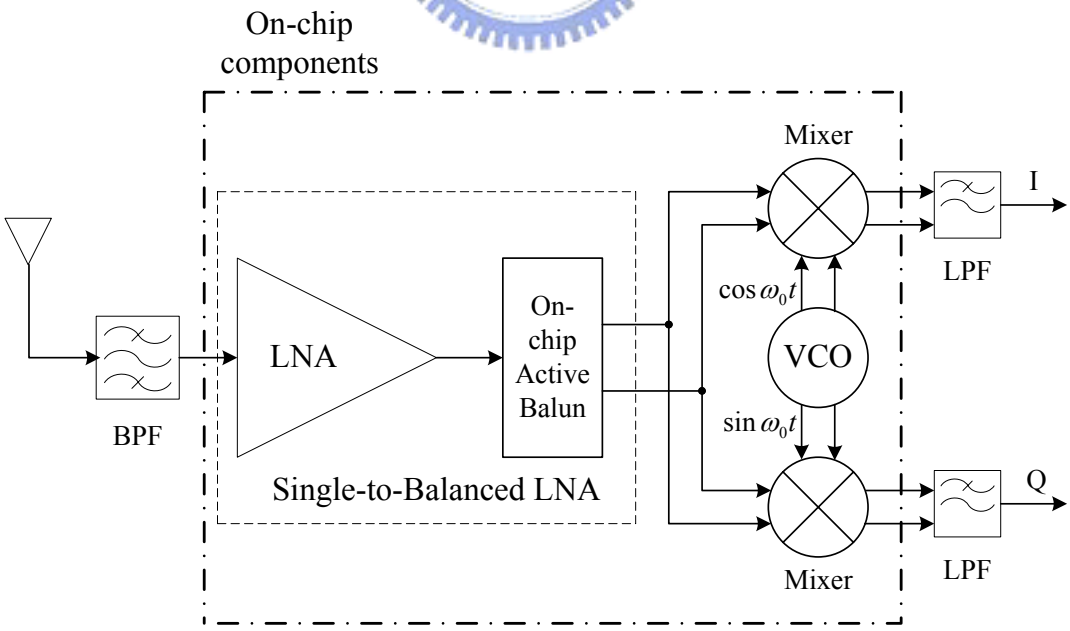


Fig. 1-1 Proposed architecture of the low-IF receiver RF front-end

In circuit design, a balanced architecture is preferred to an unbalanced one owing

to its higher insensitivity to common mode substrate noise and other noise sources. However, since an incoming RF signal is an unbalanced one, it is often desirable to split this into two differential signals opposite in phase and equal in amplitude and this is typically done by a narrow-band off-chip passive balun. For demand of higher integration, it is unsuitable to use the passive balun. So we propose an on-chip active balun as an intermediate stage between the single-ended LNA and the double-balanced mixer as a solution of a fully-integrated low-voltage RF receiver front-end in CMOS 0.18-μm technology. Following we will discuss the design of low-voltage folded-switching mixer as shown in Fig. 1-2 in the chapter 2 and the design of low-voltage single-to-balanced LNA as shown in Fig. 1-3 will be introduced in the Appendix.

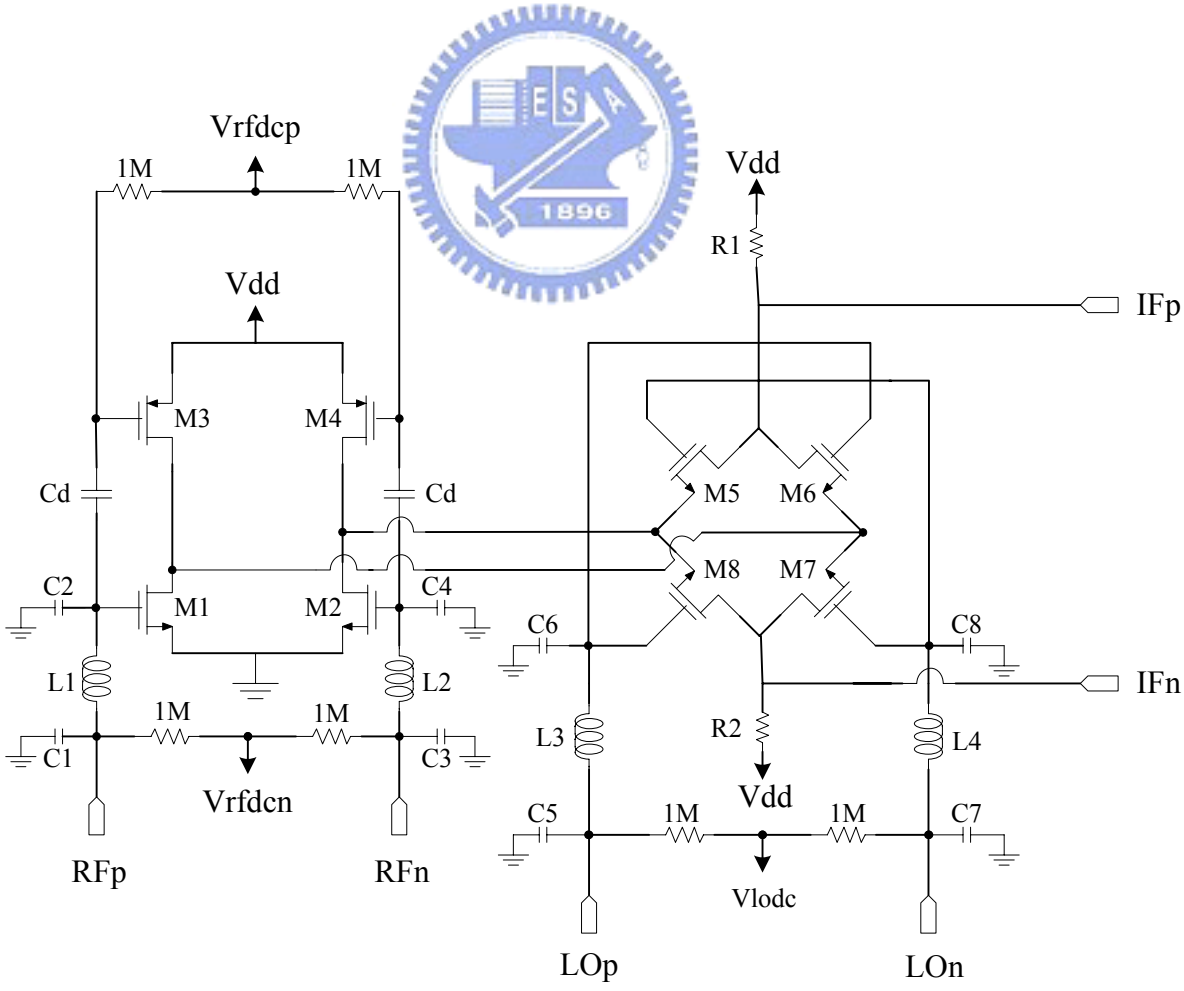


Fig. 1-2 Schematic of low-voltage folded-switching mixer

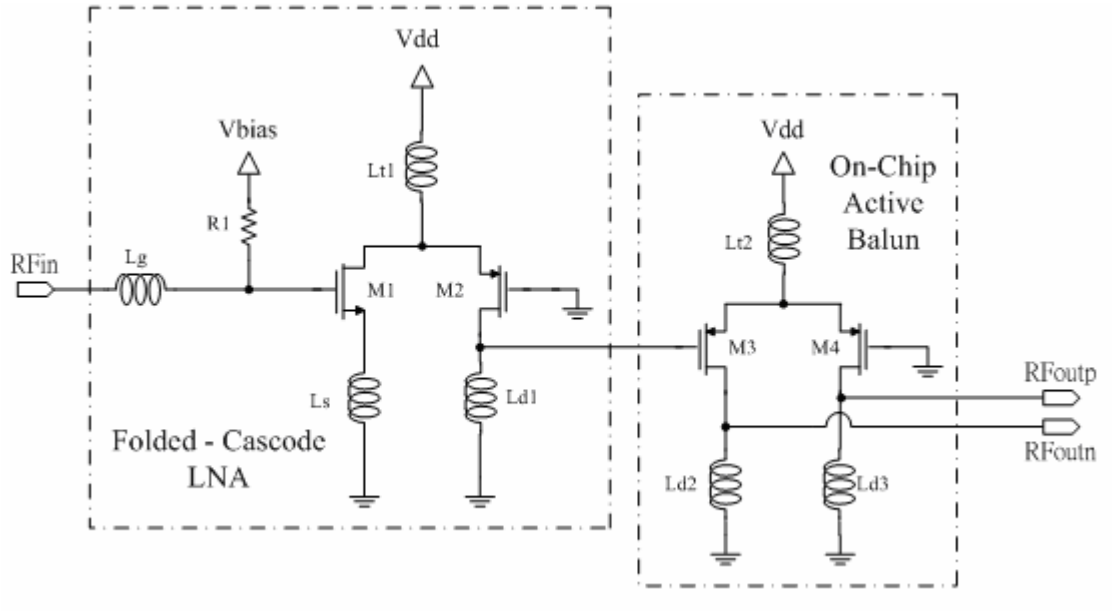


Fig. 1-3 Schematic of low-voltage single-to-balanced LNA

1.2 Thesis Organization

This thesis contains two building blocks of low voltage low-IF receiver RF front-end. One is the 0.7V 2.45-GHz single-to-balanced LNA and the other is 0.7V 2.45-GHz folded-switching mixer. We will present the design flows and characteristic analyses of these two circuits.

In Chapter 2, we will introduce the design of low-voltage folded-switching mixer including the analyses of conversion voltage gain, noise figure, linearity, and DC stability. A basic review of single-balanced and double-balanced mixer architecture is also presented in this chapter. At last, the simulation and experimental results and their comparisons are presented.

In Chapter 3, a simple conclusion about this work is made and future works are discussed.

In Chapter 4, we will describe the design of low-voltage single-to-balanced LNA and show the simulation results as an appendix. Also, we will present the analyses of input matching, noise figure, and power consumption in terms of circuit component

parameters.

Chapter 2

Low-Voltage (0.7V)

Folded-Switching Mixer

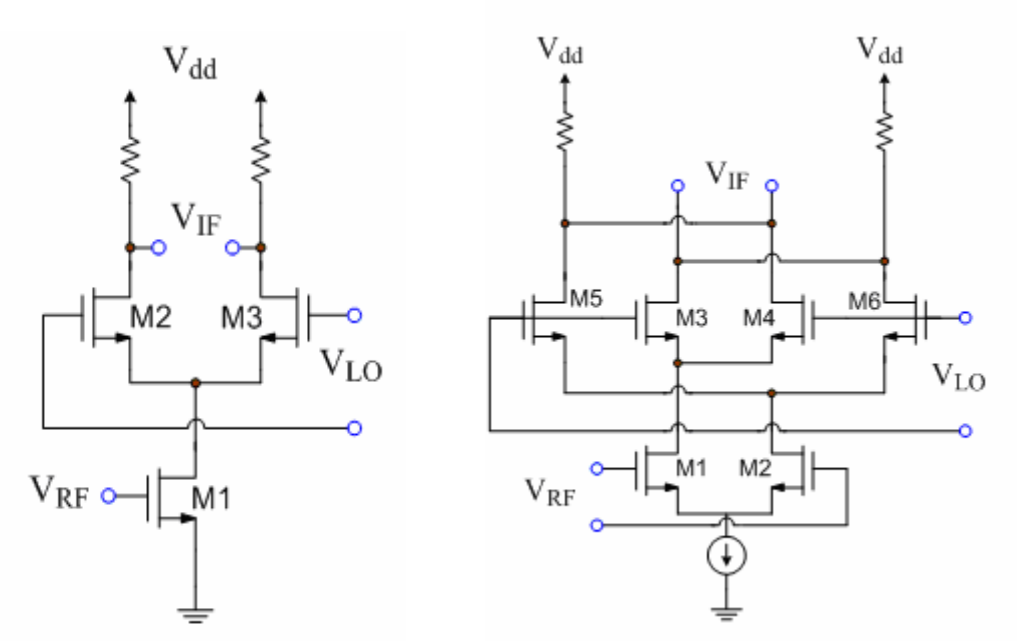
2.1 Review of the Basic Mixer

Mixers employed in the receiver path perform frequency translation to a lower frequency for further processing by multiplying two signals in the time domain. Since linear, time-invariant systems cannot produce outputs with spectral components not present at the input, mixers must be either nonlinear or time-varying elements in order to provide frequency translation.

Mixers based directly on multiplication, such as Gilbert cell mixers [7], [8], generally have superior performance because they ideally produce only the desired intermodulation product. Furthermore, since the inputs to a multiplier enter at separate ports, higher port-to-port isolation can be achieved among all three ports (RF, LO, and IF). In this type, the output current of mixer can be expressed as：

$$i_{out} = \text{sgn}\left[\cos \omega_{LO} t\right]\left\{I_{BIAS} + I_{RF} \cos \omega_{RF} t\right\} \qquad (2.1)$$

The output thus consists of sum and difference components, each the result of an odd harmonic of the LO signal mixing with the RF signal. Fig. 2-1 shows two types of mixers based on the multiplication.



(a) (b)

Fig. 2-1(a) Single-balanced mixer (b) Double-balanced mixer

The single-balanced topology as shown in Fig. 2-1(a) has less input-referred noise for a given power consumption than the double-balanced counterpart. However, this circuit is more susceptible to noise in the LO signal. In addition, odd harmonics of the LO appear directly in the output as a consequence of the DC bias current multiplying with the LO signal, which is known of the LO-IF feedthrough. On the other hand, the double-balanced mixer as shown in Fig. 2-1(b) exploits symmetry to remove the undesired output LO component through the differential pairs M3-M4 and M5-M6 providing opposite signal phases to cancel the feedthrough from the LO to the IF and generates less even-order distortion. The double-balanced mixer also has better port-to-port isolations by the symmetry. With these advantages makes the topology be widely used in receiver architecture. However, it stacks three transistors makes the circuit unsuitable to operate at low supply voltage. There exists a demand for searching a new topology to meet the low-voltage operation, but still keeps all advantages of the double-balanced mixer.

2.2 Low-Voltage Folded-Switching Mixer Design

Typically, the low-voltage design technique uses LC-tank capacitively coupled topology, [21], to separate both the DC and AC path of a cascade circuit as shown in Fig. 2-2.

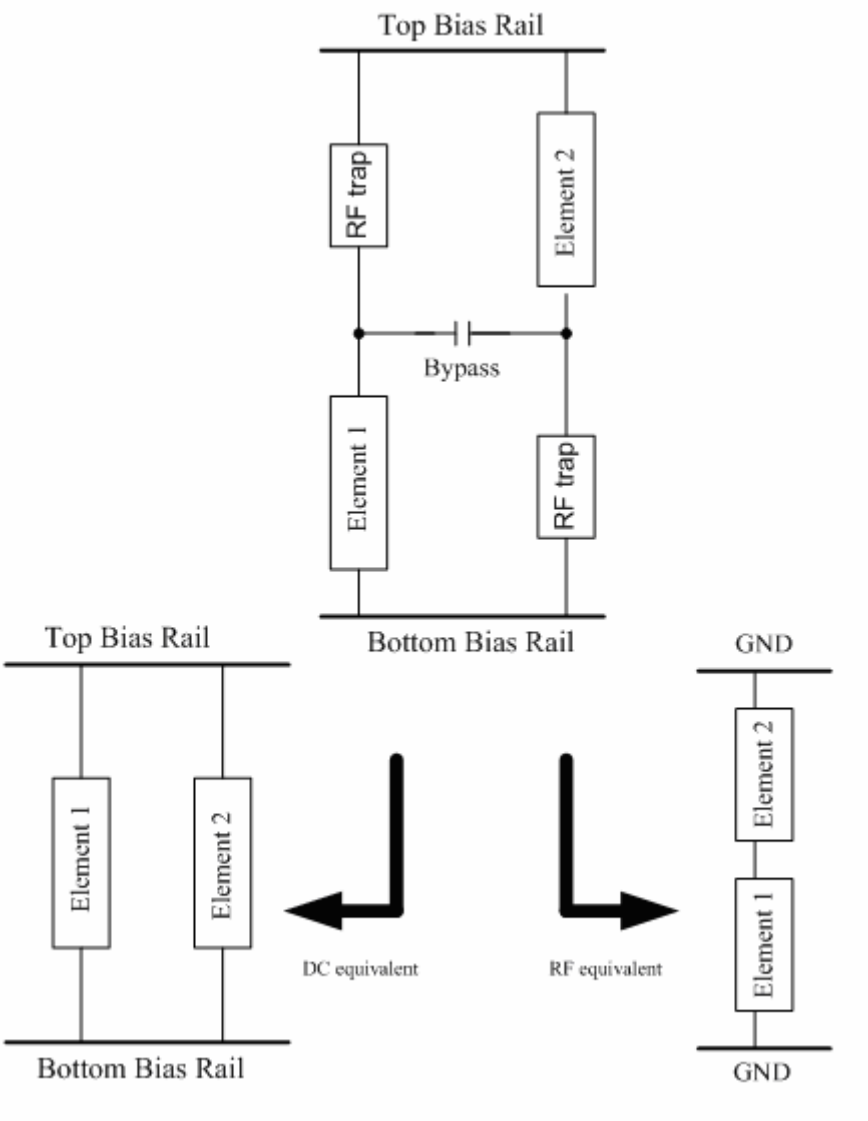
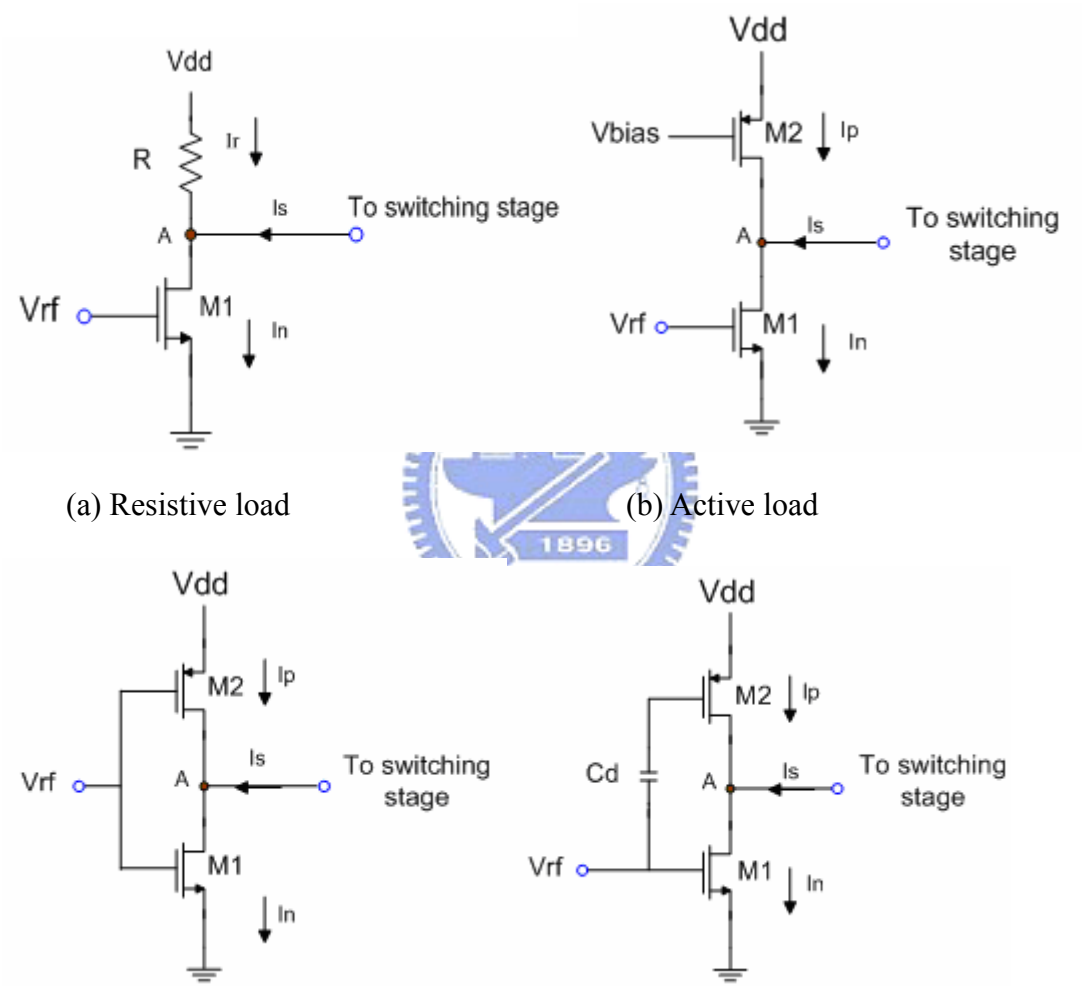


Fig. 2-2 Equivalent DC and AC signal path

Based on this topology, if we want the mixer to be differential, it needs too much on-chip inductors resulting in a large chip size, [22]. In terms of operation at low supply voltage, the goal is to reduce the voltage drops across the load resistors and the switching transistors. This can be done by designing a switching mixer in which only

a small part of dc current from the transconductor flows through the switching stage and the load resistors. Therefore, we need to change the common-source transconductors in the double-balanced mixer but remaining the switching stage as in the double-balanced mixer.

2.2.1 Transconductors for Folded-Switching Mixers



(a) Resistive load (b) Active load

(c) CMOS inverter (d) Ac-coupled CMOS inverter

Fig. 2-3 Four types of transconductors for folded-switching mixer

In the case of the doubled-balanced mixer (see Fig. 2-1(b)), the single NMOS transistor is used as the transconductor. Fig. 2-3 shows four different transconductors for application in low-voltage folded-switching mixer. Indeed, they represent

improvement of the single NMOS transconductor with respect to operation at low supply voltages.

The transconductor with resistive load is the simplest modification of the single NMOS transconductor (see Fig. 2-3(a)). The ac current I_n, which is produced in the NMOS transistor, splits to the current through the switching stage I_s and through the resistor I_r. The fact that a part of the ac current flows through the resistor R represents the drawback of this transconductor. In order to reduce I_r the value of the resistor R has to be increased. As a consequence must be taken to keep the dc voltage at the node A sufficiently high to prevent the transistor M1 entering linear region. At low supply voltage this problem is even important.

The drawback of the transconductor with resistive load can be improved by using the transconductor with active load as shown in Fig. 2-3(b). By replacing the resistor with the PMOS transistor the ac current through this transistor I_p is further reduced owing to the high output impedance of the PMOS transistor. Instead of using PMOS transistor only to increase the impedance between the node A and V_{dd}, it can be also used to amplifier the RF signals. In this way the leakage of the ac current toward the ac ground through the output impedance of the PMOS transistor can be ideally completely avoided. Therefore, a CMOS inverter as shown in Fig. 2-3(c), which is used as the transconductor, is obtained.

In the CMOS inverter, the RF signal amplificated by the PMOS transistor is a result of current reuse principle [23]. This is an efficient way to have a high gain and a low noise figure with a low power consumption. The ac current I_s is equal to the sum of the ac current I_n and I_p. Based on that the total transconductance is equal to $g_{mn} + g_{mp}$, where g_{mn} is the transconductance of transistor M1 and g_{mp} is the transconductance of transistor M2. Before going further with a detailed analysis of the folded-switching mixer that uses the CMOS inverter as the transconductor, it is

instructive to check the lowest supply voltage. It is determined by the threshold voltages V_t and by the overdrive voltages of the transistors M1 and M2. The overdrive voltages V_{ovn} of M1 and V_{ovp} can be calculated using

$$V_{ovn} = V_{rfdc} - V_t \tag{2.2}$$

$$V_{ovp} = V_{dd} - V_{rfdc} - V_t \tag{2.3}$$

V_{rfdc} is the biasing voltage applied at the gates of the transistors M1 and M2. Finally, the minimal supply voltage $V_{dd\ (min)}$, at which the mixer can operate, is expressed as

$$V_{dd(\min)} = V_{ovn} + V_{ovp} + 2V_t \tag{2.4}$$

Typical value of V_t in 0.18-μm CMOS is in the range of 500 mV. From (2.4), it is clear that the minimum supply voltage $V_{dd\ (min)}$ must be higher than 1 V. This is the disadvantage of the CMOS inverter, which is used as the transconductor in the low-voltage folded-switching mixer.

In order to overcome the described limitation, the biasing for NMOS and PMOS transistors in the CMOS inverter have to be separated. In this way we obtain an ac-coupled complementary transconductor as shown in Fig. 2-3(d). If V_{rfdcn} is the gate biasing voltage of M1 and V_{rfdcp} of M2, (2.4) becomes

$$V_{dd(\min)} = V_{ovn} + V_{ovp} + 2V_t + V_{rfdcp} - V_{rfdcn} \tag{2.5}$$

Choosing V_{rfdcn} to be greater than V_{rfdcp}, $V_{dd\ (min)}$ can be further reduced. In this work, we set V_{rfdcn} equal to 0.7 V and V_{rfdcp} to be DC ground and assume V_t is approximately 0.5 V, then the $V_{ovn} = V_{ovp} = 0.2$ V, so the $V_{dd\ (min)}$ becomes

$$V_{dd(\min)} = 0.2 + 0.2 + 2*0.5 + 0 - 0.7 = 0.7(V) \tag{2.6}$$

a minimum supply voltage using in this work. Combining the ac-coupled complementary transconductor with the switching stage and load resistors, the ac-coupled folded-switching mixer is obtained and shown in Fig. 2-4.

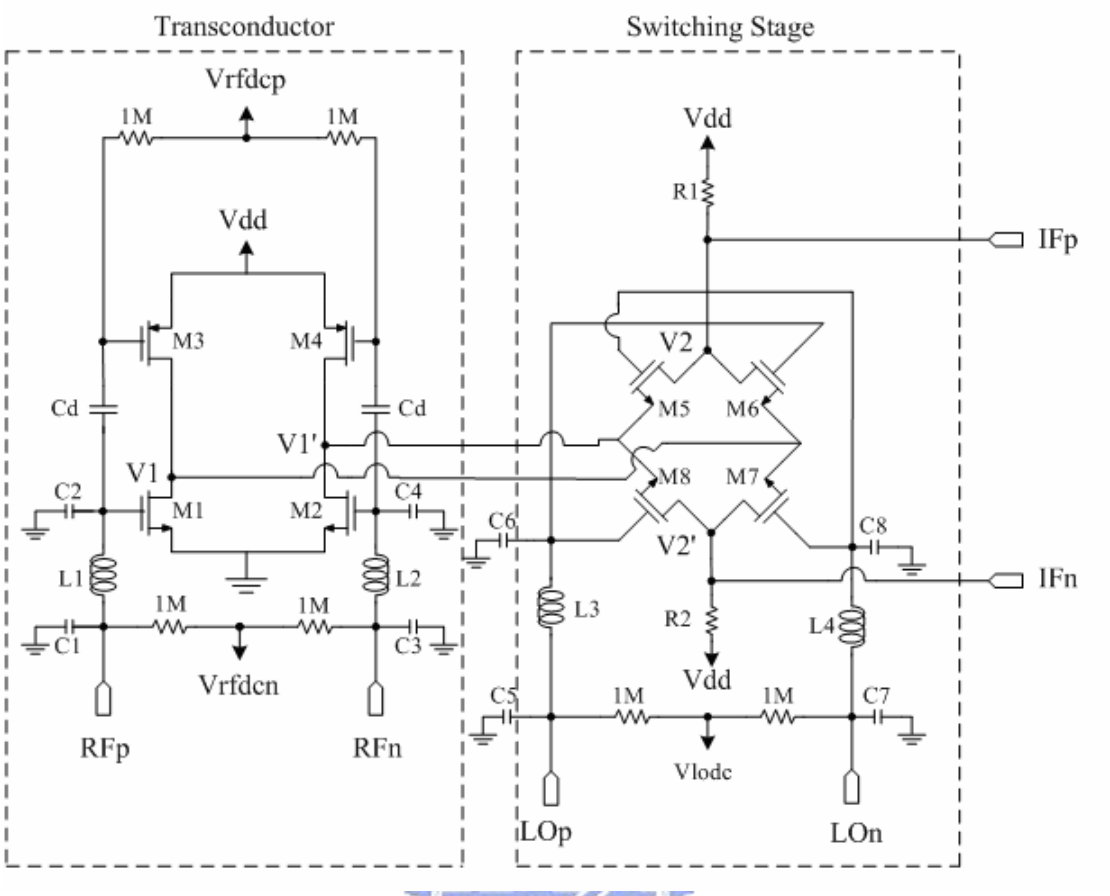


Fig. 2-4 Ac-coupled folded-switching mixer

2.2.2 Gain and Noise Figure

Assuming that LO signal is an ideal square wave, the voltage gain of the mixer shown in Fig. 2-4 can be approximated by, [25],

$$G = 20\log\left[\frac{2}{\pi}\left(g_{mn} + g_{mp}\right)R\right] \tag{2.7}$$

where g_{mn} is the transconductance of M1 and M2, g_{mp} is the transconductance of M3 and M4 and R is the load resistor. Since only a small part of the dc current from the switching stage flows through the transconductor, large load resistors can be used. Hence, the voltage gain is improved, but at the same time the switching transistors have to handle a large output signal swing. Therefore, the dc voltage V2 and V2' has to be kept sufficiently high and voltage V1 sufficiently low (see Fig. 2-4). On the

other hand, voltage V1 should be sufficiently high in order to keep the transistors M1 and M2 saturated.

The noise figure of the ac-coupled folded-switching mixer with current-reuse, under the assumption that the LO signal is ideal square wave and take into account the noise folding from the image frequency, can be approximated by, [25],

$$NF = 10\log\left(2 + \frac{4\gamma\left(g_{mn} + g_{mp}\right)}{R_s\left(g_{mn} + g_{mp}\right)^2} + \frac{\pi^2}{2RR_s\left(g_{mn} + g_{mp}\right)^2}\right) \qquad (2.8)$$

where R_s is the source resistance and the coefficient γ is equal to *2/3* for long channel transistors and need to be replaced with a larger value for submicron MOSFETs, [24],.

2.2.3 Linearity

Nonlinearity in the mixer voltage transfer function is caused by operation of the switching transistors in the linear region. The switching transistors will be turned off by the high voltage swing at the nodes V1 and V1' (see Fig. 2-4). In this case a high current pushed by the transistors M3 or M4 will cause a high voltage across the output impedance of the transistors M1 or M2 that will turn the switching transistors M7 and M6 or M8 and M5 off. Linearity manly depends on input signal dynamic range which does not make the operation of transistors in the linear region. In the folded-switching mixer with current-reuse, the linearity can be improved by decreasing the DC voltages V1 and V1', and the deviation from a linear transfer function can be reduced by keeping the switching transistors far from the linear region.

2.2.4 DC Stability

In order to design a robust ac-coupled folded-switching mixer with current-reuse that can stand at least supply voltage variations of 10%, it is necessary to calculate the variations of voltage V1 and V1' as a function of the supply voltage variations ΔV_{rfdcn}

and ΔV_{rfdcp}. Small signal analysis is applied to this calculation assuming that the variations of voltages V_{rfdcn} and V_{rfdcp} are small. Substituting the small signal model for each transistor (parallel connection of transistor output impedance and ideal current source with value $g_m V_{in}$, where g_m is the transconductance and V_{in} the small signal voltage applied at the gate) the variations of voltage V1 and V1' can be expressed as

$$\Delta V1 = -\frac{g_{mp}\Delta V_{rfdcp} + g_{mn}\Delta V_{rfdcn}}{1/R_{op} + 1/R_{on} + 2g_{ms}} \tag{2.9}$$

R_{on} and R_{op} is the output impedances of transistors M1 and M3. g_{ms} is the transconductance of the switching transistors. In the denominator of (2.9) g_{ms} dominates and reduces the variations of the voltage V1 by a larger value g_{ms}.

2.3 Layout and Measurement Consideration

Layout is an important step in optimizing a radio frequency circuit design. A poor layout could result in great degradation between expected and actual circuit's performances. The chip layout of the low-voltage folded-switching mixer is shown in Fig. 2-5 and is fabricated in TSMC 0.18-μm CMOS technology. To minimize the impacts of substrate noise on the circuit, guard rings are added to the devices and inductors, which also improve the quality factor Q of the inductor. Furthermore, traces connected to all inductors are made wide enough to minimize series parasitic resistances and inductances, and thus avoid inductor Q degradation. The RF and LO input are placed in opposite position to improve the port-to-port isolations. Since PCB on-chip testing is to measure the performances of the mixer, two shielded differential signal GSGSG pads are placed at RF and LO input respectively. In low-voltage operation, the resistances of the biasing traces have large effects on circuit's operation and performances. It may cause undesired voltage drops on the DC path and hence

reduces the voltage headroom, an important issue needed to be taken into account. Therefore, the biasing traces must be as short and wide as possible to reduce the parasitic resistance of metal lines. The total layout area of the mixer is 1.24 × 1.19 mm^2 .

The low-voltage mixer is designed for PCB on-wafer measurement so the layout must follow the rules of CIC's (Chip Implementation Center) probing testing [13]. The measurement of the mixer is PCB on-wafer so we have to take the effects of bond wires into account in the design of the mixer. The measurement needs two input differential GSGSG probes, one for RF port and the other for LO port. The output signals IFp and IFn are bonded and connected to SMA connectors for measuring. Fig. 2-5 shows the layout of low-voltage mixer. Fig. 2-6 shows the die photograph of mixer. Fig. 2-7 shows the picture of the testing board. Fig. 2-8 is the picture of PCB on-wafer measurement setup for the ac-coupled folded-switching mixer. The S-parameter measurement setup is shown in Fig. 2-9. Fig. 2-11 shows the measurement setup for noise figure. Fig. 2-11 is the setup for measuring conversion power gain and one dB compression point and the measurement setup for IIP3 is shown in Fig. 2-12.

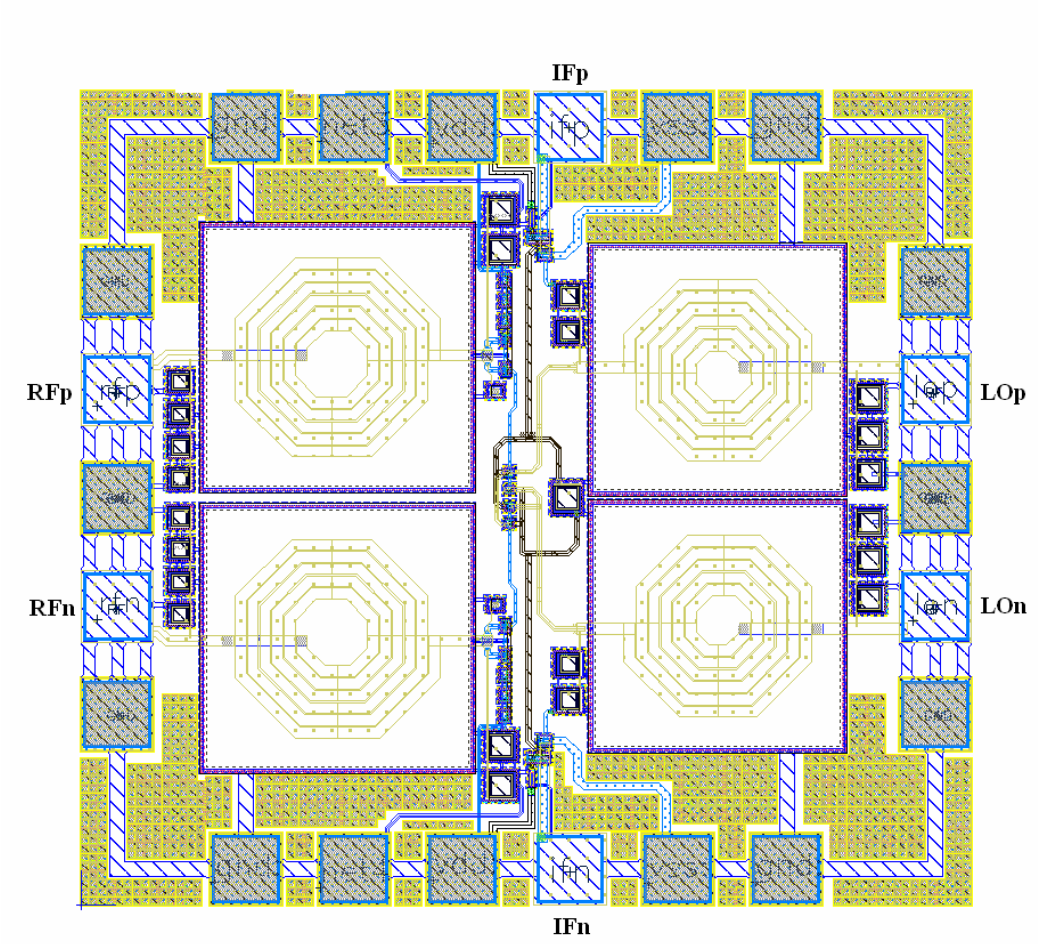


Fig. 2-5 The layout of ac-coupled folded-switching mixer

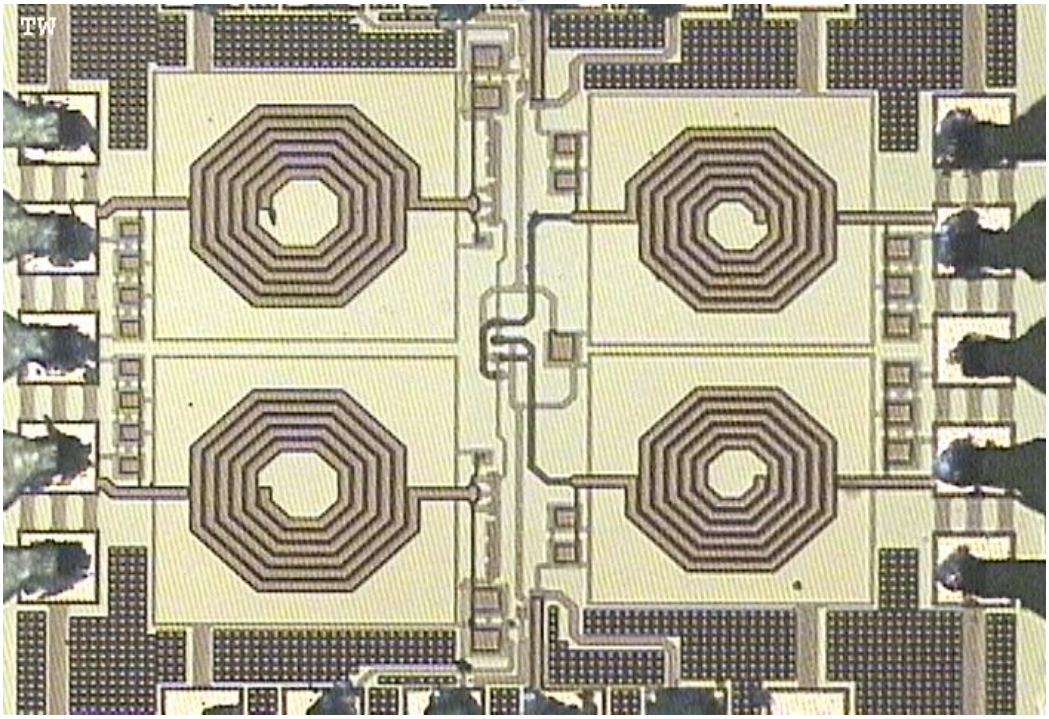


Fig. 2-6 Die photograph of low-voltage mixer

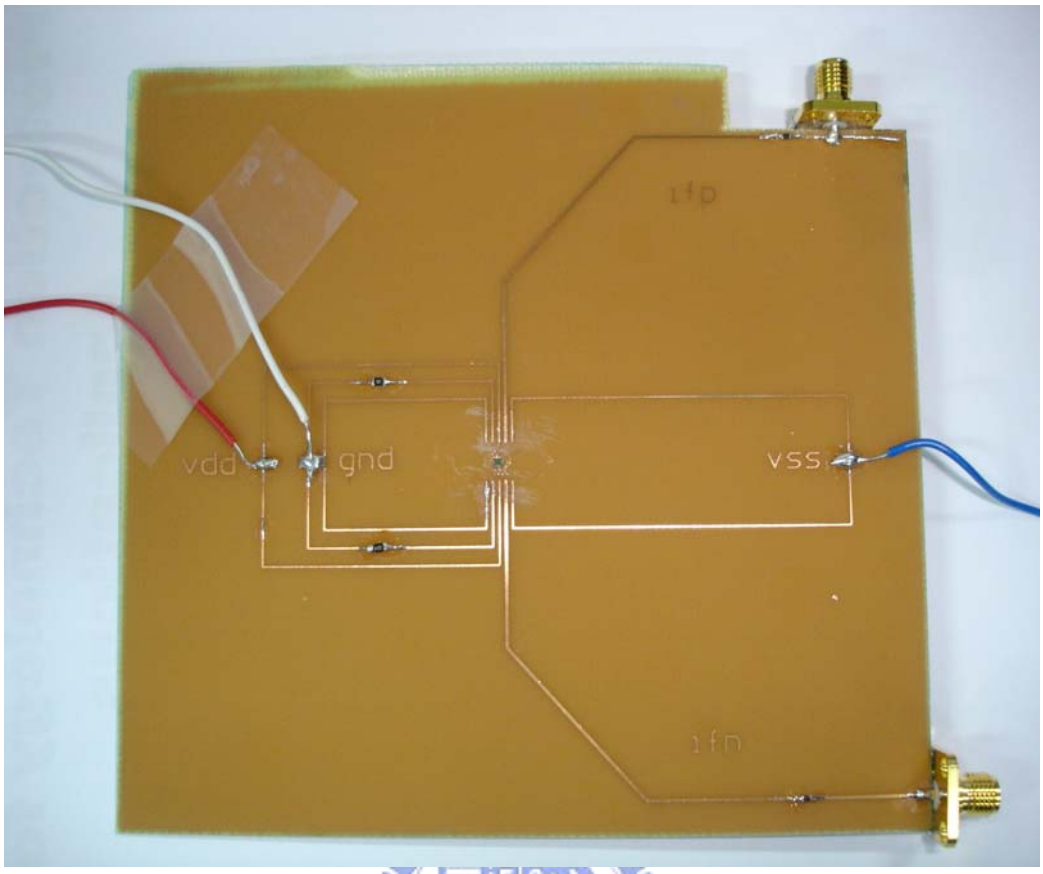


Fig. 2-7 PCB testing board picture of the mixer

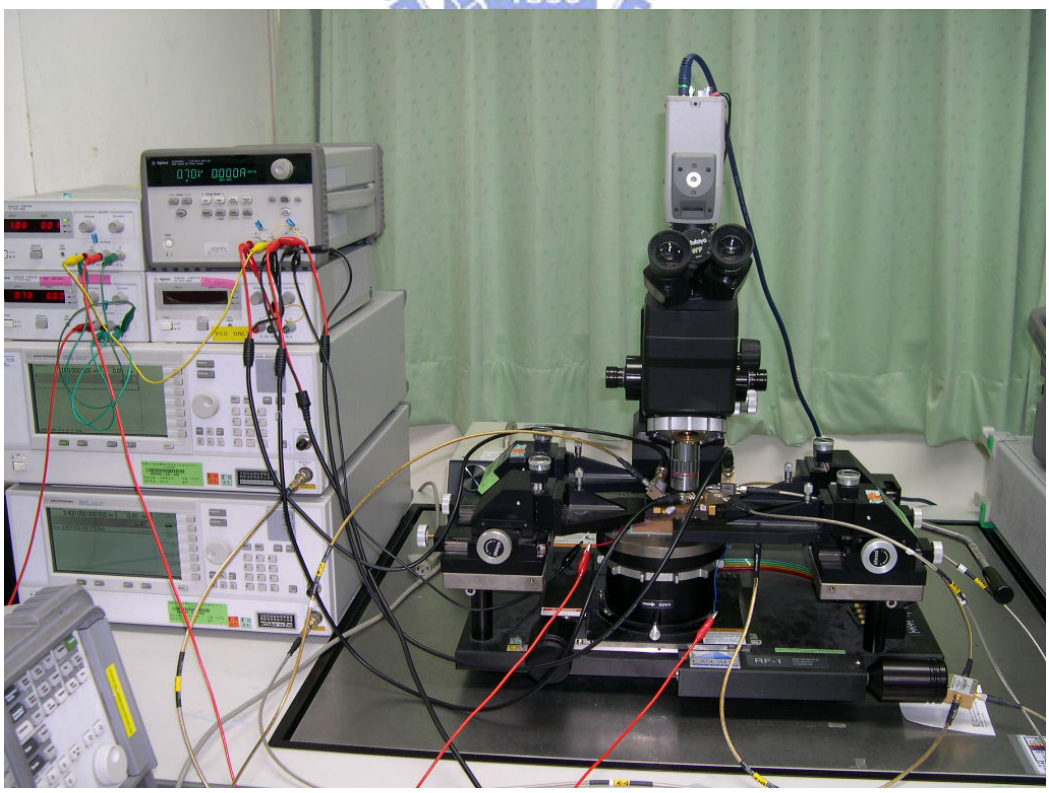


Fig. 2-8 Picture of measurement setup

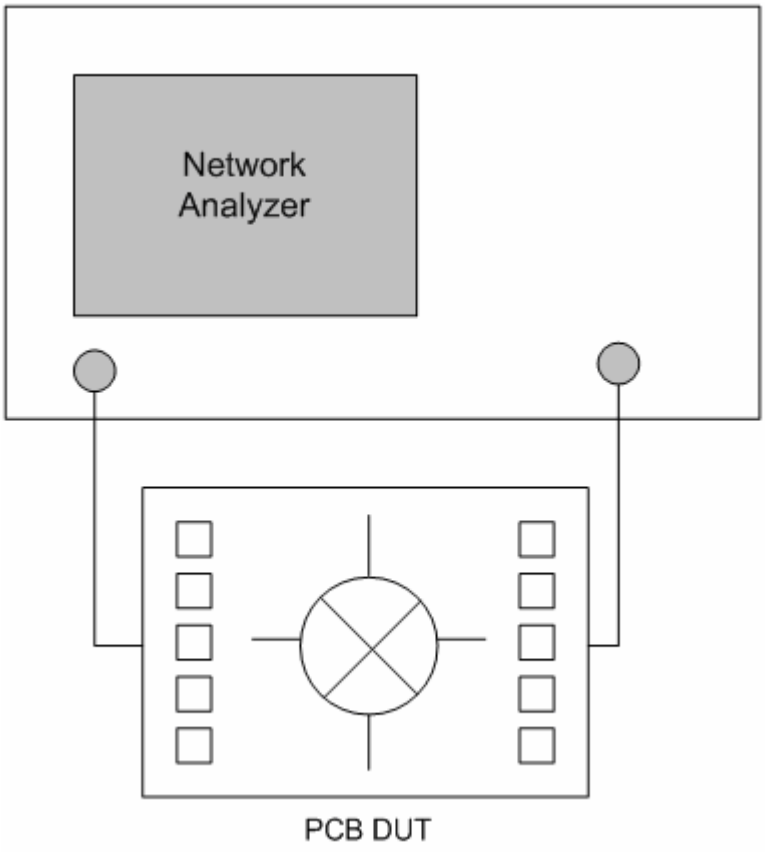


Fig. 2-9 Measurement setup for S-parameter

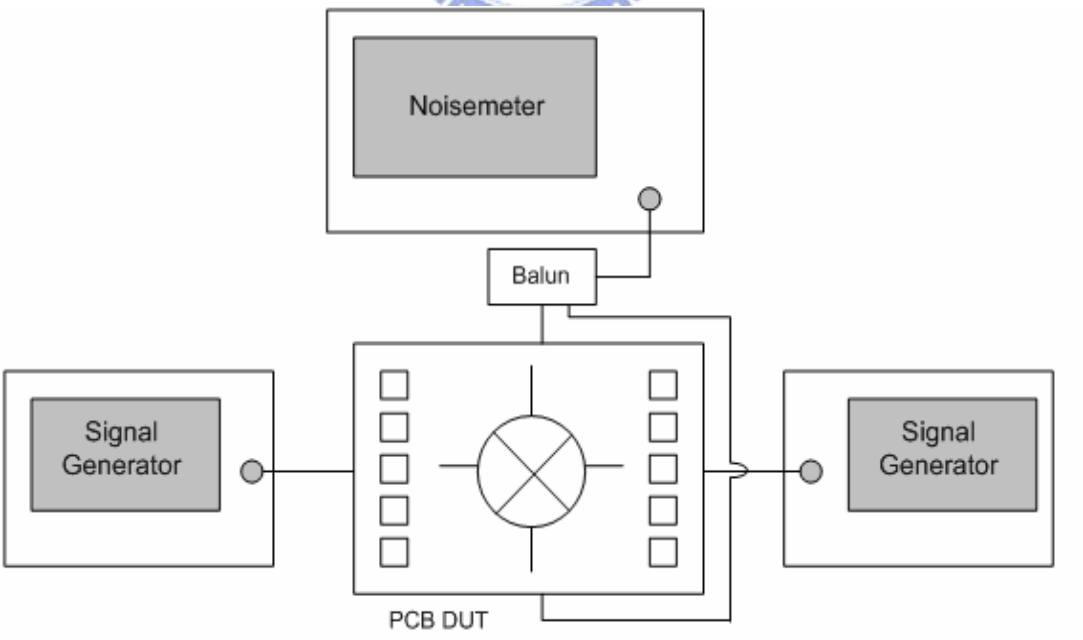


Fig. 2-10 Measurement setup for noise figure

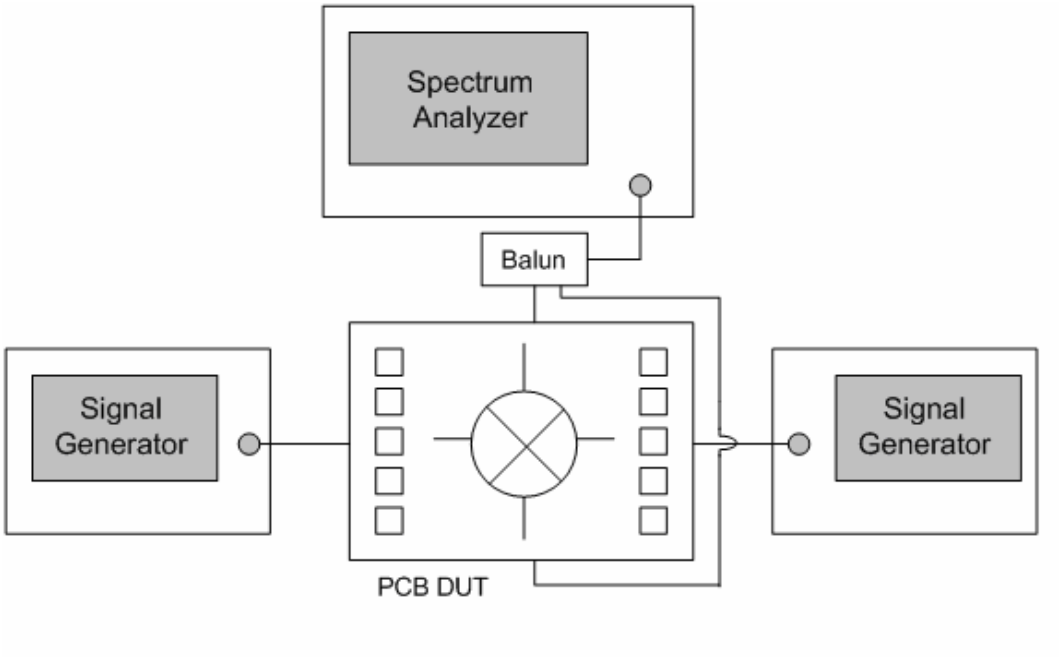


Fig. 2-11 Measurement setup for conversion gain and P1dB

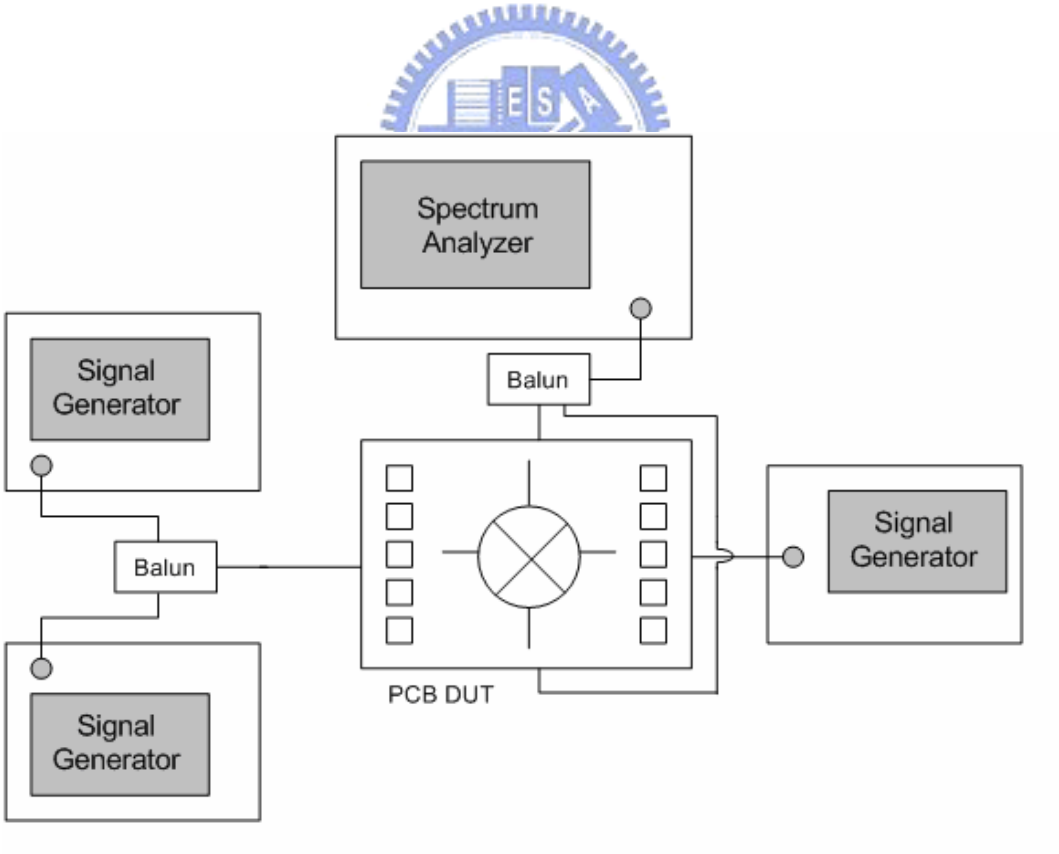


Fig. 2-12 Measurement setup for IIP3

2.4 Simulation and Experimental Results

The low-voltage folded-switching mixer was simulated and fabricated by CMOS 0.18-μm technology. The measurement results show that it has 6.21dB RF port return loss, 12.7dB LO port return loss, 8.99dB conversion voltage gain and 6.96dB conversion power gain at 0dBm LO power, -9dBm P1dB, and 4dBm IIP3. The total power consumption is 2.87 mW very close to the simulated one, 2.83mW.

Fig. 2-13 shows the RF port input matching. The measured RF port input matching is shifting down to 1.5 ~ 1.9 GHz due to the inductance of L_1 or L_2 (see Fig. 2-4) increasing and the parasitic capacitances to the substrate being more serious than simulation. At 2.45 GHz, The measured RF port input matching is -6.21 dB and the simulated one is -13.2 dB. Fig. 2-14 is the comparisons between measured and simulated LO port input matching. The measured result is matched to the simulation. But more parasitic capacitances to the substrate than the simulation result in not as sharp as the simulated curve at 2.45 GHz. The measured LO port input matching is -12.7 dB and the simulated one is -34.5 dB at 2.45 GHz.

Fig. 2-15 shows the measured and simulated conversion power gain. The primary reason for the two curves not matching is that the load resistors becoming larger by the process variations make the transistors in the switching stage (see Fig. 2-4) operate in linear region. The larger load resistors have more voltage drops across them and force the transistors in switching stage entering linear region due to insufficient voltage head room. By simulation again, the modified curve shown in Fig. 2-15 confirms this conclusion. There is 3-dB difference between the modified and measured conversion power curves resulting from the twice of simulated RF port input matching to the measured one. The measured conversion power gain at 0 dBm LO power is 6.96 dB. Fig. 2-16 shows the simulated and measured one dB

compression point. The simulated and measured P1dB is -15.5 and -9 dBm respectively. Fig. 2-17 is the comparisons between the simulated and measured third order intercept point. The simulated and measured IIP3 is -6 and 4 dBm respectively. The linearity is improved due to the conversion gain decreasing. Fig. 2-18 is IF output waveform. From Fig. 2-18, the conversion voltage gain by the calculation is 8.99 dB. We can not provide the measured noise figure because the measurement type is not accepted by CIC. The summary of the simulated and measured performances of the low- voltage folded-switching mixer is shown in Table 2-1.

Table 2-2 shows the comparisons with recently published works. Compared with other low-voltage mixers, this work has moderate conversion gain, higher linearity, and the lowest power consumption under 0.7V supply voltage.

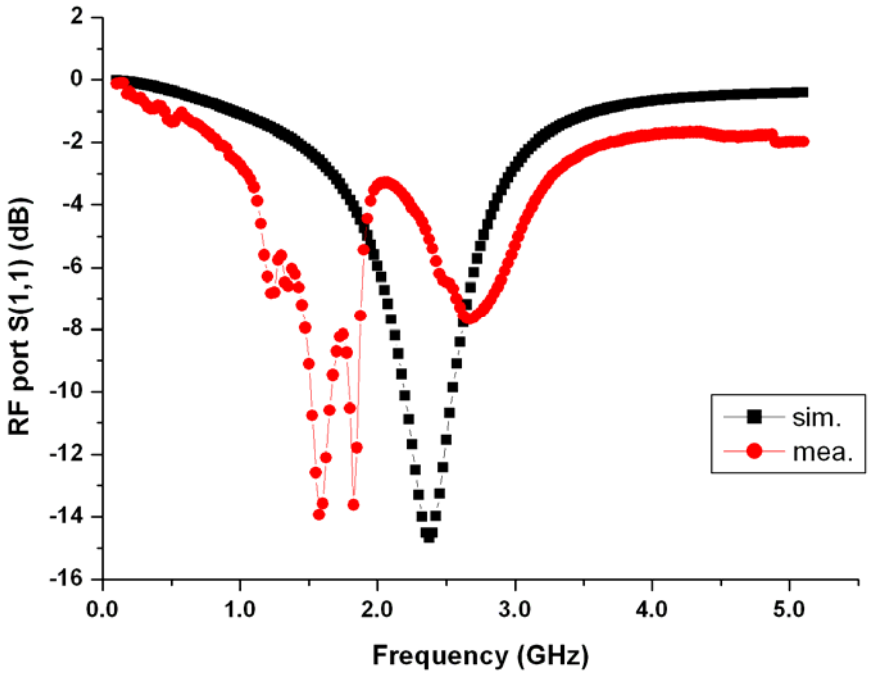


Fig. 2-13 Simulated and measured RF port input matching

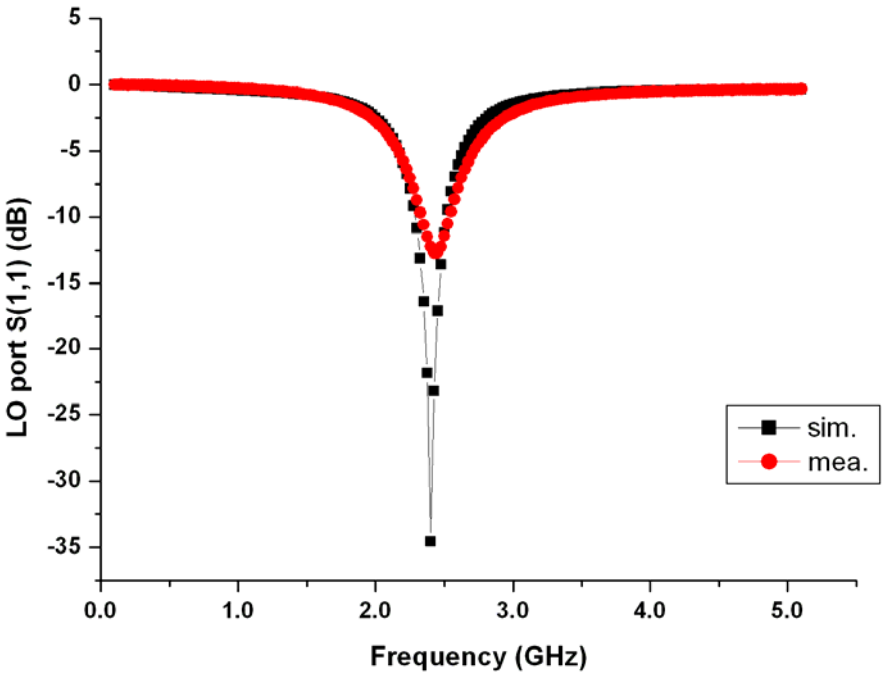


Fig. 2-14 Simulated and measured LO port input matching

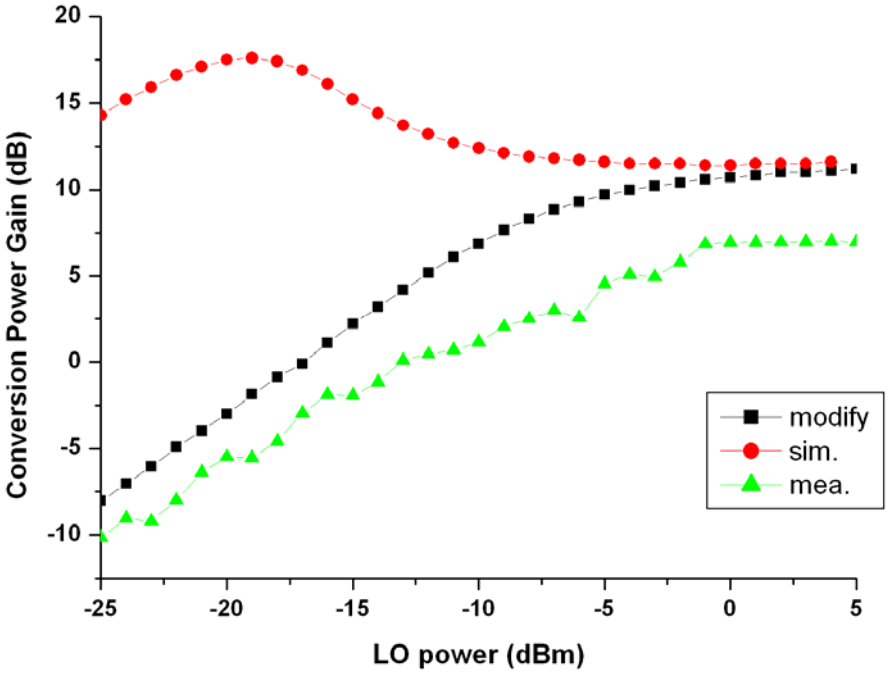


Fig. 2-15 Simulated and measured conversion power gain

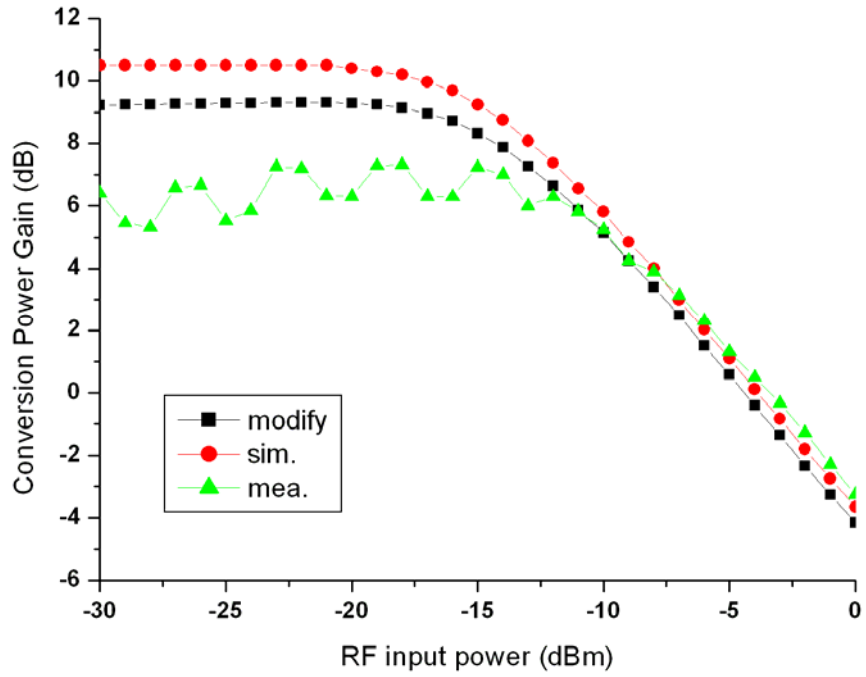


Fig. 2-16 Simulated and measured one dB compression point

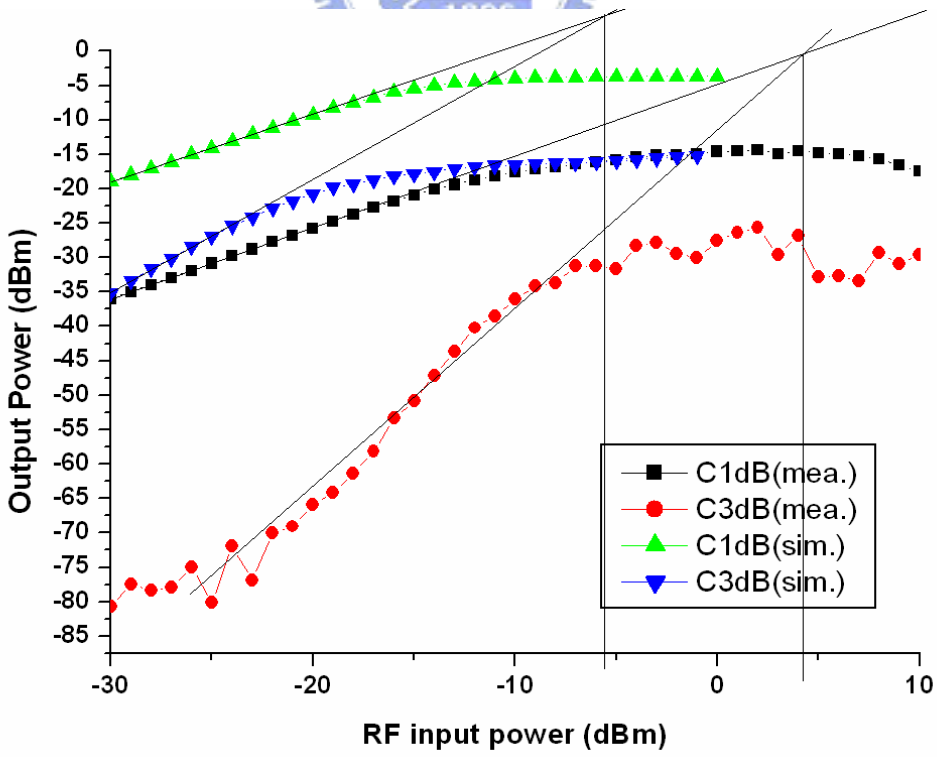


Fig. 2-17 Simulated and measured third order intercept point

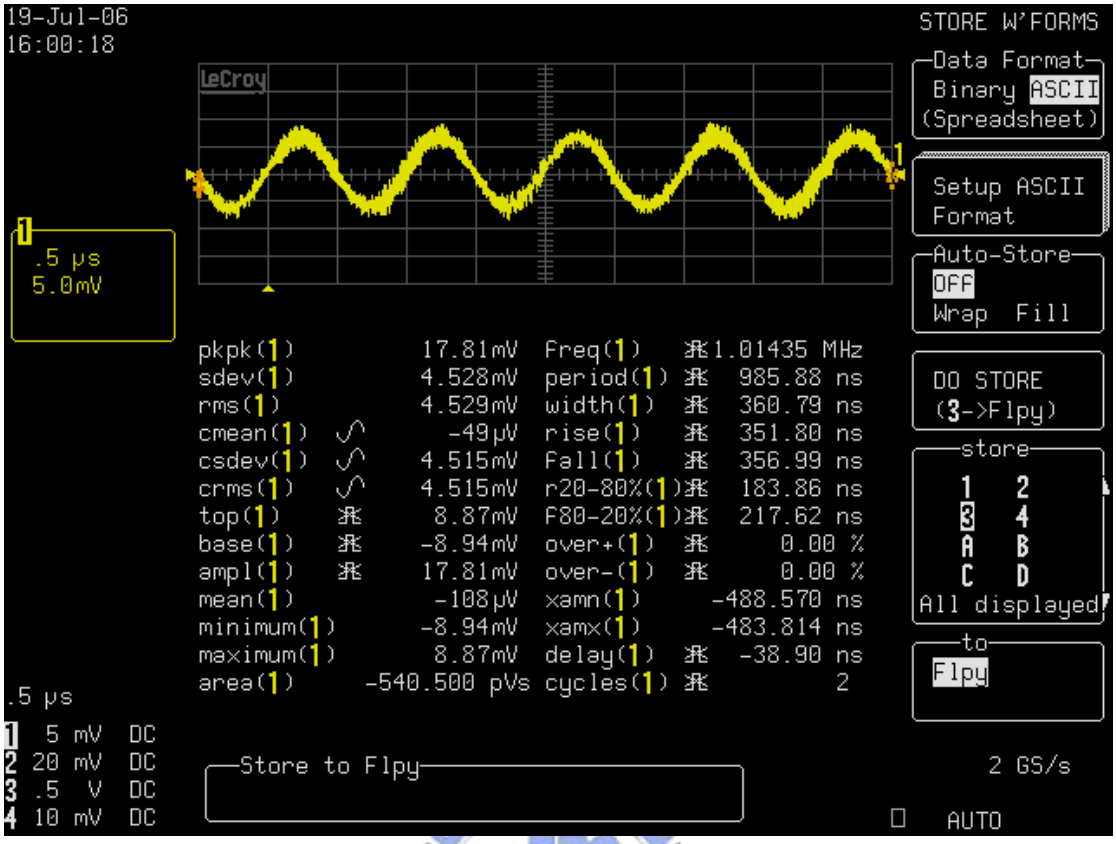


Fig. 2-18 IF output waveform of low-voltage mixer

Table 2-1 Summary of the performances of low-voltage folded-switching mixer

Specification	Simulation	Measurement
IF	1 MHz	1 MHz
Supply voltage (V)	0.7	0.7
RF input matching (dB)	-13.2	-6.21
LO input matching (dB)	-34.5	-12.7
Conversion power gain (dB)	11.4 @ LO 0dBm	6.96 @ LO 0dBm
P1dB (dBm)	-15.5	-9
IIP3 (dBm)	-6	4

NF (dB)	**10.3**	**N/A**
Conversion voltage gain (dB)	**13.8**	**8.99**
Core power dissipation (mW)	**2.83**	**2.87**
Total power dissipation (mW)	**20.46**	**24.87**

Table 2-2 Comparisons with recently published works

	[25]	**[26]**	**[27]**	**This work**
Freq. (GHZ)	**2.4**	**2.5**	**2.4**	**2.4**
Topology	**folded-switching**	**transformer based**	**Gilbert cell**	**folded-switching**
Vdd (V)	**1**	**0.6/0.8**	**1**	**0.7**
NF (dB)	**13.9**	**14.8/15.9**	**14**	**N/A**
Gain (dB)	**11.9**	**5.4/5.7**	**11**	**8.99**
IIP3 (dBm)	**-3**	**-2.8/4.3**	**4.1**	**4**
Power (mW)	**3.2**	**1.62/2.4**	**6.6**	**2.87**
Other Remarks	**CMOS 0.18-μm**	**CMOS 0.13-μm**	**Switched Transconductor**	**CMOS 0.18-μm**

Chapter 3

Conclusion and Future Work

3.1 Conclusion

In this thesis, we analyze the design of the low-voltage folded-switching mixer and low-voltage single-to-balanced LNA for the proposed architecture of low-IF receiver RF front-end. The two circuit blocks are implemented in TSMC CMOS 0.18-μm technology and simulated through Eldo-RF simulator. We have presented the measured parameters of the mixer in the Chapter 2. But the LNA is still under fabricated; we only provide simulated results in the Appendix.

A fully integrated, low-voltage, low-power, high gain, ac-coupled folded-switching mixer with current reuse is presented. The main advantages of the proposed new mixer topology are high voltage gain (8.99 dB), moderate noise figure (10.3 dB in simulation), moderate linearity (P1dB = -9 dBm and IIP3 = 4 dBm), operation at low supply voltage (V_{dd} = 0.7 V), and low power consumption (2.87 mW), and simplicity due to no common-mode feedback is necessary. As a result of process variations make the load resistors become larger and hence the measured results of the proposed mixer are not as good as the simulated results.

3.2 Future work

For higher frequency applications more accurate RF CMOS component models such as large size MIM capacitors and different inductance spiral inductors with higher Q-value should be built up for exactly matching network design in the future. All parasitic effects including parasitic capacitance, series resistance and inductance must be considered carefully. A more precise and efficient EDA tool for extraction of the parasitic effects is quietly important.

For the RF front-end integrating with base band circuits, reduced supply voltages for RF front-end are necessary. Therefore it needs more efforts to make the RF and analog circuit blocks operate at sub-1V supply voltage and still have enough dynamic ranges and other comparable circuit performances.

In the future, the low-voltage folded-switching mixer and the low-voltage single-to-balanced LNA (see Chapter 4) need to be integrated in a single chip to realize the proposed low-IF receiver architecture.

Chapter 4

Appendix ：

Low-voltage (0.7V) Single-to-Balanced Low-Noise Amplifier

4.1 Low-Voltage Single-to-Balanced LNA Design

As the first stage of receiver, a low-noise amplifier's (LNA) main function is to provide enough gain to overcome the noise of the subsequent stages while adding as little noise as possible. Besides, an LNA should accommodate large signals without distortion, and frequently must also present the specific impedance, such as 50Ω, to the input source. The impedance is particularly important if a passive filter precedes the LNA, since the transfer function of many filters are quite sensitive to the quality of the termination.

In this work, we present a low-voltage single-to-balanced LNA operating at 0.7V supply voltage. It consists of two stages. One is the single-ended folded-cascode LNA

and the other is common-source/common-gate PMOS pair active balun. The schematic is shown in

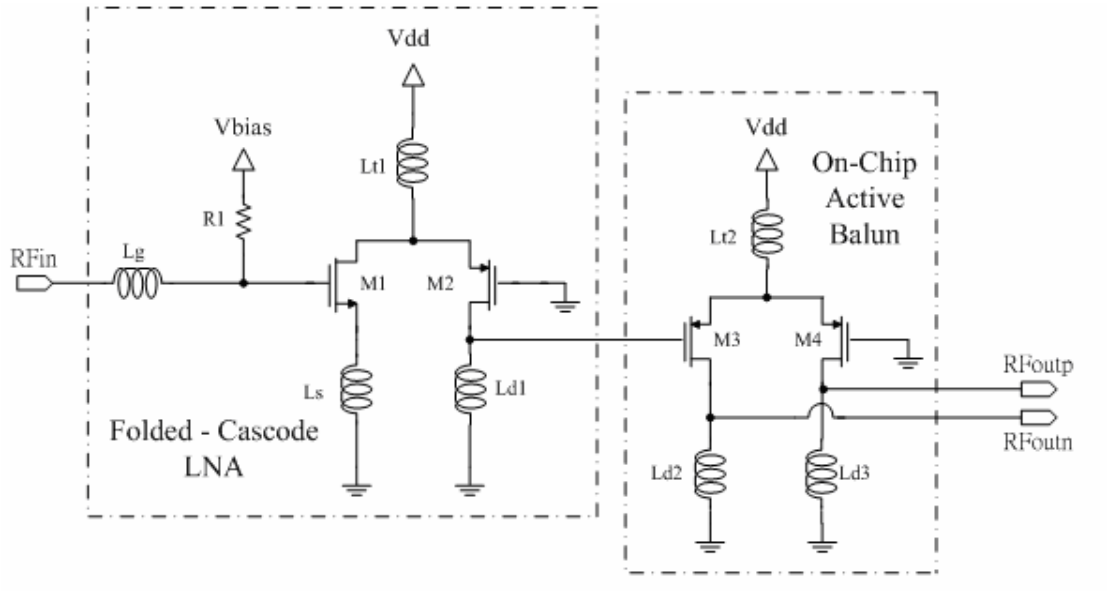


Fig. 4-1. Following subsections we will discuss the analyses of input matching network, noise figure, and power consumption of the proposed LNA.

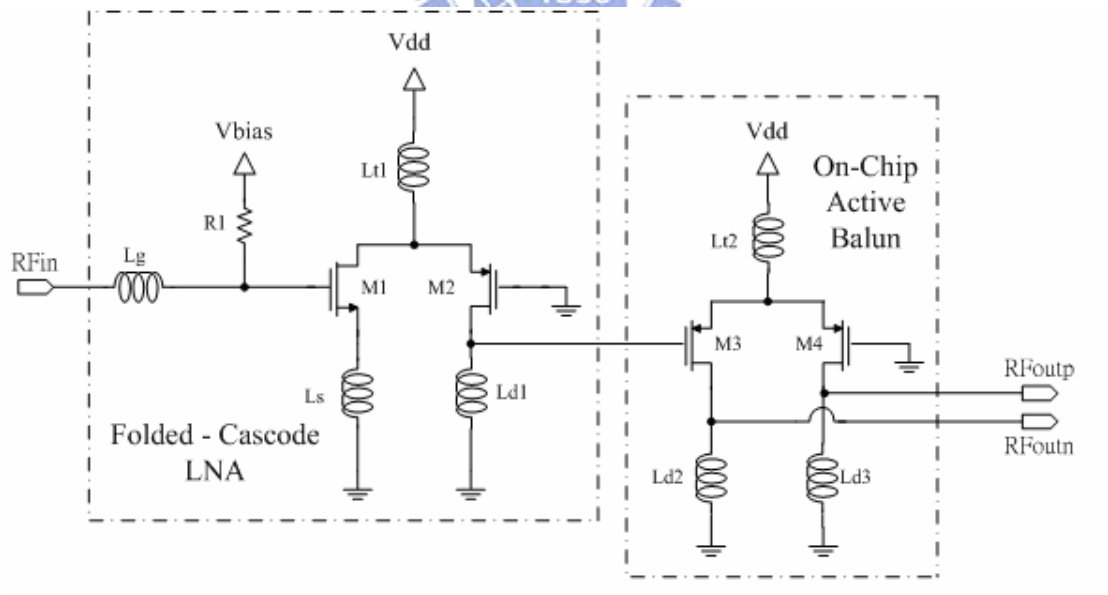
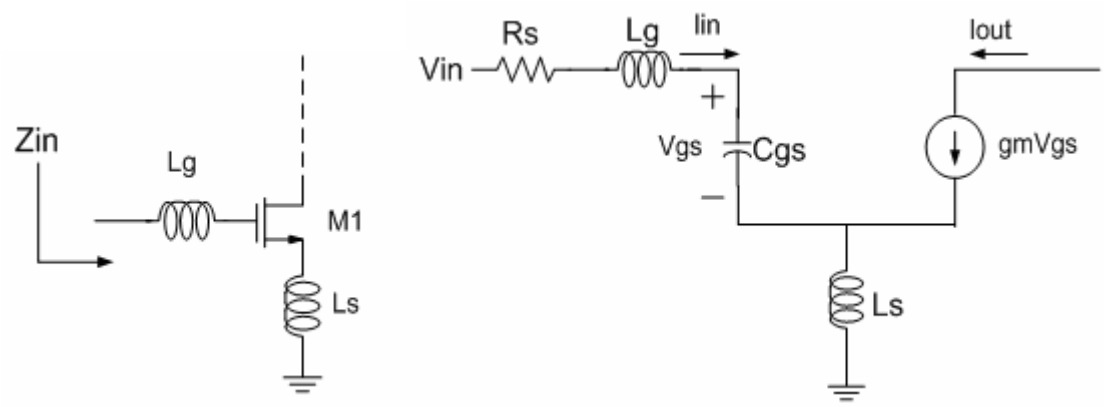


Fig. 4-1 Schematic of low-voltage single-to-balanced LNA

4.1.1 Input Matching

The input matching network is using inductive source degeneration. Fig. 4-2(a) is the input stage of the LNA and Fig. 4-2(b) is the small-signal equivalent model for the input stage of the LNA.



(a) (b)

Fig. 4-2 Narrowband LNA (a) with inductive source degeneration (b) and its equivalent small-signal model

Applying KVL to the input loop in the Fig. 4-2(b) we can write

$$V_{in} = I_{in}(j\omega L_g + j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{g_{m1}}{C_{gs}} L_s) \tag{4.1}$$

Therefore, the input impedance is

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \left(\frac{g_{m1}}{C_{gs}}\right) L_s \tag{4.2}$$

$$\approx \omega_T L_s \quad \text{(at resonance)} \tag{4.3}$$

For matching to the source impedance *Rs*,

$$L_s = \frac{C_{gs}}{g_{m1}} R_s \tag{4.4}$$

And at series resonance,

$$\omega_0 = \sqrt{(L_g + L_s)C_{gs}} \tag{4.5}$$

It can be seen from above equations that at series resonance the input impedance is purely real and proportion to *Ls*. By choosing *Ls* appropriately, this real term can be made equal to 50Ω. The gate inductor *Lg* is used to set the resonance frequency once the *Ls* is chosen to satisfy the criterion of a 50-Ω input impedance.

4.1.2 Noise Figure

In this subsection we will introduce the power-constrained noise optimization technique and apply this to the design of the proposed LNA [6], [9], [10]. First, use (2.5) to determine the necessary optimum device width for the power-constrained optimum NF.

$$W_{opt} \approx \frac{1}{3\omega L C_{ox} R_s} \tag{4.6}$$

Then, bias the device with the amount of current allowed by power constrain. Finally, select the value of source degeneration inductance required for the desired input impedance and set the gate inductance to resonate at the operating frequency.

Having outlined the basic design procedure, we now turn the attention to the derivation of the noise figure.

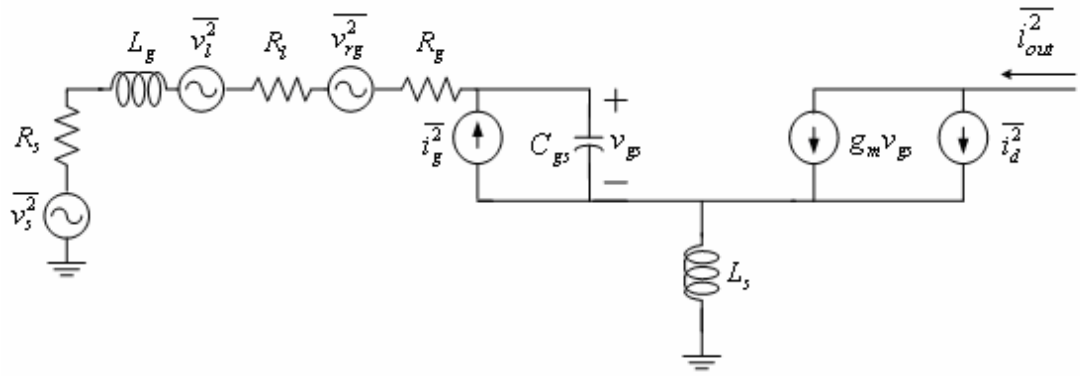


Fig. 4-3 shows the complete small-signal model for LNA noise calculation.

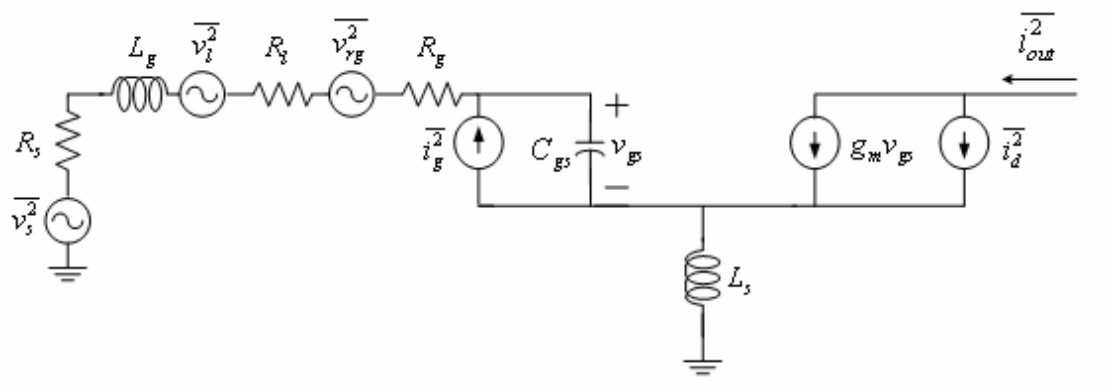


Fig. 4-3 Small-signal noise model of the MOS

In this model, R_l represents the series resistance of the inductor Lg, R_g represents the distributed gate resistance of the NMOS device and its value is given by [11],

$$R_g = \frac{R_{sheet} W}{3n^2 L} \tag{4.7}$$

$\overline{i_g^2}$ is the induced gate noise current, and $\overline{i_d^2}$ is the channel thermal noise of the device. The noise power due to R_l can be neglected because the metal wire of the inductor has significantly lower sheet resistance. In salicided CMOS processes the sheet resistance (R_{sheet}) can be greatly reduced, so the thermal noise contribution of R_g to the output noise power is also neglected. For simplicity, assuming that the channel thermal noise dominates for noise figure calculations, we have

$$\overline{v_i^2} = \frac{\overline{i_d^2}}{|G_m|} \tag{4.8}$$

Where G_m is the overall input stage transconductance and at resonance is equal to

$$G_m = g_{m1} Q_{in} = \frac{1}{\omega_0 C_{gs} Z_{in}} \tag{4.9}$$

Substitute (4.9) to (4.8), yielding

$$\overline{v_i^2} = \frac{4kT\gamma g_{m1}\Delta f}{g_{m1}^2 Q_{in}^2} \tag{4.10}$$

Substitute (2.9) into $N_{add} = \frac{\overline{v_i^2}}{\Delta f}$ will give

$$NF = 1 + \frac{N_{add}}{N_{in}} = 1 + \frac{4kTg_{m1}\gamma}{g_{m1}^2 Q_{in}^2 (4kTR_s)} = 1 + \frac{\gamma}{g_{m1} Q_{in}^2 R_s} \tag{4.11}$$

where $Q_{in} = \frac{1}{\omega_0 C_{gs} Z_{in}}$ denotes the quality factor of the input matching network. According to (2.10), the best noise figure is obtained for Q_{in} approach to ∞, which means Z_{in} must be zero and the input matching condition and the minimum noise figure can not be reached simultaneously. But if we set the device width with W_{opt}, a reasonable input match is guaranteed while providing nearly the best noise figure with specified power consumption by the inductive source degeneration.

To gain more insight to (2.10), let us rearrange the NF by substitute $Z_{in} = R_s = \frac{g_{m1} L_s}{C_{gs}}$ and $L_g + L_s = \frac{1}{\omega_0^2 C_{gs}}$ into (2.10), we get

$$NF = 1 + \frac{2}{3}\frac{1}{1 + \frac{L_g}{L_s}} \approx 1 + \frac{2}{3}\frac{L_s}{L_g} \tag{4.12}$$

We can indicate that NF decreases as L_g increases. This equation provides valuable design guideline.

4.1.3 Power Dissipation

In this subsection we will derive the dependence of power dissipation on technology and circuit parameters under matching condition with a given bias voltage. At first,

$$P_D = I_D V_{DD} \tag{4.13}$$

where I_D is the drain current of the M_1 operated in saturation region and I_D is

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_T\right)^2 \tag{4.14}$$

Therefore,

$$P_D \propto \mu_n C_{ox}\frac{W}{L} \tag{4.15}$$

Next, form the $g_{m1} \propto \mu_n C_{ox}\frac{W}{L}$ and $C_{gs} = \frac{2}{3}WLC_{ox}$, we obtain

$$P_D \propto \frac{g_{m1}^2}{C_{gs}}\frac{L^2}{\mu_n} \tag{4.16}$$

Finally, we want to express g_m and C_{gs} in terms of circuit element parameters under matching condition. That is

$$g_{m1} = \frac{R_s C_{gs}}{L_s} \tag{4.17}$$

$$C_{gs} = \frac{1}{\omega_0^2\left(L_g + L_s\right)} \tag{4.18}$$

Then, substitute (4.16) and (4.17) into (4.15), we get

$$P_D \propto \frac{L^2}{\mu_n}\left(\frac{R_s}{\omega_0}\right)^2 \frac{1}{L_s^3\left(1+\frac{L_g}{L_s}\right)} \tag{4.19}$$

From (4.19), we conclude that P_D decreases as L_g goes up. A similar situation is in *NF*.

4.1.4 On-Chip Active Balun

There are various types of baluns [11] such as a passive type, a source/drain type [12], a push-pull active type [13], a distributed active type [14], and a

common-source/common-drain FET pair active type [15], [16]. The passive balun has a large circuit area and is not suitable for integration request. A push-pull type and distributed active balun does not have low power consumption. A source/drain type does not have broadband performance. On the other hand, a common-source/common-drain FET pair type as shown in Fig. 2-4 has broadband performance and low power consumption and hence is a strong candidate for this work.

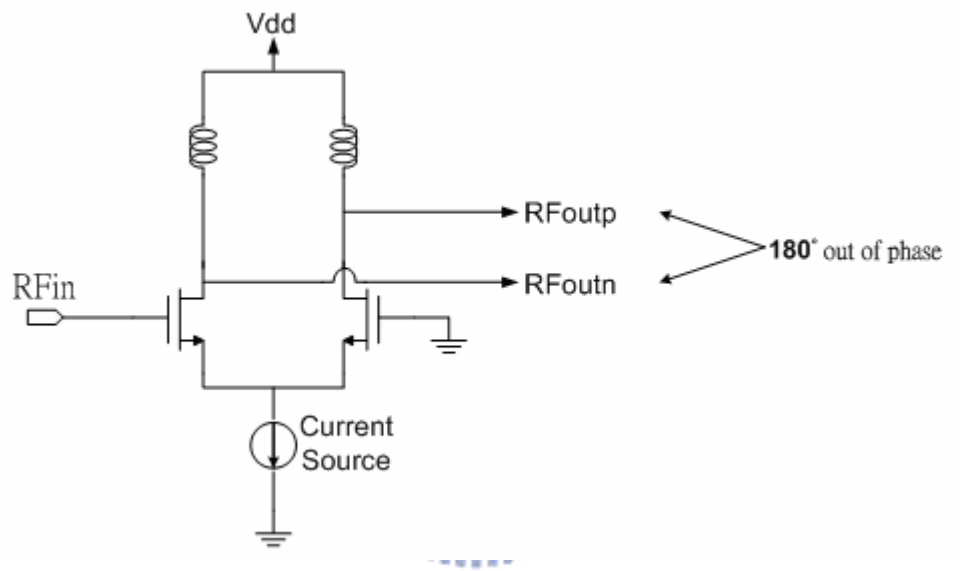


Fig. 4-4 Differential topology for active balun

The RF signal applied to the gate of the transistor will ideally split equally in magnitude and have 180° phase difference between the two output signals (see Fig. 4-4). In other words, the small signal gate-source voltage for the pair is equal, and can be expressed as

$$V_{gs1} = V_{gs2} = \frac{V_{RF}}{2} \tag{4.20}$$

Because of the non-ideal current source results in unequal signal distribution, therefore leading imbalance in the differential signal. In this work, we proposed a modified topology as shown in Fig. 2-5 to improve output impedance of the current source and to make the balun suitable to operate at low supply voltage.

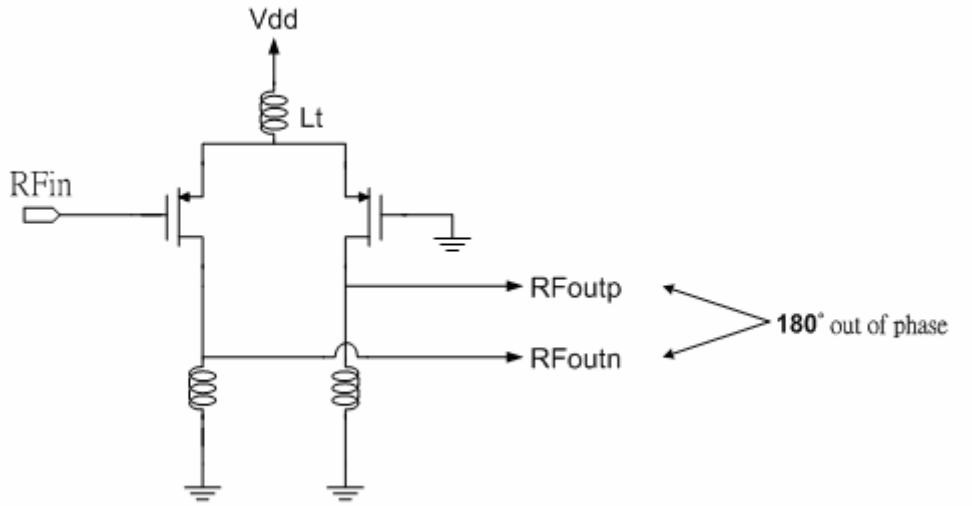


Fig. 4-5 New differential active balun topology

In Fig. 4-5, we use an inductor L_t to replace the current source. Besides, the NMOS pair is replaced by the PMOS one for the reason of biasing this balun. So the original current source biasing is turned to fixed gate voltage biasing while the topology has the same circuit function as the one shown in Fig. 4-4. Further more, it is unsuitable for low supply headroom that a current source is stacked below the NMOS pair (see Fig. 4-4). In Fig. 4-5, the inductor L_t served as a RF choke is short-circuited at DC and hence ideally has no voltage drop to reduce voltage headroom, which makes the topology shown in Fig. 4-5 suitable to operate at low supply voltage. In addition, L_t is like a source degeneration inductor and hence improves linearity of the LNA. The complete schematic of proposed low-voltage single-to-balanced LNA is shown in

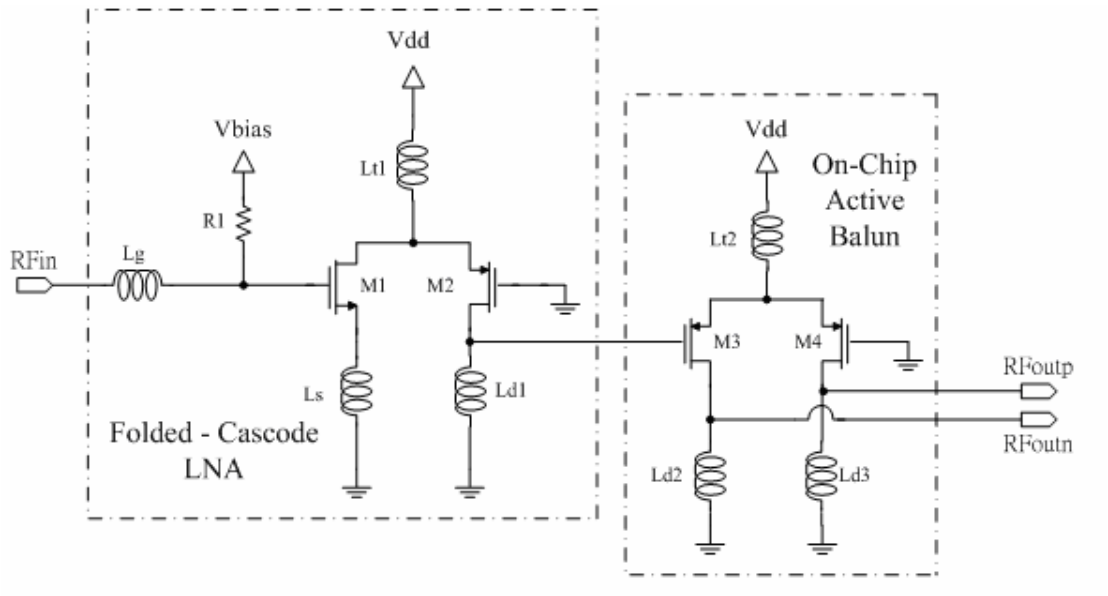


Fig. 4-1.

4.2 Layout and Measurement Consideration

The most layout guidelines for the single-to-balanced LNA are the same in section 2.3. Fig. 4-6 shows the layout of the LNA, and the total chip size is 1.393 × 1.383 mm^2. The low-voltage LNA is designed for on-wafer measurement so the layout must follow the rules of CIC (Chip Implementation Center)'s probing testing [13]. This circuit needs a 3-pin RF GSG probe, a 5-pin differential RF GSGSG probe, and two three- pin DC probes. Fig. 4-7 shows the on-wafer measurement setup with the four probes. The top and bottom probes are DC PGP probes which provide power supply and necessary DC bias for the circuit. The left and right is RF GSG and RF GSGSG probes respectively. The Fig. 4-7 ~ Fig. 4-10 show the measurement setup for S-parameters, noise figure, 1 dB compression point, and input-referred third-order intercept point. We will discuss the simulation results in the following subsection.

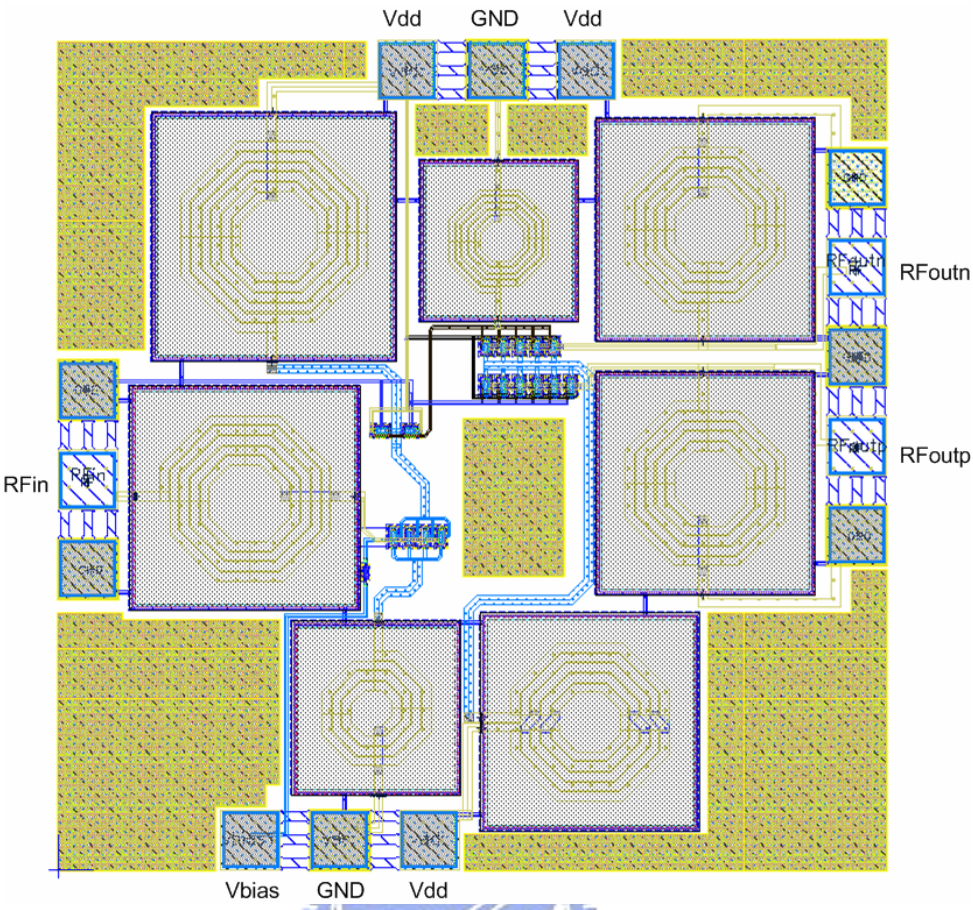


Fig. 4-6 Chip layout of the proposed LNA

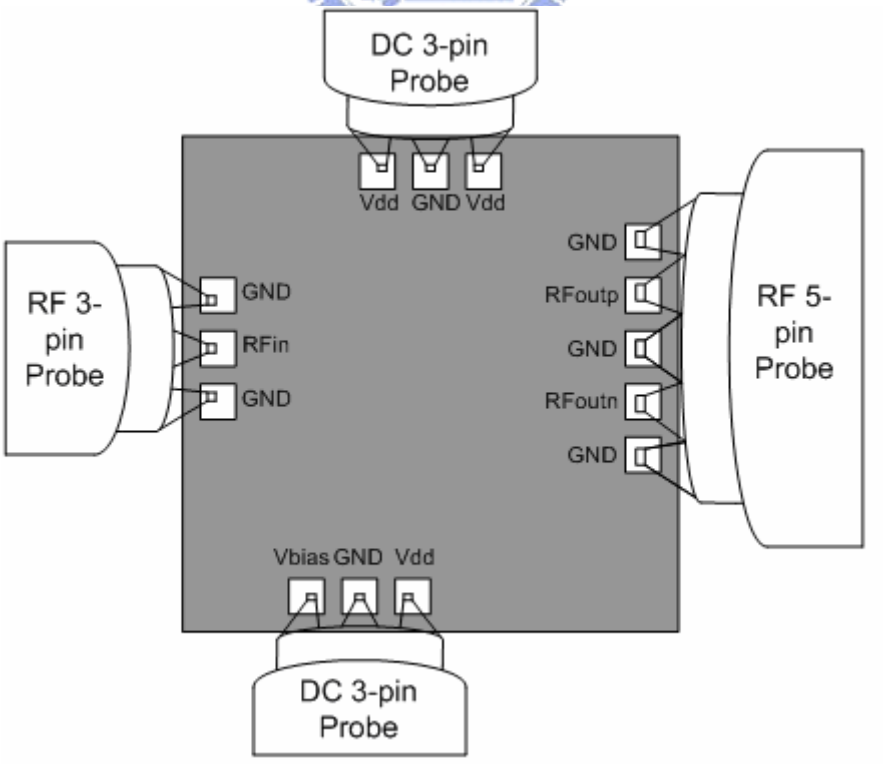
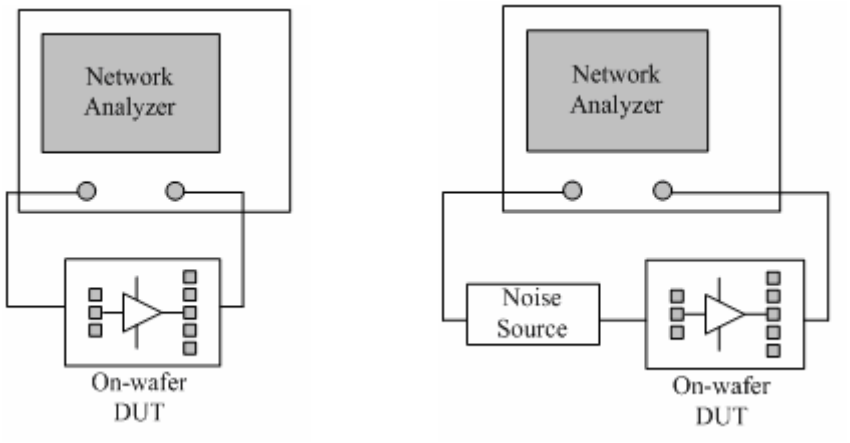


Fig. 4-7 On-wafer measurement diagram



(a) (b)

Fig. 4-8 Measurement setup for (a) S-parameters (b) noise figure

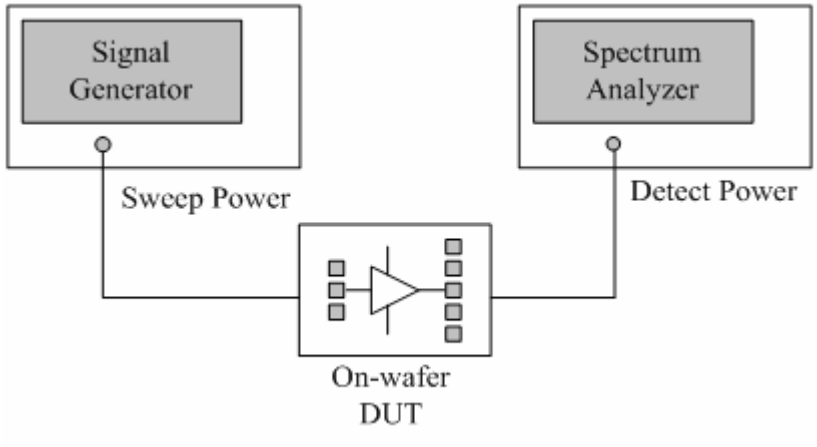


Fig. 4-9 Measurement setup for 1-dB compression point

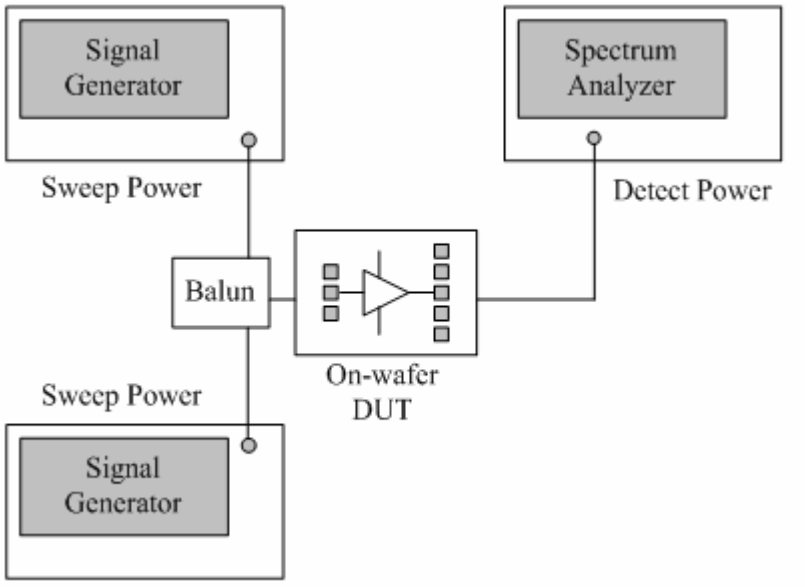


Fig. 4-10 Measurement setup for input-referred third-order intercept point

4.3 Simulation Results and Comparisons

The simulation results at 2.45GHz reveal that input matching is -37.6dB (shown in Fig. 4-11), gain (S_{21}/S_{31}) is 13.6 / 14.2dB (shown in Fig. 4-12), reversed isolation (S_{12}/S_{13}) is -69/-47dB (shown in Fig. 4-13), noise figure is 2.81dB (shown in Fig. 4-14), power gain is 14.6dB, P_{1dB} is -12.7dBm (shown in Fig. 4-15), and IIP3 is -8.24dBm (shown in Fig. 4-16). The simulated gain and phase mismatch is below 1dB and 2 degrees around 180° in the 700MHz bandwidth from 2GHz to 2.7GHz (see Fig. 4-17 and Fig. 4-18). The total power consumption is 15.66mW. The summary of performances of proposed LNA is listed in Table 4-1. Table 4-2 shows comparisons of the proposed LNA and recently published low-voltage LNA designs.

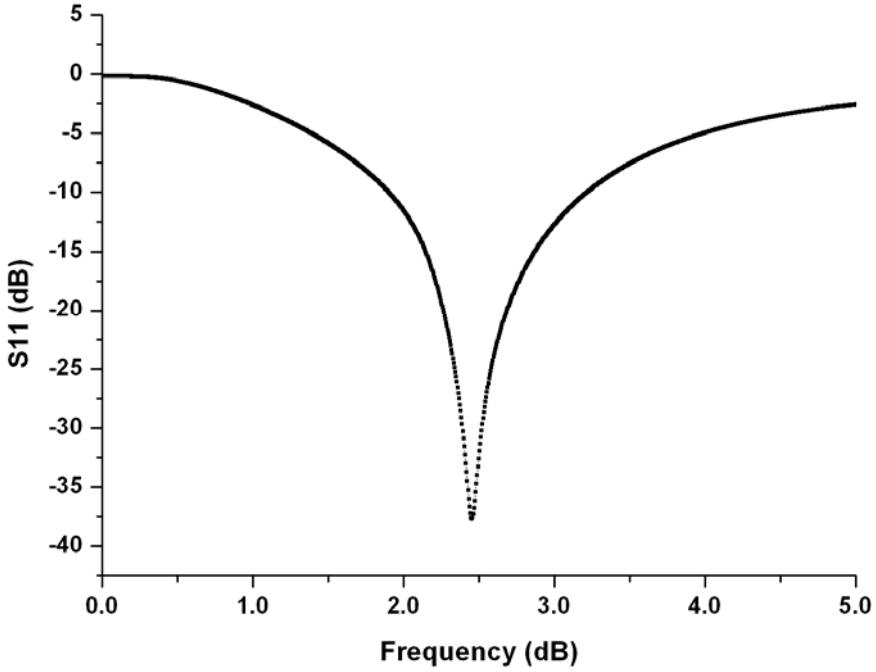


Fig. 4-11 Simulated input matching (S_{11})

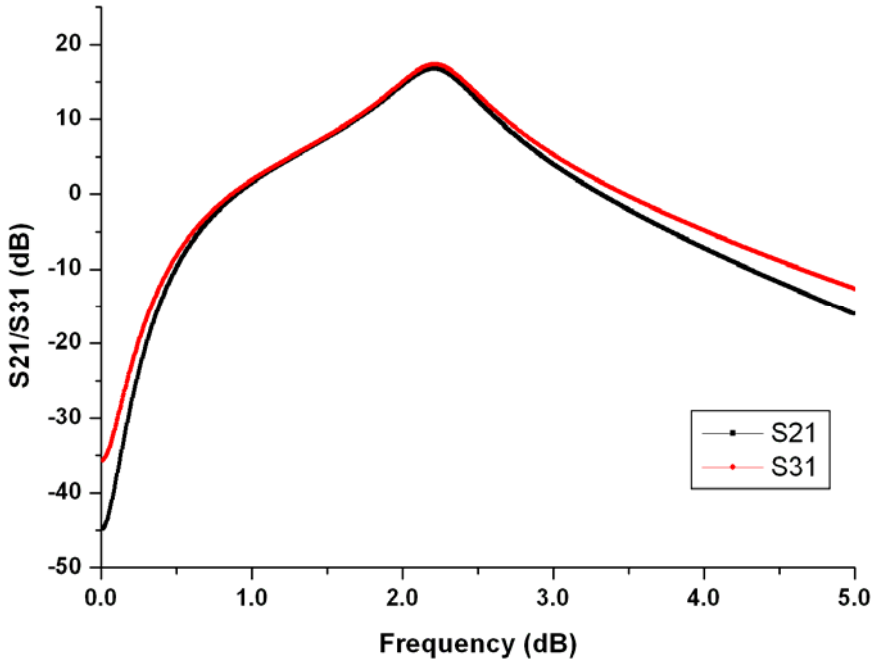


Fig. 4-12 Simulated gain (S_{21}/S_{31})

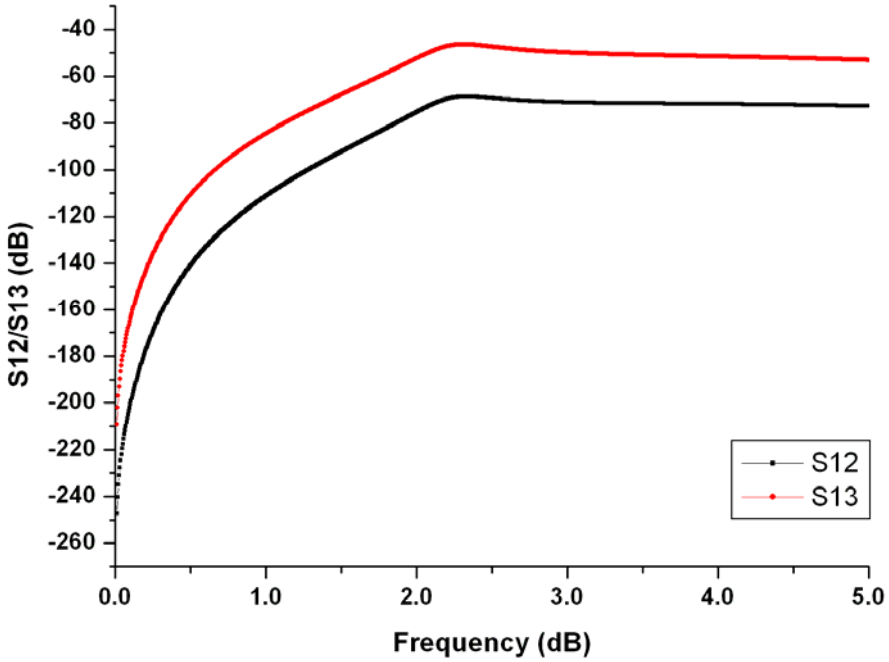


Fig. 4-13 Simulated reversed isolation (S_{12}/S_{13})

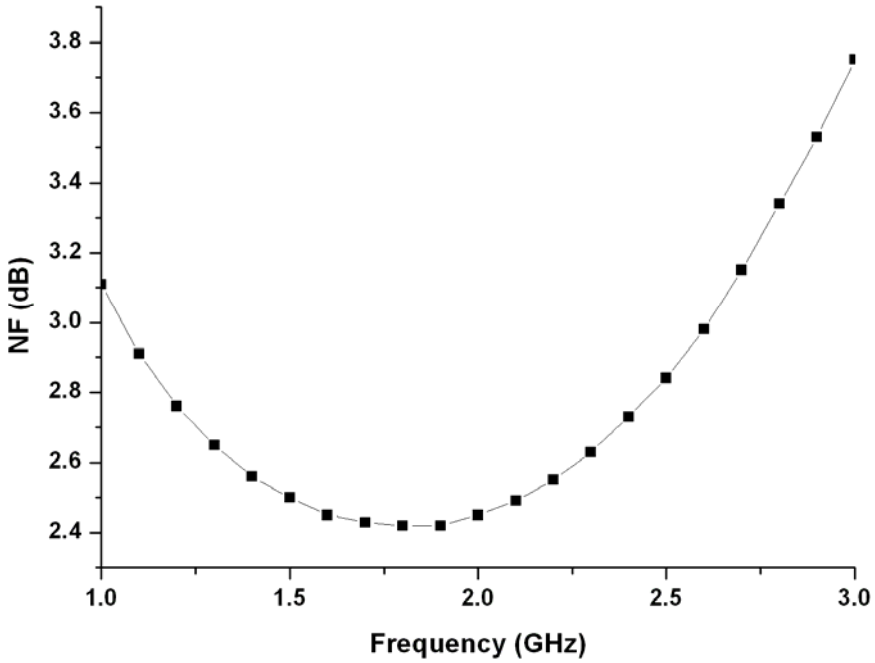


Fig. 4-14 Simulated noise figure

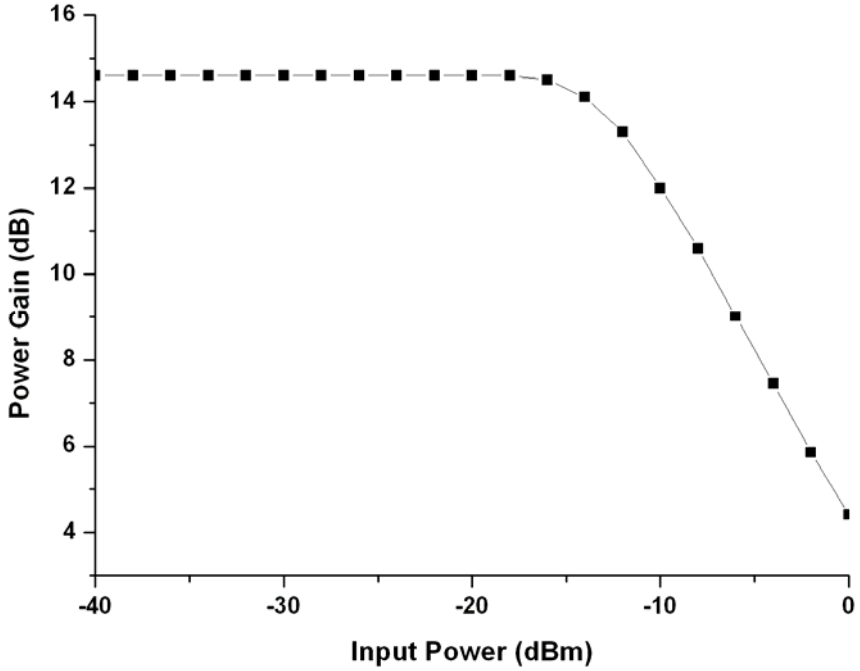


Fig. 4-15 Simulated 1-dB compression point

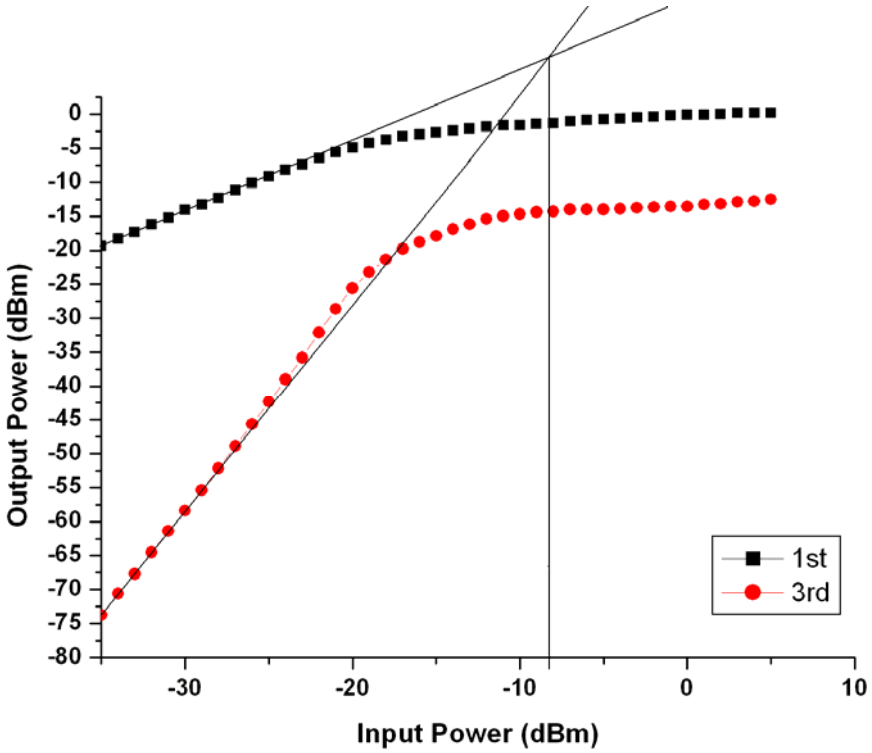


Fig. 4-16 Simulated input-referred third-order intercept point

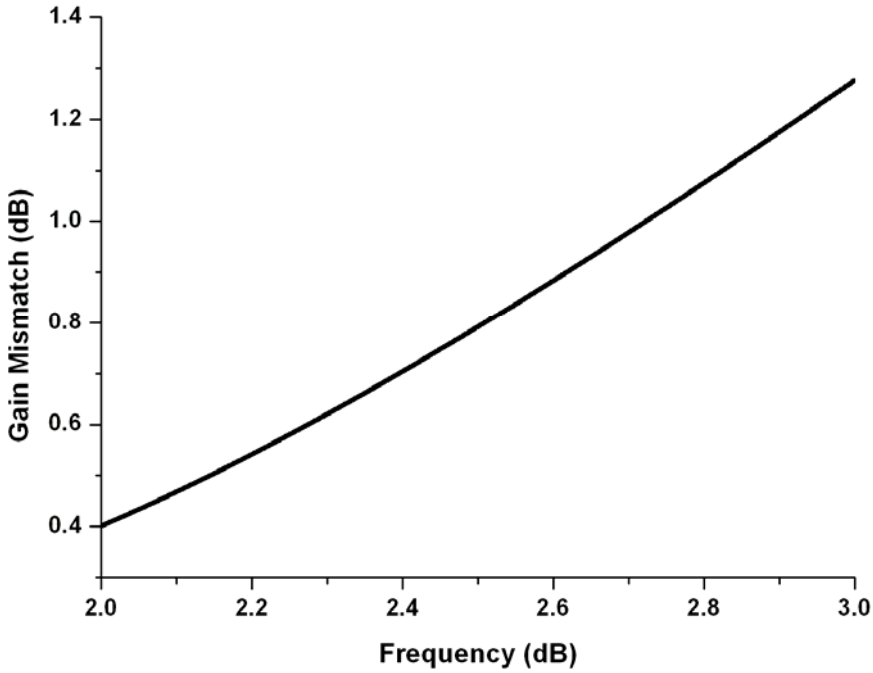


Fig. 4-17 Simulated gain mismatch between S_{21} and S_{31}

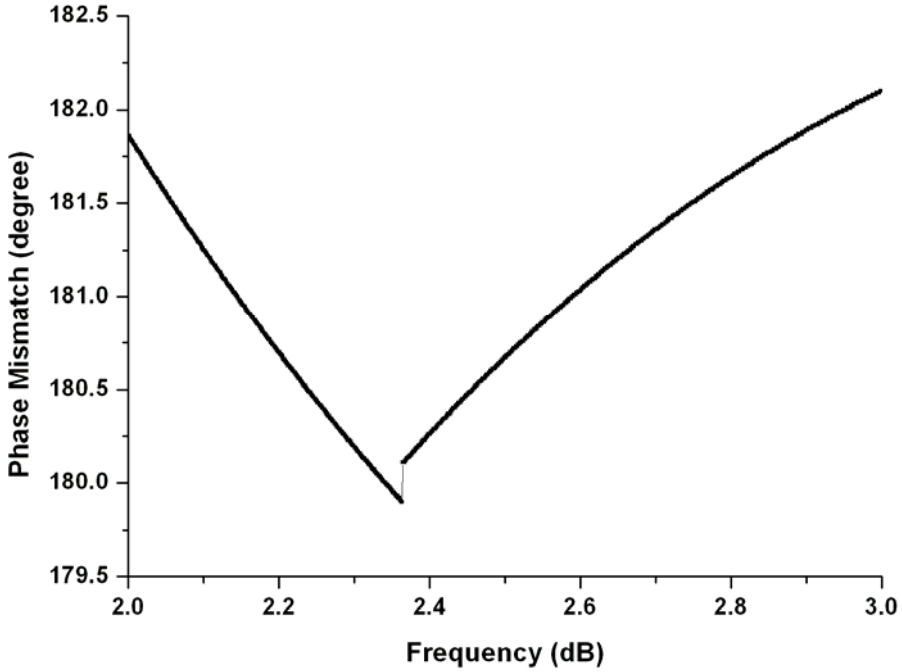


Fig. 4-18 Simulated phase mismatch between S_{21} and S_{31}

Table 4-1 Performance summary of the low-voltage single to balanced LNA

Specification	Simulation
Frequency	**2.45 GHz**
Vdd	**0.7 V**
S_{11}	**-37.6 dB**
S_{21}/S_{31}	**13.6 / 14.2 dB**
S_{12}/S_{13}	**-69 / -47 dB**
NF	**2.81 dB**
Power Gain	**14.6 dB**
P1dB	**-12.7 dBm**
IIP3	**-8.24 dBm**
Power Consumption	**15.66 mW**

Table 4-2 Comparisons of recently published low-voltage LNA designs and this work

	ISCAS 2002 [18]	JSSC 2003 [19]	VLSI 2004 [20]	This Work
Technology	CMOS 0.18μm	CMOS 0.18μm	CMOS 0.09μm	CMOS 0.18μm
Topology	Folded Cascode	Single Transistor	Folded Cascode	Folded Cascode
F_o (GHz)	5.8	5.75	5.5	2.45
V_{dd} (V)	1 / 0.7	1	1 / 0.6	0.7
S_{21} (dB)	13.2 / 7	14.2	15 / 11.2	13.6 / 14.2
P_{dd} (mW)	22.2 / 12.5	16	11.1 / 2.1	15.66
NF (dB)	2.5 / 2.68	0.9	2.8 / 3.2	2.81
P_{-1dB} (dBm)	-14 / -9	-9.1	-17.9 / -17.5	-12.7
Other Remarks	Gain and freq. tuning	Differential LNA, transformer feedback	More advanced technology	Single-to-balanced LNA

Reference

[1] A.Rofougaran, J. Y. C. Chang, M. Rofougaran, and A. A. Abidi, "A 1-GHz CMOS RF front-end IC for a direct-conversion wireless receiver," *IEEE J. Solid State Circuits*, vol. 31, pp. 880-889, July 1996.

[2] J. Crols and M. S. J. Steyaert, "A single-chip 900-MHz CMOS receiver front-end with high-performance low-If topology," *IEEE J. Solid State Circuits*, vol. 30, pp. 1483-1492, Dec. 1995.

[3] J. C. Rudell, J.-J. Ou, T. B. Cho, G. Chien, F. Brianti, J. A. Weldon, and P. R. Gray," A 1.9-GHz wide-band IF double conversion CMOS integrated receiver for cordless telephone applications," *IEEE J. Solid State Circuits*, vol. 32, pp. 2071-2088, Dec. 1997

[4] B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *IEEE J. Solid State Circuits*, vol. 33, pp. 2219-2231, Dec. 1998.

[5] D. K. Shaeffer, S. S. Mohan, H. Samavati, H. R. Rategh, M. d. M. Hershenson, M. Xu, C. P. Yue, D. J. Eddleman, and T. H. Lee, "A 115-mW 0.5-μm CMOS GPS receiver with wide dynamic range active filters," *IEEE J. Solid State Circuits*, vol. 33, pp. 2219-2231, Dec. 1998.

[6] D. K. Shaeffer and T. H. Lee, "A 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid State Circuits*, vol. 32, pp. 745-759, May 1997.

[7] B. Gilbert, "A precise four qudrarant multiplier with subnanosecond response," *IEEE J. Solid State Circuits*, vol. 3, pp. 365-373, Dec. 1968.

[8] P. J. Sullivan, B. A. Xavier, and W. H. Ku, "Low-voltage performance of a microwave CMOS Gilbert cell mixer," *IEEE J. Solid State Circuits*, vol. 32, pp. 1151-1155, July 1997.

[9] Thomas H. LEE, "The design of CMOS radio-frequency integrated circuits,"

Cambridge, U. K. : Cambridge University Press, 1998.

[10] Bosco Leung, "VLSI for Wireless Communication," Prentice Hall Co., 2002.

[11] I. D. Robertson, and S. Lucyszyn, "RFIC and MMIC design and technology," *The institution of Electrical Engineers*, the United Kingdom, 2001.

[12] H. Koizumi, S. Nagata, K. Tateoka, K. Kanazawa, and D. Ueda, "A GaAs Single balanced mixer MMIC with built-in active balun for personal communication systems," *IEEE 1995 Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp. 77-80, 1995.

[13] J. Lin, C. Zelley, O. Boric-Lubecke, P. Gould, and R. Yan, "A silicon MMIC active balun/buffer amplifier with high linearity and low residual phase noise," *2000 IEEE MTT-S International Microwave Symposium Dig.*, vol. 3, pp. 1289-1292, 2000.

[14] A. H. Baree, and I. D. Robertson, "Monoliyhic MESFET distributed baluns based on the distributed amplifier gate-line termination technique," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 188-195, Feb. 1997.

[15] M. Kawashima, T. Nakagawa, and K. Araki, "A novel broadband active balun," *33rd European Microwave Conference - Munich*, vol. 2, pp. 495-498, 7-9 Oct. 2003.

[16] M. Rajashekharaiah, P. Upadhyaya, D. Heo, and Emery Chen, "A new 0.25um CMOS on-chip active balun with gain controllability for 5GHz DCR," *Southeast conference, 2005. Procedings. IEEE*, pp. 71-74, 8-10 April 2005.

[17] http://www.cic.org.tw/cic_v13/

[18] T. Tsang and M. El-Gamal, "Gain and Frequency Controllable Sub-1 V 5.8 GHz CMOS LNA," *ISCAS 2002*, pp. 795-798, May 2002.

[19] D. J. Cassan and J. R. Long, "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18 um CMOS," *IEEE JSSC*, pp.

427-435, Mar. 2003.

[20] D. Linten et al., "Low Power 5 GHz LNA and VCO in 90 nm RF CMOS," *2004 VLSI Circuits Dig.*, pp. 372-375, Jun. 2004.

[21] T. Manku, G. Beck, and E. J. Shin, "A Low-Voltage Design Technique for RF Integrated Circuits," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, pp. 1408-1413, Oct. 1998.

[22] E. Abou-Allam, J. J. Nisbet, and M. C. Maliepaard, "Low-Voltage 1.9-GHz Front-End Receiver in 0.5-μm CMOS Technology," *IEEE J .Solid State of Circuits*, vol. 36, no. 10, pp. 1434-1443, Oct. 2001.

[23] Andrew N. Karanicolas, "A 2.7-V 900-MHz CMOS LNA and Mixer," *IEEE J. Solid State Circuits*, vol. 31, pp. 1939-1944, Dec. 1996.

[24] B. Razavi, *Design of Analog CMOS Integrated circuits*. New York, NY:McGraw-Hill, 2001.

[25] V. Vidojkovic, J. Tang, A. Leeuwenburgh, and A. H. M. Roermunnd, "A Low-Voltage Folded-Switching Mixer in 0.18-μm CMOS," *IEEE J. Solid State Circuits*, vol. 40, pp. 1259-1264, June, 2005.

[26] C. Hermann *et al*., "A 0.6V 1.6mW transformer based 2.5 GHz down-conversion mixer with 5.4 dB gain and -2.8 IIP3 in 0.13 um CMOS," in *Proc. Radio Frequency Integrated Circuits Symp*. (RFIC), 2004, pp. 35-38.

[27] E. Klumperrink *et al*., "A CMOS switched transconductor mixer," *IEEE J. Solid State Circuits*, vol. 39, pp. 1231-1240, Aug. 2004.