# 國 立 交 通 大 學

# 電信工程學系

# 碩 士 論 文

## 應用於多頻帶正交分頻多工超寬頻系統之
## 全積體化低功率快速鎖定整數型頻率合成器

A Fully Integrated, Low Power, Fast-Locking, Integer-N

Frequency Synthesizer for MB-OFDM UWB System

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中 華 民 國 九 十 五 年 六 月

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# 應用於多頻帶正交分頻多工超寬頻系統之全積體化低功率快速鎖定整數型頻率合成器

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## 摘　　要

本論文中主要提出一個應用於之全積體化低功率快速鎖定整數型頻率合成器，另外還有一個寬頻壓控震盪器與其除頻電路，這兩個電路都是應用於多頻帶正交分頻多工超寬頻系統。

首先，利用台積電 0.18 微米互補式金氧半導體製程來實現一個寬頻壓控震盪器和其除頻電路，可以產生多頻帶正交分頻多工超寬頻系統的第一、第三和第四個頻帶群所需要的八個載波頻率。量測結果如下：可調頻寬為 6122～9149 兆赫茲（壓控震盪器產生）與 3061～3930 兆赫茲（除頻電路產生），在距離一兆赫茲處的相位雜訊為-105.5～-115.1 分貝/赫茲，總功率消耗為 36.63 毫瓦。

接下來也是利用台積電 0.18 微米互補式金氧半導體製程來實現一個低功率快速鎖定整數型頻率合成器，產生多頻帶正交分頻多工超寬頻系統的第三和第四個頻帶群所需要的六個載波頻率。其模擬結果如下：可調頻寬為 6279～9170 兆赫茲，在距離一兆赫茲處的相位雜訊為-109.8～-113.6 分貝/赫茲，寄生雜頻較主頻低-34.2～-55.5 分貝，鎖定時間小於 0.3 微秒，正交相位誤差為 3.1 度，總功率消耗為 46.35 毫瓦。

A Fully Integrated, Low Power, Fast-Locking, Integer-N

Frequency Synthesizer for MB-OFDM UWB System

Student: Shih-Hao Tarng Advisor: Dr. Christina F. Jou

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## ABSTRACT

In this thesis, a low power and fast-locking integer-N frequency synthesizer is introduced. Additionally, a wideband voltage-controlled oscillator (VCO) and its frequency divider are designed. These two circuits are both suitable for MB-OFDM UWB application.

First, the wideband VCO and its frequency divider are demonstrated. They are fabricated in TSMC 0.18 μm CMOS process. They can generate eight carrier frequencies in Band Group #1, #3, and #4. The measurement shows that the tuning range is 6122~9149 MHz from the VCO and 3061~3930 MHz from the divider. Moreover, the phase noise is -105.5~-115.1 dBc/Hz at 1 MHz offset and the total power dissipation is 36.63 mW.

Besides, the low power and fast-locking integer-N frequency synthesizer using TSMC 0.18 μm CMOS process is also described. It provides six carrier frequencies in Band Group #3 and #4. The simulated results are listed: the tuning range is 6279~9170 MHz, the phase noise is -109.8~-113.6 dBc/Hz at 1 MHz offset, the spurious tone is -34.2~-55.5 dBc, the locking time is less than 3 nsec, the I/Q phase mismatch is 3.1°, and total power dissipation is 46.35 mW.

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# Chapter 1
# Introduction

## 1.1 Background and Motivation

In recent years, the demand for the wireless communication is dramatically increasing and the fully integrated monolithic radio transceiver is critical to this application. For this reason, study on radio frequency integrated circuits (RFIC) is ongoing to seek methods for performance improvement. At the same time, the development of advanced CMOS technology with the shrunk channel length is achieving higher cut-off frequency and then drawing more RF designers' attention. Instead of bipolar and GaAs (Gallium Arsenic), *CMOS* is very attractive for RFIC due to the ability of system-on-chip (*SOC*) implementation. In the market of the wireless communication, low power consumption leads to long battery life and becomes a target of portable device design. In addition to this benefit, scaling CMOS technology also satisfies the requirement of reduced cost and smaller size.

In the RF front-end circuits, frequency synthesizers act as a local oscillator (LO) for up/down conversion in the transceiver circuits. In Fig. 1-1, a block diagram of typical transceivers is shown. Besides the frequency synthesizer, it also includes a low noise amplifier (LNA), a power amplifier (PA), mixers, variable-gain amplifiers (VGA), low-pass filters and a T/R switch. The noise performance of frequency synthesizers is very important because adjacent channel signals can cause distortion due to this undesired effect. Moreover, settling time is another significant parameter thanks to channel switching requirement. But there is a trade-off between settling time and spurious tones for a phase-locked loop (PLL)

system. Therefore frequency synthesizers have to be designed with both system and circuit level consideration. It indeed poses a big challenge to meet all these specification.

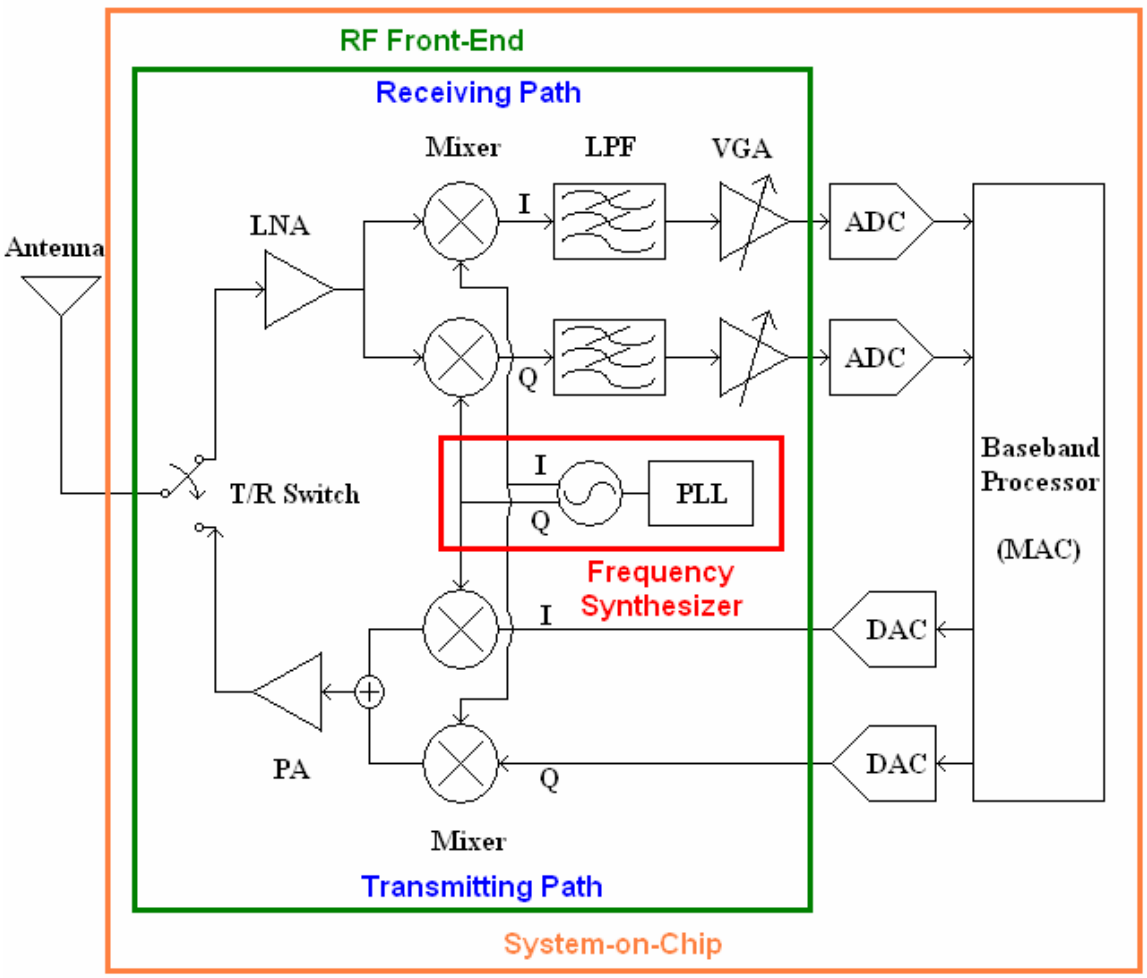



Fig. 1-1 Block diagram of a typical transceiver in wireless communication

Nowadays wireless communication is bringing people more convenience and therefore wireline system is being gradually replaced. Cellular phones, wireless local area networks (WLANs), and Bluetooth are already common in our daily life. Due to the flexibility, the demand for high-speed data transmission is increasing, such as real-time video and wireless USB. But according to Table 1-1, most wireless communication systems support the data rate up to a few tens megabits per second only. For the personal short-range use, Bluetooth is very popular and able to integrate several wireless devices. However, there is a disadvantage of Bluetooth: poor data rate (1 Mbps). In other words, longer time is inevitable when a lot of data are accessed or different wireless devices work simultaneously. In order to raise the data

rate, Ultra Wide-Band (UWB) can be a solution. In fact, UWB communication has been adopted in the military and radar application since 1980. In 2002 the Federal Communications Commission (FCC) has allocated 7500 MHz of spectrum for UWB system in 3.1~10.6 GHz frequency band. This technology promises that the data rate is 110 Mbps at a distance of 10 meters and up to 480 Mbps at a distance of 2 meters in the realistic multi-path environment while very low power is consumed[1][2]. As a result, within a personal area, multimedia consumer products can be connected together without cables.

Table 1-1 Wireless communication system characteristic

| **System** | **Cellular phones** | **WLAN** | | **WPAN** | |
|---|---|---|---|---|---|
| | **WCDMA** | **802.11 b/g** | **802.11 a** | **Bluetooth** | **UWB** |
| **Frequency (GHz)** | 1.92~1.98<br>2.11~2.17 | 2.4~2.4835 | 5.15~5.35 | 2.4~2.48 | 3.1~10.6 |
| **Modulation** | QPSK | QPSK/OFDM | OFDM | GFSK | DSSS or QPSK |
| **Channel Bandwidth** | 5 MHz | 20 MHz | 20 MHz | 1 MHz | 528 MHz (QPSK) |
| **Data Rate (bit/sec)** | 384 k/2 M | 11/54 M | 54 M | 1 M | 110/480 M (QPSK) |

There are two proposals for UWB system: DS-CDMA (Direct-Sequence Code Division Multiplexing Access) and MB-OFDM (Multi-Band Orthogonal Frequency Division Multiplexing). Both proposals have their own supporters and IEEE still have not concluded the final standard. DS-CDMA uses a sequence of Gaussian monocycle pulses which their spectrum is spread in the 3.1~10.6 GHz bandwidth. MB-OFDM divides the whole spectrum into five band groups. According to Fig. 1-2, four band groups contain three bands each while Band Group #5 comprises two only. The Band Group #1 is considered as mandatory and the

remaining band groups are left as optional to enable expansion of the system capabilities. In addition, all carrier frequencies are 528 MHz apart from each other[3]. The benefits from adopting MB-OFDM are robustness in multi-path fading channel, good spectral efficiency, inherent resilience to narrowband RF interference, and spectral flexibility for the emerging wireless standards[4]. Recently, Bluetooth SIG (Special Interest Group) announced that MB-ODFM UWB is chosen for the next generation of Bluetooth. Due to many advantages and better market development, circuits in this thesis are suitable for MB-OFDM UWB proposal.

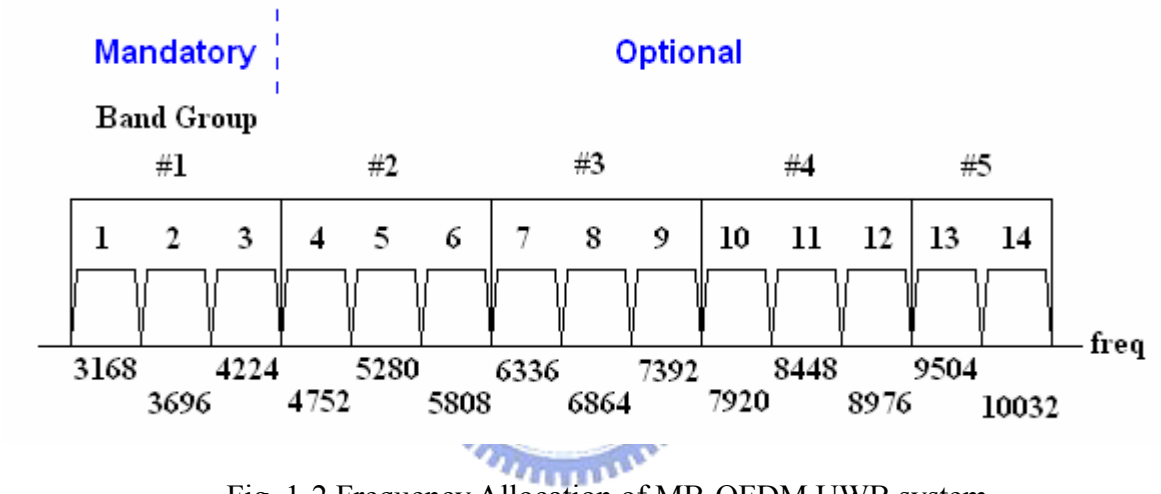



Fig. 1-2 Frequency Allocation of MB-OFDM UWB system

## 1.2 Specification of the Frequency Synthesizer

As mentioned in the previous section, the frequency synthesizer is a significant block in the RF frond-end circuits. Here it will be demonstrated in detail. Ideally only the wanted signal is up/down-converted into the IF band by the pure LO signal. But in the real case, two undesired effects reduce the signal-to-noise ratio (SNR) of the wanted signal. One is phase noise which is from the noise in the oscillator itself. Another is spurious tone which is from the rest parts of the frequency synthesizer. The most important portion is from the charge pump due to the switching at a frequency equal to the reference signal. Therefore the

switching noise modulates the oscillator and up-converts into two sides of the carrier. The phase noise of the LO signal can down-convert the unwanted signal into the IF band and pollute the wanted signal. This phenomenon is shown in Fig. 1-3. Also, the spurious tone affects the IF signal in a similar way in Fig. 1-4. As a result, the output of the frequency synthesizer should be sharp enough with lower spurious tones.

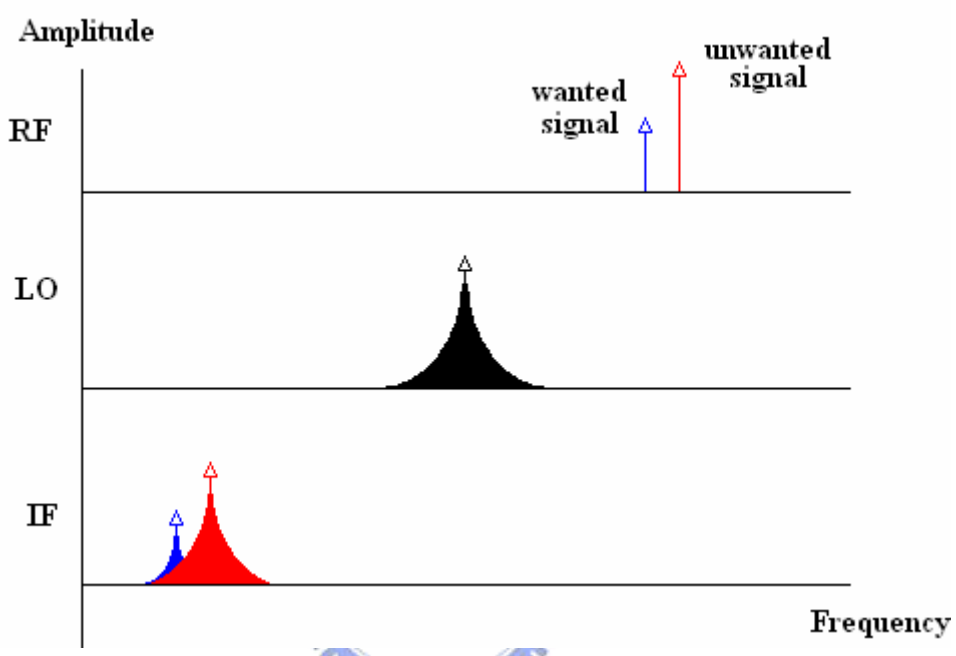



Fig. 1-3 Non-ideal LO in the receiving path

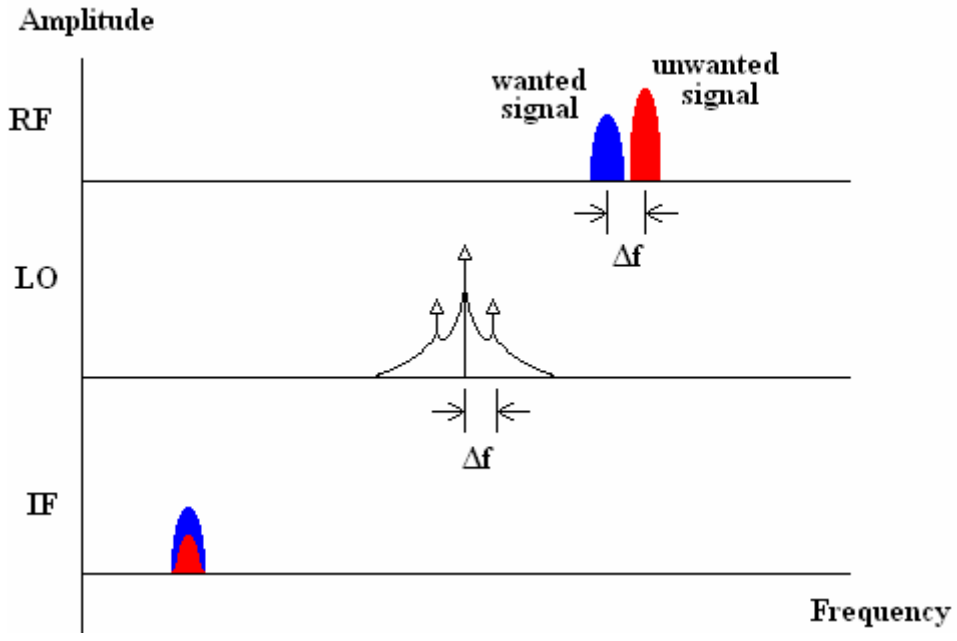



Fig. 1-4 Spurious tone in the receiving path

According to [3] and [5], the frequency synthesizer specification can be calculated under

the condition of a 480 Mbps data transmission in additive white Gaussian noise (AWGN) channel. For a packet error rate of 8% with a 1024-byte packet, the target bit error rate (BER) is $10^{-5}$ when using a coding rate R=3/4. The required phase noise performance is expressed in Eq. ( 1-1 ).

$$L\{\Delta f\} = \frac{1}{\pi} \cdot \frac{\beta}{(\Delta f)^2 + \beta^2} \qquad (1\text{-}1)$$

β is the 3-dB bandwidth of the PSD for a locked PLL and equals to 7 kHz with those given parameters above. Therefore the phase noise has to be smaller than -86.5 dBc/Hz at 1 MHz offset. As for another undesired effect, if the degradation in the sensitivity is less than 0.1 dB, the spurious tone that appears at frequencies corresponding to other bands must be less than -24 dBc. Additionally the phase mismatch between I and Q channels needs to be within 5° for smaller than 0.6 dB of the degradation in the sensitivity. There is extra requirement that makes the frequency synthesizer for MB-OFDM UWB system different from the widely explored PLL-based ones for the conventional wireless communication: the time to switch between different carrier frequencies should be less than 9.47 nsec[3]. This characteristic calls for other type of frequency generation architecture. All the mentioned specifications are summarized in Table 1-2.

Table 1-2 Summary of the synthesizer specification

| | |
|---|---|
| **Band Spacing** | 528 MHz |
| **Phase noise @ 1 MHz offset** | < -86.5 dBc/Hz |
| **Spurious tone** | < -24dBc |
| **I/Q phase mismatch** | < 5° |
| **Switching time** | < 9.47 nsec. |

## 1.3 Thesis Organization

In this thesis, one fully integrated integer-N type frequency synthesizer and one wide tuning range voltage-controlled oscillators (VCO) are realized in TSMC RF 1P6M 0.18 μm

CMOS technology.

Chapter 2 will introduce a multi-band voltage-controlled oscillator and its frequency divider. The characteristic of very wide tuning range supports for MB-OFDM UWB system. Both the simulation and the measurement result are discussed.

Chapter 3 will introduce a fully integrated, fast-locked, and low power integer-N frequency synthesizer for MB-OFDM UWB wireless communication. The architecture will be discussed and compared to other synthesizers for the same application. The simulation of each building block is also presented.

Finally, Chapter 4 will give the summary and conclusions of these circuits. Also the future work will be mentioned.

# Chapter 2
# Wideband Voltage-Controlled Oscillator and Its Frequency Divider for MB-OFDM UWB system

In this chapter, a wide tuning range voltage-controlled oscillator (VCO) and a divider-by-2 circuit are combined together to fulfill a local oscillator for the UWB system application. Besides, a 2-to-1 multiplexer is used to select which path the output signal is from. This circuit is implemented in TSMC RF 1P6M 0.18 μm CMOS technology and fabricated in February 2006. In the following sections, three blocks of this circuit will be explained individually. In addition, both the simulation and measurement results will also be discussed.

## 2.1 Circuit Design Consideration

In MB-OFDM UWB system, carrier frequencies are distributed in a spectrum of 3.1~10.6 GHz and with 528 MHz apart from each other. To meet this specification a voltage-controlled oscillator is necessary to have very wide tuning range. However, it's difficult for LC-VCO to cover such a wide range. Therefore a 6~9 GHz VCO and its frequency divider are designed to provide carrier frequencies for Band Group #1, #3 and #4 in MB-OFDM UWB system[3]. The Band Group #2 is bypassed because occupied by 802.11a and HiperLAN devices. The architecture is shown in Fig. 2-1.

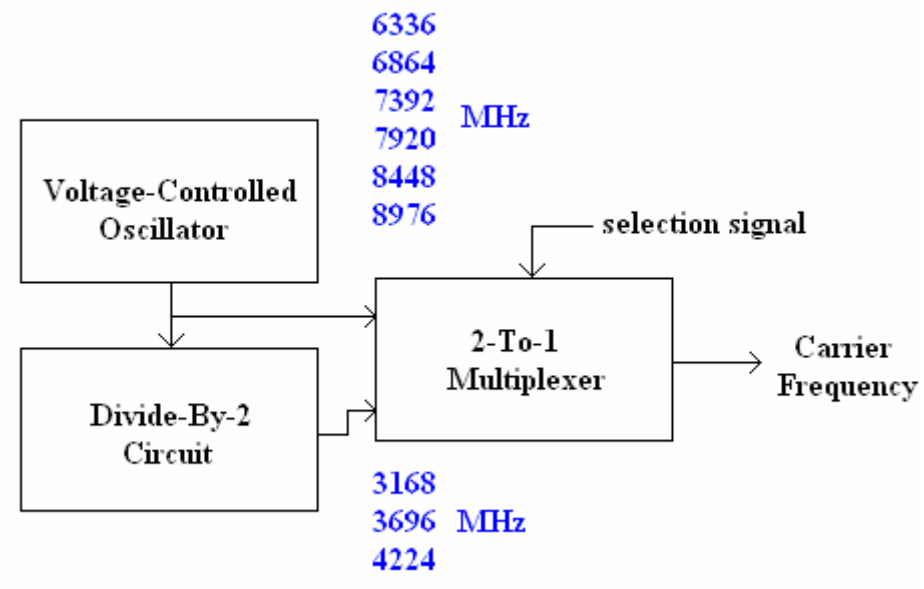



Fig. 2-1 Architecture of VCO and its divider

### 2.1.1 Multi-Band Voltage-Controlled Oscillator

The model of LC-resonant oscillators is shown in Fig. 2-2. The oscillation frequency is decided by the equivalent inductance $L_{eq}$ and capacitance $C_{eq}$ in the tank. For the purpose of frequency tuning, it is common to use varactors which can vary $C_{eq}$ in LC-resonant oscillators. The tuning range has to be very wide to meet the UWB system specification. Unfortunately the noise on the control voltage translates into phase noise and wider tuning range makes this problem more serious. Moreover, the size of the varactors has to be increased and the nonlinearity of larger varactors converts more amplitude noise into phase noise. Therefore, the SCA (Switched-Capacitor-Array) is added to avoid using large varactors[6][7]. Another advantage of SCA is that MIM (metal-insulator-metal) capacitors have a higher Q-value (about 1000) than varactors do. Due to this SCA design characteristic, the noise performance is improved. Fig. 2-3 shows the schematic of this multi-band VCO.

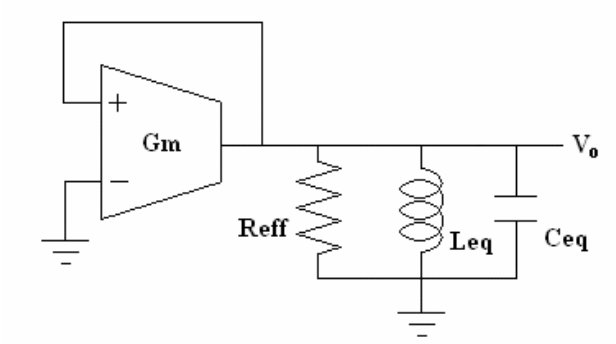



Fig. 2-2 Model of the ideal LC-resonant oscillator

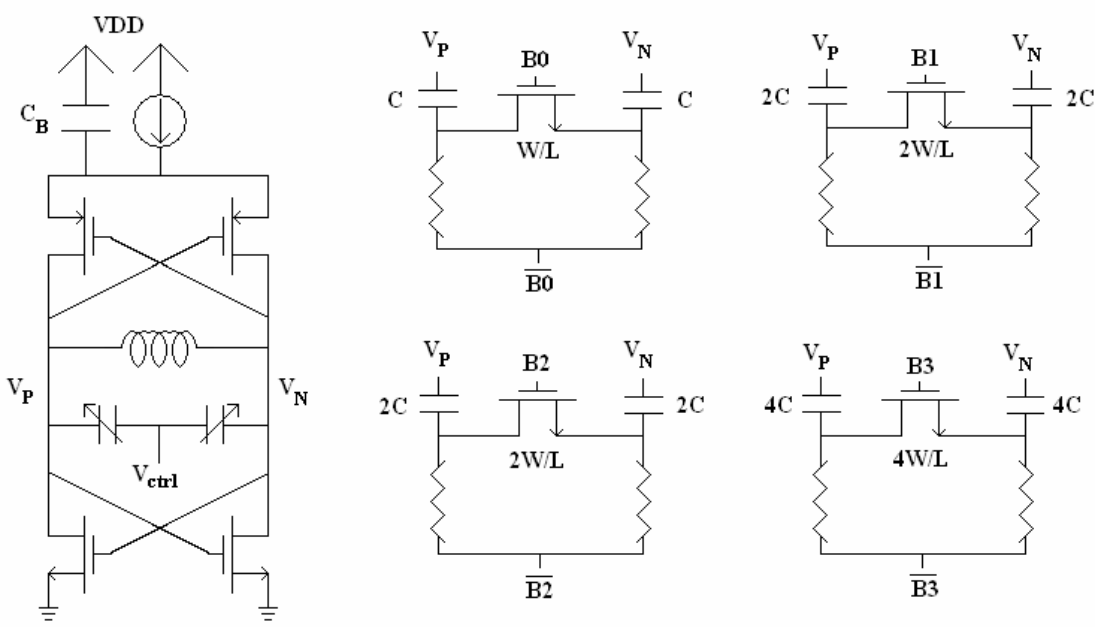



Fig. 2-3 Voltage-controlled oscillator and the switched-capacitor-array

This VCO adopts a complementary cross-coupled negative-gm configuration which has several benefits: (1) only one inductor is needed and large chip area is saved (2) smaller voltage drop across the MOS transistors reduces the effect of velocity saturation in the short channel regime (3) the complementary structure offers higher trans-conductance for a given current, which results in fast switching of the cross-coupled pair (4) the output swing is more symmetry to alleviate the noise up-conversion effect and then phase noise performance is improved[8]. In addition, the current source is in parallel with a capacitor which provides a path to remove the noise disturbance from the current source. For symmetry the capacitor is actually placed at both sides of the current source.

The SCA (switched-capacitor-array) is formed with four pairs of binary-weighted MIM capacitors and four MOS transistors as digital-control switches. But actually the term 2C is replaced for the original term 8C because the bandwidth is already sufficient and using larger capacitors means increasing the load. The SCA provides coarse tuning while the varactors are in charge of fine tuning. In other words, the digital-control signal (B0, B1, B2, and B3) decides that which band the oscillation frequency is in and then analog-control voltage (Vctrl) controls the actual oscillation frequency. According to the rule mentioned above, the requirement for varactors is relaxed because the varactors are not responsible for the whole bandwidth. Fig. 2-4 shows the SCA modification. The MOS switches are not directly connected to the ground, and instead they are connected to both capacitors. This topology can avoid the substrate noise coupling into the tank and halve the number of the MOS switches. Therefore the on-resistance can be reduced and phase noise is improved. The inverted digital-control signals assure that both gate-source and gate-drain junctions are reverse-biased in the OFF state and vice versa[9]. As a result, the effective capacitance of SCA is:

$$C_{eff} = \sum_{i=0}^{3} B_i \cdot \frac{C_i}{2} \qquad (2\text{-}1)$$

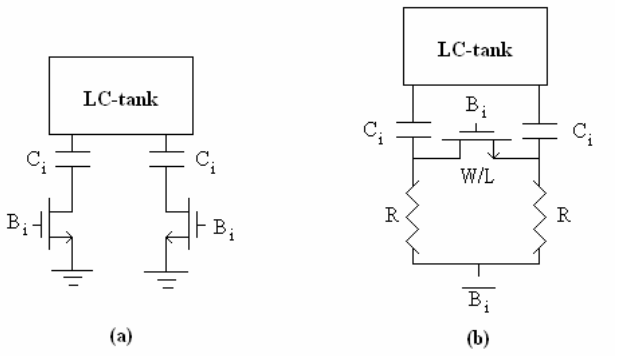



Fig. 2-4 (a) The conventional SCA and (B) the adopted SCA in this circuit

According to Fig. 2-2, the topology of LC-resonant oscillators is positive feedback. For the sake of stable oscillation, the trans-conductance has to be large enough to restore energy dissipated in the resistance of the LC-tank. In other words, the impedance of the active network should be equal to $-R_{eff}$ and the unity loop gain is achieved[10]. Consequently, the

oscillation frequency and required trans-conductance are:

$$f_O = \frac{1}{2\pi \cdot \sqrt{L_{eq} \cdot C_{eq}}} \quad (2\text{-}2)$$

$$G_m = \frac{1}{R_{eff}} \quad (2\text{-}3)$$

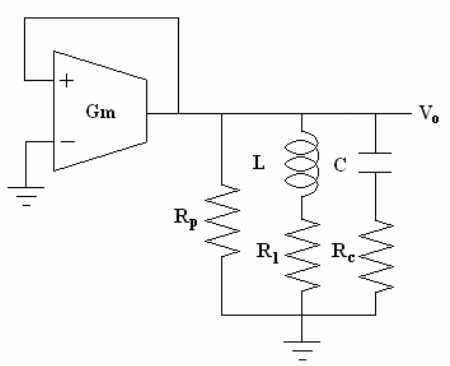



Fig. 2-5 Model of the LC-resonant oscillator with parasitic resistance

In regard to low power consumption, the bias current is supposed to be small and then trans-conductance shrinks. As a result, the bias current should be chosen carefully. Also the overdrive voltage of the cross-coupled transistors needs prudent consideration to accomplish a good compromise between phase noise, tuning range, and power dissipation. Considering the parasitic resistance and non-ideal passive components in Fig. 2-5, the required trans-conductance can be expressed as

$$G_m = \frac{1}{R_{eff}} = \frac{R_c}{(2\pi \cdot f_O \cdot L)^2} + \frac{R_l}{(2\pi \cdot f_O \cdot L)^2} + \frac{1}{R_p} \quad (2\text{-}4)$$

with $f_o$ the oscillation frequency, $R_c$ the capacitor series resistance, $R_l$ the inductor series resistance, and $R_p$ the parasitic resistance. Moreover, to ensure reliable start-up, the active network has to provide 2~3 times required trans-conductance[10]. Now the bias current can be determined:

$$I_{bias} = 2I_{mn} = 2 \cdot \frac{g_{mn} \cdot V_{OD}}{2} \quad (2\text{-}5)$$

where $I_{mn}$, $g_{mn}$ and $V_{OD}$ are the bias current, trans-conductance, and overdrive voltage of the NMOS transistors in Fig. 2-3. Finally, the phase noise can be found in the following

expression

$$L\{\Delta f\} = \frac{kT \cdot [R_c + R_l + \frac{(2\pi \cdot f_O L)^2}{R_p}] \cdot (1 + A) \cdot (\frac{f_O}{\Delta f})^2}{V_A^2 / 2} \quad (2\text{-}6)$$

where $V_A$ is the amplitude of the output swing, A is the noise contribution factor of the active network (usually equal to or larger than 1), and $\Delta f$ is the offset frequency from the carrier at $f_o$. Through Eq. ( 2-6 ), there is trade-off between power dissipation and phase noise performance. Therefore a power-frequency-normalized (PFN) figure-of-merit (FOM) is often used to compare the performance of VCOs for both power consumption and phase noise[11].

$$FOM = 10 \cdot \log[\frac{kT}{P_{dis}} \cdot (\frac{f_O}{\Delta f})^2] - L\{\Delta f\} \quad (2\text{-}7)$$

In Eq. ( 2-7 ), $P_{dis}$ is the dc power dissipation in the VCO and FOM is often expressed in dB. A greater FOM corresponds to a better oscillator.

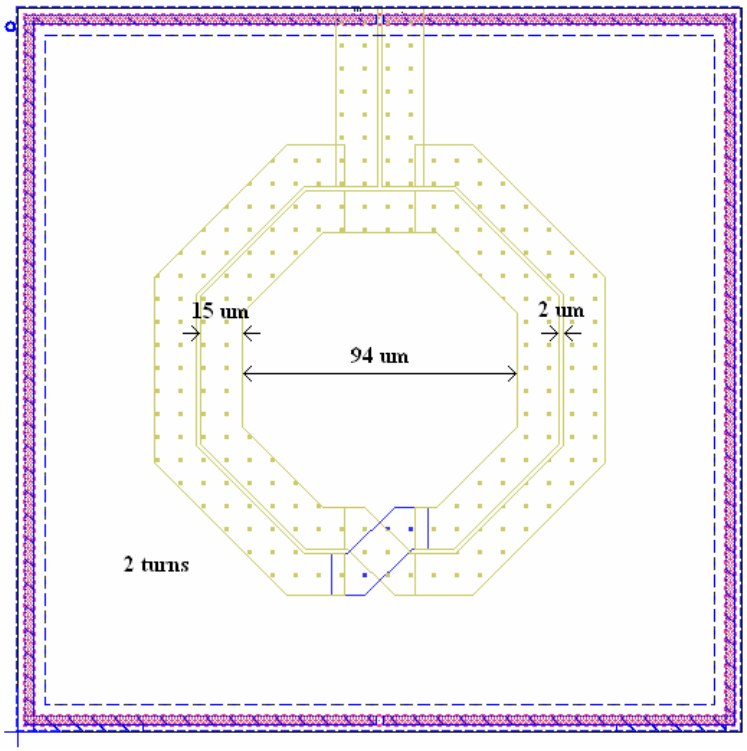
There are several new RF passive elements in TSMC RF 1P6M 0.18 μm CMOS technology. The improvement of the passive element leads to the better circuit performance. In the fully integrated VCOs, the low Q-factor LC-tank is mainly caused by the spiral inductors. Symmetric inductors have higher Q-value thanks to their geometric characteristic. The layout of the symmetric inductor in this circuit and its equivalent lumped circuit are shown in Fig. 2-6 with spacing=2 μm, width=15 μm, radius=47 μm, and 2 turns. The equivalent inductance $L_{eq}$ is about 0.555 nH and the parasitic resistance $R_l$ is 1.8 Ω. In addition, the accumulation-mode MOS varactors is offered with a higher Q-value and larger capacitance variation range than diode varactor[12]. Here Fig. 2-7 shows the layout of the varactor and its equivalent lumped model. The MOS varactor has 17 branches in one group. The equivalent capacitance $C_{eq}$ is about 40.8~153 fF and the parasitic resistance $R_c$ is 6.24 Ω. After considering the SCA, VCO output stage and parasitic effect from the chip layout, the simulated VCO oscillation frequency is around 8.9 GHz. Due to the lumped models of spiral inductor and MOS varactors, the required trans-conductance and bias current can be decided

by Eq. ( 2-4 )and ( 2-5 ).

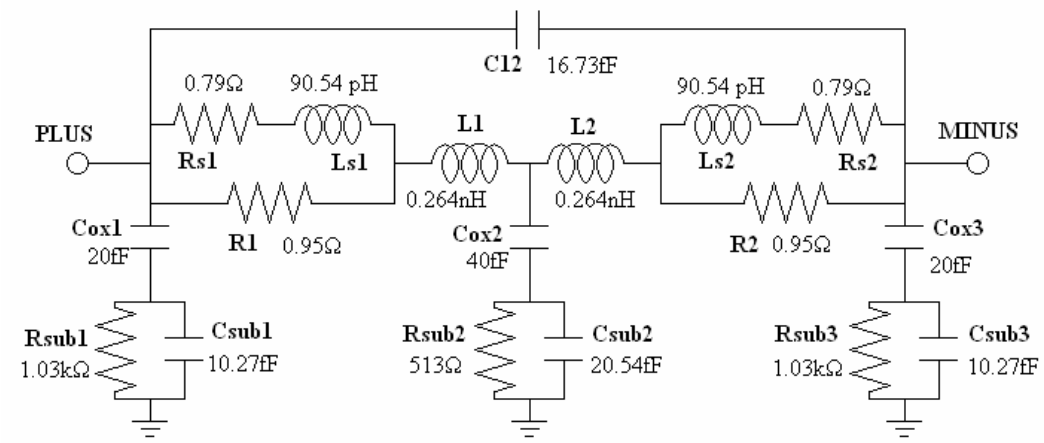
$$G_m = \frac{1}{R_{eff}} = \frac{(6.24+1.8)}{(2\pi \cdot 9G \cdot 0.555n)^2} = 8.16 \quad mA/V$$

$$I_{bias} = 2 \cdot \frac{4.08m \cdot 0.9}{2} = 3.67 \quad mA$$

Besides, it is possible that the $G_m$ and $I_{BIAS}$ are a little bit insufficient owing to omitting some parasitic resistance. But it still provides a good starting point for the design.

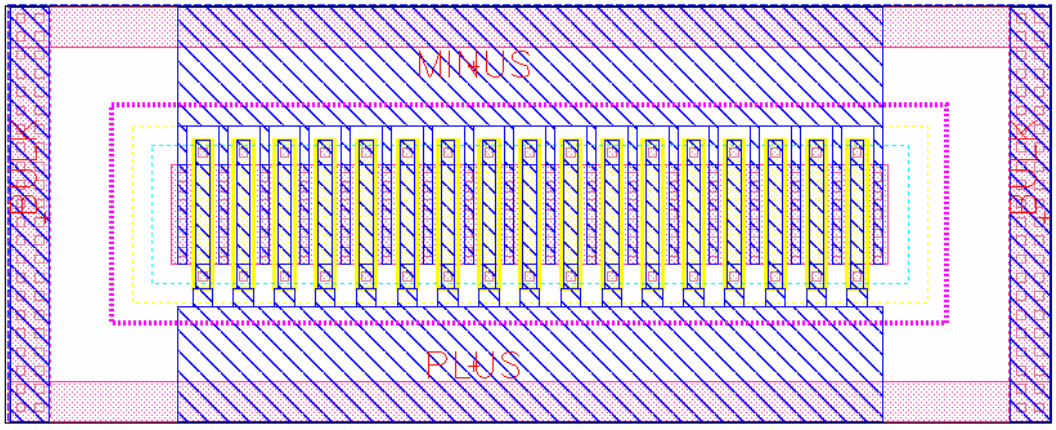



**(a)**

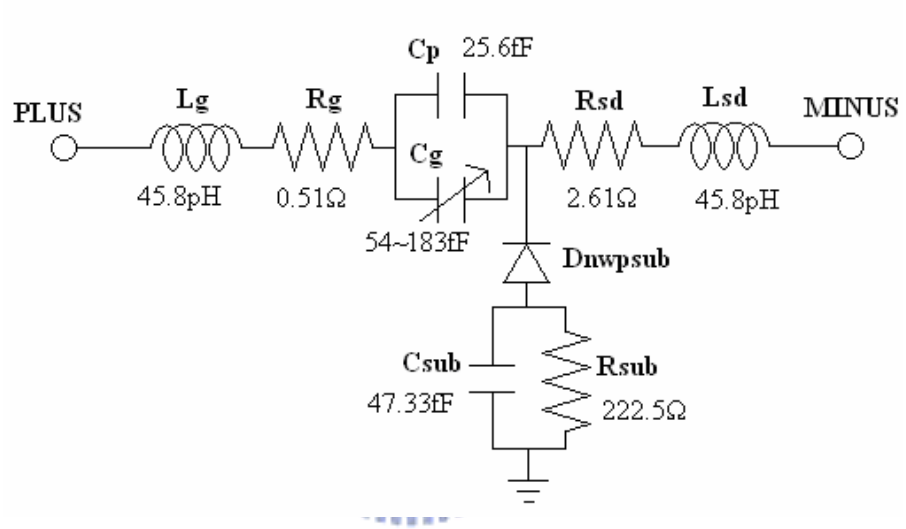



**(b)**

Fig. 2-6 (a) Layout and (b) its lumped model of the symmetric spiral inductor




(a)




(b)

Fig. 2-7 (a) Layout and (b) its lumped model of the MOS varactor

### 2.1.2 High Frequency Divider

Frequency dividers operating at high frequency are one of the key blocks in the RF circuits because dividers must function properly over the required bandwidth and provide enough output swing for the next stage. Three kinds of dividers are often used: digital CMOS logic, current-mode logic (CML), and injection-locked frequency dividers (ILFD)[13]. Digital CMOS logic is seldom used since full-scale swing is needed and the operating frequency is relatively low. Compared with CML, ILFD has lower power consumption with larger area and

narrower locking range. Due to very wide bandwidth of VCO, the CML is chosen in this work[14].

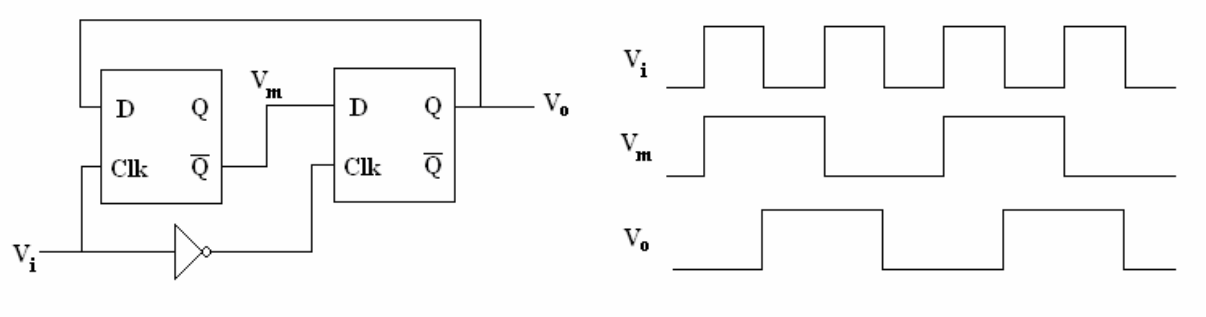



Fig. 2-8 Block diagram of the CML frequency dividers

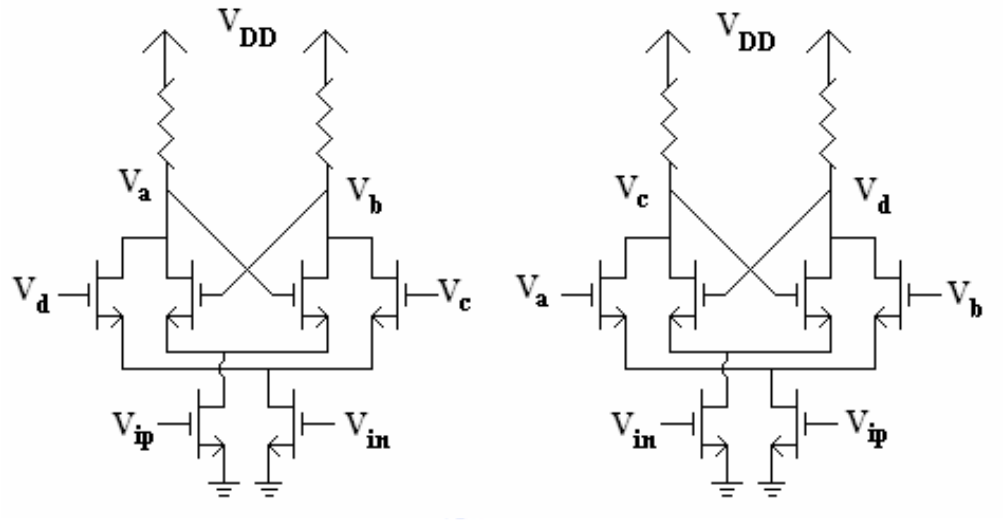
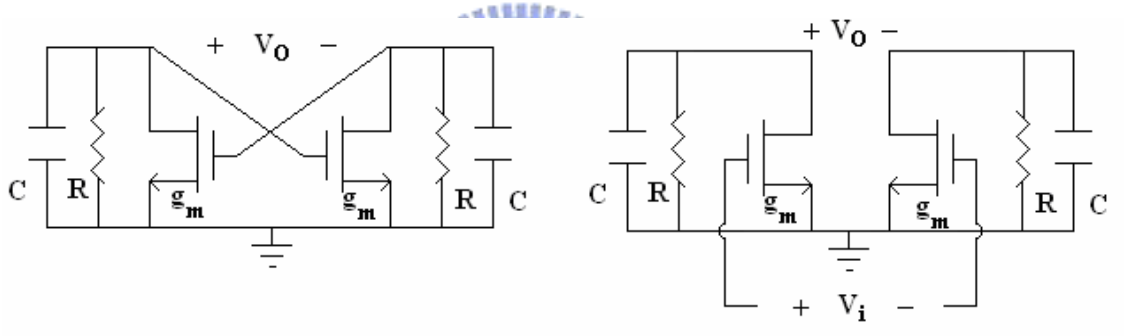



Fig. 2-9 Schematic of the CML frequency dividers

The block diagram of CML frequency dividers is shown in Fig. 2-8. The frequency of both $V_m$ and $V_o$ is half the frequency of $V_i$. Meanwhile the phase difference between $V_m$ and $V_o$ is just 90 degree and quadrature outputs are obtained. In other words, CML is also a kind of quadrature signal generators owing to the characteristic of the output nodes. According to Fig. 2-9, the master and slave D-FFs (D-type flip-flop) are clocked by complementary clocked signals and the differential outputs of LC-VCO in the previous section provide this kind of input signals. Consequently, the inverter in Fig. 2-8 is implemented without adding any circuit. The D-FFs implemented in CML are composed of a clocked differential sensing amplifier pair and inversely clocked latching pair. In contrast with common CML circuits, the bias current source is eliminated to increase the maximum operating frequency about 10 %[15].

Only NMOS transistors are used in this circuit because the drain parasitic capacitance and power dissipation should be minimized. Due to omitting the current source, the bias point of this divider is determined by the DC level of the input signals, the size of the clock transistors and the load resistance. The trans-conductance of clock transistors has to be large and then the small input signals can drive them from the linear region to the saturation region. Therefore the sensitivity to the DC level of input signals is increased. The load resistance is another key parameter since the dominant pole is decided by the load resistance and parasitic capacitance from transistors, interconnection, and next stage. As a result, the load resistance has to be kept small to make the dominant pole high enough and it is inevitable to raise the bias current to assure the next stage of proper DC input level.




(a) (b)

Fig. 2-10 Schematic of (a) the latching pair and (b) the sensing pair

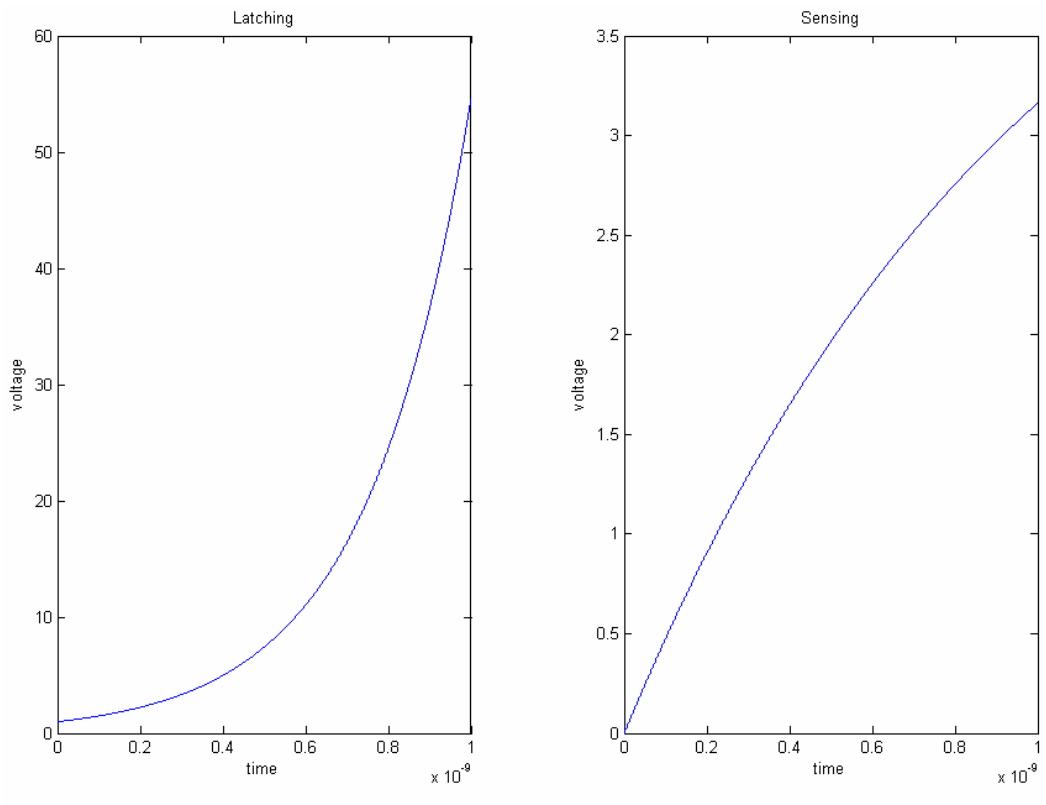



Fig. 2-11 Comparison of amplification in (a) the latching and (b) the sensing

As shown in Fig. 2-10, the latching pair works in positive-feedback regeneration while sensing pair is in common-source configuration.

$$\text{latching pair}: \quad \frac{V_o(t)}{V_o(0)} = \exp\left(\frac{g_m R - 1}{RC} \cdot t\right) \qquad (2\text{-}8)$$

$$\text{sensing pair}: \quad \frac{V_o(t)}{V_i(t)} = g_m R \cdot [1 - \exp(\frac{-t}{RC})] \qquad (2\text{-}9)$$

According to Eq. ( 2-8 ) and ( 2-9 ), Fig. 2-11 is plotted under the same condition. The latching pair boosts the output exponentially while the sensing pair is an approximately linear amplifier. When the trans-conductance of latching pair is large, the latching is fast but changing state is difficult. Additionally, the clock is fed by sinusoidal signal rather than square wave. The grey area is wider between latching and sensing. In consequence the size of the sensing pair transistors has to be a bit greater than the size of the latching pair ones.

### 2.1.3 2-to-1 Multiplexer

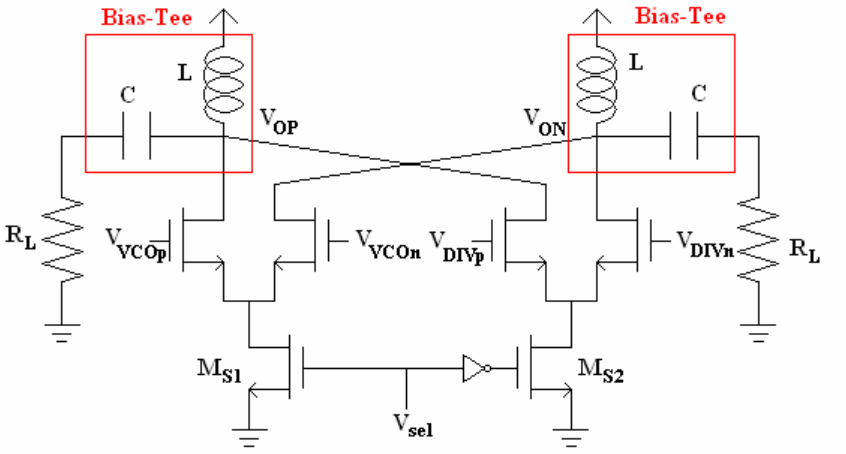



Fig. 2-12 Schematic of the 2-to-1 multiplexer

In the beginning of this chapter, it is mentioned that a multi-band VCO provides carrier frequencies in Band Group #3 and #4 while a frequency divider is in charge of frequencies in Band Group #1 for the MB-OFDM UWB system. As a result, there is a 2-to1 multiplexer to decide that the output is generated from VCO or the divider. Fig. 2-12 shows the schematic of the multiplexer. Again the current source is removed to relax the voltage headroom problem[16]. When $V_{sel}$ is high, $M_{S2}$ is off and the output is only from the VCO. On the contrary, when $V_{sel}$ is low, $M_{S1}$ is off and the output is only from the divider. Because the output signals are spread in a very wide range of spectrum, the gain must be insensitive to the operating frequency. The load inductors and capacitors should be designed as large as possible to alleviate the impedance variation with the frequency. Therefore the bias-tee is chosen as the load impedance. The inductor and capacitor in the bias-tee can be treated as infinitely large at the multi-GHz frequency. For this reason, the load impedance is approximately only $R_L$ (50 ohm). The pure-resistive impedance fulfills a gain without dependency of the operating frequency.

In MB-OFDM UWB system, the channel switching time is about only 9.5 nsec. As a result, the multiplexer must change the output signals in a time less than the required period. Because $M_{S1}$ and $M_{S2}$ work as complementary switches, the length of these two transistors is

kept the minimum value and the width is supposed to be a reasonable value to compromise between parasitic capacitance and trans-conductance.

## 2.2 Chip Layout and Simulation Results

A signal generator for UWB system is designed and optimized through Eldo RF simulator. The whole chip is 0.83×1.12 $mm^2$ and fabricated in TSMC RF 1P6M 0.18 μm CMOS technology. Fig. 2-13 is the layout of this circuit. In order to extract the parasitic effect from the interconnection, Calibre xRC is adopted for the post-simulation. However it is insufficient to consider parasitic capacitance and resistance only. Parasitic inductance accompanies the interconnections in the circuits operating at multi-GHz band. Consequently, Sonnet software is also used to convert critical parts of the layout into s-parameter files and the interconnections are treated as transmission lines. Several parts of the whole chip are processed by Sonnet software and Fig. 2-14 shows one example. Besides, the layout should be kept symmetry to equalize the amplitude of the differential outputs. The power dissipation of each block is listed in Table 2-1.

As shown in Fig. 2-15, the tuning range is 5.97~9.22 GHz (about 42.8% of the center frequency) for the total 10 curves. A particular digital-control signal obtains its corresponding curve. Overlapping between curves is necessary to cover the entire band. In the lower bands, the slopes of these tuning curves and the distances between curves are smaller. The following equation can prove this.

$$f_1 = \frac{1}{\sqrt{LC}} \qquad f_2 = \frac{1}{\sqrt{L(C+\Delta C)}}$$

$$\Delta f = f_1 - f_2 = \frac{1}{\sqrt{LC}}[1 - \frac{1}{\sqrt{(1+\Delta C/C)}}] \cong \frac{1}{\sqrt{LC}}[1-(1-\frac{\Delta C}{2C})] \quad \text{(Assumes } \Delta C << C) \quad (2\text{-}10)$$

$$= \frac{1}{\sqrt{LC}} \cdot \frac{\Delta C}{2C}$$

Due to larger capacitance in the lower bands, Δf becomes smaller. In other words, the oscillation frequencies in the lower band don't vary as much as those in the higher bands.

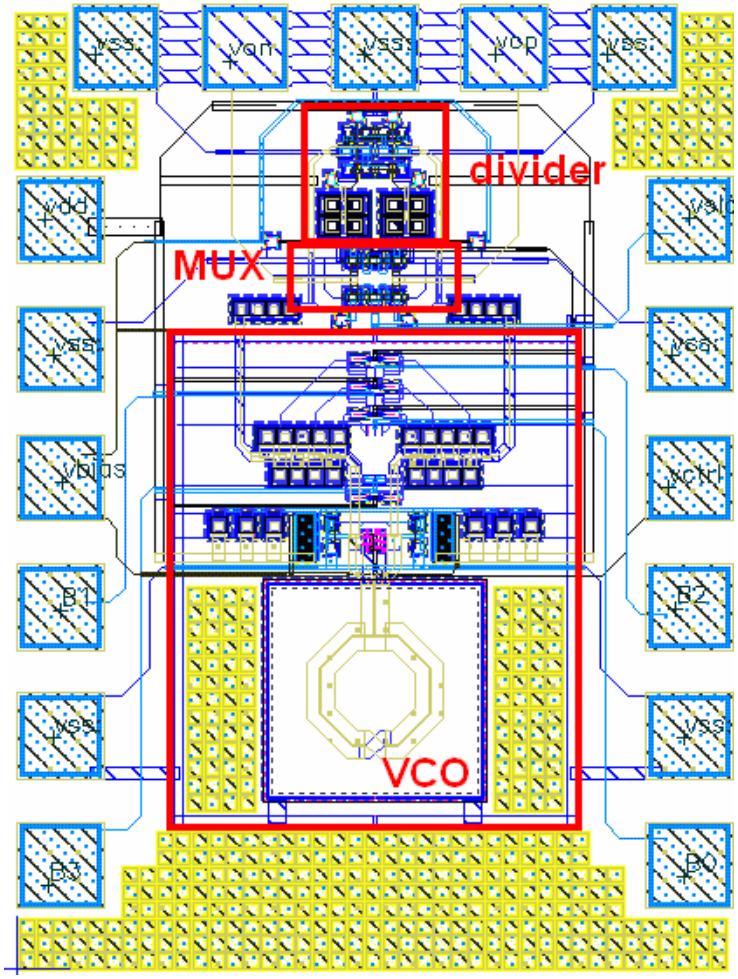
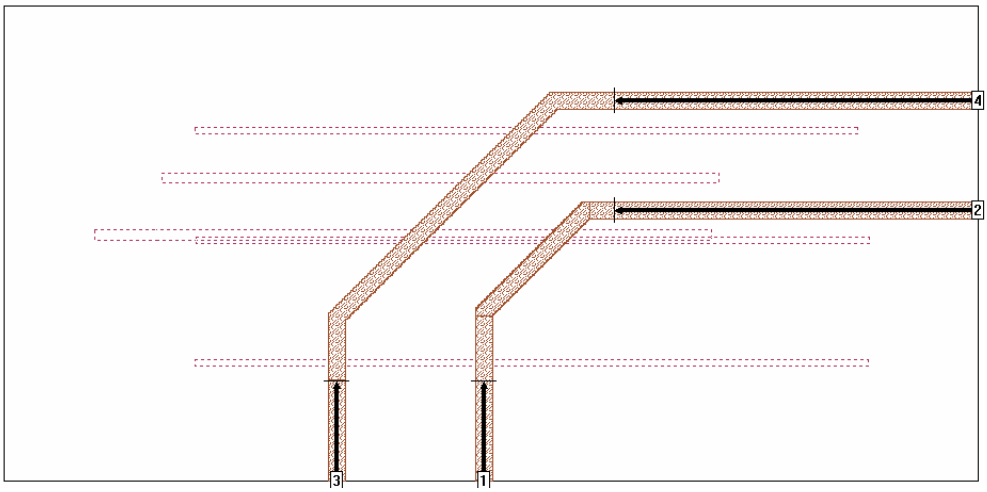
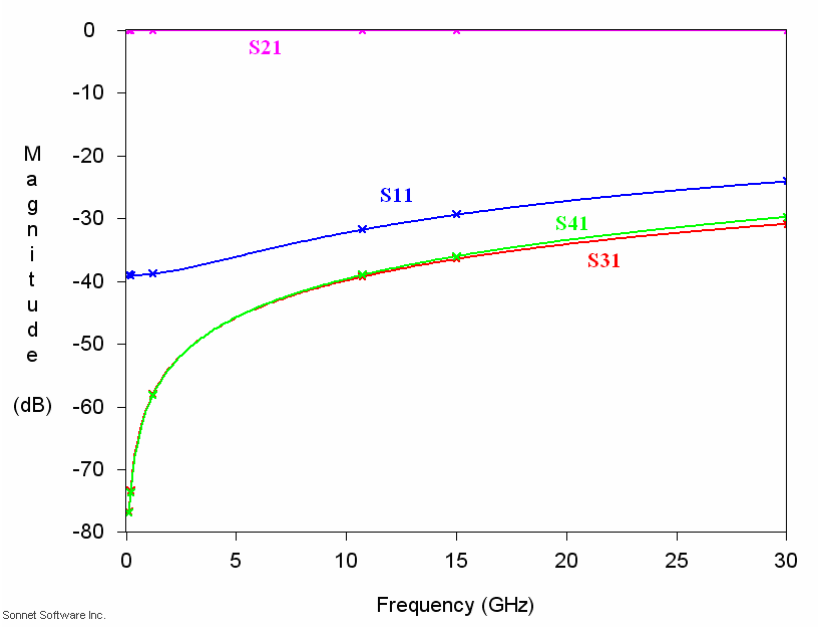



Fig. 2-13 Layout of the whole chip




(a)




(b)

Fig. 2-14 (a) Imported layout and (b) extracted S-parameter in Sonnet software

Table 2-1 Power dissipation of each blocks in this circuit

| | Power | Current |
|---|---|---|
| **VCO** | 7.09 mW | 3.94 mA |
| **divider** | 9.43 mW | 5.24 mA |
| **multiplexer** | 21.39 mW | 11.88 mA |
| **total** | 37.91 mW | 21.06 mA |

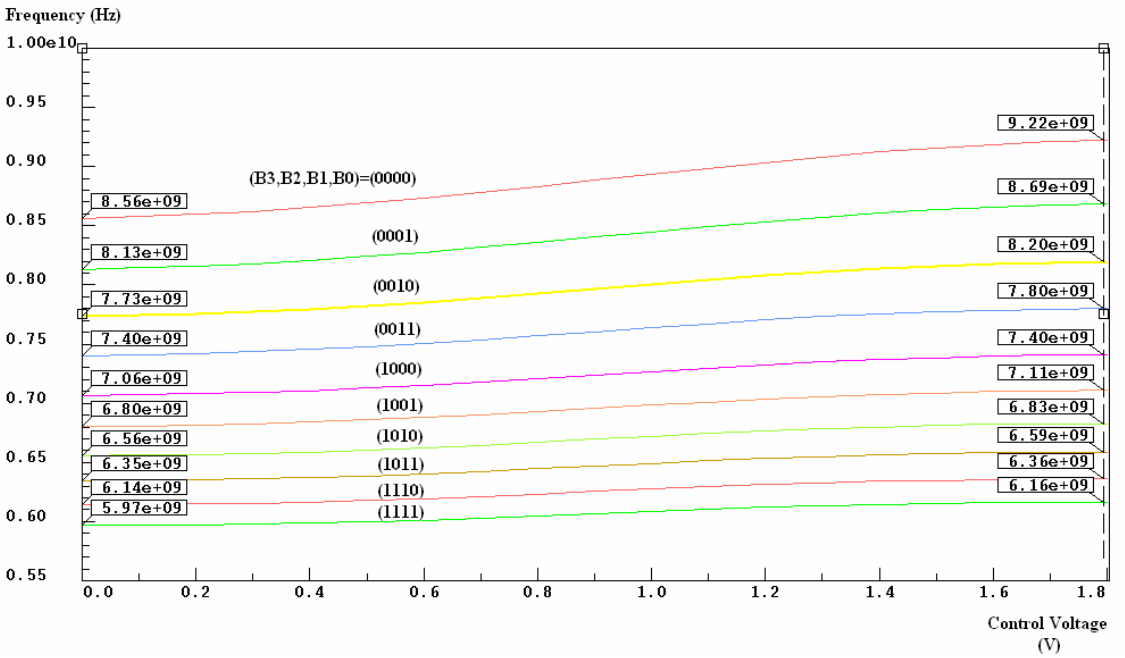



Fig. 2-15 Tuning range curves of VCO with different banks

When the control voltage is 1.05 V with digital input (0,0,0,0), the oscillation frequency is 8.976 GHz. The output swing is 0.95 $V_{PP}$ (3.53 dBm) and the phase noise is -111 dBc/Hz at 1 MHz offset. Through the frequency divider, another signal at 4.488 GHz is also generated. These results are shown in Fig. 2-16 and Fig. 2-17.

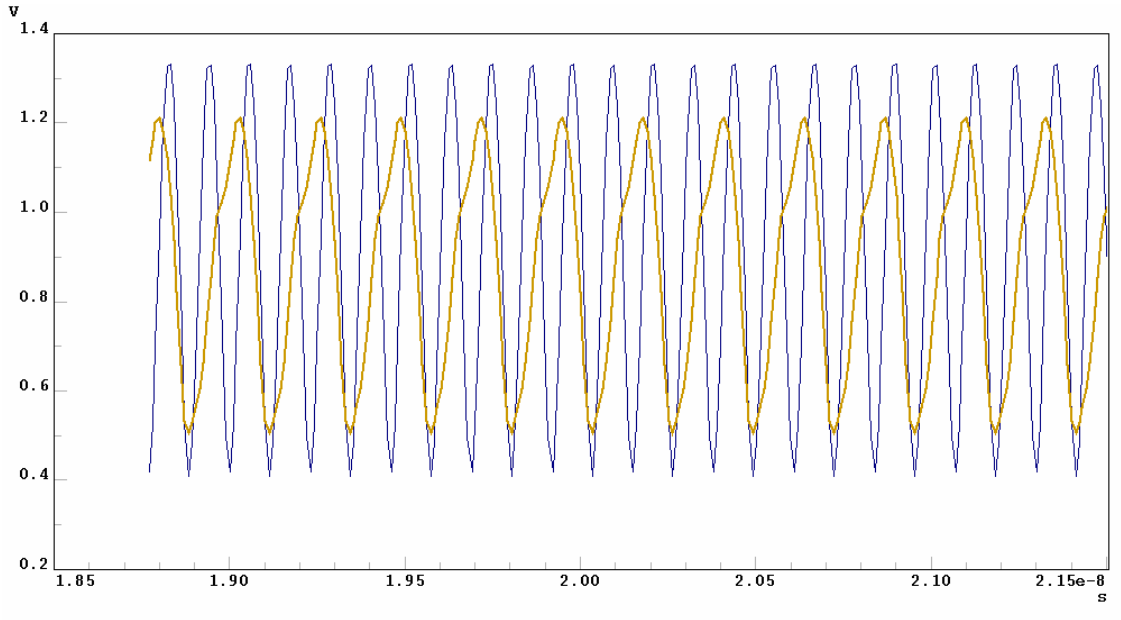



Fig. 2-16 Output waveform of VCO and frequency divider

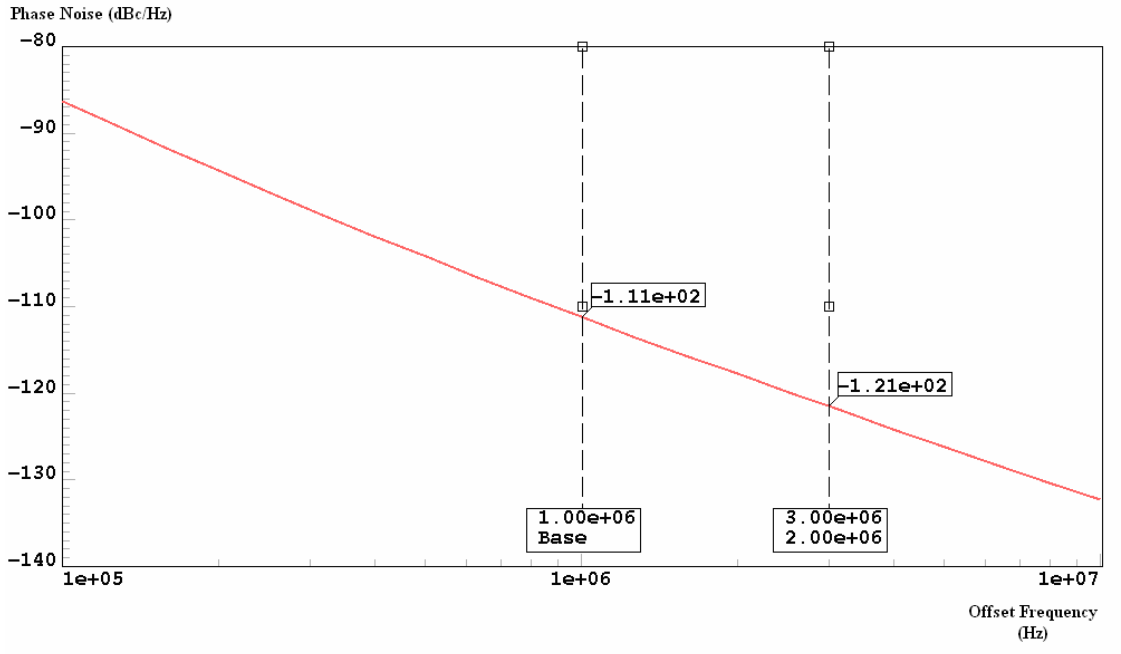



Fig. 2-17 Phase noise with oscillation frequency at 8.976 GHz

When the control voltage is 0.98 V with digital input (0,0,0,1), the oscillation frequency is 8.448 GHz. The output swing is 0.86 $V_{PP}$ (2.67 dBm) and the phase noise is -111 dBc/Hz at 1 MHz offset. Through the frequency divider, another signal at 4.224 GHz is also generated. These results are shown in Fig. 2-18 and Fig. 2-19.

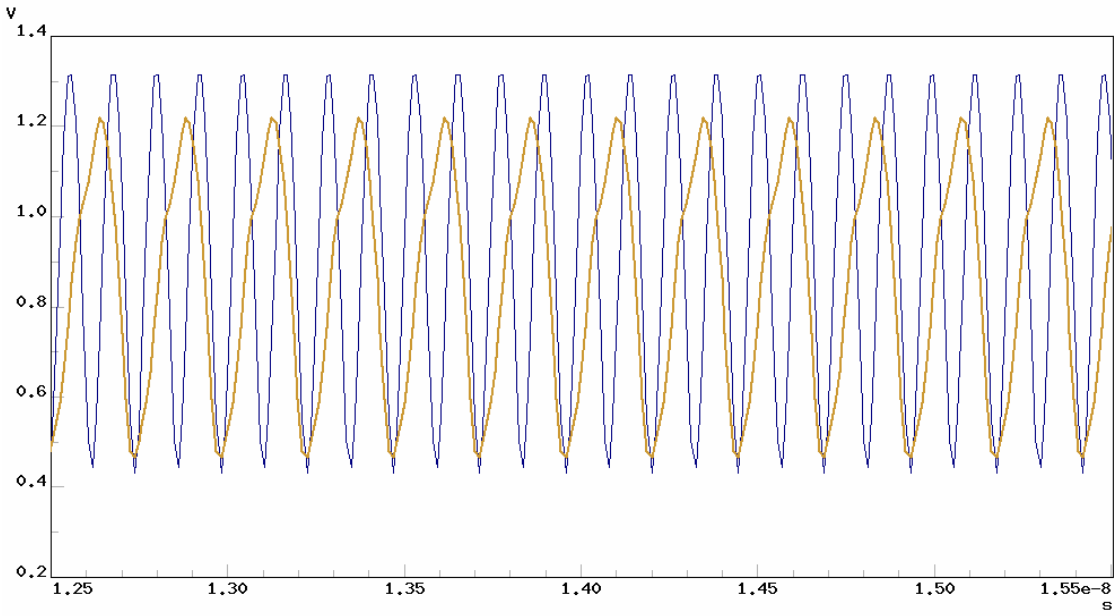



Fig. 2-18 Output waveform of VCO and frequency divider

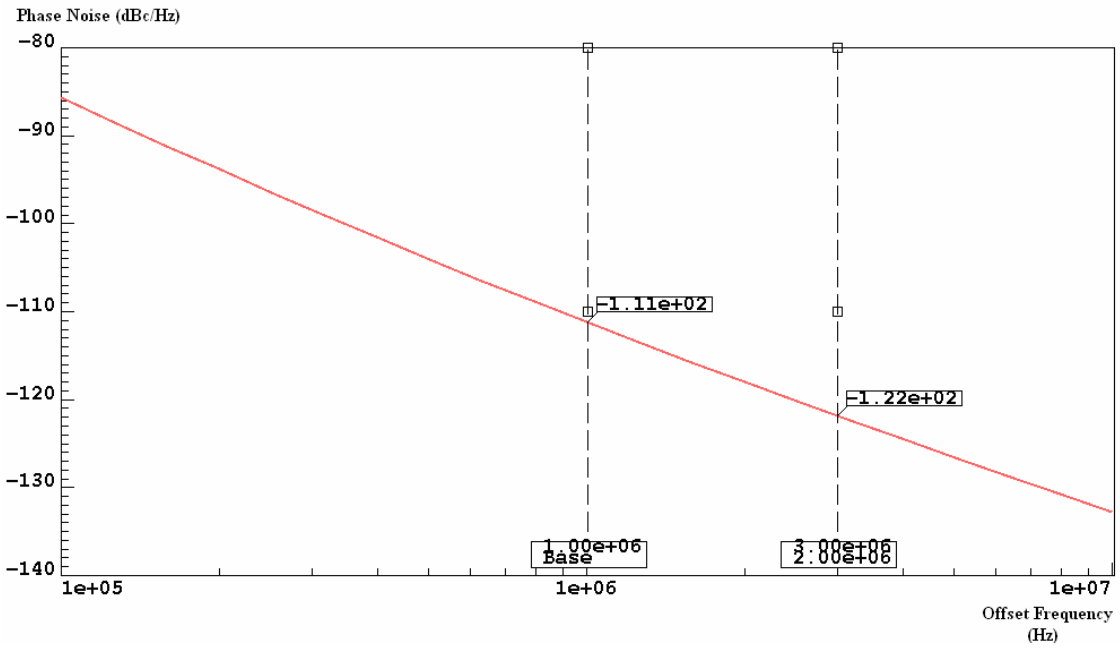



Fig. 2-19 Phase noise with oscillation frequency at 8.448 GHz

When the control voltage is 0.77 V with digital input (0,0,1,0), the oscillation frequency is 7.92 GHz. The output swing is 0.82 $V_{PP}$ (2.26 dBm) and the phase noise is -112 dBc/Hz at 1 MHz offset. Through the frequency divider, another signal at 3.96 GHz is also generated. These results are shown in Fig. 2-20 and Fig. 2-21.

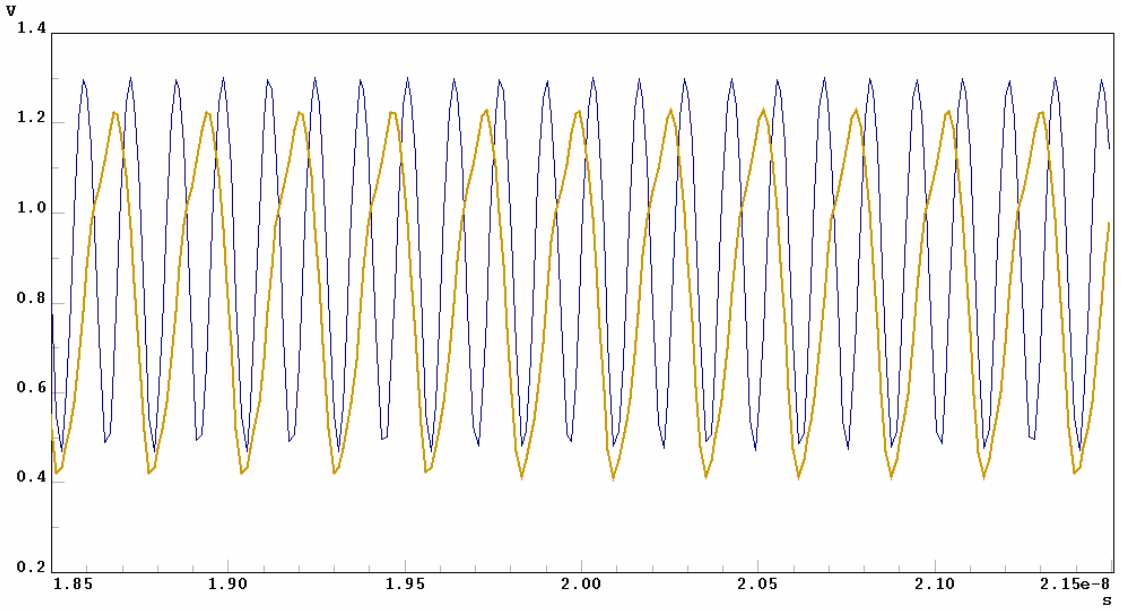



Fig. 2-20 Output waveform of VCO and frequency divider

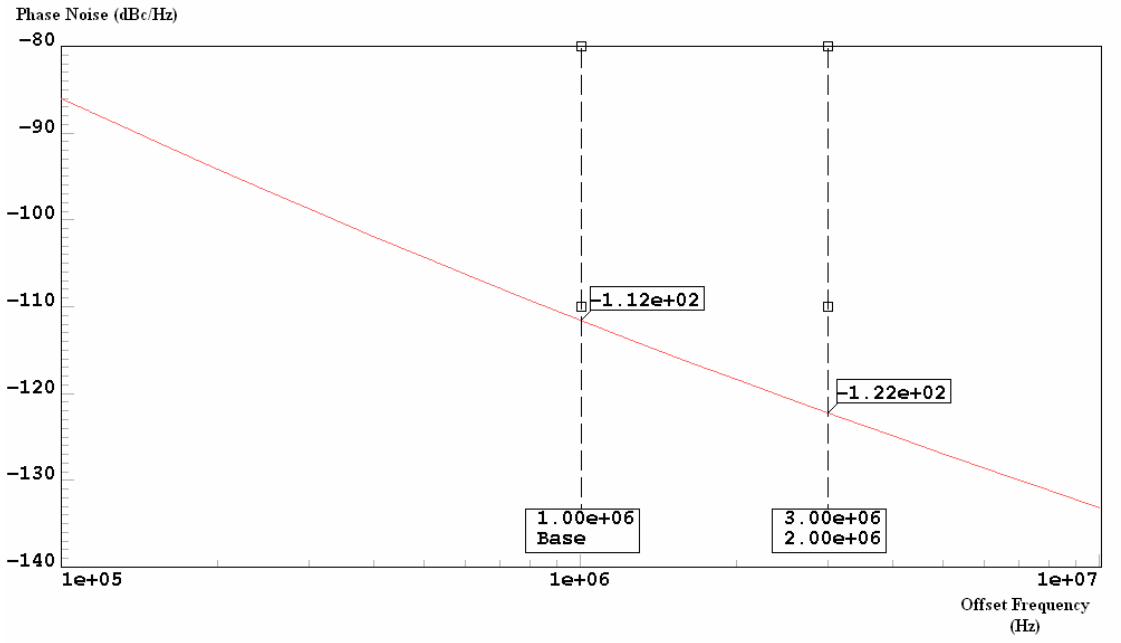



Fig. 2-21 Phase noise with oscillation frequency at 7.92 GHz

When the control voltage is 1.47 V with digital input (1,0,0,0), the oscillation frequency is 7.392 GHz. The output swing is 0.8 $V_{PP}$ (2.04 dBm) and the phase noise is -113 dBc/Hz at 1 MHz offset. Through the frequency divider, another signal at 3.696 GHz is also generated. These results are shown in Fig. 2-22 and Fig. 2-23.

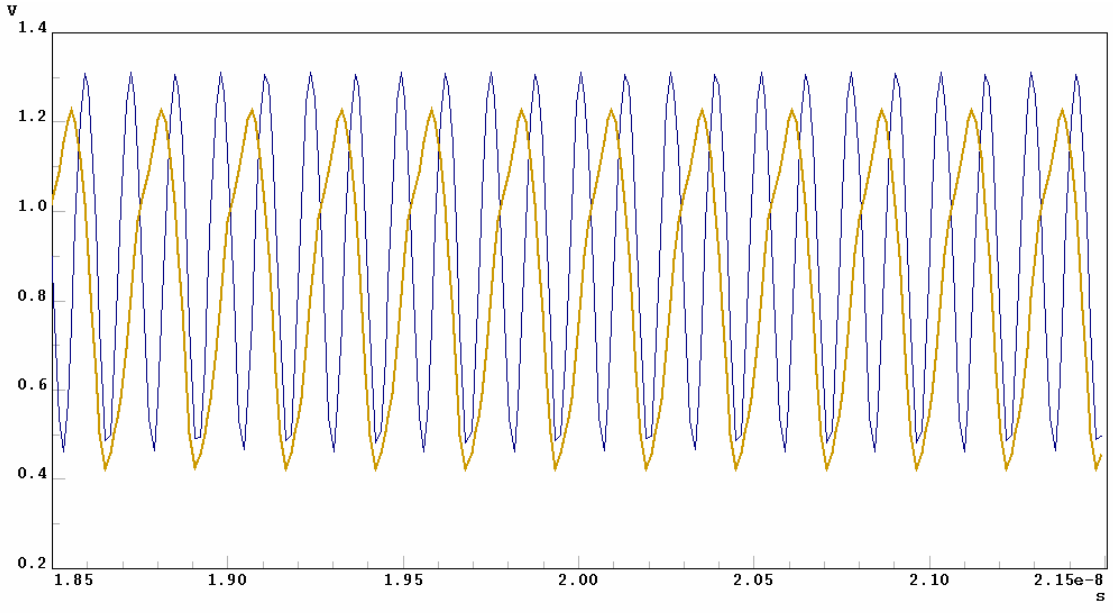



Fig. 2-22 Output waveform of VCO and frequency divider

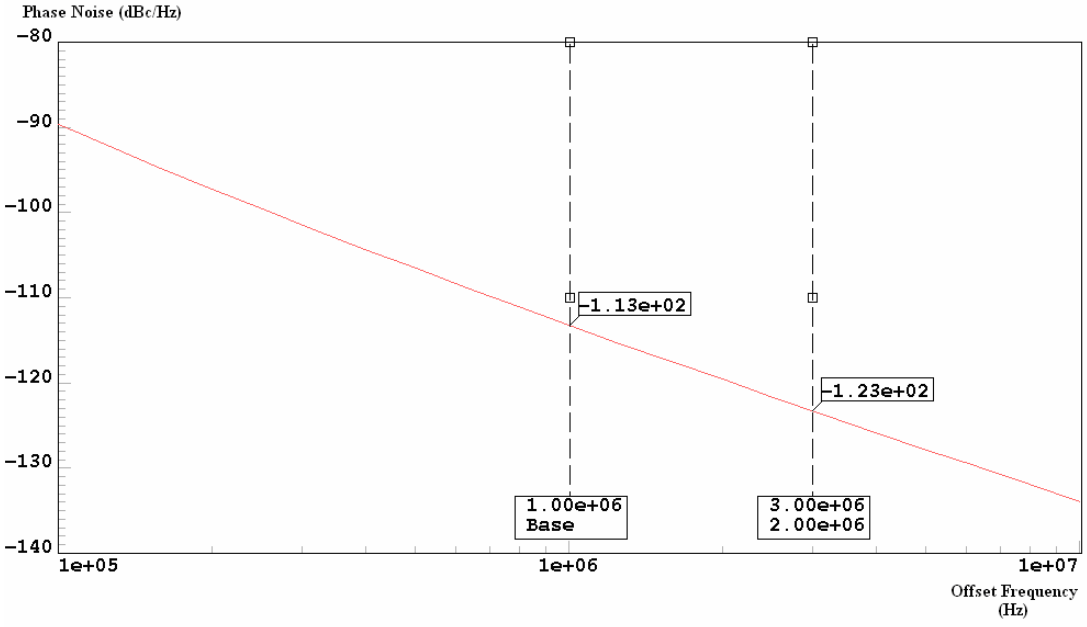



Fig. 2-23 Phase noise with oscillation frequency at 7.392 GHz

When the control voltage is 0.5 V with digital input (1,0,0,1), the oscillation frequency is 6.864 GHz. The output swing is 0.7 $V_{PP}$ (0.88 dBm) and the phase noise is -114 dBc/Hz at 1 MHz offset. Through the frequency divider, another signal at 3.432 GHz is also generated. These results are shown in Fig. 2-24 and Fig. 2-25.

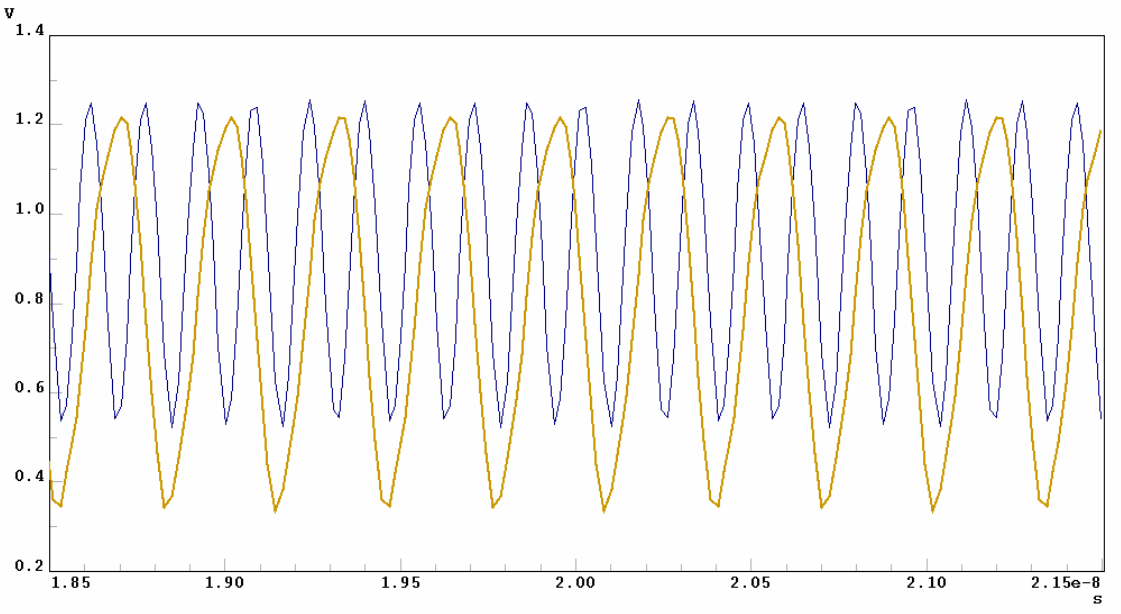



Fig. 2-24 Output waveform of VCO and frequency divider

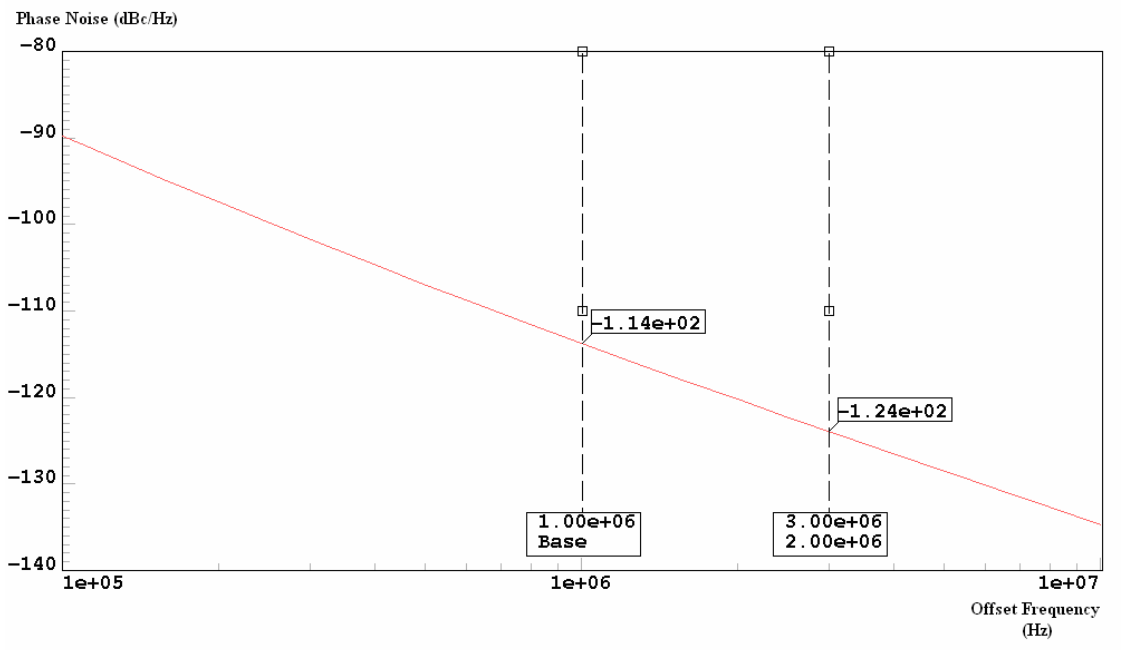



Fig. 2-25 Phase noise with oscillation frequency at 6.864 GHz

When the control voltage is 1.27 V with digital input (1,1,1,0), the oscillation frequency is 6.336 GHz. The output swing is 0.64 $V_{PP}$ (0.1 dBm) and the phase noise is -113 dBc/Hz at 1 MHz offset. Through the frequency divider, another signal at 3.168 GHz is also generated. These results are shown in Fig. 2-26 and Fig. 2-27. Finally, the output power and the phase noise are listed for all carrier frequencies in Table 2-2.

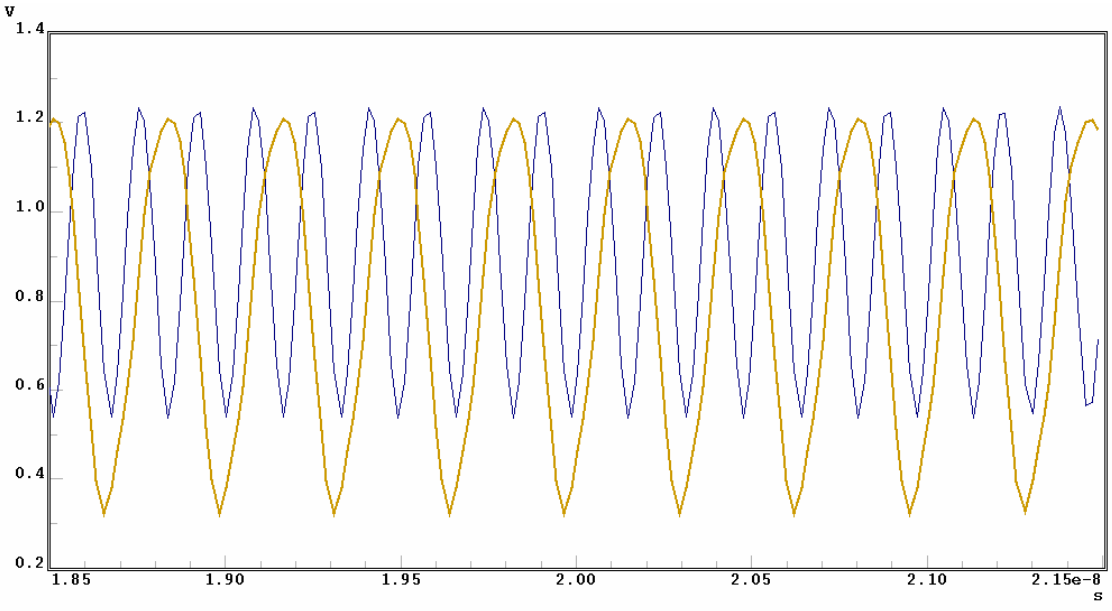



Fig. 2-26 Output waveform of VCO and frequency divider

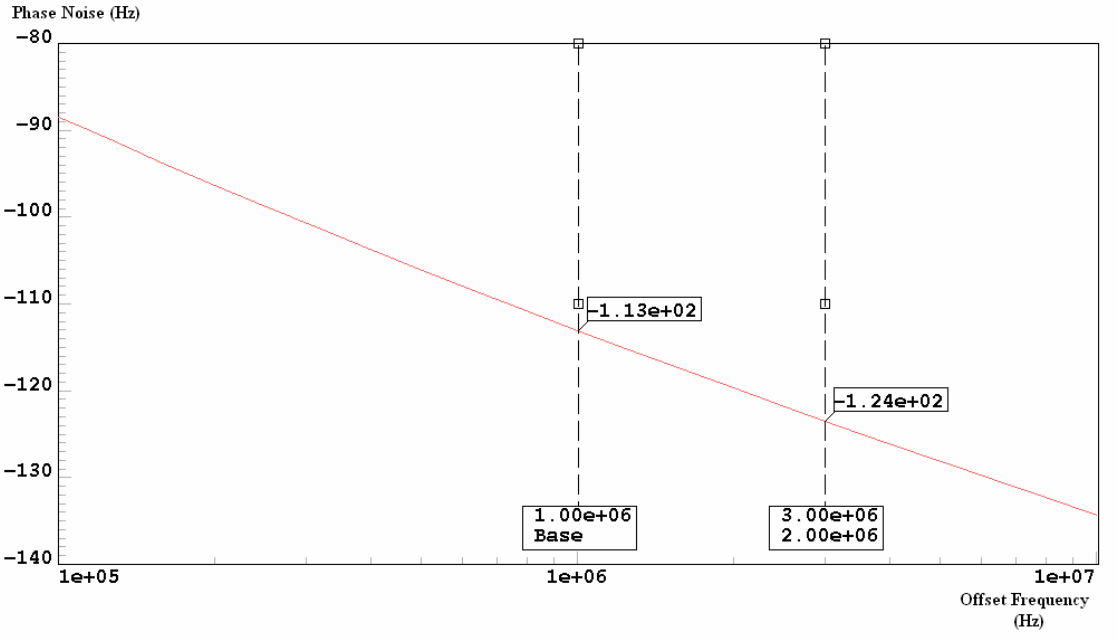



Fig. 2-27 Phase noise with oscillation frequency at 6.336 GHz

Table 2-2 Output power and phase noise performance of the carrier frequencies

| Carrier Frequency | Output Power | Phase noise @ 1MHz | FOM |
|---|---|---|---|
| 6.336 GHz | 0.1 dBm | -113 dBc/Hz | 180.53 |
| 6.864 GHz | 0.88 dBm | -114 dBc/Hz | 182.23 |
| 7.392 GHz | 2.04 dBm | -113 dBc/Hz | 181.87 |
| 7.920 GHz | 2.26 dBm | -112 dBc/Hz | 181.46 |
| 8.448 GHz | 2.67 dBm | -111 dBc/Hz | 181.03 |
| 8.976 GHz | 3.53 dBm | -111 dBc/Hz | 181.56 |

Because the 2-to-1 multiplexer is in charge of the output signals from VCO or the frequency divider, its bandwidth and switching time are important parameters. A very large bandwidth (10M~10GHz) is achieved in Fig. 2-28. According to Fig. 2-29, the switching period is 0.8 nsec when the multiplexer changes the output from VCO to the divider. Furthermore, the band switching in the VCO also needs to be short enough. In Fig. 2-30, the band switching is completed in about 0.65 nsec. In consequence, both of the periods are much shorter than the required time (9.5 nsec).

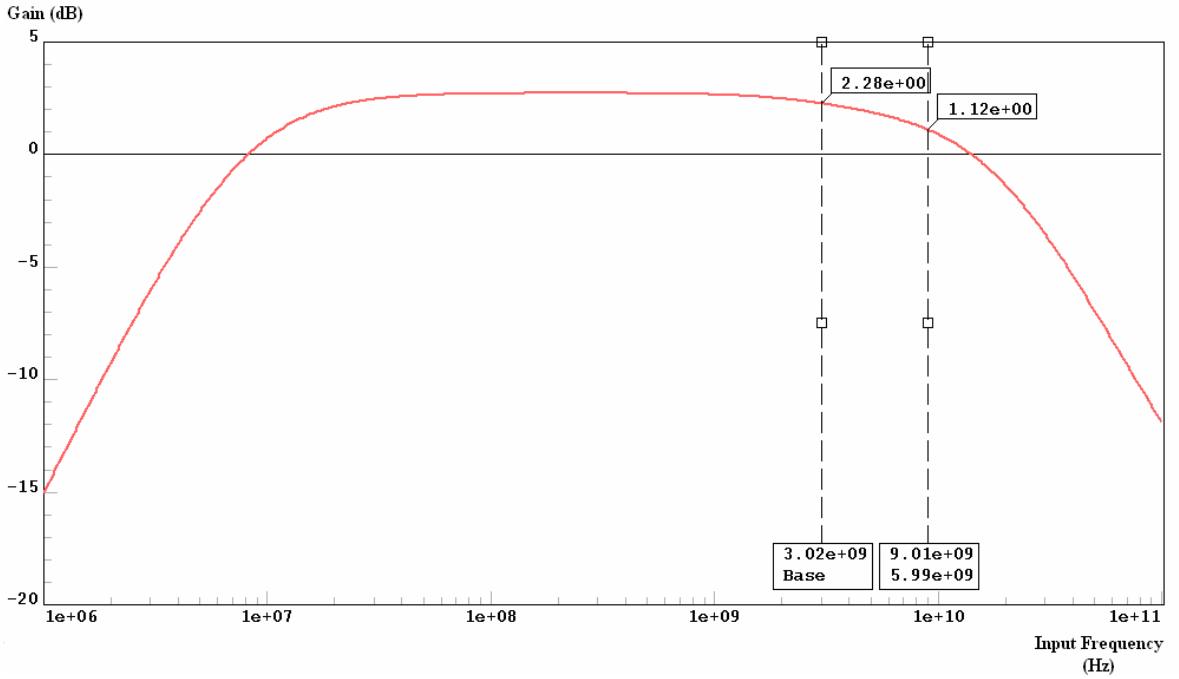



Fig. 2-28 Gain of the multiplexer vs. the input frequency

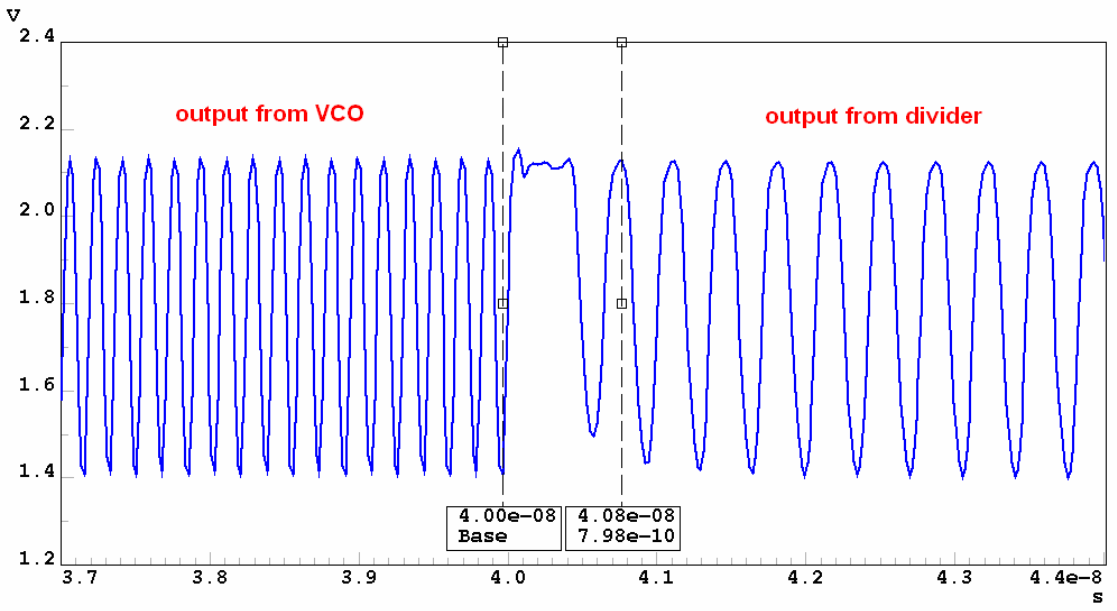



Fig. 2-29 Output waveform switching from VCO to the divider

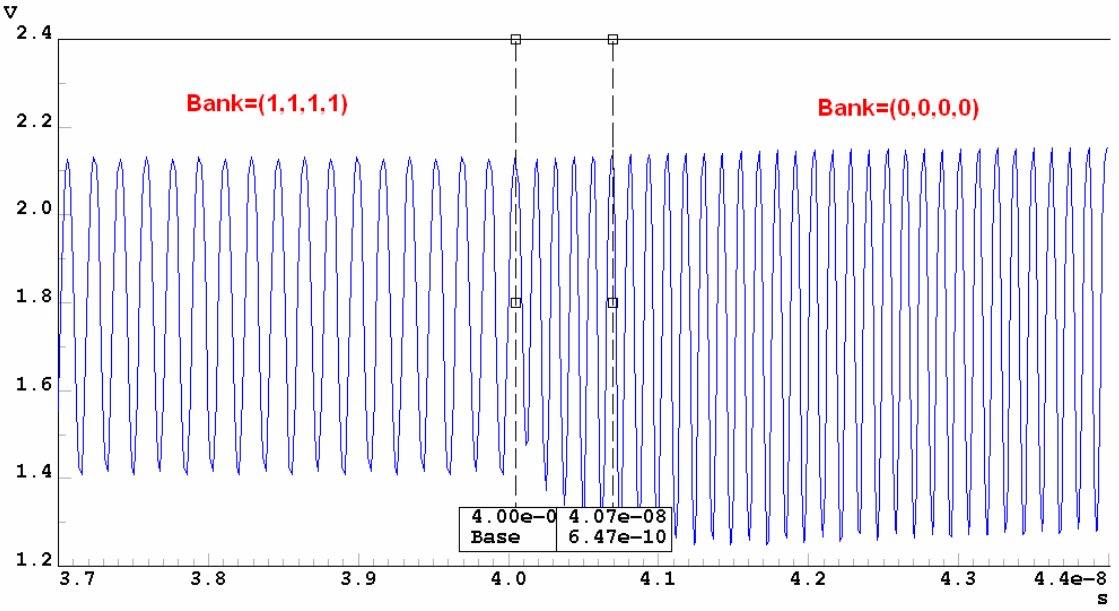



Fig. 2-30 Output waveform switching from bank (1,1,1,1) to bank (0,0,0,0)

The simulation also considers PVT (process-voltage-temperature) corner variations. The tuning range curves are simulated under different conditions. The results are shown in Fig. 2-31~Fig. 2-36 and summarized in Table 2-3. The curves are almost invariant regardless of any corner variation.

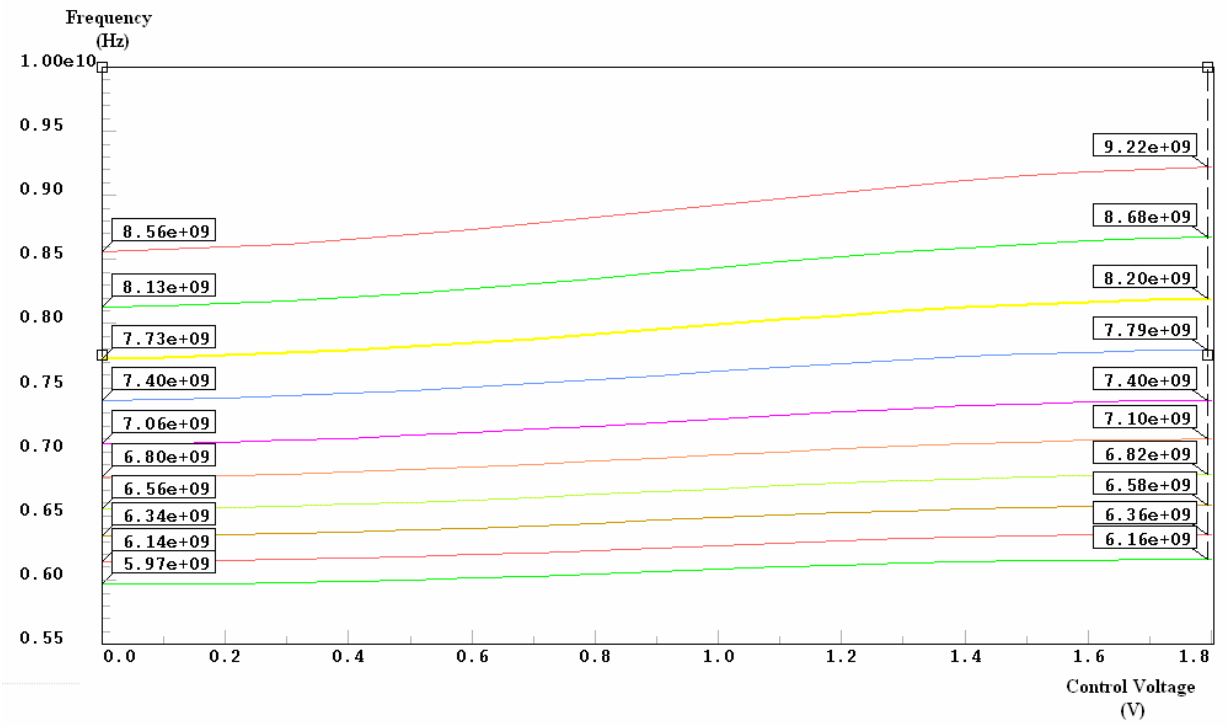



Fig. 2-31 Tuning range curves at FF corner

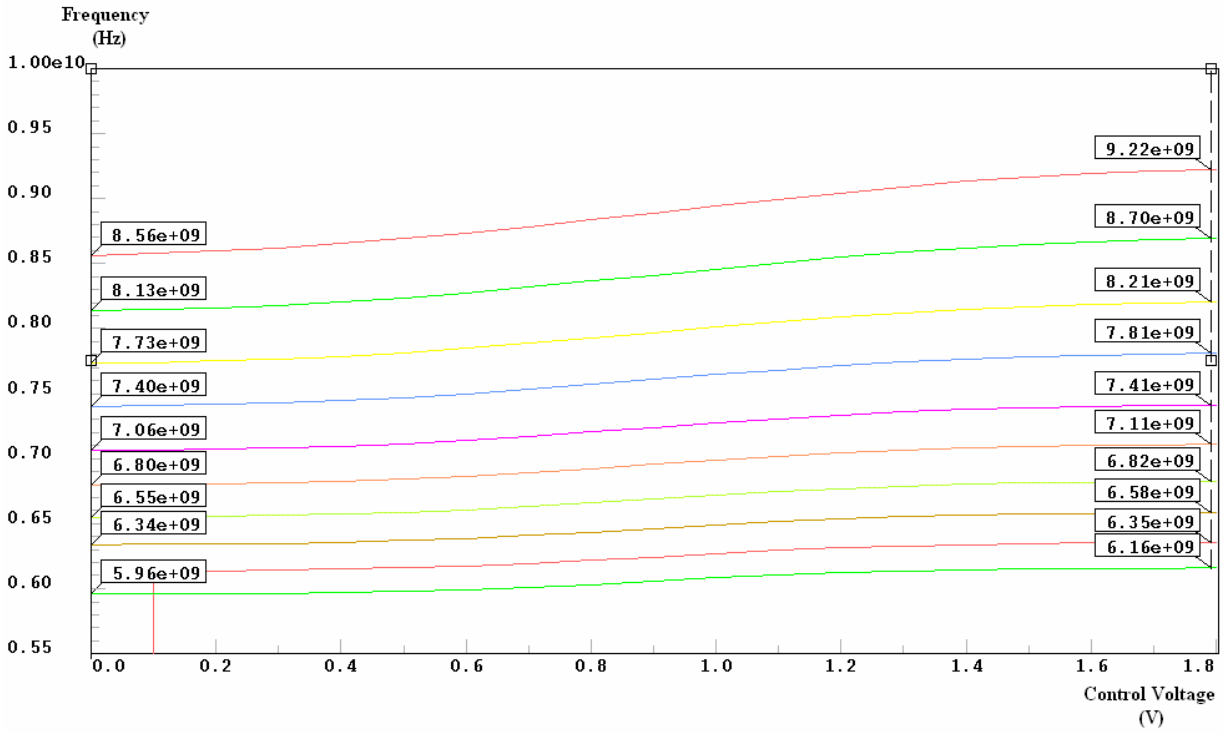



Fig. 2-32 Tuning range curves at SS corner

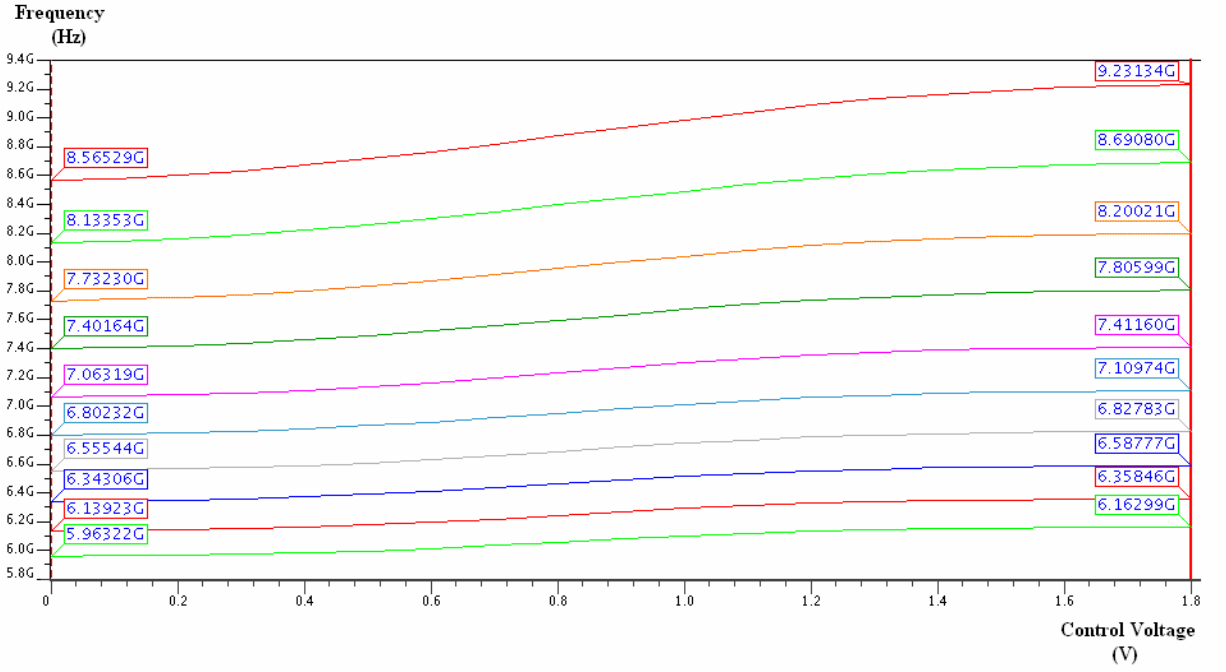



Fig. 2-33 Tuning range curves at $V_{DD}$=1.62 V

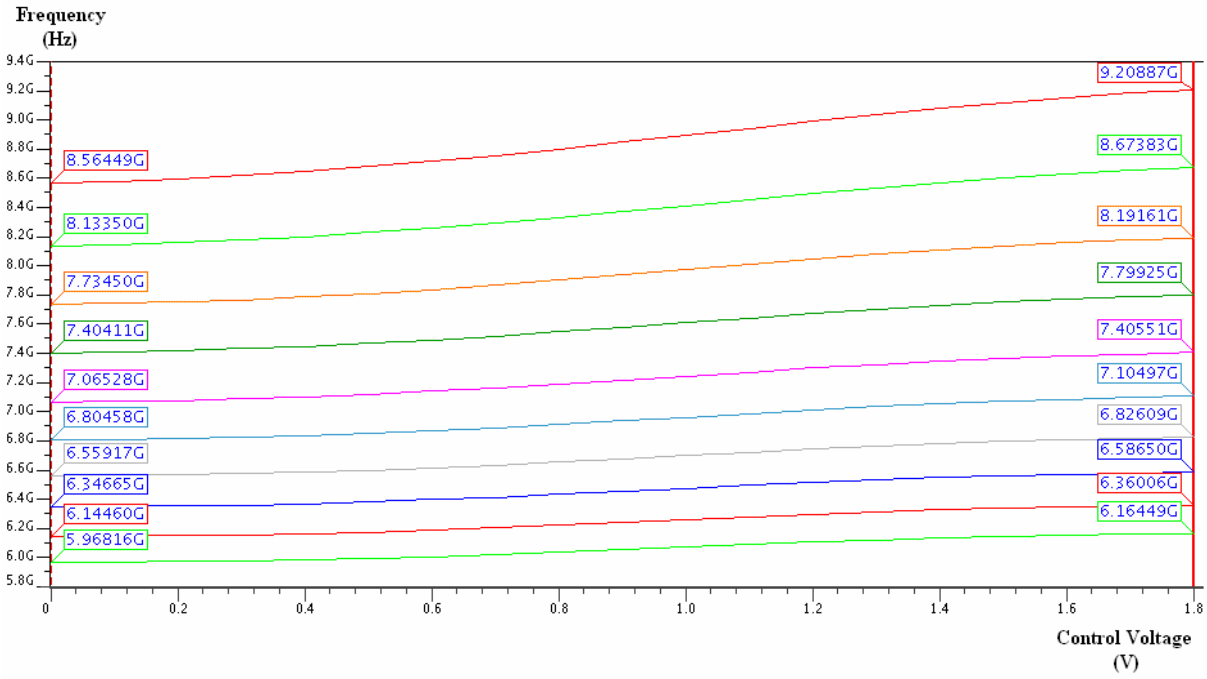



Fig. 2-34 Tuning range curves at $V_{DD}$=1.98 V

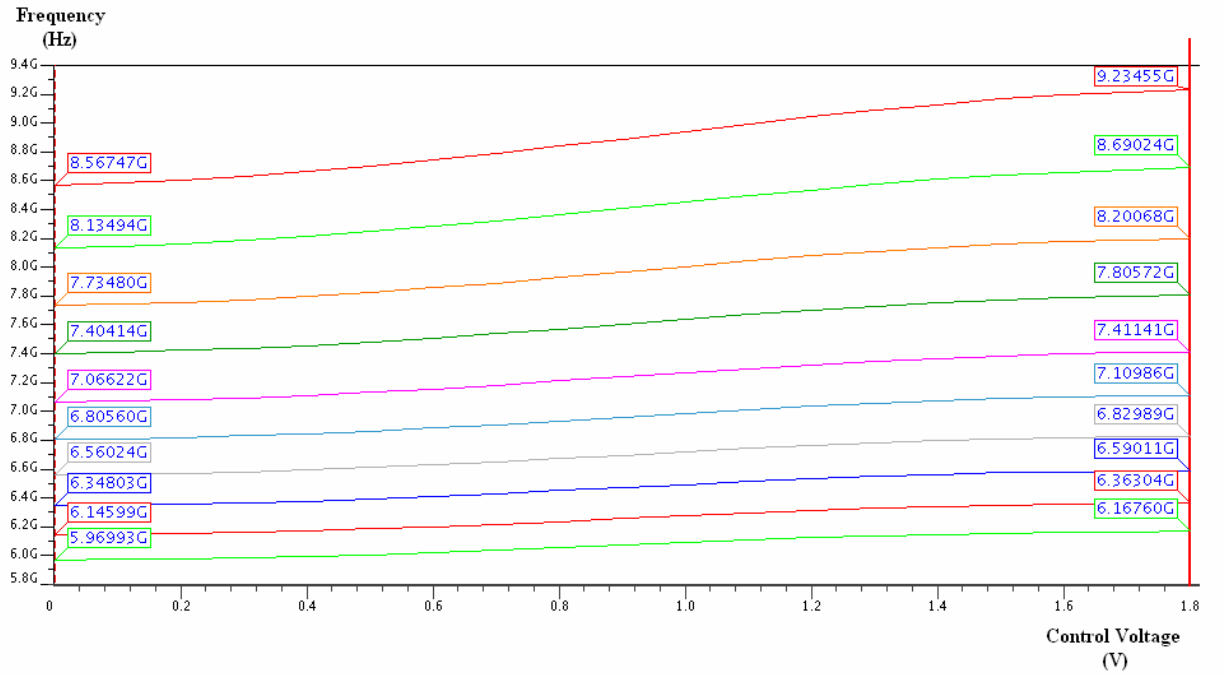



Fig. 2-35 Tuning range curves at T=-10°C

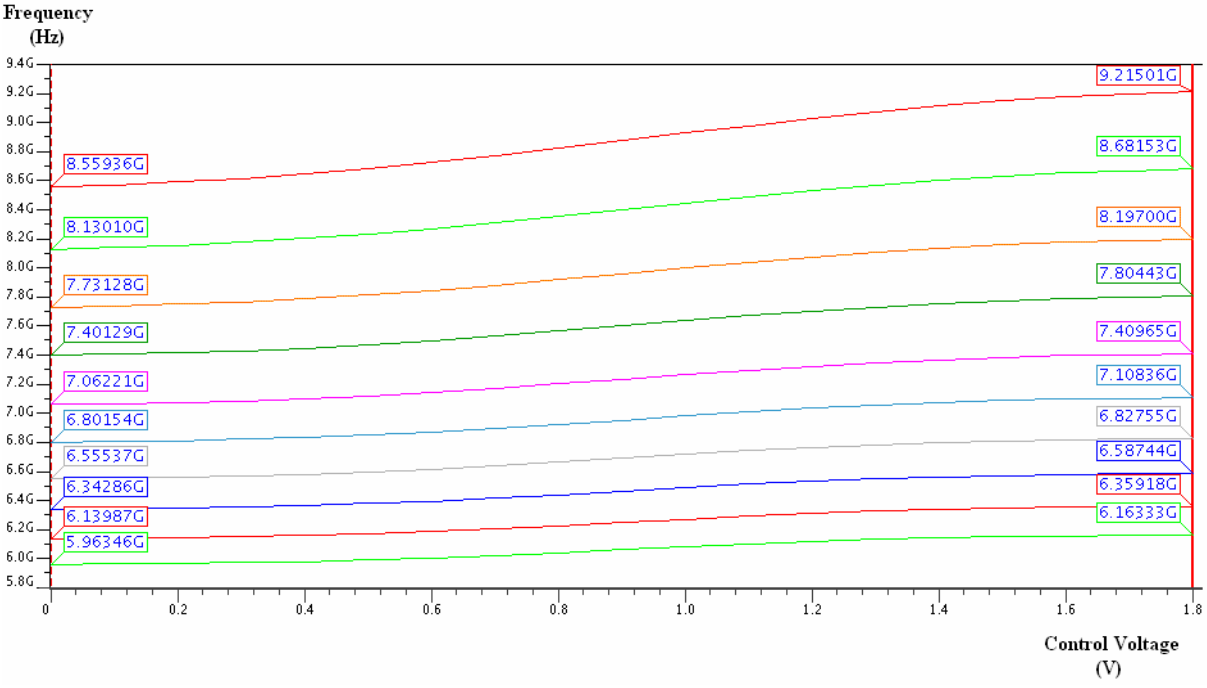



Fig. 2-36 Tuning range curves at T=60°C

Table 2-3 VCO tuning range under different conditions

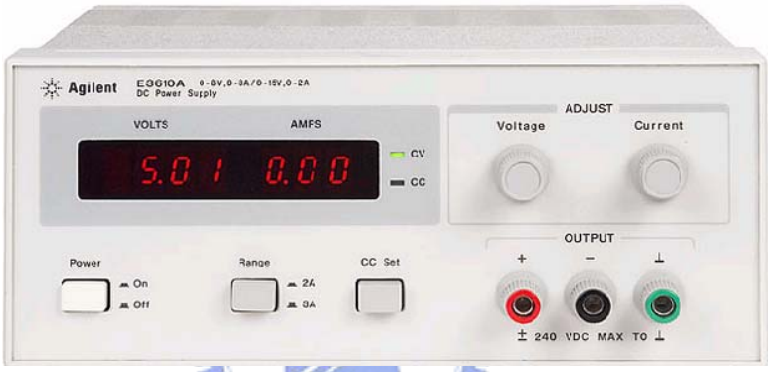
| **Process corner** | **SS** | **TT** | **FF** |
|---|---|---|---|
| | 5.97~9.22 GHz | 5.97~9.22 GHz | 5.96~9.22 GHz |
| **Supply voltage** | **1.62 V** | **1.8 V** | **1.98 V** |
| | 5.97~9.21 GHz | 5.97~9.22 GHz | 5.96~9.23 GHz |
| **Temperature** | **-10°C** | **25°C** | **60°C** |
| | 5.97~9.23 GHz | 5.97~9.22 GHz | 5.96~9.22 GHz |

## 2.3 Measurement Results

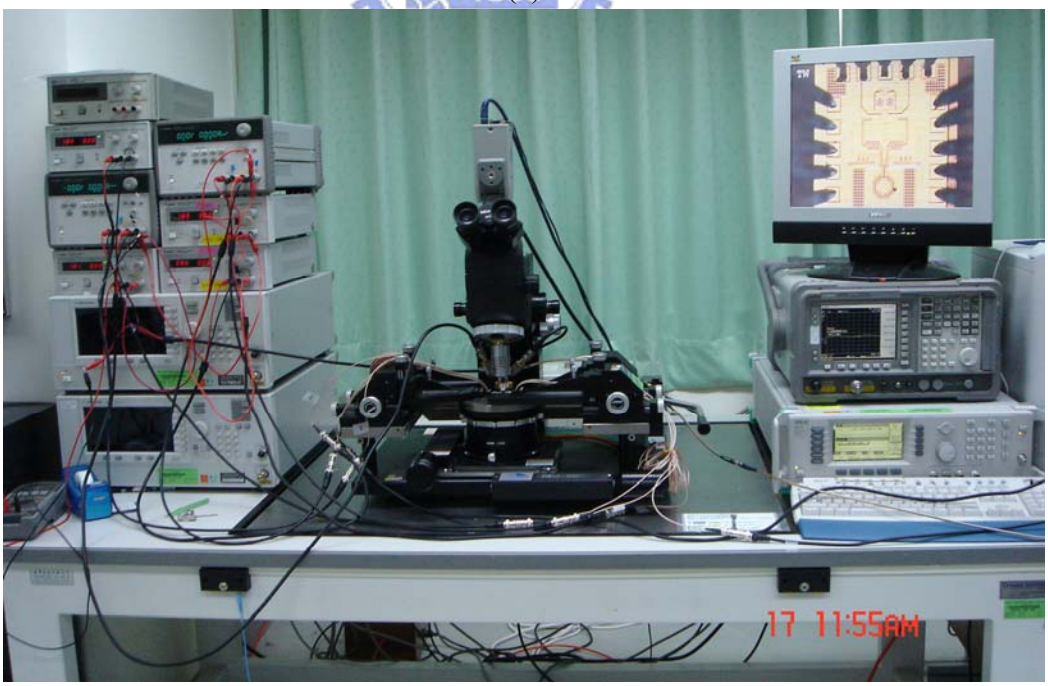
The results are obtained from on wafer circuit measurement in National Chip Implementation Center (CIC). The instruments contain Agilent E5052A signal source analyzer, E4407B spectrum analyzer, and E3615A DC power supply in Fig. 2-37. Also the whole chip photograph is shown in Fig. 2-38.

(a)

(b)




(c)




(d)

Fig. 2-37 Measurement instruments (a) Agilent E5052A signal source analyzer (b) E4407B spectrum analyzer (c)E3615A DC power supply and (d) whole test set

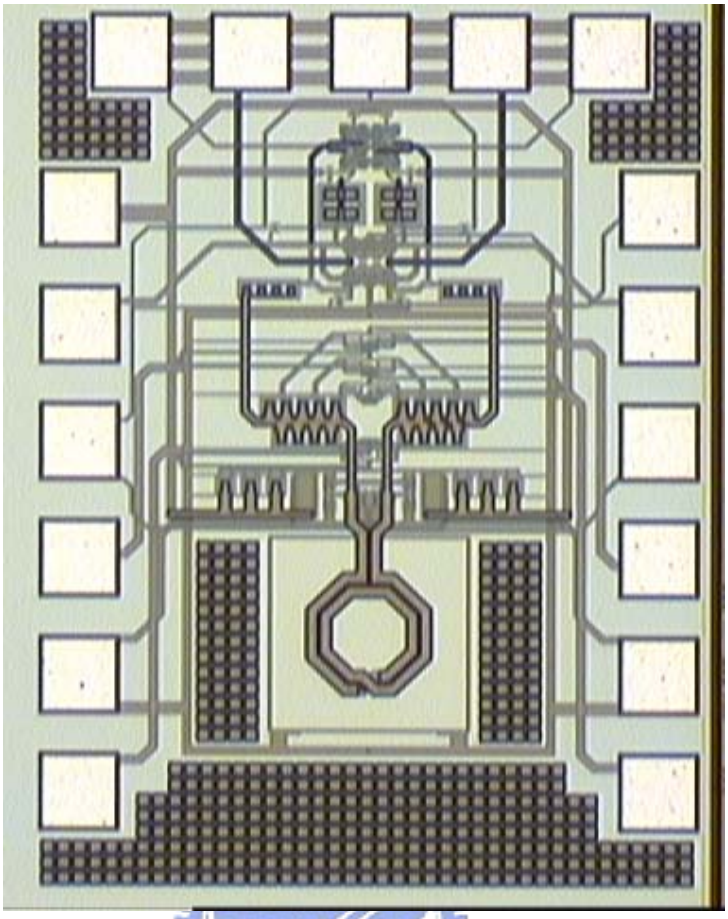


Fig. 2-38 Chip photograph

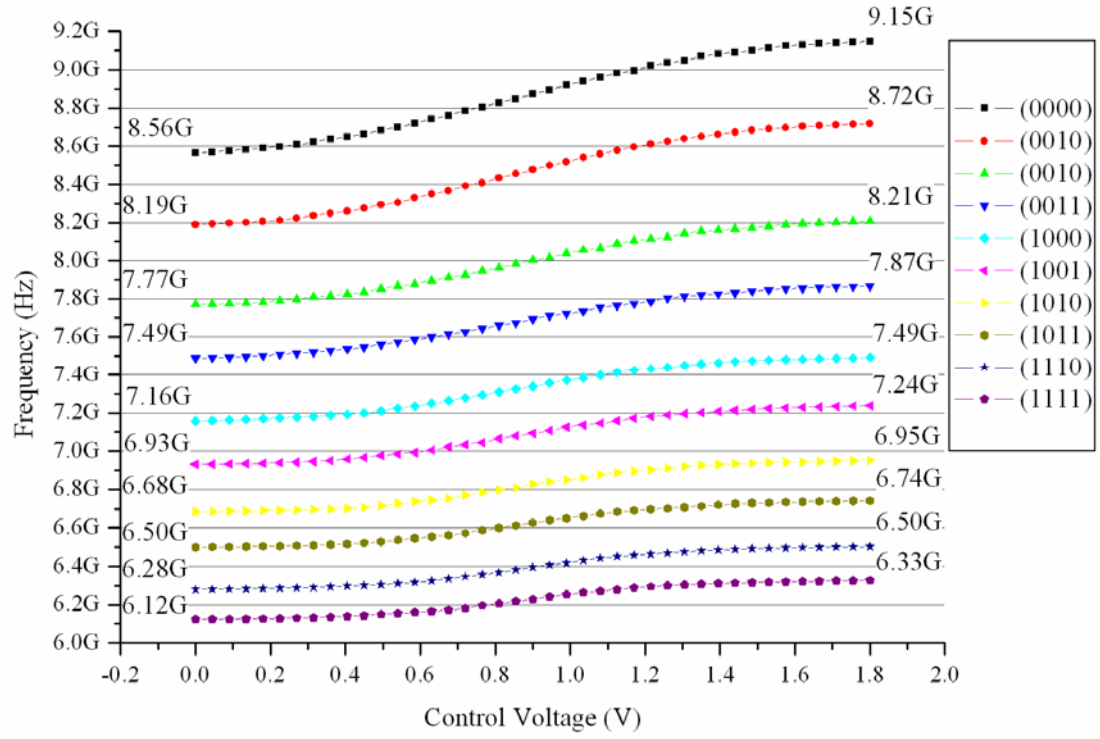


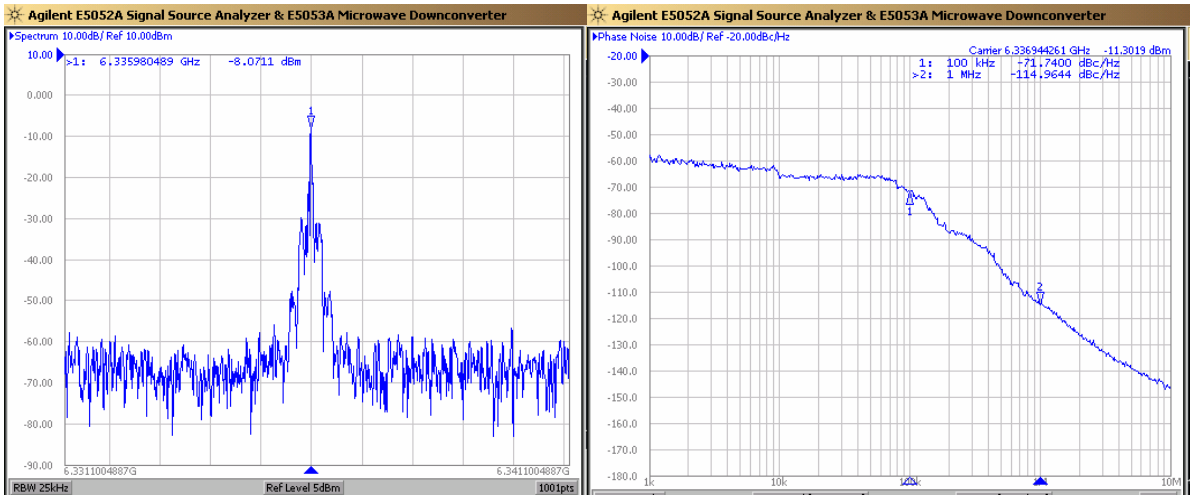

Fig. 2-39 Measured tuning range curves with different banks

According to Fig. 2-39, the 10 tuning range curves cover each other and signal at 6.12~9.15 GHz can all be generated. This range includes the whole required bandwidth. Comparing with 5.97~9.22 GHz bandwidth in the simulation results, the total tuning range is a little shrunk. Because the gain of the VCO is little changed in Table 2-4, the compressed tuning range is mainly from the overestimated capacitors in SCA.

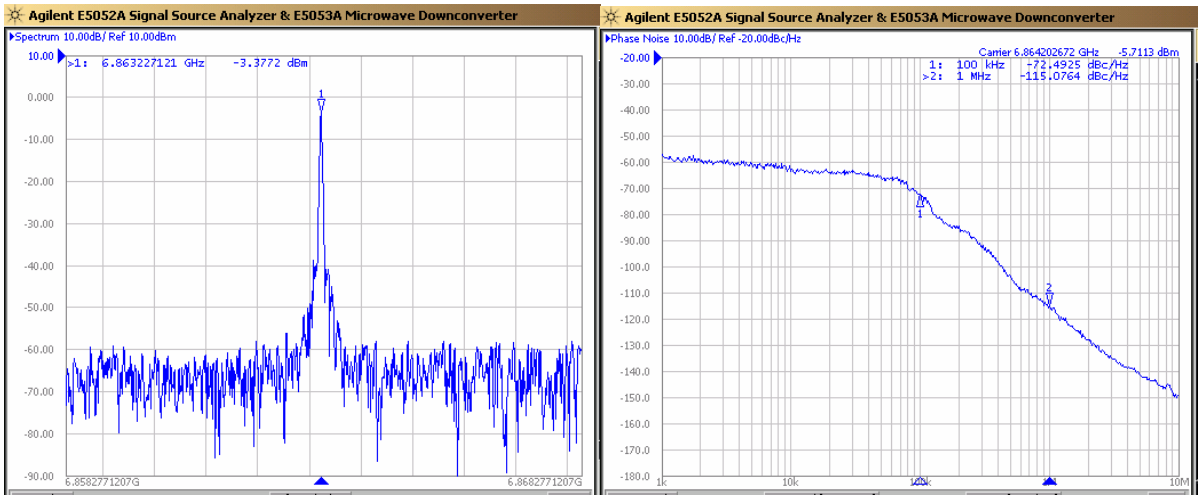
Table 2-4 $K_{VCO}$ Comparison between the simulation and the measurement result

| | **simulation** | **measurement** |
|---|---|---|
| **(0,0,0,0)** | 428.57 MHz/V | 403.71 MHz/V |
| **(0,0,0,1)** | 373.02 MHz/V | 372.19 MHz/V |
| **(0,0,1,0)** | 317.46 MHz/V | 302.38 MHz/V |
| **(0,0,1,1)** | 269.84 MHz/V | 263.49 MHz/V |
| **(1,0,0,0)** | 246.03 MHz/V | 238.91 MHz/V |
| **(1,0,0,1)** | 222.22 MHz/V | 221.49 MHz/V |
| **(1,0,1,0)** | 182.54 MHz/V | 196.06 MHz/V |
| **(1,0,1,1)** | 174.60 MHz/V | 177.73 MHz/V |
| **(1,1,1,0)** | 150.79 MHz/V | 162.74 MHz/V |
| **(1,1,1,1)** | 134.92 MHz/V | 148.88 MHz/V |

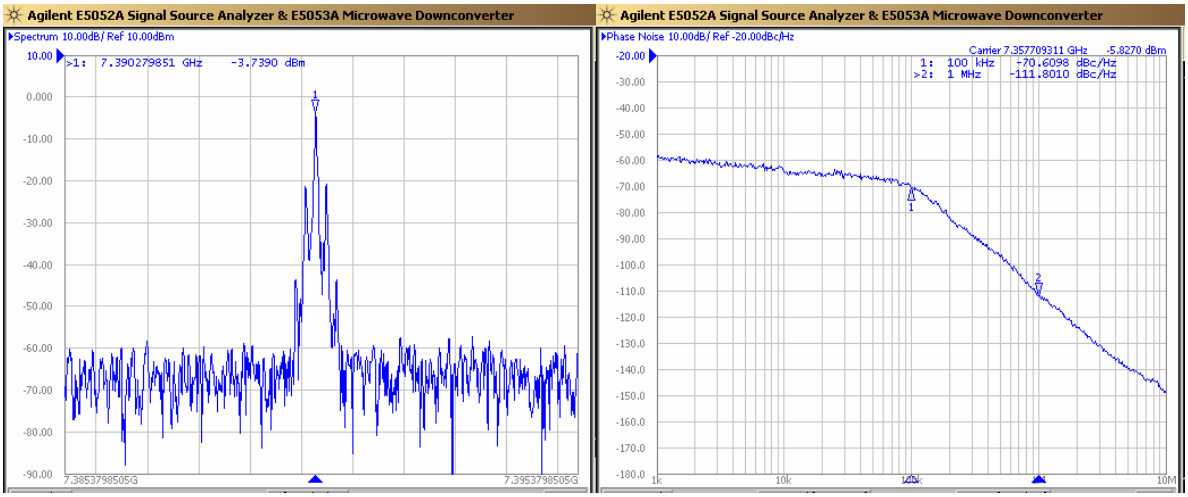
Following the tuning range, the output power and phase noise performance is measured in Fig. 2-40 and Table 2-5. The measured value of the phase noise is approximately equal to the simulated one while the output power is about 5 dB smaller than the simulation result. This is probably caused by the loss of the coaxial line. Especially two series coaxial lines are connected for the longer distance between the chip and the instruments. According to data in CIC, the loss is compensated and actual output power is obtained. Therefore, the signal attenuation can be considerable.



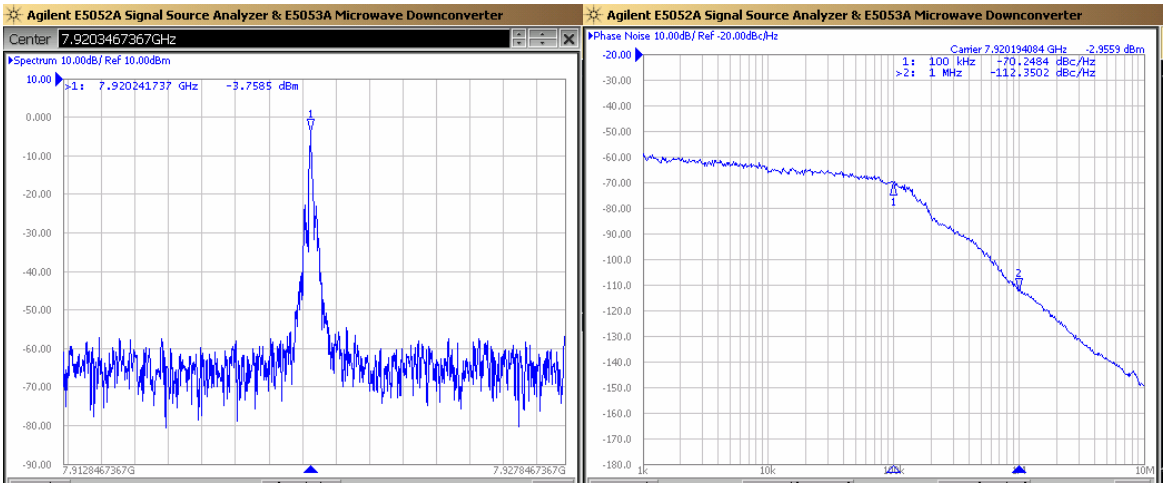

(a) 6.336 GHz



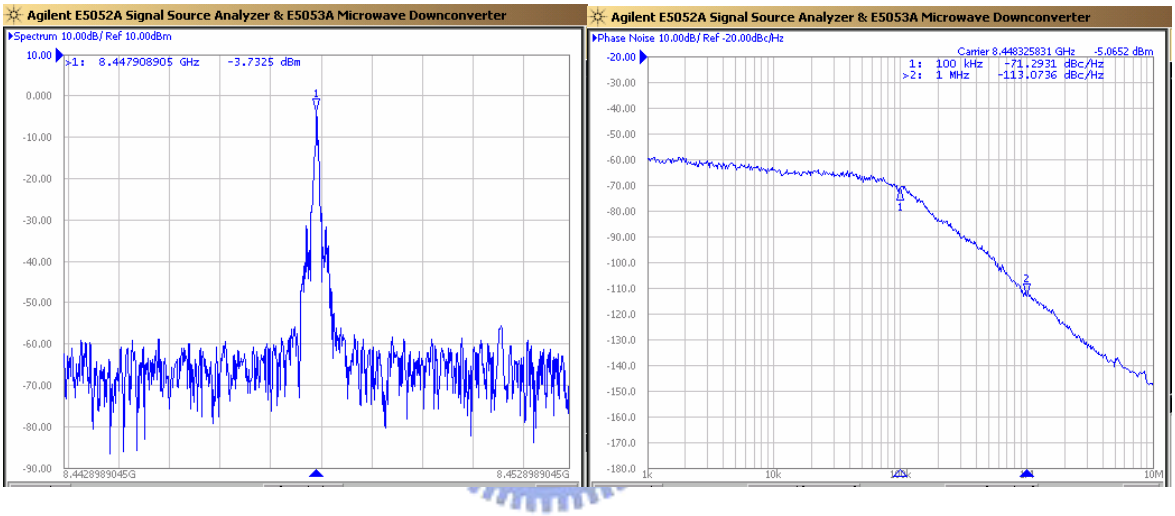

(b) 6.864 GHz



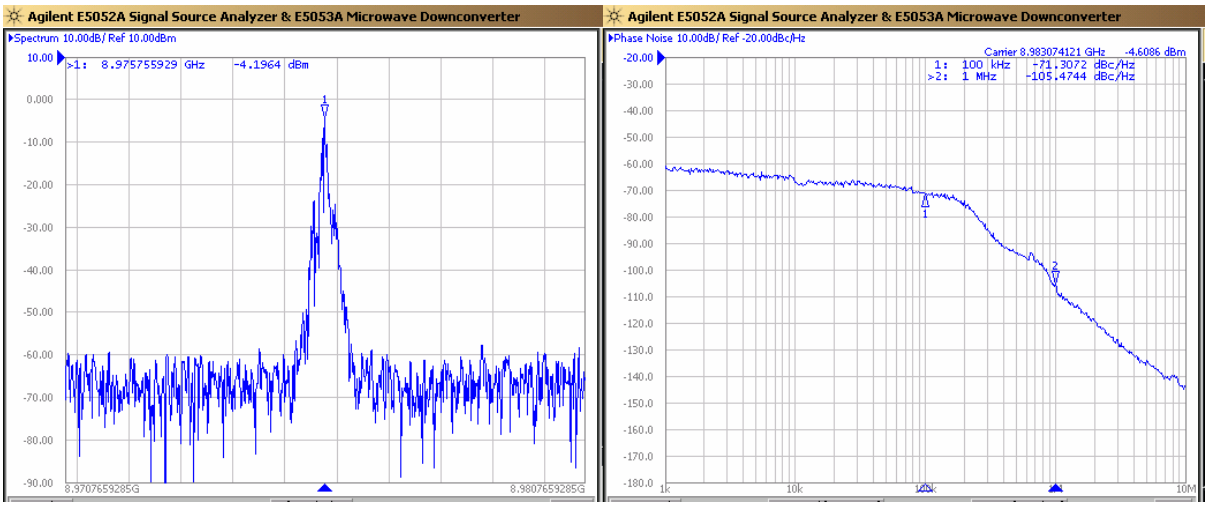

(c) 7.392 GHz




(d) 7.920 GHz




(e) 8.448 GHz



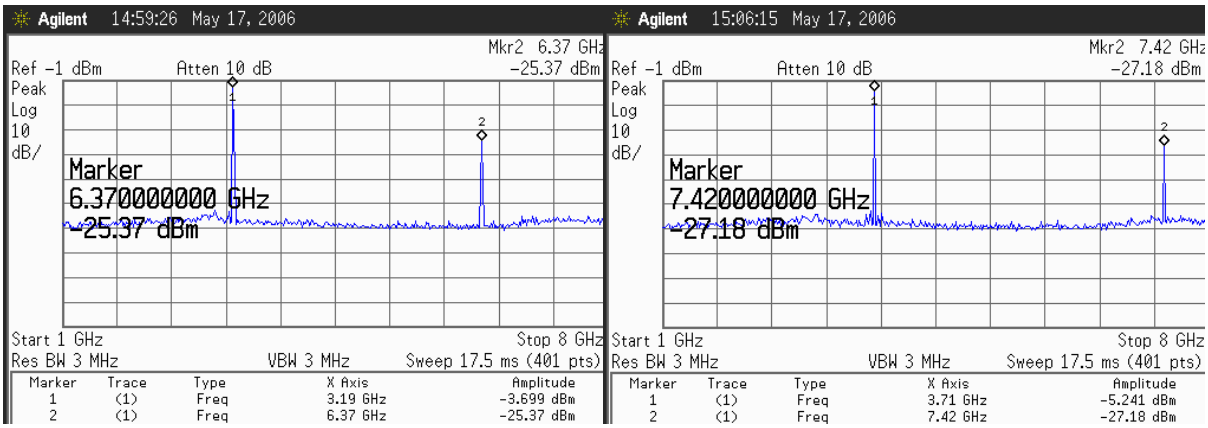

(f) 8.976 GHz

Fig. 2-40 Measurement of output power and phase noise at six carrier frequencies

Table 2-5 Measurement of output power and phase noise performance at six frequencies

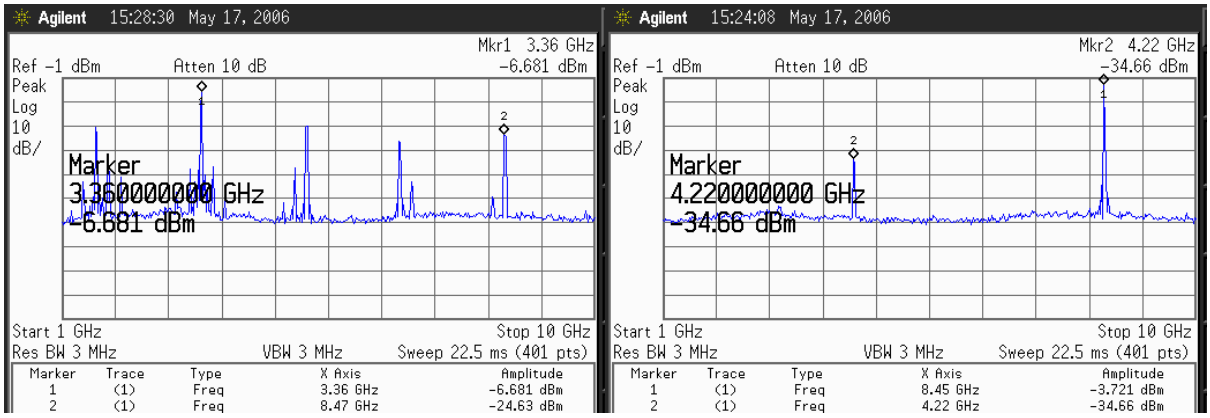
| Carrier Frequency | Output Power | Phase noise @ 1MHz | FOM |
|---|---|---|---|
| 6.336 GHz | -5.85 dBm | -114.96 dBc/Hz | 182.49 |
| 6.864 GHz | -1.08 dBm | -115.08 dBc/Hz | 183.31 |
| 7.392 GHz | -1.33 dBm | -111.80 dBc/Hz | 180.67 |
| 7.920 GHz | -0.99 dBm | -112.35 dBc/Hz | 181.81 |
| 8.448 GHz | -1.17 dBm | -113.07 dBc/Hz | 183.10 |
| 8.976 GHz | -1.54 dBm | -105.47 dBc/Hz | 176.03 |

Besides the VCO, the performance of the divider-by-2 circuit is measured in Fig. 2-41. The multiplexer suppresses the VCO signal about 20 dB when the frequency divider is selected. But at 4.224 GHz the divider doesn't work properly in Fig. 2-42. The reason is likely that the parasitic effect at the output nodes of the divider is not completely extracted and the behavior can't be accurately predicted in the post-simulation. As a result, the control voltage of VCO is tuned and the locking range of the frequency divider is up to 7.84 GHz. The measurement is shown in Fig. 2-43. Finally, the power dissipation in the measurement is very close to the result in the simulation.




(a) (b)

Fig. 2-41 Output power of the carrier frequency at (a) 3.168 and (b) 3.696 GHz




(a) (b)

Fig. 2-42 MUX output at 4.224 GHz when (a) the divider or (b) VCO is selected

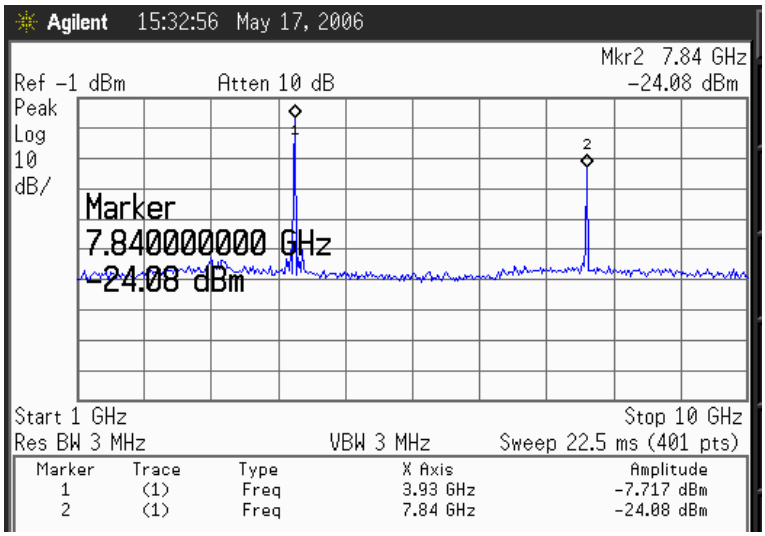



Fig. 2-43 Maximal frequency in the locking range of the divider

## 2.4 Summary and Comparison

The performance in the measurement is close to the results in the simulation except that 4.224 GHz signal is not generated successfully. To improve this, the layout parasitic extraction by EM software has to be more detailed although this will take a far longer time. The summary of this work is listed in Table 2-6. In addition, the comparison with other wideband VCOs is made in Table 2-7. Through the figure-of-merit (FOM), this work really achieves better performance.

Table 2-6 Summary of the performance in the simulation and measurement

| Performance | Post-Simulation | Measurement |
|---|---|---|
| **Supply Voltage** | 1.8V | |
| **Power Consumption** | 37.91 mW | 36.63 mW |
| **Tuning Range** | 5.97~9.22 GHz | 6.12~9.15 GHz |
| **Phase Noise @ 1MHz** | -111~-114 dBc/Hz | -105.5~-115 dBc/Hz |
| **Output Power** | 0.1~3.53 dBm | -5.85~-0.99 dBm |

Table 2-7 Comparison with the recent published papers about wideband VCOs

| | **MAPE 2005 [17]** | **MWCL 2005 [18]** | **ISCAS 2005 [19]** | **This Work** |
|---|---|---|---|---|
| **Technology** | 0.35 μm SiGe | 0.18 μm CMOS | 0.18 μm CMOS | 0.18 μm CMOS |
| **Supply Voltage** | 3 V | 1.8 V | 1.5 V | 1.8 V |
| **Tuning Range** | 2.08~2.51 GHz<br>430 MHz, 17.6% | 5.5~6.7 GHz<br>1.2 GHz, 20% | 3.5~5.3 GHz<br>1.8 GHz, 40.9% | 6.12~9.15 GHz<br>3 GHz, 39.7% |
| **Phase Noise** | -110 dBc/Hz<br>@ 1 MHz | -115 dBc/Hz<br>@ 1MHz | -115 dBc/Hz<br>@ 1 MHz | -115 dBc/Hz<br>@ 1 MHz |
| **Power Dissipation** | 12.06 mW | 5.8 mW | 6 mW | 36.63 mW<br>(7.09 mW in VCO core) |
| **FOM** | 166.97 | 182.17 | 180.09 | 183.31 |

# Chapter 3
# Low Power and Fast-Locking Integer-N Frequency Synthesizer for MB-OFDM UWB System

In this chapter, a low power and fast-locking integer-N frequency synthesizer is presented for the MB-OFDM UWB application. Because of the frequency divider in this proposed synthesizer, a remarkable reduction in the power dissipation is achieved. Additionally, the choice of the reference clock leads immunity against the spurious tone. This circuit is designed by using TSMC RF 1P6M 0.18 μm CMOS technology and applied to be fabricated in June 2006. In the following sections, the architecture and circuit design consideration is demonstrated first. Then each block in this frequency synthesizer will be explained individually. Finally, the simulation results and comparison will also be discussed.

## 3.1 Architecture

There are three ways to perform frequency generation for MB-OFDM UWB system. One approach is to have multiple PLLs in parallel which are responsible for different frequencies. In [20], three fixed-modulus PLLs are used for the frequencies in Band Group #1. This method is most direct and easy to meet the specifications. However, it will need too many PLLs while all 14 carrier frequencies are used. It will demand too much power dissipation and large chip area to be practical. The second method is to integrate PLLs with external multiplexers and single side-band (SSB) mixers[21]-[23]. Two specified frequencies are

generated by PLLs and SSB mixers can up/down-convert these two signals into the desired carrier frequency. But the SSB mixers need accurate quadrature inputs and should be highly linear for low spurious tones. These requirements add more complexity and difficulty to the circuits. The third method is using two fast-settling frequency synthesizers to generate the desired signal by turns[24]. As proposed in [3], the symbol interval is 312.5 nsec and the guard time is 9.47 nsec. Therefore a single PLL has to be locked with about 322 nsec. It becomes more practical for a conventional frequency synthesizer which is easy to be implemented. Here the third method is adopted in this thesis.

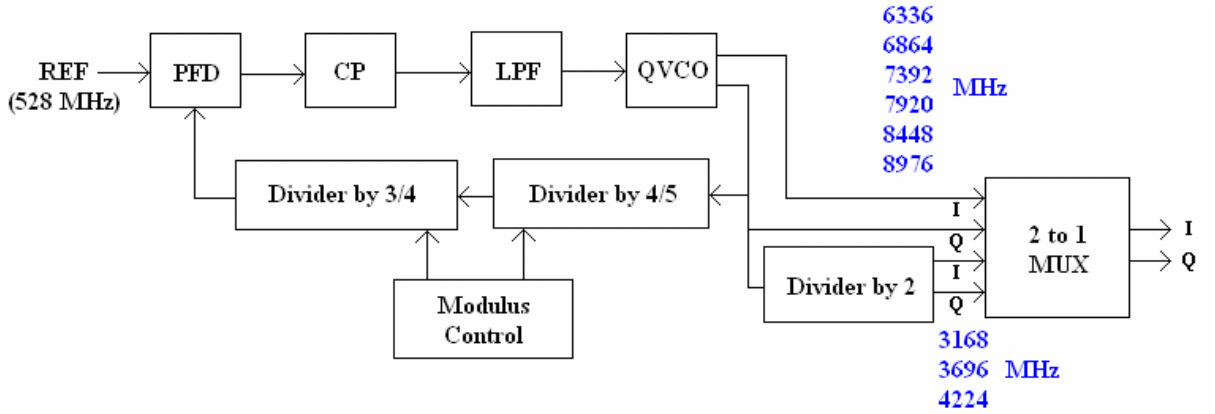



Fig. 3-1 Block diagram of the synthesizer in [24]

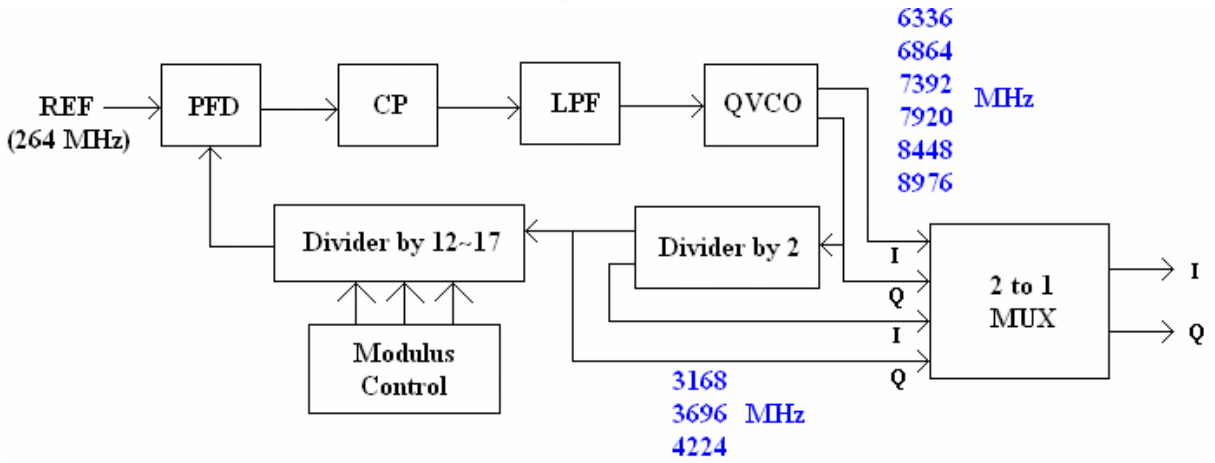



Fig. 3-2 Block diagram of the proposed synthesizer

As shown in Fig. 3-2, QVCO in the proposed synthesizer does not have to generate all signals for whole 3.1~10.6 GHz band. In fact, QVCO is merely responsible for Band Group #3 and #4 while Band Group #1 is left for the divider-by-2 circuit. Band Group #2 is ignored

for the better coexistence with other wireless standards and Band Group #5 is reserved for the future research. Comparing with [24], there are several modifications in this proposed synthesizer. First, the divider-by-2 circuit is included in the loop. In [24], the dual-modulus /4/5 divider contains six CML DFFs which are power-hungry when operating at high frequencies from QVCO. Therefore it is replaced by a divider-by-2 circuit which consumes less than half original power (including the external divider-by-2) and the load of the oscillator becomes smaller because only two DFFs are needed. Second, two dual-modulus /2/3 dividers are substituted for the /4/5 divider. This reduces the power in the multi-modulus divider again. Section 3.2.2 will give explanation for why the power reduction is made. Third, the frequency of the reference clock is halved. Although this causes the settling time longer, the specification is still met. Moreover the reference frequency is half of the channel bandwidth and then the spur effect on the channel is eliminated. It is resulted from that spurs occur at the center of two neighboring channels and do not pollute the channel anymore (shown in Fig. 3-3). The requirement of the spurious tones is greatly relaxed.

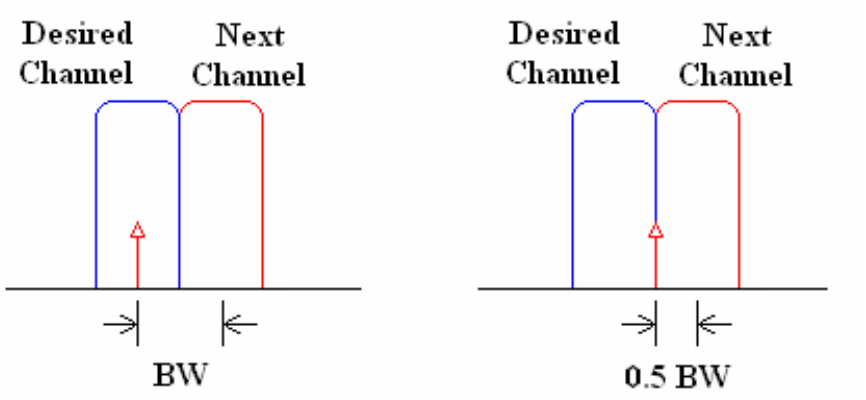



Fig. 3-3 Comparison of spur at different frequencies

## 3.2 Circuit Design Consideration

According to Fig. 3-2, the proposed frequency synthesizer is based on an integer-N type

phase-locked loop. In contrast with fractional-N type, integer-N type has a fixed division number in every reference clock and then spurious tone is lowered. In addition, it is a simpler structure and dissipates less power. Due to the relatively large frequency resolution (528 MHz) and sufficient locking time, integer-N type is more suitable in this design.

This frequency synthesizer is composed of a quadrature voltage-controlled oscillator (QVCO), a multi-modulus frequency divider, a fast phase-frequency detector, a charge pump with variable current, and an on-chip third-order passive loop filter. There are seven digital input signals: four are to select the tuning range curves of the QVCO and the remainders are to control the division ratio in the multi-modulus divider.

As mentioned in the preceding section, the frequency synthesizer has to settle with 322 nsec over PVT (process-voltage-temperature) corner variations. Therefore the settling time is designed to be approximately 200 nsec. The essential open-loop bandwidth to achieve a settling time of 200 nsec can be roughly calculated by the following equation

$$BW = \frac{1}{T_{lock}\zeta_e(PM)} \cdot \ln\left(\frac{f_{step}}{f_{error}}\right) \qquad (3\text{-}1)$$

where $T_{lock}$ is the locking time, $\zeta_e(PM)$ is the effective damping coefficient as a function of the loop phase margin PM, $f_{step}$ is the magnitude of the frequency jump, and $f_{error}$ is the allowable frequency error after locking[25]. This equation is derived from continuous-time approximation. As far as the fastest locking time is concerned, the phase margin should be set to 50°, and $\zeta_e(50°)$ will be about 5[26]. In the case of 528 MHz frequency jump and 1 KHz frequency error tolerance, BW is about 13.2 MHz from Eq. ( 3-1 ). In a PLL design, the reference frequency has to be greater than 10 times of the loop bandwidth in order to guarantee the loop stability[27]. In other words, the assumption of the 264 MHz reference frequency above is quite acceptable. Although the frequency of a conventional crystal oscillator is merely up to tens MHz, a simple PLL can be employed for the synthesis of the reference clock for the consideration of SOC. A narrow band PLL is preferred because phase

noise at an offset above a few hundred kHz has to as low as possible.

In the principle of designing PLLs, wider loop bandwidth leads to more suppression of the in-band VCO phase noise. As a result, noise from other blocks, such as reference, charge pump, and loop filter becomes more important within the loop bandwidth. By the UWB system proposal, the noise requirement is defined as the overall integrated rms phase noise from 0 Hz to infinity and the obtained value should be lower than 3.5°. This integrated phase noise can be calculated by this formula:

$$rms \quad noise = \frac{180}{\pi} \cdot 10^{0.05k} \sqrt{BW \cdot (1 + 10^{0.1p}) + 2 \cdot 10^{0.1p}} \qquad (3\text{-}2)$$

where k is the in-band phase noise density (dBc/Hz) and p is the peaking of k[24]. In order to achieve the integrated phase noise below 3.5°, k should be less than -95.5 dBc/Hz while p is assumed to be 0.

Spurious tones from the ripple on the QVCO control voltage do not get much attenuation by the loop filter because of the wide bandwidth. To reduce these spurious tones can be accomplished by matching the current sources in the charge pump. At the output nodes of QVCO, the relative magnitude of the primary sidebands is given by:

$$spur = \frac{A_{ripple} \cdot K_V}{2 \cdot 2\pi \cdot f_{REF}} \qquad (3\text{-}3)$$

where $A_{ripple}$ is the peak amplitude of the first harmonic of the ripple, $K_V$ is the gain of the QVCO, and $f_{REF}$ is the reference frequency[29]. For smaller spurious tones, $A_{ripple}$ and $K_V$ should be minimized. Current matching in the charge pump is a method to lower $A_{ripple}$. $K_V$ should be as small as possible while the tuning range still meets the specification. In this circuit, $K_V$ is large and up to 500 MHz/V because a 6~9 GHz band needs to be covered. Under the condition of the maximal $K_V$ and the given 264 MHz reference frequency, the peak fundamental ripple amplitude must be less 10.6 mV to guarantee than sidebands are 50 dB below the carrier.

The output frequency is determined by the multi-modulus frequency divider. The

division factor is controllable even number from 24 to 34. The frequency synthesizer can provide six carrier frequencies which are spread from 6.336 to 8.976 GHz in steps of 528 MHz.

### 3.2.1 Quadrature Voltage-Controlled Oscillator

There are several ways to obtain quadrature signals: divider-by-2 circuit, RC poly-phase filters, and two interleaved voltage-controlled oscillators. The divider-by-2 circuit needs an oscillator operating at 2 times higher than the desired frequency and a high-speed frequency divider. Both circuits dissipate a lot of power in spite of a smaller chip size. RC poly-phase filters attenuate the signal and increase the effective capacitance of the tank. Also a lot of chip area is needed for a good matching of the filters. For the low power consumption and quadrature phase accuracy, two interleaved voltage-controlled oscillators are adopted in this circuit[28]. According to the Barkhausen criterion, oscillation occurs only when the loop gain $[A(j\omega)]^4$ is unity in Fig. 3-4. Therefore $A(j\omega)$ has amplitude of one with a 90 degree phase shift and quadrature signals are obtained at the four outputs of these two VCOs.

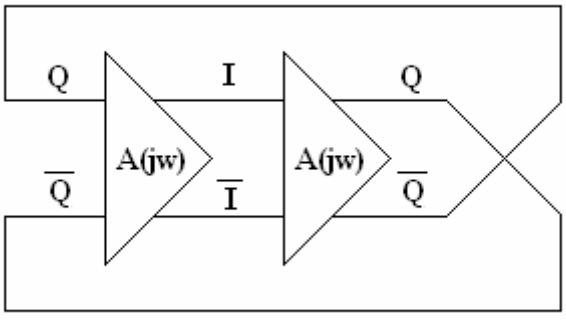
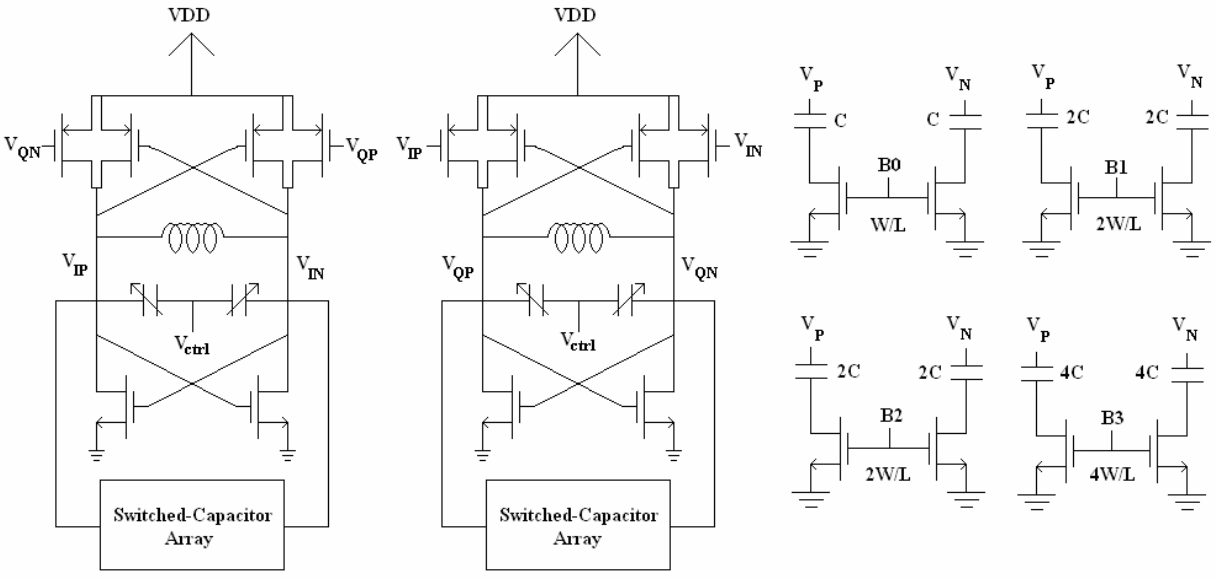



Fig. 3-4 Two interleaved VCO configuration

As shown in Fig. 3-5(a), the VCO is in a complementary cross-coupled negative-gm configuration. The advantages of this configuration are mentioned in Chapter 2. However, there is a difference from the VCO in Chapter 2. The tail current source is removed to

maximize the output swing. Two benefits are also achieved thanks to the removal of the current source. First the current source is the main contributor to the phase noise[30]. Second, when all transistors in the VCO core are put in GHz-switching bias condition, flicker noise will apparently be reduced by about 10 dB[31]. The dimension of four cross-coupling PMOS transistors is an important parameter. If cross-coupling is made weak, two-tones oscillation exists probably; if it is made strong, DC power is wasted and more capacitance is added into the LC-tank. By means of transient simulations, the optimal width of the cross-coupling transistors should be set to one-third of the width of the core transistors while the length of all transistors is chosen as the minimal length (0.18 μm in this circuit)[32].



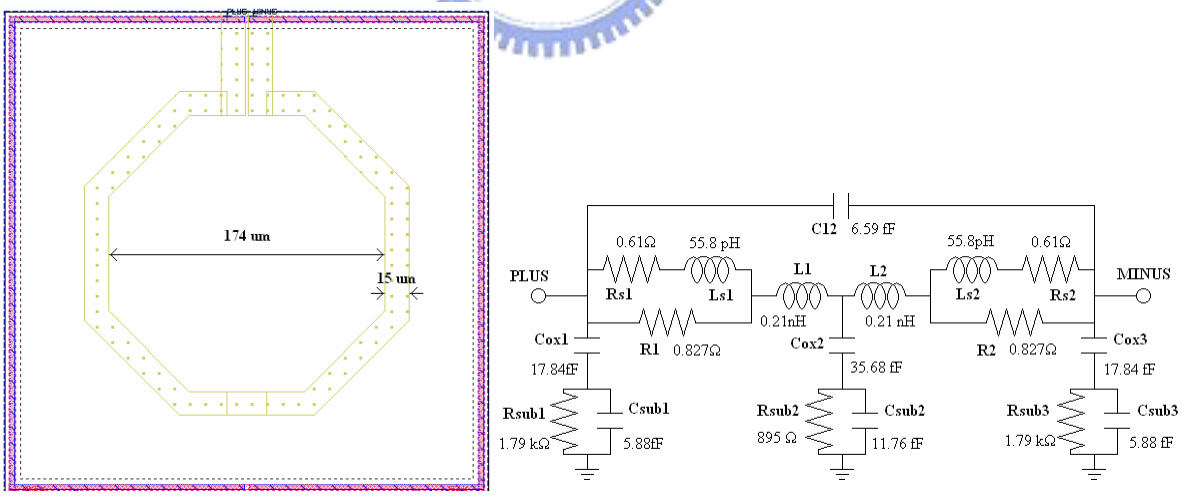

(a) (b)

Fig. 3-5 (a) Quadrature voltage-controlled oscillator and (b) switch-capacitor array

For a wide tuning range of 6~9 GHz, the SCA (switched-capacitor-array) is used as well as in Chapter 2. SCA is composed of four pairs of binary-weighted MIM capacitors and eight NMOS transistors as digital-control switches. The SCA decides the tuning range curve and then the varactors are for actual frequency. Therefore no bulky varactors are required because the whole bandwidth is not covered only by the varacters. Fig. 3-5 shows the SCA configuration. The NMOS switches are connected to ground directly rather than connected

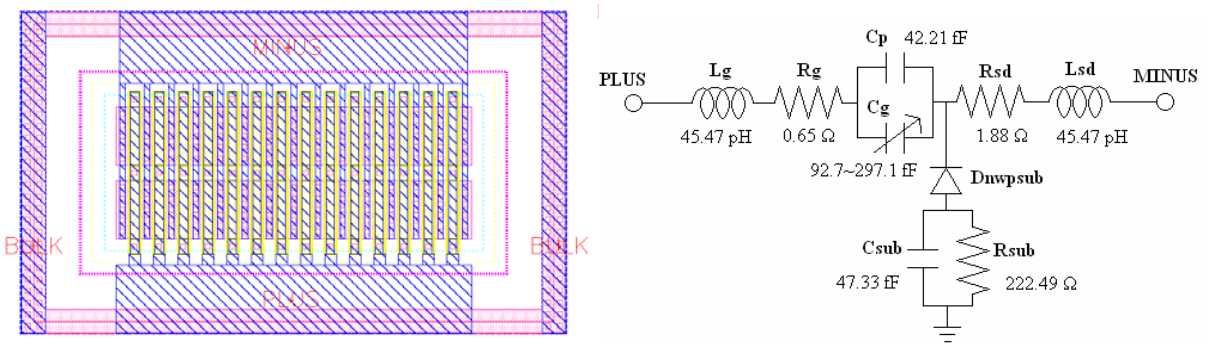
with bottoms of two MIM capacitors. Despite of several advantages remarked in Chapter 2, NMOS switches connected with the MIM capacitors leads to a more complicated layout and serious parasitic effect.

The passive components in LC tank are symmetric spiral inductors and accumulation-mode varactors again. They improve the phase noise performance due to their higher Q-value and the reason is mentioned in Chapter 2. The layout of the symmetric inductor in this circuit and its equivalent lumped circuit are shown in Fig. 3-6 with spacing=2 μm, width=15 μm, and radius=87 μm. The equivalent inductance $L_{eq}$ is about 0.43 nH and the parasitic resistance $R_l$ is 1.49 Ω. Fig. 3-7 shows the layout of the varactor and its equivalent lumped model. The MOS varactor has 14 branches and two groups. The equivalent capacitance $C_{eq}$ is about 140.29~339.33 fF and the parasitic resistance $R_c$ is 2.53 Ω. After considering the SCA, VCO output stage and parasitic effect from the chip layout, the simulated VCO oscillation frequency is around 8.9 GHz under the condition of $V_{ctrl}$=0.9 V and bank(0000). The simulated $K_V$ is distributed from 240~500 MHz/V.




**(a)** **(b)**

Fig. 3-6 (a) Layout and (b) its lumped model of the symmetric spiral inductor




(a) (b)

Fig. 3-7 (a) Layout and (b) its lumped model of the MOS varactor

### 3.2.2 Multi-Modulus Divider

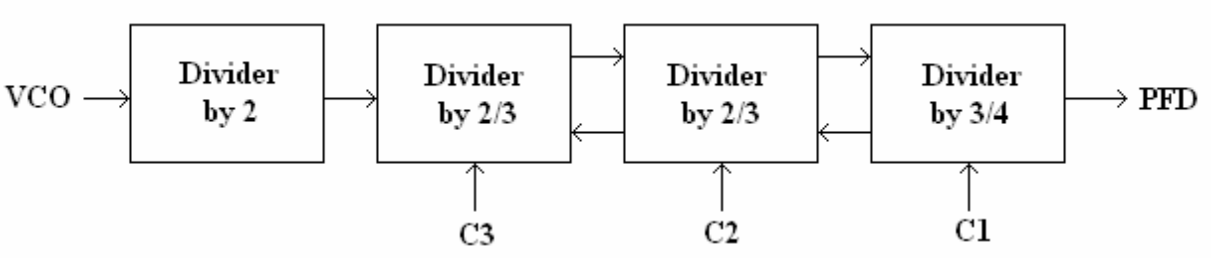



Fig. 3-8 Programmable frequency Divider Block Diagram

As shown in Fig. 3-8, a programmable frequency divider is implemented by cascaded a divider-by-2 circuit and three dual-modulus asynchronous frequency dividers. This design assures only the first divider works at the highest frequency and no pulse swallow counter or phase select state machine is needed. Moreover, the modulus-control signals of the last stage are produced first and given to the followed stage. Thus the delay in the critical path (the feedback of the first divider) is minimized[33]. In order to integrate the divider-by-2 into the loop, the division ratios are all even. In other words, a step increment is 2. The output frequency can be expressed by the following equation[34].

$$f_{out} = \frac{1}{2 \cdot (3 \cdot 2^2 + C1 \cdot 2^2 + C2 \cdot 2 + C3)} f_{in} \qquad (3\text{-}4)$$

The required division numbers are distributed over 24~34 while 36 and 38 are reserved for future integration with Band Group #5.

For the wideband locking-range and high reference frequency consideration, current-mode logic (CML) is adopted in the whole programmable frequency divider. The principle of divider-by-2 circuit is already described in Chapter 2. The dual-modulus /2/3 divider and its timing diagram are shown in Fig. 3-9. Every DFF is made up of master-slave latches. When MC bit is low, the output of the first DFF is always high and has no effect on the second DFF. It behaves as a divider-by-2 circuit. By contrast, when MC bit is high, the $V_m$ can be low and delay the negative half-cycle for one input clock. Therefore the division ratio is turned into 3. The NAND logic gates in Fig. 3-9 can be combined with the DFF as shown in Fig. 3-10[14]. The advantages of this structure over the conventional dual-modulus divider are its simpler and more symmetric layout, improved speed, fully differential schematic, and no extra current for the logic gates[35]. The dual-modulus /3/4 divider functions in a similar way. In Fig. 3-11, a DFF is inserted at the output to lengthen one more reference cycle. As a result, a variable division ratio of 3 or 4 is achieved. The complete multi-modulus frequency divider is shown in Fig. 3-12. Several feedback AND gates are inserted into the feedback path of the individual divider.

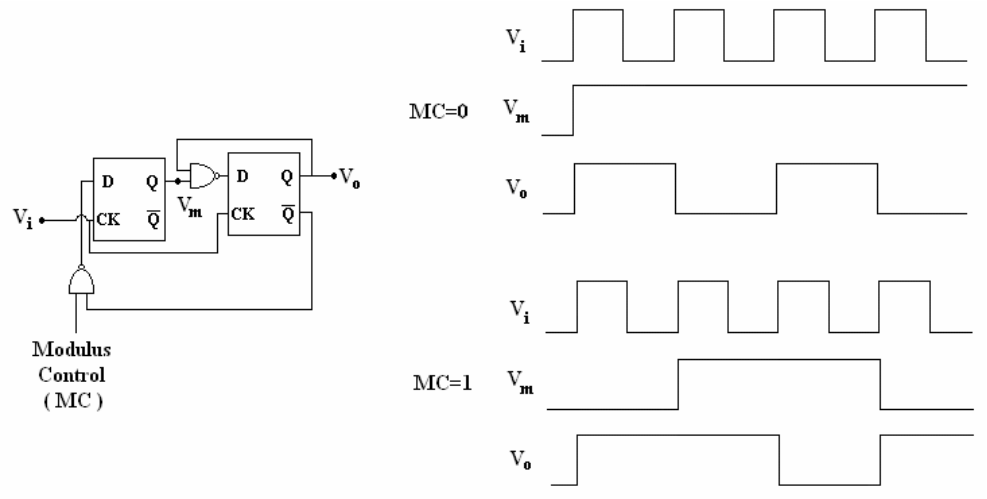



Fig. 3-9 Schematic of the /2/3 divider

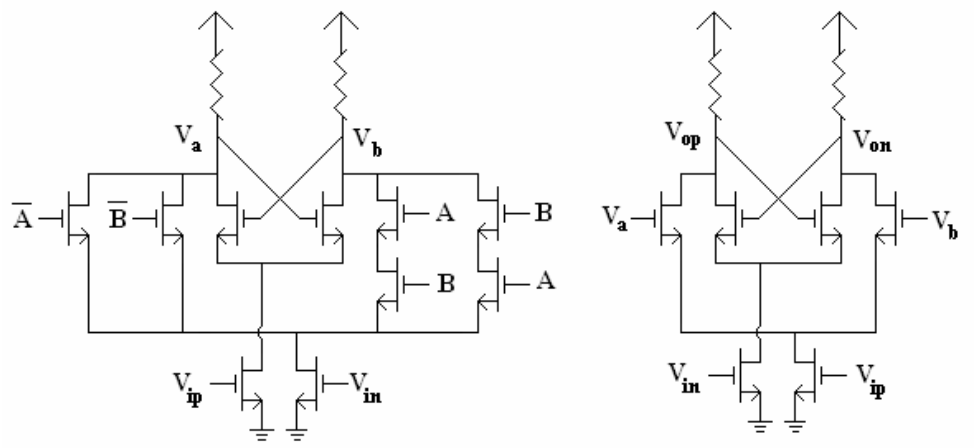



Fig. 3-10 Circuit implementation of the NAND/flip-flop combination

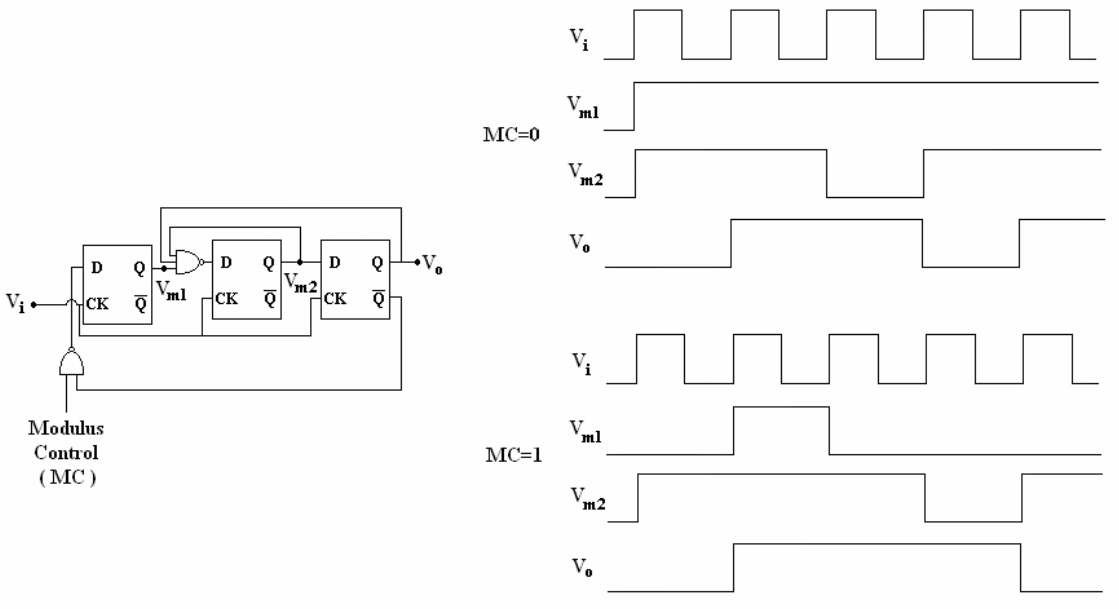



Fig. 3-11 Schematic of the /3/4 divider

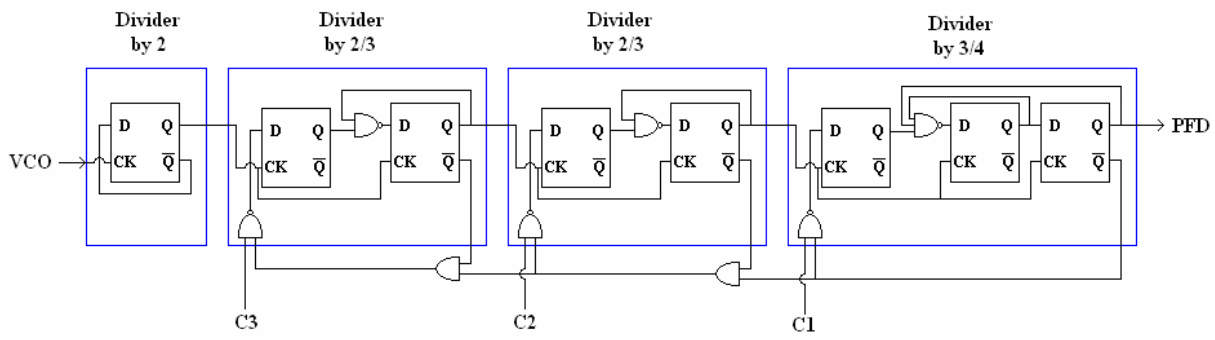



Fig. 3-12 Schematic of the programmable frequency divider

From the schematic, the first DFF in a dual-modulus divider is only loaded with one flip-flop while the second is with more than two including the next stage. Consequently, the

second DFF dissipates approximately twice power as much as the first one. Additionally the consumed power in a divider is also about 50% of the one in the previous divider because the maximum operating frequency halves. According to this power scaling rule, less power of the divider in this work than [24] can be explained. Both /4/5 and /3/4 frequency dividers are required and one divider-by-2 circuit is also essential for Band Group #1 carriers in [24]. It is assumed that the weight is one for a DFF loaded with a flip-flop in the first stage. If the load doubles or the maximum operating frequency halves, the weight will alter proportionally. According to Table 3-1, power dissipation is theoretically only 45.6% of the power in [24]. The DC power reduction is accomplished indeed.

Table 3-1 Theoretical comparison of power dissipation in dividers

| | **1st stage** | **2nd stage** | **3rd stage** | **4th stage** | **total** |
|---|---|---|---|---|---|
| **[24]** | 1+2+2 (/4/5)<br>1 (/2) | 1+2+2 (/3/4) | N/A | N/A | 6+5/2=8.5 |
| **This work** | 1 (/2) | 1+2 (/2/3) | 1+2 (/2/3) | 1+2+2 (/3/4) | 1+3/2+3/4+5/8=3.875 |

### 3.2.3 Fast Phase-Frequency Detector

The phase-frequency detector (PFD) compares two inputs from the reference clock and the output at the last stage of the frequency divider. The result decides that the control voltage of VCO is increasing or decreasing and then the output frequency is approaching to the desired value. A conventional tri-state PFD is widely used for the simplicity and wide comparable range of almost ±2π radians. Moreover it can detect both phase and frequency. The schematic of tri-state PFD is shown in Fig. 3-13. If REF arrives earlier, UP is triggered to high level and then reset to low level until DIV arrives; contrarily if DIV arrives earlier, DN is triggered to high level and reset to low level until REF arrives. Therefore greater phase error

causes longer duration which UP or DN is at high level. The characteristic curve is plotted in Fig. 3-13. Although the comparable range is supposed to be ±2π the comparison produces wrong signals when the phase error is near ±2π practically. This non-ideal phenomenon is from the delay buffer in the reset path of the PFD which is to avoid a dead zone problem. The actually valid phase comparison range shrinks to ±|2π-Δ|. Δ can be found out by

$$\Delta = 2\pi \cdot t_{delay} \cdot f_{REF} \qquad (3\text{-}5)$$

$t_{delay}$ is the delay time in the rest path and $f_{REF}$ is the reference frequency[36]. In a conventional design, the reference frequency is only a few MHz and Δ is small to ignore. Now the reference clock is 264 MHz and Δ becomes considerable. Therefore the control signal will not monotonically approach to lock-in range and the settling slows. While Δ is even larger than π, the possibility of incorrect comparisons is over 50% and the locking behavior may not be guaranteed anymore. In this case $t_{delay}$ is about 312 psec and Δ is 0.16π. This value can increase the setting time to some extent.

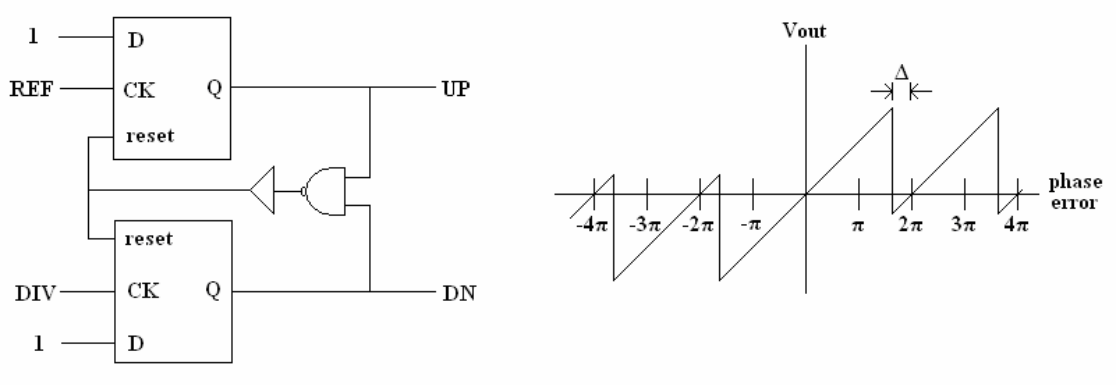



Fig. 3-13 Schematic and characteristic of a conventional PFD

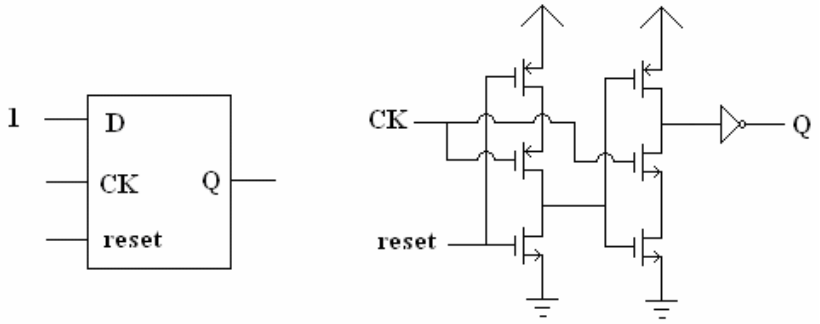



Fig. 3-14 Topology of TSPC-based DFF

In order to solve such a problem, the precharged PFD is used[36]. The DFF implemented in true single phase clock (TSPC) type is shown in Fig. 3-14. The precharged PFD is to insert one delay stage between CK and the input PMOS of TSPC-type DFFs and the schematic is shown in Fig. 3-15[24]. According to Fig. 3-15, this precharged PFD can still generate effective control signals when the phase error is close to $\pm 2\pi$. Despite of the similar characteristic, this PFD has some advantages over the proposed latch-based PFD in [36]. Lower power consumption and higher accuracy are obtained because the dynamic logic circuits have lower propagation delay and better matching. Fig. 3-16 shows the operation of the precharged PFD. td1 is the delay between REF and D_REF (DIV and D_DIV) and td2 is the duration from a rising edge of a lagging input between REF and DIV to the falling edge of the reset signal. At the second rising edge of REF, the phase error $\Phi$ is between $2\pi-\Delta$ and $2\pi-\delta$. At the falling edge of the following reset signal, D_REF is low and node A is charged to high level. Because REF is high at the same time, node B is discharged to low level and UP becomes high earlier than DN. Therefore the PFD does not miss the signal arriving during reset and provides correct control signal. At the third rising edge of REF, the phase error is greater than $2\pi-\delta$. The falling edge of the reset signal occurs while D_REF is already high. As a result, A cannot be charged to high level and B is still high. In other word, UP remains low and wrong comparison is made. Additionally, td1 is supposed to be a little shorter than td2, otherwise the PFD will not reach the locking state when the phase error is zero. The failure is caused by that reset still can charge node A for a "low" delayed input clocks. In a consequence, the valid comparison range is extended within $\pm|2\pi-\delta|$.

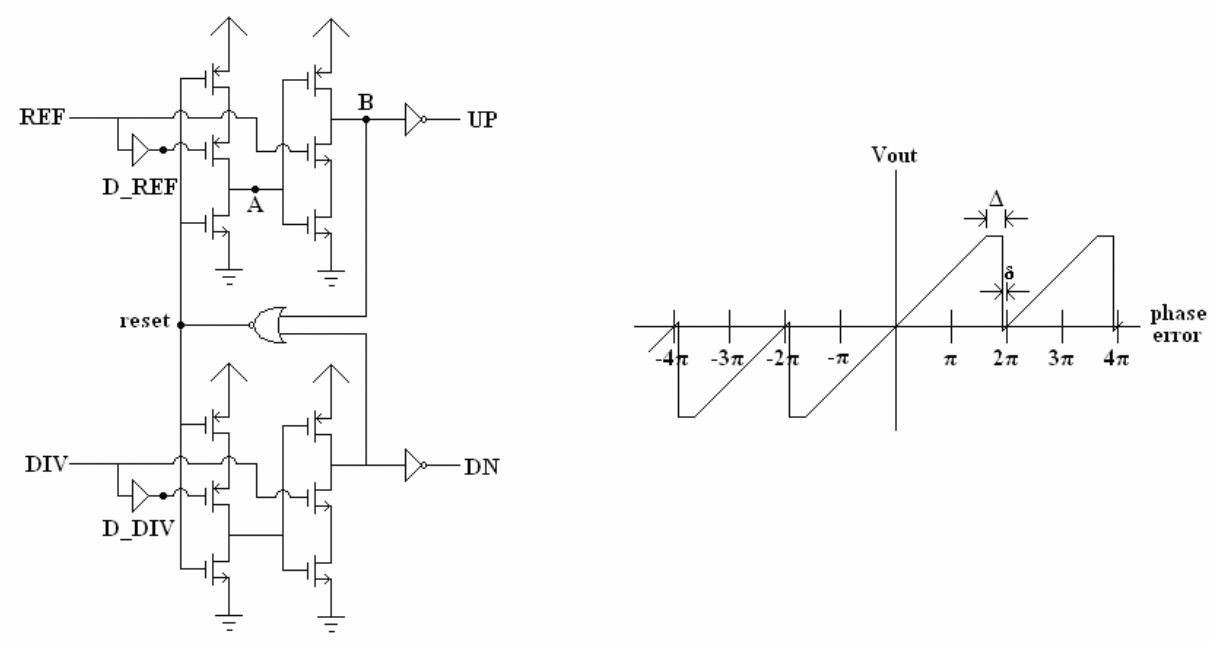



Fig. 3-15 Schematic and characteristic of a precharged PFD

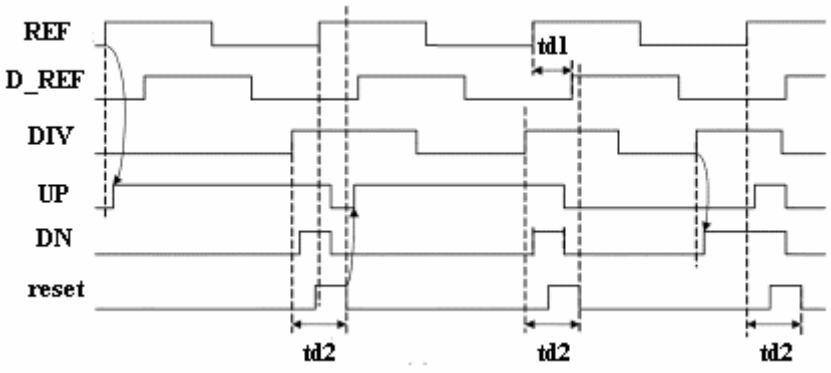



Fig. 3-16 Timing diagram of the precharged PFD

With a higher duty cycle of input clocks, the precharged PFD can operate at higher frequency because the inputs have to be high while the delayed inputs are rising. Luckily, the programmable frequency divider provides output with a duty cycle of 67% (C1=0) or 75% (C1=1). Assuming a 50% duty cycle, this precharged PFD functions properly at a frequency up to $0.5/t_{delay}$. In this circuit, the maximum operating frequency is around 1.6 GHz. Therefore the reference frequency of 264 MHz is much lower than the upper limit and PFD works reliably.

### 3.2.4 Charge Pump

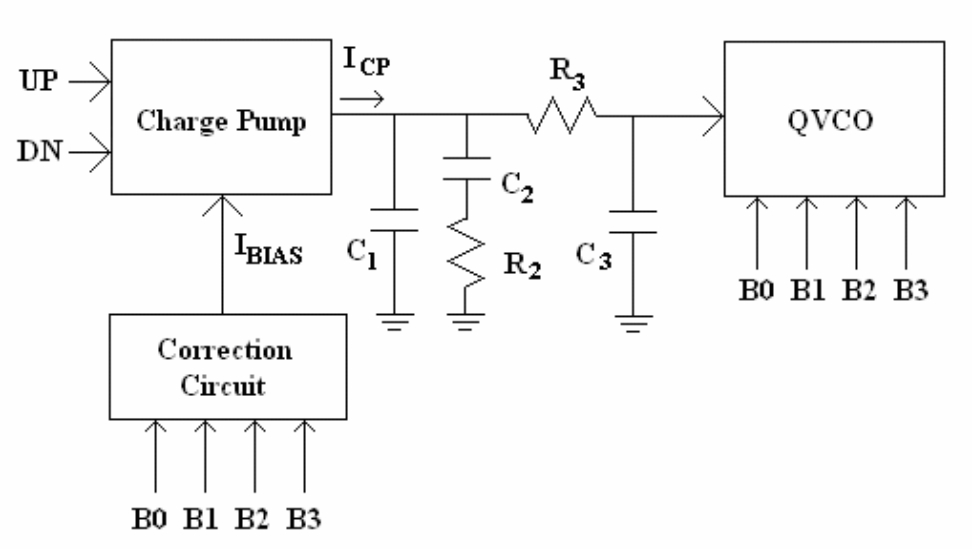



Fig. 3-17 Block diagram of charge pump, loop filter, and QVCO

According to [37], both the natural frequency and damping factor of a charge-pump PLL are proportional to $\sqrt{\frac{K_V . I_{CP}}{N_{DIV}}}$ where $K_V$ is the gain of VCO, $I_{CP}$ is the charge/discharge current, and $N_{DIV}$ is the division ratio. As mentioned in Chapter 2, $K_V$ changes with different tuning range curves. When the digital control signal of SCA is increased, more capacitors are included into the LC-tank. The gain of QVCO decreases because the ratio of varactor capacitance to total capacitance is reduced. Simultaneously the division ratio varies with the bank switching to reach a desired carrier frequency. In a consequence, $I_{CP}$ should be adjustable to keep natural frequency and damping factor fixed. A correction circuit is controlled by the same digital inputs of SCA and generates a variable reference current $I_{BIAS}$ to determine $I_{CP}$. The minimum $I_{CP}$ is chosen to be 2 mA for a reasonable design of the loop filter which will be discussed later.

The schematic of the complete charge pump with its correction circuit is shown in Fig. 3-18. At the left side, $I_{BIAS}$ is composed of five currents which are specified by the width of the MOS transistors. At the right side, a charge pump with complementary inputs is used[33]. To achieve a wide output voltage range of the charge pump, the size of current-mirror

transistors must be chosen carefully. Also a precise layout of the charge pump is important to improve the matching of charging and discharging currents. Mismatch currents produce spurious tones, interference with adjacent channel, and undesired spectral emission in RF front-end circuits. Two additional transistors ($M_{CP4}$ and $M_{CN4}$) are used to assure that the source nodes of $M_{CP3}$ and $M_{CN3}$ are already precharged when switching. This topology can reduce current peaks during the switching.

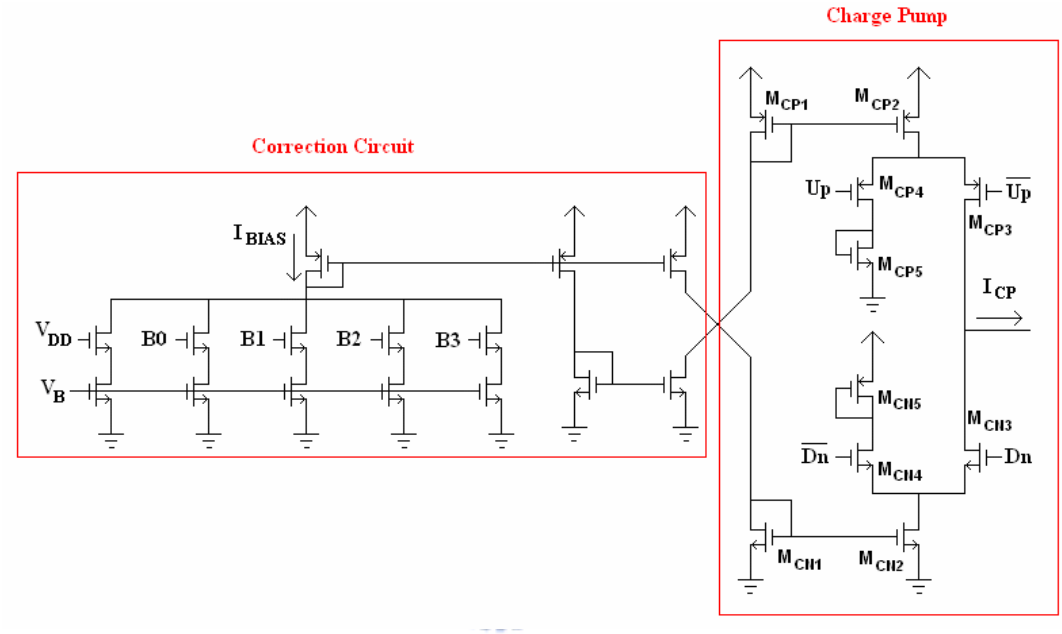



Fig. 3-18 Schematic of charge pump and its correction circuit

## 3.2.5 Loop Filter

The loop filter is the key parameter to decide the characteristic of a PLL since VCO, frequency divider, PFD and charge pump are already determined. In order to obtain the required values of elements in the loop filter, every block in PLL has to be linearly modeled in mathematics type and then integrated to predict the whole loop behavior.

At first, the oscillation frequency of the QVCO can be approximately expressed by a linear function of the control voltage though it is nonlinear actually.

$$f_{osc} = f_{free} + K_V \cdot V_{ctrl} \quad (3\text{-}6)$$

where $f_{free}$ is the free-running frequency and $K_V$ is the gain (or the sensitivity) of the VCO. Through the frequency divider, the oscillation frequency is divided by the division ratio N.

$$f_{div} = \frac{f_{osc}}{N} = \frac{K_V \cdot V_{ctrl}}{N} \quad (3\text{-}7)$$

For the simplicity, the term of $f_{free}$ is omitted. Due to phase comparison in PFD, the output frequency of the divider must be transformed into phase by integration. The relationship between the output phase and the control voltage is obtained in Laplace transform of Eq. ( 3-7 ).

$$\frac{\theta_{div}}{V_{ctrl}}(s) = \frac{2\pi}{s} \cdot \frac{K_V}{N} \quad (3\text{-}8)$$

Second, the phase error between the output phase and the reference clock is given by PFD and then amplified by the charge pump. For the loop gain calculation, the input reference clock is set to 0. Therefore, at the output of the charge pump, the current can be written by:

$$\frac{I_{out}}{\theta_{error}}(s) = \frac{I_{out}}{-\theta_{div}}(s) = \frac{I_{CP}}{2\pi} \quad (3\text{-}9)$$

Finally, the loop filter turns the current from the charge pump into the control voltage to adjust the oscillation frequency.

$$\frac{V_{ctrl}}{I_{out}}(s) = F(s) \quad (3\text{-}10)$$

where F(s) is the transfer function of the loop filter. Therefore the model of a PLL can be established in Fig. 3-19. The resultant loop gain can be represented as:

$$G(s) = \frac{I_{CP} K_V}{N} \cdot \frac{F(s)}{s} \quad (3\text{-}11)$$

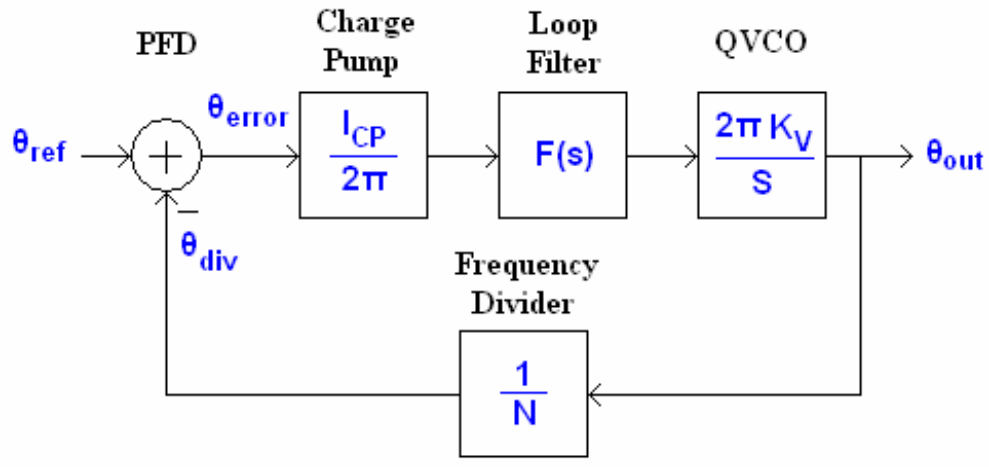



Fig. 3-19 PLL linear model

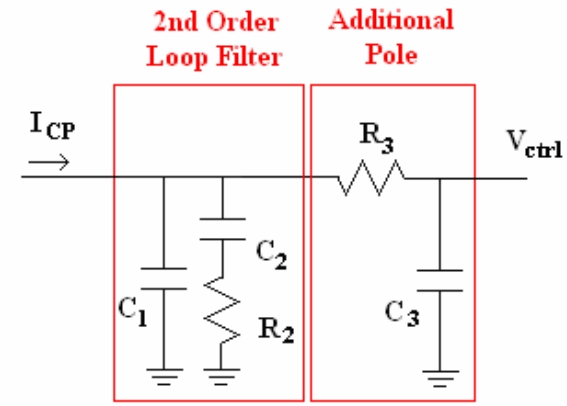



Fig. 3-20 Third-order passive loop filter

In this frequency synthesizer, a third-order passive loop filter is used as shown in Fig. 3-20. This kind of loop filters is widely used in modern frequency synthesizers. The transfer function of the loop filter can be found:

$$F(s) \cong \frac{1}{C_1 C_3 R_3} \cdot \frac{(s+\frac{1}{\tau_2})}{s(s+\frac{1}{\tau_1})(s+\frac{1}{\tau_3})} \qquad (3\text{-}12)$$

$$\tau_1 = R_2 \frac{C_1 C_2}{C_1 + C_2} \quad \tau_2 = R_2 C_2 \quad \tau_3 = R_3 C_3$$

The passive third-order filter avoids larger noise contribution from the op amp in the active filter. Moreover, the additional pole formed by $C_3$ and $R_3$ can attenuate more spurious tones from the current mismatch in the charge pump than the second-order filter. Now the complete transfer function of loop gain is

$$G(s) = \frac{I_{CP} K_V}{N C_1 C_3 R_3} \cdot \frac{(s + \frac{1}{\tau_2})}{s^2 (s + \frac{1}{\tau_1})(s + \frac{1}{\tau_3})} \qquad (3\text{-}13)$$

In the beginning of this section, the required loop bandwidth, reference clock, and phase margin are already decided. The current of the charge pump, the gain of VCO, and the division number are also obtained from the simulation. Since the closed-loop behavior is based on Eq. ( 3-13 ), the loop filter can be designed accordingly. As a result, the elements in the loop filter can be extracted under the condition of locking at 8.976 GHz[38]. With that, the remaining charge pump currents can also be calculated in order to reach the same settling time for different carrier frequencies.

### 3.2.6 Wideband Output Buffer

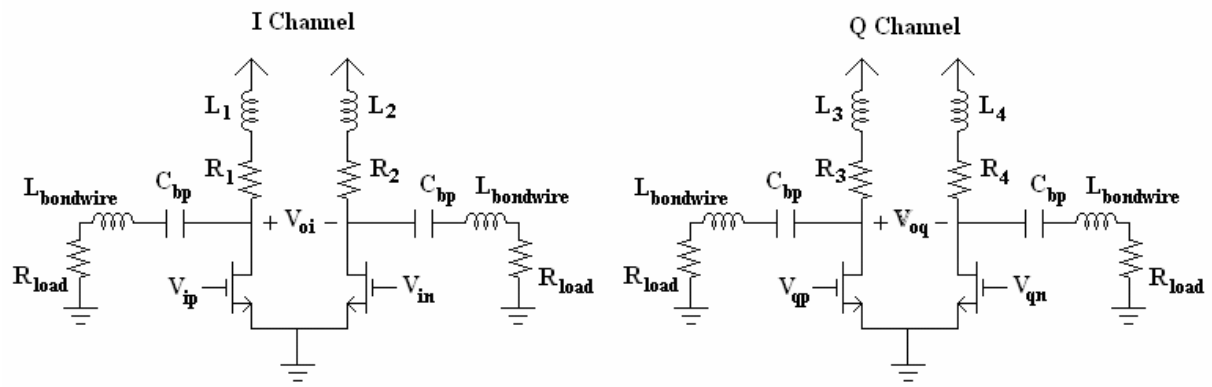



Fig. 3-21 Schematic of wideband output buffers

For the Band Group #3 and #4 in MB-OFDM UWB system, the signals produced from QVCO are spread in a wide range of 6~9 GHz. Therefore a reasonably flat frequency response is essential to keep the output power constant over all carrier frequencies. A conventional source-follower or common-source configuration is not suitable as an output buffer here. For example, the gain of a purely resistively loaded common-source amplifier is proportional to $g_m R_L$. When the parasitic capacitance load is included, the gain eventually falls off as frequency increases. In order to alleviate this, a shunt-peaking technique is adopted

for the bandwidth enhancement[39]. The schematic is shown in Fig. 3-21 and the bond wire is considered as a part of the load. A small resistor is in series with the inductor to extend the bandwidth. But there is a disadvantage: a bulky chip area because of four spiral inductors. To reduce the chip size, two center-tapped spiral inductors are used instead. The center-tapped spiral inductor is formed by two coupled inductors. The induced Eddy current can be eliminated for the differential mode operation because magnetic flux cancels each other while entering the lossy silicon substrate. In other words, less loss is achieved and Q-factor is improved. Here the center-tapped spiral inductor in this circuit is shown in Fig. 3-22. The effective inductance is 0.278 nH with a series resistance 0.91 Ω. The Q-factor is about 17.1 and actually higher than the nominal value of other spiral inductors.

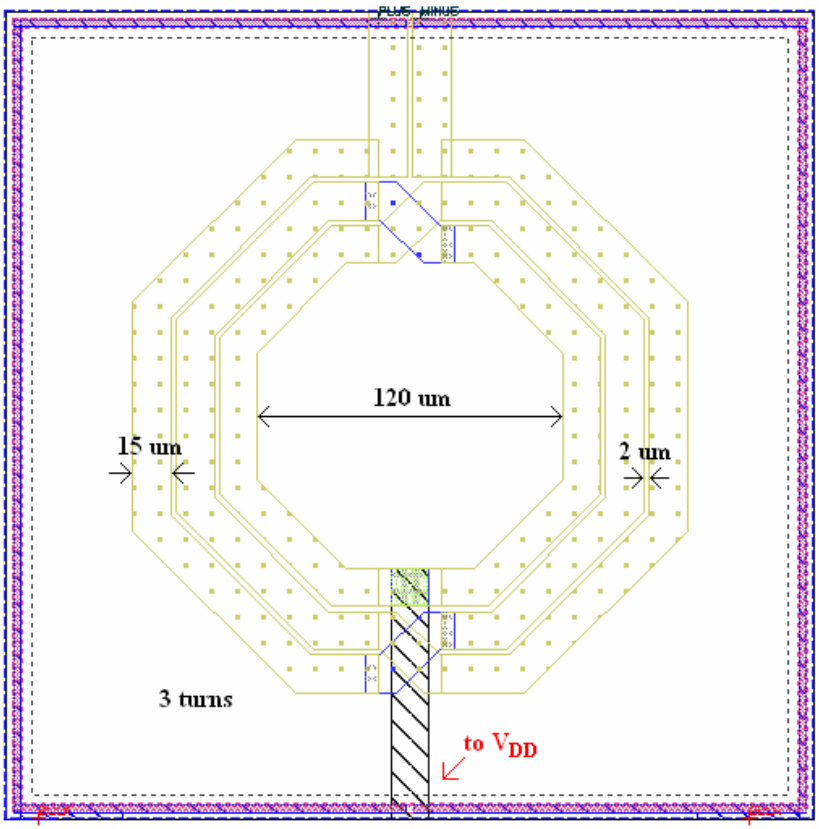



Fig. 3-22 Layout of the center-tapped spiral inductor

## 3.3 Chip Layout and Simulation Results

A low power and fast-locking frequency synthesizer is designed for MB-OFDM UWB system. TSMC RF 1P6M 0.18 μm CMOS technology is used for the simulation. The simulation is performed by Eldo RF. The layout of this frequency synthesizer is shown in Fig. 3-23 and occupies about 1.75x1.23 $mm^2$. As mentioned in Chapter 2, the parasitic effect is again extracted by both Calibre xRC for complete consideration in several giga-hertz band. The layout should be kept compact and symmetry for less undesired parasitic effect and more balanced outputs. The power dissipation of each block is listed in Table 3-2.

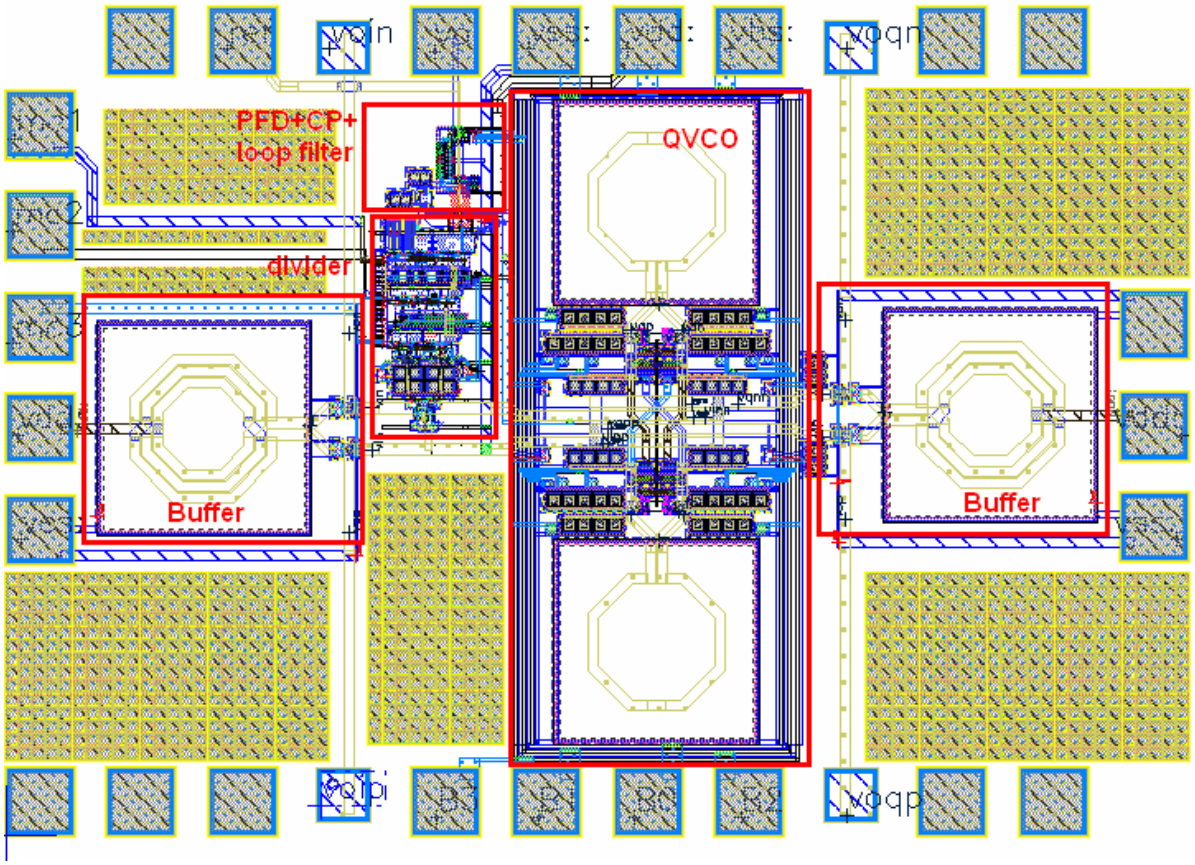



Fig. 3-23 Layout of the whole chip

Table 3-2 Power dissipation of every block in this PLL

| | Power (mW) | Current (mA) |
|---|---|---|
| **QVCO** | 11.09 | 7.39 |
| **Divider** | 21.64 | 14.43 |
| **PFD** | 0.35 | 0.24 |
| **Charge Pump** | 4.45~6.62 | 2.96~4.41 |
| **Buffers** | 10.17 | 6.78 |
| **total** | 47.7~50 | 31.8~33.3 |

### 3.3.1 Behavior Simulation

First, the tuning range curves of the QVCO are shown in Fig. 3-24. The total tuning range is about 3 GHz wide (6.2~9.2 GHz) and no gap occurs between each band. According to this, the gains of the QVCO $K_V$ can be obtained. As mentioned in Section 3.2.4, $\sqrt{\frac{K_V . I_{CP}}{N_{DIV}}}$ should keep constant with every carrier frequency. Therefore $I_{CP}$ can be extracted and listed in Table 3-3. The six carrier frequencies are distributed in six different banks. Now, except the loop filter, the linear models of all blocks in PLL are determined. According to [38], the elements of the loop filter is optimized and shown in Fig. 3-25. Additionally, due to the relatively wide loop bandwidth, the component values of the loop filter are quite small and on-chip integration is achieved for $C_1$, $R_3$, and $C_3$. As a result, the behavior simulation can be performed by MATLAB. It is to verify that these parameters in the circuit are reasonable. The closed-loop frequency response of the circuit is Fig. 3-26. In addition, the transient waveforms of these six carrier frequencies are simulated individually to assure the loop locking within the specified time. These waveforms are shown in Fig. 3-27 and the settling times are all about 200 nsec.

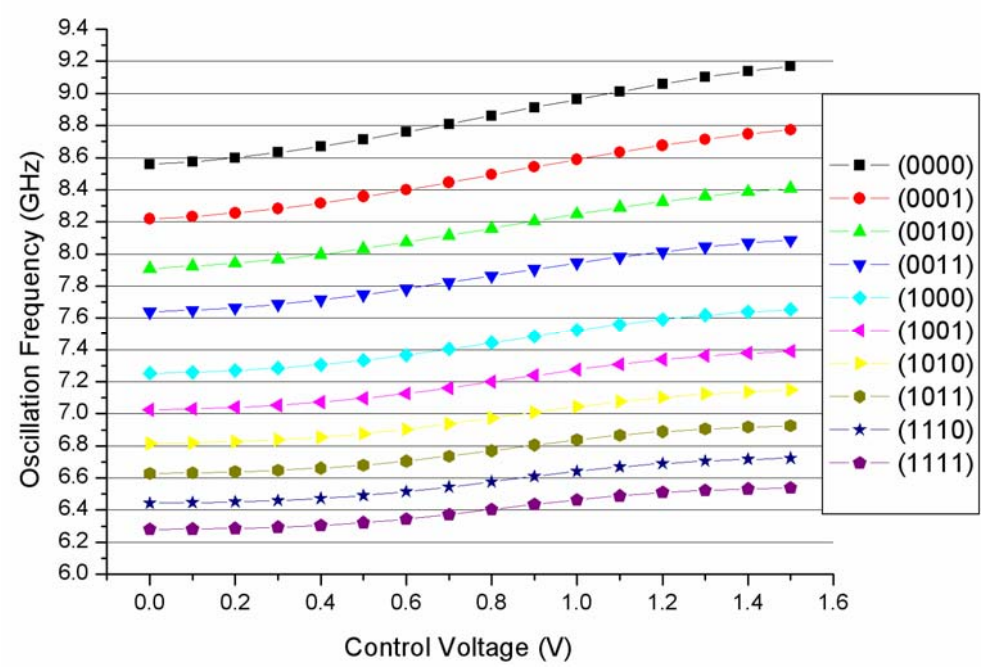



Fig. 3-24 Tuning range curves of the QVCO

Table 3-3 Parameters of the synthesizer with different banks

| Bank | Carrier (GHz) | $K_V$ (MHz/V) | N | $I_{CP}$ (mA) | Bank | Carrier (GHz) | $K_V$ (MHz/V) | N | $I_{CP}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|
| 0000 | 8.976 | 474.44 | 34 | 2 | 1001 | | 316.67 | | |
| 0001 | 8.448 | 436.67 | 32 | 2.1 | 1010 | | 293.33 | | |
| 0010 | | 401.11 | | | 1011 | 6.864 | 268.89 | 26 | 2.7 |
| 0011 | 7.920 | 364.44 | 30 | 2.3 | 1110 | | 255.56 | | |
| 1000 | 7.392 | 342.22 | 28 | 2.4 | 1111 | 6.336 | 238.89 | 24 | 2.8 |

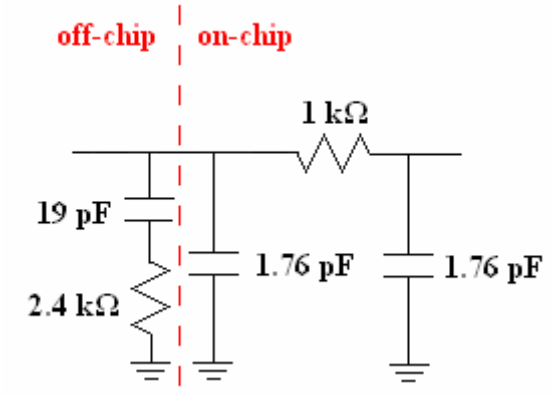



Fig. 3-25 Optimized loop filter

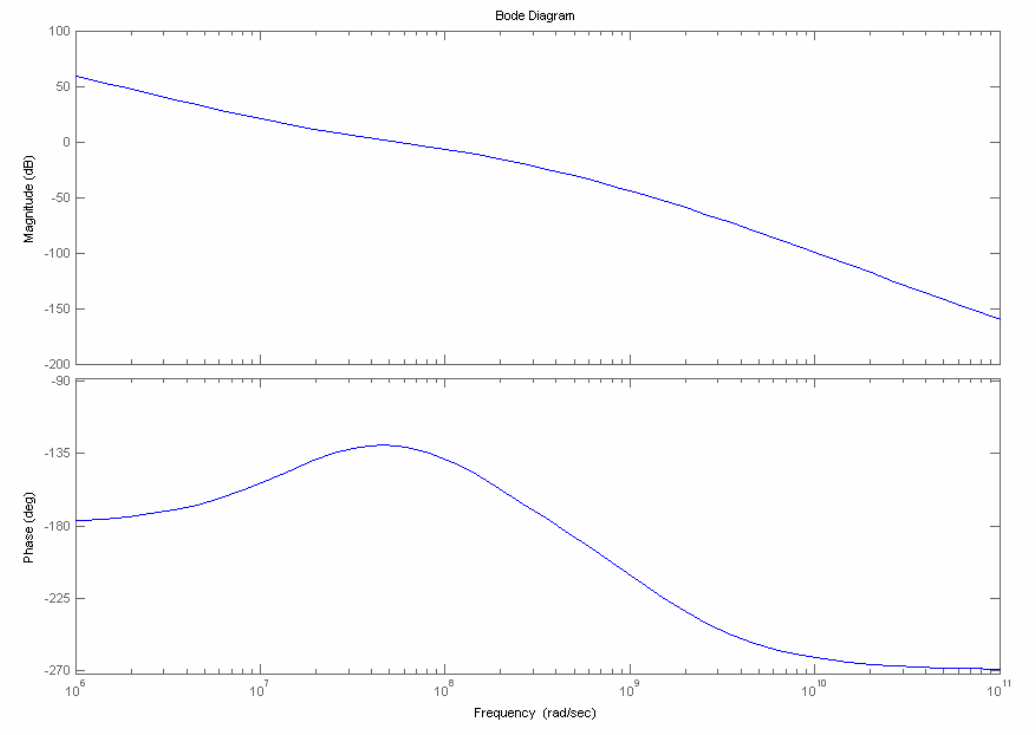
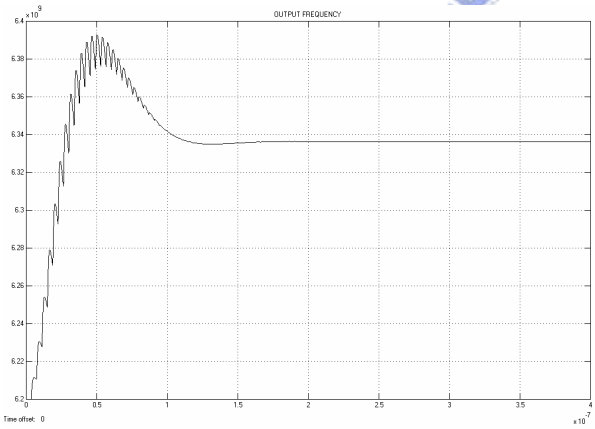
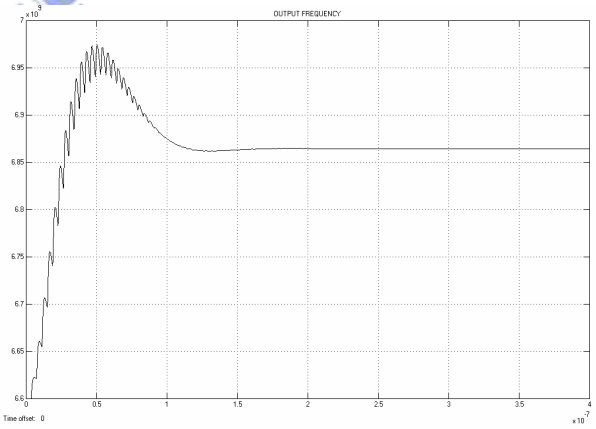


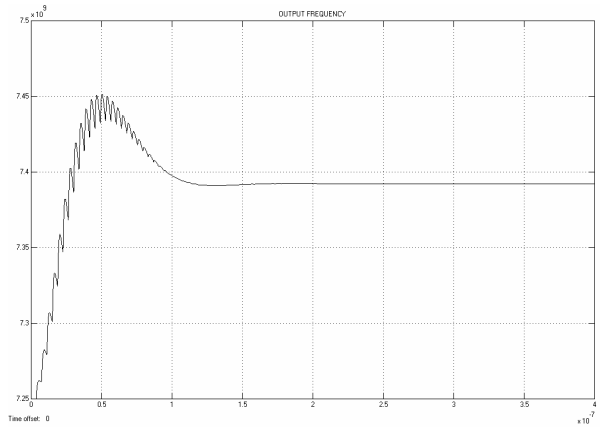

Fig. 3-26 Closed-loop frequency response of this circuit



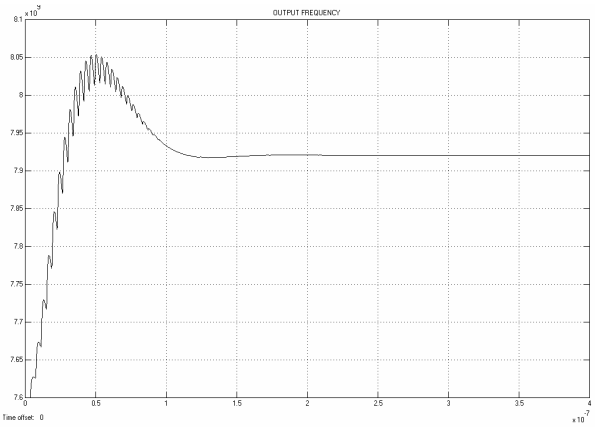

(a)6.336 GHz



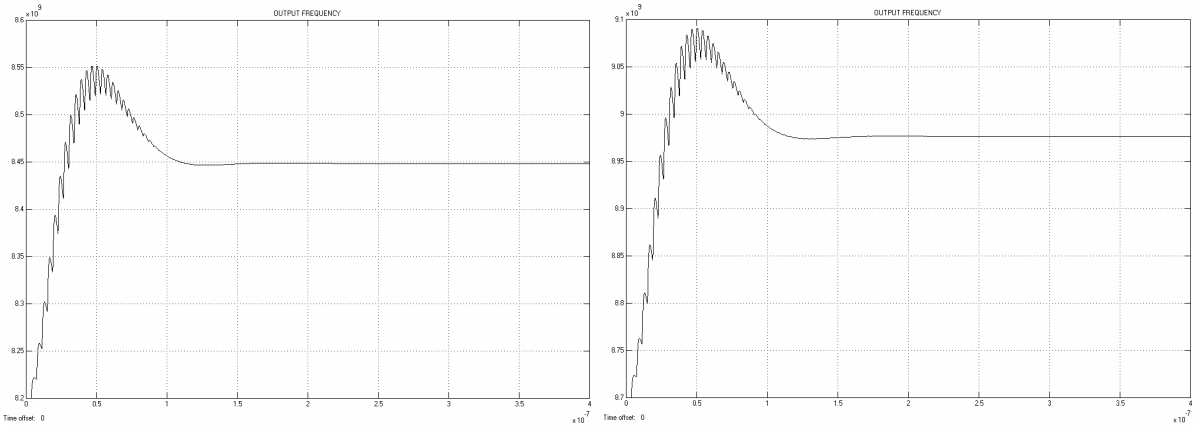

(b)6.864 GHz




(c)7.392 GHz




(d)7.920 GHz




(e)8.448 GHz (f)8.976 GHz

Fig. 3-27 Loop locking with six frequencies (behavior model)

## 3.3.2 Circuit Simulation

According to the simulation results from Eldo RF, the multi-modulus frequency divider works properly at 10 GHz maximally. The waveforms at four stages of the frequency dividers with a division ratio 34 are shown in Fig. 3-28 to prove its locking range. This ensures the output signal can be divided accurately to be compared with the reference clock at any time. Then, Fig. 3-29 shows the correct comparison result when REF leads DIV 0.95 cycle. Under the condition of bank (0000), the characteristic of the PFD and the charge pump is shown in Fig. 3-30 which is similar to Fig. 3-15. According to the simulation, the valid comparison range is about ±1.89π. It helps the loop to settle rapidly. Also the frequency response of the wideband buffer is shown in Fig. 3-31. The amplitude error in the desired band is smaller than 1 dB.

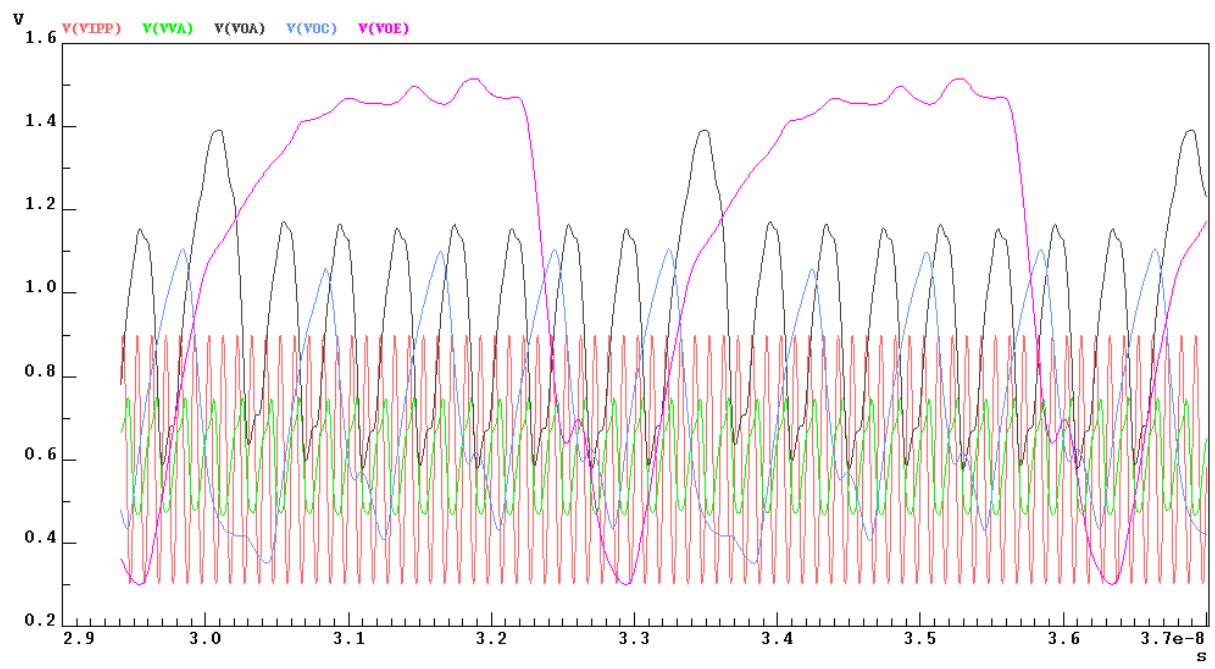



Fig. 3-28 Individual waveforms of dividers at 10 GHz input signal

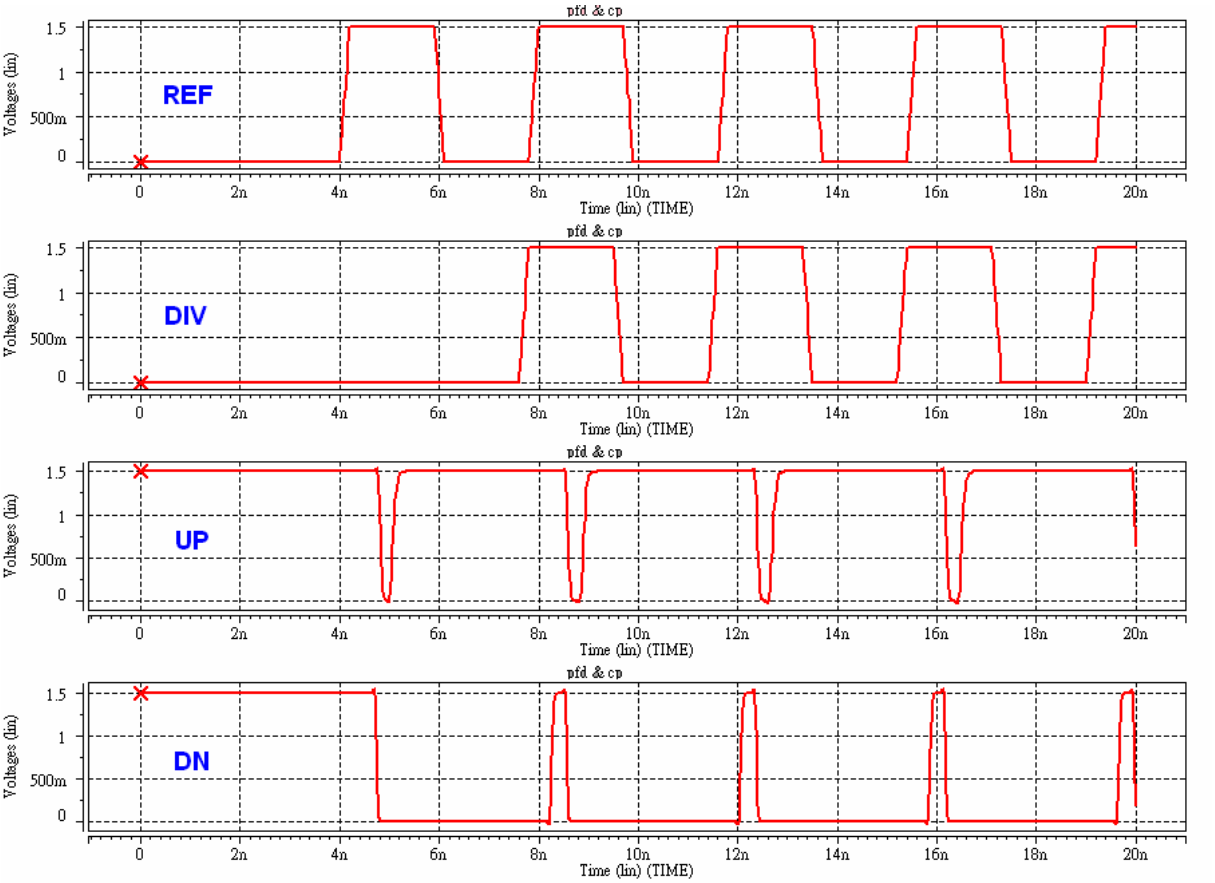



Fig. 3-29 Waveforms when REF leads DIV 0.95 period

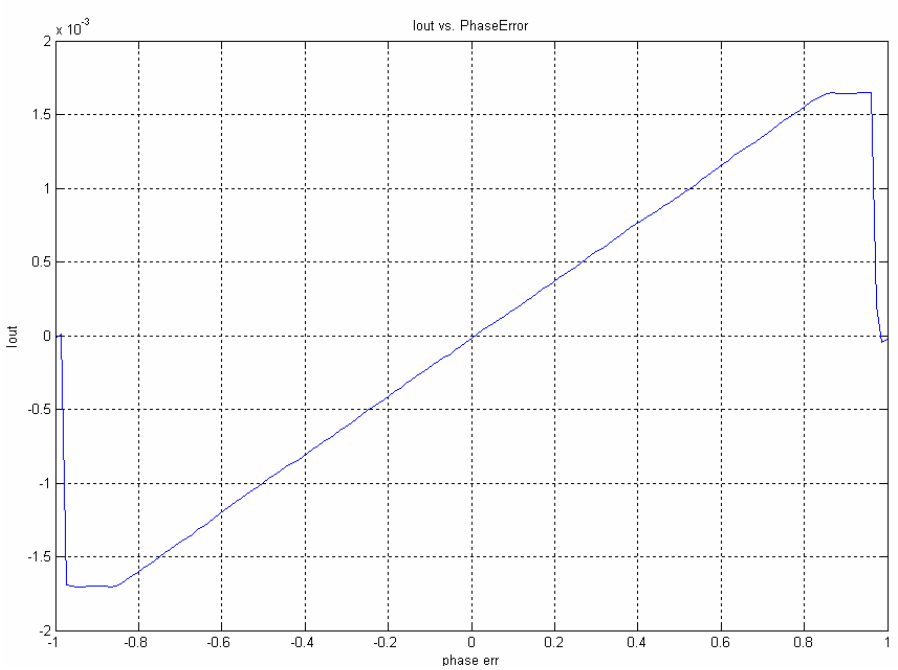



Fig. 3-30 Characteristic of the PFD and the charge pump

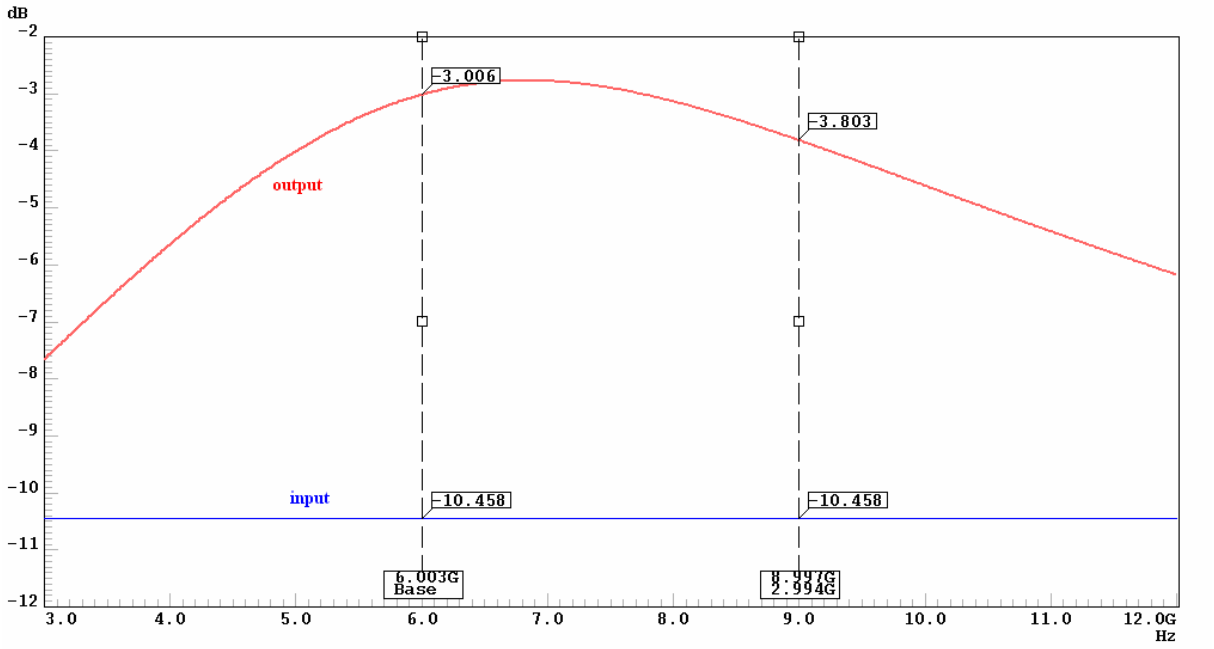



Fig. 3-31 Frequency response of the wideband buffer

The transient waveforms and power spectrums at six carrier frequencies are shown in Fig. 3-32~Fig. 3-43. The locking time is less than 300 nsec with different carriers. It is a little longer than the values in both the hand calculation and the behavior simulation. But this interval is still met the specification. The spurious tone is smaller than -34.2 dBc at 264 MHz offset. In fact, the spur is not critical in this synthesizer because the reference frequency is just

half of the channel bandwidth, which is an advantage mentioned in section 3.2. Moreover, the worst phase noise is -109.8 dBc/Hz at 1 MHz offset and far lower than the value (-86.5 dBc/Hz) specified in Section 1.2. Finally, according to Fig. 3-44, the maximal I/Q channel phase mismatch is about 3.1° and still tolerable in the system requirement.

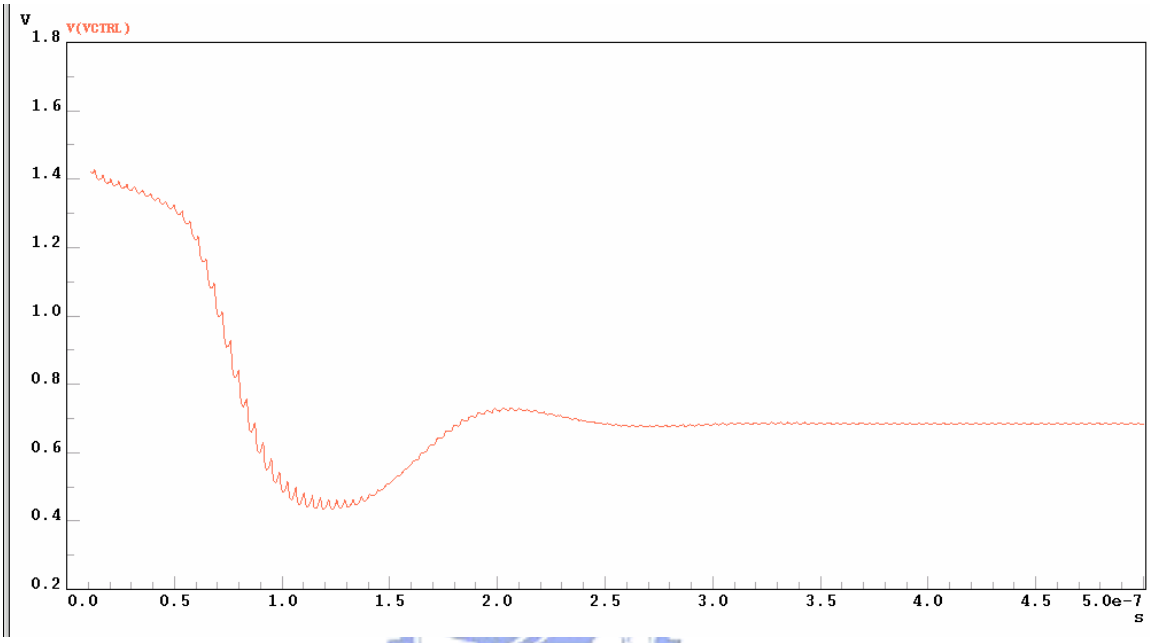



Fig. 3-32 Transient waveform when locking at 6.336 GHz

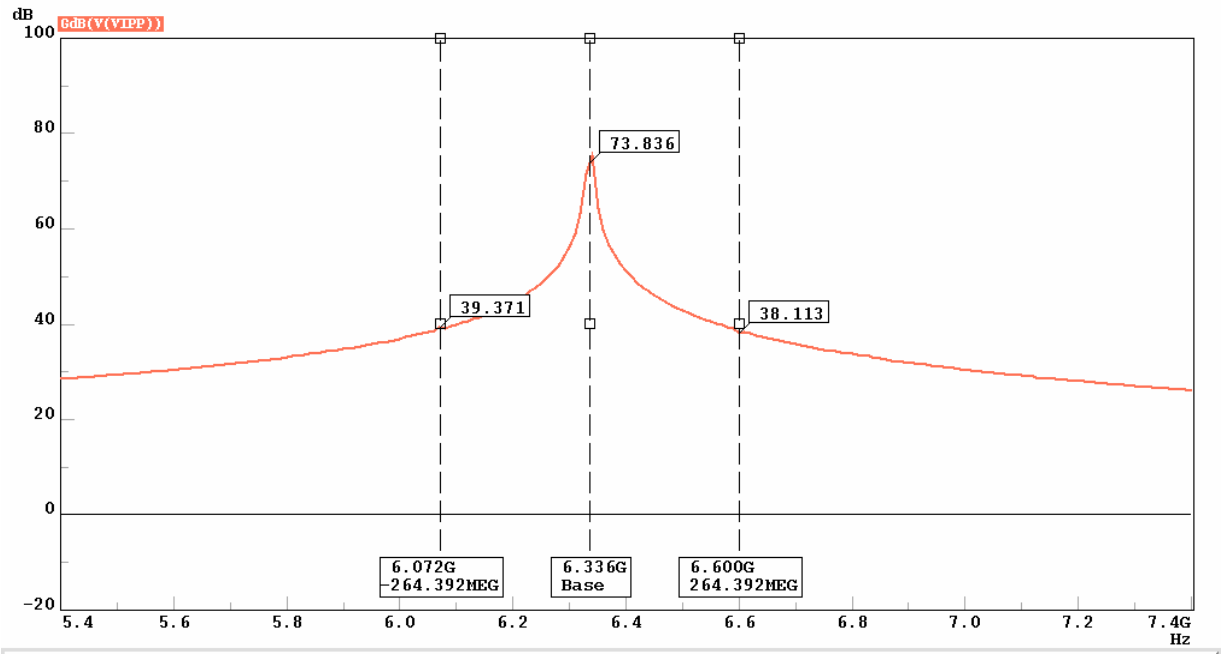



Fig. 3-33 Power Spectrum of the output at 6.336 GHz

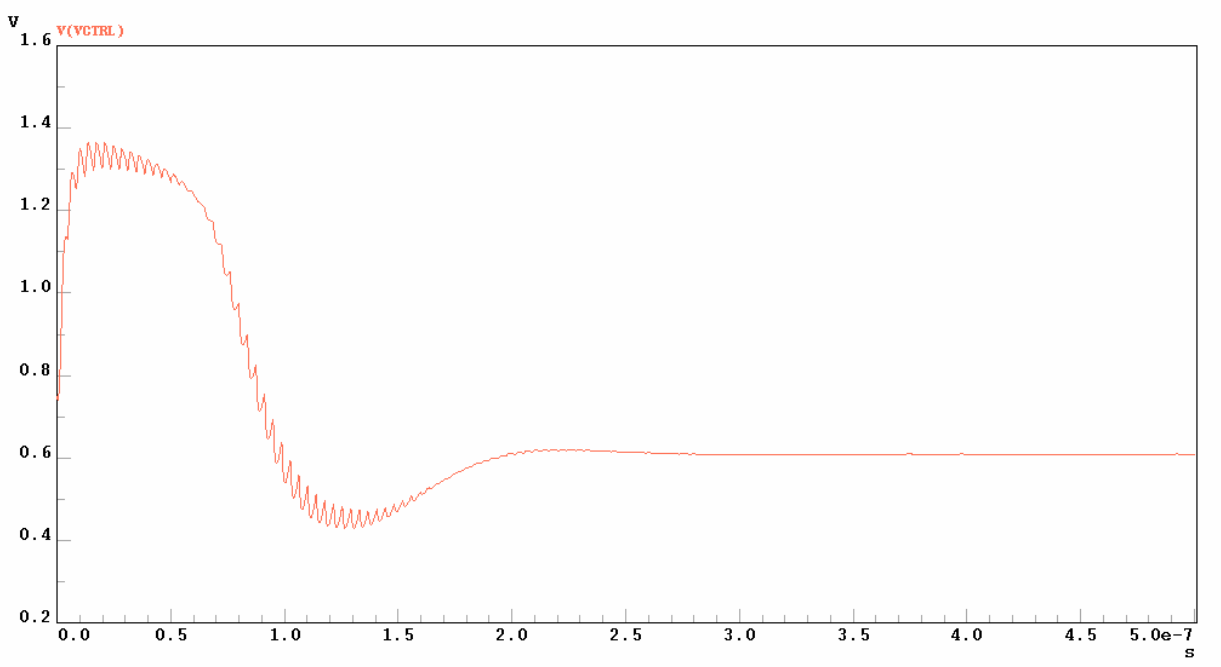



Fig. 3-34 Transient waveform when locking at 6.864 GHz

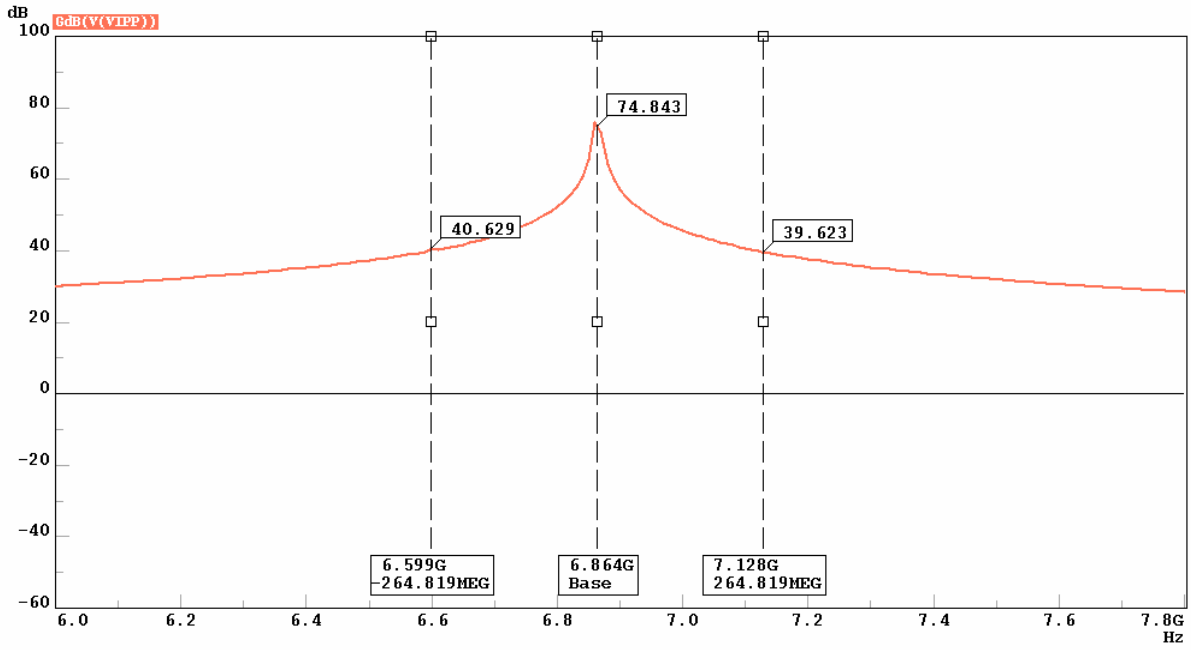



Fig. 3-35 Power Spectrum of the output at 6.864 GHz

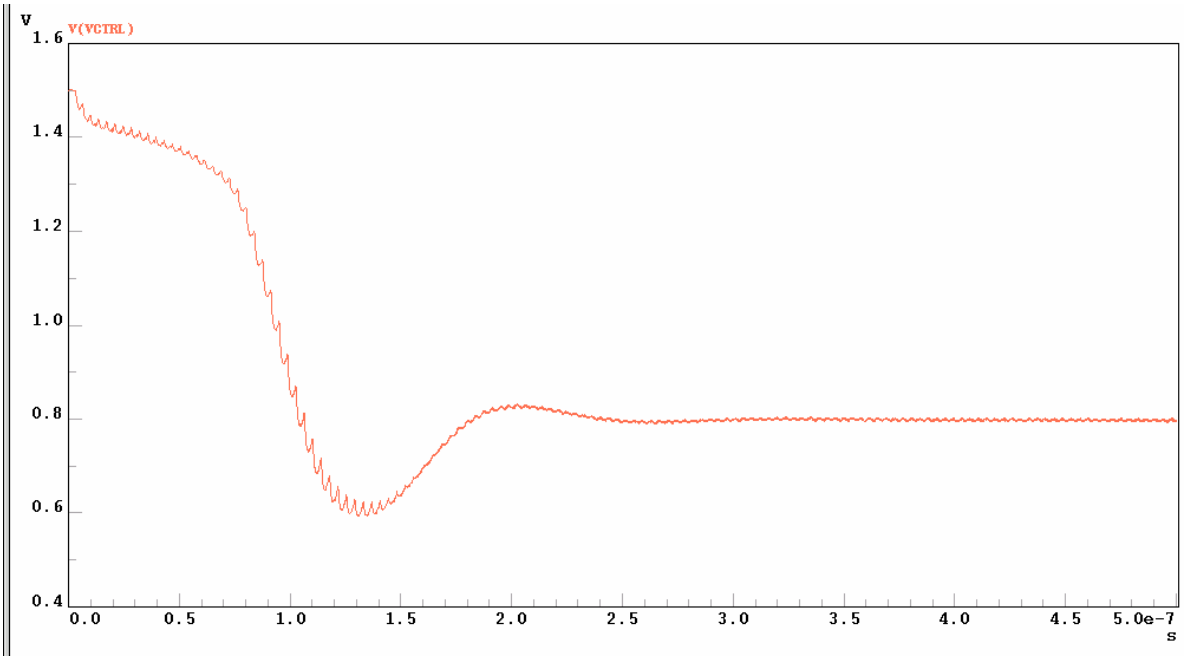



Fig. 3-36 Transient waveform when locking at 7.392 GHz

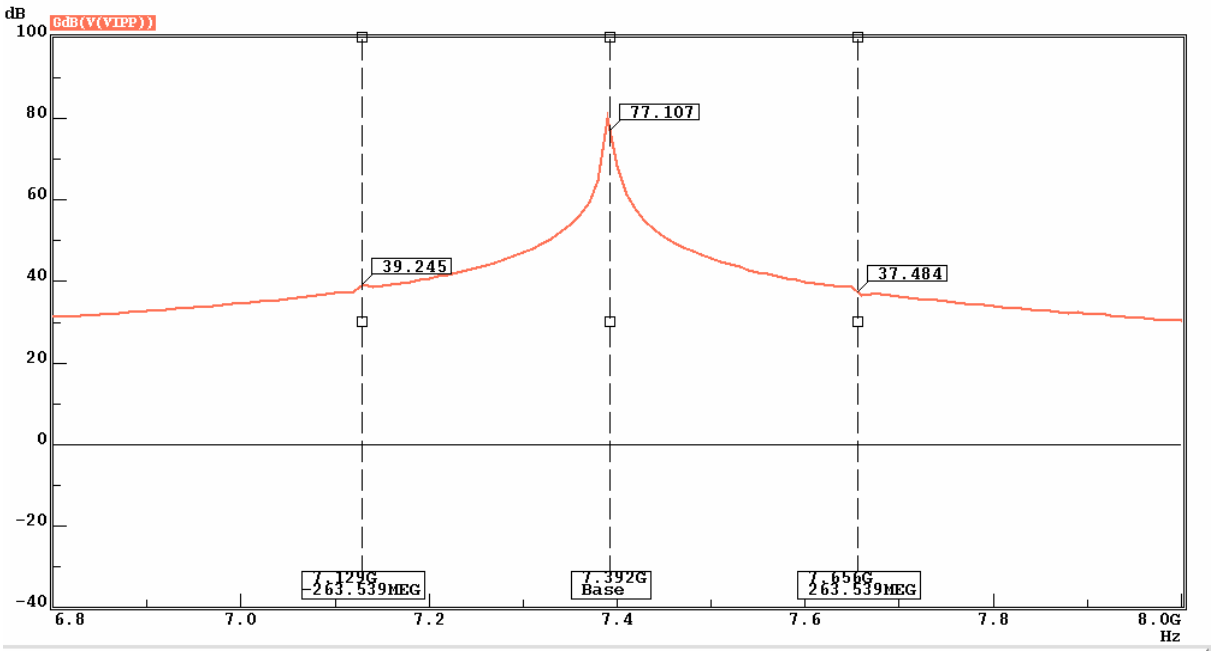



Fig. 3-37 Power Spectrum of the output at 7.392 GHz

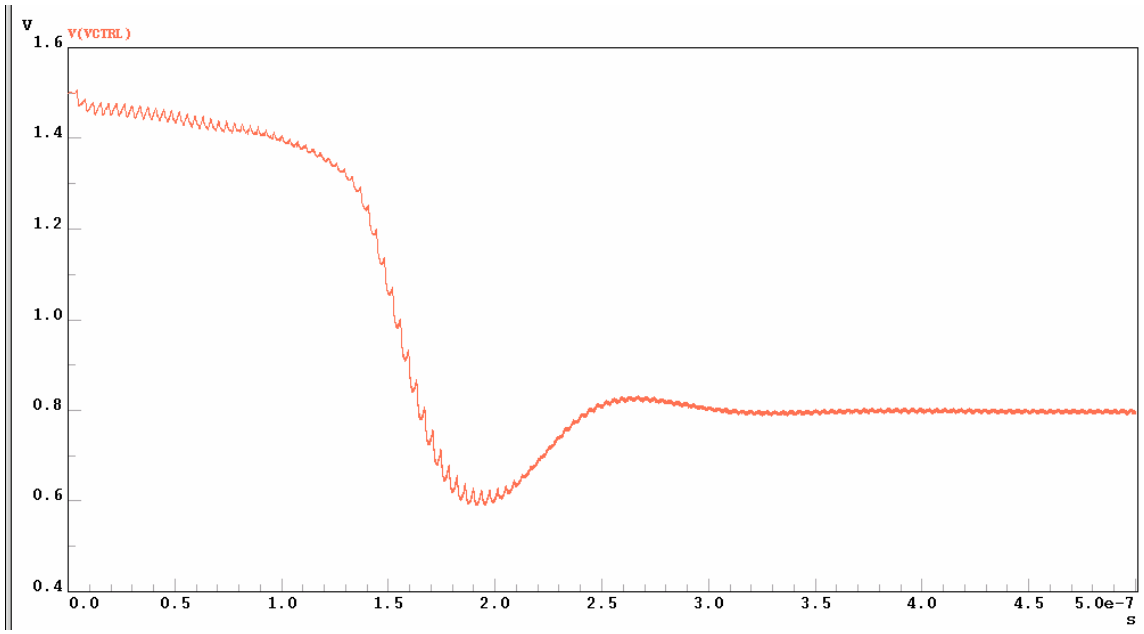



Fig. 3-38 Transient waveform when locking at 7.920 GHz

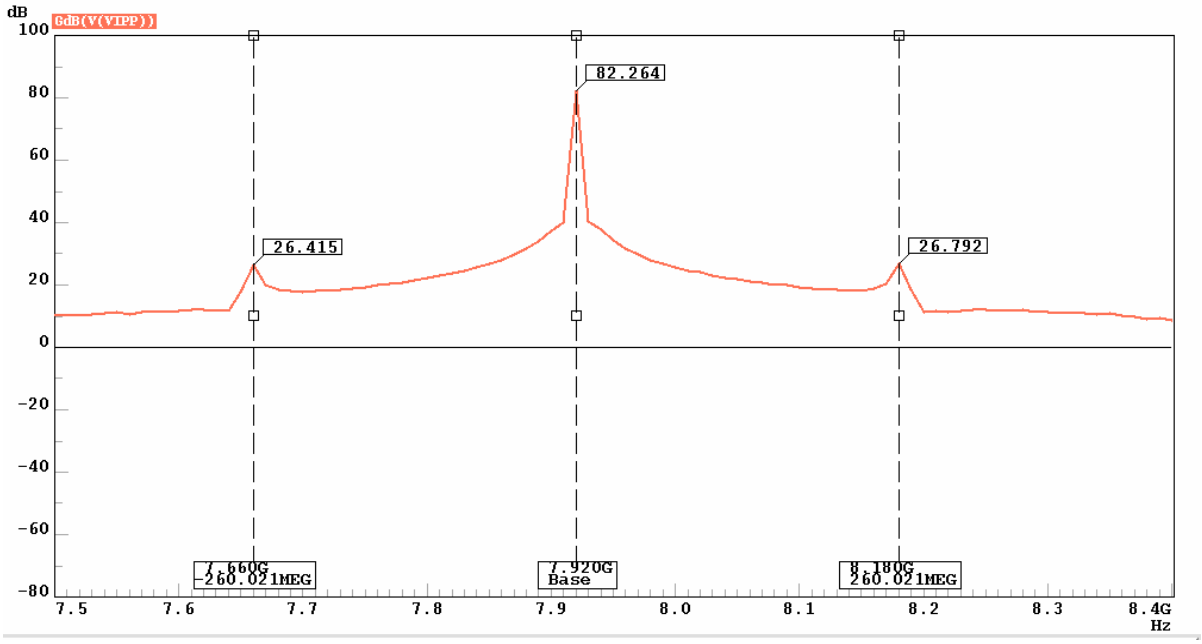



Fig. 3-39 Power Spectrum of the output at 7.920 GHz

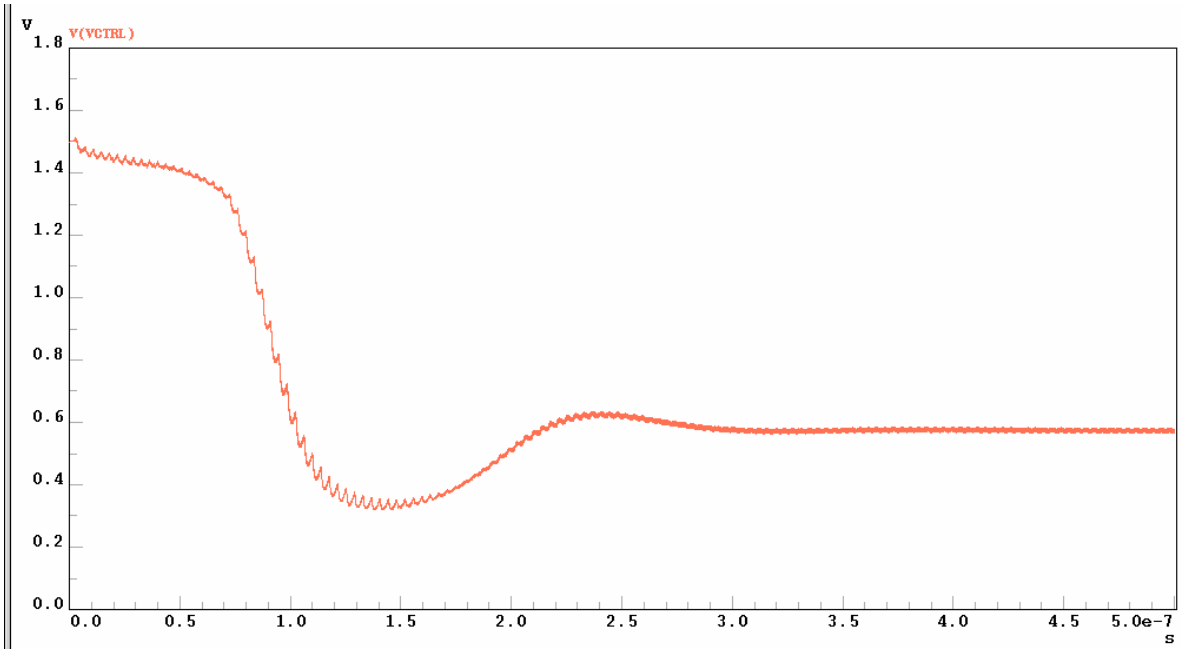



Fig. 3-40 Transient waveform when locking at 8.448 GHz

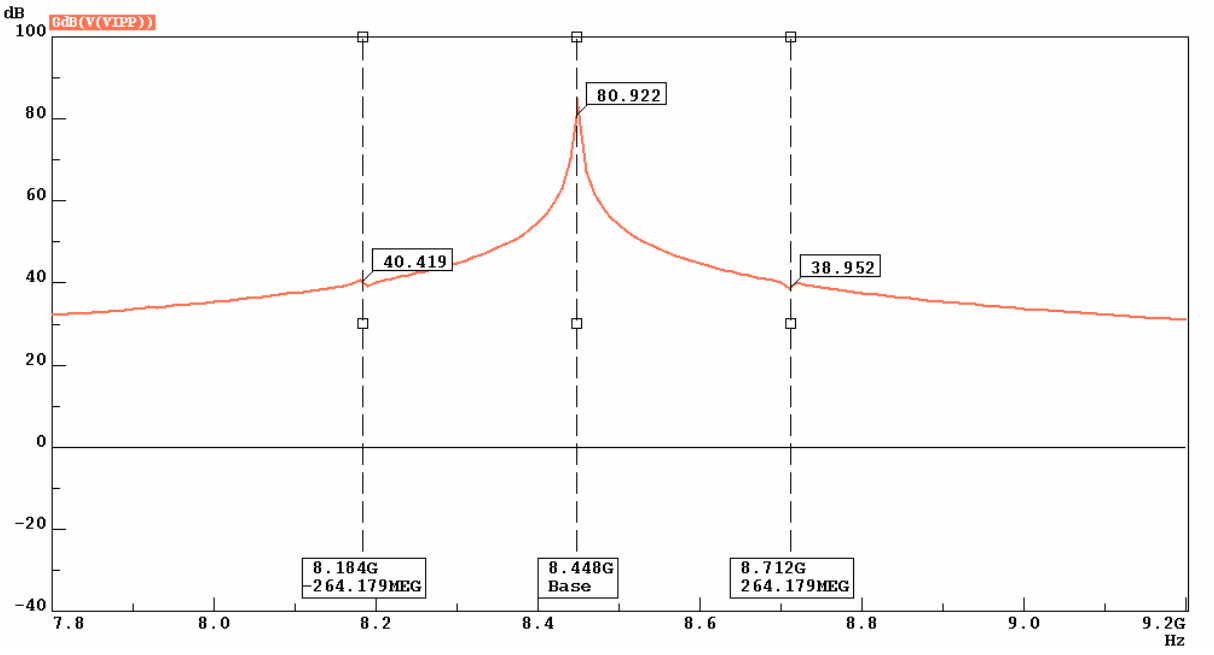



Fig. 3-41 Power Spectrum of the output at 8.448 GHz

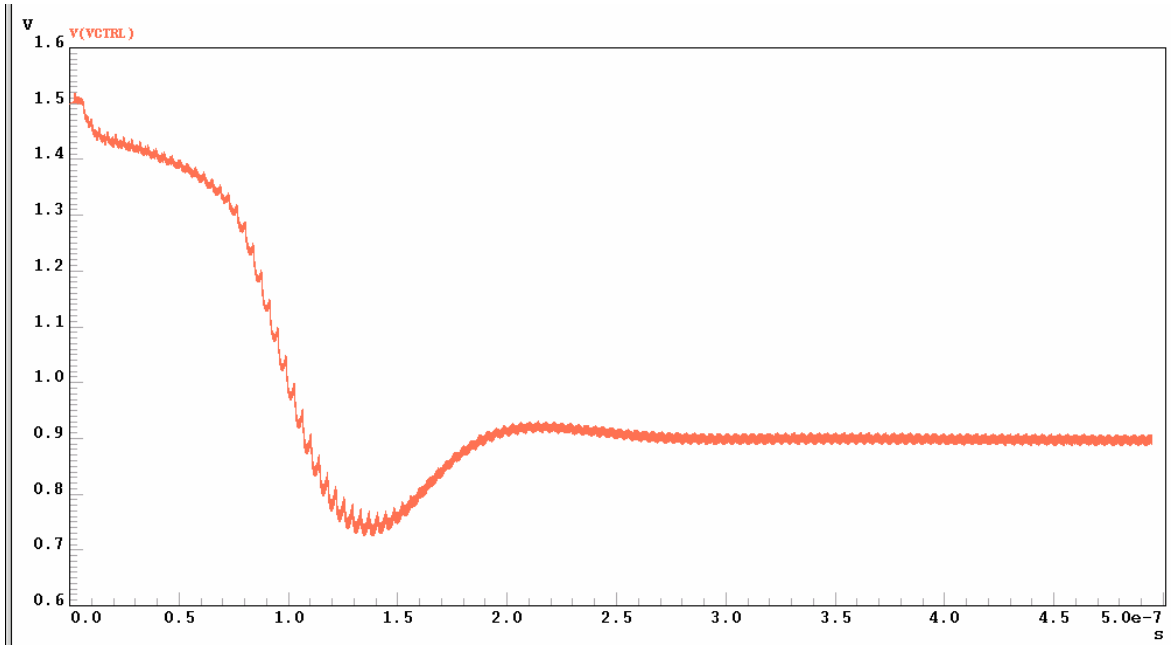



Fig. 3-42 Transient waveform when locking at 8.976 GHz

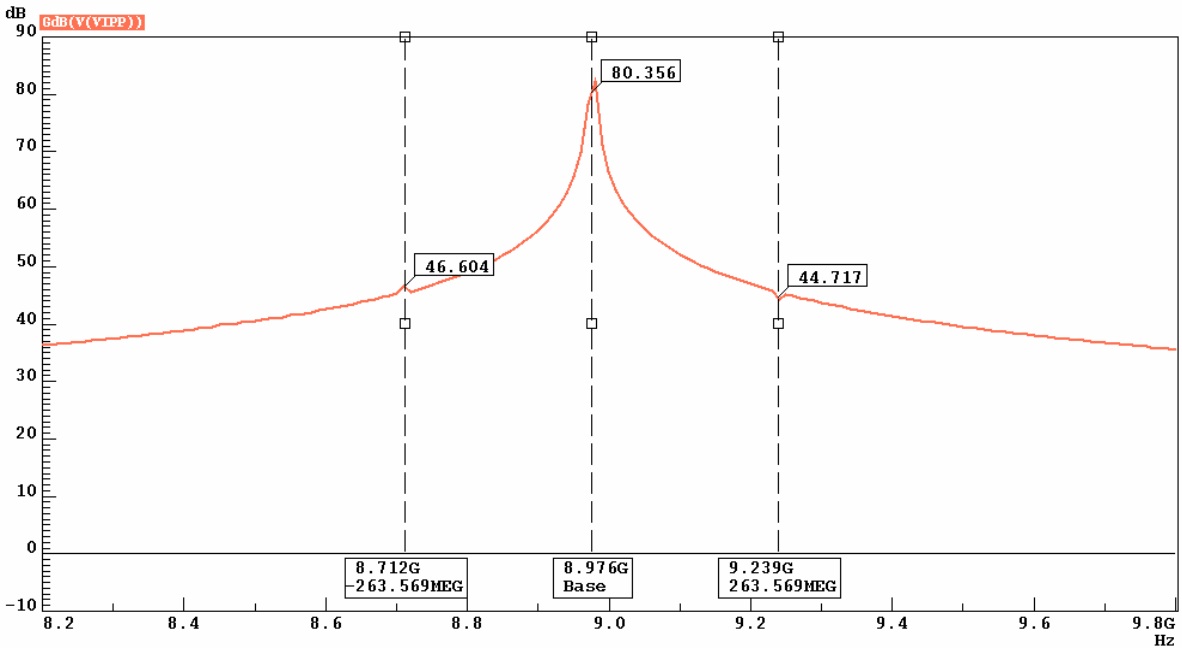



Fig. 3-43 Power Spectrum of the output at 8.976 GHz

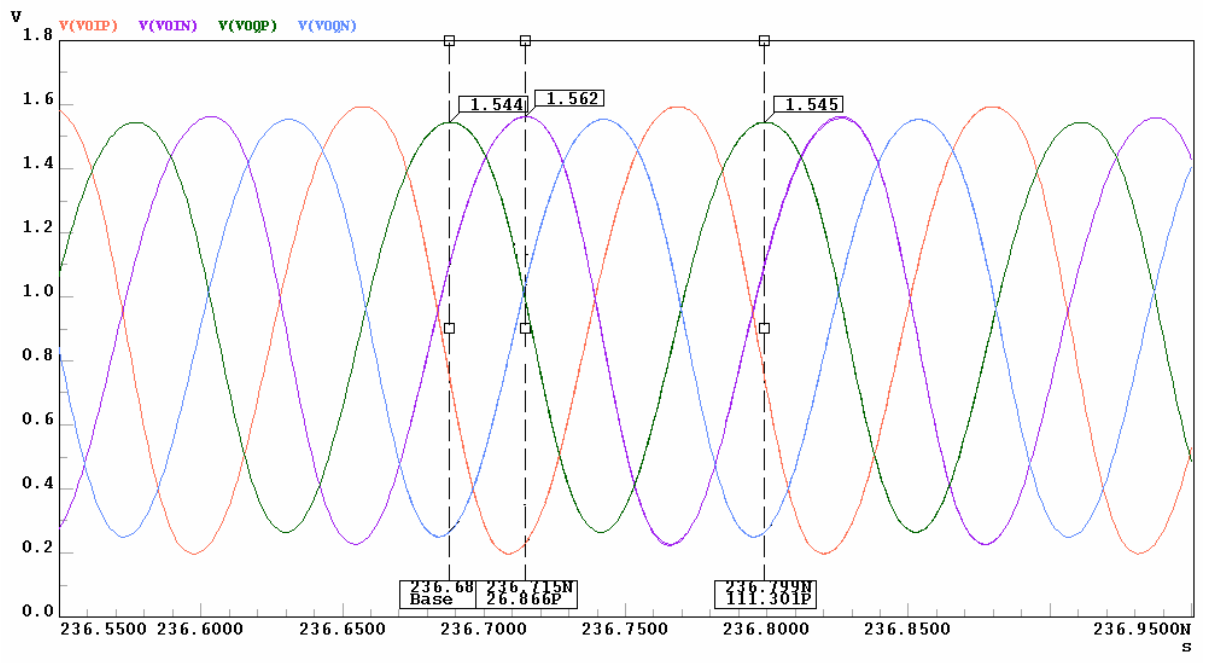



Fig. 3-44 Waveform of the quadrature output

## 3.4 Summary and Comparison

A fast-settling and low power frequency synthesizer is designed for MB-OFDM UWB system. The performance is summarized in Table 3-4. It meets all specifications which are found out in Section 1.2. The power dissipation in each block is also listed in Table 3-5. Due to the adjustable current in the charge pump, the total power consumption is varied from 46.35 to 48.24 mW. In the end, the comparison is made with the reference paper [24]. The major target of reducing power dissipation is achieved. This work consumes only 54.4% of the power in [24]. The noise performance is also better than the reference's. The setting time is approximately twice in consequence of slower reference clock. However, the specification is still met.

Table 3-4 Output power and noise performance of the six carrier frequencies

| Carrier Frequency | Output Power | Phase Noise @ 1 MHz offset | Spurious Tone | FOM |
|---|---|---|---|---|
| **6.336 GHz** | 1.08 dBm | -110.50 dBc/Hz | -34.5 dBc | 178.6 |
| **6.864 GHz** | 2.17 dBm | -109.83 dBc/Hz | -34.2 dBc | 178.6 |
| **7.392 GHz** | 4.10 dBm | -110.62 dBc/Hz | -37.9 dBc | 180.1 |
| **7.920 GHz** | 5.44 dBm | -113.63 dBc/Hz | -55.5 dBc | 183.7 |
| **8.448 GHz** | 6.41 dBm | -111.11 dBc/Hz | -40.5 dBc | 181.7 |
| **8.976 GHz** | 6.86 dBm | -110.34 dBc/Hz | -35.6 dBc | 181.5 |

Table 3-5 Power dissipation of each block

| | Power (mW) | Current (mA) |
|---|---|---|
| **QVCO** | 12.46 | 8.31 |
| **Divider** | 21.42 | 14.28 |
| **PFD** | 0.39 | 0.26 |
| **Charge Pump** | 4.46~6.35 | 2.98~4.23 |
| **Buffers** | 7.62 | 5.08 |
| **total** | 46.35~48.24 | 30.91~32.16 |

Table 3-6 Comparison with the reference paper

| | **JSSC, Aug. 2005[24] (measurement)** | **This work (simulation)** |
|---|---|---|
| **Technology** | 0.18 μm CMOS | 0.18 μm CMOS |
| **Voltage Supply** | 1.8 V | 1.5 V |
| **Reference** | 528 MHz | 264 MHz |
| **Frequency Tuning Range** | 6.17～9.11 GHz | 6.28~9.17 GHz |
| **Average Phase Noise (dBc/Hz)** | -109.48 @ 1 MHz | -111.01 @ 1 MHz |
| **FOM** | 178.53 | 180.7 |
| **Sidebands** | < -52 dBc @ 528 MHz | < -34.2 dBc @ 264 MHz |
| **Settling Time** | < 150 ns | < 300ns |
| **Power Dissipation** | | |
| **QVCO** | 14.4 mW | 12.46 mW |
| **Divider** | 31.5 mW | 21.42 mW |
| **PFD + CP** | 5.04 mW | 4.85 mW |
| **Buffers** | 34.2 mW | 7.62 mW |
| **total** | 85.14 mW | 46.35 mW |

# Chapter 4
# Conclusions and Future Work

## 4.1 Conclusions

In this thesis, a fast-locking and low power frequency synthesizer is designed for MB-OFDM UWB system. The locking time is less than 300 nsec to meet the specification when two frequency synthesizers are used by turns. This can avoid adopting many complicated single side-band mixers and multiplexers. The reference frequency is 264 MHz and the spurious tones have no undesired effect upon the channel. Moreover, the whole chip power dissipation is only 46.35 mW and greatly reduced because of the proposed topology of the programmable multi-modulus divider. The simulation results are listed and compared with the reference paper. It indeed shows a better performance.

In addition, a signal generator for MB-OFDM UWB system is also demonstrated. The VCO has a very wide tuning range (6.12~9.15 GHz) to cover Band Group #3 and #4. A divider-by-2 circuit follows the VCO and provides carriers in Band Group #1. Besides, a 2-to-1 wideband multiplexer has a flat frequency response over the 3~9 GHz and is included to select the output source: VCO or the divider. The measured tuning range and phase noise approximately agree with the simulation results. The best phase noise is -115 dBc/Hz at 1 MHz offset. The total power consumption is 36.63 mW while the VCO core dissipates 7.09 mW. By the power-frequency-normalized figure-of-merit (FOM), a VCO with both wide tuning range and low phase noise is presented in this circuit.

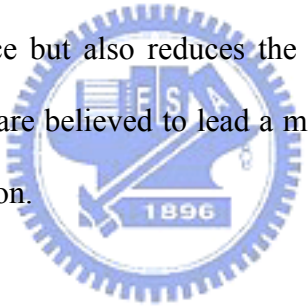
Table 4-1 Performance of two works in this thesis

| | **MB-VCO and Its Frequency Divider** | **Fast-Locking and Low Power Frequency Synthesizer** |
|---|---|---|
| **Technology** | 0.18 μm CMOS | 0.18 μm CMOS |
| **Voltage Supply** | 1.8 V | 1.5 V |
| **Reference** | NA | 264 MHz |
| **Frequency Tuning Range** | 6.12～9.15 GHz | 6.28~9.17 GHz |
| **Average Phase Noise (dBc/Hz)** | -115 @ 1 MHz | -111 @ 1 MHz |
| **FOM** | 183.3 | 180.7 |
| **Sidebands** | NA | < -34.2 dBc @ 264 MHz |
| **Swiching Time** | < 1 ns | < 300ns |
| **Power Dissipation** | | |
| **QVCO** | 7.09 mW | 12.46 mW |
| **Divider** | 9.43 mW | 21.42 mW |
| **PFD + CP** | | 4.85 mW |
| **Buffers** | 20.11 mW | 7.62 mW |
| **total** | 36.63 mW | 46.35 mW |

## 4.2 Future Works

There are several ways to improve the design of the frequency synthesizer for MB-OFDM UWB system. First, the wideband multiplexers have to replace the output buffers.

As a result, both the QVCO and divider-by-2 circuit can provide carriers for Band Group #1, #3, and #4. This leads a larger load for the divider-by-2 circuit. Therefore the divider should be re-designed and a complicated layout needs to be planned well. Second, the adopted passive loop filter produces less noise but causes the narrower valid range at the control voltage. In consequence, the carrier frequencies should be located at the centers of tuning range curves for predicted transient behavior and low spur. If an op-amp can be implemented with low noise, the performance is supposed to be improved further. Third, the EM parasitic effect has to be extracted more extensively. This takes much longer time in simulation but brings more reliable results. Finally, the supply voltage is chosen as 1.5 V for battery use. In the measurement, the battery means less noise and cleaner DC source. For the practical application, band-gap reference circuits can be used for every bias voltage. It not only improves the noise performance but also reduces the number of the required pads. All the mentioned future works above are believed to lead a mature frequency synthesizer design for the MB-OFDM UWB application.



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# Publishing Remarks

## International Conference Paper:

1. **Shih-Hao Tarng** and Christina F. Jou, "A 10 GHz Low Power CMOS Quadrature Voltage-Controlled Oscillator," *IEEE Asia-Pacific Microwave Conference (APMC),* Vol. 2, Dec. 2004

## Submitting Papers:

1. **Shih-Hao Tarng** and Christina F. Jou, "A Fully-Integrated, Low Power, Fast-Locking, Integer-N Frequency Synthesizer for MB-OFDM UWB System," *Progress In Electromagnetics Research Symposium (PIERS),* Mar. 2007
2. **Shih-Hao Tarng** and Christina F. Jou, "A Signal Generator for MB-OFDM UWB System in 0.18 um CMOS Process," *Progress In Electromagnetics Research Symposium (PIERS),* Mar. 2007