國 立 交 通 大 學

電信工程學系

碩 士 論 文

應用於數位電視寬頻調諧器之
三角積分調變頻率合成器

Delta-Sigma Frequency Synthesizer for DTV Broadband RF Tuner

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中 華 民 國 95 年 10 月

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摘　　要

近年來，射頻積體電路(RFIC)技術迅速地發展演進。由於低成本以及低功率消耗等優點，射頻積體電路在於無線通訊上的應用更是引人注目。在設計收發機系統時的一大挑戰，便是在於如何合成所需要的任何本地震盪源(LO)訊號。因此，頻率合成器隨即被發展出來以解決此種需求。

論文中提出分析一個整合於單一晶片，無須外掛其他被動元件的三角積分調變除小數頻率合成器。此頻率合成器是以 TSMC 0.18-微米互補式金氧半製程製造，可以合成 1.27 GHz 到 2.08 GHz 頻帶範圍，提供數位電視系統 135 個頻道切換。模擬結果以及量測數據將會在內文中加以討論、解釋。

本論文主要區分為五部分。第一部分介紹數位電視系統相關知識。第二部分探討鎖相迴路以及三角積分調變基本原理。我們將著重於電路設計概念以及介紹一些現有的技術。第三部分呈現頻率合成器架構和組成方塊，包含修正後的壓控振盪器、相位檢測器、電荷幫浦、迴路濾波器、可程式除頻器以及三角積分調變器均會詳細地介紹。第四部分展示模擬及量測結果。最後，針對此次結果我們作一總結。對於未來可行的改良建議事項將列於論文的最後作為結束。

Delta-Sigma Frequency Synthesizer for DTV Broadband RF Tuner

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ABSTRACT

Radio Frequency Integrated Circuits (RFIC) have been progressed rapidly in recent years. RFIC becomes attractive for applications in wireless communication due to its low cost and low power. One of the major challenges in the design of the transceiver system is the frequency synthesis of the local oscillator (LO) signal. Therefore, the frequency synthesizer is developed for this purpose.

In this thesis, a Delta-Sigma fractional-N frequency synthesizer in a single chip without any external discrete components is proposed and analyzed. The synthesizer was fabricated in TSMC 0.18μm CMOS process and can support all 135 channels of the DTV system from 1.27 GHz to 2.08 GHz. The simulation results and measurement data are discussed and explained in the content.

The thesis is mainly divided into five parts. The first section introduces the

related knowledge of the DTV system. The second section discusses the basic principle of the Phase-Locked-Loop and Delta-Sigma modulation. We focus on the important circuit design concepts and existent techniques. The third section presents the architecture and components of a frequency synthesizer. In this section, a modified voltage-controlled oscillator, a phase-frequency detector, a charge pump, a loop filter, a programmable divider, and a delta-sigma modulator are all described in details. The fourth section shows our simulations and measurement results. Finally, a conclusion to this work is given. Suggestions for future works are recommended at the ending of this thesis.

誌　　謝

本論文能夠順利完成，首先要感謝我的指導教授洪崇智博士。感謝恩師在二年碩士生涯中細心教導，不斷地指引學生正確的方向，使我對於研究學問的方法及態度有更深一層的領悟，得以更快邁向成功的一步。若沒有老師的鞭策，本論文絕對無法順利完成。另承蒙劉萬榮教授，黃淑絹教授，闕河鳴教授對本論文的諸多指導與建議，使其能夠更趨完整與正確，在這裡謝謝每一位老師。還有，感謝國家系統晶片中心提供先進的半導體製程，讓晶片的製作得以順利完成。

此外，感謝扶輪社提供高額獎學金，使我不必擔心經濟上的問題，能夠全心投入於研究之中。感謝實驗室的莊誌倫、羅天佑、張家瑋、邱俊宏、李三益、楊峻岳等諸位學長在這兩年的幫助與指導，讓我在求學路上能夠更加順利。感恩在實驗室裡和我打拼了兩年的同學，林政翰、蔡宗諺、何俊達、楊家泰，謝謝你們在研究及生活上的協助與鼓舞，使得我能夠堅持到最後一刻。還有許多學弟們，為這實驗室帶來歡笑與活力，讓我們在苦樂中研究，歡樂中成長，也衷心的謝謝你們。謝謝這一路支持我的女友，有了妳的陪伴，原本平淡無奇的生活頓時變得多采多姿，讓我緊繃的情緒適時地獲得舒緩。

最後，最要感謝的是我的母親，含辛茹苦的一手拉拔我長大，給予我舒適的環境讓我專心致力於學業上，追求自己的理想。您至高無上的愛，深植我心，千言萬語都難以表達我內心的感動，希望您永遠健康、快樂。一路走來，得之於人者太多，出之於己者太少。僅以此聊表心意，感謝所有曾經幫助過我的人。

黃琳家 于 交通大學電資大樓 710 研究室

九五年 十月

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Chapter 1

Introduction

1.1 Motivation

Television is the most important medium that educates, informs, and entertains the general public around the world. With the development of communication electronic, the demand for high-quality seeing and hearing information grows increasingly. Traditional television had been already difficult to satisfy customers, so digital television (DTV) technology was proposed to improve this problem. In recent years, DTV system has expanded maturely. Many countries such as America, Europe, Japan, have already advertised relative transmission standard and rules of application [1]. At the same time, Taiwan has also started the transition from analog to digital television.

DTV not only delivers distortion-free audio and video signals but also achieves much higher spectrum efficiency than analog television. DTV can also interface with other communication systems, digital media, and computer networks, making datacasting and multimedia interactive services possible [2][3]. In view of this, it is a key point of the ongoing digital leading toward the information society. A receiver or tuner must be needed in a digital television set to implement channel selection. Thus, it can be seen that a receiver plays an important role in our future digital broadcasting.

Frequency synthesizer is a essential function block in the receiver. It can provide a precise clock frequency to the tuner. By double conversion system, it can select the channel what we want. How to implement a frequency synthesizer by current technology will become a basilic study in the future. Based on this requirement, we use a fractional-N PLL with a second-order modulator to synthesize all frequency range that we need.

1.2 Digital television Development

1.2.1 Conventional Analog television

Traditional analog television is mainly divided into three independent transmission standards. They are NTSC (National Television System Committee), SECAM (Sequential Couleur Avec Memoire or Sequential Colour with Memory), SECAM (Sequential Colour with Memory), PAL (Phase Alternating Line). Besides Taiwan, many countries in the world has also adopted NTSC standard for a long time. This format has been in use from 1954. This technology is achieved by transmitting varying frequencies of radio waves. It uses 525 horizontal lines of picture resolution. This type of TV signal did have the flexibility to add some characteristics such as closed captioning, stereo sound, the second audio program feature, and the transmission of other data. Nevertheless, Analog television signals degrade over distance and are extremely susceptible to sources of interference. This means that some problems such as ghost images or snow may appear, even with expensive equipment and powerful transmitters.

1.2.2 Introduction to Digital television

Television is in the process of converting from analog to digital technology nowadays. Digital technology transmits in strings of 1's and 0's. Compared with analog signals, digital form is susceptible to signal loss over distance and is less probably to degrade due to interference. Therefore, digital signals are the preferred media of future transmission due to the simple fact that a 1 is still a 1 regardless of how strong the signal is or is not. In addition to these advantages, the digital signal can be compressed and store more information in less space.

The digital television standard is designed to transmit high-quality video, audio and ancillary data over a 6 MHz channel, which is the same bandwidth used for one analog NTSC channel today. The system is designed to reliably deliver about 19 Mbps (million bits per second) of data in a single terrestrial broadcast channel. DTV can carry standard definition television (SDTV) and high definition television (HDTV). HDTV encompasses six video formats, including the 1080-line interlaced (1080i) mode at either 24, 30 or 60 pictures per second, and the 720-line progressive (720p) format at the same picture rates. All these formats will have a wide-screen, 16:9, aspect ratio. This can be 2 to 3 times as many lines producing a higher picture density. The SDTV formats encompass 12 different versions of a 480-line signal-some progressive, some interlaced. The aspect ratio for the 480-line signal can be either the wide-screen, 16:9 format or the standard width, 4:3 format. SDTV has less resolution but allows the bandwidth of a DTV channel to be subdivided into multiple sub-channels. Broadcasters have the flexibility to select between offering a high definition picture and offering multiple programming options.

The technology of DTV will allow broadcasters to provide free television with CD-quality sound and movie-quality picture and manifold other enhancements.

DTV will also make the rapid delivery of large amounts of information services over your television set possible. Because DTV can free up valuable broadcast spectrum, it will be available for other information and communication services. However, it will depend on individual broadcasters to choose which services they will make available with DTV. Based on previous description, digital skills indeed afford a lot of benefits on DTV.

1.2.3 DTV in Taiwan

Today, the DTV specification development over the world mainly is divided into three segments. They are ASTC (Advanced Television Systems Committee), DVB (Digital Video Broadcasting), ISDB (Integrated Services Digital Broadcasting). Relevant comparisons between them are listed in Table I.

TABLE I Comparison between Different DTV Standards [6]

	DVB-T	ATSC	ISDB-T
Audio	MPEG1-layer2	AC-3	MPEG1-layer2
Image	MPEG-2	MPEG-2	MPEG2
Bandwidth	6/7/8 MHz	6 MHz	5.6 MHz
Modulation	COFDM	8VSB	DQPSK/QPSK/16QAM /64QAM/OFDM

DVB-T is in operation in many countries around the world, but several countries follows the U.S. in adopting ATSC instead (Canada, South Korea, and Argentina). Japan is the only country to use ISDB. Taiwan terrestrial broadcasters started broadcasting digital programs in July 2004 using the DVB-T transmission system because of its superior features on mobile or portable reception, indoor reception, the support of country-wide single-frequency networks (SFN), compatible

characteristic with DVB-C and DVB-S, and so on.

In one way or another, we must all face the simple fact that the change of TV signals from analog to digital is avoidless. Currently there are 1 million DVB-T receivers being used in Taiwan, including car STB's, in home STB's and PC or Notebook PC DVB-T receivers. The government expected that they will recall the existing analogue TV signal and change into digital broadcasting in an all-round manner, when the DTV rating is up to 85% on January 1 , 2006. In the transition years, the government will ask for stations to convert their systems to the DTV standards and will allow them to broadcast analog and digital signals simultaneously. However, broadcasters will be forced to give up the analog portion of their signals at the end of the transition period. There are also provisions established that will extend the transition period. For example, analog signal will not cease until 85% or more of a given market owns a DTV capable television. Nowadays, Taiwan has not yet made a precise decision on an analogue switch off date but continues to go forward with Digital TV.

1.3 Digital Television Broadband RF Tuner

In order to watch digital television, there must be a receiver in the TV set to implement function of downconversion. Generally speaking, there are four types of receivers, comprising Superheterodyne Receiver, Direct-Conversion Receiver, Low-IF Receiver, Double Conversion Receiver. Most of the traditional TV have adopted "Superheterodyne Receiver" structure, but it was unsuited for portable products because of its huge volume. Fig. 1.1 shows the traditional Superheterodyne tuner.

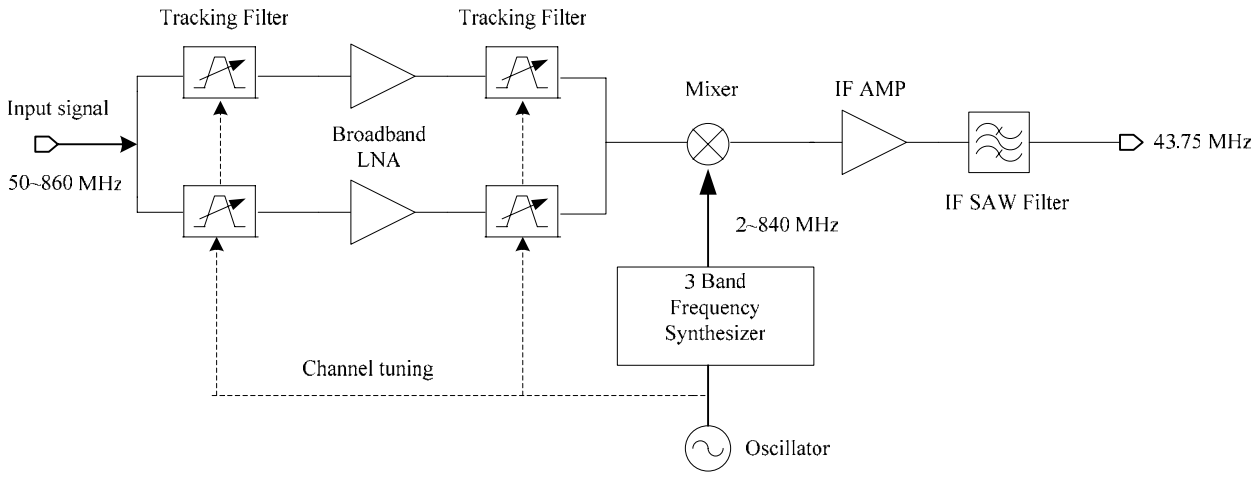


Fig. 1.1 Superheterodyne tuner

For the sake of reducing the demand for tracking filter, more and more tuners are designed by Double Conversion structure, composed of frequency synthesizers, mixers, and low noise amplifiers, as shown in Fig. 1.2. The first local oscillator (LO) is synthesized by a PLL and controlled by a microprocessor. The second LO is a fixed reference oscillator. This type of tuner converts the entire input band of 50-860MHz up to a fixed first intermediate frequency (IF), that is above the highest input frequency of interest, and selects the desired channel by the RF saw filter. This process rejects the image of the downconversion. Then, the selected channel is down converted to the second intermediate center at 43.75MHz and passes through the second IF saw filter. Finally, the output signal feeds the next stage to demodulate DTV signal. The detailed spectrum is shown in Fig. 1.3.

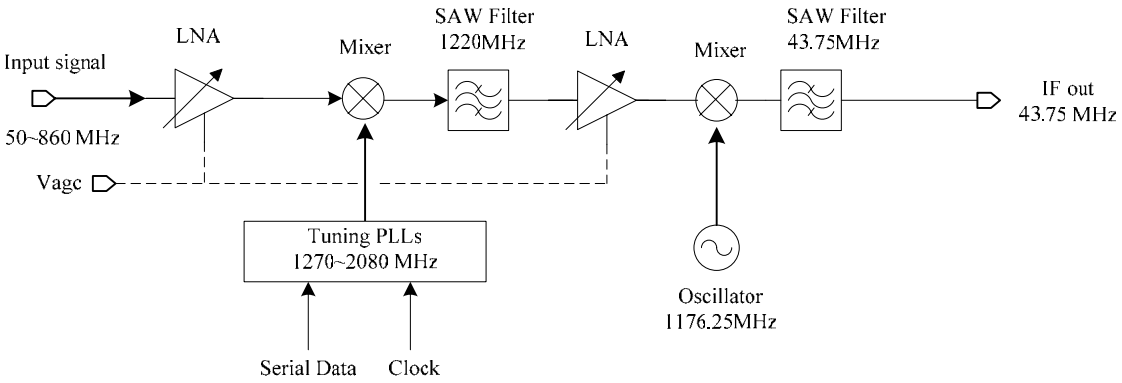


Fig. 1.2 Double-Conversion tuner

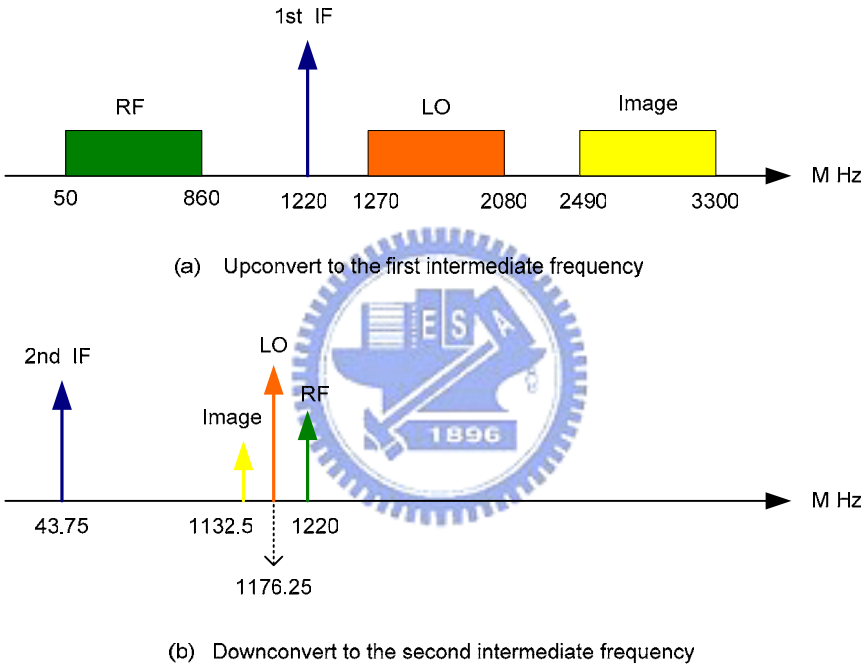


Fig. 1.3 Double-Conversion system spectrum

1.4 Thesis Overview

This thesis comprises five chapters of which this introduction is the first. Chapter 2 begins with basic ideas of phase-locked loops as well as some important characteristics in a frequency synthesizer. The most important part describes the design concepts and every building block in a PLL.

In Chapter 3, we show several techniques to implement fractional-N PLL. The most significant part is the theorems of delta-sigma modulation. We also derive its analytic function to prove the abilities of randomization and noise shaping.

In Chapter 4, a completely integrated delta-sigma frequency synthesizer fabricated in 0.18μm CMOS 1P6M process is presented. We first introduce the architecture of the synthesizer and the behavior simulation in MATLAB. Then, every building block such as the phase frequency detector, the charge pump, the loop filter, the voltage-controlled oscillator, the programmable divider, and the delta-sigma modulator, are discussed and designed.

In Chapter 5, we present the testing environment, including the instruments and components on the print circuit board (PCB). The experimental results for the ΣΔ frequency synthesizer described in Chapter 4 will be presented.

Chapter 6 gives conclusions to this work, in which a delta-sigma fractional-N frequency synthesizer is designed and verified to be feasible. Suggestions for future works are recommended at the end of this thesis.

Chapter 2

Basic theories of Phase-Locked Loop

2.1 Introduction to PLL

Phase-locked loops are used widely in the modern system such as communications, command, telemetry, radar, time and frequency control, computer, and instrumentation systems. Today, it is rare to find a piece of electronic equipment that does not employ a PLL in some form. Take communications for instance, they can recover the carrier from satellite transmission signals, recover clock from digital data signals, synthesize exact frequencies for receiver tuning, perform frequency and phase modulation and demodulation, and reduce EMI effects.

A PLL circuit can make a particular system to track with another one. More definitely, a PLL synchronizes the output signal of an oscillator with a reference signal in frequency as well as in phase. When PLL is locked, the phase error between the reference signal and the oscillator's output signal is zero or remains constant.

Some examples are described as follows [6]:

1. Carrier recovery: In all applications related to coherent telecommunications, it is necessary to reconstruct a carrier reference from a noise-corrupted version of the received signal first. Fig. 2.1 shows a received signal v_i consisting of bursts of a

sinusoid. When a burst occurs, a PLL can detect the error and then create a output signal v_o to correct the phase.

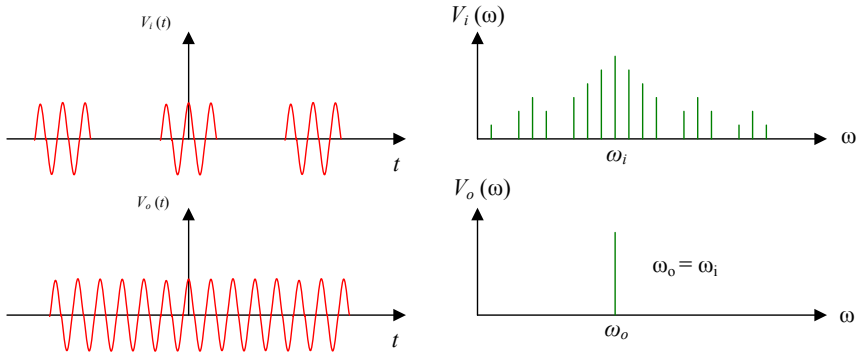


Fig. 2.1 Carrier recovery

2. Clock recovery : A clock signal is need to be synchronized to a digital data signal v_i in some application. As shown in Fig. 2.2, v_i represents the data sequence which is 1,0,1,1,0,1,1,1,0,0,1. Analyzing this data signal knows that there is a component at ω_i, where $2\pi/\omega_i$ is the spacing between logic symbols. A PLL can lock the oscillator frequency ω_o to the ω_i, producing the clock signal v_o.

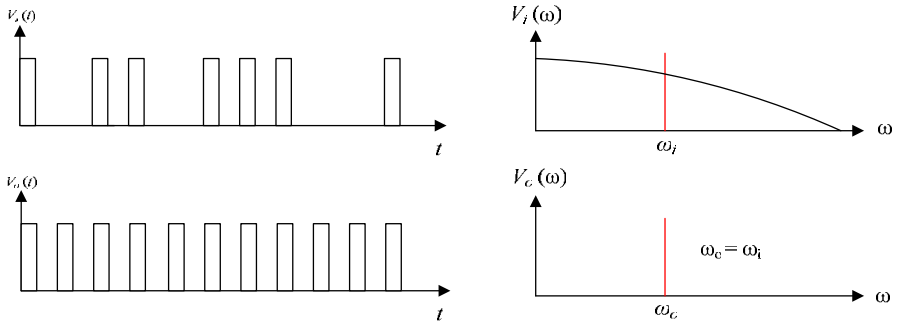


Fig. 2.2 Clock recovery

3. Frequency demodulation and Phase demodulation: Most FM receivers today adopt a PLL for frequency demodulation. If the bandwidth of the PLL is wide enough, the PLL output frequency ω_o can track the input frequency ω_i as it varies

according to the modulation. If the control voltage v_c of the voltage control oscillator (VCO) is proportional to ω_o , it is also proportional to ω_i. Consequently, v_c is the demodulated signal, as shown in Fig. 2.3. Similar concepts can be used for phase demodulation.

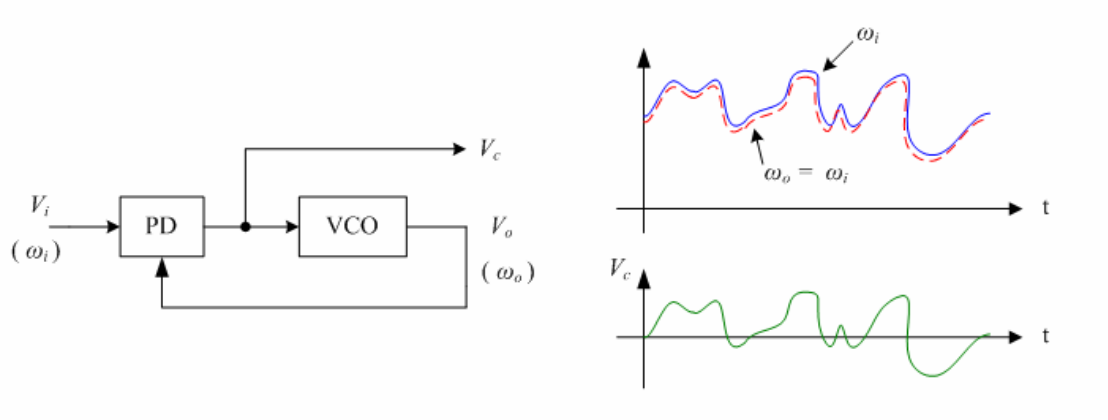


Fig. 2.3 Frequency demodulation

2.2 Architecture of Frequency Synthesizer

Frequency synthesizers play an crucial role in the field of communications. The frequency synthesizer was a system creating a set of frequencies what we need. Generally speaking, three common frequency synthesizer types can be distinguished: the direct synthesizer, the indirect or phase-locked synthesizer, and the table-look-up or digital synthesizer. Because the direct synthesizer is too bulky to integrate on a chip and the digital frequency synthesizer can not be used for high output frequencies, most synthesizers used in modern high frequency communication systems are of the phase-locked loop type.

A indirect synthesizer generates multiples of an accurate reference frequency. It is composed of five parts: a phase/frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a programmable frequency divider with a divider ratio N. The simplest form of this synthesizer is

shown in Fig. 2.4.

The operation of the PLL is as follows: the VCO output frequency (F_{out}) is divided by N. The PFD compares the divided frequency (f_{div}) with the reference frequency (F_{ref}), then it gives digital up or down signals, which is equal to the phase difference between them, to control the CP. The CP would change the digital signals to the corresponding analog voltage signals. After that, the voltage signal is low-pass filtered by the loop filter, and is used to control the frequency of VCO. When PLL is locked, the phase of the divided output signal accurately tracks the phase of the reference signal. The phase-lock process forces f_{div} and F_{ref} to be equal. Finally, we can obtain

$$F_{out} = N \cdot F_{ref} \tag{2.1}$$

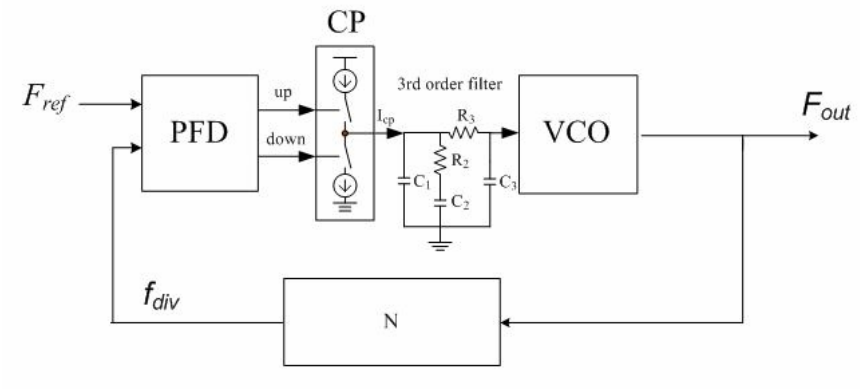
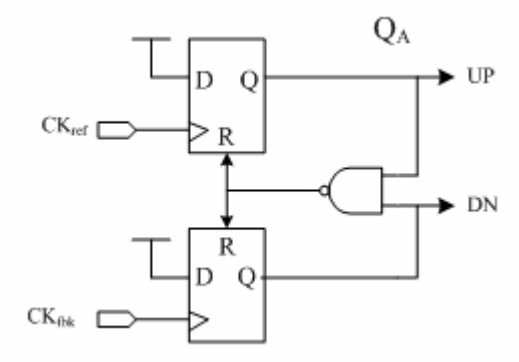


Fig. 2.4 The simplest diagram of frequency synthesizer

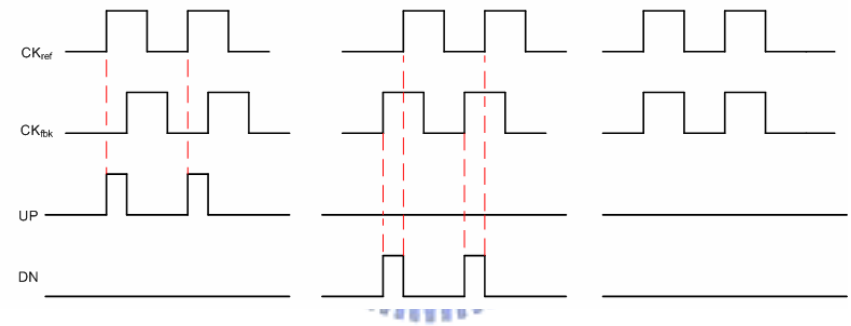
2.3 Phase / Frequency Detector

A PFD, which is usually built with a state machine with memory elements such as flip-flops, can monitor the difference between two input signals. Fig. 2.5 illustrates a common linear PFD structure using resettable DFFs and its operation diagram. If the reference signal leads the feedback signal, PFD will output an UP

signal with its pulse width proportional to the phase difference. However, if the reference signal lags the feedback signal, PFD will output a corresponding DN signal.



(a)



(b)

Fig. 2.5 (a) Linear PFD architecture (b) Operation of PFD

We could make a state diagram according to the operation of PFD, as shown in Fig. 2.6. Initially, outputs are both low. When one of the PFD inputs rises, the corresponding output becomes high. The state of the finite-state machine changes from an initial state to an Up or Down state. The state is held until the second input goes high, which in turn resets the circuit and returns the finite-state machine to the initial state. Fig. 2.7 illustrates that the characteristic of the PFD is ideally linear for the entire range of input phase differences form -2π to 2π.

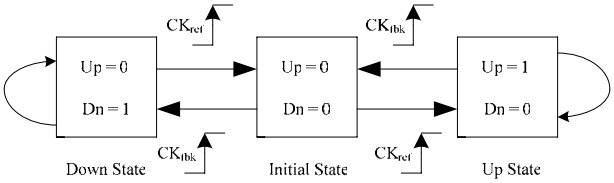


Fig. 2.6 PFD state diagram

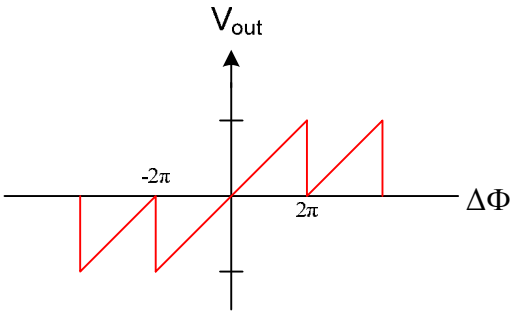


Fig. 2.7 Ideal linear characteristic

A conventional CMOS PFD is shown in Fig. 2.8. This PFD has large dead zone, which is shown in Fig. 2.9, in the phase characteristic at the equilibrium point, which generates a large jitter in locked state in PLL. Furthermore, the maximum speed is limited because of the total gate delay [7][8].

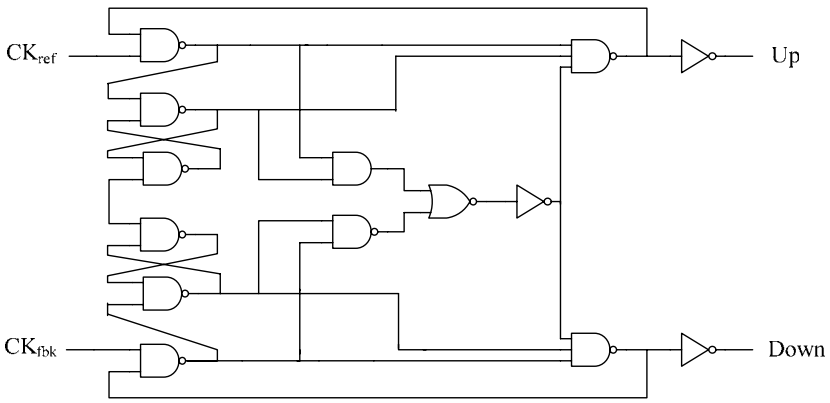


Fig. 2.8 Conventional PFD

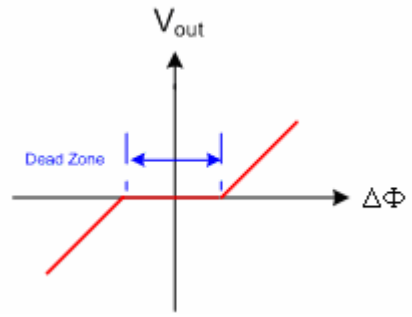


Fig. 2.9 Dead zone problem

2.4 Charge pump

The charge pump (CP) is an analog circuit controlled by the PFD outputs. It generates phase error correction current pulses to the loop filter, in order to pull the control voltage of the VCO up or down to adjust the frequency of the VCO output signal. The conventional CP is shown in Fig. 2.10. Depending on which switch is activated, the CP will either charge or discharge the load-capacitor.

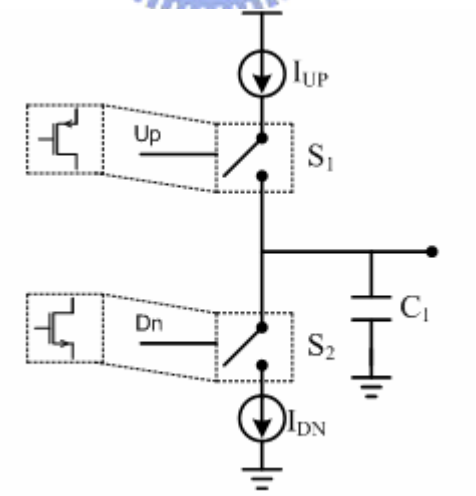


Fig. 2.10 Charge pump

Because these switches consist of MOS transistors, they suffer from several non-ideal effects, such as mismatches, charge injection, clock feedthrough, and

charge sharing, giving rise to clock-skew and reference spurs in the output of PLL. Fig. 2.11 illustrates those effects on the output voltage.

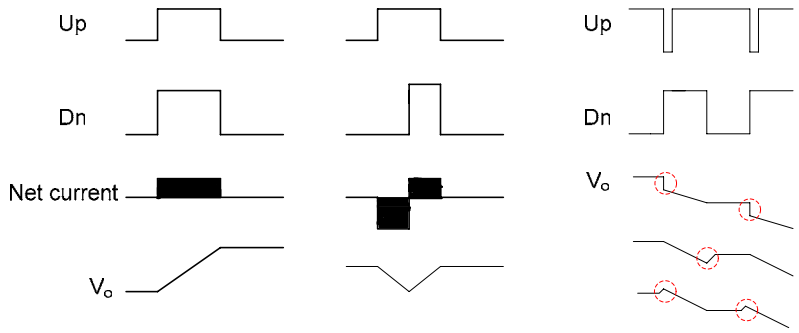


Fig. 2.11 CP non-ideal effects

Subsequently, we discuss the PFD combined with CP. If the phase error between reference signal and feedback signal is $\Delta\phi$, the charge or discharge current of the CP is I_p, the average error current in a cycle is I_e, then

$$I_e = \frac{\Delta\phi}{2\pi} I_p \tag{2.2}$$

$$K_d = \frac{I_e}{\Delta\phi} = \frac{I_p}{2\pi} \tag{2.3}$$

2.5 Voltage-Controlled Oscillator

The voltage-controlled oscillator (VCO) operates at the highest frequency and usually determines the out-of-band noise of the frequency synthesizer. Different applications usually require different specification for the VCO. These requirements are often in conflict with one another, and therefore a compromise is needed. The most important specifications of the VCO are the tuning range, the power consumption, the phase noise, the tuning linearity, and the frequency pushing/pulling. Some well-defined descriptions are as follows [11]:

- Tuning range: the VCO must be able to cover the complete required frequency band of the application, taking account of process variations.
- Tuning linearity: to simplify the design of the PLL, the VCO gain K_{vco} should be constant.
- Frequency pushing: the dependency of the center frequency on the power supply voltage (in [*MHz*/ *V*]).
- Frequency pulling: the dependency of the center frequency on the output load impedance.

The output frequency (F_{out}) of the VCO is dependent on its control voltage ($V_{control}$). The relationship between them can be written as

$$\omega_{out} = \omega_{center} + K_{vco}(V_{control}) \bullet V_{control} \tag{2.4}$$

, where $K_{vco}(V_{control})$ is the VCO gain factor in [Hz/V] and ω_{out} is the free running frequency. The relationship of phase θ_o of the VCO signal with the control voltage $V_{control}$ can be derived as

$$\theta_o(t) = \int \omega_{out}(t)\, dt \tag{2.5}$$

$$= \int (\omega_{center} + K_{vco}(V_{control}) \bullet V_{control})\, dt \tag{2.6}$$

Dropping the first term of the integral, which is not dependent on V_{tune}, results in

$$\theta_o(t) = \int K_{vco}(V_{control}) \bullet V_{control}\, dt \tag{2.7}$$

After phase and frequency lock is achieved, $V_{control}$ is nearly constant, so the dependency of K_{vco} on $V_{control}$ can be neglected. Taking the Laplace transform of (2.7) yields

$$\frac{\theta_o(s)}{V_{control}} = \frac{K_{vco}}{s} \tag{2.8}$$

We will discuss the most often used oscillator types now.

2.5.1 Crystal Oscillators

The most stable oscillator is the crystal oscillator. The symbol and equivalent circuit is shown in Fig. 2.12. From it, we can derive that a crystal has two resonance modes. At series resonance frequency ω_s, the impedance of the crystal becomes almost zero. At parallel resonance frequency ω_p, the impedance of the crystal is infinite. The corresponding resonance frequencies ω_s and ω_p are

$$\omega_s^2 = \frac{1}{L_s C_s} \qquad \omega_p^2 = \frac{1}{L_s} \bullet \left(\frac{1}{C_s} + \frac{1}{C_p} \right) \tag{2.9}$$

Since C_p is much larger than C_s, ω_s and ω_p are very close together. This is the reason why crystal oscillators achieve very low phase noise. Their low noise and good stability let them the first choice for generating the reference signal in a frequency synthesizer .

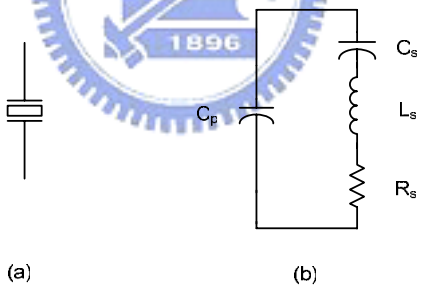


Fig. 2.12: An oscillator crystal: (a) Symbol (b) Equivalent circuit

2.5.2 Ring Oscillators

The ring oscillator is one of the most popular oscillators for clock recovery circuits and integrated PLLs because it is simple and easy to integrate. The periodic signal is generated by a ring of inverters. They can be built of three or more inverters, but the number must be odd to assure the ring to oscillate. The oscillation frequency

is $1 / 2n \cdot T_d$, where n is the number of inverters in the ring and T_d is the delay of one inverter. Fig. 2.13 shows the simplest ring oscillator. The tuning range is large. However, the phase noise is inferior,impeding its use in high-quality communication systems.

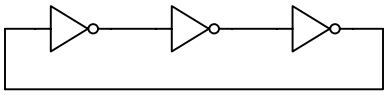


Fig. 2.13 The simplest ring oscillator

2.5.3 LC Oscillators

To improve the phase noise of the ring oscillator, the power consumption will become unacceptably high. The best way to overcome this problem is to utilize the LC oscillator. Since this structure uses high Q passive elements to be their loads, it is expected that it will have a pure spectrum. Generally speaking, the phase noise of LC oscillators is 20dB better than those of ring oscillators. Also high speed operation is achieved because of the simple working principle. Nevertheless, the biggest challenges are how to realize inductors and to reduce needed area.

2.6 Loop Filter

The loop filter provides the current-to-voltage conversion from the charge pump signal to the tuning voltage input of the VCO. The purity of the tuning voltage determines how the spectrum of the VCO output signal is. In consequence, most of the PLL's specifications will be determined by the loop filter. In the loop filter, extra poles and zeros can be introduced in the open loop transfer function, which are used to set the noise and transient performance of the PLL. The standard second-order

passive loop filter configuration is shown in Fig. 2.14. The shunt capacitor C1 is used to mitigate discrete voltage steps at the control port of the VCO because of the instantaneous changes in the CP current output.

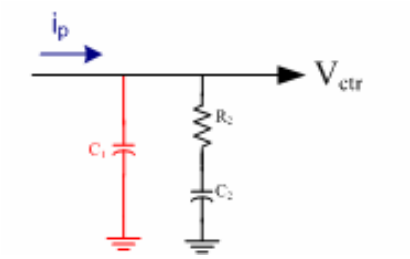


Fig. 2.14 Second order passive loop filter

Then we will discuss its design considerations by adding PFD and CP. The impedance of Fig. 2.14 is

$$Z(s) = C_1 \,//\, \left(R_2 + \frac{1}{sC_2}\right) \tag{2.10}$$

$$= \frac{C_2 R_2 (s + \frac{1}{C_2 R_2})}{(C_1 + C_2)s\left(\frac{s}{\frac{(C_1 + C_2)}{C_1 C_2 R_2}} + 1\right)} \equiv K_h \frac{s + \omega_z}{s(\frac{s}{\omega_p} + 1)} \tag{2.11}$$

$$\omega_z = \frac{1}{C_2 R_2}, \quad \omega_p = \frac{C_1 + C_2}{C_1 C_2 R_2} = \omega_z \cdot \left(1 + \frac{C_2}{C_1}\right)$$

With this transfer function, we can easily draw the Bode Plot to observe its behavior and use the open loop gain bandwidth and phase margin to determine the component. Fig. 2.15 shows its Bode plot. Typically, we locate the unity gain frequency ω_t between ω_z and ω_p to ensure loop stability.

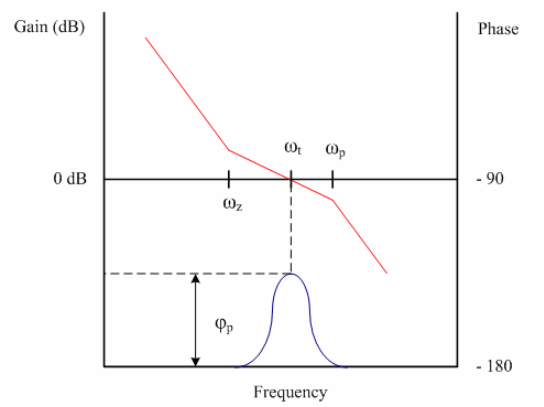


Fig. 2.15 Open loop response Bode Plot

However, additional pole is often necessary for suppressing the reference spur. For this application, we place a series resistor and a shunt capacitor prior to the VCO for more attenuation of unwanted spurs. The recommended filter configuration is shown in Fig. 2.16. The added attenuation from the low pass filter is:

$$\text{Attenuation} = 20\log\left[\left(\omega_{ref} R_3 C_3\right)^2 + 1\right] \qquad (2.12)$$

Besides, it is worthy to notice that the added pole must be lower than the reference frequency, in order to significantly attenuate the spurs, but must be at least 5 times higher than the loop bandwidth to keep system stable.

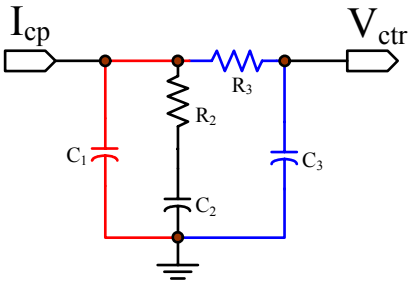


Fig. 2.16 Third order filter

2.7 Frequency Divider

Frequency dividers are used to synthesize a high frequency LO from a precise low frequency crystal oscillator. The output frequency f_{div} equals the input frequency f_{in} divided by an integer number. From this information we could derive a model for the divider in the phase domain.

The phase θ_{in} of the input signal is given by

$$\theta_{in}(t) = 2\pi f_{in} t + \theta_p \sin 2\pi f_m t \tag{2.13}$$

and the instantaneous frequency of the input signal is

$$f_{inst}(t) = \frac{1}{2\pi} \frac{d\theta_{in}(t)}{dt} = f_{in} + \theta_p f_m \cos 2\pi f_m t \tag{2.14}$$

$$f_{div} = \frac{f_{inst}}{N} = \frac{f_{in}}{N} + \frac{\theta_p f_m \cos 2\pi f_m t}{N} \tag{2.15}$$

and the phase of the output signal can now be found as

$$\begin{aligned} \theta_{div}(t) &= \int 2\pi f_{div}(t)\, dt \\ &= 2\pi \frac{f_{in}}{N} t + \frac{\theta_p}{N} \sin 2\pi f_m t = \frac{\theta_{in}(t)}{N} \end{aligned} \tag{2.16}$$

2.8 Noise Analysis of a PLL Synthesizer

Apart from channel selection and frequency accuracy, there are several other aspects of frequency synthesizers which have an influence on the performance of a transceiver, like phase noise and reference spur.

2.8.1 Phase Noise

A frequency synthesizer is expected to provide a pure spectral signal as shown in Fig. 2.17(a). There should be no unwanted frequency/phase modulation or

amplitude in the output spectrum because those undesired effect will reduce the channel selectivity and degrade the bit error rate of the receiver. However, the phase of the oscillation will fluctuate because of some noise at the frequency control input of the oscillator or the thermal noise of the resistors and transistors in the oscillator. The phase fluctuation forms “skirts” around the carrier in the frequency domain as shown in Fig. 2.17(b). So, the phase noise is developed in order to determine how the performance of a VCO is. The phase noise is characterized as the power ratio of the noise within an unit bandwidth at an offset $\Delta\omega$ with respect to ω_c to the carrier.

$$L\{\Delta f\}\ (dBc/Hz) = X(dBm) - Y(dBm) - 10\log(RBW) \qquad (2.17)$$

where Δf is the offset frequency from carrier and RBW is the resolution bandwidth of spectrum analyzer.

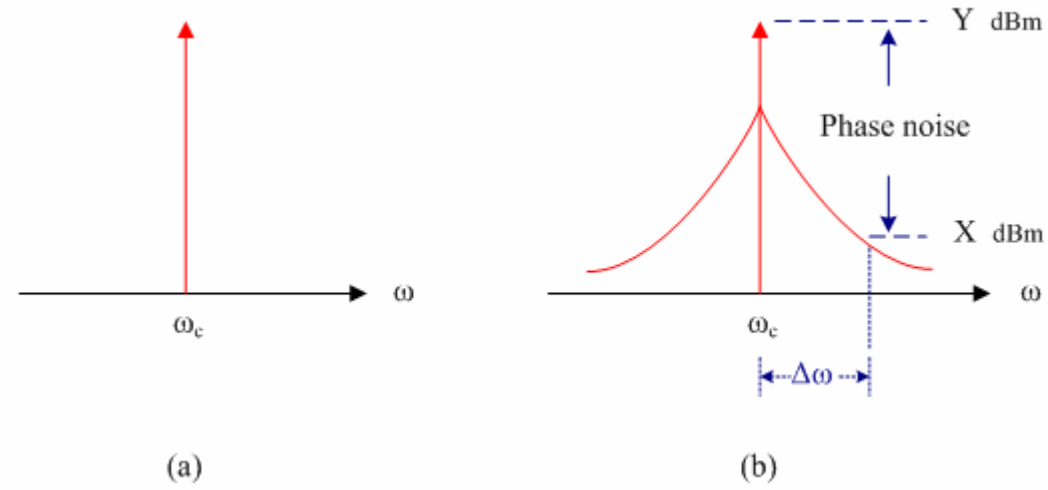


Fig. 2.17 Output spectrum of (a) Ideal (b) Actual oscillator

The phase noise has a great effect upon both the receiver and transmitter. As illustrated in the Fig. 2.18(a), if there is a large interference signal near the small desired signal and the LO exhibits phase noise, both the desired signal and the interference will be mixed down to the IF. However, both signals will suffer from

significant noise which is generated from the LO signal since the down-conversions is actually a convolution in frequency domain. If the powers of the interference signals are large, the signal-to-noise ratio (SNR) of the desired signal will be reduced. This effect is called “reciprocal mixing.” On the other hand, for the receiver, large-power transmitted signals with substantial phase noise will corrupt nearby weak signals. Therefore, the output spectrum of the LO must be extremely sharp to avoid being detected by mistake. Fig. 2.18(b) describes this appearance [13].

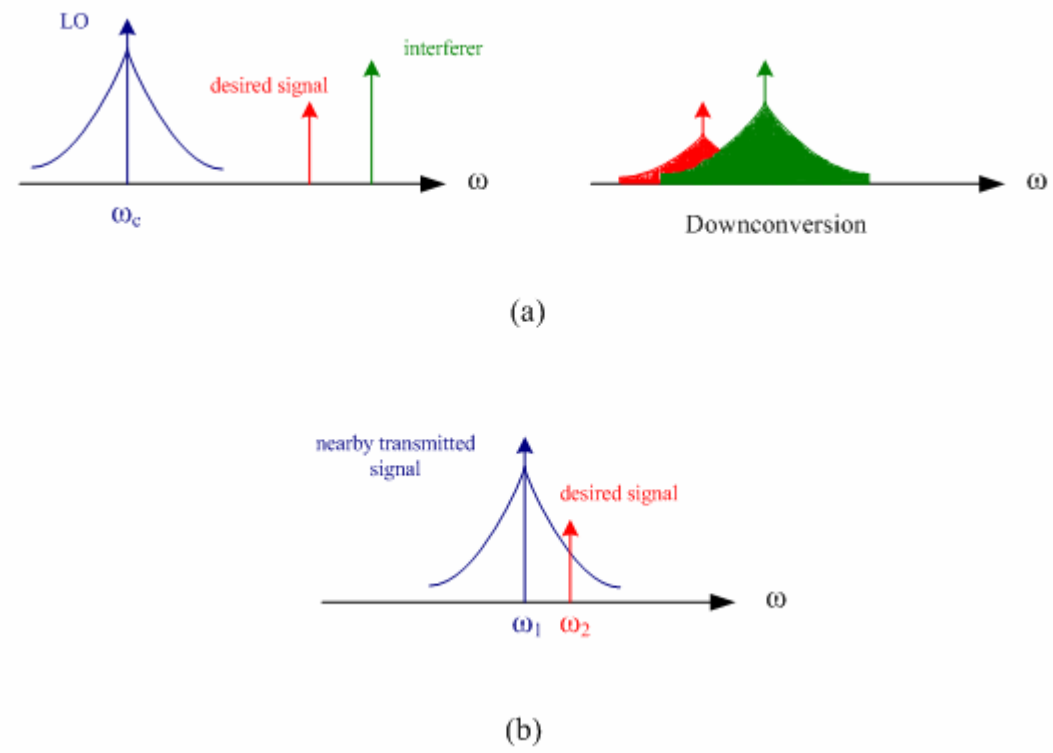


Fig. 2.18 Effect of phase noise in the (a) Receiver and (b) Transmitter

2.8.2 Spurs

In addition to phase noise, the oscillator can also be modulated by some fixed frequency noise due to the switching of other circuits in the synthesizer. Take current

switching noise in the divider and the CP at the reference rate for example, they may cause unwanted FM sidebands at the LO. Fig 2.19 illustrates this circumstance that two tones appear at the upper and lower sideband of the carrier. These tones are called “spurs”. It is similar to the case of phase noise that these spurious sidebands will also cause noise in adjacent channels and degrade the SNR of the desired signal.

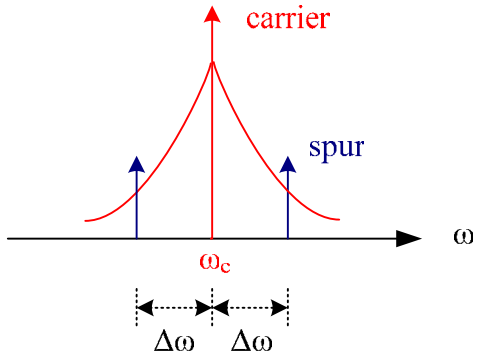


Fig. 2.19 Spurs

2.8.3 Noise Source at input

Fig. 2.20 shows the linear PLL model to analysis the input noise effect on the PLL output signal. The transfer function from $\Phi_{in}(s)$ to $\Phi_{out}(s)$ is derived as

$$H(s)=\frac{\Phi_{out}(s)}{\Phi_{in}(s)}=\frac{\frac{Ip}{2\pi}\cdot F(S)\cdot\frac{K_{vco}}{s}\cdot\frac{1}{N}}{1+\frac{Ip}{2\pi}\cdot F(S)\cdot\frac{K_{vco}}{s}\cdot\frac{1}{N}} \tag{2.18}$$

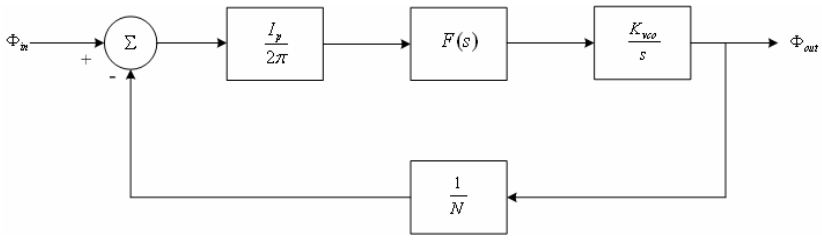


Fig. 2.20 Noise transfer function of the PLL from input to output

For simplicity, we use first-order loop filter to rewrite the above equation as

$$H(s)=\frac{\frac{sCR+1}{sC}\cdot\frac{Ip}{2\pi}\cdot\frac{K_{vco}}{s}\cdot\frac{1}{N}}{1+\frac{sCR+1}{sC}\cdot\frac{Ip}{2\pi}\cdot\frac{K_{vco}}{s}\cdot\frac{1}{N}}=N\cdot\frac{2\xi\cdot\omega_n s+\omega_n{}^2}{s^2+2\xi\cdot\omega_n s+\omega_n{}^2} \tag{2.19}$$

where $\omega_n=\sqrt{\frac{I_pK_{vco}}{2\pi NC}}$ and $\xi=\frac{R}{2}\sqrt{\frac{I_pK_{vco}C}{2\pi N}}$

Fig. 2.21 shows Bode plot of the transfer function. The input phase noise is shaped by the low-pass characteristic of the second-order PLL. For the sake of reducing the phase noise in the output signal because of the input noise, it is expected to let the PLL bandwidth as narrow as possible.

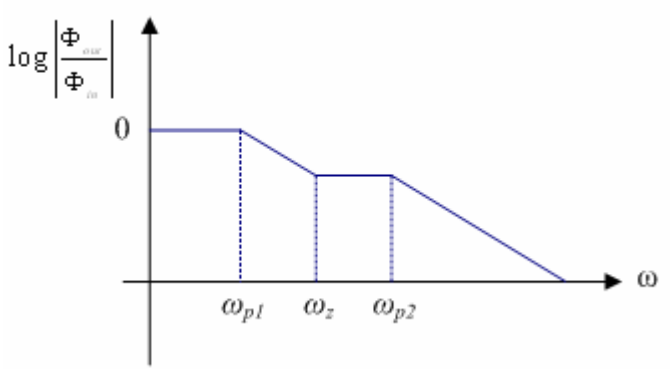


Fig. 2.21 Bode plot of the normalized transfer function

2.8.4 Noise of VCO

The phase noise of the VCO can be modeled as Fig. 2.22. Similar to Eq. 2.19, we also use the first-order filter to derive the transfer function. It can be expressed as

$$H(s)=\frac{1}{1+\frac{sCR+1}{sC}\cdot\frac{Ip}{2\pi}\cdot\frac{K_{vco}}{s}\cdot\frac{1}{N}}=\frac{s^2}{s^2+2\xi\cdot\omega_n s+\omega_n{}^2} \tag{2.20}$$

where $\omega_n=\sqrt{\frac{I_pK_{vco}}{2\pi NC}}$ and $\xi=\frac{R}{2}\sqrt{\frac{I_pK_{vco}C}{2\pi N}}$

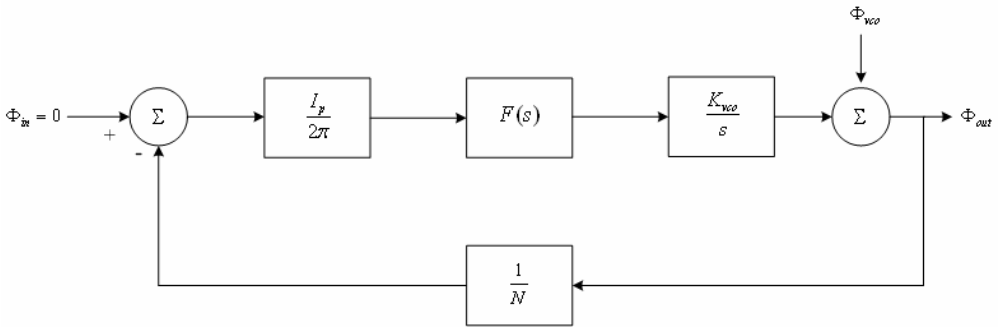


Fig. 2.22 Noise transfer function of the PLL from VCO to output

Compared with the input noise, the VCO phase noise is shaped by a high-pass characteristic by the second-order PLL. If we want to reduce the VCO phase noise, we need to make the PLL bandwidth as wide as possible. In view of this, we can know there is a tradeoff in the bandwidth position. The optimum loop bandwidth depends on the application. However, it is common to increase the loop bandwidth since the dominant source of noise is usually the VCO in fully integrated frequency synthesizer. Fig. 2.23 shows the PLL effect on the VCO output spectrum.

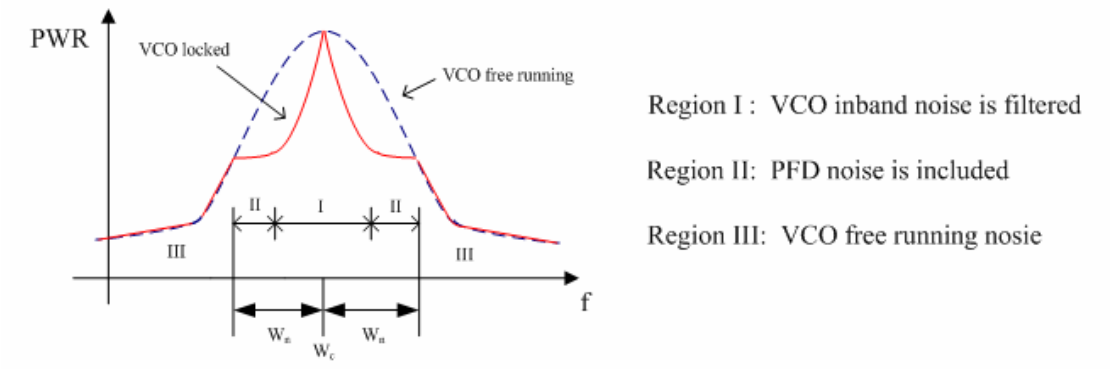


Fig. 2.23 Phase noise performance of the VCO

Chapter 3

Principles of Frequency Synthesizers

3.1 Frequency Synthesizer Types and Comparison

Frequency synthesizers can traditionally be considered to be of two main forms. One is the integer-N frequency synthesizer, and the other is the fractional-N frequency synthesizer. For the integer-N synthesizer, its output frequency is always an integer multiple of the reference frequency. On the other hand, in the fractional-N frequency synthesizer the output frequency can be a fractional ratio of the reference frequency.

The inherent limitation of an integer-N frequency synthesizer is that its frequency resolution is equal to the PLL reference frequency F_{ref}. Fine frequency resolution needs a small F_{ref} and a correspondingly small loop bandwidth. Narrow loop bandwidths are undesired due to inadequate suppression of VCO phase noise, long switching times, and susceptibility to noise. So, the fractional-N frequency synthesizer has been developed to solve this problem [13]. With the same channel spacing, the fractional-N frequency synthesizer can be designed with a higher loop bandwidth than the integer-N frequency synthesizer. Higher loop bandwidth results in faster frequency switching and thereby dynamic bandwidth techniques can be used more efficiently [14][15]. This will also relax the PLL requirements in terms of the noise reduction and the reference spur attenuation. Fractional-N frequency

synthesis solves the frequency resolution issue, but it also generates other unwanted problems.

3.2 Fractional-N architectures

When designing a fractional-N frequency synthesizer, we suffer from a trade-off between loop bandwidth, tuning bandwidth, frequency switching speed, and power consumption. There are four Fractional-N frequency synthesizer techniques: pulse swallowing, phase interpolation, Wheatly random jittering and Delta-Sigma modulation [16][17].

3.2.1 Pulse swallowing

Let us consider a pulse swallowing fractional-N synthesizer shown in Fig. 3.1. The condition of overflow in the accumulator is used to shift the divider modulus from n to n+1. For a M-bit accumulator, the average division factor N will be controlled by the accumulator input k as the following formula:

$$N = n + \frac{k}{2^M} \tag{3.1}$$

On every cycle of the divider output, k is added to the accumulator content X, so the new accumulator value would be X+k except the accumulator overflows. Then, the value assigned to accumulator is $X+k-2^M$. In the condition of overflow, a carry output is generated to switch the divider modulus.

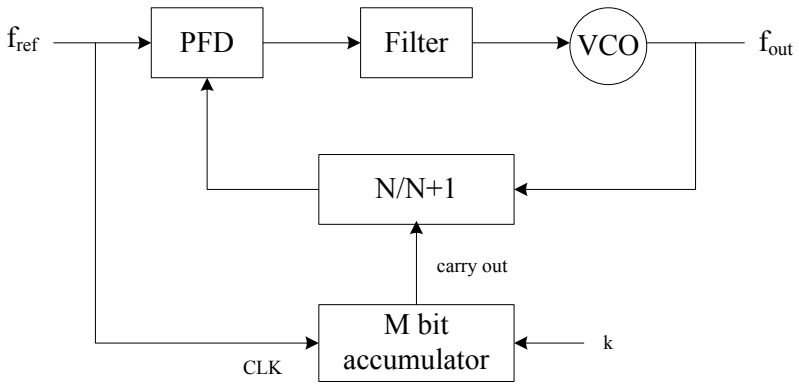


Fig. 3.1 Pulse swallowing fractional-N synthesizer

The main problem of this operation is the phase error between the instantaneous frequency and the wanted frequency, at the phase detector. Although the final phase error over the complete cycle is zero, the periodic peak will arise when the frequency division changes from N to N+1 as shown in Fig. 3.2. If the phase error is unfiltered, it may cause severe spurious signals at the output of the VCO.

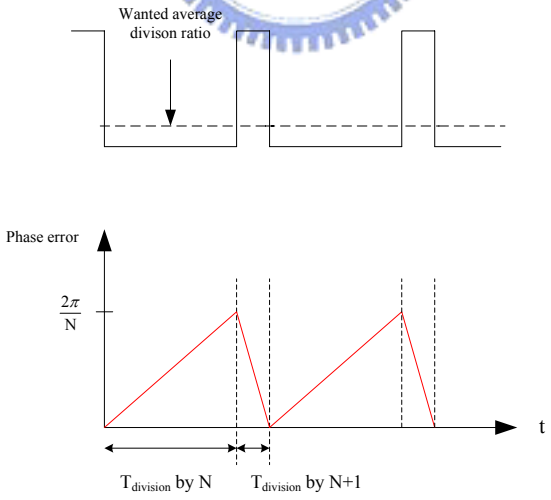


Fig. 3.2 Sawtooth phase error

3.2.2 Phase interpolating

The phase interpolation is a spur reduction skill to suppress the spurious tones as seen in the pulse swallowing approach. The technique uses amplitude compensation to the PFD output utilizing a digital to analog converter (DAC), as shown in Fig. 3.3. The accumulation of the phase of the fractional part is subtracted from the output of the PFD with that of the DAC. If the two signals exactly match, the phase error signal and output spurious are eliminated because fractional synthesis is reduced. However, the precision of the compensation directly rely on the DAC accuracy. Even if the system is well compensated during the production phase og the design, the compensation does not remain accurate as the characteristics of the analog elements are varied by temperature and aging.

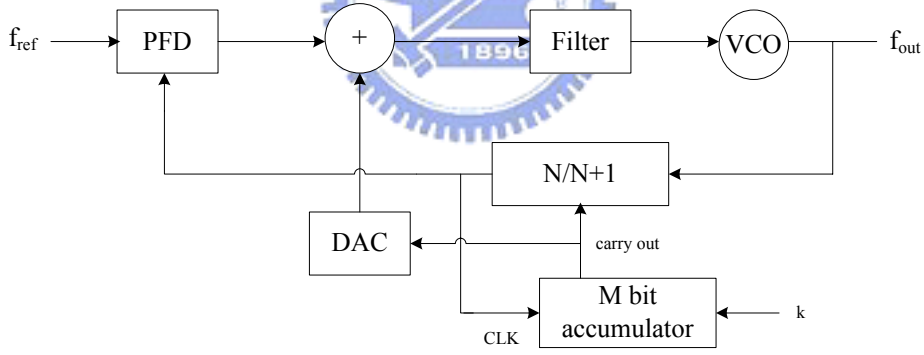


Fig. 3.3 Amplitude compensation approach

3.2.3 Random jittering

This skill employs a random sequence generator to randomize the division modulus and so converts the output spurs to jitter [18]. Fig. 3.4 illustrates this concept. The comparator output is one bit in order to control the divider module.

This technique brings a main drawback that the output spectrum displays a $1/f^2$ phase noise near the output frequency.

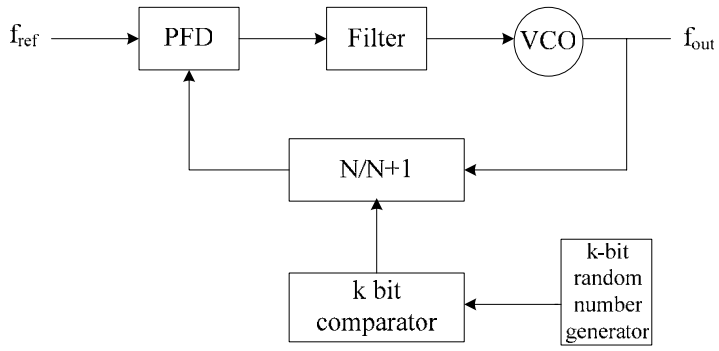


Fig. 3.4 Random jittering approach

3.2.4 Delta-Sigma modulation

Fig. 3.5 shows a Delta-sigma (ΣΔ) modulation frequency synthesizer. The divider operates as the coarse quantizer, as only integer division ratios can be realized. By switching of the division between two or more integers, the average value of the division ratio is generated at the output of the frequency synthesizer. A ΣΔ modulator has the characteristic of noise shaping, so it can shape the phase noise resulting from randomization and quantization to a higher offset frequency. In this way, the SNR and dynamic range at the relevant frequency range is improved and the shaped quantization noise can be eliminated by filtering. However, it has a large power consumption and relatively high complexity.

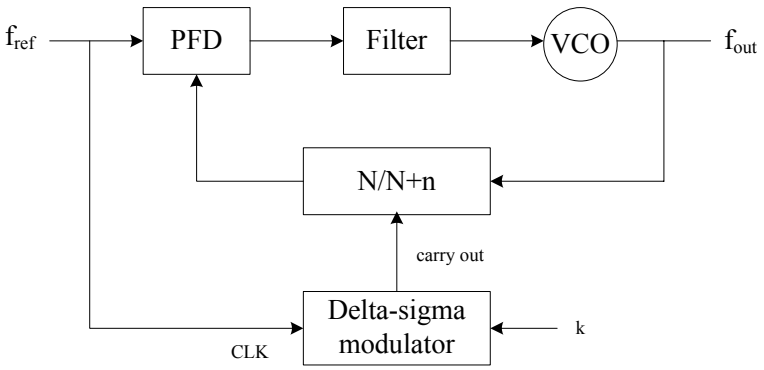


Fig. 3.5 Delta-sigma modulation frequency synthesizer

3.2.5 Performance comparison

A brief overview of different fractional-N frequency synthesizers is presented in this section. Each of these structures has advantages and disadvantages as summarized in Table II. As a result of the best performance of the ΣΔ modulation, we choose this architecture to implement our circuit.

TABLE II Total Performance comparison

Technique	Pulse swallowing	Phase interpolation	Random jittering	ΣΔ modulation
Spurious	Yes	No	No	No
Additional Components	1 accumulator	DAC	1 accumulator + generator	2 accumulator
Broad band noise	No	No	Yes	No

3.3 Delta-sigma frequency synthesis

Delta-sigma modulation technique was primarily used in over-sampling converters until Riley used the modulator noise shaping property to improve the random jitter and phase noise.

3.3.1 Fundamental concepts

Fig. 3.6(a) shows that a ΣΔ modulator consists of three components such as the integrator, the quantizer, and the differentiator. Their frequency response and power spectrum is shown in Fig. 3.6(b). In an analog to digital converter, the analog input propagates to an integrator followed by a quantizer working at a high sampling frequency compared to the Nyquist frequency. Then, the output of the quantizer is delivered to the differentiator. Fig. 3.6(c) illustrate the operation of this process, we can find that the ΣΔ modulator noise transfer characteristic is high pass in nature and results in very low in-band noise levels. So, the in-band quantization noise is alleviated and higher out-of-band quantization noise can be suppressed by the low pass loop filter.

In a fractional-N synthesizer, the input of the ΣΔ modulator is usually a digital word representing the wanted fractional value and the output of the modulator is a stream of integer numbers used to control the divider modulus. This stream forces the VCO output frequency to be fractional ratio of the reference frequency. Over time, the average if the ΣΔ modulator output converges to the desired fractional ratio.

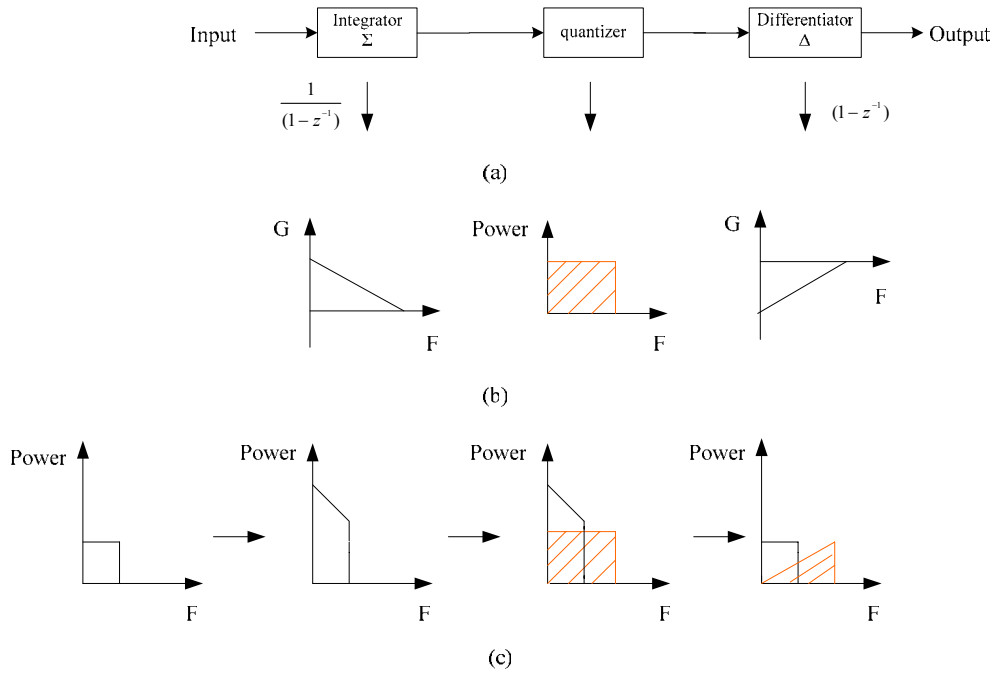


Fig. 3.6 ΣΔ modulation structure and principle

3.3.2 First-order ΣΔ modulator

The equivalent model of a first-order ΣΔ modulator is shown in Fig. 3.7.

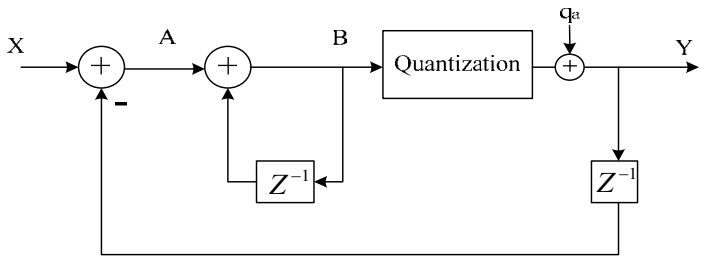


Fig. 3.7 The equivalent model of a first-order ΣΔ modulator

we can get the transfer function as follows:

$$Y = X + (1 - z^{-1})q_a \tag{3.2}$$

Now, we consider an accumulator and its equivalent block diagram, as shown in Fig. 3.8.

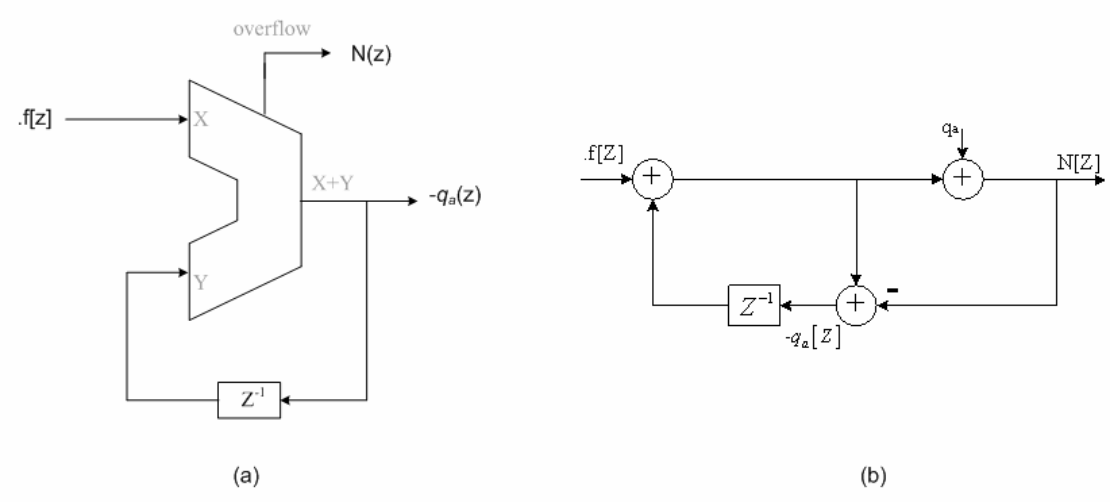


Fig. 3.8 (a) Implementation (b) block diagram of a accumulator

A transfer function of the accumulator can be derived as follows:

$$N[z] = .f[z] + (1 - z^{-1}) q_a[z] \tag{3.3}$$

From Eq. (3.3), we find the output is a delayed version of the input with shaped quantization noise. Because the input is a constant, Eq. (3.2) and Eq. (3.3) are equal. We prove that the implementation of ΣΔ modulator can be achieved by a accumulator.

In order to know the effect of noise shaping, we incorporate the ΣΔ modulator in the PLL to control the divider modulus, as shown in Fig. 3.9.

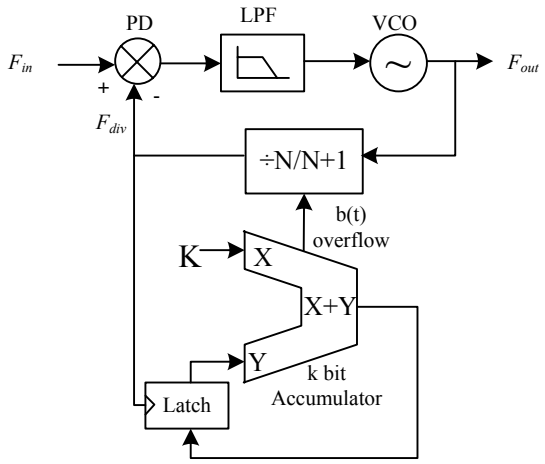


Fig. 3.9 Realization of ΣΔ modulator

A discussion of the effects of quantization noise on the overall output, F_{out} , follows. Our first step is to evaluate the phase noise in F_{div} supposing an ideal VCO at a fixed frequency. The instantaneous frequency of $F_{div}(t)$, is determined by the VCO frequency, F_{out}, and the instantaneous of division rate. The instantaneous frequency division rate in the case of Σ-Δ modulated dual-modulus divider is given by $n + b(t)$, where $b(t)$ is the bit stream alternating between 0 and 1; hence

$$F_{div}(t) = \frac{F_{out}}{n + b(t)} \tag{3.4}$$

Then, the bit stream can be broke up into the desired dc value, K/M, and an additive quantization noise [19][20]. In the time domain the quantization noise is labeled $q_e(t)$, giving

$$F_{div}(t) = \frac{F_{out}}{n + \frac{K}{2^k} + q_e(t)} \equiv \frac{F_{out}}{N_{eff} + q_e(t)} \tag{3.5}$$

The normalized instantaneous frequency departure is defined as

$$F_{diff}(t) = \frac{F_{in} - F_{div}(t)}{F_{in}} = 1 - \frac{1}{1 + \frac{q_e(t)}{N_{eff}}} \cong \frac{q_e(t)}{N_{eff}} \tag{3.6}$$

, where $\frac{1}{1+\varepsilon} \cong 1 - \varepsilon$ for small ε

Then,

$$\theta_e(t) = 2\pi \cdot \int [F_{in} - F_{div}(t)]\, dt = 2\pi \cdot F_{in} \cdot \int F_{div}(t)\, dt$$
$$= 2\pi \cdot \frac{F_{in}}{N_{eff}} \cdot \int q_e(t) \tag{3.7}$$

$$\theta_e^{'} = 2\pi \cdot \frac{F_{in} \cdot q_e(t)}{N_{eff}} \tag{3.8}$$

If the rms spectral density of the quantization noise is labeled S_{qe}(f), then the power spectral density of the normalized phase deviation will be given by

$$S_{\theta_e}(f)=\frac{1}{(2\pi f)^2}\cdot S_{\dot{\theta}_e}(f)=\left(\frac{2\pi F_{in}}{2\pi f\cdot N_{eff}}\right)^2\cdot S_{q_e}(f)$$
$$=\left(\frac{F_{in}}{f\cdot N_{eff}}\right)^2\cdot S_{q_e}(f) \tag{3.9}$$

According to Eq. (3.3)

$$q_e[z]=(1-z^{-1})q_a[z] \tag{3.10}$$

Because the quantizer in first order ΣΔ modulator is one bit,

$$q_a[z]=\frac{1}{12F_{in}} \tag{3.11}$$

The power spectral density of the quantization noise through the quantizer can be described as follows:

$$S_{q_e}(f)=|H(f)|^2\cdot S_{q_a}(f) \tag{3.12}$$

$$|H(f)|=\sqrt{\left|(1-z^{-1})\right|^2_{z=e^{\frac{j2\pi f}{F_{in}}}}}=2\sin\left(\frac{\pi f}{F_{in}}\right) \tag{3.13}$$

Combine Eq. (3.12) with Eq. (3.13), we can find its noise shaping ability

$$S_{q_e}(f)=\frac{1}{3F_{in}}\cdot\sin^2\left(\frac{\pi f}{F_{in}}\right)\ \text{rad}^2/\text{Hz},\ f\le\frac{F_{in}}{2} \tag{3.14}$$

Then from Eq. (3.9), we can get the final power spectral density of quantization noise is

$$S_{\theta_e}(f)=\frac{F_{in}}{3(N_{eff}\cdot f)^2}\cdot\sin^2\left(\frac{\pi f}{F_{in}}\right)\propto f^0 \tag{3.15}$$

However, from Eq. (3.15), we know that the noise un the output of VCO is flat, not the differential as we expected. In view of this, in order to obtain the noise shaping effectively, we must adopt the higher order ΣΔ modulator.

3.3.3 High order ΣΔ modulator

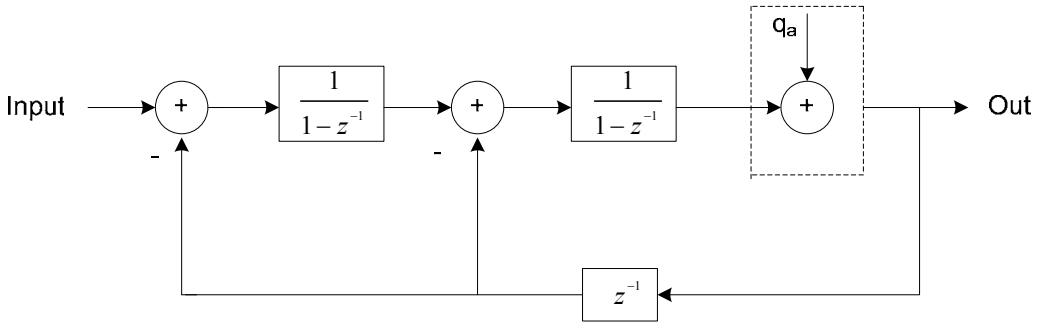
Based on the previous section, it is clear that implementing a fractional-N synthesizer with an accumulator known as a first-order ΣΔ modulator to control the divider is unwise. These shortcomings are greatly alleviated by implementing the division control with higher-order ΣΔ modulators. With this structure, the switching of the divider ratio is randomized, such that the spurious signals are no longer present in the output signal of the synthesizer. Fig. 3.10 (a) shows the second-order ΣΔ modulator and Fig. 3.10 (b) shows the third-order ΣΔ modulator. By principles of the superposition, we can easily know their outputs which the quantization noise is reduced more through noise shaping.

Second-order:

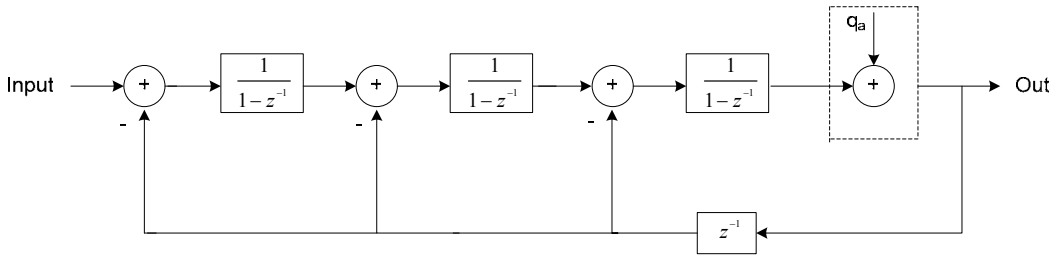
$$\text{Output} = \text{Input} + q_a(1-z^{-1})^2 \tag{3.16}$$

Third-order:

$$\text{Output} = \text{Input} + q_a(1-z^{-1})^3 \tag{3.17}$$



(a)



(b)

Fig. 3.10 Basic structures of (a) second-order modulator (b) third-order modulator

3.4 Mash implementations of ΣΔ modulator

Higher-order delta-sigma modulators improve the noise shaping characteristic, even so, they are not always stable because there are several feedback loops in the system. Fortunately, this problem was solved in the structure referred as Multistage Noise Shaping Technique (MASH) [21][22][23].

The MASH or cascade 1-1-1 ΣΔ modulator is depicted in Fig. 3.11(a). The MASH modulator consists of a cascade of first-order modulators and of a combiner stage. Fig. 3.11(b) shows the block diagram of the MASH 1-1-1. The operation of the modulator is as follows: each subsequent first-order modulator performs a quantization operation on the quantization error from the previous stages; the combiner stage, on its turn, realizes a noise shaping operation on the output signals from the first-order modulators. The math equation description is as follows:

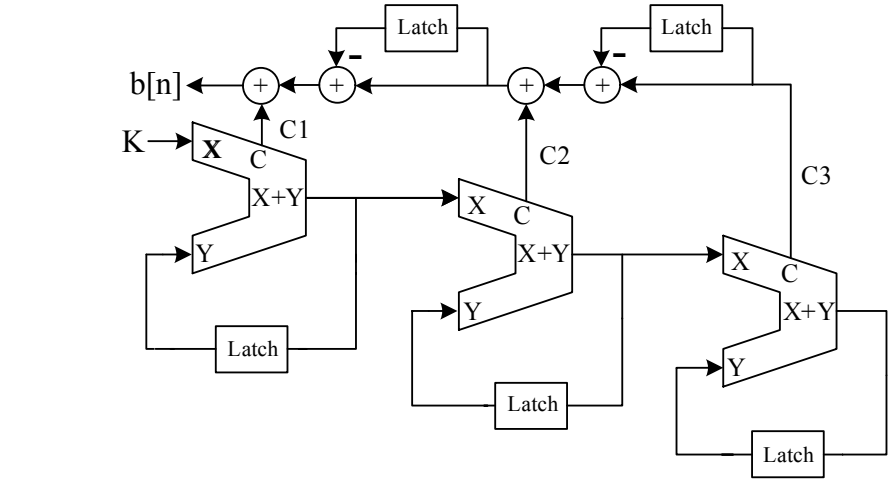
$$N_1(z) = .f(z) + (1 - z^{-1})q_{a1} \tag{3.18}$$

$$N_2(z) = -q_{a1} + (1 - z^{-1})q_{a2} \tag{3.19}$$

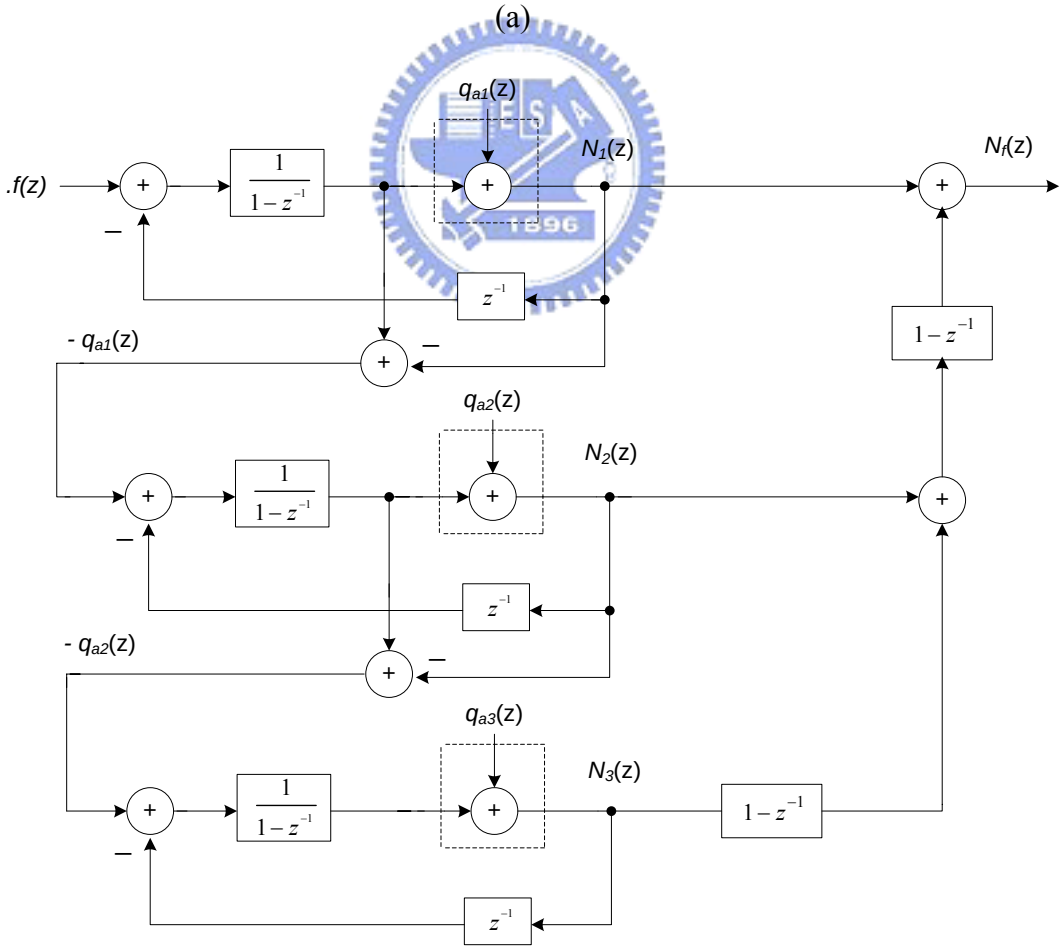
$$N_3(z) = -q_{a2} + (1 - z^{-1})q_3 \tag{3.20}$$

So, the output of third-order modulator is:

$$
\begin{aligned}
N_f(z) &= N_1(z) + (1-z^{-1})N_2(z) + (1-z^{-1})^2 N_3(z) \\
&= .f(z) + (1-z^{-1})^3 \cdot q_{a3}
\end{aligned}
\tag{3.21}
$$



(a)



(b)

Fig. 3.11 (a) Implementation and (b) block diagram of MASH 1-1-1

Similar to first-order ΣΔ modulator, we can also change the noise transfer function to H(f) = (1-z^{-1})^3 and get the final power spectral density of output noise.

$$S_{\theta_e}(f) = \frac{16 F_{in}}{3\left(N_{eff} \cdot f\right)^2} \cdot \sin^6\left(\frac{\pi f}{F_{in}}\right) \propto f^4 \qquad (3.22)$$

According to Eq. (3.22), we find that the output power spectral density is now proportional to f^4, showing that the quantization noise is suppressed in the signal band. Through the process of the derivation, we can conclude that the for ith order ΣΔ modulator the power spectral density of the phase noise is [24]

$$S_{\theta_e}(f) = \frac{F_{in}}{12\left(N_{eff} \cdot f\right)^2} \cdot \left[2\sin\left(\frac{\pi f}{F_{in}}\right)\right]^{2i} rad^2/Hz \qquad (3.23)$$

Chapter 4

Frequency Synthesizers for DTV Tuner

4.1 Introduction

Today's high-performance RF frequency synthesizer are often required: (1) to have smooth transition among channel intervals; (2) to have low phase noise and frequency variation; (3) to work over a wide frequency range which can cover the desired range; (4) to have an integrated loop filter on the chip. In the previous chapters we discussed system level design issues of a frequency synthesizer. Based on the knowledge, we will implement a ΣΔ frequency synthesizer for a DTV broadband RF tuner. This synthesizer is fabricated in a 0.18μm standard CMOS technology. Provided a 36MHz input reference signal and several bits digital codes, the circuit can generate a frequency tuning range from 1.27 to 2.08 GHz with 6 MHz channel bandwidth.

4.2 System architecture

Fig. 4.1 shows this ΣΔ frequency synthesizer. It consists of phase frequency detector (PFD), charge pump (CP), voltage controlled oscillator (VCO), loop filter (LP), programmable divider, and ΣΔ modulator. The specification of every component must be designed with extreme care. The PFD must operate correctly to

distinguish phase error and frequency error, the filter must provide an optimum compromise in output noise, switching speed, and frequency settling. In addition to these, the VCO must be of high quality and the programmable divider should work at high speed.

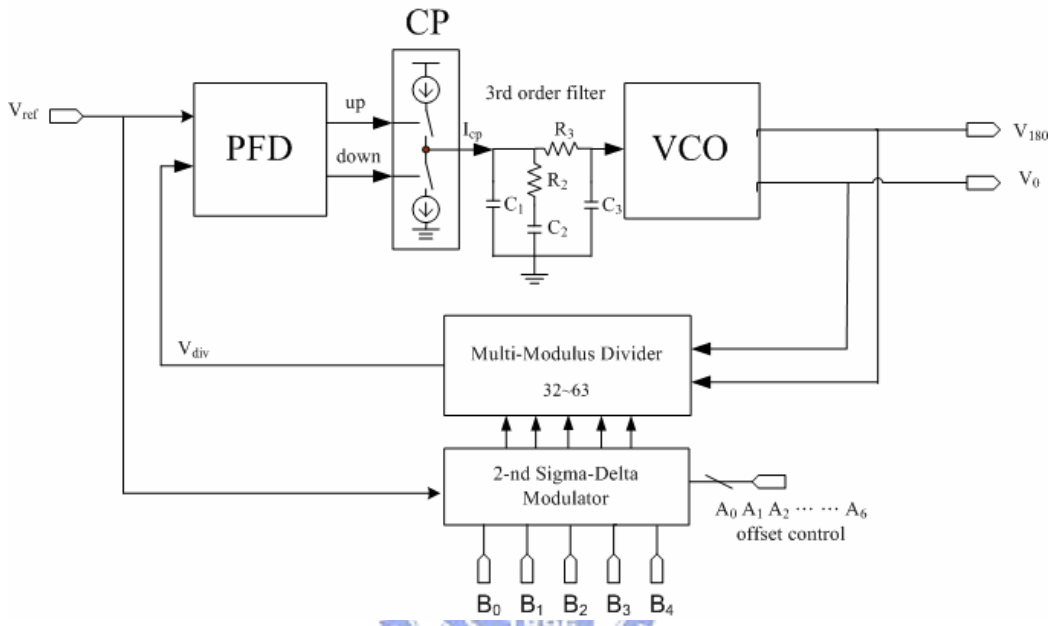


Fig. 4.1 the architecture of ΣΔ frequency synthesizer

In the Fig. 4.1, we choose the second-order ΣΔ modulator to realize modulus control. When the output of the ΣΔ modulator is -1, 0, 1, and 2, we select the modulus of the divider as N+1, N, N-1, and N-2 respectively. Thus, a fractional division ratio from $n f_{ref}$ to $(n + 1) f_{ref}$ is achieved as known in previous chapters. We use 7 bits accumulators to construct the modulator due to the minimum frequency resolution.

4.3 Behavior simulation

Due to the tremendous amount of gates counts in a frequency synthesizer, the closed-loop simulation with HSPICE will spend a lot of time. For the reason, some

simulations can be made with SIMULINK to test and verify transient response and system parameters rapidly. The behavior model of the frequency synthesizer is implemented in SIMULINK as shown in Fig. 4.2. The behavior simulation results of the system are shown in Fig. 4.3 and Fig. 4.4.

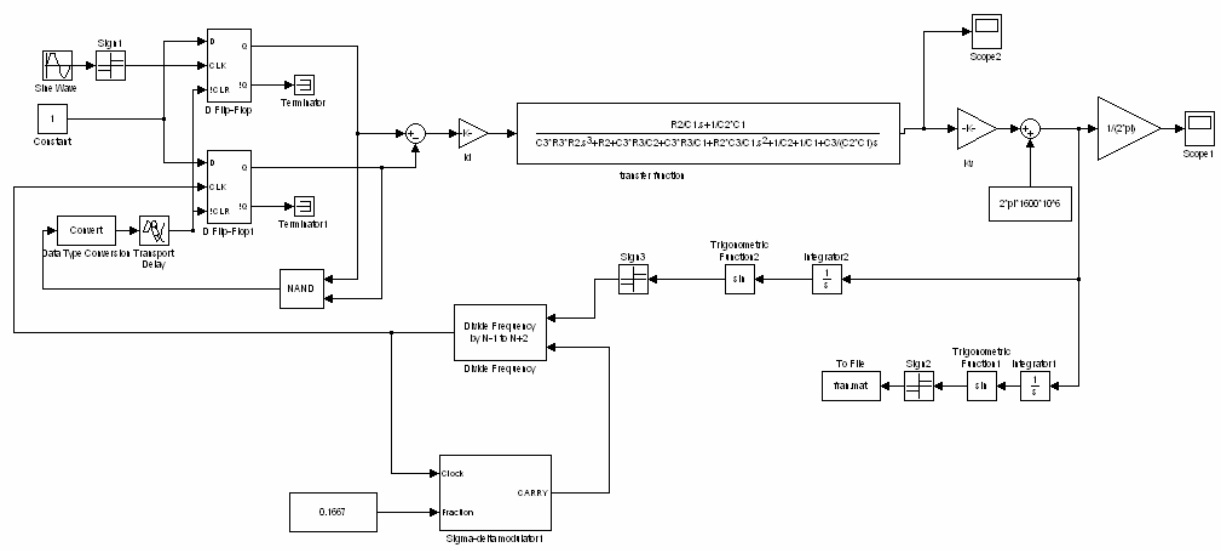
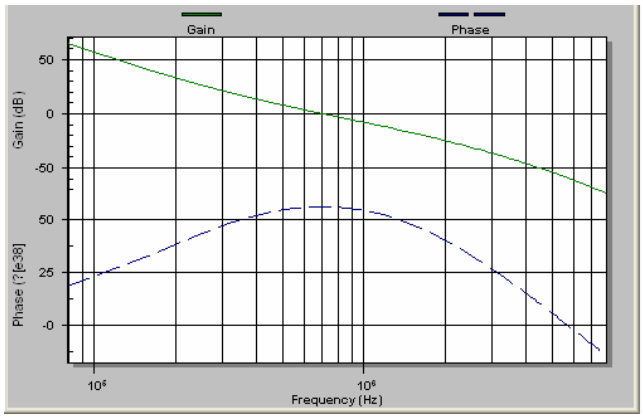
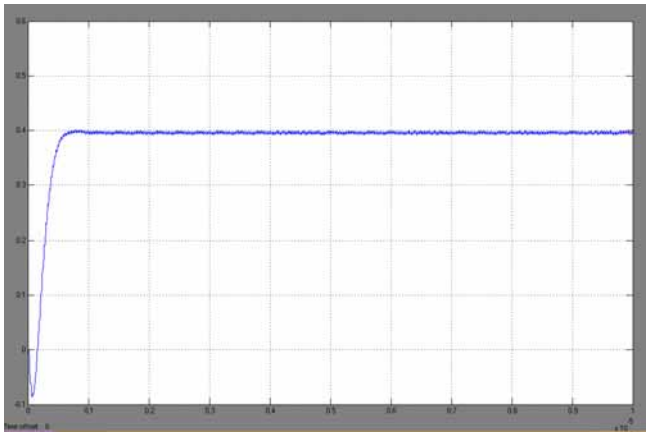


Fig. 4.2 Behavior model of the fractional-N frequency synthesizer



(a)



(b)

Fig. 4.3 Simulation results of fractional-N frequency synthesizer (a) Bode plot of open-loop response (b) transient response

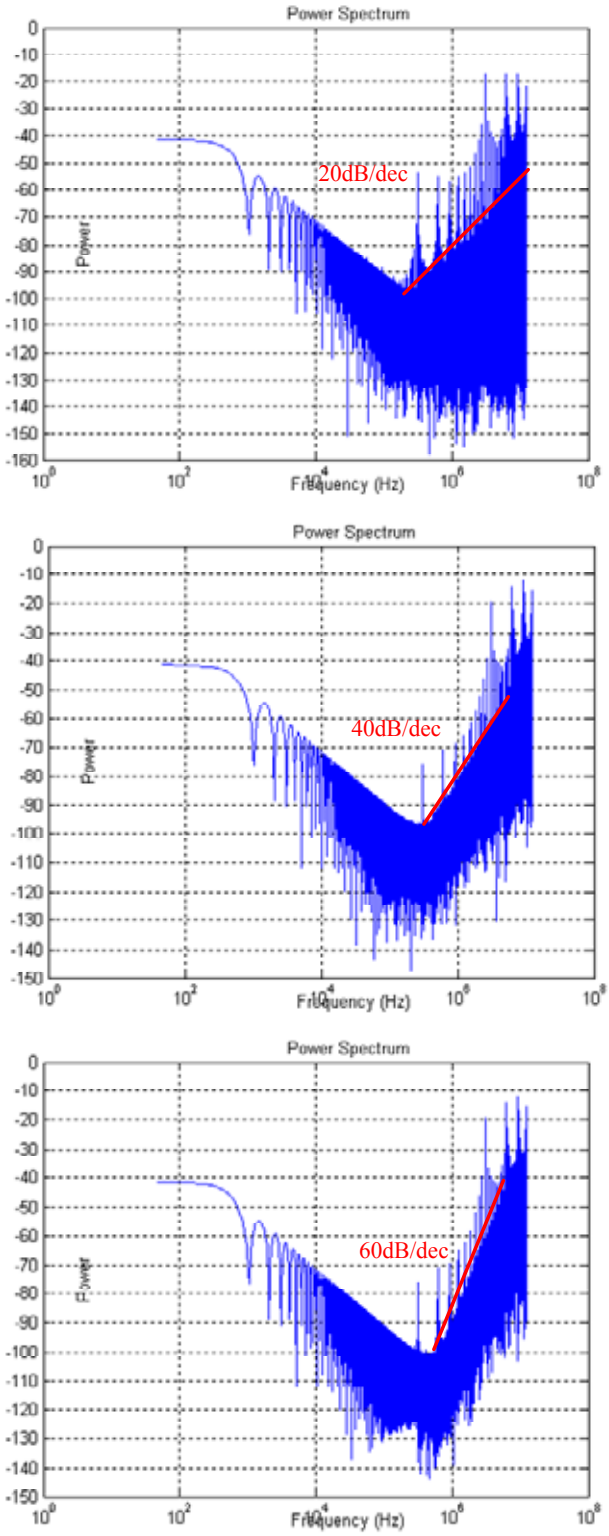


Fig. 4.4 PSD of ΣΔ modulator (a) 1st order (b) 2nd order (c) 3rd order

4.4 Circuit Implementation

4.4.1 Phase Frequency Detector

A common drawback for some phase frequency detector is a dead zone in the phase characteristic at the equilibrium point. The dead zone generates phase jitter because the control system does not change the control voltage when the phase error is within the dead zone. This influence can be improved by increasing the precision of the PFD. To reduce the dead zone and to overcome the speed limitation, we choose the dynamic phase frequency detector shown in Fig. 4.5 [25]. Compared with the conventional PFD, the transistor numbers are decreased to 12 and thus possesses smaller parasitic inherently. According to the phase difference between both input signals, UP is used to increase and DN is used to decrease the frequency of the output signal. Fig. 4.6 simulates its operation situation.

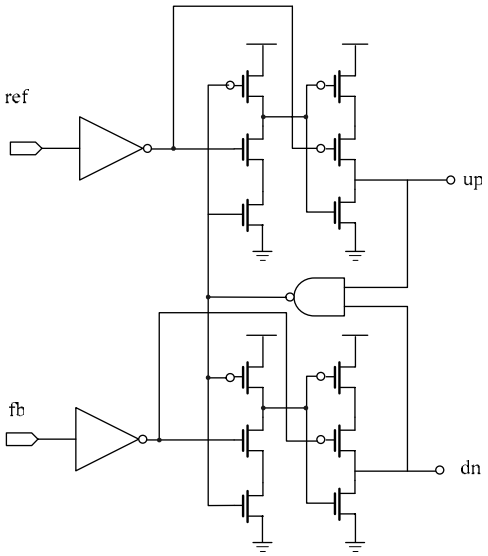


Fig. 4.5 Phase frequency detector

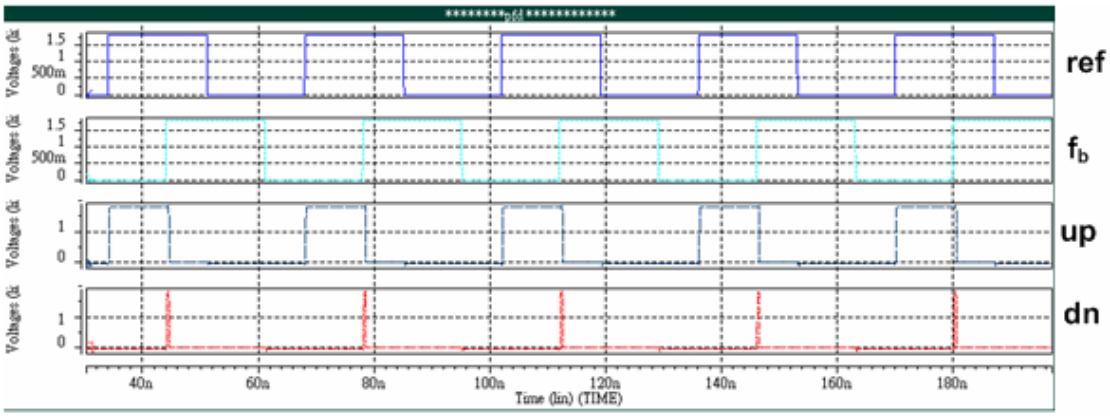


Fig. 4.6 The time diagram of the PFD

4.4.2 Charge Pump

As discussed in section 2.4, the non-ideal behavior of MOS switches such as charge injection and clockfeedthrough introduce phase noise and spurious tones in the VCO output. A lot of research has been developed to solve these problems. Among them, current steering has been usually used due to their fast switching speed and low charge injection errors. Fig. 4.7 (a) shows the basic circuit proposed in [26]. When UP is greater than $\overline{UP}$, I_B is steered on M2. The current difference between I_B and I_S is mirrored by M3 and M4, generating the charge or discharge current. On the contrary, when $\overline{UP}$ is greater than UP, I_B is steered on M1. The pull-up circuit M5 and M6 is used to increase the charge speed of the node A which is the slow path of the structure. If this pull-up circuit is not used, M1 and M3 may produces a temporal current which may modulate the VCO and then cause phase noise. However, it also has several drawbacks. The modified circuit is shown in Fig. 4.7 (b). It employs the current reuse technique to save more power than Fig. 4.7 (a) and to turn off M4 faster. Finally, by adding M7 the slow path – node B- is improved. The use of positive feedback and current reuse can obtain a faster switching speed without increasing the power consumption. The complete circuit we use is shown in

Fig. 4.8.

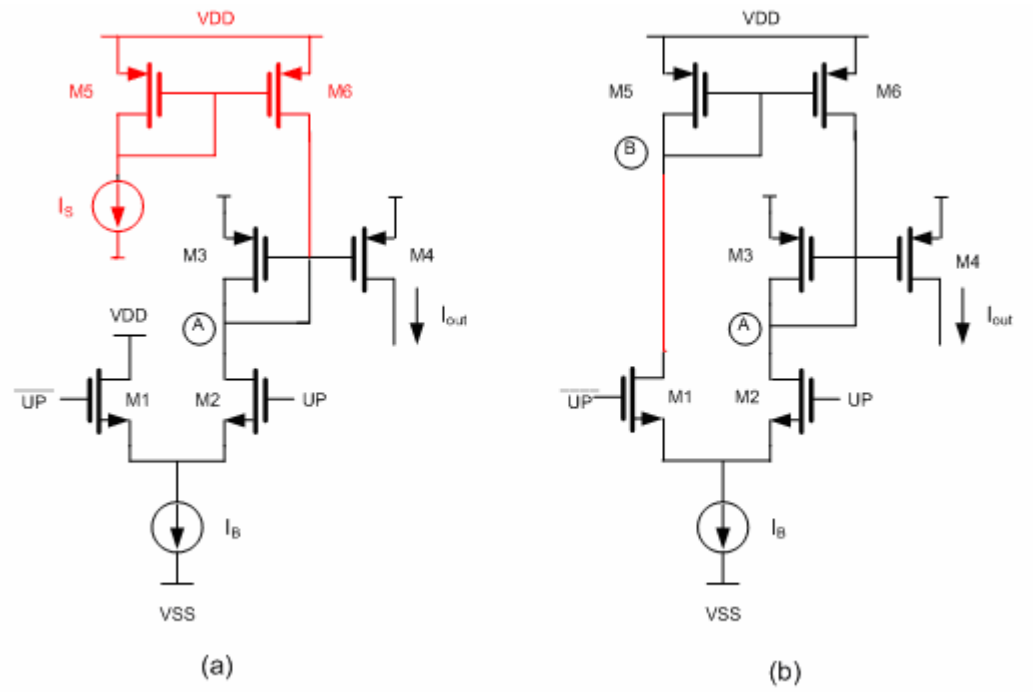


Fig. 4.7 (a) Basic charge pump (b) Modification for current reuse

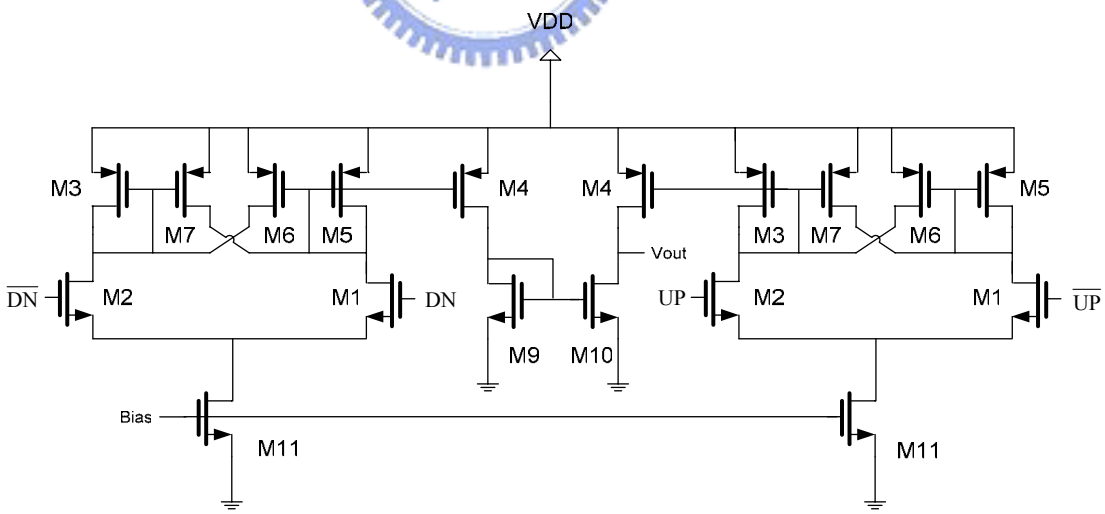


Fig. 4.8 Charge pump used in this synthesizer

Combine PFD with charge pump, some important simulations which may affect the performance of the overall system are done. Fig. 4.9 shows the charge situation

of the circuit. Fig. 4.10 shows the dead zone simulation. Even very small phase error can be distinguished, so there is no dead zone. By carefully design, we can make the range of V_{out} as large as possible in order to generate wider tuning frequency, as shown in Fig. 4.11 [27].

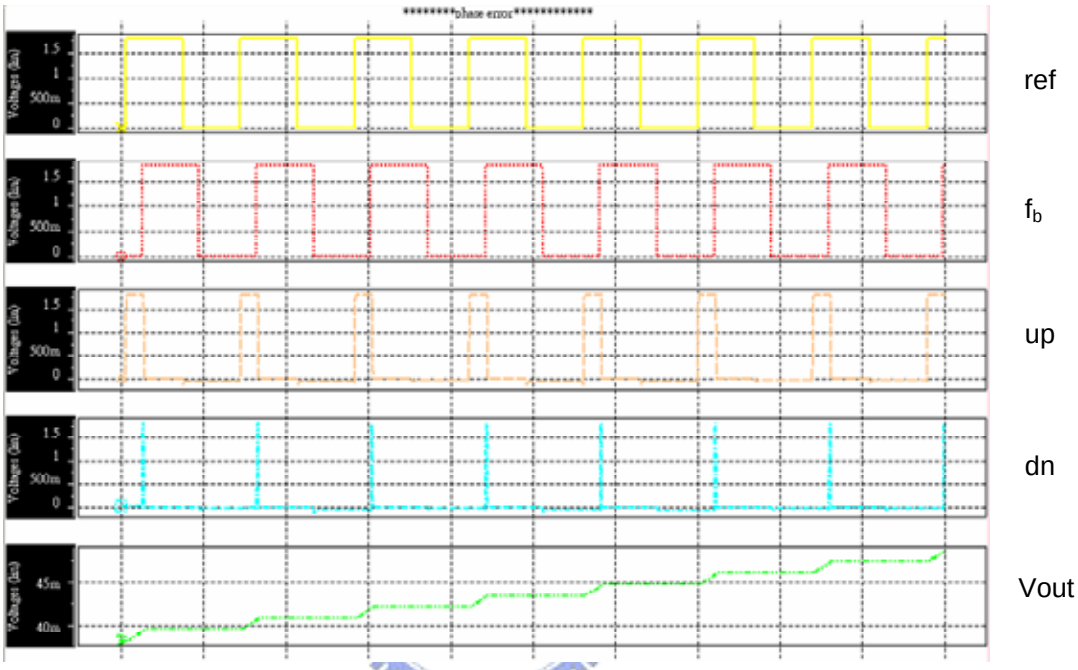


Fig. 4.9 The charge situation of the charge pump

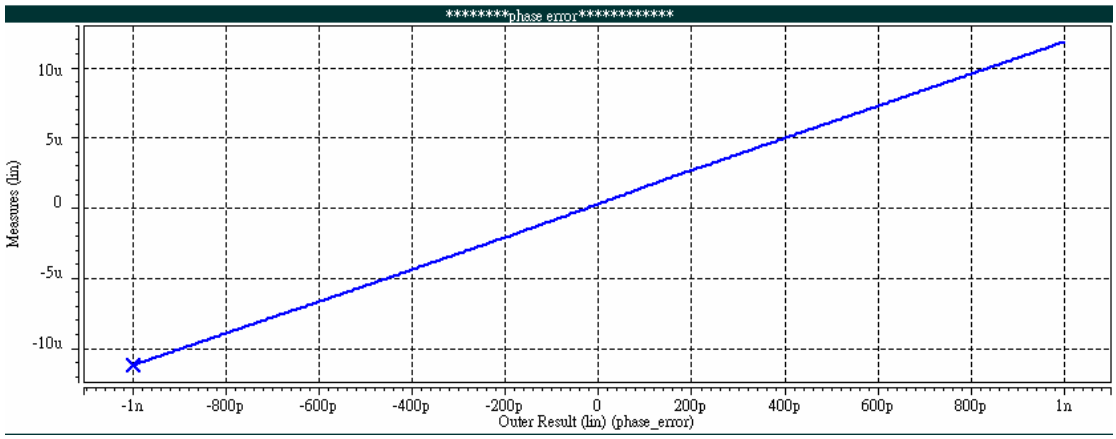


Fig. 4.10 Dead zone simulation of PFD with CP

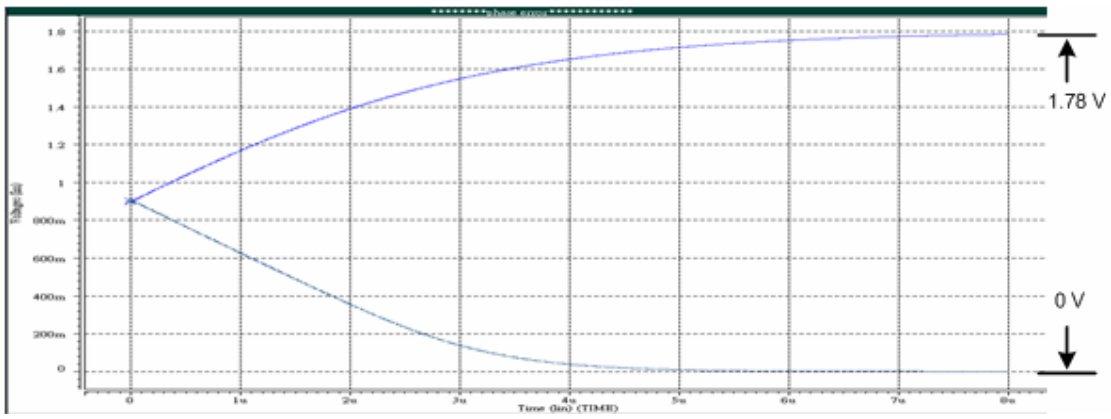


Fig. 4.11 the output voltage range of charge pump

4.4.3 Loop Filter

Loop filter design is chiefly concerned with the order of loop filter, bandwidth, and phase margin. It determines most specifications of the synthesizer and should be carefully designed. In terms of the order of loop filter, the most fundamental one is the second order filter. In the ΣΔ fractional-N PLL, however, the loop filter must equal to or higher than the order of ΣΔ modulator that ensures the extra noise from the modulator being filtered out properly. In view of this, we select the third order loop filter shown in Fig. 4.12 to implement our synthesizer. Besides, the phase margin relates to the stability of a system. Generally speaking, the phase margin is chosen from 45 degrees to 60 degrees.

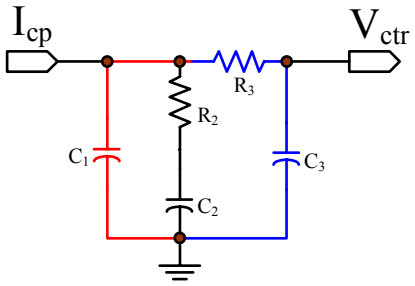


Fig. 4.12 the third order filter

After deciding the order of the loop filter, we can easily determine the parameters of each element step by step [28]. The basic design considerations are shown in Fig. 4.13.

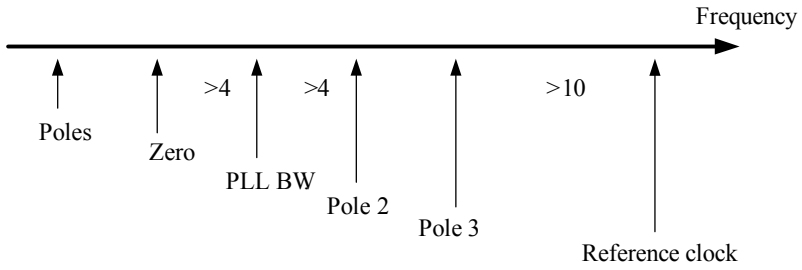


Fig. 4.13 Basic design considerations of the third order filter

1. Calculate the time constant T_1 and T_3. Then we can get the new unity-gain bandwidth ω_C because of the added third pole.

$$T_1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \tag{4.1}$$

$$T_3 = R_3 C_3 = \sqrt{\frac{10^{(ATTEN/10)} - 1}{(2\pi F_{ref})^2}} \tag{4.2}$$

$$\omega_c = \frac{\tan\phi \cdot (T_1 + T_3)}{\left[(T_1 + T_3)^2 + T_1 T_3\right]} \times \left[\sqrt{1 + \frac{(T_1 + T_3)^2 + T_1 T_3}{\left[\tan\phi \cdot (T_1 + T_3)\right]^2}} - 1\right] \tag{4.3}$$

2. Calculate the time constant T_2.

$$T_2 = 1 \Big/ \left[\omega_c^2 (T1 + T3)\right] \tag{4.4}$$

3. Thus we can derive the value of each element.

$$C_1 = \frac{T_1}{T_2} \frac{K_{pd} K_{vco}}{\omega_c^2 N} \left[\frac{(1 + \omega_c^2 T_2^2)}{(1 + \omega_c^2 T_1^2)(1 + \omega_c^2 T_3^2)}\right]^{1/2} \tag{4.5}$$

$$C_2 = C_1 \left(\frac{T_2}{T_1} - 1\right), \quad R_2 = \frac{T_2}{C_2} \tag{4.6}$$

4. As rule of thumb chooses $C_3 \le C_1/10$, otherwise T_3 will interact with the primary poles of the filter.

$$C_3 = C_1/10, \quad R_3 = T_3/C_3 \tag{4.7}$$

By following these steps, the calculated values of the elements which are all on-chip and some important parameters are listed in the following Table. The Bode diagram of the PLL is shown in Fig. 4.14.

Design parameters

Parameter	Value
F_{ref}	36 MHz
PLL BW	900 kHz
K_{vco}	866 MHz / V
I_p	0.06 mA
C_1	7.245 pF
R_2	8.05 kΩ
C_2	91.88 pF
R_3	18.3 kΩ
C_3	724.53 fF

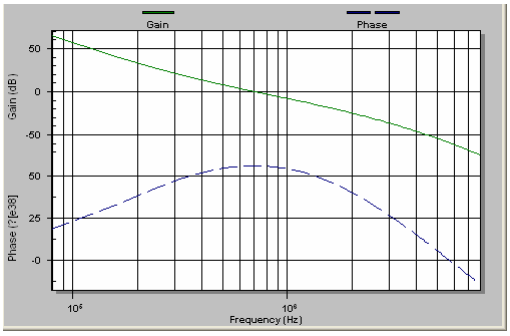


Fig. 4.14 Bode diagram simulation of the PLL

4.4.4 Voltage-Controlled Oscillator

A CMOS VCO can be built using ring structures or LC tanks. The LC design has the best noise and frequency performance because of the large quality factor Q achievable with resonant networks [29]. However, the limited tuning range and large area have become serious drawbacks in LC VCOs. On the other hand, ring VCOs have several attractive characteristics such as the ease of integration with standard CMOS process, the small chip area, and the wide frequency tuning range. Furthermore, they can be used to generate both in-phase and quadrature-phase outputs with an even number of delay cells [30]. Therefore, taking System On Chip (SOC) and other advantages into consideration, we choose the ring oscillator to realize our VCO.

Several techniques have been devised to reduce the smallest achievable delay per stage because of the frequency limitations of a single-loop ring oscillator [31][32][33]. One of them is dual-delay paths method, as shown in Fig.4.15. The key point of the concept is that adding another feedforward loop to make the delay time smaller than that of the single-loop oscillator. The bold lines seen in Fig. 4.15 represent the primary loop and the dotted lines represent the auxiliary loop [34][35].

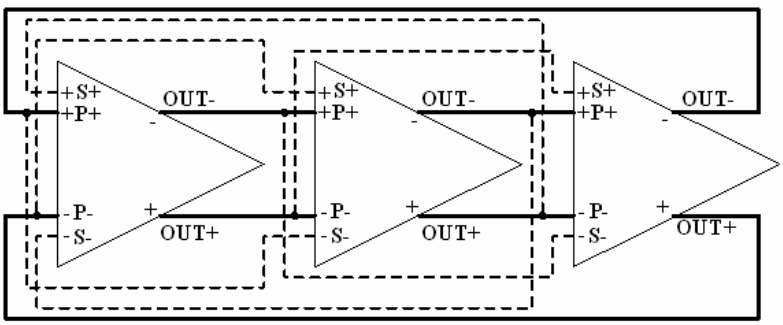


Fig. 4.15 Block diagram of ring oscillator with dual-delay paths

The design of delay cell is depicted in Fig. 4.16. M1 and M2 are the input pair of the primary loop, while M5 and M6 form the input pair of the second loop. M3 and M4 serve as variable resistances which are controlled by tuning the gate voltage of them in order to change the operating frequency. The cross-coupled NMOS, M7 and M8, can boost the operating frequency and reduce the transition time of the output signal. In the end, M9 and M10 are added as the load to prevent the oscillator from failing to oscillator when the control voltage approaches 1.8V [36]. Fig. 4.17 shows the simulation for the frequency-voltage characteristic of the three stage ring oscillator.

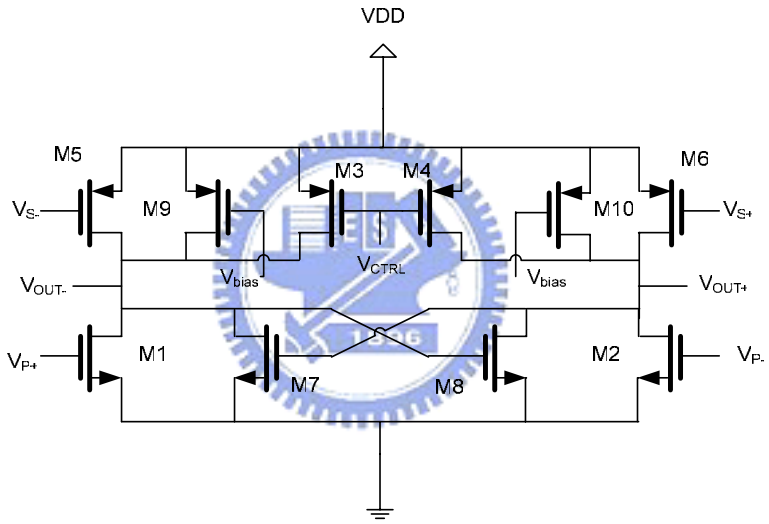


Fig. 4.16 Original delay cell of the ring oscillator

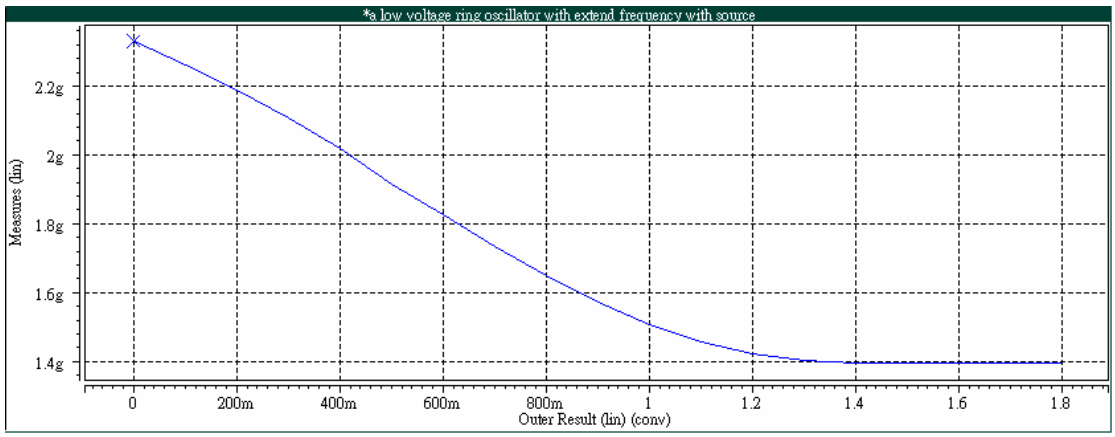


Fig. 4.17 Tuning characteristic of the original ring oscillator

According to Fig. 4.17, we find that the output frequency of the VCO changes barely when the control voltage is above 1.2V. This is because that at this time M3 and M4 tend to turn off, only leaving load resistance M9 and M10 biased at a constant voltage. In view of this, we propose a improved circuit minutely working when the control voltage is above 1.2V, as shown in Fig. 4.18. In the Fig. 4.18, by adding M11 and M12 the control voltage will be level shift and is used to bias the gate voltage of M9 and M10. At this time, the operation of M9 and M10 are so like variable resistances that they will also affect the output frequency of the VCO. Consequently, the ideal is obviously known that M3 and M4 dominate the output frequency with the control voltage from 0V to 1.2V , on the contrary, M9 and M10 dominate the output frequency with the control voltage from 1.2V to 1.8V. So, the VCO can work normally with the control voltage from 0V to 1.8V. With careful design, we can find the frequency tuning range of the VCO is extended and has good linearity over the control voltage being 0V~1.8V. The VCO provides a frequency tuning range from 770 MHz to 2330 MHz and fits in with the desired output frequency. Take measurements into account, we use the open drain structure as the output buffer due to its high driving ability, as shown in Fig. 4.19. Fig. 4.20 shows the frequency-voltage characteristic of our VCO. Fig. 4.21 shows its phase noise performance. Fig. 4.22 shows the out swing is approach 190mV considering the PAD effect.

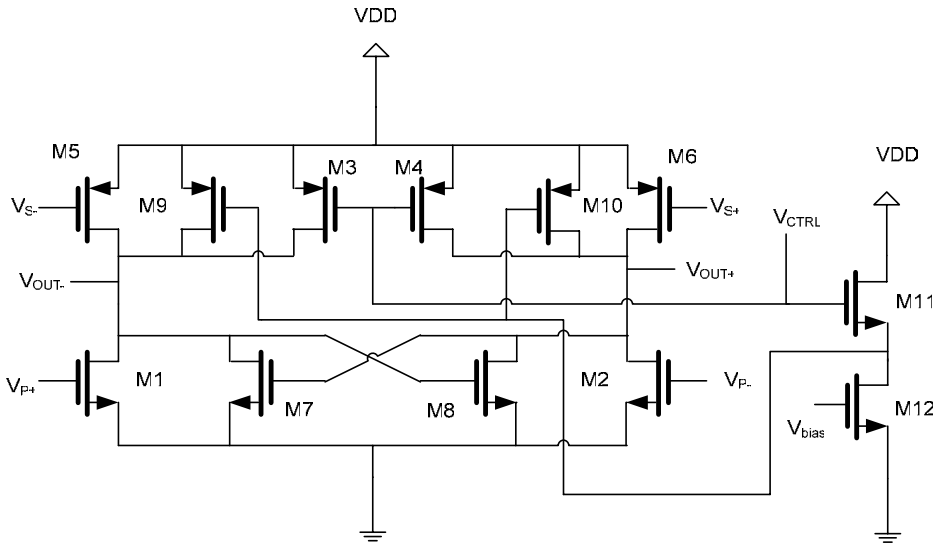


Fig. 4.18 The proposed delay cell

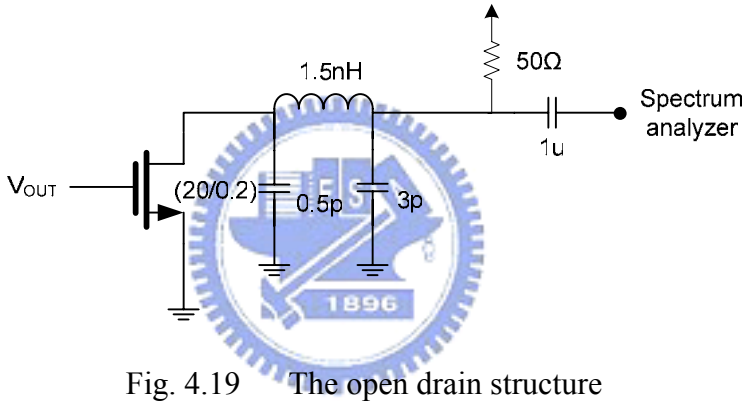


Fig. 4.19 The open drain structure

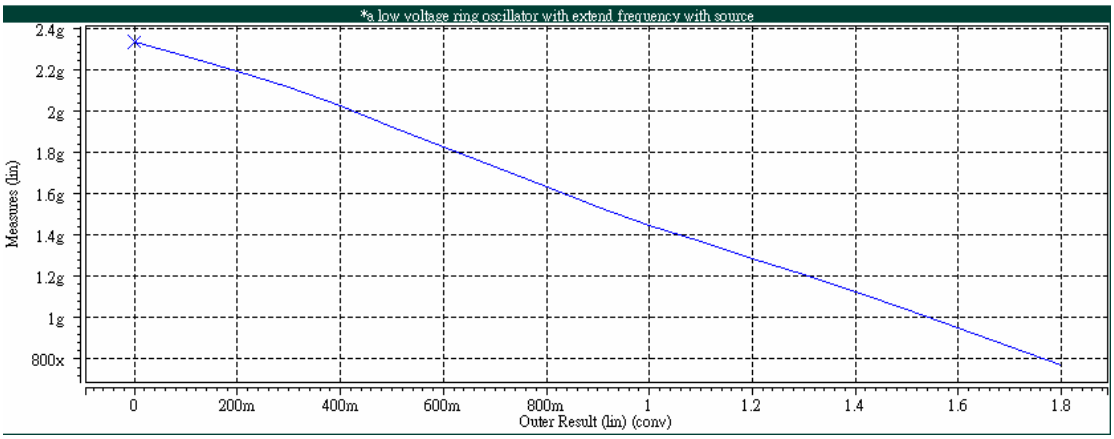


Fig. 4.20 Tuning characteristic of the proposed ring oscillator

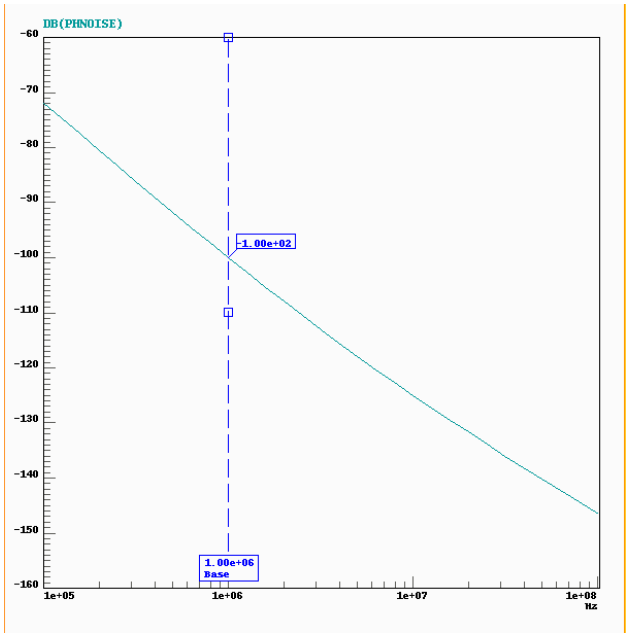


Fig. 4.21 Phase noise of the VCO

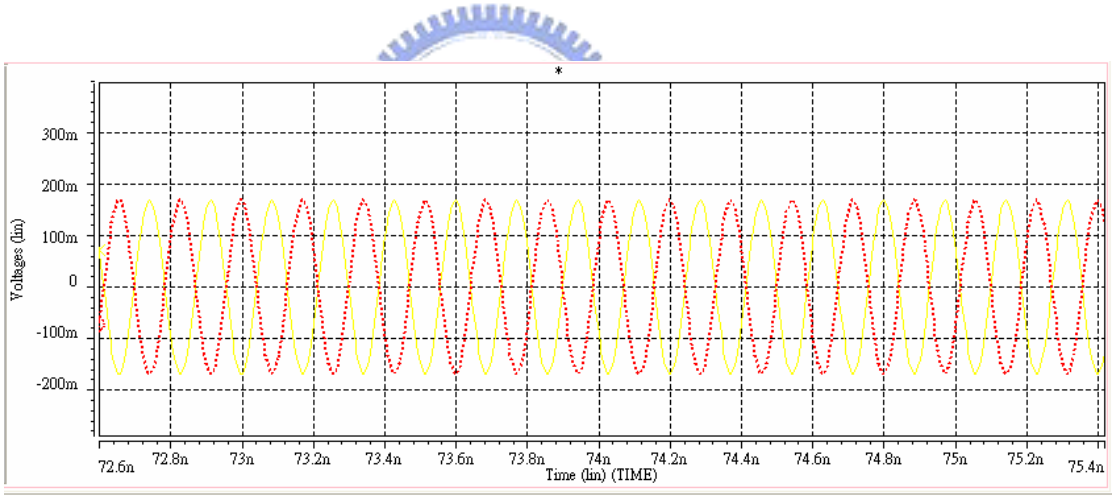


Fig. 4.22 The output swing with the PAD effect

Finally, we simulate the VCO tuning range in the different corner conditions shown in Fig. 4.23 and summarize the results in the Table III. According to Table III, results illustrate that the VCO with the different corner conditions can all cover the wanted frequency range.

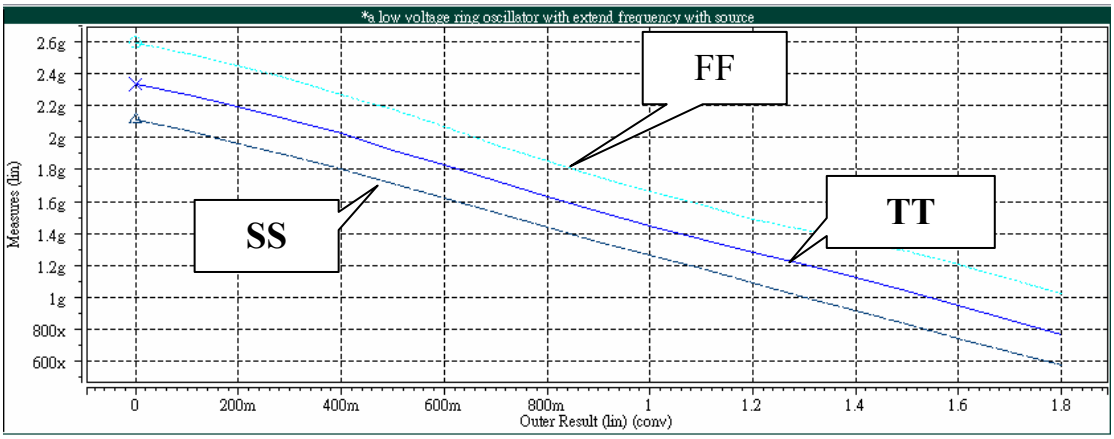


Fig. 4.23 Tuning range of the VCO with corner model variation

TABLE III Process corners simulation

Process Corners	TT	FF	FS	SS	SF
Frequency(MHz)	770~2330	1020~2590	817~2340	576~2110	742~2340

4.4.5 Programmable Frequency Divider

Programmable dividers have to operate at the highest VCO frequency. Therefore, the choice of the divider architecture is essential for achieving low power dissipation and high design flexibility. Fig. 4.24 depicts the programmable frequency divider. These feedback lines enable simple optimization of power dissipation. Another advantage is that the topology of the different cells in the divider is the same, therefore facilitating layout work.

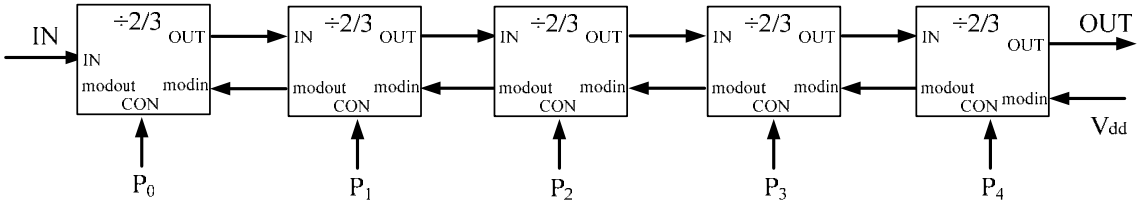


Fig. 4.24 The architecture of programmable frequency divider

The programmable divider can provide an output signal with a period of

$$T_{out} = \left(2^5 + p_4 \cdot 2^4 + p_3 \cdot 2^3 + p_2 \cdot 2^2 + p_1 \cdot 2^1 + p_0\right) \times T_{in} \qquad (4.8)$$

Therefore, this equation shows that the division ratios from 32 (if all p_n=0) to 63 (if all p_n=1) is achieved. The circuit of the 2/3 divider is shown in Fig. 4.25. The logic functions of the 2/3 cells are implemented with the Source Coupled Logic (SCL) structure presented in Fig. 4.26. The logic tree combines a latch function with an AND gate [37]. Fig. 4.27 shows the simulation of divide-by-62 frequency divider.

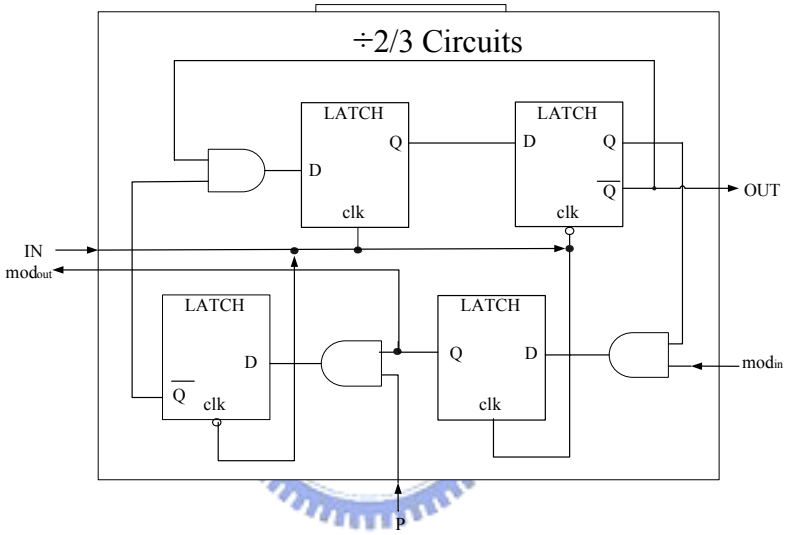


Fig. 4.25 Functional blocks and logic implementation of a 2/3 divider cell

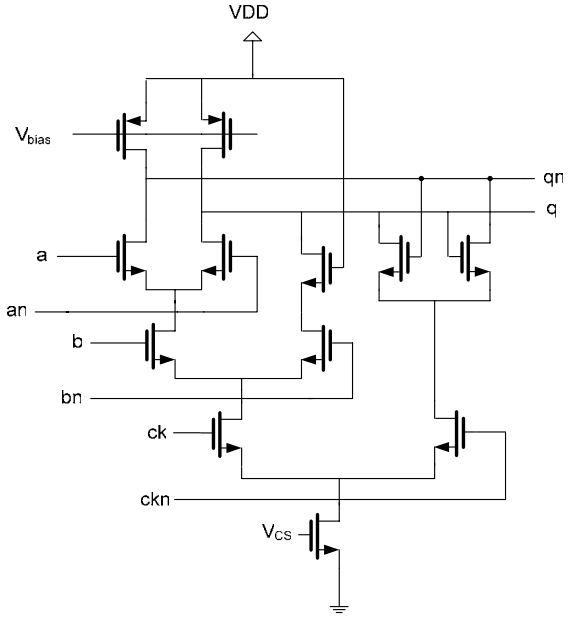


Fig. 4.26 SCL implementation of an AND gate combined with a latch function

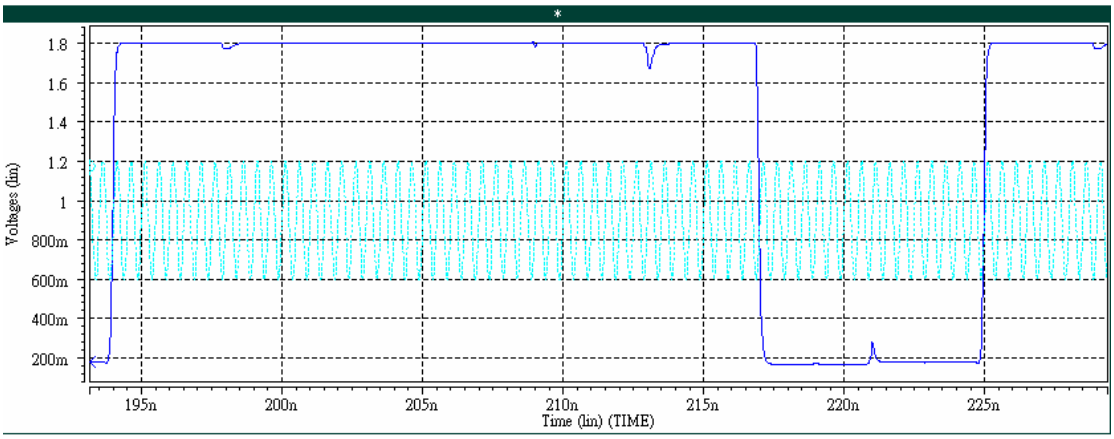


Fig. 4.27 The simulation of divide-by-62 frequency divider

4.4.6 Sigma-Delta Modulator

The sigma-delta modulator can randomize the feedback division ratio and result in a helpful noise shaping of the phase noise introduced by fractional-N division. The digital realization of a 7-bits pipelined second order ΣΔ modulator is shown in Fig. 4.28. It is composed of two accumulators and a noise cancellation network. Each accumulator only employs a 7-bits adder and several registers. However, the noise cancellation network is more complex. The detail of the noise cancellation network design will be discussed in the following.

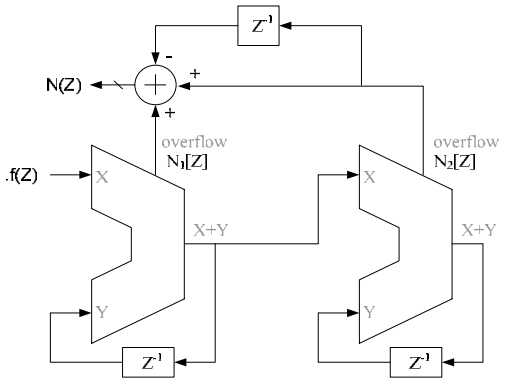


Fig. 4.28 Second order ΣΔ modulator

Fig. 4.29 shows the noise cancellation network of the second order ΣΔ modulator. In order to simply design, we analyze each adder's logics states and design the decoder for it. First of all, the adder A has three states such as -1, 0, and 1, as shown in Table IV.

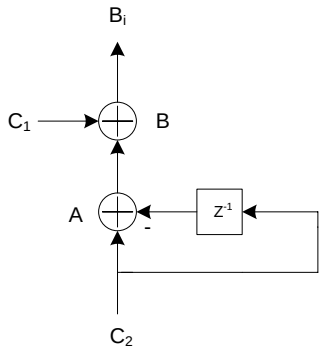


Fig. 4.29 Noise cancellation network

TABLE IV Noise cancellation Network coding (A)

C_2	C_2^{-1}	Decimal number	2's complement
0	0	0	000
0	1	-1	111
1	0	1	001
1	1	0	000

Observe the 2's complement table, we can find that the highest two bits are the same. So, we can simplify the out of adder A as

$$\text{Two MSB} = \overline{C_2} \times C_2^{-1} \tag{4.9}$$

$$\text{LSB} = C_2 \oplus C_2^{-1} \tag{4.10}$$

Then, we check the adder B where C_1 is added to the output of adder A. Only three half-adders are used here and adder B's output is tabulated in Table V. According to Table V, we can conclude that the output of adder B has only four states (000, 001, 010, 111) and can control the division modulus as N, N+1, N+2, N-1. From the above analysis, the total error cancellation network is shown in Fig. 4.30 [38]. Finally, a simplified flow chart of the modulation is illustrated in Fig. 4.31.

TABLE V Noise cancellation Network coding (B)

C_2	C_2^{-1}	C_1	Decimal number	2's complement
0	0	0	0	000
0	1	0	-1	111
1	0	0	1	001
1	1	0	0	000
0	0	1	1	001
0	1	1	0	000
1	0	1	2	010
1	1	1	1	001

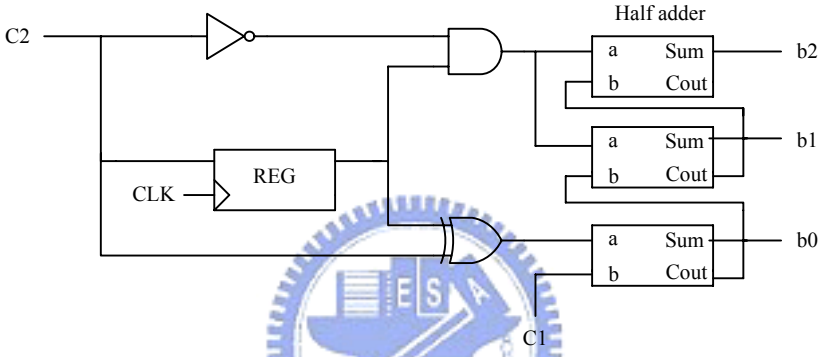


Fig. 4.30 Realization of the noise cancellation network

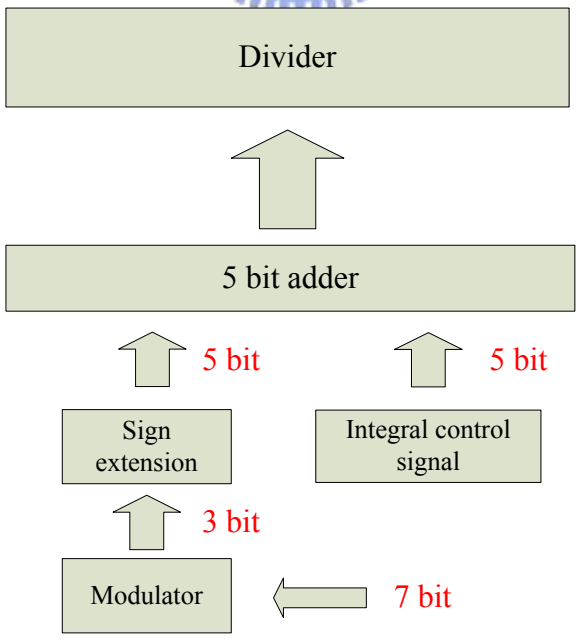
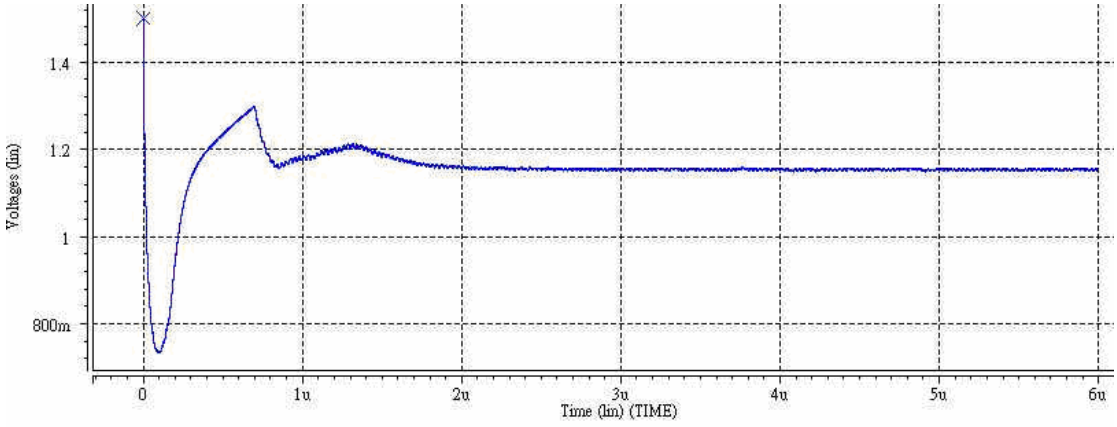


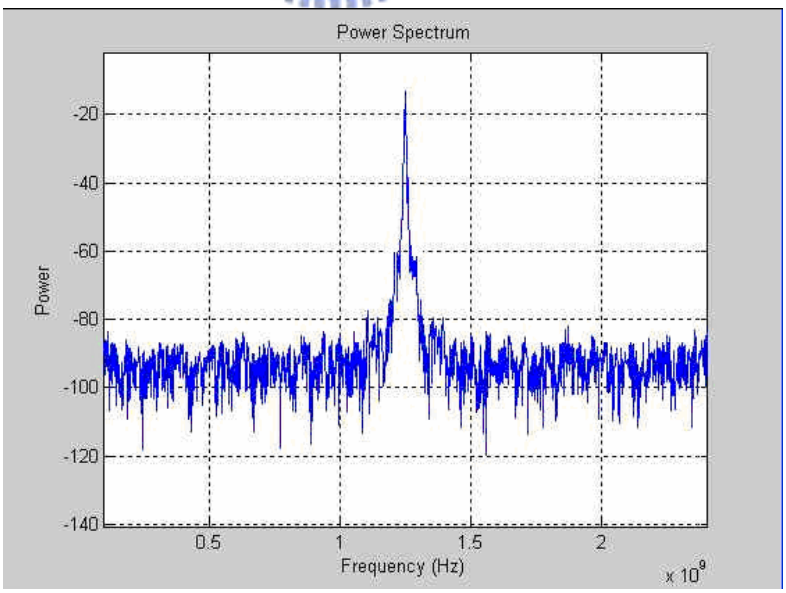
Fig. 4.31 The flow chart of the modulation

4.5 Fractional-N Frequency Synthesizer System

By providing external digital control codes, the synthesizer can generate any desired frequency. Two extreme conditions are considered. Fig. 4.32 shows the transient response of the control voltage of the VCO and its output spectrum when 1.27 GHz LO is needed. On the other hand, Fig. 4.33 shows the simulation results when 2.08 GHz LO is needed.

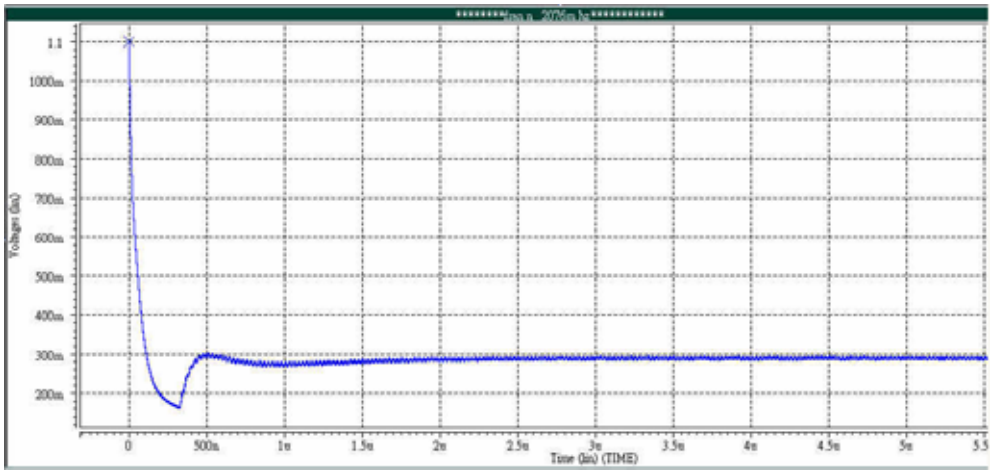


(a)

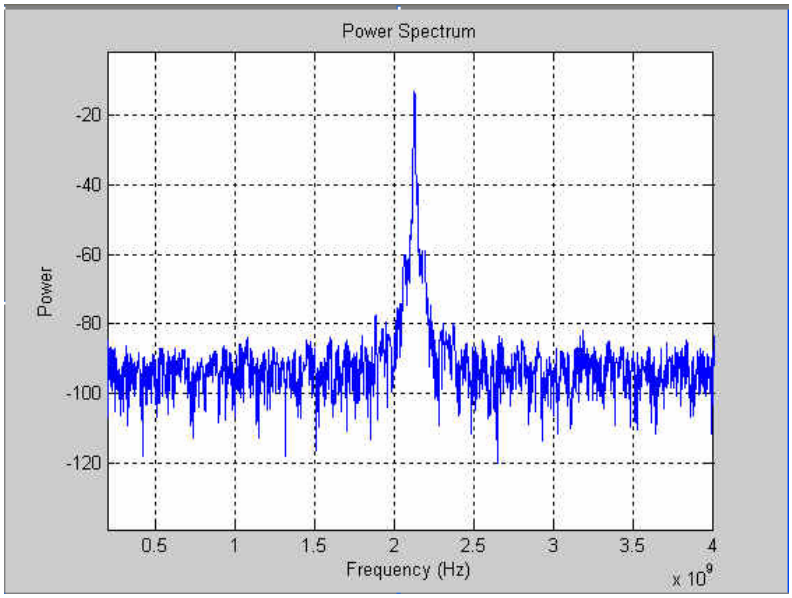


(b)

Fig. 4.32 (a) VCO control voltage and (b) Out Spectrum when LO is 1.27GHz



(a)



(b)

Fig. 4.33 (a) VCO control voltage and (b) Out Spectrum when LO is 2.08 GHz

With Fig. 4.32 and Fig. 4.33, we prove that the frequency synthesizer can meet all the frequency range which we expect through the change of the control voltage of the VCO. The parameters and performance summaries of the frequency synthesizer are listed in Table VI.

TABLE VI Performance of the ΣΔ frequency synthesizer

Technology	TSMC 0.18-um 1P6M CMOS
Chip area	0.92mm × 0.92mm
Supply voltage	1.8V
Reference frequency	36 MHz
Output frequency	1.27 GHz ~ 2.08 GHz
VCO gain	866 MHz / V
VCO output swing	190 mV
Phase noise@1 MHz offset	-100 dB / Hz
Phase margin	56 degree
Loop bandwidth	900 kHz
Channel bandwidth	6 MHz
Setting time	< 3us
Maximum power consumption	13.08 mW

The overall synthesizer layout is shown in Fig. 4.34 and the PCB layout is shown in Fig. 4.35.

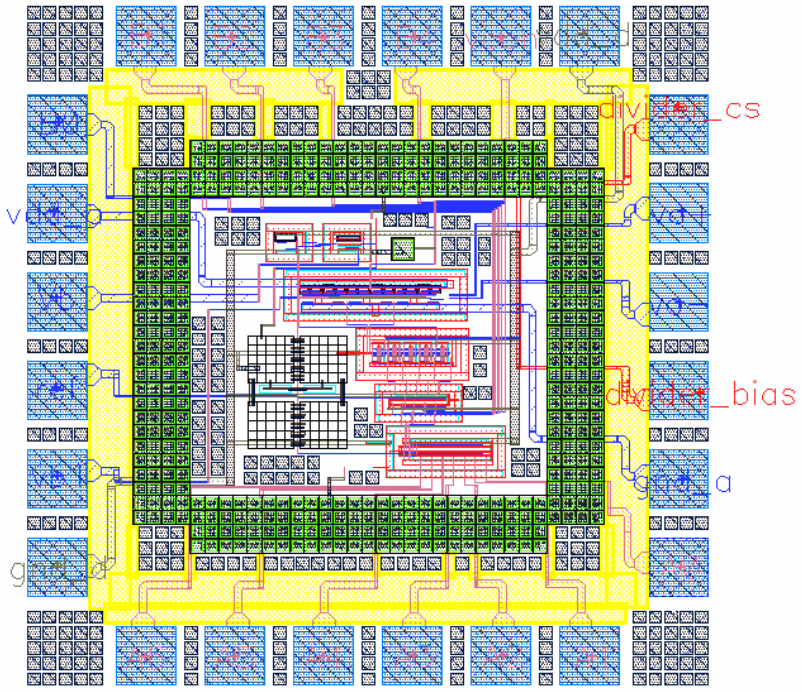


Fig. 4.34 Physical layout of the ΣΔ frequency synthesizer

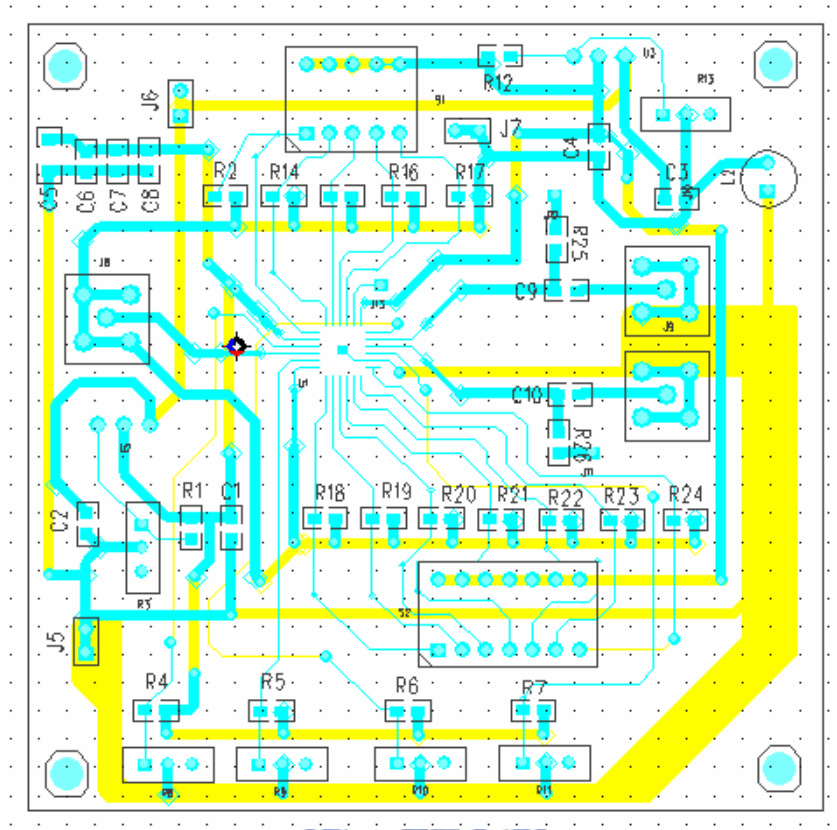


Fig. 4.35 The PCB layout

Chapter 5

Testing Setup and Experimental Results

5.1 Introduction

In this Chapter, we present the testing environment, including the instruments and components on the print circuit board (PCB). The experimental results for the ΣΔ frequency synthesizer described in Chapter 4 will be presented.

5.2 Experimental Results

5.2.1 Prototype

The proposed ΣΔ frequency synthesizer has been implemented in a single IC that has been fabricated in a 0.18-μm 1P6M CMOS process. Fig. 5.1 shows the microphotograph of the synthesizer. This chip uses a total of 24 pads including reference clock input, VCO differential outputs, digital control signals, and bias voltages. The total area of the chip is 0.92×0.92 mm^2.

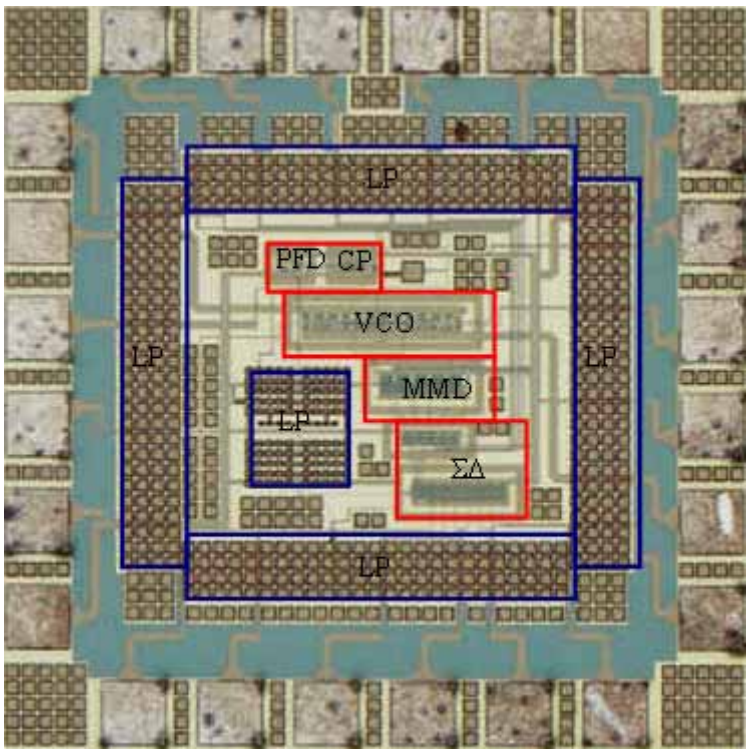


Fig. 5.1 Die microphotograph

5.2.2 Test Setup

The fabricated synthesizer was tested to determine its performance. Measurement was performed with raw dies mounted on the PCB to prevent the parasitic effect of the package. Because the synthesizer is a mixed-mode system, we separate the powers and grounds of digital and analog parts. Then, we connect the ground of analog part and that of digital part with an inductor. The inductor shorts the DC voltage of the digital and analog grounds, while preventing the high-frequency noise in the digital circuit from coupling to the analog circuit by their grounds.

The analog and digital powers are generated by LM317 adjustable regulators as shown in Figure 5.2. The regulator circuit is easy to use and the output voltage could be predicted by equation (5.1)

$$V_{OUT} = 1.25\left(1 + R_1 / R_2\right) + I_{ADJ} \cdot R_2 \qquad (5.1)$$

The I_{ADJ} is the DC current that flows out of the ADJ terminal of the regulator. Besides, the capacitors C_1 and C_2 are the bypass capacitors.

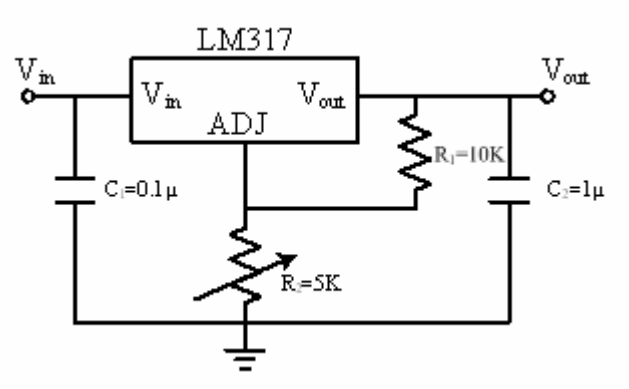


Fig. 5.2 LM317 regulator

The outputs of the regulators are bypassed on the PCB with the parallel combination capacitors then connected to the chip. The bypass filter network is combined by 10μF, 1μF, 0.1μF and 0.01μF capacitors as shown in Fig. 5.3. The arrangement can provide decoupling of both low-frequency noise with large amplitudes and high-frequency noise with small amplitudes [39].

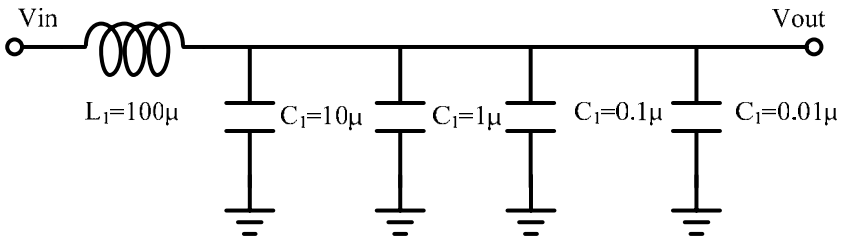


Fig. 5.3 Bypass filter at the regulator output

The measurement setup of the synthesizer is shown in Fig. 5.4. The input clock is produced from the signal generator (Agilent 33250A). The output spectrum is observed by a Spectrum Analyzer (Agilent E4440A). Fig. 5.5 shows the photograph of the related instruments. The testing PCB is shown in Fig. 5.6.

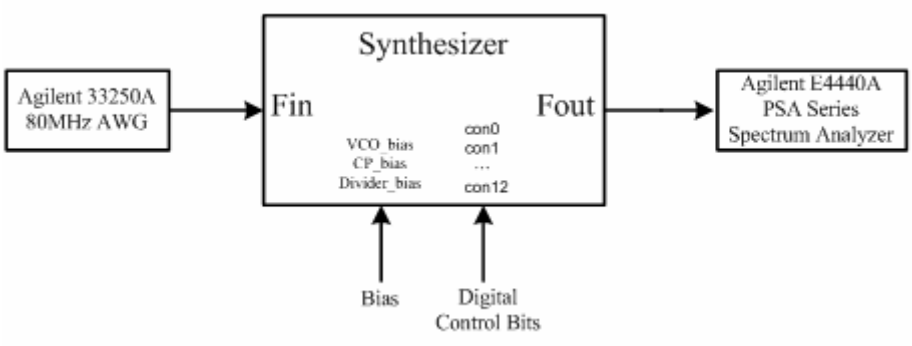


Fig. 5.4 Measurement setup of the synthesizer

(a)

(b)

Fig. 5.5 Photograph of (a) Waveform generator (b) Spectrum analyzer

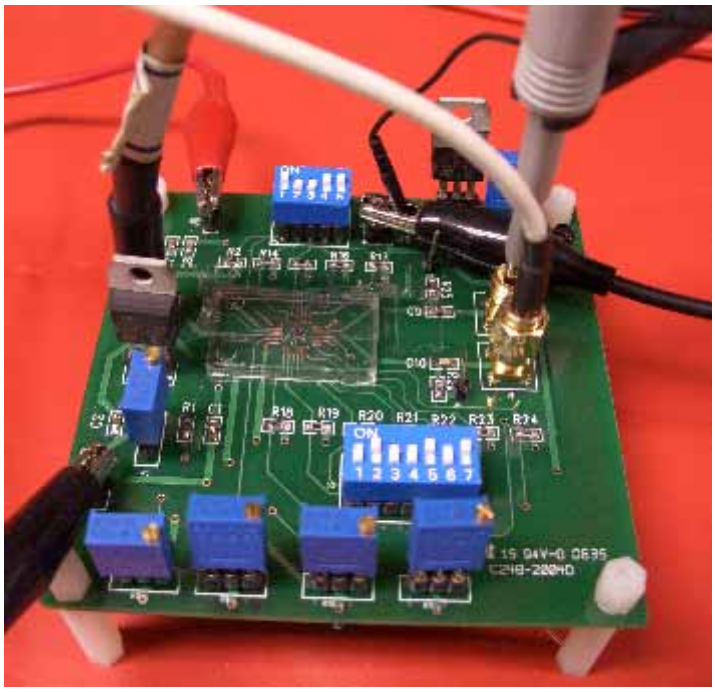


Fig. 5.6 The testing PCB in the synthesizer

5.2.3 Measurement Results

In this section, we will discuss the measurement results of the synthesizer. Firstly, we test the VCO's free running frequency and tuning range. The measured VCO transfer curve is shown in Fig. 5.7. The free running frequency for the VCO is within the process corner and has a tuning range between 844 MHz and 2340 MHz. Table VII compares the simulation results with the measurement results

Secondly, we test the overall system of the frequency synthesizer. By changing the digital control bits, we can synthesize different output frequency. Fig. 5.8 displays the output signal spectrum of 2.28 GHz with the phase noise -66.79 dBc/Hz at 1-MHz offset. Fig. 5.9 shows the measured phase noise. Table VIII summarizes the measured performance of the synthesizer.

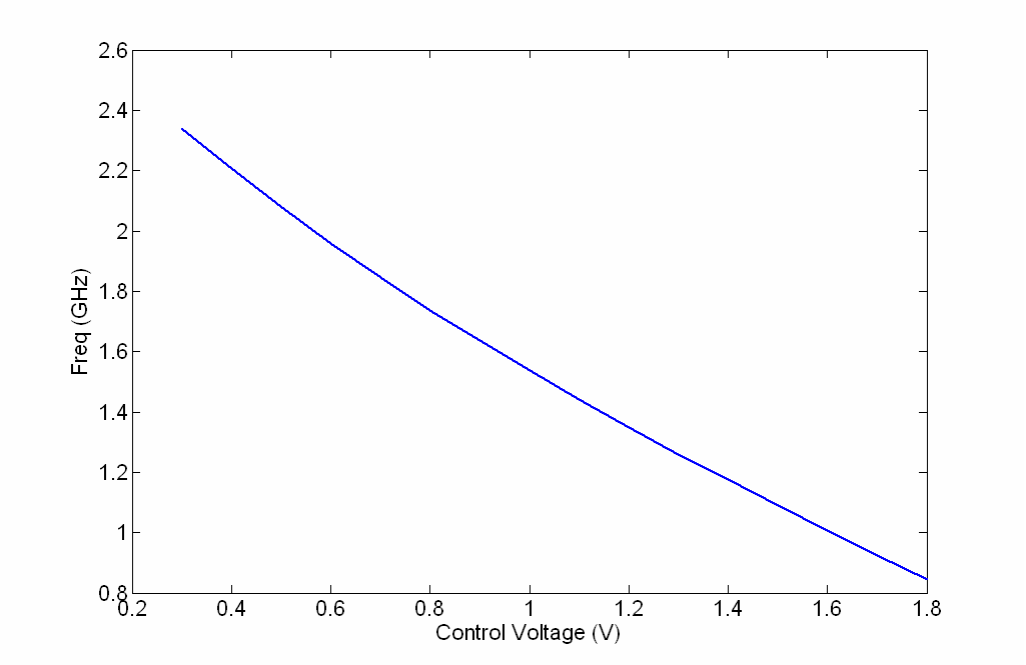
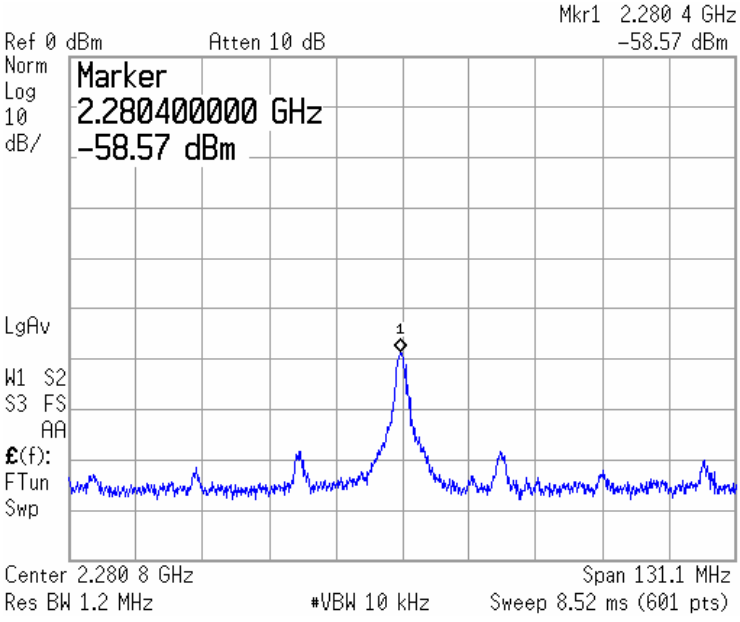


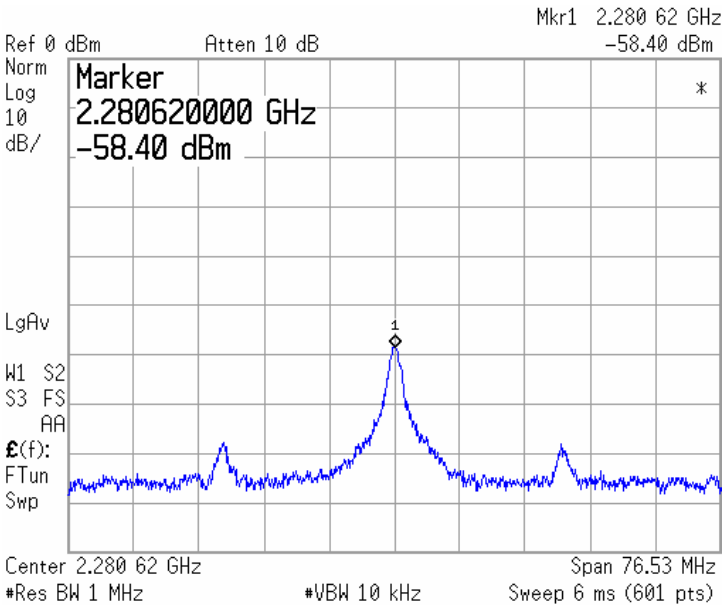
Fig. 5.7 The measured VCO transfer curve

TABLE VII Comparisons between simulation and measurement

Spec	Simulation	Measurement
f_{max} (MHz)	2330	2340
f_{min} (MHz)	770	844
tuning range	1560	1496
K_{VCO} (MHz / V)	867	831



(a)



(b)

Fig. 5.8 The output spectrum of the synthesizer at 2.28 GHz with (a) Span = 131.1 MHz and (b) Span = 76.53 MHz

Fig. 5.9 The measured phase noise

TABLE VIII Performance summary

Technology	TSMC 0.18-um 1P6M CMOS
Chip area	0.92mm × 0.92mm
Supply voltage	1.8V
Reference frequency	36 MHz
Output frequency	1.69 GHz ~ 2.28 GHz
Synthesizer output swing	30 mV
Phase noise@1 MHz offset	-66.79 dB / Hz
Channel bandwidth	6 MHz
Maximum power consumption	20.3 mW

5.3 Conclusion and Discussion

From the measurement, the function of the synthesizer is verified but the output power is small. We guess that the phenomenon results from the improper operation voltage at the open drain buffer. The loading effect of the divider causes the large size NMOS to operate in the linear region. So, the out signal is not amplified. The way to improve the problem is that we make the output of the VCO to feed a coupling capacitor, and then connects to the open-drain buffer with a resistor biasing its gate terminal, as shown in Fig. 5.10.

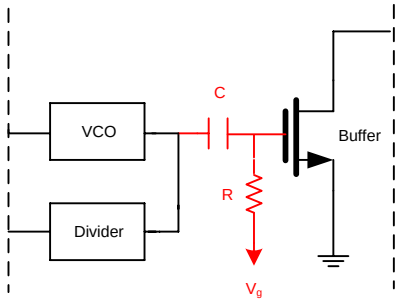


Fig. 5.10 The modified output buffer

Another problem is that the synthesizer can not cover the full frequency band of interest. Besides, the phase noise is not good as we expected. Trace the reason carefully, we find that the defect might come from the process variation and un-prefect layout skill. It affects the linearity of the VCO and the designed loop filter parameters. These factors may cause the PLL to be unlocked in some region. In view of this, we should get more insight into the layout skill and process variation.

Chapter 6

Conclusions and Future Work

A fractional-N synthesizer is presented in this thesis including the history, the simulation and the fabrication to the measurement. Basically, the PLL synthesizer is composed of five building blocks: the phase detector, the charge pump, the loop filter, the VCO and the programmable divider. A lot of design challenges can be found in each block, but this work has tackled the problems of the VCO tuning range. We proposed a improved VCO circuit to widen its frequency tuning range and then to integrate in the frequency synthesizer.

Another interesting study is the delta-sigma modulator. The all-digital DSM is widely used in the fractional-N synthesizer because of many good properties. One major advantage is the reduction of the reference spur by randomizing the feedback division ratio such that the quantization noise of the fractional-N divider is transferred to higher frequency. Researches on all-digital DSM could be another topic for the fractional-N synthesizer.

In order to optimize the synthesizer performance, some features should be taken care of. Firstly, the divider should be designed more cagily because it is another component in the synthesizer to operate at radio-frequency. Secondly, the layout of the whole synthesizer, especially the VCO, should be considered carefully. Finally, the analog and digital supplies should be separated for reducing the noise

coupling.

Some suggestions for the future work are given as follows. Firstly, the ESD protection should be considered in the circuit design and physical layout to avoid the instantaneous high voltage breaking down the circuit. Secondly, the voltage supplies of different functional blocks of the synthesizer should be separated for debugging. Finally, parallel control bits of the modulator can be designed as serial input scheme to reduce the large number of PAD, which will save the area.

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