國立交通大學

電信工程學系

碩士論文

應用於 IEEE 802.11a/b/g 之雙頻帶低雜訊放大器和偶次諧波降頻混頻器以及使用 0.18um CMOS 製作之 Ka 頻低雜訊放大器和 K 頻壓控震盪器

A Dual-Band LNA and a Sub-harmonic Mixer for IEEE 802.11a/b/g Application and a Ka Band Low Noise Amplifier and a K Band VCO by Using 0.18um CMOS Process

研究生：張文明

指導教授：周復芳　博士

中 華 民 國 九 十 五 年 六 月

應用於 IEEE 802.11a/b/g 之雙頻帶低雜訊放大器和偶次諧波降頻混頻器以及使用 0.18um CMOS 製作之 Ka 頻低雜訊放大器和 K 頻壓控震盪器

A Dual-Band LNA and a Sub-harmonic Mixer for IEEE 802.11a/b/g Application and a Ka Band Low Noise Amplifier and a K Band VCO by Using 0.18um CMOS Process

研究生：張文明　　Student: Win-Ming Chang

指導教授：周復芳　博士　　Advisor: Dr. Christina F. Jou

國 立 交 通 大 學

電 信 工 程 學 系 碩 士 班

碩 士 論 文

A thesis

Submitted to Department of Communication Engineering

College of Electrical and Computer Engineering

National Chiao Tung University

In Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in Communication Engineering

June 2006

Hsinchu, Taiwan, Republic of China

中華民國九十五年六月

應用於 IEEE 802.11a/b/g 之雙頻帶低雜訊放大器和偶次諧波降頻混頻器以及使用 0.18um CMOS 製作之 Ka 頻低雜訊放大器和 K 頻壓控震盪器

研究生：張文明　　指導教授：周復芳　博士

國立交通大學電信工程研究所　碩士班

摘　　要

本論文討論應用於射頻接收機的高頻電路設計且主要分為兩個主題探討。其中第一部份是增益可調切換式雙頻帶低雜訊放大器及一個新型切換轉導式偶次諧波降頻混頻器的分析和設計。另一部份是一個 Ka 頻帶的低雜訊放大器驗證，最後我們以一個 K 頻帶頻率信號源作為未來的研究專題。

緊接著我們設計並製作一個使用 0.18um CMOS 製程，操作在 2.45GHz/ 5.25GHz 的增益調整式雙頻帶低雜訊放大器。在高增益模式時，此放大器在 2.45-GHz 表現 14.4dB 的功率增益及 3.54dB 的雜訊指數。在 5.25-GHz 則有 12.02dB 的功率增益及 2.88dB 的雜訊指數。此低雜訊放大器在雙頻帶皆有大約 11dB 的增益可調範圍，

我們使用 0.18um CMOS 製程設計並驗證切換轉導技術的新型偶次諧波降頻混器。此全整合的次諧波混頻器量測結果顯示使用 4dBm 的本地震盪器，在中頻 10MHz 可得到 12.8dB 的降頻轉換功率增益，-1.8dBm 三階諧波交會點，和 14.0dB DSB 雜訊指數。

接下來，一個使用標準 0.18um CMOS 製程的三級 Ka 頻帶低雜訊放大器被製作及驗證。在 32-GHz 時，量測出 12.08dB 的功率增益及 5.325dB 的雜訊指數，總功率消耗為 15.58 毫瓦。

最後，一個使用 0.18um CMOS 低相位雜訊 X 頻帶四項位壓控震盪器倍頻而成的 K 頻帶頻率訊號源已被模擬，此 K 頻訊號源也當作此論文的將來專題研究

A Dual-Band LNA and a Sub-harmonic Mixer for IEEE 802.11a/b/g Application and a Ka Band Low Noise Amplifier and a K Band VCO by Using 0.18um CMOS Process

Student: Win-Ming Chang Advisor: Dr. Christina F. Jou

Institute of Communication Engineering

National Chiao Tung University

ABSTRACT

This thesis discusses high frequency circuit design for RF receivers and it mainly includes two parts. One is the analysis and design of a switched dual-band LNA with variable gain and a new switched Gm sub-harmonic mixer. The other is the demonstration of a Ka band LNA, and finally a K band frequency source with X band low phase noise quadrature VCO is simulated for feature work.

A switched dual-band low noise amplifier with four gain control modes operating at 2.45-GHz/5.2-GHz has been designed and demonstrated based on a 0.18-um CMOS process. In the high gain mode, the LNA approaches 14.4 dB maximum power gain and 3.54 dB DSB noise figure at 2.45-GHz. In the 5.25-GHz band, the maximum power gain is 12.02 dB and the DSB noise figure is 2.88 dB.

A new prototype of sub-harmonic mixer using switched Gm technique is designed and implemented in a standard 0.18um CMOS technology. This fully integrated sub-harmonic mixer achieves measured high conversion power gain of 12.8 dB, -1.8 dBm IIP3, and 14.0 dB noise figure at 10-MHz with 4 dBm LO power.

A 3-stage Ka band LNA has been designed and verified by using standard CMOS 0.18um process. The measured power gain at 32-GHz is 12.08 dB with noise figure of 5.325 dB while consuming 15.58 mW.

Finally, a K band frequency source with X band 0.18um CMOS low phase noise quadrature VCO has been simulated. This K band frequency source is treated as feature work in our thesis.

Acknowledgement

首先，我要感謝指導教授周復芳老師，在這短短兩年的指導及關心，尤其是在發表國際論文上提供很多寶貴意見且抽空幫學生修改，讓學生在碩士生涯獲益良多。並且感謝博士班鄭國華學長的耐心指點，在問題重重的兩年提供我不少研究方向，並在學業上鼓勵及給予信心。

在此要特別感謝系上的高銘盛老師對此論文的細心更改及提供意見，讓此論文更有深度，且感謝老師在當初進到交大電信系時的指導及方向指引，讓學生真正在研究路上找到自己的興趣所在。

還有感謝 919 實驗室的博班學長學匯儀，同學宏斌，仕豪，政展，秋榜，博揚以及學弟妹子豪，宇清，宜星，智鵬，瑞嫻，寶明一起在實驗室的日子，雖然研究是辛苦的，但是實驗室夥伴的共同闖拼讓這兩年過的相當充實快樂。

最後謝謝家人的支持，不管事精神上或是實質的供給，讓我無後顧之憂得順利取得碩士學位，也能諒解我平常假日幾乎回不了家的苦衷。

CONTENTS

LIST OF TABLE

LIST OF FIGURE

Chapter 1

INTRODUCTION

1.1 Background and Motivations

The multi-standard wireless LAN transceiver and millimeter-wave integrated circuits using CMOS technologies are becoming the major design because of the consideration of low-cost and high integration. In the application of wireless LAN, IEEE 802.11a and IEEE 802.11b/g use frequency bands of 5.15-GHz ~ 5.35-GHz and 2.4-GHz ~ 2.4835-GHz, respectively. Therefore a dual-band RF receiver front-end is required for the integration of wireless LAN.

The growing demand for larger bandwidth motivates integrated circuits to move toward higher frequencies. In the past, GaAs-based HEMT and HBT technology dominate most of the applications due to lossless substrate in these processes. But the more attractive process, CMOS, has resulted in a strong motivation to implement these high-frequency and high-performance RF systems. A high performance CMOS front-end for applications above 20-GHz has been reported and the performance of these CMOS circuits show CMOS process has potential for building RF systems above 20-GHz. Finally, a K band frequency source has been simulated and this work is treated as feature work of our thesis.

The following thesis presents a switched dual-band LNA with four gain modes, a new switched Gm sub-harmonic mixer and a Ka band LNA. These circuits are simulated with Eldo RF, ADS 2004A, and sonnet 9.52. The fabricated chips using TSMC 0.18um CMOS process are tested and measured in CIC and National Center University.

1.2 Thesis Organization

This thesis discusses about high frequency circuit design for RF receivers and it includes two parts. One is the analysis and design of a switched dual-band LNA with variable gain and a proposed new sub-harmonic mixer. The other is the design procedure and analysis of a LNA for Ka band application. These two parts will be illustrated in chapter 2 and chapter 3 and these RF components are all implemented and verified by TSMC 0.18um CMOS technology.

In chapter 2, first we introduce the system applications of 802.11a/b/g that are widely used in recent days. And the frequency occupation of these systems is the major discussion for our RF circuits design. The proposed dual-band receiver will also be discussed in Section 2.4.1. The design flows of the switched dual-band LNA and the proposed new sub-harmonic mixer will then be explained in Section 2.4.2~2.4.3. The characteristic of a switched dual-band LNA is similar to a single-band LNA. Hence, the analysis including input matching, noise figure and power dispassion are expressed for a single band LNA. The down conversion principle is the major discussion for our proposed new sub-harmonic mixer. To understand the down conversion operation and switched Gm technique, we start from the basic Gilber mixer, a switched Gm mixer and finally a tradition sub-harmonic mixer. By these mixer prototype analyses, the proposed new sub-harmonic mixer is organized and presented in Section 2.4.3.3. Also the measurement results, discussion and comparisons with other literatures are presented in this chapter.

In chapter 3, a Ka-band LNA is designed and verified by using TSMC 0.18um CMOS process. The design procedures of a millimeter-wave circuit are based on the analysis of [1], and they are explained in Section 3.3.1~3.3.5. Two simulators including sonnet 9.52 and ADS 2004A is applied in this Ka band LNA design. The simulation results are shown in Section 3.3.6. Finally the measurement results and comparisons with recent published literatures are also illustrated in this chapter.

In chapter 4, a K band frequency source is treated as a feature work in our thesis. By doubling an X band quadrature CMOS VCO, the K band VCO performs low phase noise and high FOM. The K band frequency source has been simulated by TSMC 0.18um CMOS process, and the chip will be tested in August, 2006.

Chapter 2

SWITCHED DUAL-BAND LNA WITH FOUR GAIN MODES AND NEW SWITCHED GM SUB-HARMONIC MIXER

2.1 Introduction

As the wireless applications expand, requirements for radio which can support multiple bands and multiple standards are increasing. These demands are typically realized by using more than one set of RF blocks which can govern the bands. But these must increase unnecessary power consumption, die area, which in turn increase cost [2]. A way to alleviate these conditions can be accomplished by using one RF block that can handle multiple bands, such as a switched-band RF block, which not only reduces the power consumption but also rejects out-of band signals compared to broadband circuits that cover multiple bands. [1] [13].

The multi-standard wireless LAN transceiver using CMOS technologies are becoming the major design because of the consideration of low cost and high integration. In the applications of wireless LAN, IEEE 802.11a uses the frequency bands of 5.15-GHz ~ 5.35-GHz and 5.725-GHz ~ 5.825-GHz while IEEE802.11b/g uses 2.4-GHz~2.4835-GHz [18]~[20]. And these standards have similar characteristics such as channel bandwidth and modulation method that they have potential to integrate together in a single receiver to lower the cost. To integrate the two bands into a single receiver, a dual-band LNA operating in both 2.4-GHz and 5-GHz band is required first. To prevent the signals in both bands affect each

other, a switched dual-band LNA prototype is used in the integration. The receiver blocks are also designed to have higher performance including integration complexity, image rejection, and power consumption. A low intermediate frequency (IF) structure is selected to lower the integration complexity and therefore lower the cost [10]~[11]. Image signal is still a serious issue in a low IF receiver. In the proposed dual-band receiver, the I/Q signal are useful in an image rejection architecture. With the usage of sub-harmonic mixer in the proposed receiver, only a quadrature signal frequency synthesizer is demanded to down convert the dual-band signals. The practice of sub-harmonic mixer significantly reduces the receiver complexity as well as power consumption [11]. As illustrated above, the switched dual-band LNA and the sub-harmonic mixer must be realized first to achieve the proposed dual-band receiver.

2.2 Comments

2.2.1 Switched Dual-Band LNA

There are two types of dual-band LNA, one is concurrent receiving and the other is switched bands. The concurrent receiving may suffer a serious problem. While a strong signal received in one band in this concurrent LNA, the circuit will exhibit in saturation that causes the other band to operate irregularly. Switched dual-band procedure can select the desired band without receiving the other one. The switched dual-band LNA presented here operates at 2.45-GHz and 5.25-GHz for wireless LAN application. And it achieves high gain and low noise figure in both bands

In addition, as the power of the received RF signals vary with the distance from the transmitter. In order to linearly amplify the RF signals or keep each RF block to operate at linear region, the LNA must be able to have high gain and low gain modes to avoid saturating the next RF block. The switched dual-band LNA proposed in this paper can switch between 2.45-GHz/5.2-GHz by switching the inductor on /off at the output resonator, and also the

input transistors gain modes. The gain control scheme is accomplished by lowering down the gate bias of the input transistors. In low gain modes, the power consumption can be economized. However, the input return loss (S_{11}) must shift to low frequency. The four shunt NMOS transistors cascading on the input transistors can modify the input transistor's drain-to-source voltage and hence the S_{11}. The four shunt NMOS transistors can be controlled by baseband as the receiving power is too large to saturate the following RF blocks [3].

2.2.2 Proposed Switched Gm Sub-Harmonic Mixer

Mixers are widely used for frequency translation in radio frequency communication systems. In a radio receiver, the down-conversion mixer is the key building block since it dominates the system linearity [4]~[6]. Among many proposed active mixers, the Gilbert-cell mixer has been widely used and the double-balanced mixer has been preferred since it can suppress large LO leakage signals at output. The conversion gain, noise figure and linearity are key performance parameters. Here, we take these parameters into account in our proposed sub-harmonic mixer.

Sub-harmonic mixer architectures use second or higher order harmonics of the LO signal for up or down conversion. Lower LO frequency significantly simplifies transceiver design, especially for blocks like frequency synthesizers, oscillators. These mixers are also suitable for constructing multi-standard systems sharing a common LO signal generation scheme [30].

The proposed sub-harmonic mixer can be used in dual-band receivers that the higher band frequency is almost twice of the lower one. Take 2.45-GHz and 5.25-GHz dual-band receiver for example. By the usage of sub-harmonic mixer, there is only one frequency synthesizer needed to receive dual band signals [32].

By the switched Gm prototype, the proposed sub-harmonic mixer consumes no dc power without LO input. Otherwise, the combination of switched Gm technique and PMOS active

load let the proposed mixer exhibit sufficient voltage headroom and therefore conversion gain will not be limited.

The measured buffer power consumption, 22.36mW, reveals that the fabricated mixer locates in SS-corner. Although the results are different from the desired TT-corner, we still compare the SS-corner simulation with the measured results.

2.3 Wireless LAN Standard Review

In this section, the wireless LAN standard, IEEE802.11a/b/g, will be reviewed. It will help us to understand the identical characteristics in these bands and tell us why integrating these standards together. The IEEE802.11b standard at the 2.4-GHz ISM (industrial, scientific, and medical) band provides data rate up to 11Mbits/s with the direct sequence spread spectrum (DSSS). The standard was released by IEEE in 1999. The 802.11a standard at 5-GHz U-NII band provides data rate up to 54Mbits/s using OFDM (orthogonal frequency division multiplexing) modulation. The IEEE 802.11g standard, operating at the same band of 802.11b, uses OFDM modulation and contributes data rate up to 54Mbits/s. There are several identical properties in these standards and they will be introduced in the following illustration.

2.3.1 IEEE 802.11a

As shown in Fig. 2-1, the 802.11a standard has three U-NII (Unlicensed National Information infrastructure) bands. They includes the lower band (5.15-GHz ~ 5.25-GHz), the middle band (5.25-GHz ~ 5.35-GHz) and the upper band (5.725-GHz ~ 5.825GHz). The lower and middle sub-bands have rooms for eight channels in the total bandwidth of 200-MHz. The upper band has rooms for four channels in a bandwidth of 100-MHz. The centers of the outermost channel shall be at a spacing of 30-MHz from the edge of band for the lower and middle bands, and 20-MHz for the upper band. The bandwidth of each channel is 20-MHz, and each channel has 52 sub-carries for OFDM modulation with each sub-carrier

has bandwidth of 312.5-KHz. Each sub-carrier can be either a BPSK, DQPSK, 16QAM, 64QAM signal. [18] Each data rate corresponding to modulation is listed in Table 1.

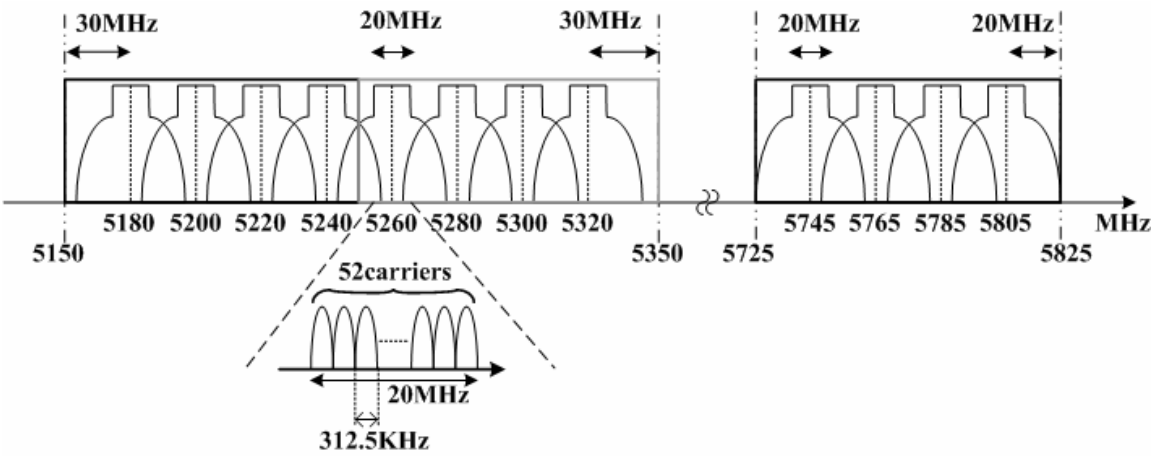


Fig. 2-1 Channel allocation of IEEE 802.11a standard

Modulation	Data Rate (Mbps)
BPSK	6,9
DQPSK	12,18
16QAM	24,36
64QAM	48,64

Table 1 Comparison of each modulation and its transferring data rate in IEEE 802.11a standard

2.3.2 IEEE 802.11b

IEEE 802.11b standard can be discriminated between operating in North American and European. In North American, its operating frequency is from 2400-MHz to 2472-MHz while the frequency range in European is from 2400-MHz to 2483.5-MHz. Here we adopt the former. For non-overlapping operation three channels are used and the channel center frequencies are 2412-MHz, 2437-MHz, and 2462-MHz. For overlapping operation, six channels are selected. The center frequency of each channel has a spacing of 10-MHz. Fig.

2-2 is the channel location of 802.11b standard for non-overlapping and overlapping. The standard offers a data rate up to 11 Mbps and uses direct sequence spread spectrum (DSSS) and the complementary code keying (CCK) modulation [19].

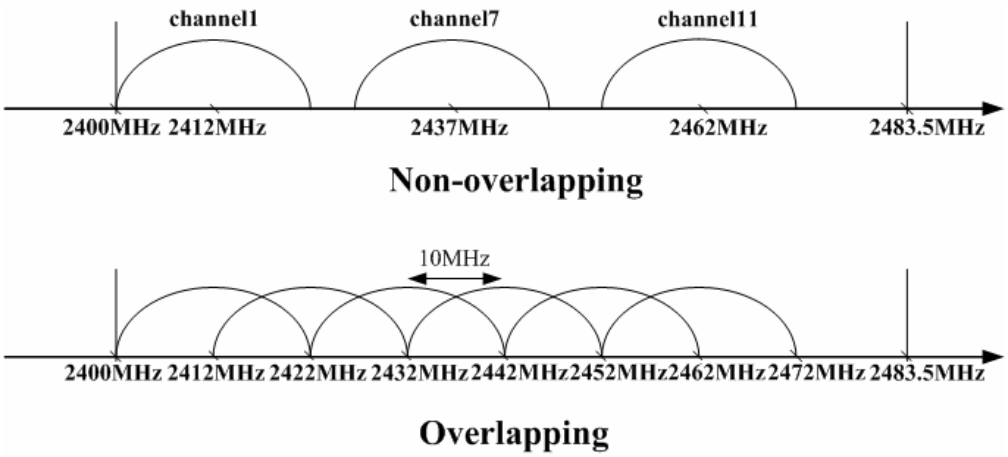


Fig. 2-2 The North American channel selection of non-overlapping and overlapping

2.3.3 IEEE 802.11g

The IEEE802.11g operates from 2412-MHz to 2483-MHz, and the bandwidth is 20-MHz for each channel. It extends the data rate of 802.11b to 54 Mbps in the 2.4-GHz band using OFDM modulation. It also has three non-overlapping channels [20]. The three standards are compared and listed in Table 2.

Standards	IEEE 802.11a	IEEE 802.11b	IEEE 802.11g	
Frequency (MHz)	5150~5350 5725~5825	2400~2483	2400~2483	
Modulation	OFDM	CCK	OFDM	CCK
Data Rate (Mbps)	6~54	1~11	6~54	1~11
Available Spectrum (MHz)	300	83.5	83.5	
Channel Bandwidth (MHz)	20	25	25	25

Table 2 The comparison of the 802.11 a/b/g standards

2.4 Circuit Design Consideration

2.4.1 Proposed Dual-Band Receiver

As illustrated in the introduction, low-IF architecture is preferred because it reduces the integration complexity and has no dc offset issue [6]. On the other hand, the low-IF receivers do have image problems. This problem can be solved by the image cancellation schemes, and we proposed the Weaver architecture in our receiver to do image rejection [4]. Since the digital modulation of IEEE802.11a/b/g compared above illustrates the I/Q formats are required to demodulate the transmitted signal, the I/Q down conversion is also considered in this proposed dual-band receiver.

With a simple modification the Weaver architecture readily provides quadrature outputs [4], as is needed for many modulation types, and it is this architecture that is used in this receiver. The modification involves replacing the second set of modulators by two pairs of quadrature mixers and then properly combining their contributions.

Fig. 2-3 is the proposed dual-band receiver in this project. The receiver can be divided into two frequency translations, one is down conversion to 10-MHz and then down conversion to baseband by a 10-MHz oscillator. A 10-MHz LO signal is convenient to be obtained by the reference signal of the synthesizer using in the first down conversion and this arrangement lower cost significantly. The two frequency translations compose the quadrature Weaver architecture to alleviate the issue of image signal and simultaneously produce the I/Q signals. The IF-band pass filter is easy to design and it exhibits high selectivity because of the selected low intermediate frequency. Fig. 2-4 is the frequency plan in this dual-band receiver. For simplicity, the dual-band LNA and sub-harmonic mixer designed here obey the frequency in Fig. 2-4. That is, the RF is 5.25-GHz for 5-GHz band and 2.45-GHz for 2.4-GHz band; the LO is 2.62-GHz and 2.44-GHz for 5-GHz and 2.4-GHz frequency down conversion,

respectively. By the IEEE802.11a/b/g standards, the frequency synthesizer demanded here must provide a tuning range from 2.39-GHz to 2.67-GHz. The tuning range is about 11% of the oscillation center frequency.

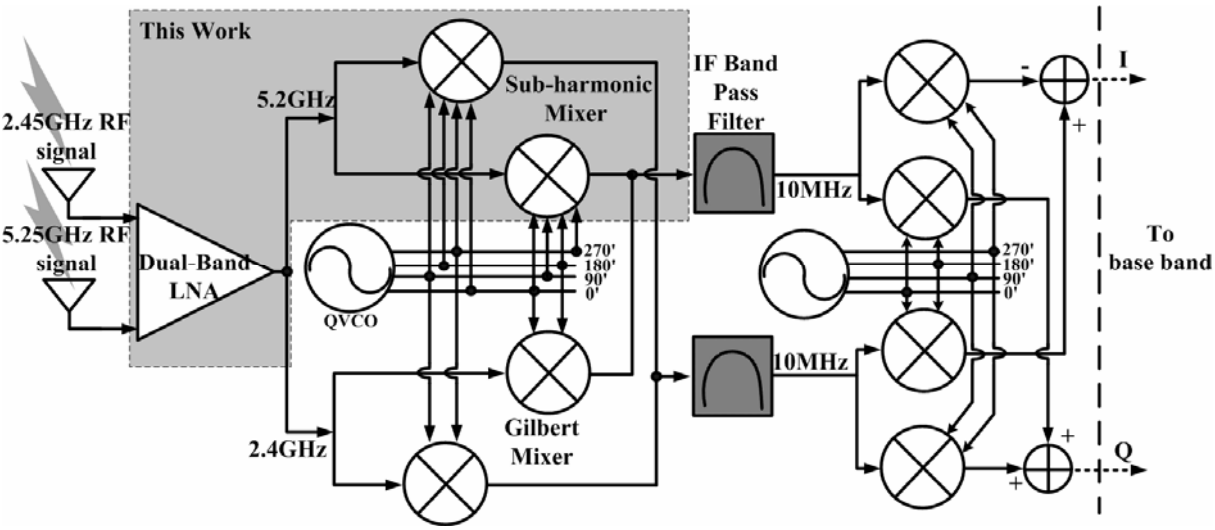


Fig. 2-3 The proposed dual-band receiver

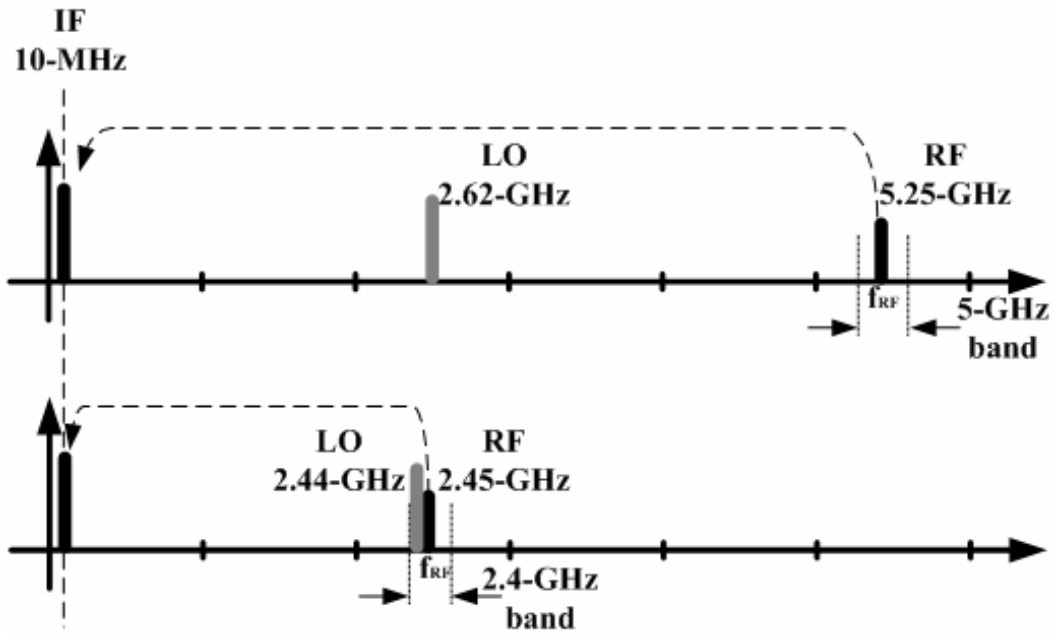


Fig. 2-4 The frequency planning in the proposed dual-band receiver

2.4.2 Switched Dual-Band LNA

A switched dual-band low noise amplifier with four gain control modes operating at the 2.45-GHz/5.25GHz has been simulated based on a 0.18-um TSMC CMOS process. This

dual-band LNA with two input channels and each tuned to 2.45-GHz and 5.25-GHz separately, by switching the output resonator inductor on /off, the input transistors are enabled / disabled for band selection. A novel gain control scheme is introduced, and this gain control scheme has low circuit complexity. The four gain control modes are executed by turning on/off the four shunted NMOS at the output of this cascode topology, and the four gain modes can be controlled digitally to adapt to the received RF signals. Comparing with the current literatures, this novel gain control scheme not only have high gain control range in both bands, but also have reasonable noise figure in the low gain mode even with 11 dB power gain lower than the high gain mode. The P_{1dB} of the proposed LNA in the low gain mode is about 11 dB higher than the one in the high gain mode in both bands. The peak of the input and output return loss is locked in band in each gain mode which is an important feature of this proposed LNA. In the high gain mode, the LNA approaches 14.4 dB maximum power gain and 3.54 dB noise figure at 2.45-GHz. In the 5.25-GHz band, the maximum power gain is 12 dB and the noise figure is 2.88 dB. The gain can be switched by about 11 dB between the high gain and the low gain mode at 2.45-GHz and 5.2-GHz. Because the switched dual-band LNA operation is similar to a single band, we discuss a single band LNA fist in Section 2.4.2.1~2.4.2.3.

2.4.2.1 *Input Matching*

For a single band LNA, the total width of the input transistor is determined by

$$W_{opt} \cong 1/(3\omega L C_{ox} R_s) \qquad (2.1)$$

where ω is the operating frequency, L is the channel length of the transistor, C_{ox} is the gate oxide capacitor and R_s is generally 50Ω [4]. In this work, the total width of the input transistor in each band is optimized to (2.1).

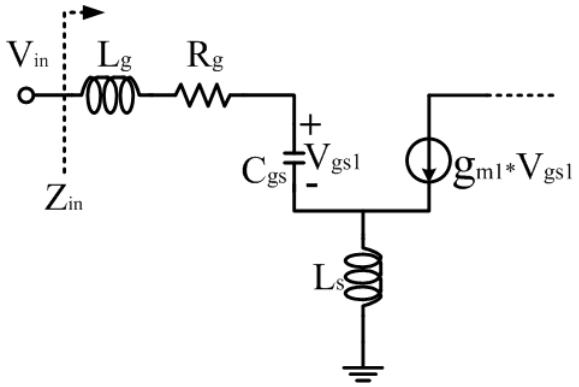


Fig. 2-5 The input stage of the single band cascade LNA

The input matching network quality factor $Q_{in} = (1/\omega_c C_{gs} R_s)$ of the LNA is a key factor which determines the power consumption, gain and noise. The following analysis is finally translated to a form with Q_{in}, and the effect of Q_{in} is clear. Analyzing the input stage of the LNA in Fig. 2-5, and the input resistance can be expressed in (2.2).

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + R_g + \frac{g_m L_s}{C_{gs}} \tag{2.2}$$

For matching condition, $Z_{in} = R_s$, reveals the input impedance and resonating frequency.

$$R_s = R_g + \frac{g_m}{C_{gs}} L_s \tag{2.3}$$

$$\omega_c = \frac{1}{\sqrt{(L_g + L_s) C_{gs}}} \tag{2.4}$$

The quality factor of the equivalent input matching network must be introduced first and it is useful in the following analysis about noise figure. As shown in Fig. 2-6, the input matching network is equal to a series RLC tank. The quality factor of the series RLC tank is (2.5) [5].

$$Q_{in} = \frac{1}{R_s}\sqrt{\frac{L_s + L_g}{C_{gs}}} = \frac{1}{R_s \omega_c C_{gs}} \tag{2.5}$$

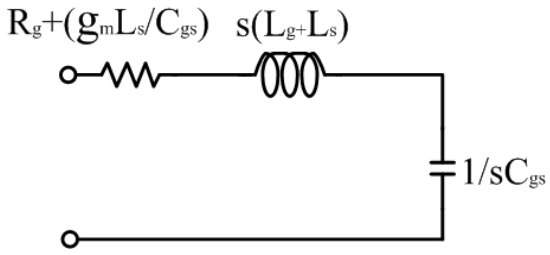


Fig. 2-6 The equivalent series RLC tank of the input matching network

2.4.2.2 *Noise Figure*

To estimate the noise figure of a cascode LNA, we take two dominate noise source for consideration. The thermal noise of the drain current from M1 and thermal noise of resistor Rg are estimated in our noise figure calculation. Fig. 2-7 shows the small signal model of the input stage, where $\overline{i_{nd}^2}$ denotes the thermal noise of the drain current from M1 and $\overline{V_{n,Rg}^2}$ denotes the thermal noise of resistor Rg. The transconductance including input matching network is G_m, and it is derived in terms of g_m, Z_{in}, ω, and C_{gs} [5].

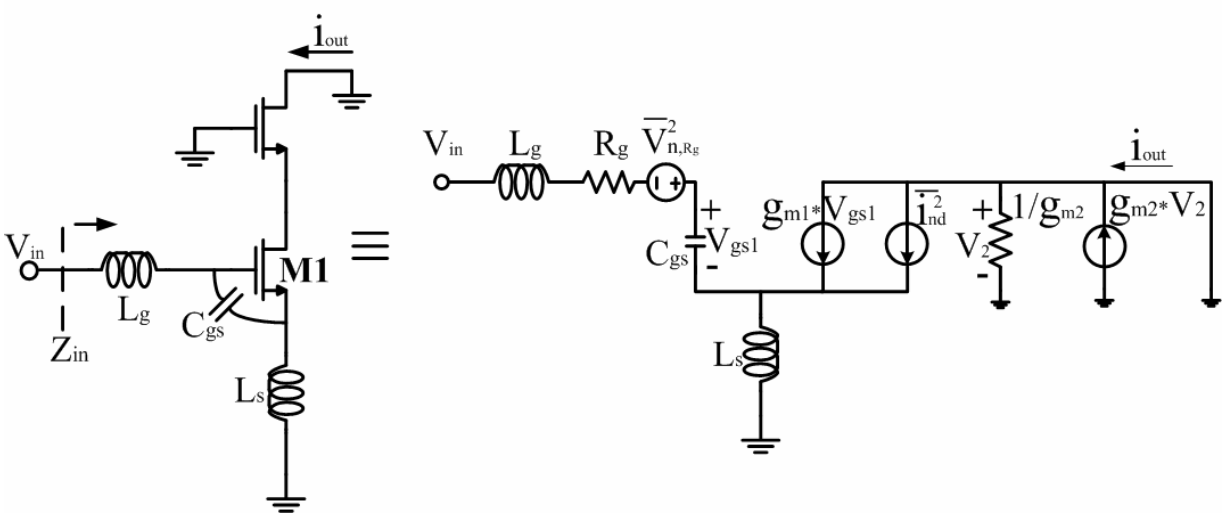


Fig. 2-7 The equivalent noise and small signal model of the input matching network

$$G_m = \frac{g_m}{Z_{in} j\omega C_{gs}} \tag{2.6}$$

At matching condition, the transconductance G_m can be rewritten as:

$$G_m = \frac{g_m}{R_s j\omega_c C_{gs}} = \frac{g_m Q_{in}}{j} \tag{2.7}$$

The input referred noise can be expressed as:

$$\overline{v_{n,referred}^2} = \frac{\overline{i_{out}^2}}{|G_m|^2} = \frac{1}{g_m^2 Q_{in}^2}\left[\frac{4kTR_g g_m^2}{R_s^2 \omega_c^2 C_{gs}^2} + 4kT\gamma g_m\right] \tag{2.8}$$

Finally, the noise figure can be derived:

$$NF = 1 + \frac{\overline{v_{n,referred}^2}}{4kTR_s} = 1 + \frac{R_g}{R_s} + \frac{\gamma}{g_m R_s Q_{in}^2} \tag{2.9}$$

where γ is the body-effect coefficient. To have an insight into the effect influenced by the quality factor of Lg, Q_{Lg} and the NF can be rewritten as:

$$Q_{Lg} = \frac{\omega_c L_g}{R_g} \tag{2.10}$$

$$NF = 1 + \frac{\omega_c L_g}{Q_{Lg} R_s} + \frac{\gamma}{g_m R_s Q_{in}^2} \tag{2.11}$$

(2.11) clearly illustrates the degradation of poor quality factor of the input inductor

2.4.2.3 *Power Dissipation*

The power dissipation is also an issue for a LNA. The power dissipation is proportional to the designed inductors Lg and Ls, which can be derived as follow:

$$P = I_D V_{DD} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 V_{DD} \propto \mu C_{ox}\frac{W}{L} \tag{2.12}$$

where W is total width of input transistor, and L is 0.18um in this work. Using the input transistor's gate-to-drain capacitance, Cgs, and (2.14), the (2.12) can be rewritten as (2.15).

$$C_{gs} = \frac{2}{3}WLC_{ox} \tag{2.13}$$

$$g_m \propto \mu C_{ox}\frac{W}{L} \tag{2.14}$$

$$P \propto \frac{g_m^2}{C_{gs}} \frac{L^2}{\mu} \tag{2.15}$$

By (2.3) and (2.4), we get

$$P \propto \frac{L^2}{\mu} \frac{(R_s - R_g)^2}{L_s^2} \frac{1}{\omega_c^2 (L_s + L_g)} = \frac{L^2}{\mu} [\frac{(R_s - R_g)}{\omega_c}]^2 \frac{1}{L_s^3 (1 + \frac{L_g}{L_s})} \tag{2.16}$$

To have an insight of the effect of Q_{in}, (2.16) is rewritten as:

$$P \propto \frac{C_{ox}^2 W^2 L^4}{\mu} (R_s - R_g)^2 R_s^2 \frac{Q_{in}^2}{L_s^3 (1 + \frac{L_g}{L_s})} \tag{2.17}$$

2.4.2.4 *The Switched Dual-Band LNA Design Consideration*

The switched dual-band LNA provides high amplification of the signals in the desired dual bands to reduce the effect of the following high noise stages and it presents low noise figure in the first stage in the receiving chain. Fig. 2-8 shows the proposed switched dual-band LNA. M1 and M2 are input transistors of the LNA. M1 is used for 2.45-GHz band, and M2 is used for 5.2-GHz band. When the LNA operates in one band, the other one is disabled by turning the corresponding input transistor off. The matching network is similar to a single band cascade LNA, and the design method is illustrated in last section. Since there are two input transistors in the dual-band LNA, the input matching network can be independently optimized for each band.

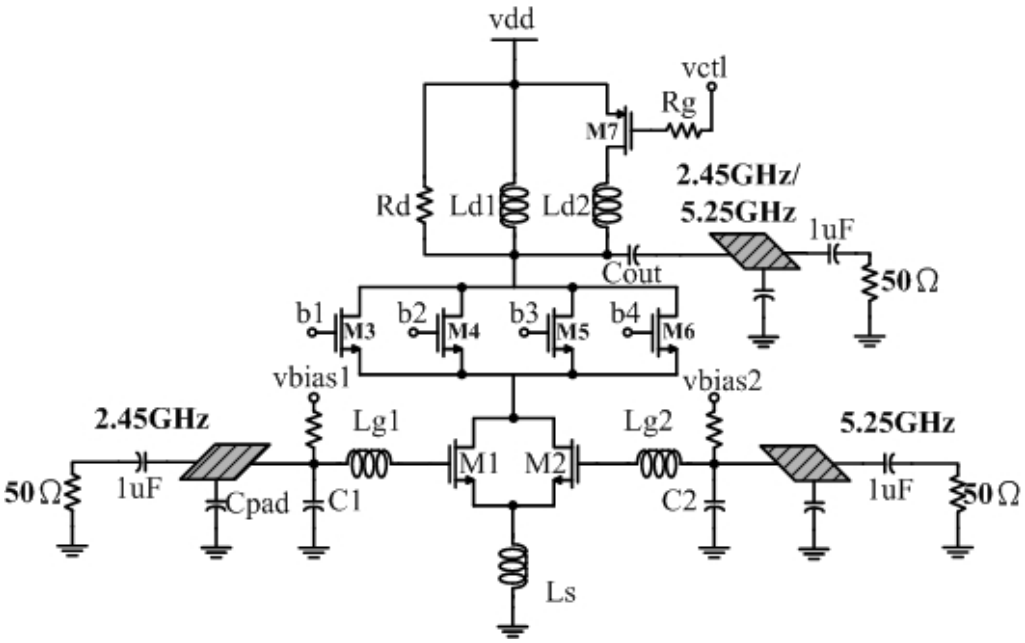


Fig. 2-8 The schematic of the proposed dual-band LNA

The switched resonator is composed of Ld1, Ld2, M7, Rg and Rd. The band selection of the LNA is performed by turning the PMOS M7 on/off. The control voltage, Vctl, applied to the PMOS M7 through a resistor Rg. Fig. 2-9 shows that when Vctl is 1.8V, and the PMOS, M7, is turned off. The Ld2 path exhibits high impedance. Thus the output resonator is dominated by Ld1 and Rd. Design Ld1 to let the output matching network resonate at 2.45-GHz. Fig. 2-10 shows that when Vctl is 0V, and M7 is turned on at triode region, and M7 exhibits its channel resistance (Ron). Thus the output resonator is dominated by Ld1 parallel with Ld2, and Ld2 is designed to keep the output matching network resonate at 5.2-GHz.

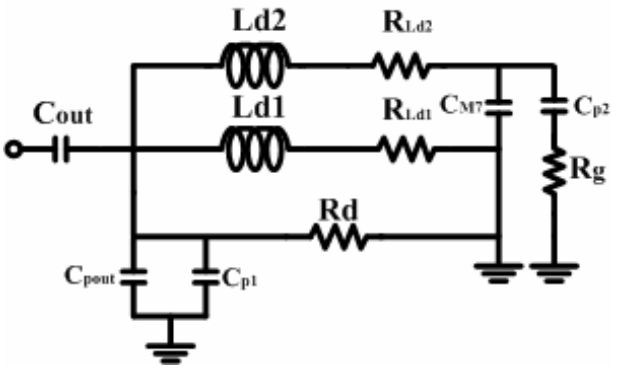


Fig. 2-9 M7 is off and the parasitic capacitance, CM7, provides a high reactance at 2.45-GHz.

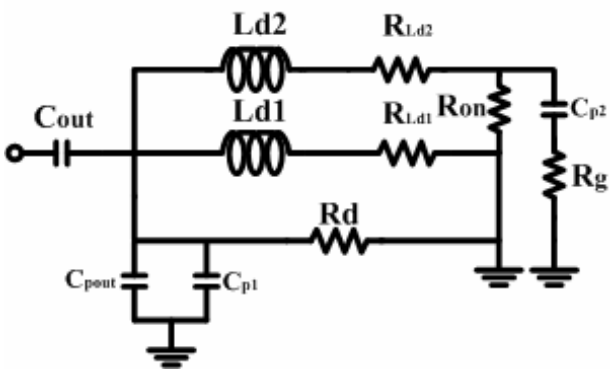


Fig. 2-10 M7 is on and provides a turn on resistance Ron at 5.25-GHz.

There exists several types of variable gain LNA solutions in the literature (e.g. [14] ~[17])： They include: i) The variance of gate bias of the common gate MOS. The gain tuning range will be limited by biasing the common gate MOS in off region and the power consumption can not be economized at low gain mode. ii) A switching control type which provides gain controllability by switching on/off active gain components. The gain control range is limited by switching the active gain components in linear region. iii) The two-stage LNA-VGA type, which achieves gain control through the use of a VGA as a second stage. This additive gain-control functionality comes at a price of higher circuit complexity, which also results in an increase in power consumption and noise degradation.

In this work, we propose a novel gain control scheme. The gain control scheme can be performed by lowering the transconductance, gm, of the input transistor. However, lowering gm definitely causes the input impedance differ from Rs and the input equivalent tank will not resonate in the desired band anymore. Therefore, a new compensation method is proposed to overcome this shortage. The cascode transistor in the traditional LNA prototype is now extended to four shunted transistors. As shown in Fig. 2-8, M3~M6 are the compensative transistors in this gain control scheme. The gain control scheme provides four gain modes to adapt to the RF signal power and behaves the best communication quality. The gain control

signals are controlled by the base band and shown in Table 3

	Vbias1	Vbias2
Mode1	0.65	0.70
Mode2	0.59	0.62
Mode3	0.55	0.55
Mode4	0.52	0.53

	b1	b2	b3	b4
Mode1	1.8	1.8	1.8	1.8
Mode2	0	1.8	1.8	1.8
Mode3	0	0	1.8	1.8
Mode4	0	0	0	1.8

Table 3 Gain control signal from base band

While the RF signal power is large enough to saturate the blocks of the receiver, the baseband will sense the failure of receiving signals and sends a control signal to the gain controllable LNA. The multiple gain modes are required for the consideration of adapting to the unpredictable RF signal power. In this work, four gain control modes are planed and the gain tuning range 11.5 dB has been measured. IIP3 is the more significant parameter to identify the gain control scheme is beneficial to the receiver. The IIP3 improvement supports the LNA to adapt to the higher power signals and preserve the following blocks from saturation. The general gain tuning range is about 10 dB and it follows 10 dB IIP3 improvement. In this project, this principle has been accomplished.

2.4.3 Switched Gm Sub-Harmonic Mixer

A new prototype of sub-harmonic mixer suitable for 5.2-GHz ISM band is designed and implemented in a standard 0.18um CMOS technology. By the PMOS active load and a switched Gm prototype at LO port, the new sub-harmonic mixer achieves high conversion gain but still remain high linearity. The fully integrated sub-harmonic mixer achieves high conversion gain of 12.8dB, -1.8 dBm IIP3, and 14.0 dB noise figure at 10-MHz with 4 dBm LO power. Moreover, the proposed sub-harmonic mixer doesn't consume dc power while there is no LO power.

2.4.3.1 *Review of The Gilbert Mixer & Sub-Harmonic Mixer*

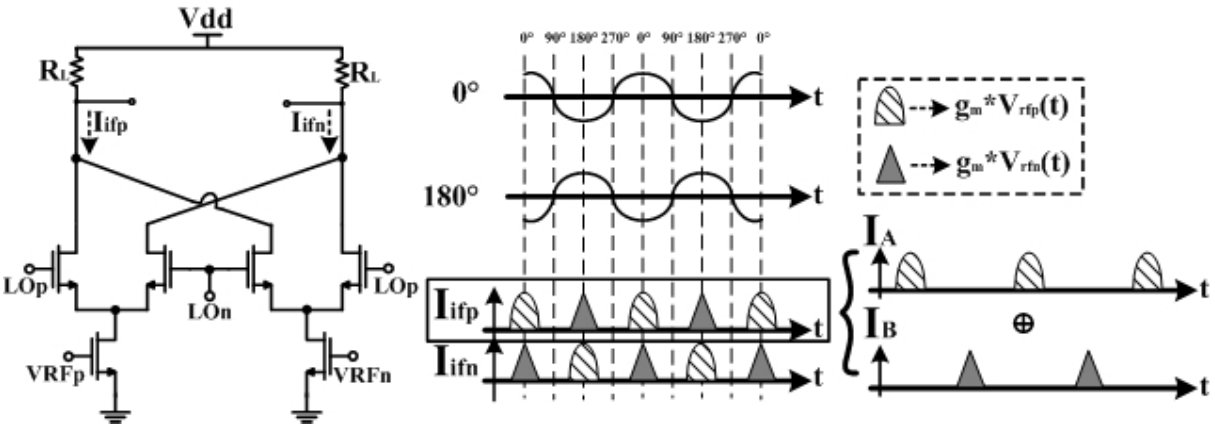


Fig. 2-11 A basic Gilbert Mixer and the waveforms of output IF current

The double balanced or Gilbert-cell mixer in Fig. 2-11 is most desirable for high port-to-port isolation and spurious output rejection applications [4]~[6]. It can provide high conversion gain and low noise figure. The linearity is reasonably good. There are many design considerations about conversion gain, linearity and noise figure for a Gilbert mixer [25]. Here we only verify that the frequency conversion is attainable. By the waveform shown in Fig. 2-11, the output IF current, I_{ifp}, can be thought of as the superposition of I_A and I_B. We can simply model the switching on/off as a square wave and the RF signal as cosine based wave with amplitude A. The down conversion principle is derived as follow:

$$\begin{aligned} I_{ifp} &= A\cos(\omega_{rf}t)[\frac{1}{2}-\frac{2}{\pi}\{\sin[\omega_{LO}t]+\frac{1}{3}\sin[3\omega_{LO}t]+\frac{1}{5}\sin[5\omega_{LO}t]+.....\}] \\ &+A\cos(\omega_{rf}t+\pi)[\frac{1}{2}-\frac{2}{\pi}\{\sin[\omega_{LO}(t+\frac{\pi}{\omega_{LO}})]+\frac{1}{3}\sin[3\omega_{LO}(t+\frac{\pi}{\omega_{LO}})]\}+\frac{1}{5}\sin[5\omega_{LO}(t+\frac{\pi}{\omega_{LO}})]+.....\}] \qquad (2.18) \\ &= -\frac{2}{\pi}A\cos(\omega_{rf}t)\{(\sin[\omega_{LO}t]-\sin[\omega_{LO}(t+\frac{\pi}{\omega_{LO}})]) \\ &\quad +\frac{1}{3}(\sin[3\omega_{LO}t]-\sin[3\omega_{LO}(t+\frac{\pi}{\omega_{LO}})]) \\ &\quad +\frac{1}{5}(\sin[5\omega_{LO}t]-\sin[5\omega_{LO}(t+\frac{\pi}{\omega_{LO}})]) \\ &\quad +.....\} \qquad (2.19) \end{aligned}$$

$$= -\frac{2}{\pi} A\cos(\omega_{rf} t)\{2\cos[\frac{2\omega_{LO} t + \pi}{2}]\sin[-\frac{\pi}{2}]$$
$$+ \frac{2}{3}\cos[\frac{6\omega_{LO} t + 3\pi}{2}]\sin[-\frac{3\pi}{2}]$$
$$+ \frac{2}{5}\cos[\frac{10\omega_{LO} t + 5\pi}{2}]\sin[-\frac{5\pi}{2}]$$
$$+ .....\} \quad (2.20)$$

$$= -\frac{2}{\pi} A\cos(\omega_{rf} t)\sum_{n=1,3,5}^{\infty}\frac{2}{n}\{\cos[n(\frac{2\omega_{LO} t + \pi}{2})]\sin[-\frac{n\pi}{2}]\} \quad (2.21)$$

$$= -\frac{4}{\pi} A\cos(\omega_{rf} t)\{-\cos[\frac{2\omega_{LO} t + \pi}{2}] + \frac{1}{3}\cos(\frac{6\omega_{LO} t + 3\pi}{2}) - \frac{1}{5}\cos(\frac{10\omega_{LO} t + 5\pi}{2}) + ...\} \quad (2.22)$$

$$= -\frac{4}{\pi} A\cos(\omega_{rf} t)\{\sin(\omega_{LO} t) + \frac{1}{3}\sin(3\omega_{LO} t) + \frac{1}{5}\sin(5\omega_{LO} t) + ...\} \quad (2.23)$$

$$= -\frac{2}{\pi} A\{(\sin[(\omega_{rf} + \omega_{LO})t] - \sin[(\omega_{rf} - \omega_{LO})t])$$
$$+ \frac{1}{3}(\sin[(\omega_{rf} + 3\omega_{LO})t] - \sin[(\omega_{rf} - 3\omega_{LO})t])$$
$$+ \frac{1}{5}(\sin[(\omega_{rf} + 5\omega_{LO})t] - \sin[(\omega_{rf} - 5\omega_{LO})t])$$
$$+ .....\} \quad (2.24)$$

$$= \sum_{n=1,3,5}^{\infty}\frac{2A}{n\pi}\{\sin[(\omega_{rf} - n\cdot\omega_{LO})t] - \sin[(\omega_{rf} + n\cdot\omega_{LO})t]\} \quad (2.25)$$

Eq. (2.25) shows the Gilbert mixer can execute frequency down conversion. The derivation demonstrated above will repeat for sub-harmonic mixer and we compare the difference of frequency translation between Gilbert mixer and sub-harmonic mixer.

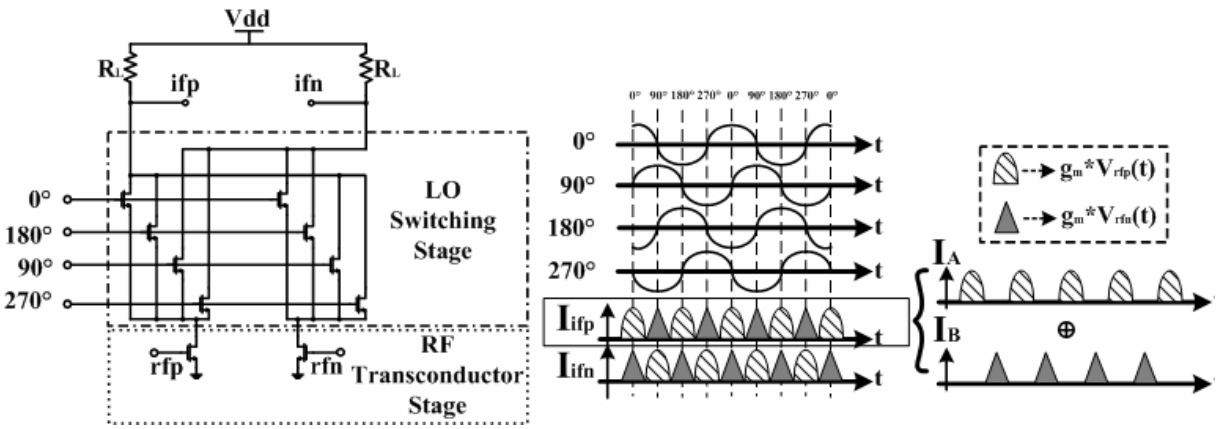


Fig. 2-12 Traditional sub-harmonic mixer and waveforms of output IF current

The sub-harmonic mixing method is originally used in microwave circuits. The method uses a LO excitation with quadrature phase operating at a fraction of RF frequency [28]. The traditional sub-harmonic mixers can be implemented based on poly-phase LO switching, however, the circuit don't have enough voltage headroom. Therefore, they aren't suitable for voltage scaling down [29]. As shown in Fig. 2-12, the gate bias of the NMOS in the LO switching stage must be biased at least 1V for IIP3 well above 0dBm of a 10dB conversion gain [27]. The conventional method of operating the switching transistors at LO port in saturation region requires significant voltage headroom, thus, reducing the head room available for the load and hence limiting the achievable conversion gain. The tradition sub-harmonic mixer is similar to the basic Gilbert mixer, but the LO switching stage is driven by a quadrature LO signal such that only half of the RF frequency is needed for LO to down convert the RF signal. The RF transconductor stage translates the voltage signal to current signal by transconductance, gm. By the waveform shown in Fig. 2-12, the output IF current, I_{ifp}, can be thought of as superposition of currents I_A and I_B. The down conversion principle of traditional sub-harmonic mixer is derived as follow:

$$I_{rfp} = A\cos(\omega_{rf}t)[\frac{1}{2} - \frac{2}{\pi}\{\sin[2\omega_{LO}t] + \frac{1}{3}\sin[6\omega_{LO}t] + \frac{1}{5}\sin[10\omega_{LO}t] + ...\}]$$

$$+A\cos(\omega_{rf}t+\pi)[\frac{1}{2}-\frac{2}{\pi}\{\sin[2\omega_{LO}(t+\frac{\pi}{2\omega_{LO}})]+\frac{1}{3}\sin[6\omega_{LO}(t+\frac{\pi}{2\omega_{LO}})]+\frac{1}{5}\sin[10\omega_{LO}(t+\frac{\pi}{2\omega_{LO}})]+.....\}] \quad (2.26)$$

$$=-\frac{2}{\pi}A\cos(\omega_{rf}t)\{(\sin[2\omega_{LO}t]-\sin[2\omega_{LO}(t+\frac{\pi}{2\omega_{LO}})])$$
$$+\frac{1}{3}(\sin[6\omega_{LO}t]-\sin[6\omega_{LO}(t+\frac{\pi}{2\omega_{LO}})])$$
$$+\frac{1}{5}(\sin[10\omega_{LO}t]-\sin[10\omega_{LO}(t+\frac{\pi}{2\omega_{LO}})])$$
$$+.....\} \quad (2.27)$$

$$=-\frac{2}{\pi}A\cos(\omega_{rf}t)\{2\cos[\frac{4\omega_{LO}t+\pi}{2}]\sin[-\frac{\pi}{2}]$$
$$+\frac{2}{3}\cos[\frac{12\omega_{LO}t+3\pi}{2}]\sin[-\frac{3\pi}{2}]$$
$$+\frac{2}{5}\cos[\frac{20\omega_{LO}t+5\pi}{2}]\sin[-\frac{5\pi}{2}]$$
$$+.....\} \quad (2.28)$$

$$=-\frac{4}{\pi}A\cos(\omega_{rf}t)\{-\cos[\frac{4\omega_{LO}t+\pi}{2}]+\frac{1}{3}\cos(\frac{12\omega_{LO}t+3\pi}{2})-\frac{1}{5}\cos(\frac{20\omega_{LO}t+5\pi}{2})+.....\} \quad (2.29)$$

$$=-\frac{4}{\pi}A\cos(\omega_{rf}t)\{\sin(2\omega_{LO}t)+\frac{1}{3}\sin(6\omega_{LO}t)+\frac{1}{5}\sin(10\omega_{LO}t)+.....\} \quad (2.30)$$

$$=-\frac{2}{\pi}A\{(\sin[(\omega_{rf}+2\omega_{LO})t]-\sin[(\omega_{rf}-2\omega_{LO})t])$$
$$+\frac{1}{3}(\sin[(\omega_{rf}+6\omega_{LO})t]-\sin[(\omega_{rf}-6\omega_{LO})t])$$
$$+\frac{1}{5}(\sin[(\omega_{rf}+10\omega_{LO})t]-\sin[(\omega_{rf}-10\omega_{LO})t])$$
$$+.....\} \quad (2.31)$$

$$=\sum_{n=1,3,5}^{\infty}\frac{2A}{n\pi}\{\sin[(\omega_{rf}-2n\cdot\omega_{LO})t]-\sin[(\omega_{rf}+2n\cdot\omega_{LO})t]\} \quad (2.32)$$

The down conversion principle can be understood distinctly by the derivated results. Comparing (2.32) with (2.25), the RF frequencies are down converted by a fundamental LO frequency and a 2nd harmonic LO one for Gilbert mixer and sub-harmonic mixer, respectively. By the derivation illustrated above, the operation of Gilbert mixer and sub-harmonic mixer

are understood and the new proposed switched Gm sub-harmonic mixer will be identified as the same operation.

2.4.3.2 *Switched Gm Mixer*

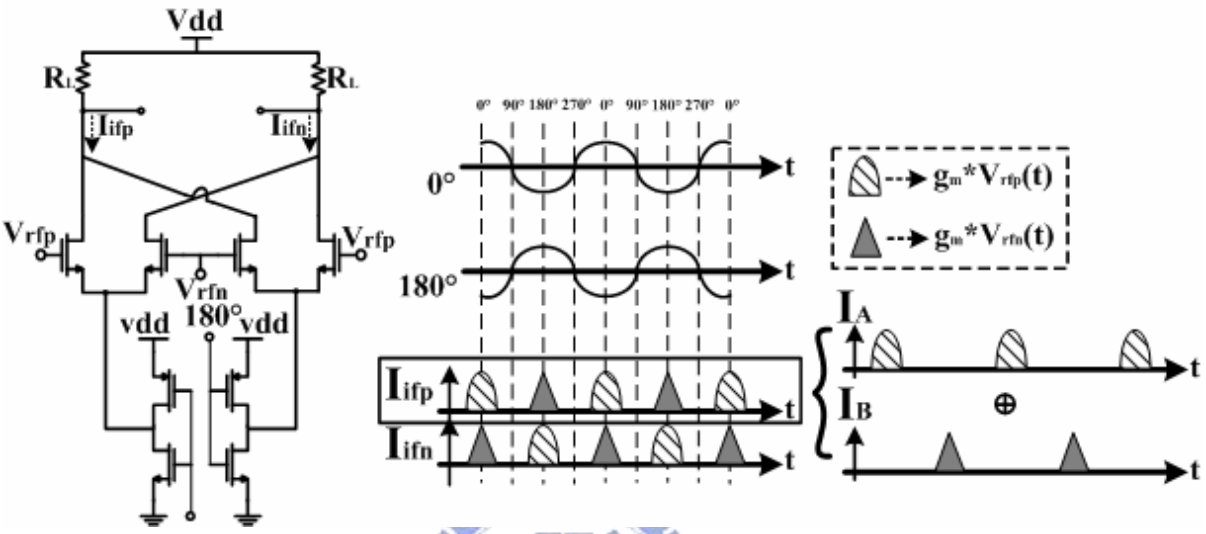


Fig. 2-13 Switched Gm mixer and the waveforms of IF output current

The switched Gm mixer was first published in 2003 [26]. Because only switches with a conductive channel connected to either Vss or Vdd are used, it requires almost no voltage headroom across the switch and does not require gate-drive voltages outside the supply rails. As a result, the gate-oxide stress of the switch devices is low, as desired for reliability concern. Even if oxide reliability is no issue, the conventional method of operating the switch transistors M2 and M3 in saturation requires significant voltage headroom, reducing the headroom available for the load and hence limiting the achievable conversion gain. By using low ohmic switches with a low-voltage drop compared to Vdd, almost the full supply voltage headroom can be reserved for the transconductance device and load, allowing for more conversion gain. By the time domain IF current plotting in Fig. 2-13, the same down conversion principle can be derived as (2.25). And the differential conversion gain can be obtained by multiplying $2g_mR_L$ to (2.25), that is:

$$CG = \frac{4}{\pi} g_m R_L \tag{2.33}$$

2.4.3.3 *Proposed New Sub-Harmonic Mixer*

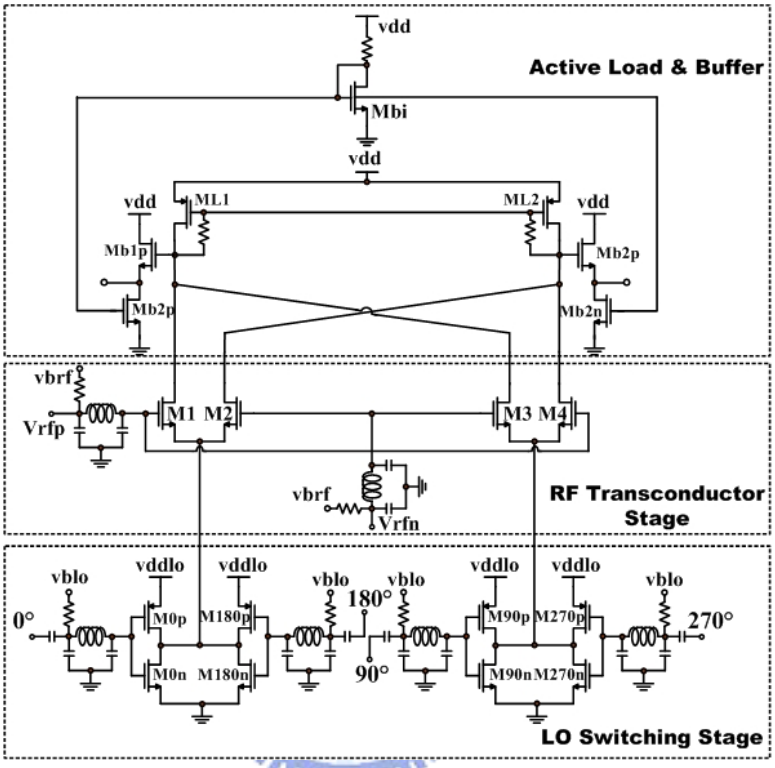


Fig. 2-14 Proposed switched Gm sub-harmonic mixer

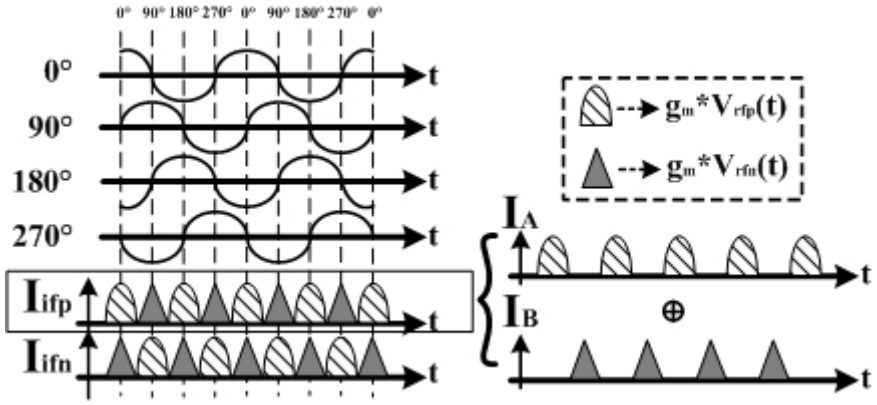


Fig. 2-15 Waveform of the switched Gm sub-harmonic mixer

In this work, we combine a switched Gm technique at LO switching stage and a PMOS active load to implement a new sub-harmonic mixer that we can alleviate the shortage of the

voltage headroom at IF output [4]. Fig. 2-14 shows the topology of the new switched Gm sub-harmonic mixer. There are four inverters in the LO switching stage which are driven by a quadratue LO signal. Therefore, no power is consumed for this mixer while there is no LO input. Only one of the inverters can be activated to let either source of M1 and M2 or source of M3 and M4 be at low voltage.

By the same derivation as illustrated in the sub-harmonic mixer, the new sub-harmonic mixer has the same down conversion principle and it can be derived as follow:

$$I_{ifp} = A\cos(\omega_{rf}t)[\frac{1}{2} - \sum_{n=1,3,5...}^{\infty} \frac{2}{n\pi}\sin(2n\omega_{LO}t)]$$

$$+ A\cos(\omega_{rf}t + \pi)\{\frac{1}{2} - \sum_{n=1,3,5...}^{\infty} \frac{2}{n\pi}\sin[2n\omega_{LO}(t + \frac{\pi}{2})]\} \quad (2.34)$$

$$= \sum_{n=1,3,5}^{\infty} \frac{4A}{n\pi}\cos(\omega_{rf}t)\{\cos[n(\frac{4\omega_{LO}t + \pi}{2})]\sin[\frac{n\pi}{2}]\} \quad (2.35)$$

$$= \sum_{n=1,3,5}^{\infty} \frac{2A}{n\pi}\{\sin[(\omega_{rf} - 2n\cdot\omega_{LO})t] - \sin[(\omega_{rf} + 2n\cdot\omega_{LO})t]\} \quad (2.36)$$

Also the output IF current, I_{ifp}, can be derived in the same skill. And we can verify that the maximum differential conversion gain of the new sub-harmonic mixer is

$$CG = \frac{4}{\pi} g_m R_L \quad (2.37)$$

However, the advantage of the sufficient voltage headroom at IF ports support the achievable conversion gain and keeps the mixer exhibits high linearity.

In (2.36), we can clearly identify that the proposed sub-harmonic mixer can down convert RF signal by operating the LO signal at half of the RF frequency. The maximum differential conversion gain is identical with the conventional one, but the noise and linearity is not the same case as illustrated in [27]. To acquire more conversion gain and keep the voltage head room sufficient, the PMOS active load is applied to the new sub-harmonic mixer. For measurement consideration, there are π matching networks in front of each RF and LO

signals. And a source follower is acted as the output buffer for the 50Ω system.

The finite ON-resistance of the switches may reduce the linearity and conversion gain of the switched Gm mixer, and this undesired effect must be estimated. We can model the switch with a finite ON-resistance, R_{on}, and it "allows" for source voltage variation. This voltage can mix with the RF signal at the gate via the second-order term of the MOSFET, resulting in a differential output current:

$$i_{out} = g_1 v_{RF} + (\frac{g_3}{4} - \frac{g_2^2 R_{on}}{1+2g_1 R_{on}})v_{RF}^3 \qquad (2.38)$$

where g_1, g_2, and g_3 are the Taylor series coefficients derived by taking the derivative of $I_d(V_{gs})$ of the transconductor MOSFET. If the switch resistance is significantly lower than $1/g_1$, the linearity can be better [27].

2.5 Measurement Consideration and Results

2.5.1 Switched Dual-Band LNA

2.5.1.1 *Measurement Consideration*

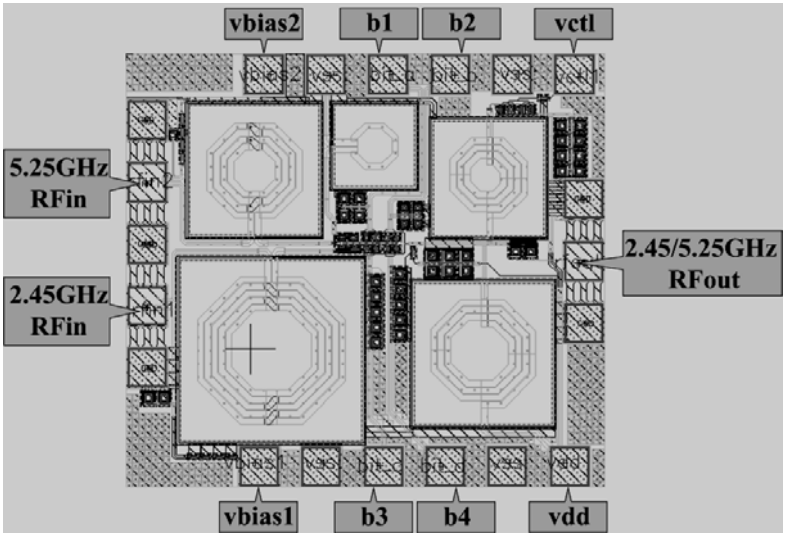


Fig. 2-16 The layout of the proposed switched dual-band LNA

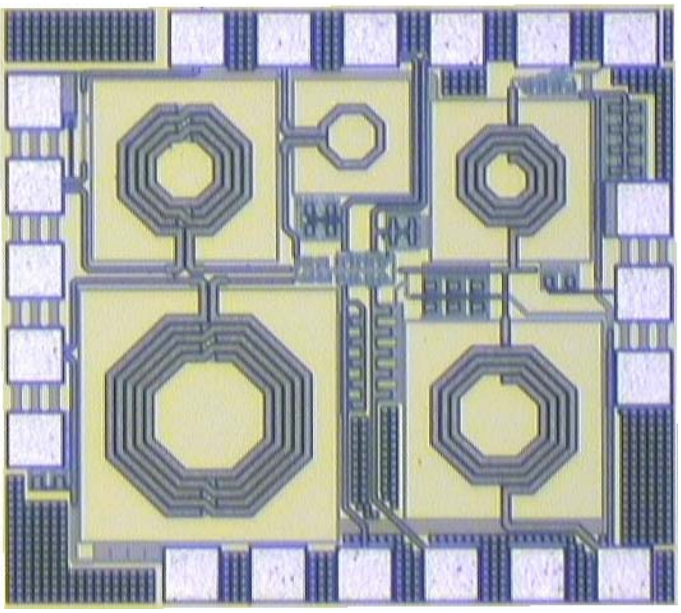
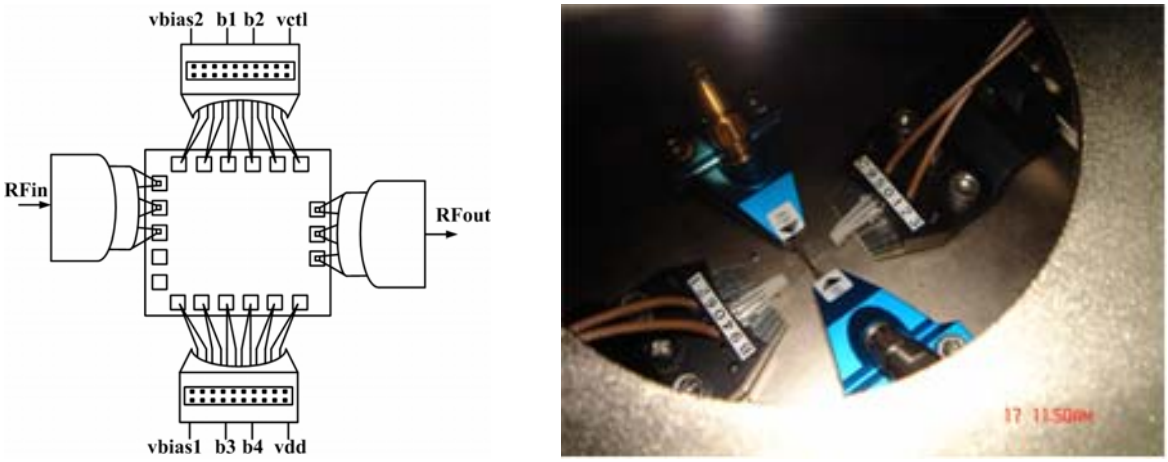


Fig. 2-17 The micrographic of the proposed switched dual-band LNA

The switched dual band LNA is designed for fully on-wafer measurement, therefore the arrangement of each pad must satisfy the probe station testing rules. By the layout shown in Fig. 2-16, two six-pin dc probes are required to feed with eight dc voltages. In addition, two RF probes are also needed for RF signals. Fig. 2-18 (a~b) shows the arrangement for dc and RF probes. The top and bottom are six-pin dc probes, while the left side is GSG RF probes for RF signal input and the right side is GSG RF probes for RF signal output.

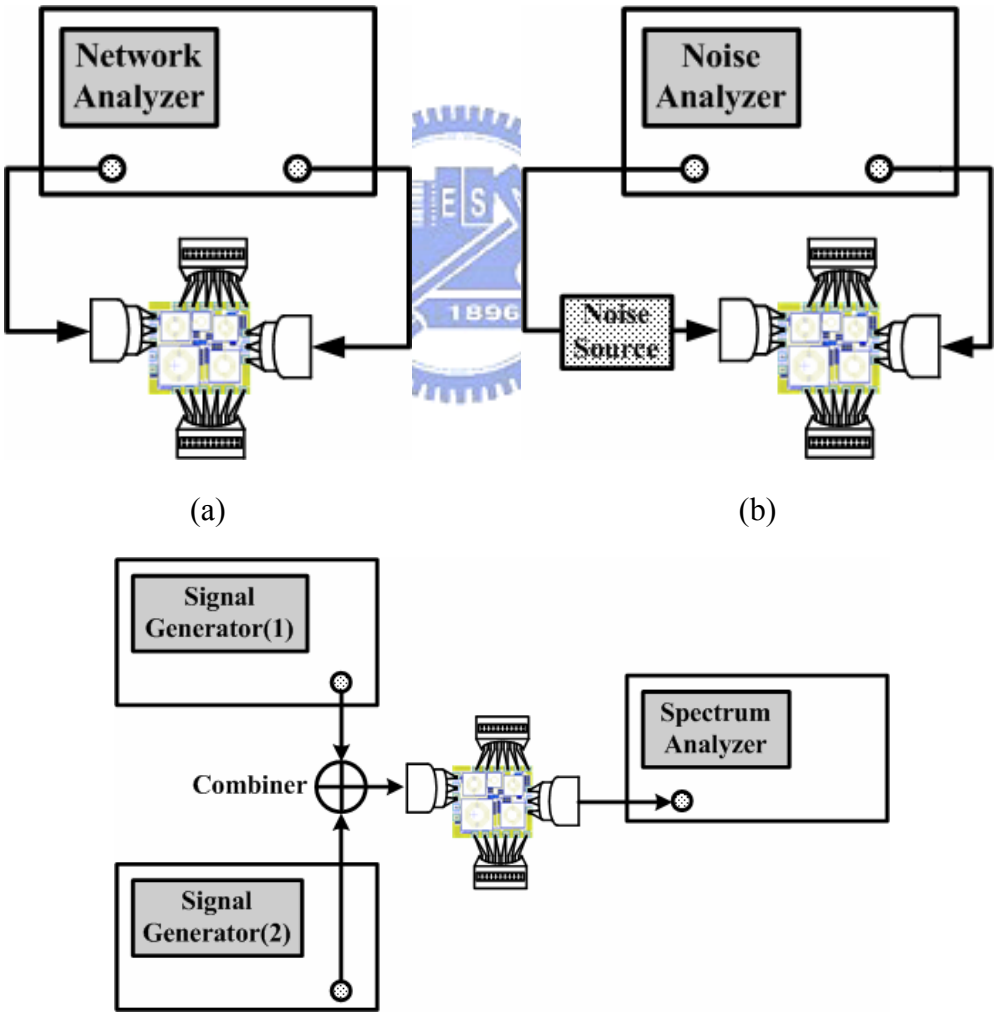
The measurement equipments include a network analyzer (HP8510C), a noise analyzer (Agilent N8975A), a spectrum analyzer (Agilent E4407B), three signal generators, and several dc power supplies. Several auxiliary equipments are also required for the measurement setup, such as cables, 50Ω terminals, and power combiners. The losses of cables, combiners, and Baluns are all needed to be considered for calibration.

The S-parameter, noise figure, 1-dB compression point, IIP3 are needed to measure to verifying the switched dual-band LNA performance, and the measurement setups for each parameters are shown in Fig. 2-19 (a~c). We will show and discuss the measured results for each parameter.



(a) (b)

Fig. 2-18 (a) On-wafer measurement test diagram(b) The photo for measurement environment



(a) (b)

(c)

Fig. 2-19 Measurement setups for (a)S-parameter (b) noise figure (c)IIP3 and P1dB

2.5.1.2 *Measurement Results and Discussion of Dual-Band LNA*

As shown in Fig. 2-20 to Fig. 2-23, the S-parameter of the four gain modes are “locked” in band and this is a benefit for a narrowband system such as 802.11a/b/g. For high gain mode, the measured S-parameter reveals 14.40 dB and 12.02 dB power gain, -12.18 dB and -11.02 dB input return loss, -6.73 dB and -12.09 dB output return loss, and -38.73 dB and -28.64 dB reverse isolation at 2.45-GHz and 5.25-GHz, respectively. For low gain mode, the power gain reduces to 3 dB and 0.18 dB at 2.45-GHz and 5.25-GHz, respectively.

The noise figure increases as the power gain switching form high gain mode to low gain mode. The measured noise figures for high gain mode are 3.54 dB and 2.88 dB at 2.45-GHz and 5.25-GHz, respectively. For low gain mode, the noise figure behaves 5.62 dB and 5.5 dB for 2.45-GHz and 5.25-GHz, respectively. The noise figure increments between high gain mode and low gain mode are 2.08 dB and 2.62 dB for 2.4-GHz and 5.2-GHz band, respectively. The noise figure increment is as expected even with about 11 dB gain tuning.

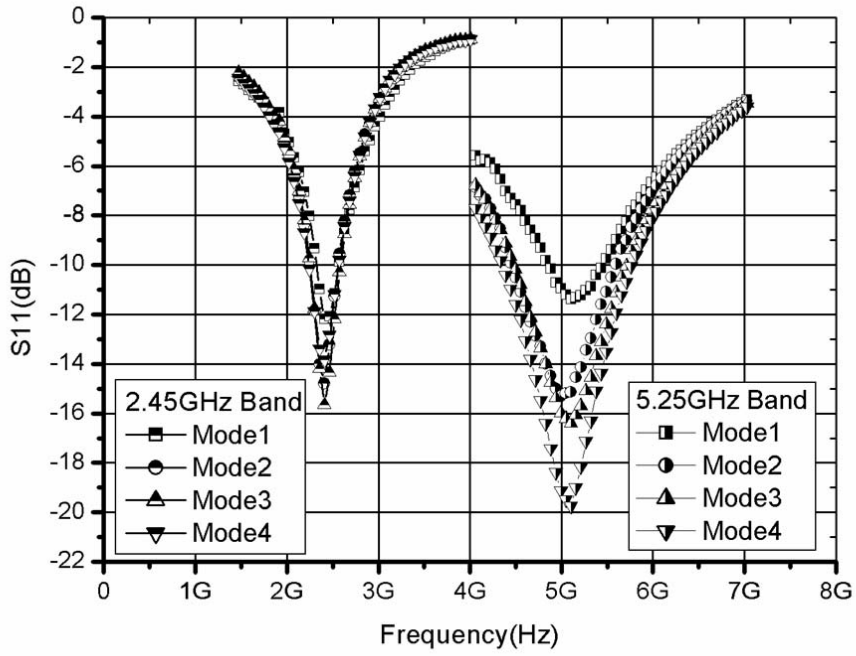


Fig. 2-20 The measured S11 of the proposed switched dual-band LNA

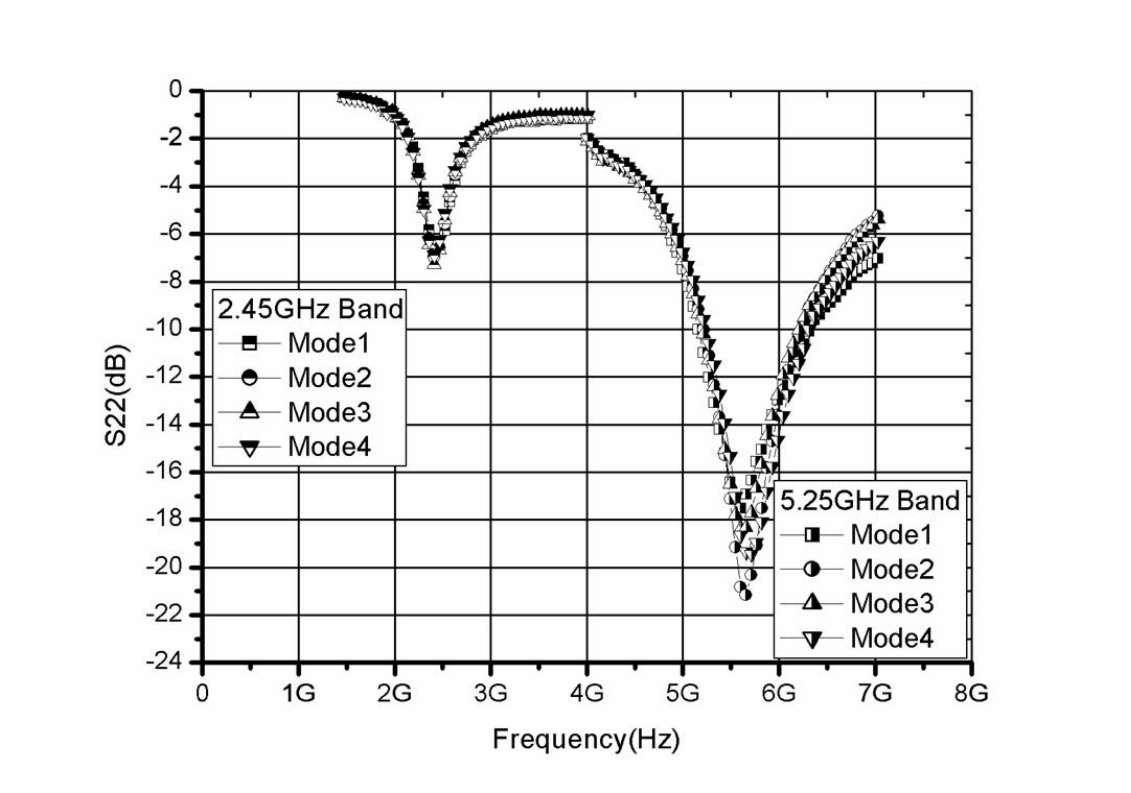


Fig. 2-21 The measured S22 of the proposed switched dual-band LNA

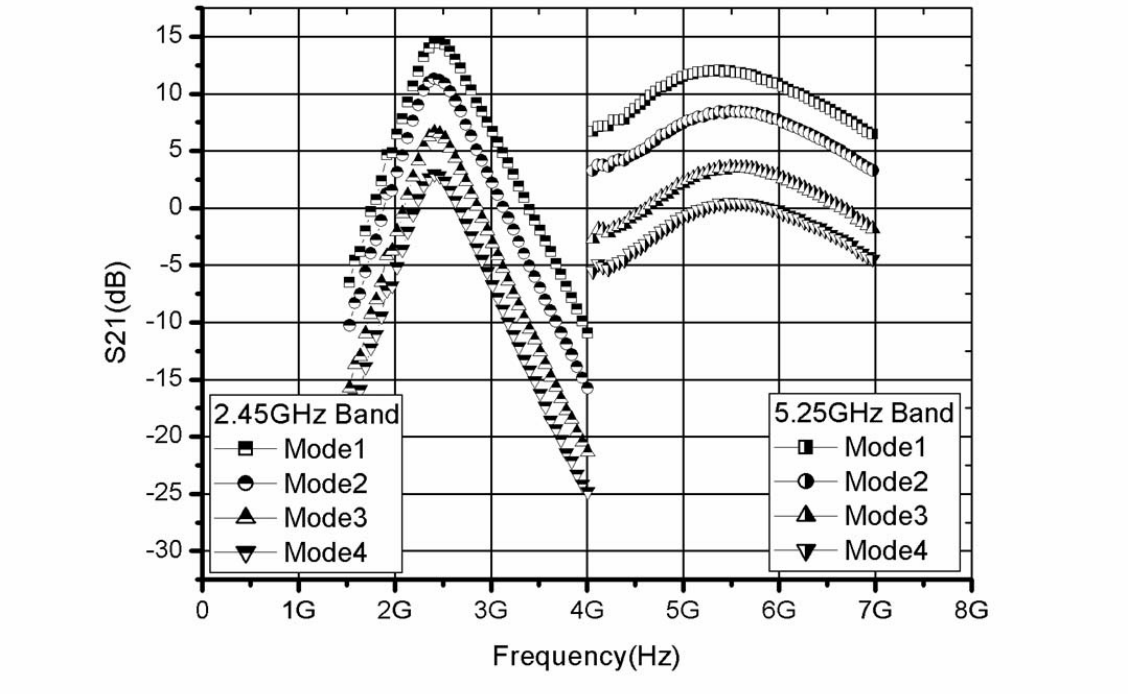


Fig. 2-22 The measured S21 of the proposed switched dual-band LNA

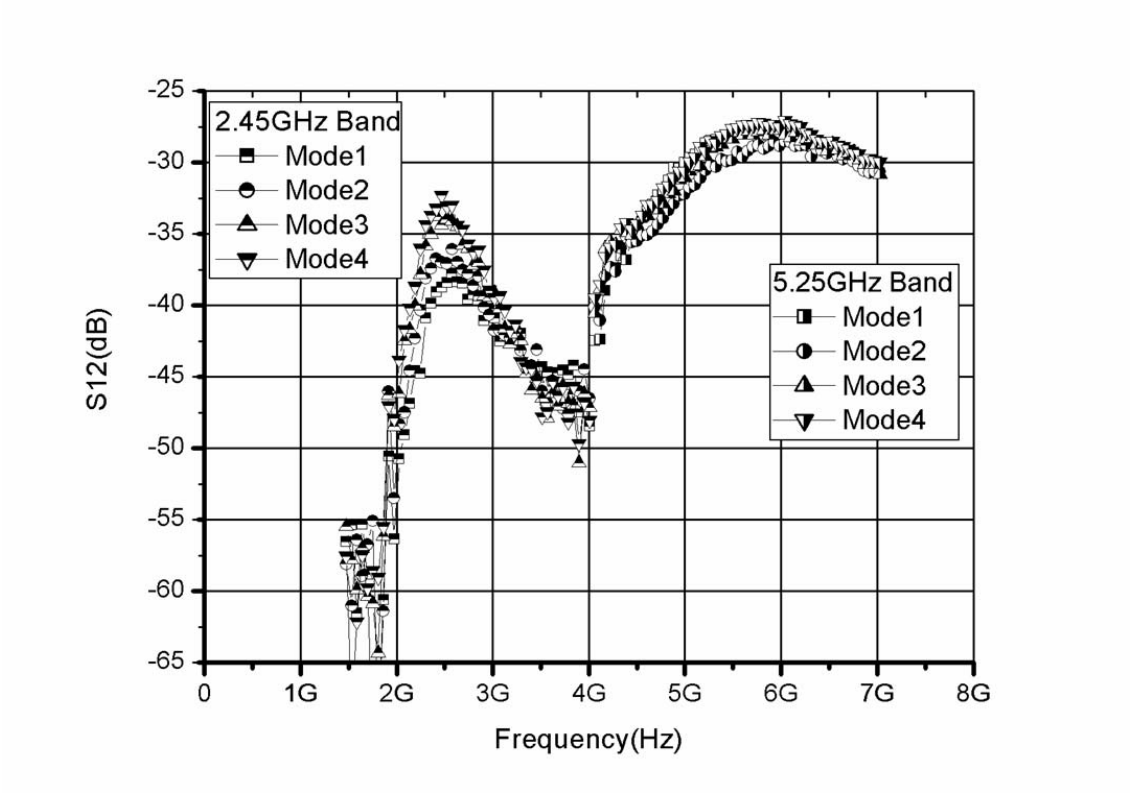


Fig. 2-23 The measured S12 of the proposed switched dual-band LNA

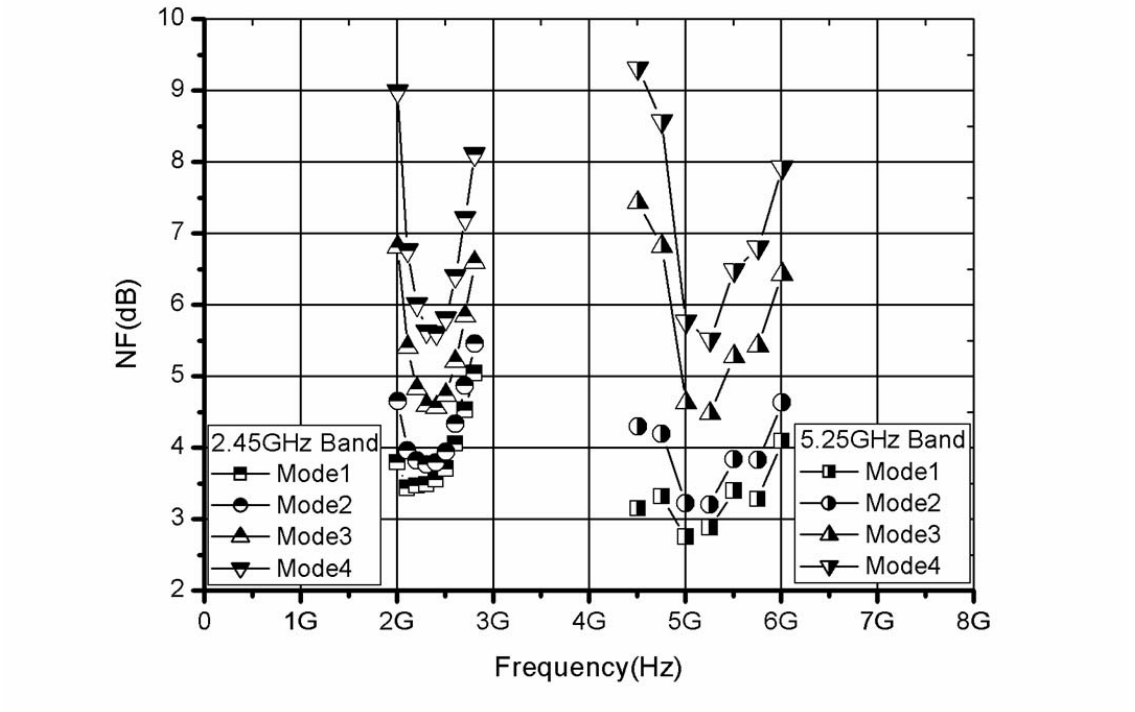


Fig. 2-24 The measured NF of the proposed switched dual-band LNA

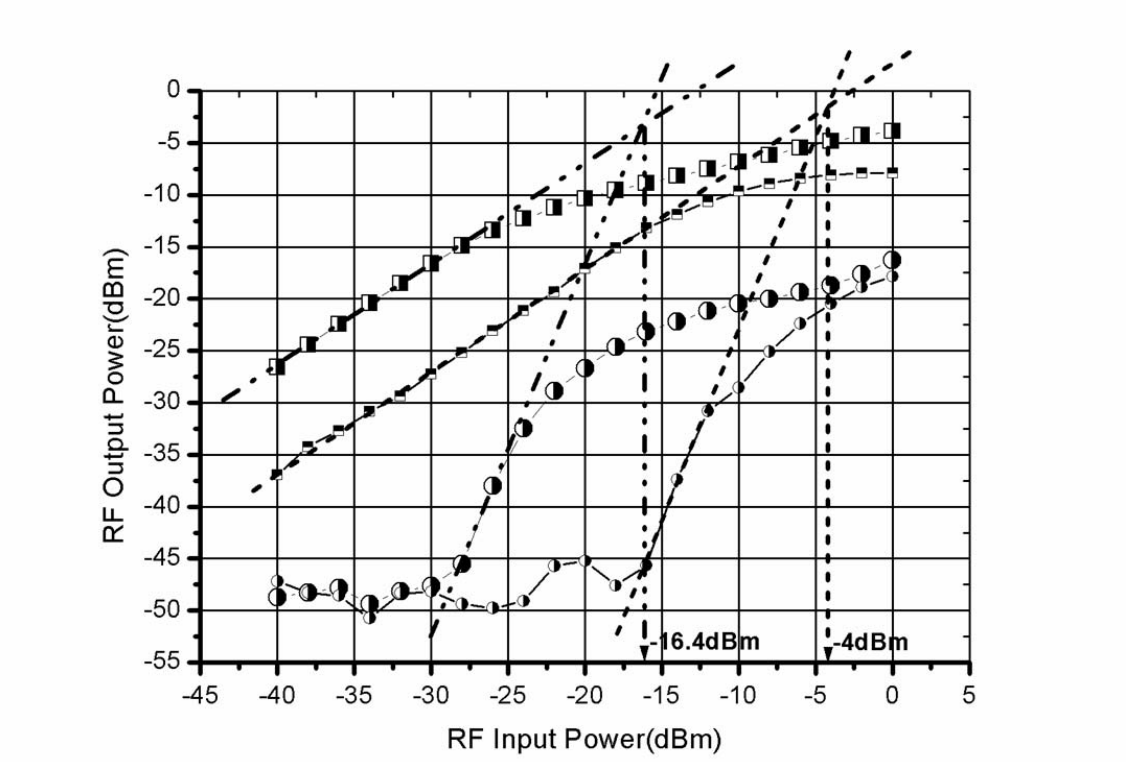


Fig. 2-25 The measured IIP3 at 2.4-GHz band of the proposed switched dual-band LNA

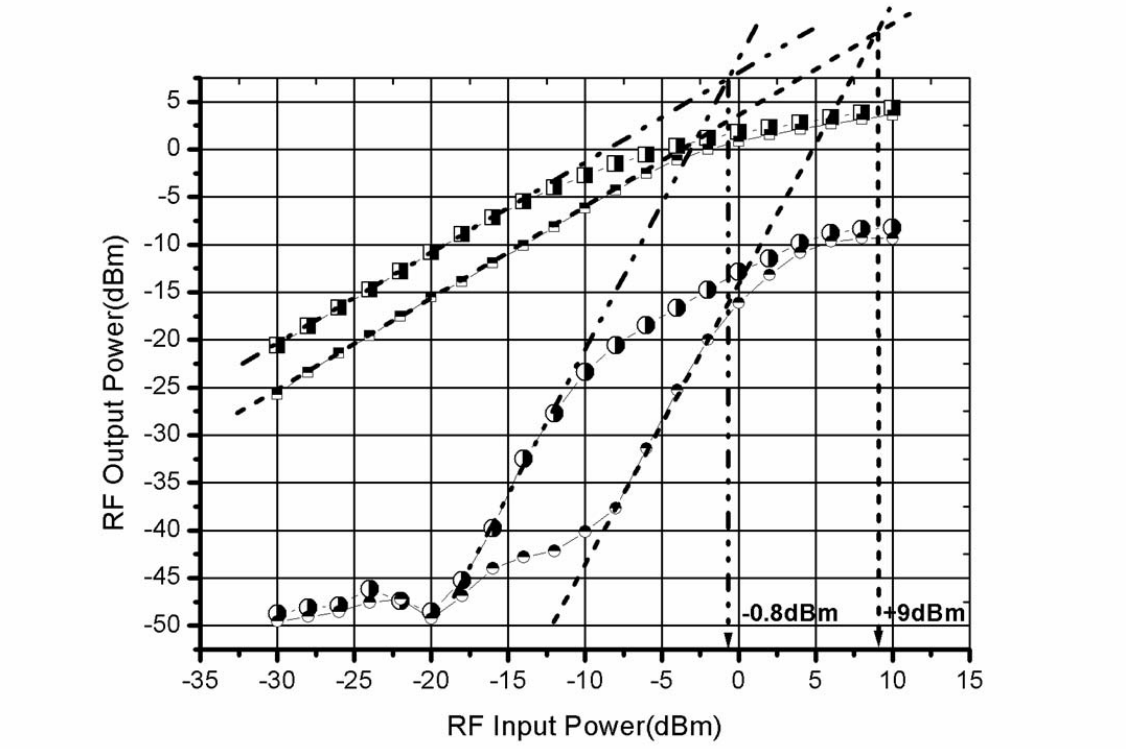


Fig. 2-26 The measured IIP3 at 5.2-GHz band of the proposed switched dual-band LNA

There are four gain modes for the proposed switched dual-band LNA, and the linearity improvement to adapting the higher input power must be considered. In the 5.2-GHz band, the measured IIP3 of the high gain mode is -16.4 dBm, and -4 dBm for low gain mode. A linearity improvement of 12.4 dB is achieved at 2.4-GHz band. On the other hand, the measured IIP3 of high gain mode and low gain mode in 5.2-GHz band are -0.8 dBm and 9 dBm, respectively. A linearity improvement of 9.8 dB is achieved in 5.2-GHz band.

2.5.1.3 *Comparison with Other Literatures*

This work combines two topics including switched dual-band and gain control ability, however, the published literatures discuss either dual-band or gain control ability. Hence, we compare these two topics independently, and comparison with dual-band LNA and gain controllable LNA are shown in Table 4 and Table 5, respectively.

	Process	Center Frequency	Vdd	S11/ S22(dB)	S21(dB)	NF (dB)	IIP3(low gain) -IIP3(high gain)	Power dispassion
This Work	**CMOS 0.18um**	**2.45GHz**	**1.8V**	**-12.18 / -6.73**	**14.4**	**3.54**	**12.4dB**	**9.42mA**
		5.25GHz		**-11.02 / -12.09**	**12.02**	**2.88**	**9.8dB**	**10.12mA**
[7]2005 MWCL	CMOS 0.18um	2.4GHz	1.8V	-10.1 / -10.5	10.1	2.9	N/A	6.5mA
		5.2GHz		-11.0 / -17.0	10.9	3.7		3.17mA
[8]2003 ISCAS	CMOS 0.18um	2.4GHz	1V/ 0.7V	-5.1 / N/A	11.6@1V 8.5@0.7V	2.3	N/A	14.2mA @1V 6.2mA @0.7V
		5GHz		-26.3 / N/A	10.8@1V 5.5@0.7V	2.9	N/A	
[9]2004	CMOS 0.18um	2.44GHz	1.8V	N/A	7.6	5.7	N/A	6mA
		5.76GHz		N/A	8.6	6.8		

Table 4 The comparison with published dual-band LNA

In dual-band LNA comparison, this work achieves highest power gain and performs good

noise figure at high gain mode in 5.25-GHz band although the power consumption is the highest. However, the power consumption of this work is endurable in IEEE 802.11 a/b/g application.

	This Work (Meas.)		[21]2005 IEE EL (Meas.)	[22]2003 MWCL (Meas.)	[23]2003 RFIC (Meas.)
Process	**CMOS 0.18um**		CMOS 0.18um	CMOS 0.18um	CMOS 0.18um
Center Frequency	**2.45GHz**	**5.25GHz**	5.7 GHz	5.7 GHz	5.75GHz
Vdd	**1.8V**		1V	1.8V	1.8V
S11/S22 (dB)	**-12.18/-6.73**	**-11.02/-12.09**	-11.0 / -15.0	-15.0 / -9.0	>7 / N/A
S21 (dB)	**14.4**	**12.02**	16.4	12.5	21.4
NF (dB)	**3.54**	**2.88**	3.5	3.7	4.4
NF(high gain) -NF(low gain)	**2.08 dB**	**2.62 dB**	2.5 dB	1.8dB	N/A
Gain Tuning	**11.4 dB**	**11.85 dB**	8 dB	8.9	10.6
IIP3(high gain) -IIP3(low gain)	**12.4 dB**	**9.8 dB**	N/A	N/A	12dB
Power Dispassion	**9.42mA**	**10.12mA**	3.2mA	8mA	9mA

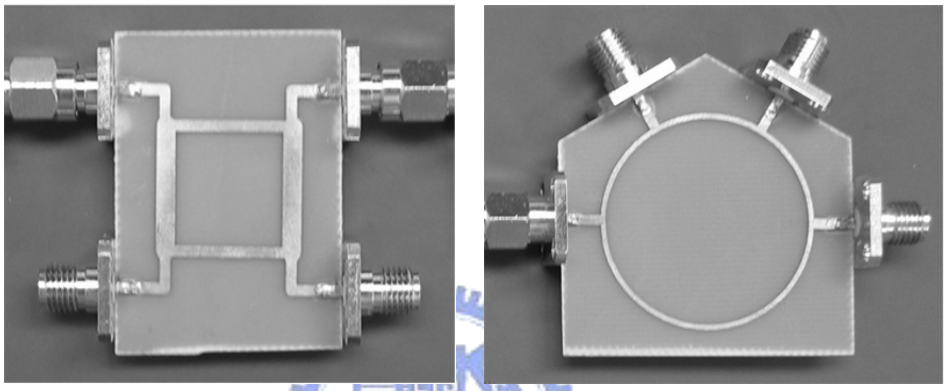
Table 5 The comparison with the published gain controllable LNA

In gain controllable LNA comparison, highest gain tuning range is presented in Table 5. The noise figure of this work in 5.25-GHz band is the lowest and linearity improvement is as expected while operating in low gain mode.

2.5.2 Switched Gm Sub-Harmonic Mixer

2.5.2.1 *Measurement Consideration*

The proposed sub-harmonic mixer is designed to down convert the 5.25-GHz differential signal, thus a Balun for 5.25-GHz is required to translate the RF signal into a differential signals. We use a Balun offered by CIC, and the Balun can operate at 5.25-GHz.



(a) (b)

Fig. 2-27 (a) The LO port quadrature hybrid (b) The LO port rat-race

In addition, a quadrature 2.62-GHz signal is also necessary for the measurement of the sub-harmonic mixer. The method we adopt here is combining a quadrature hybrid shown in Fig. 2-27 (a) with two rat-races shown in Fig. 2-27 (b). Ideally the [S] matrix for the quadrature hybrid has the following form:

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{2.39}$$

To realize the operation of the four port device, we excite a unit of signal with desired frequency into port1 of the quadrature hybrid and else ports are terminated by 50Ω. The signal power will be evenly divided between port2 and port3, and a phase shift of 90° appears between these two ports. There is no power coupled to port4, and it is the isolation port. The

quadrature signal required in this project is accomplished by a quadrature hybrid and two rat-races illustrated above. The quadrature signals are connected to the LO switching stage shown in Fig. 2-14. We use the two ports vector network analyzer to identify the 90° phase shift of the fabricated quadrature Balun. Each ports are terminated by a 50Ω load except the measuring two ports. Fig. 2-28 shows the fabricated quadrature Balun and we measure its S_{21}, S_{31}, S_{41}, S_{51} to verify 90° phase shift between port2 and port4. Furthermore, there should be 180° phase shift between port2 (port4) and port3 (port5). The measured forward transmitted S-parameters for the quadrature balun are listed below:

$S_{21} = 0.440\angle -53.379°$
$S_{31} = 0.438\angle 126.677°$
$S_{41} = 0.450\angle -146.00°$
$S_{51} = 0.449\angle 36.811°$

Table 6 The measured forward transmitted S-parameter for each port

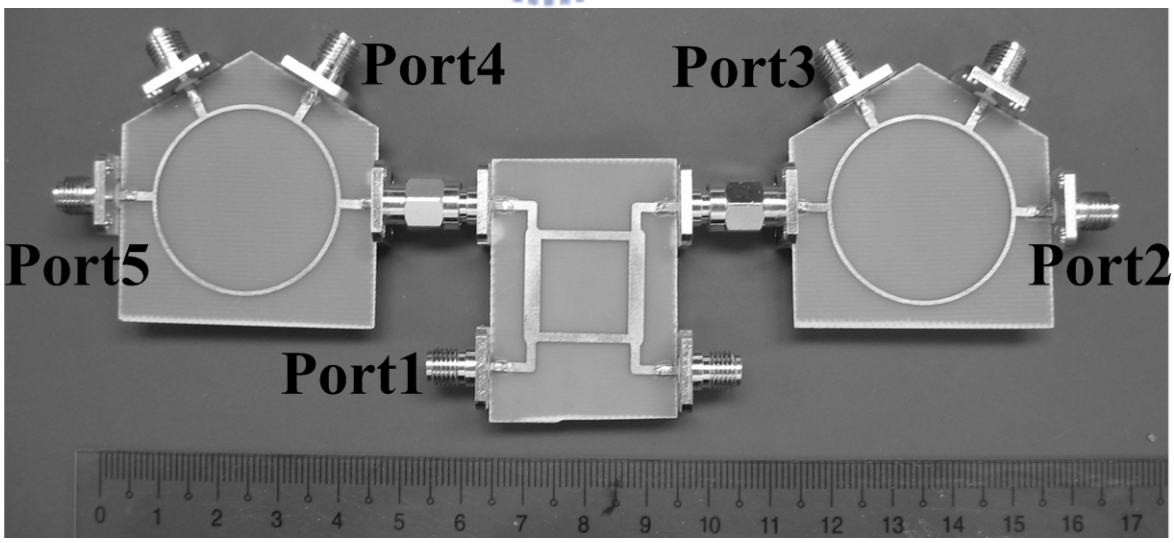


Fig. 2-28 The fabricated LO port quadrature Balun

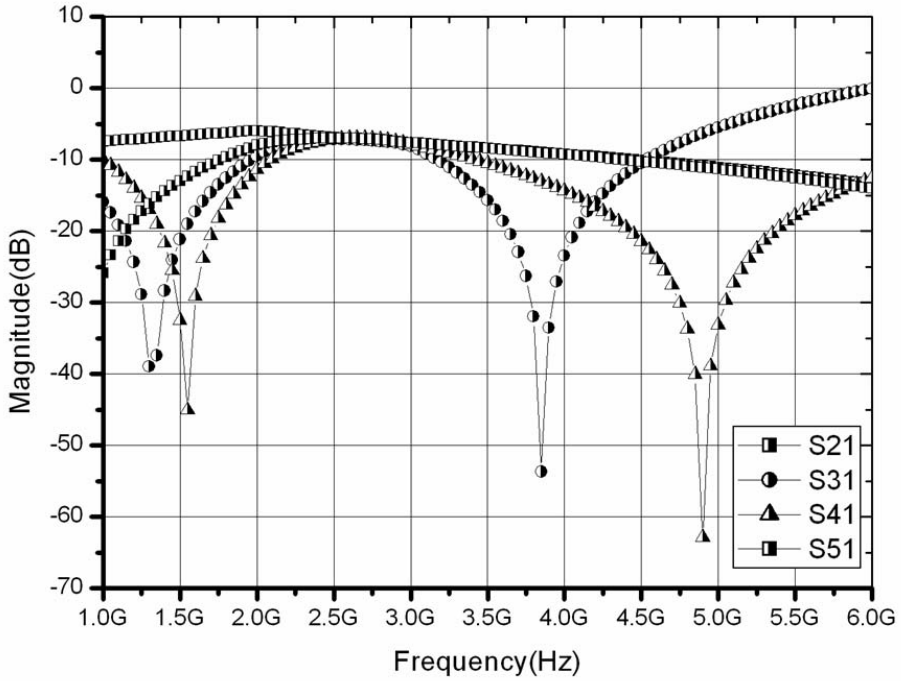


Fig. 2-29 The measured S-parameters for the fabricated quadrature Balun

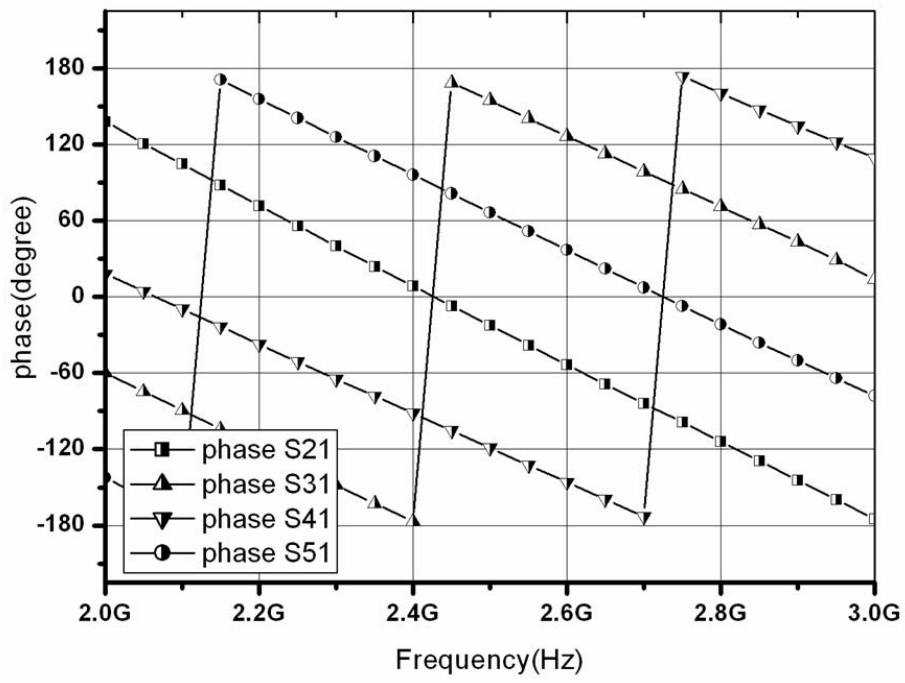


Fig. 2-30 The measured S-parameters for the fabricated quadrature Balun

The measured results show that the phase deviation less than 3° is achieved in the fabricated quadrature Balun. By the measured S-parameters, we can recognize that the fabricated quadrature Balun is suitable for our proposed sub-harmonic mixer. Fig. 2-29 and Fig. 2-30 show the magnitude in dB and phase of the measured results, respectively.

The layout of this sub-harmonic mixer is shown in Fig. 2-31, and Fig. 2-33 is the die photograph of the proposed switched Gm sub-harmonic mixer. Each bias is fed with the bonding wire connected to the prepared PCB test board except the “vdd” and “vddlo”. The bonding wire is estimated about 1nH per 1mm for the parasitic inductor, and the inductance must also be simulated with the proposed circuit. All the biases fed with bonding wires in our sub-harmonic mixer are gate biases, therefore, the variation of the estimated inductance for bonding wires cause less effect to our circuit’s performance. The PCB test board layout is shown in Fig. 2-32, and the IF differential ports are connected by bypass capacitors and SMA connectors. The selected IF here is 10MHz that the loss contributed by the PCB board and the SMA connector are negligible.

The simplified measurement setups are shown in Fig. 2-34 (a~d). The RF and LO signals are fed on wafer for elimination of undesired parasitic effects. Fig. 2-35 shows the PCB test board for this sub-harmonic mixer and the whole measurement environment in CIC.

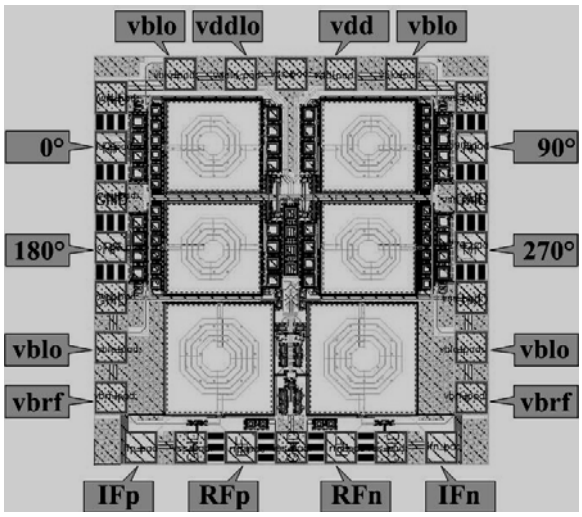


Fig. 2-31 The layout of the proposed sub-harmonic mixer

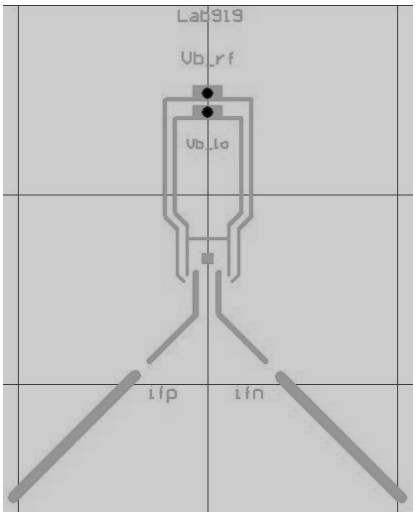


Fig. 2-32 PCB test board layout of the sub-harmonic mixer

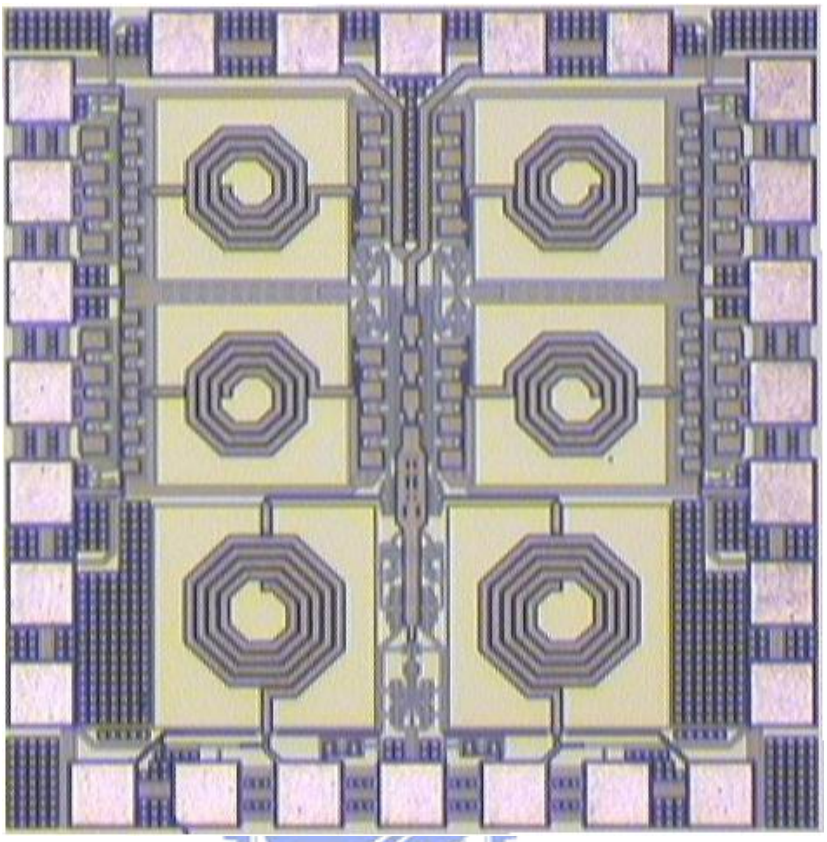


Fig. 2-33 The die photograph of the switched Gm sub-harmonic mixer

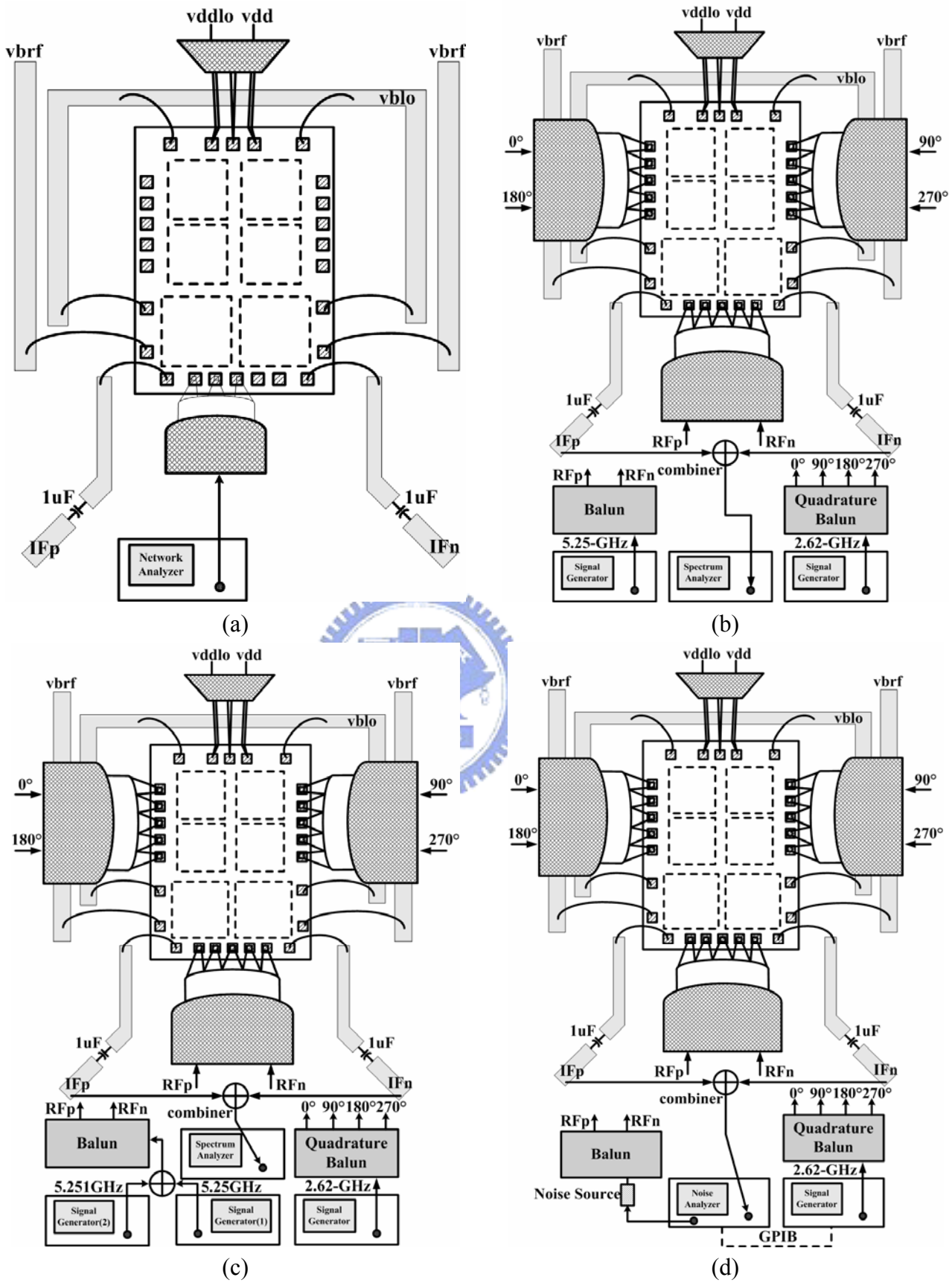
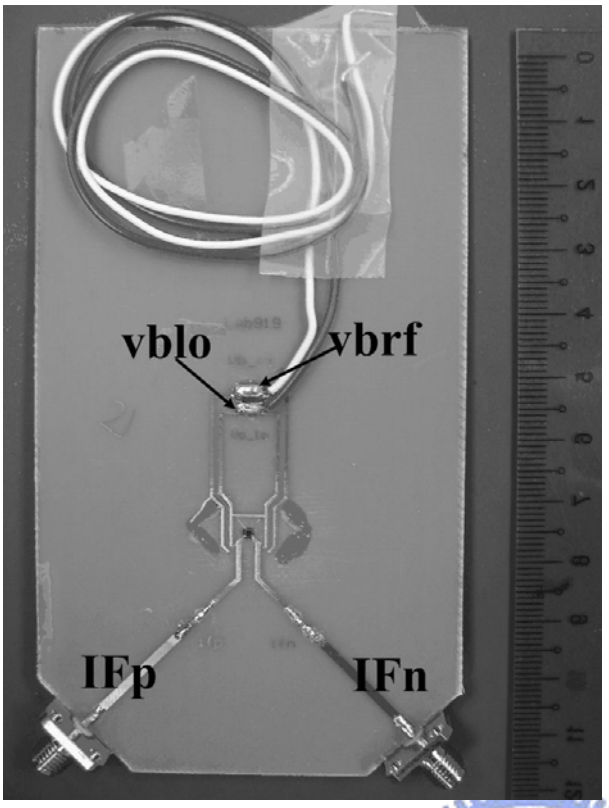
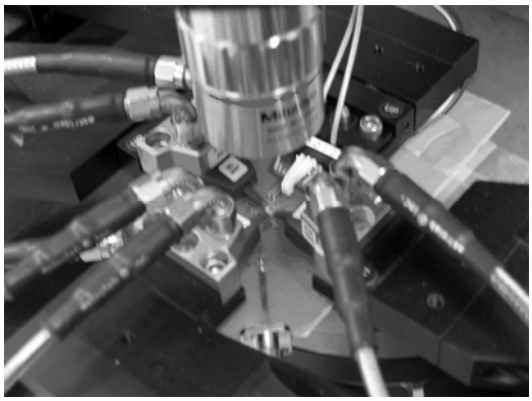
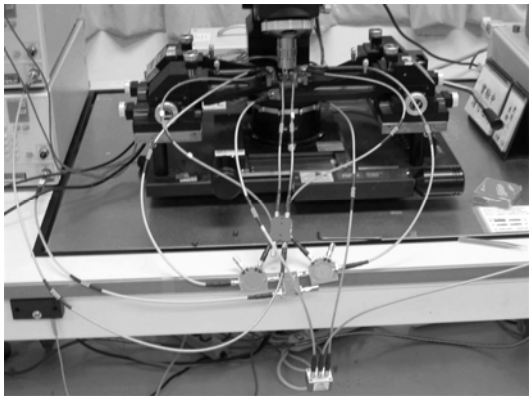


Fig. 2-34 Measurement setup of the proposed switched Gm sub-harmonic mixer for (a) input return loss (b) conversion gain (c) IIP3 and P1dB (d) noise figure

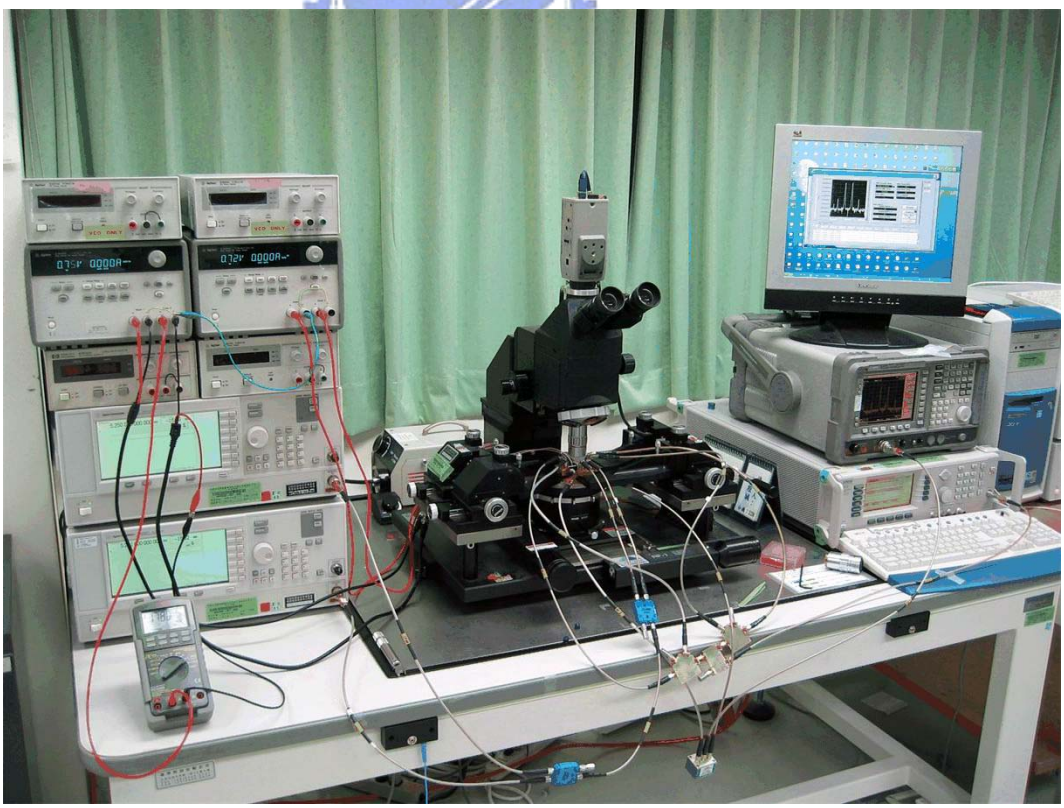


(a)





(b)



(c)

Fig. 2-35 (a) The photo of the PCB test board. (b) (c) The measurement environment in CIC

2.5.2.2 *Measurement Results*

By the measurement setups illustrated above, the measured results are listed below. The RF and LO measurement was performed on-wafer. The biases were fed with bonding wires. A quadratue LO signal source at 2.62-GHz was used. This new sub-harmonic mixer consumes no dc power while there is no LO signal input. The buffer consumes 12.42mA dc current from 1.8V power supply. Unfortunately, the measured current indicates that the process condition now falls at the vicinity of SS-corner. Therefore, the following measured results are compared with the SS-corner simulation. As shown in Fig. 2-36, the measured RF and LO input return loss are -17.2 dB at 5.25-GHz and -18.0 dB at 2.62-GHz. The input return losses are well matched to system impedance in both RF and LO inputs. In this work, a high differential conversion power gain, 12.8 dB is achieved (see Fig. 2-37). As can be seen, the maximum differential conversion power gain is happened at the LO power of 4 dBm..

Fig. 2-38 shows the DSB noise figure against the IF frequency. The LO signal is fixed to 2.62GHz, and RF signal sweep from 5.25GHz to 5.32GHz. The IF frequency we choose is 10-MHz for system integration and cost consideration [1]. The DSB noise figure is 14 dB at 10-MHz.

Finally, Fig. 2-39 shows the input 3rd order intercept point (IIP3) of -1.8 dBm. The linearity of the sub-harmonic mixer is well performed especially the mixer achieves high conversion gain.

The port to port isolation is also taken into consideration in the proposed sub-harmonic mixer. The isolation of the fundamental LO signals (2.62-GHz) to RF port and IF port are higher than 40 dB and 31 dB respectively. The more important is the second harmonic of the LO signal (5.24-GHz), and it performs higher than 67 dB and 52 dB for RF port and IF port respectively.

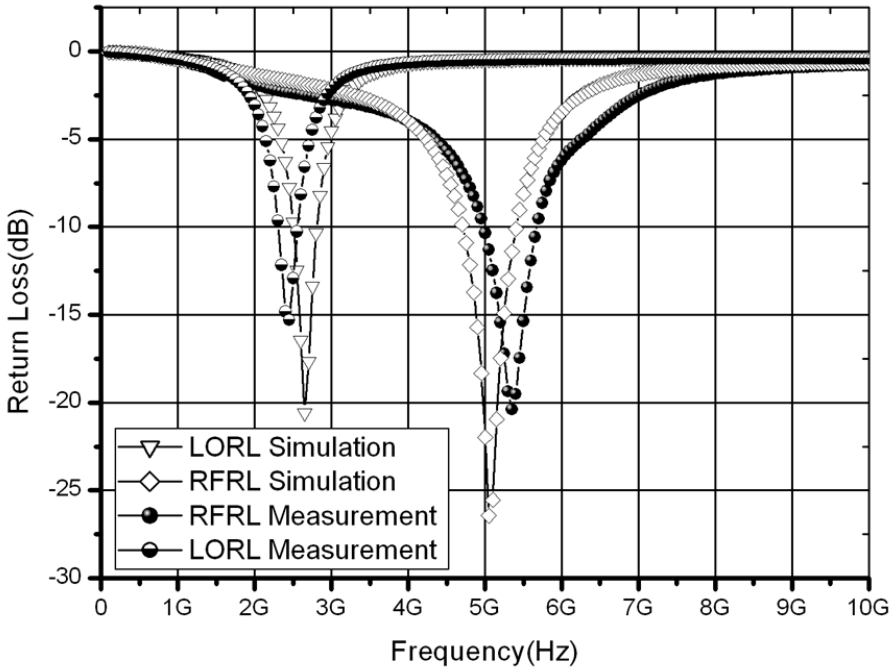


Fig. 2-36 The simulated and measured RF and LO return loss

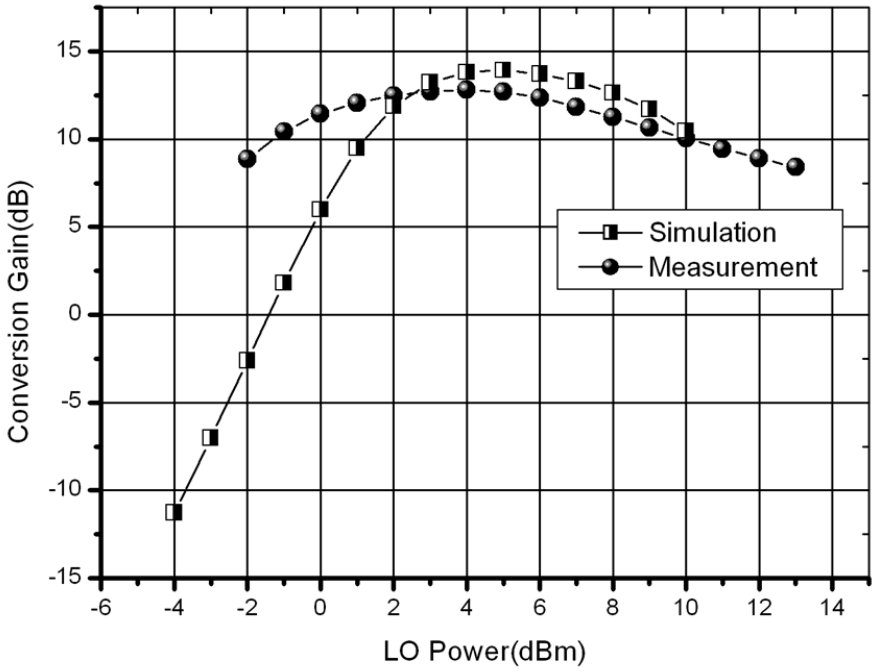


Fig. 2-37 The simulated and measured conversion power gain against the LO power

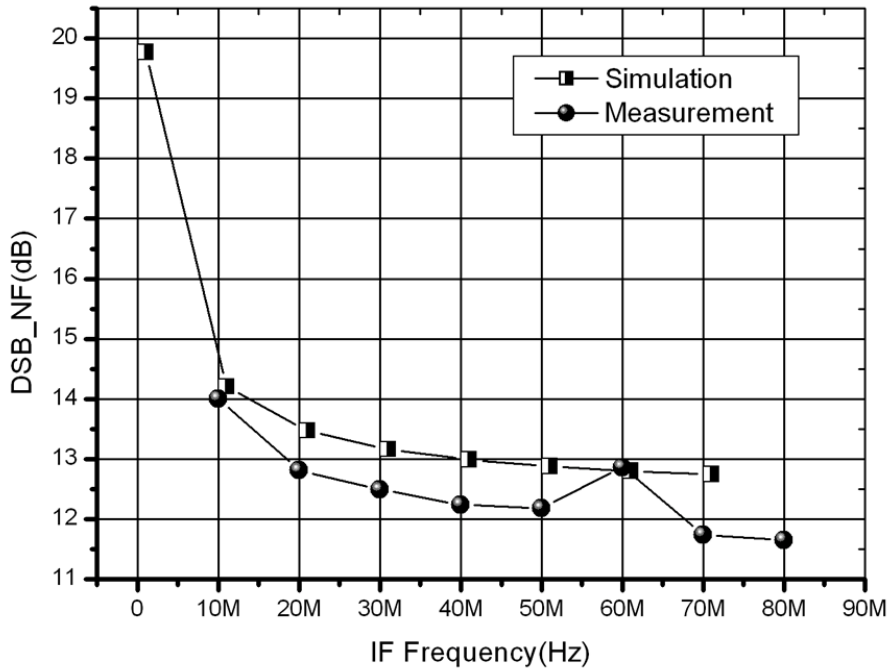


Fig. 2-38 The simulated and measured DSB noise figure

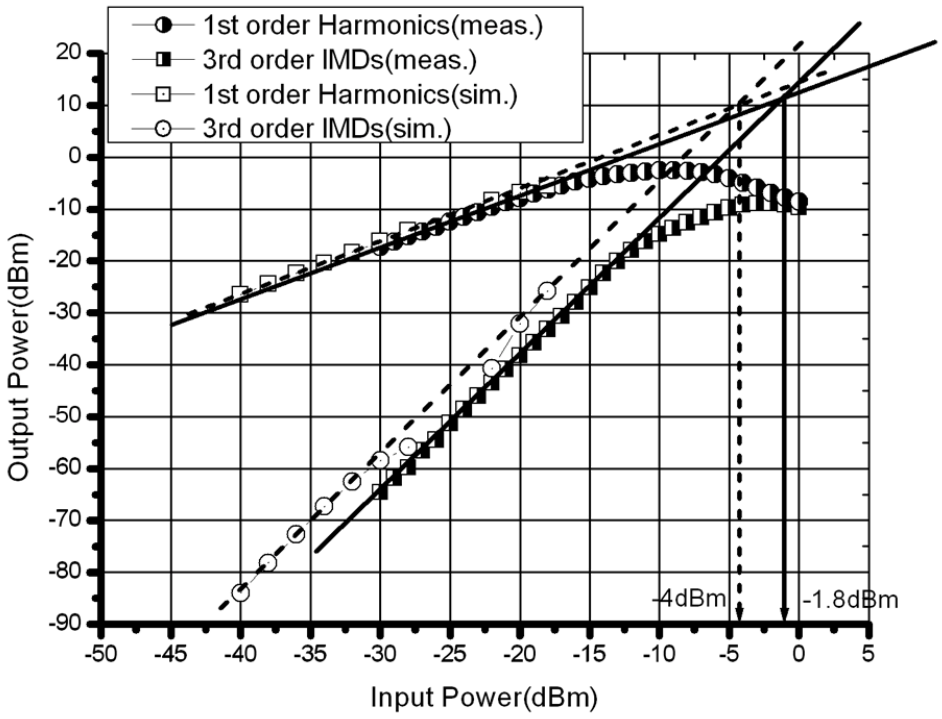


Fig. 2-39 The simulated and measured third order intercept point (IIP3)

Specification	**Measurement**	Post Simulation (SS corner)
Supply Voltage(Volt)	**1.8**	1.8
LO Power(dBm)	**4**	4
RF Return Loss(dB) @5.25GHz	**-17.22**	-14.9
LO Return Loss(dB) @2.62GHz	**-16.45**	-7.39
2LO-to-RF Isolation(dB)	**>67**	-65
Conversion Power Gain(dB)	**12.8**	13.8
IIP3(dBm)	**-1.8**	-4
Noise Figure(dB)	**14.0**	14.7
Buffer Power Consumption(mW)	**22.36**	23.956

Table 7 Summary of the measured results and post-simulation in SS-corner

2.5.2.3 *Comparison with Other Literatures*

Three sub-harmonic mixers operating at 5.2GHz band are listed and compared with our work, and they are shown in Table 8. The proposed sub-harmonic mixer achieves high conversion gain and still remains high linearity by the switched Gm prototype and the PMOS active load. In addition, it consumes no dc power while there is no LO input. The noise figure at 10MHz is 14.0dB, and this noise drawback can be alleviated by a high gain LNA in front of this sub-harmonic mixer. Comparing with the listed literatures, the measured noise figure performs well.

Ref.	Process	f_{RF} (GHz)	LO Power	CG (dB)	NF (dB)	IIP3	Pc
This Work (Meas.)	0.18um CMOS	5.25	4 dBm	12.8 @50Ω	14.0 @10MHz (DSB)	-1.8 dBm	**No dc current w/o LO**
[30] 2005 ISCAS (Meas.)	0.35um SiGe	5.205	-3.5 dBm	0 @50Ω	22.2 @50MHz (SSB)	+2.7 dBm	10.95mW
[31] 2006 MWCL (Meas.)	0.18um CMOS	5.9	15 dBm	10.8 @1MΩ	N/A	7.9 dBm	3.5mW
[29] 2005 MTT (Meas.)	0.18um CMOS	2.1	6 dBm	10.5dB @ N/A	17.7 @>200MHz (N/A)	-3.5 dBm	12.5mW
[32] 2004 (Sim.)	0.25um CMOS	5.6	N/A	8.01 @1MΩ	5.96 @0Hz (DSB)	-6.5 dBm	5.25mW
[33] 2005 (Sim.)	0.18um SiGe	5.6	N/A	8.05 @1MΩ	N/A	0 dBm	4.68mW

Table 8 The summary of this work and comparison with other literatures

Chapter 3

KA BAND LNA USING 0.18 μm CMOS

3.1 Introduction

The growing demand for wider bandwidth motivates integrated circuits to move toward higher frequencies. In the past, GaAs-based HEMT and HBT technology dominate most of the applications due to lossless substrate in these processes. But the more attractive process, CMOS, has resulted in a strong motivation to implement these high-frequency and high-performance RF systems. The loss of the Si-based substrate is a serious issue on building these high frequency circuits. For instance, the Si-based substrate caused the on-chip inductors or on-chip transmission lines to be loss and hence caused them to be low Q. However, a high performance CMOS front-end for applications above 20GHz has been reported and the performance of these CMOS circuits show CMOS process has potential for building RF systems above 20GHz [34]~[37]. Although the SOI CMOS process has demonstrated excellent performance in LNA designs, the standard bulk CMOS process still attractive due to the cost and the integration consideration. Here we use the TSMC 0.18um CMOS technology to implement the K-band low noise amplifier. The technology offers polysilicon resistor, MIM capacitance, and six metallization layers. The substrate resistivity is 15~25Ω-cm [35]. To operate upper K-band, low loss inductors with small inductance and high self-resonance frequency are required. As shown in Fig. 3-1, to minimize the resistive loss, the transmission lines which are used as inductors are placed on the top most layer with 2um thickness. Ideally the wide transmission lines are preferred to lower resistive loss, but wide transmission lines lead to more substrate loss by parasitic capacitance. Here the width of

the transmission line is optimized to have higher quality factor. All the transmission lines are simulated by the EM simulator, sonnet 9.52, to consider the radiation loss and parasitic effects.

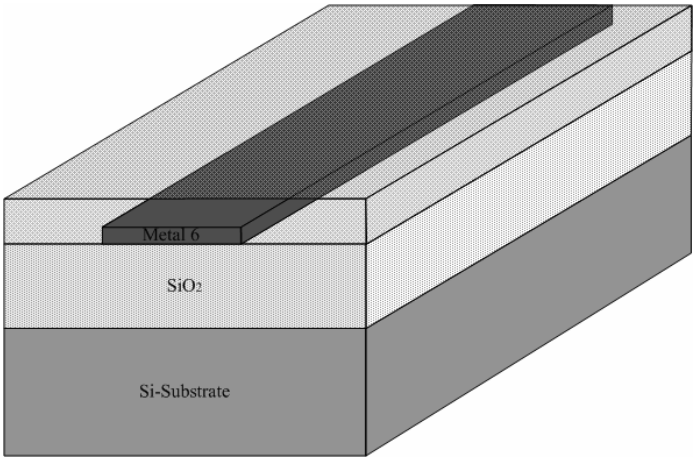


Fig. 3-1 Using top metal as the transmission line

3.2 System Application

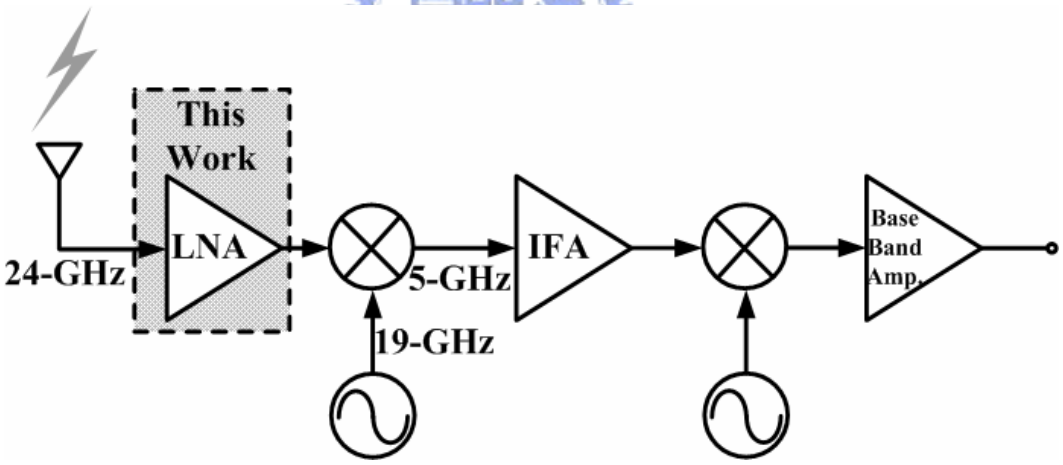


Fig. 3-2 Simplified block diagram of a 24-GHz Receiver

Fig. 3-2 shows the simplified block diagram of a typical receiver. In this architecture, the RF amplification and down conversion stage are the most challenging to implement in CMOS. In this work, a 24-GHz LNA is designed and validated by the standard 0.18um CMOS process.

A system application, LMDS, is introduced in this section and Table 9 summarizes some

features of this system [38]. LMDS is a broadband wireless point-to-point or point-to-multipoint communication system operating above 20 GHz (depending on country of licensing) that can be used to provide digital two-way voice, data, Internet, and video services. This system provides network service to area with poor or nonexistent wired infrastructure. Comparing to wire-line, lower infrastructure costs are required by LMDS.

LMDS point-to-point wireless applications include connections between cell phone towers and central offices, or trunk connections between metropolitan buildings at data rates between 150 Mbps and 620 Mbps over a range of 2 km. Point-to-multipoint products can transmit packets at 150 Mbps omnidirectionally over a distance of 1 to 3 km. LMDS operates in 24 GHz, 28 GHz, and 39 GHz frequencies achieving data rates of 100Mbps with 45 Mbps being more typical rates

System	LMDS	
Frequency Range	24GHz 28GHz 39GHz	
Application	Point-to-point	Point-to-multipoint
Distance	2km	1~3km
Data Rate	150~620 Mbps	150 Mbps
Modulation Method	TDMA FDMA CDMA	
Target Market	Large & Medium Enterprise	

Table 9 Summary of the LMDS system

3.3 Circuit Design

There are several prototypes to construct the 24GHz LNA. Since the transistor's gain is not sufficient in such high frequency, three cascaded common source stages are applied to build the proposed LNA. The choices of the MOSFET in each stage dominate the performance of the designed LNA. Taking the transistor into simulator and analyzing the major characteristic of the transistor is the first step in our design flow. To connect each stage by the transmission lines bring the problem of inter-stage matching networks. And the

inter-stage matching networks should be designed carefully to have maximum power transfer. Properly choosing the Γ_s locating between constant NF circle and constant available gain circle, and these circles help us to analyze the behavior and characteristic of the LNA.

3.3.1 Proper Device Size Choice

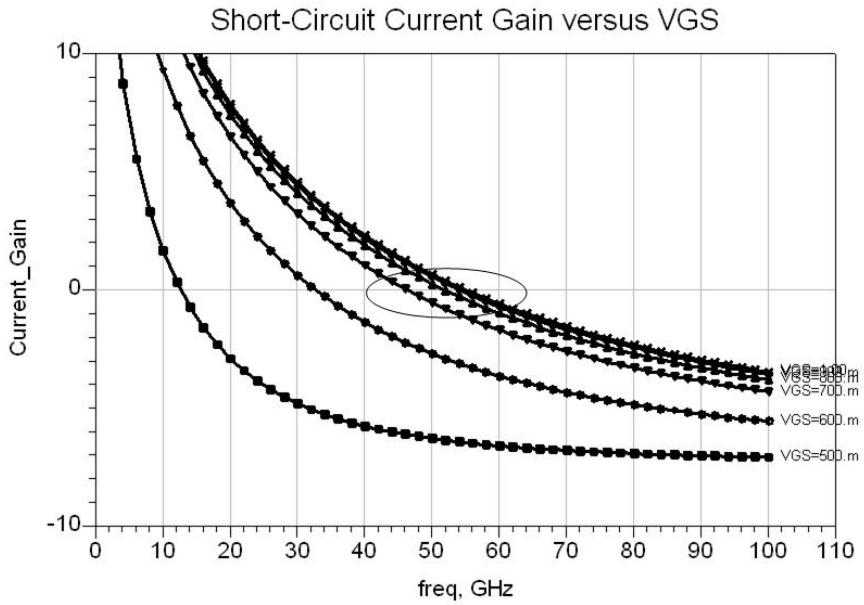


Fig. 3-3 Simulation results of f_t versus VGS

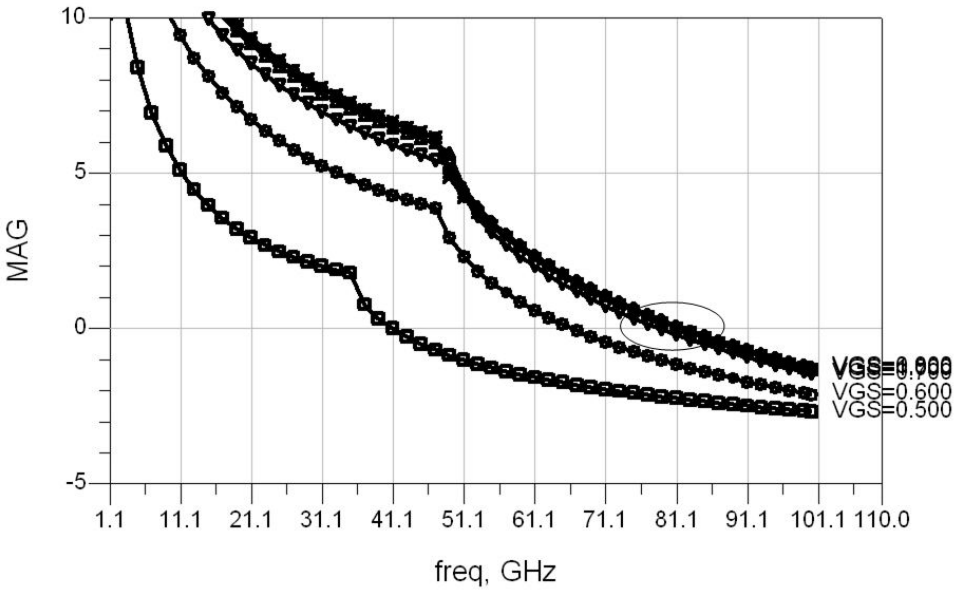


Fig. 3-4 Simulation results of $f_{\max}$ versus VGS

The TSMC 0.18um MOSFET have been demonstrated with the cut-off frequency and the maximum oscillation frequency of 70GHz and 58GHz, respectively [34]. We take the MOSFET with width 35um and length 0.18um for simulation. The modified MOSFET model for simulation is based on the BSIMv3 SPICE model, with some passive components added to take into account of the parasitic effects in the microwave. The simulated results for f_t and $f_{\max}$ versus V_{GS} are shown in Fig. 3-3 and Fig. 3-4, respectively. And it confirms our quote from [34].

The first stage of the proposed LNA should be low noise to suppress the noise figure of the LNA. Properly choosing the transistor size and the source degeneration inductor makes the minimum noise and available gain to simultaneously attain. Finally, constructing each common source stage step by step, we can illustrate the designed LNA perform gain and noise figure as expected.

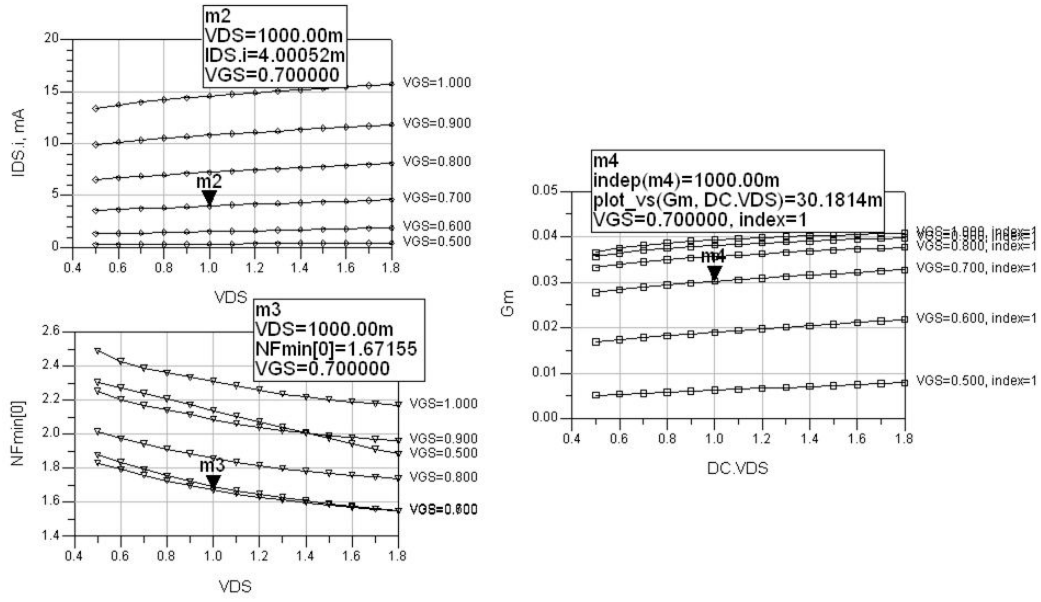


Fig. 3-5 Simulation of IDS, NFmin , and Gm versus VGS and VDS

To have insight into the characteristic of the MOSFET, the transistor has been simulated the NFmin, Gm, and current consumption against both V_{DS} and V_{GS}. As shown in Fig. 3-5, the length and width of the selected transistor is 0.18um and 80um, respectively. To perform low

power consumption, the V_{DS} of each stage are fixed to 1V. We choose V_{GS}=0.7V to get better minimal noise figure. As indicated in Fig. 3-5, the selected transistor performs current consumption of 4mA form 1V power supply, minimal noise figure of 1.67155dB, and transconductance of 30.1814mA/V.

3.3.2 Stability Circle

The stability of an amplifier is a very important consideration in a design and can be determined by the S parameter, the matching networks, and the terminations. Input and output stability circle is plotted to determine the stable region. The input and output stability circles can be plotted on Smith chart by the S-parameter of a selected transistor at one frequency point:

(Output Stability Circle)

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \text{ (radius)} \tag{3.1}$$

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \text{ (center)} \tag{3.2}$$

(Input Stability Circle)

$$r_s = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \text{ (radius)} \tag{3.3}$$

$$C_s = \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \text{ (center)} \tag{3.4}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.5}$$

(3.1) and (3.2) show the radius and center of the output stability circle. Meanwhile, (3.3) and (3.4) shows the radius and center of the input stability circle. Applying the simulated S-parameters into (3.1) ~ (3.5), we can plot the input and output stability circles. Fig. 3-6 and Fig. 3-7 show the plotted input and output stability circles at 24-GHz. We can observe that the selected MOSFET at fixed bias condition exhibits potentially unstable. If there are some variations due to CMOS process, it causes the selected Γ_s or Γ_L to be inside the unstable

region. Hence, we need to use the source degeneration to stabilize the MOSEFET.

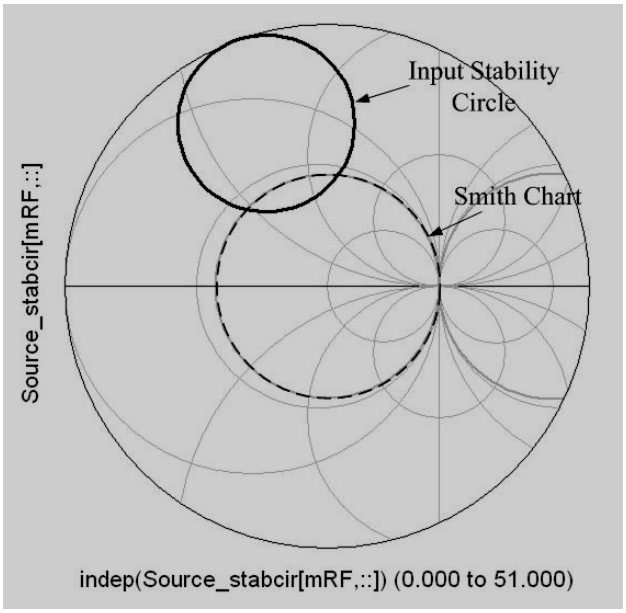


Fig. 3-6 Plot the input stability circle on smith chart without source degeneration

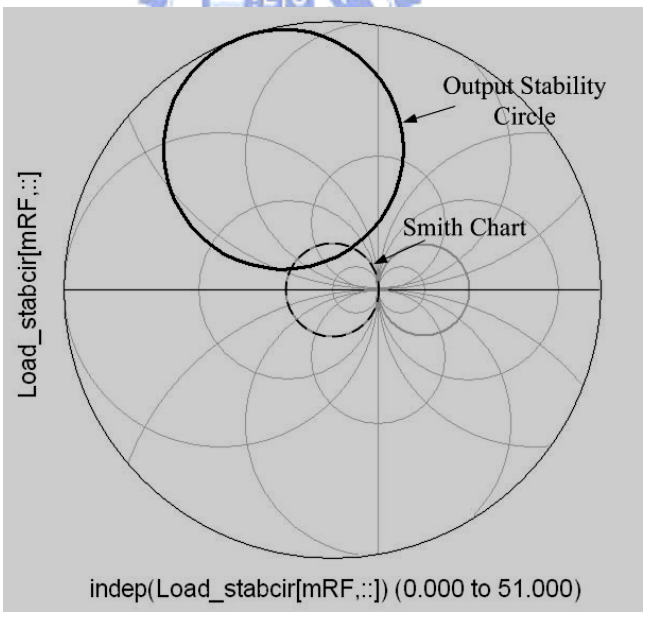


Fig. 3-7 Plot the output stability circle on smith chart without source degeneration

There is also one notice that simultaneously conjugated match implies that the two port device is unconditional stable. The simultaneously conjugated match causes the device to perform maximum available gain, and the input VSWR will be 1. However, input return loss

is often sacrificed to obtain noise matching. Hence, the source degeneration here not only keeps the MOSFET to be unconditional stable, but also makes the input impedance and noise figure match simultaneously.

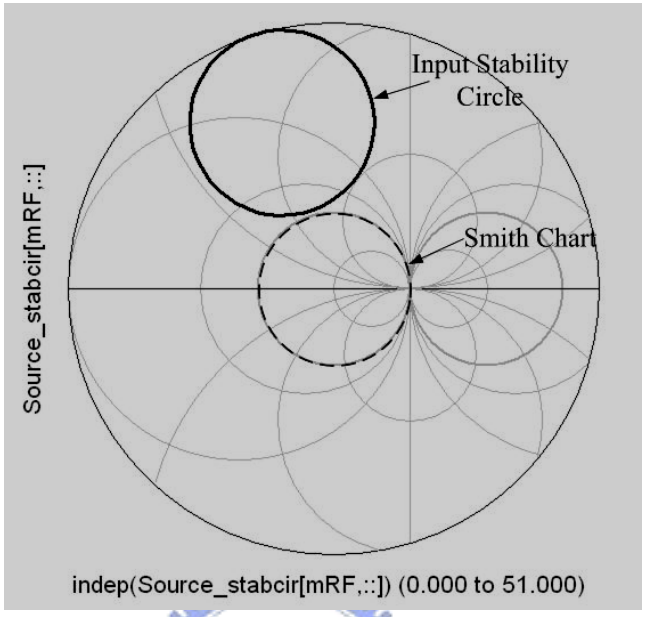


Fig. 3-8 Plot the input stability circle on smith chart with source inductor of 0.1nH

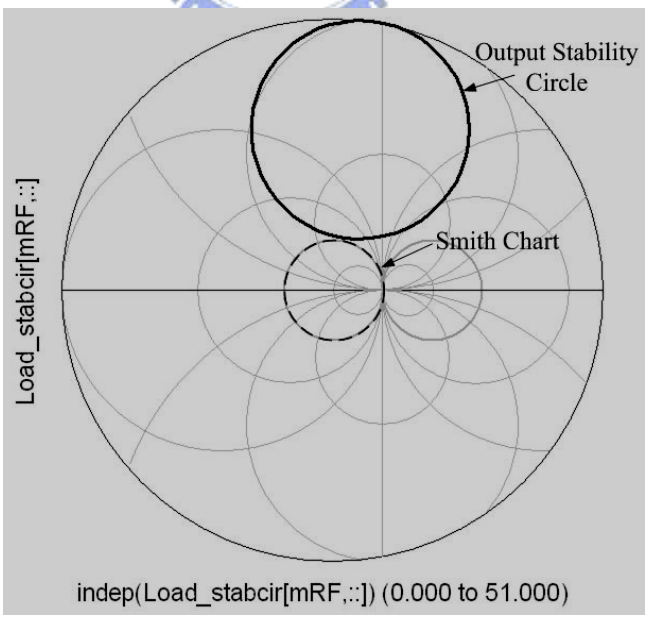


Fig. 3-9 Plot the output stability circle on smith chart with source inductor of 0.1nH

In addition, the additional source inductance doesn't seriously degrade the noise

performance. The size of the source degeneration inductor must be selected carefully, since increasing the inductance reduces amplifier gain. Here a source degeneration inductor of 0.1nH is selected, and the stability circle is plotted in Fig. 3-8 and Fig. 3-9. The MOSFET is unconditional stable now.

3.3.3 Available Gain Circle

The power gain of the proposed LNA can be estimated by plotting the constant available gain circle. (3.6) and (3.7) indicate the center and radius of the available gain circle, respectively. The g_a , K, and C_1 in (3.6) and (3.7) are listed in (3.9), (3.10), and (3.11) [1]. The C_a and r_a are both functions of $[S]$ and Γ_s. By determining the needed available gain, Γ_s must locate at the constant available gain circle. The power gain design goal of our proposed LNA is about 15 dB, this means 6 dB power gain is required for each common source stage. The selected source inductor is 0.1nH, this produces the power gain about 6.95 dB for maximum power transfer. Fig. 3-10 shows the constant available gain circles from 6.953 dB to 3.953 dB.

$$C_a = \frac{g_a C_1^*}{1 + g_a(|S_{11}|^2 - |\Delta|^2)} \tag{3.6}$$

$$r_a = \frac{[1 - 2K|S_{12}S_{21}|g_a + |S_{12}S_{21}|^2 g_a^2]^{1/2}}{|1 + g_a(|S_{11}|^2 - |\Delta|^2)|} \tag{3.7}$$

$$G_A = \frac{|S_{21}|^2 (1 - |\Gamma_s|^2)}{(1 - |\frac{S_{22} - \Delta\Gamma_s}{1 - S_{11}\Gamma_s}|^2)|1 - S_{11}\Gamma_s|^2} = |S_{21}|^2 g_a \tag{3.8}$$

$$g_a = \frac{G_A}{|S_{21}|^2} = \frac{1 - |\Gamma_s|^2}{1 - |S_{22}|^2 + |\Gamma_s|^2 (|S_{11}|^2 - |\Delta|^2) - 2\mathrm{Re}(\Gamma_s C_1)} \tag{3.9}$$

$$C_1 = S_{11} - \Delta S_{22}^* \tag{3.10}$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.11}$$

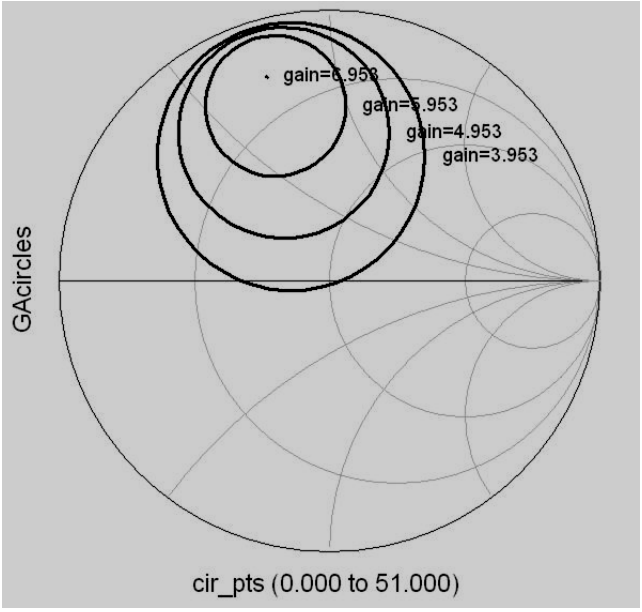


Fig. 3-10 Plot the available power gain circle on smith chart with source inductor of 0.1nH

3.3.4 Noise Circle

The noise figure is a major performance measure in a low noise amplifier design. If the MOSFET is selected and biased at a fixed voltage, the noise figure performance is dominated by the selection of Γ_s. Selection of Γ_s equal to Γ_{opt} always sacrifices the available power gain and input VSWR. Constant noise figure circles are needed to recognize the trade off between gain and noise. Eq. (3.12) shows the noise figure indication, and it depends on $F_{\min}$, r_n and Γ_{opt}. These quantities are known as the noise parameters and are given by the manufacturer of the transistor or can be determined experimentally. Hence, giving a constant noise figure, F_i, (3.12) is a function of Γ_s. (3.12) can be rewritten to a spherical form of (3.13) and N_i also can be identified by a given F_i. Therefore, a constant noise figure circle can be plotted on Γ_s plane. The center and radius of a constant noise figure circle can be determined obviously and they are listed in (3.15) and (3.16) respectively. Fig. 3-11 shows the constant noise figure circles from $F_{\min}$ of 1.508dB to NF of 2.108dB.

$$F = F_{\min} + \frac{4r_n \,|\, \Gamma_s - \Gamma_{opt} \,|^2}{(1-|\,\Gamma_s\,|^2)\,|\,1+\Gamma_{opt}\,|^2} \tag{3.12}$$

$$|\,\Gamma_s - \frac{\Gamma_{opt}}{1+N_i}\,|^2 = \frac{N_i^2 + N_i(1-|\,\Gamma_{opt}\,|^2)}{(1+N_i)^2} \tag{3.13}$$

$$N_i = \frac{F_i - F_{\min}}{4r_n}\,|\,1+\Gamma_{opt}\,|^2 \tag{3.14}$$

$$C_{Fi} = \frac{\Gamma_{opt}}{1+N_i} \tag{3.15}$$

$$r_{Fi} = \frac{1}{1+N_i}\sqrt{N_i^2 + N_i(1-|\,\Gamma_{opt}\,|^2)} \tag{3.16}$$

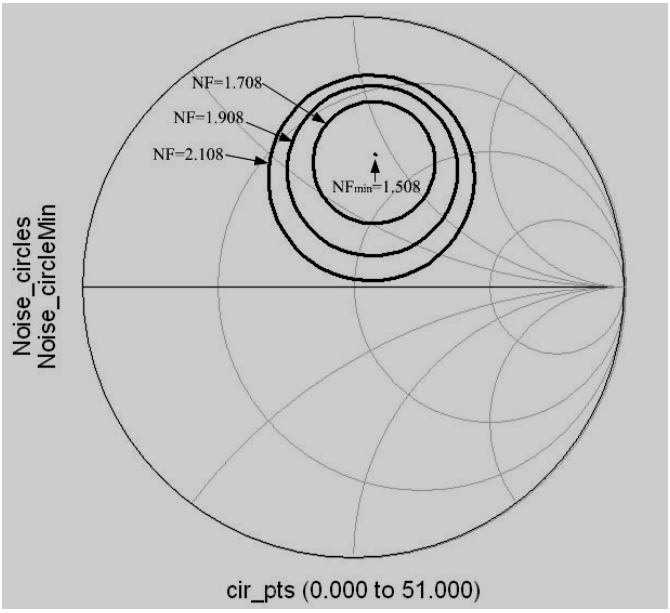


Fig. 3-11 Plot the constant noise figure circle on smith chart with source inductor of 0.1nH

Using the constant circles illustrated above and plotting these circles on a Γ_s plane, a clear inspection can be obtained. As shown in Fig. 3-12, Γ_s is selected for input VSWR consideration. If the selected Γ_s equal to Γ_{opt}, the input VSWR must be poor.

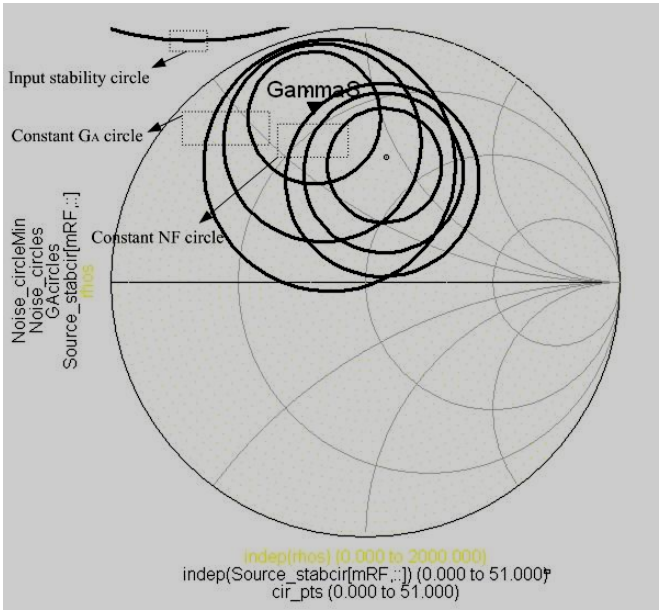


Fig. 3-12 Plot constant GA, NF circles and input stability circle on Γ_s plane

Otherwise, if the Γ_s is selected for maximum power transfer, the noise figure performance must be sacrificed. Hence, using source degeneration inductor makes these tradeoffs possible. The single stage performance of the selected Γ_s is shown in Table 10. The output matching network of each stage is designed for maximum power transfer, that is $\Gamma_L = \Gamma_{out}^*$.

Noise Figure (dB) with source impedance at marker GammaS	Source impedance at marker GammaS	Optimal load impedance for power transfer when source impedance at marker GammaS is presented to input	Transducer power gain (dB) when these source and load impedances are used
2.154	12.548+j37.103	20.701+j53.987	6.878

Table 10 Single stage performance of the selected Γ_s

Once the Γ_s is selected, the input matching network can be obtained. Fig. 3-13 shows the input matching network for selected Γ_s. The matching network is accomplished by the

Ansoft Designer SV. First, we need to assume all the lump components to be idea. After finding out all the desired values for matching network, the practical components are implemented and simulated to fit them.

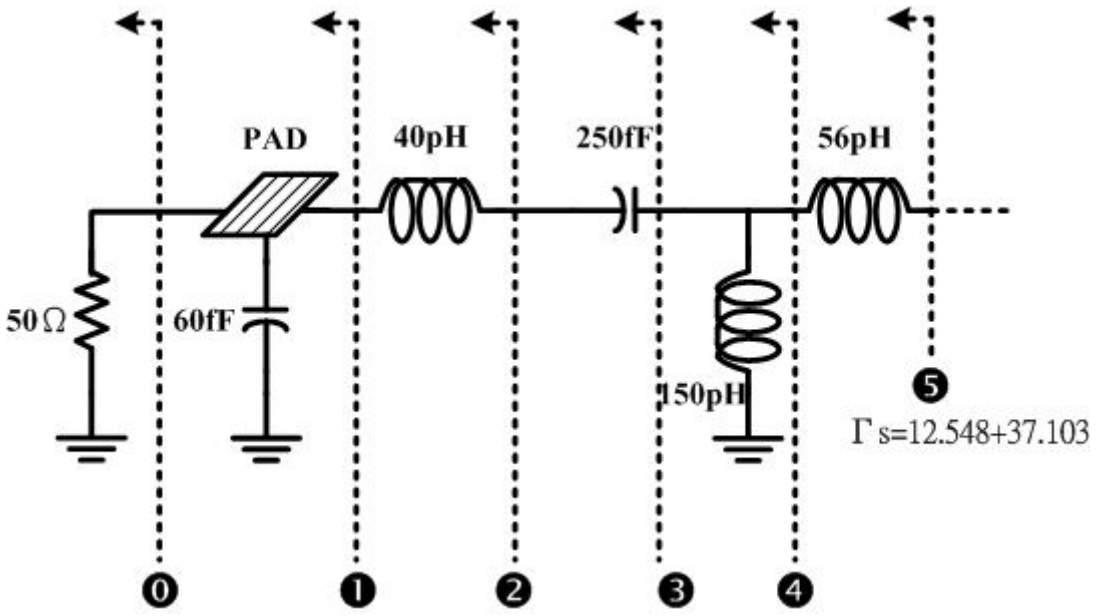


Fig. 3-13 Input matching network by the selected Γ_s

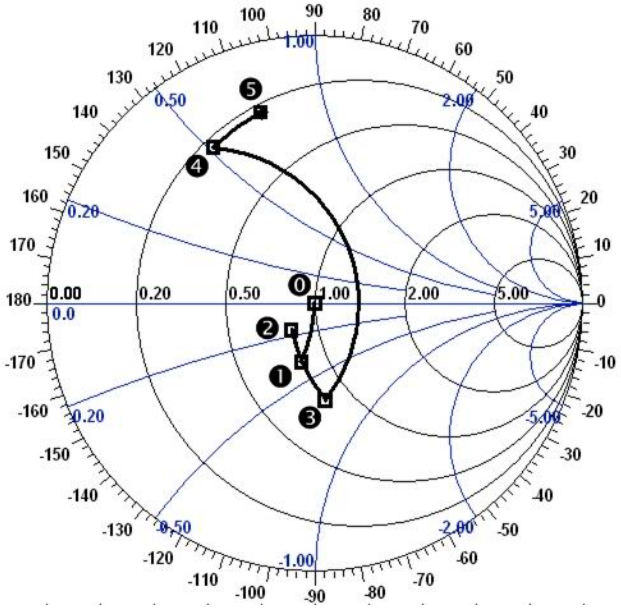


Fig. 3-14 Matching behavior form 50Ω to Γ_s

Fig. 3-14 shows the matching behavior for the consideration of bias and dc block, and the passive components are ideal. By the number of steps denoted on graphic, clearly the 50Ω

source impedance is shifted to the desired Γ_s.

The matching network has to consider the parasitic pad capacitance and any connected lines. For the size of 100um X 100um,the pad capacitance is estimated of 60fF between metal 6 and metal 1 [35]. All the inductors in such high frequency must be simulated by the EM simulator, and each inductor in the circuits must be separated at least 50um to reduce unwanted coupling effects. The series connected inductors in the input matching network are added for keeping inductors 50um away [36]. The transmission lines as well as inductors are implemented on the top metal layer made of 2-um-think AlCu.

The capacitors in the designed LNA all are shield type. For circuits operating upper than 20-GHz, the shield capacitor is expected to isolate unwanted substrate noise. The equivalent RLC model for the shield and w/o shield capacitor is shown in Fig. 3-15 and Fig. 3-16, respectively. In these two equivalent circuits, the inter-metal dielectric Cmim is the main element of the capacitor. Rtop and Ltop are the parasites existing in the electrode connected to port1, and Rbot and Lbot are the parasites existing in the electrode connected to port2. Cox of MIM without shield represents the capacitance between port2 bottom plate metal and substrate. Csub and Rsub are parasitic that presents the substrate capacitance and resistance. Cox of MIM with shield represents the capacitance between port2 bottom metal plate to metal shield. It is obvious that the MIM capacitor with metal4 shield has higher quality factor than the one without metal shield. The shield type capacitor also set the substrate noise apart that higher noise performance can be achieved. Fig. 3-17 and Fig. 3-18 show the geometric inspection of the MIM capacitor w/i and w/o shield respectively. Both of these capacitors are formed with metal6, via56, CTM5 and metal5. But one more shield plate, metal4, is below metal5 to construct of shield capacitor.

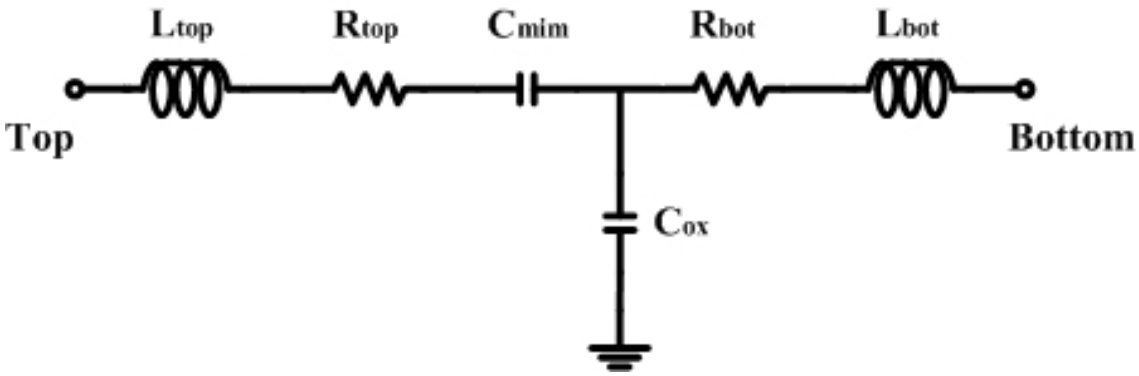


Fig. 3-15 The equivalent RLC circuit for MIM w/i shield structure

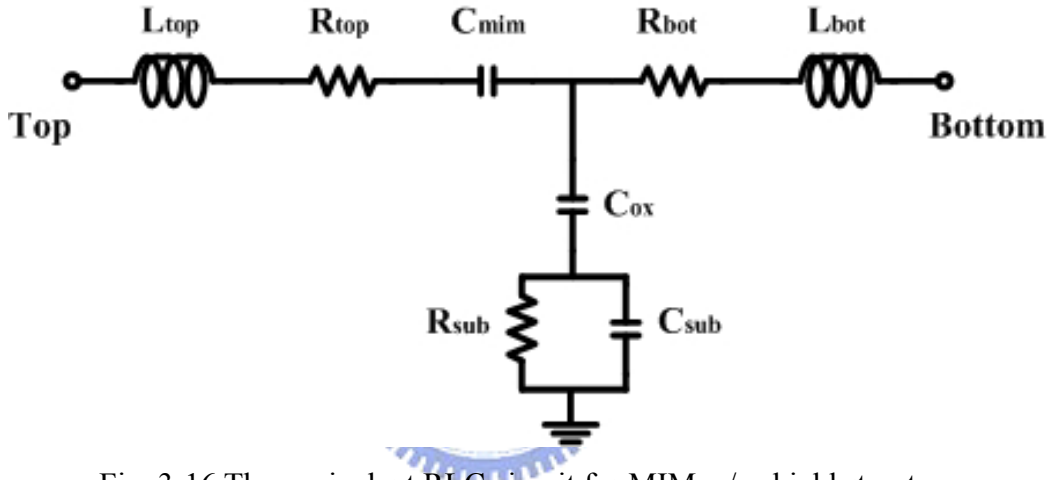


Fig. 3-16 The equivalent RLC circuit for MIM w/o shield structure

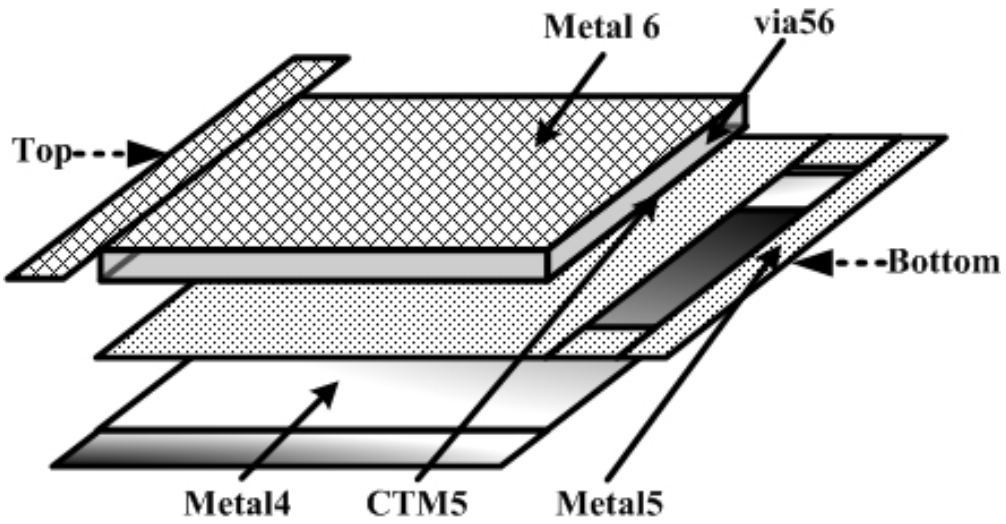


Fig. 3-17 3-D view for MIM with metal4 shield

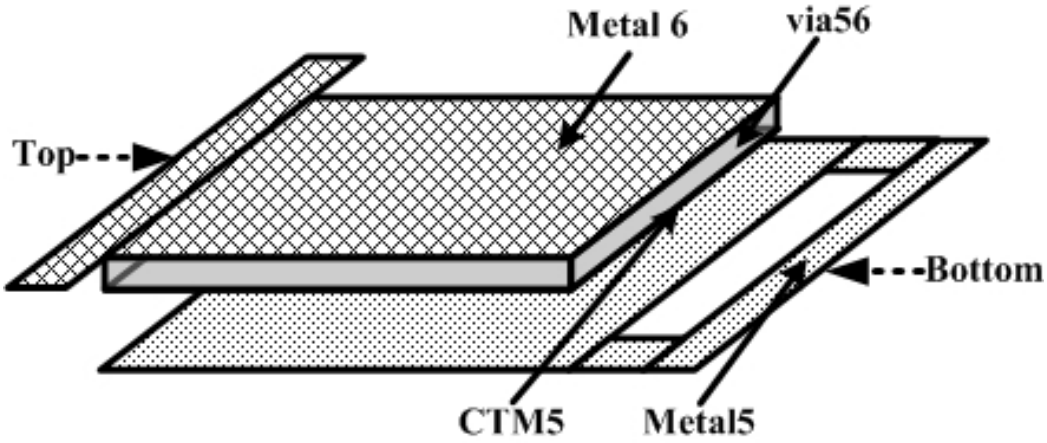


Fig. 3-18 3-D view for MIM without metal4 shield

3.3.5 Inter Stage Matching Network

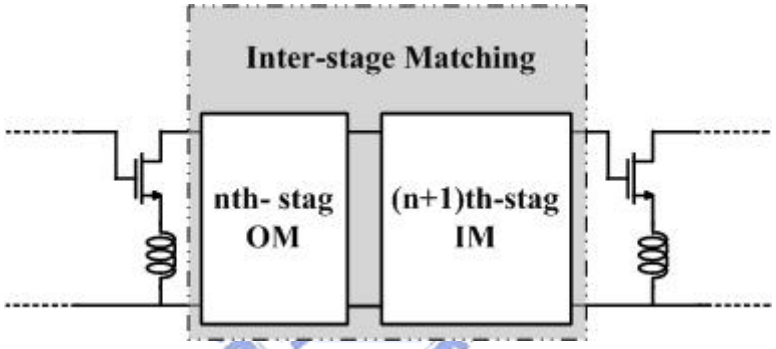


Fig. 3-19 Inter stage matching networks are needed to design

After accomplishing the input matching network for selected Γ_s, the output matching network of 1st stage and input matching network of 2nd stage must be designed simultaneously. Achieving maximum power transfer is the design goal of inter stage matching networks. This means that the output matching network of 1st stage must be complex conjugated with the input matching network of 2nd stage. Fig. 3-19 shows the inter stage networks between each stages. The matching networks should be designed to suit the bias condition and the uncomplicated consideration. The compact matching network reduces the resistive loss produced by the passive components, and achieves higher gain and lower noise contribution. By this reason, the inter stage system impedance is no longer 50Ω. The complex conjugated impedances are required for inter stage matching networks. In Fig. 3-20, 'A' and 'B' are so

called system impedances in the inter stage matching network. The impedance “A” and “B” are fixed to 10.57+j28.3. The input matching network of 2nd stage is designed first.

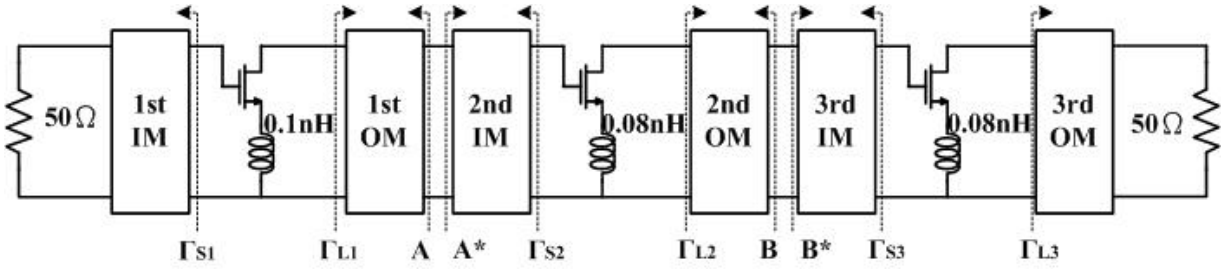


Fig. 3-20 The complex conjugated impedances are required in the proposed LNA

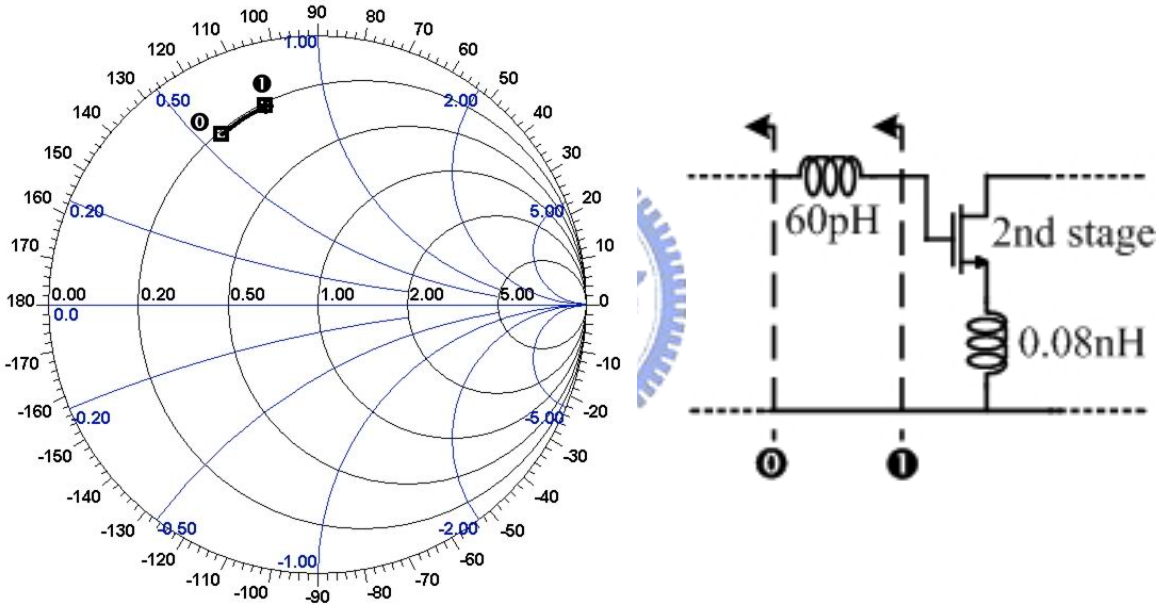


Fig. 3-21 The matching behavior and circuits from inter stage matching impedance (10.57+j28.3) to the Γ_{s2}

Fig. 3-21 shows the matching behavior on Smith chart. Only a transmission line performing an inductivity of 60pH is required, and this short line indeed reduces the parasitic loss. The output matching network of 1st stage acts as a high pass filter at the drain of the MOSFET, and it also suitable for bias. As shown in Fig. 3-22, an inductor of 164pH and a capacitor of 570fF are required to construct the L-type high pass filter. The inductor and capacitor must be selected in a realizable scale and also designed for a compact layout.

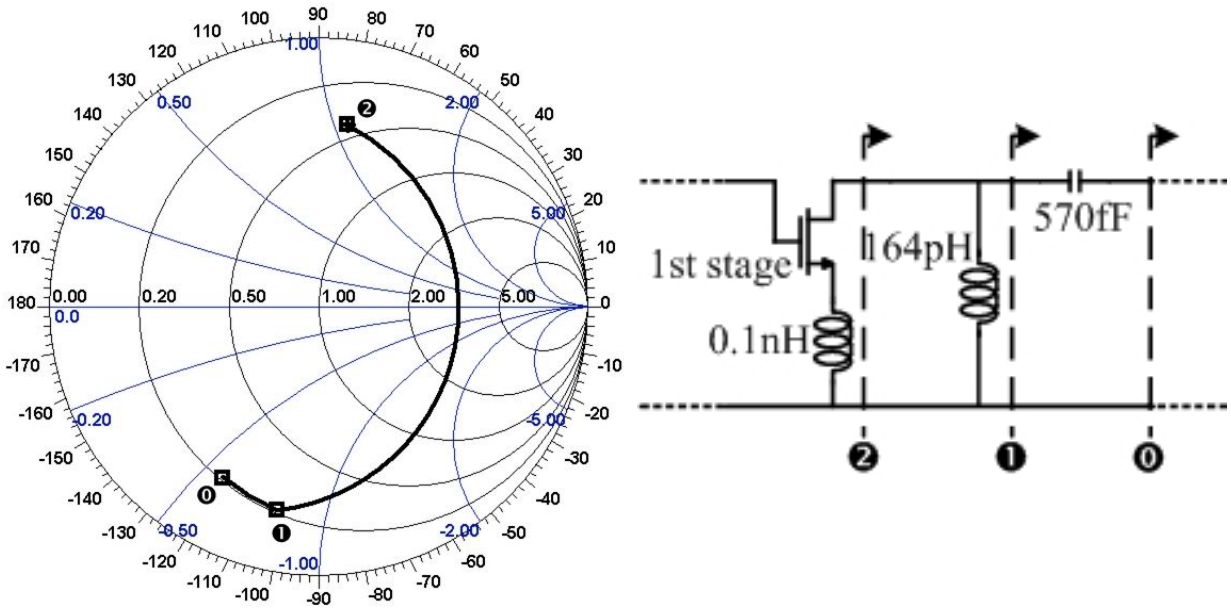


Fig. 3-22 The matching behavior and circuits from conjugated inter stage matching impedance (10.57-j28.3) to the Γ_{L2}

The inter-stage between 1st and 2nd stage now had been completed, and the design procedure of the following stages is also identical with this procedure. Because the selected Γ_s is a little different from the 1st stage, the 2nd stage output L-type matching network is different from the 1st stage output matching network.

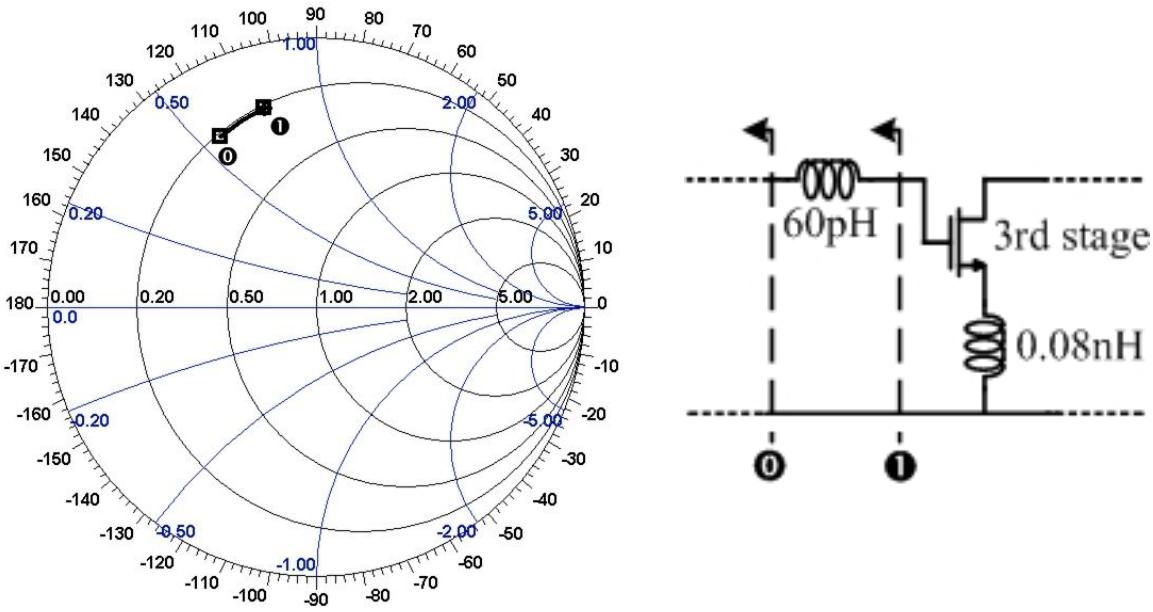


Fig. 3-23 The matching behavior and circuits from inter stage matching impedance (10.57+j28.3) to the Γ_{s3}

Fig. 3-23~Fig. 3-26 show the matching behavior on smith chart and the corresponding matching networks. Table 11 lists the input or output reflection coefficient used in each stage. Finally, the structure of the 24-GHz LNA is presented in Fig. 3-27. The simulation results with ideal passive components and on-chip one are discussed in the next section.

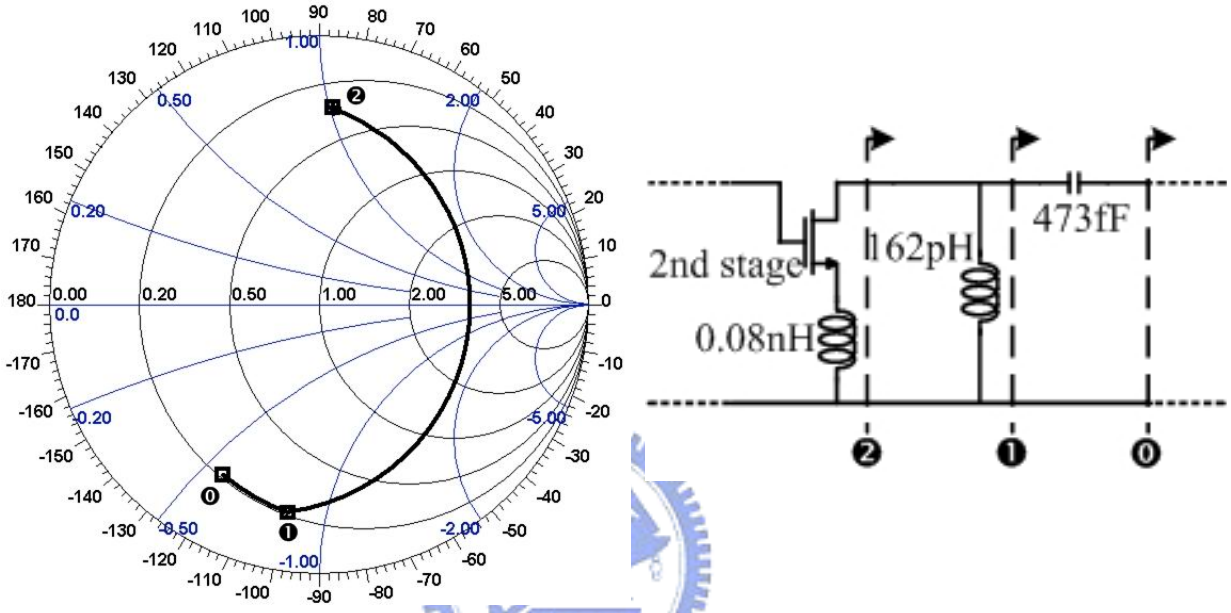


Fig. 3-24 The matching behavior and circuits from inter stage matching impedance (10.57+j28.3) to the Γ_{s3}

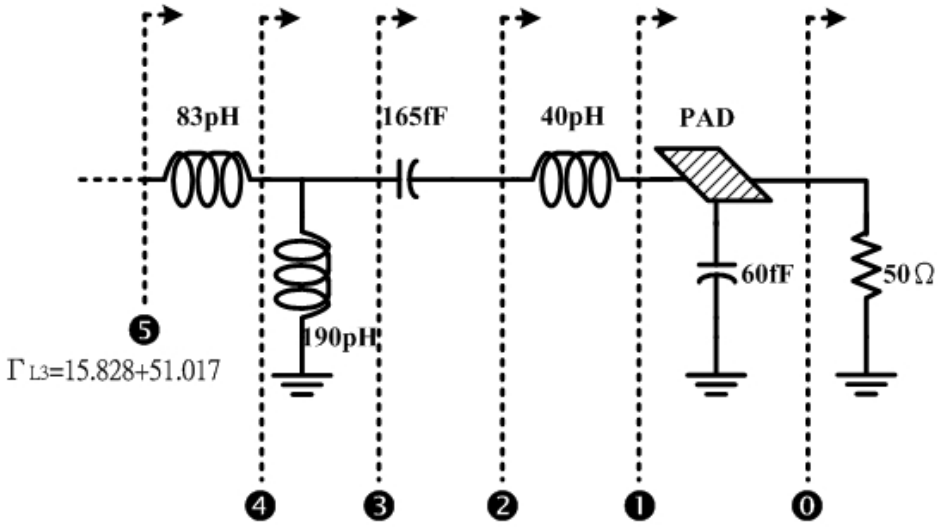


Fig. 3-25 Output matching network by the selected Γ_{L3}

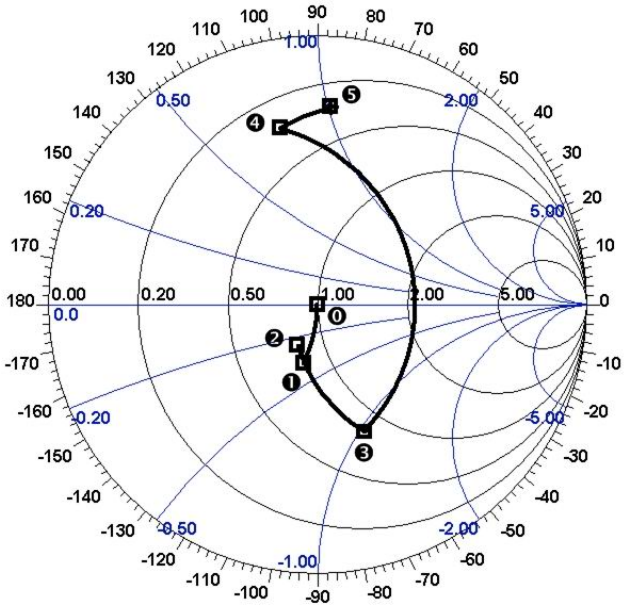


Fig. 3-26 Matching behavior form 50Ω to Γ_{L3}

Γ_{S1}	12.548+j37.103
Γ_{L1}	20.701+j53.987
Γ_{S2}	10.574+j37.688
Γ_{L2}	15.828+j51.017
Γ_{S3}	10.574+j37.688
Γ_{L3}	15.828+j51.017

Table 11 List of each complex reflection coefficient for the designed LNA

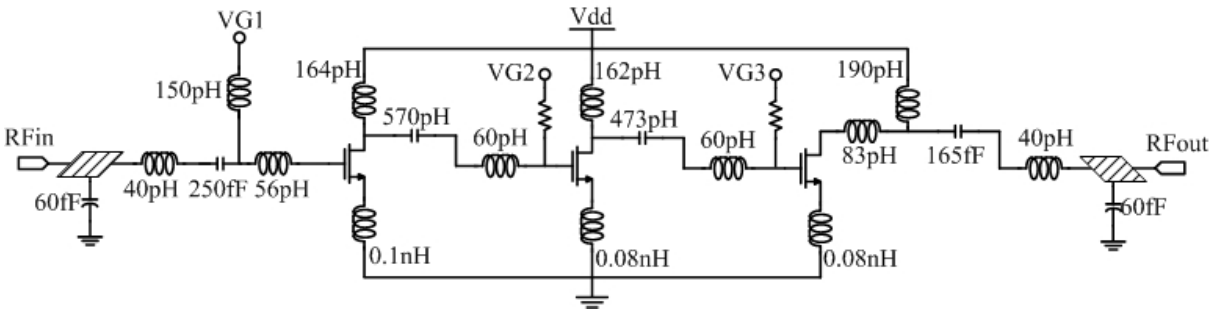


Fig. 3-27 The proposed 24-GHz LNA

3.3.6 The simulation results with ideal and on-chip inductors

The designed architecture above is simulated by the simulator ADS2004A, and the transmission lines as well as inductors are simulated by the EM simulator sonnet9.52. The ideal lump components are used, and the results are so called pre-simulation. Each transmission lines are simulated and the 'sNp' files are extracted from the simulation results. The ideal lump components are replaced with the 'sNp' files, and the simulation results are so called post-simulation. Fig. 3-28~Fig. 3-34 show the simulation results of both pre-simulation and post-simulation. The S-parameter of the pre-simulation matches our design condition illustrated above. But the post-simulation shows deviation especially both the T-junctions and the RF pads are used as simulation components. The 24-GHz LNA was designed first in our group, and the EM simulator is first applied to the design. Therefore, the 24-GHz LNA is treated as a test key for further simulation and design in the future. The post-simulation doesn't meet our desired standards of operating in 24-GHz, however, the confirmation of simulation and measurement results is the other design goal in this project. The simulated data in Fig. 3-28 ~ Fig. 3-31 revels that the best operation point shifts to 27-GHz. Both the input and output return losses of the post-simulation are higher than 10dB, and the power gain is about 13dB. Because the LNA is constructed of three stages, the reverse isolation performs well above 30dB. The noise figure exhibits about 4.5dB. With this simulated low noise figure, this designed LNA has competition with the GaAs-based HEMT and HBT technology. The simulated 1-dB compression point (P1dB) and 3rd order intercept point (IIP3) shows well linearity, and they are -12.8dBm and -4dBm, respectively. The post-simulation results are summarized in Table 12.

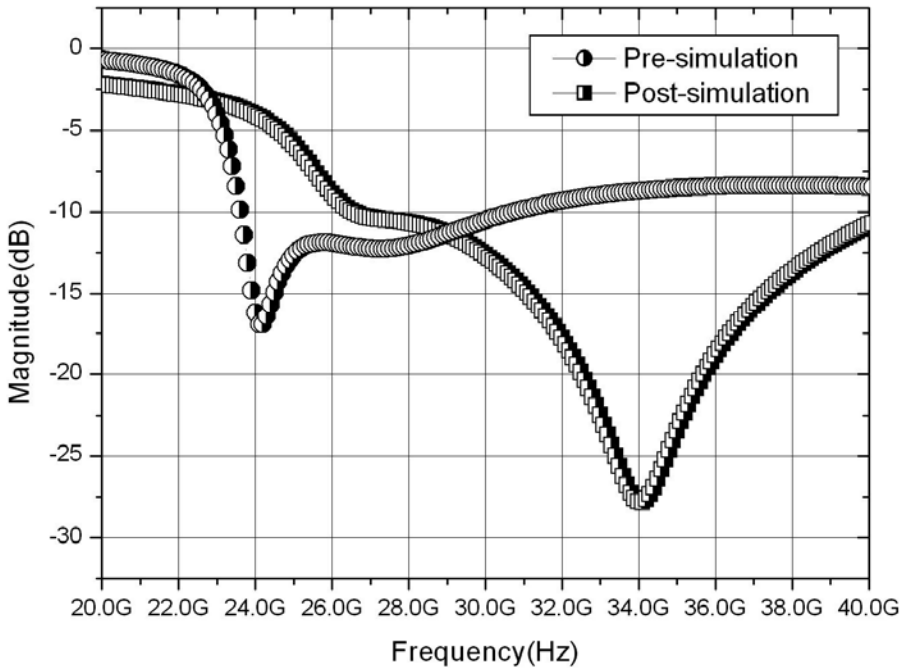


Fig. 3-28 The S11 simulated results of the proposed LNA

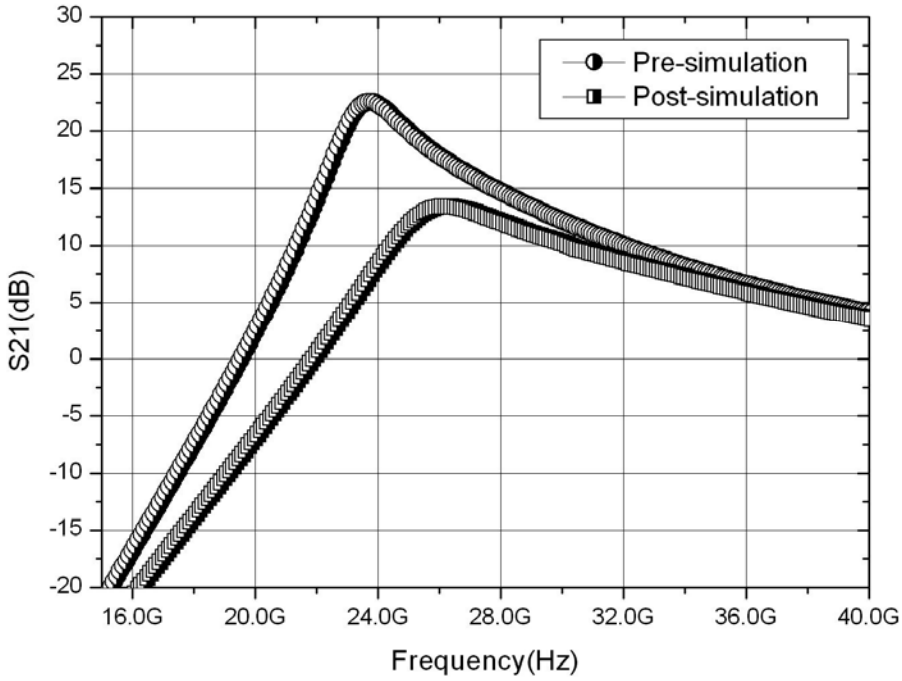


Fig. 3-29 The S21 simulated results of the proposed LNA

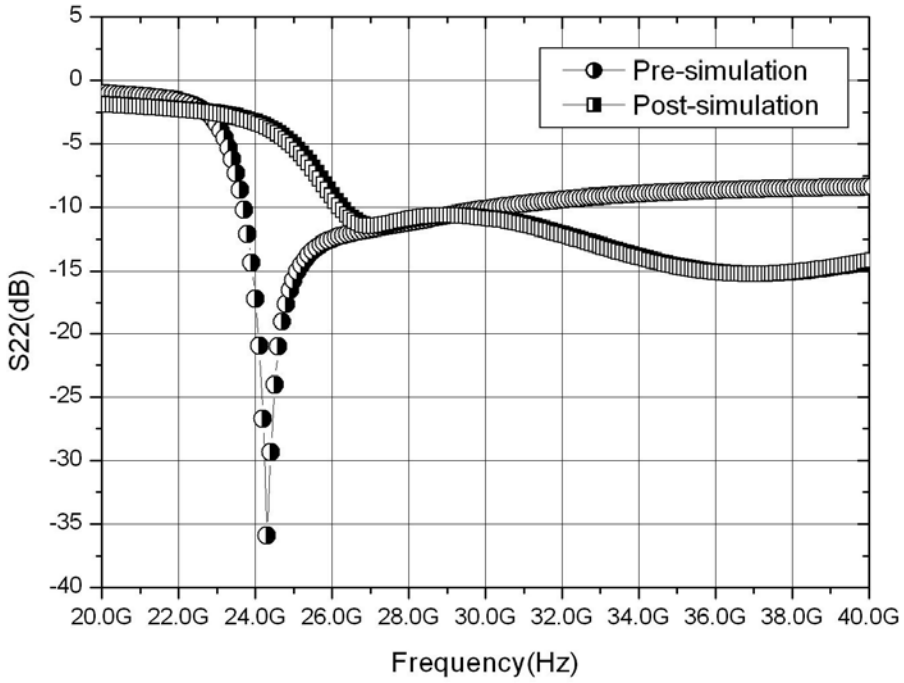


Fig. 3-30 The S22 simulated results of the proposed LNA

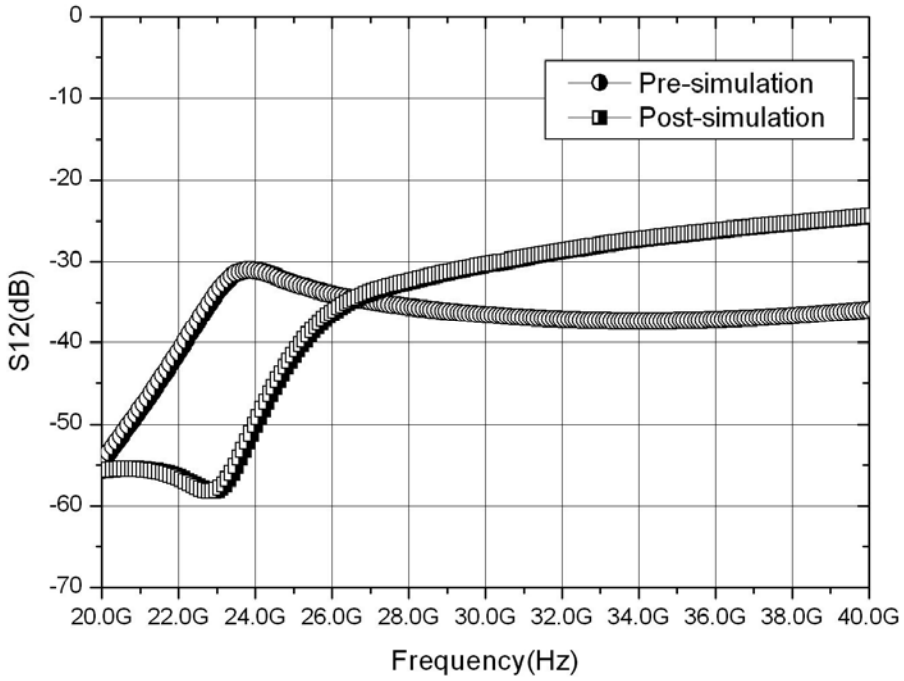


Fig. 3-31 The S12 simulated results of the proposed LNA

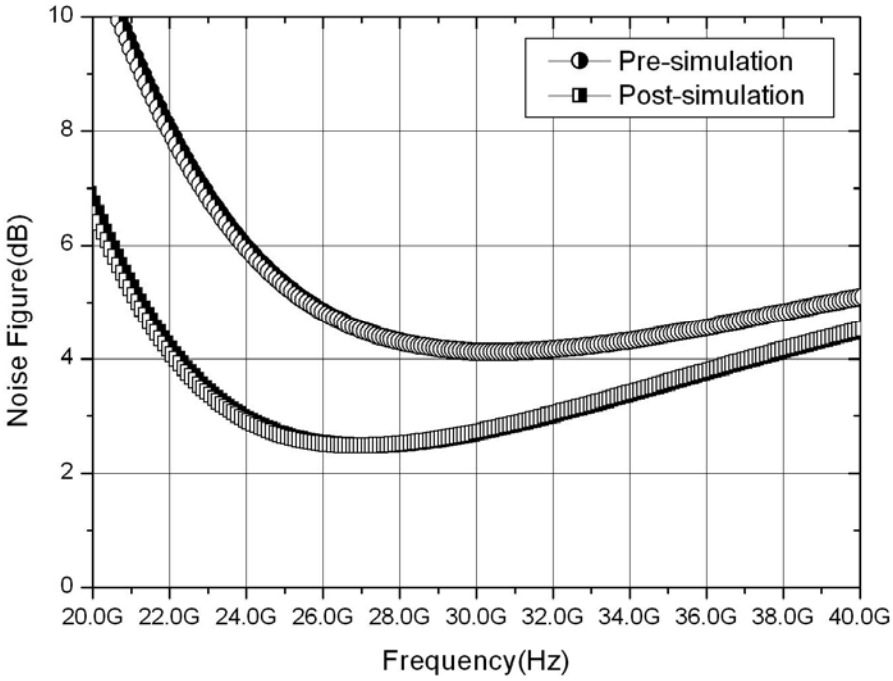


Fig. 3-32 The Noise Figure simulated results of the proposed LNA

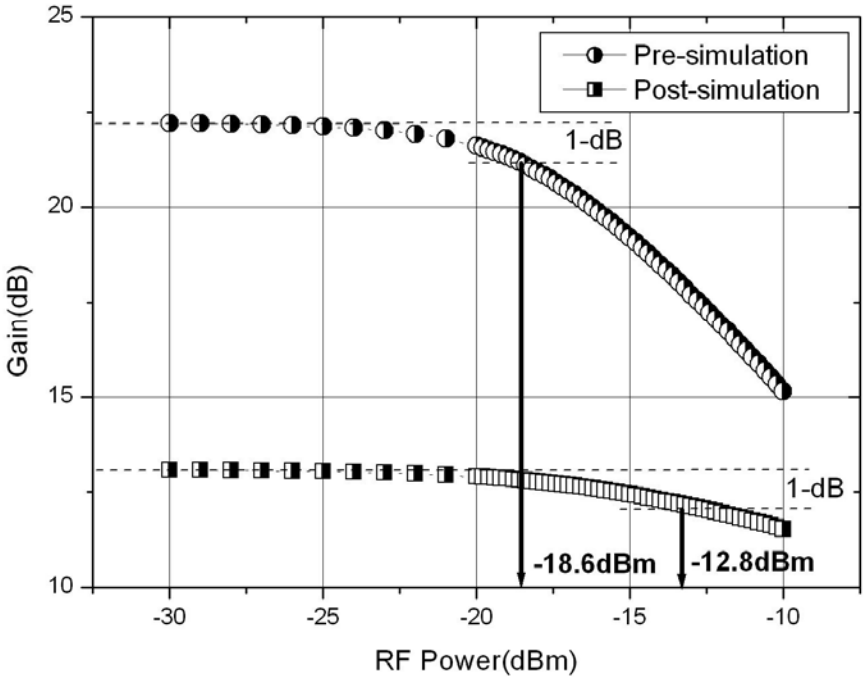


Fig. 3-33 The P1dB simulated results of the proposed LNA

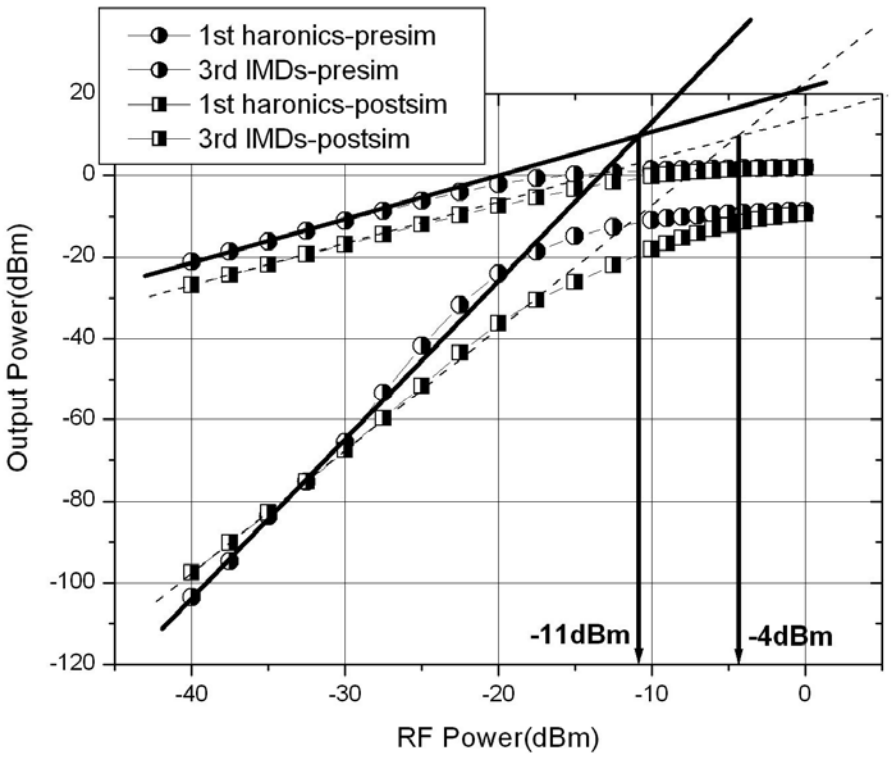


Fig. 3-34 The IIP3 simulated results of the proposed LNA

	(Pre-simulation)	(Post-simulation)
Technology	**CMOS 0.18um**	**CMOS 0.18um**
Center frequency	**24GHz**	**27GHz**
Vdd	**1V**	**1V**
S21	**22.35dB**	**13.005dB**
P1dB	**-18.6dBm**	**-12.8dBm**
IIP3	**-11dBm**	**-4dBm**
S11/S22(dB)	**-16.21/-17.23**	**-10.38/-10.50**
power dispassion	**11.85mW**	**11.85mW**
NF	**2.94dB**	**4.5dB**

Table 12 The pre-simulation and post simulation summary of the proposed LNA

3.4 Measurement Consideration and Results

3.4.1 Measurement Consideration

The 24-GHz LNA is designed for on-wafer measurement and prepared to test by CIC and Nation Center University. The layout follows the rules of CIC for testing. By the layout shown in Fig. 3-35, the LNA required two 3-pin DC probes for upper and lower side. Tow RF GSG probes are also required for RF signal, and they are posited left and right side. Fig. 3-36 is the fabricated die photo of the proposed 24-GHz LNA. The probing setup for on-wafer measurement is shown in Fig. 3-37.

The environment setups for each parameter are shown in Fig. 3-38 (a~c). The measurement instruments including network analyzer, noise analyzer are provided by CIC, and the linearity parameters are measured in Nation Center University.

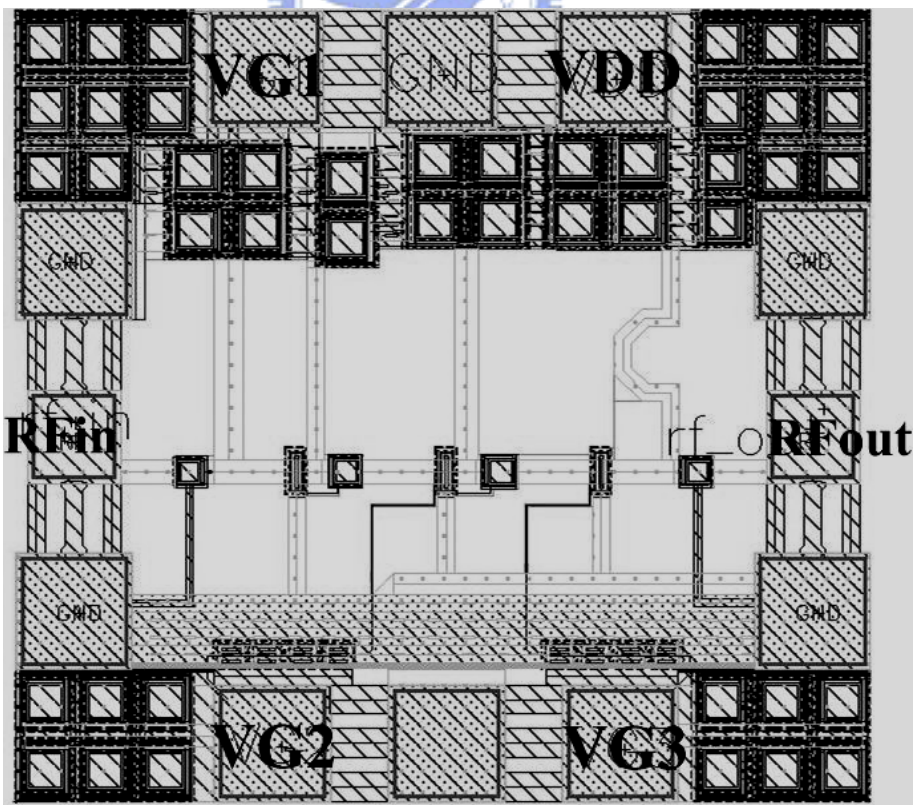


Fig. 3-35 The layout view of the proposed 24-GHz LNA

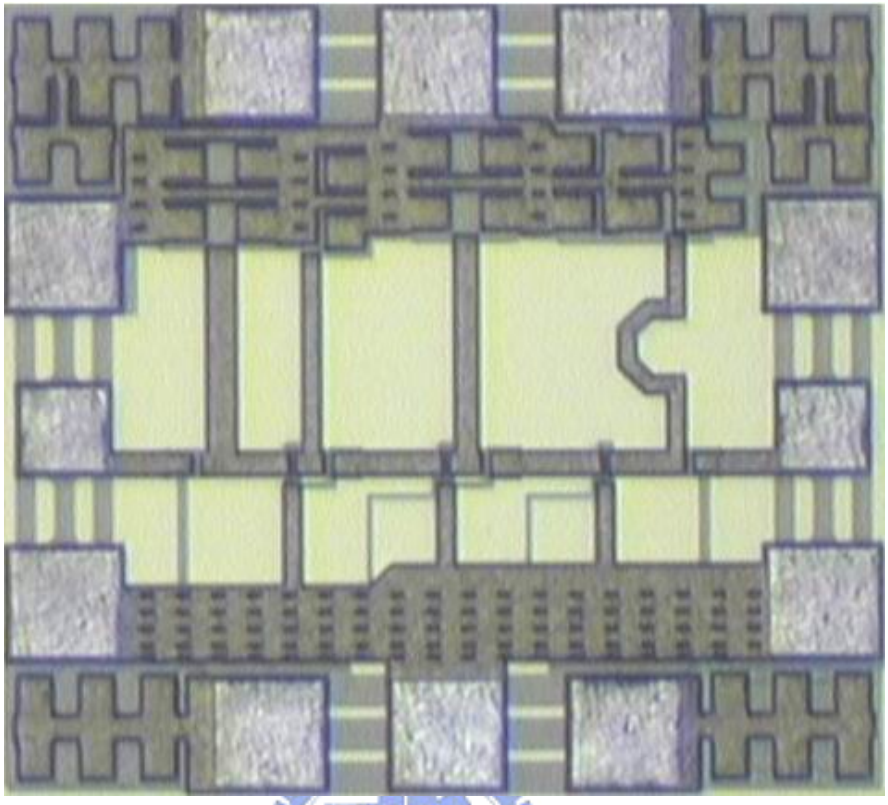


Fig. 3-36 The micrographic of the proposed 24-GHz LNA

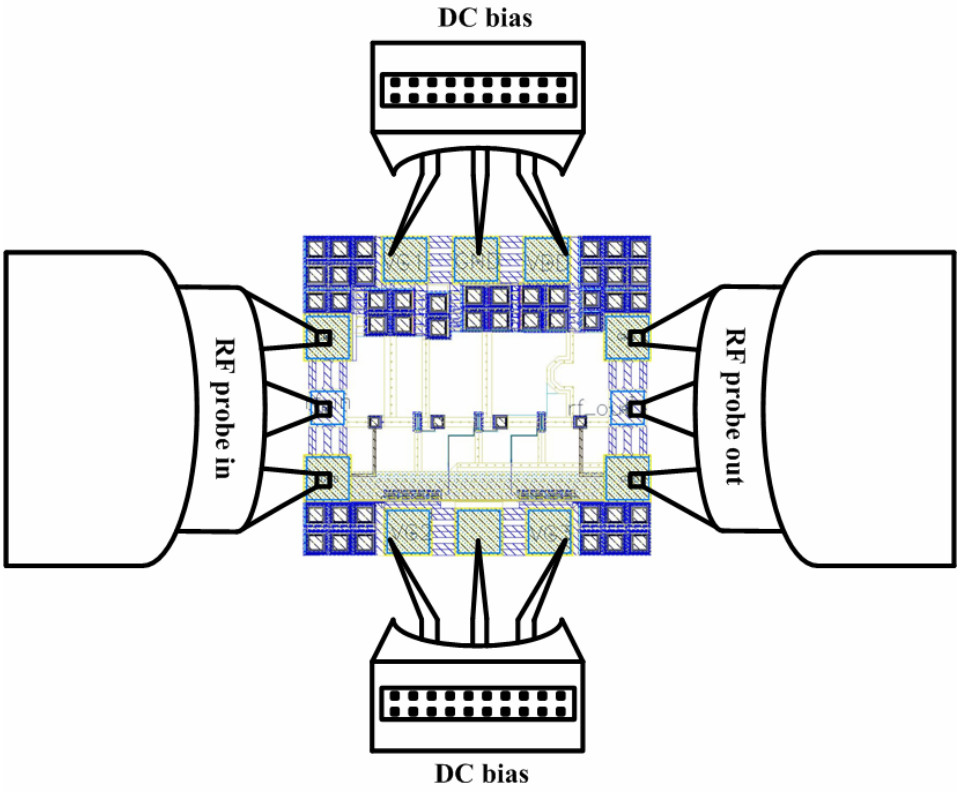
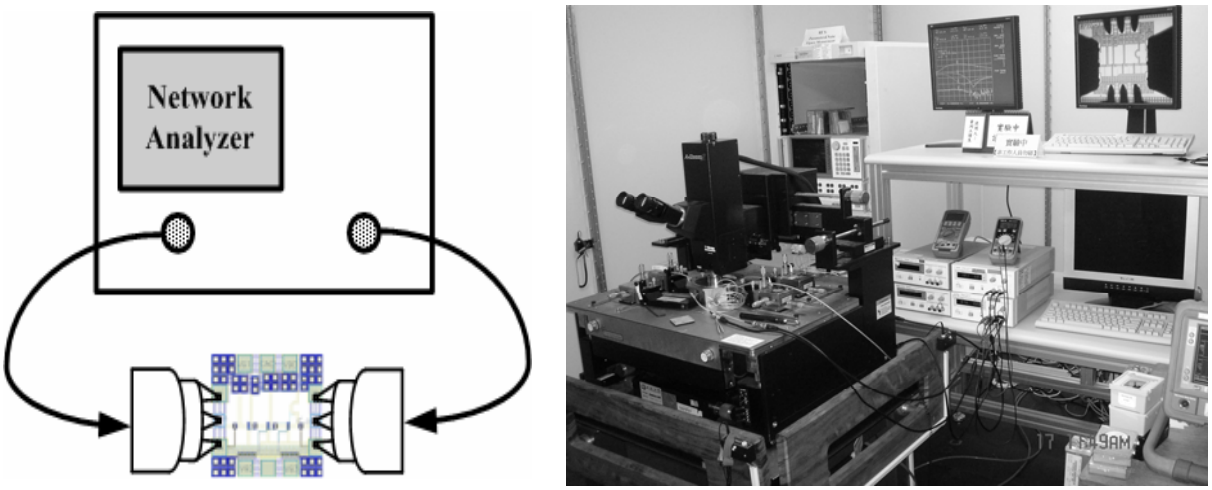
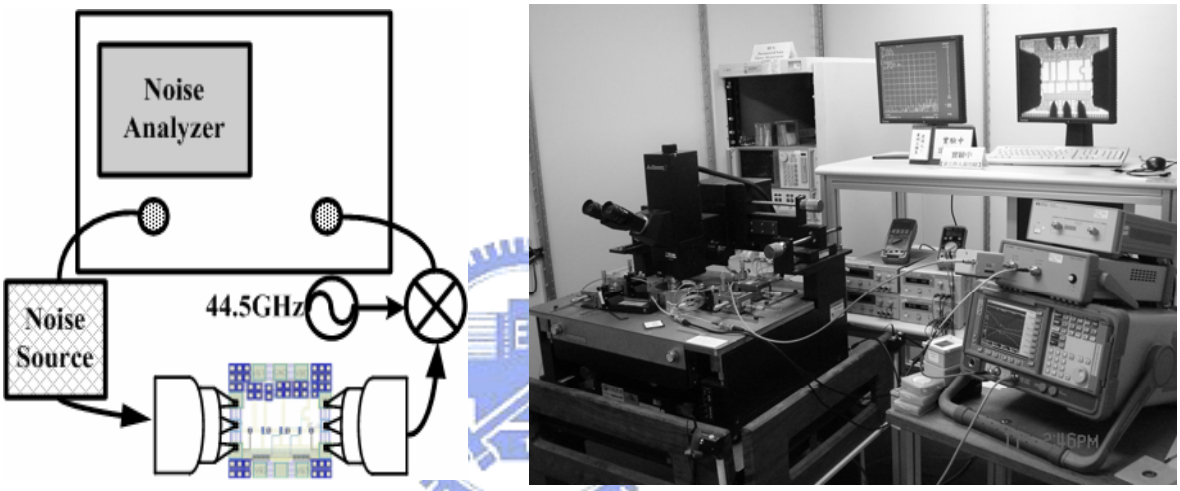


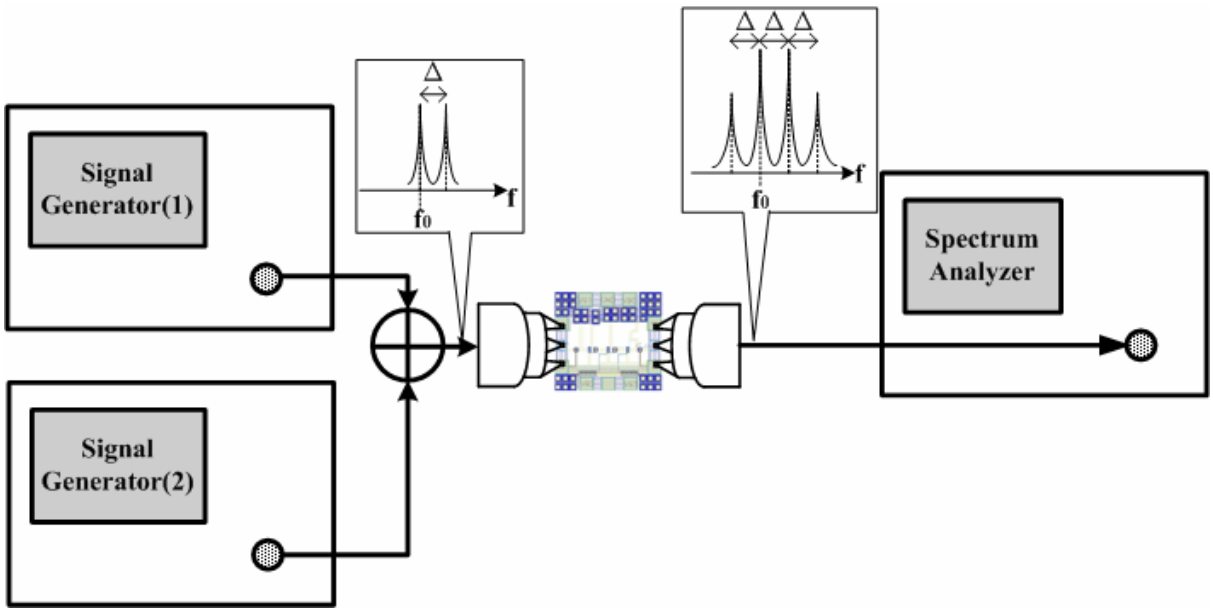
Fig. 3-37 Probing setup for on-wafer measurement



(a)



(b)



(c)

Fig. 3-38 Measurement setups of (a) S-parameter (b) noise figure (c) IIP3 and P1dB

3.4.2 Measurement Results and Discussion

The operating frequency of the post-simulation is about 27-GHz, however, the measured results shift to about 32-GHz. To show the deviation between the post-simulation and measured results, each parameter is plotted on the same figure. The calibration of the 2-port network analyzer is difficult for frequency above 30-GHz, therefore, the measured curve is slightly unsettled above 30-GHz. As shown in Fig. 3-39~ Fig. 3-44, the measured S-parameter shows that the 3-stage LNA achieves high power gain of 12.08dB, and a 5.325dB noise figure is accomplished at 32-GHz. The input and output return losses also shifts from 27-GHz to 32-GHz. At 32-GHz, the measured S11 and S22 are -6.3dB and -20.67dB, respectively.

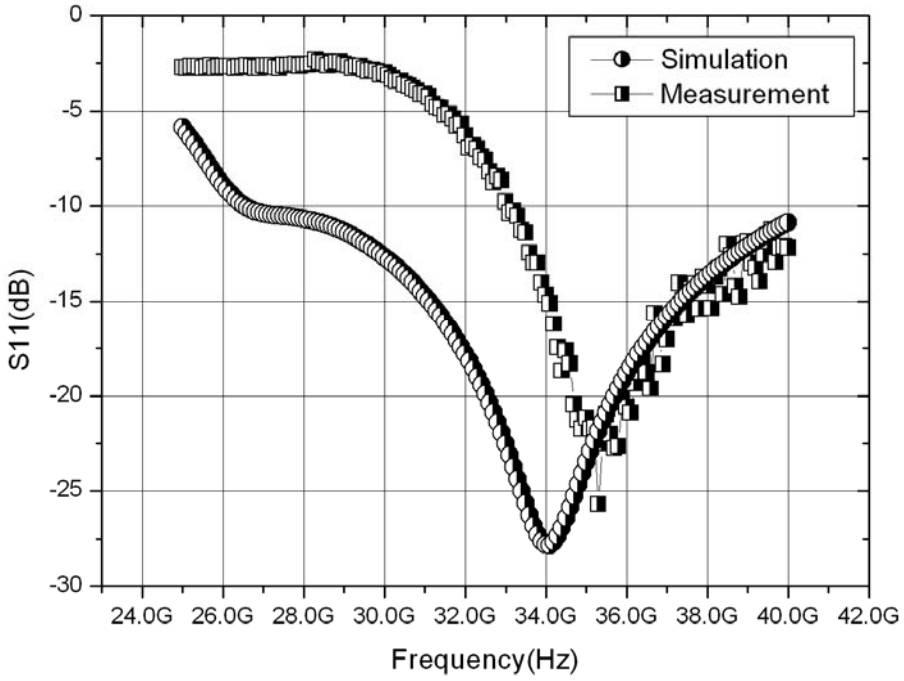


Fig. 3-39 Post-simulation and measurement of S11

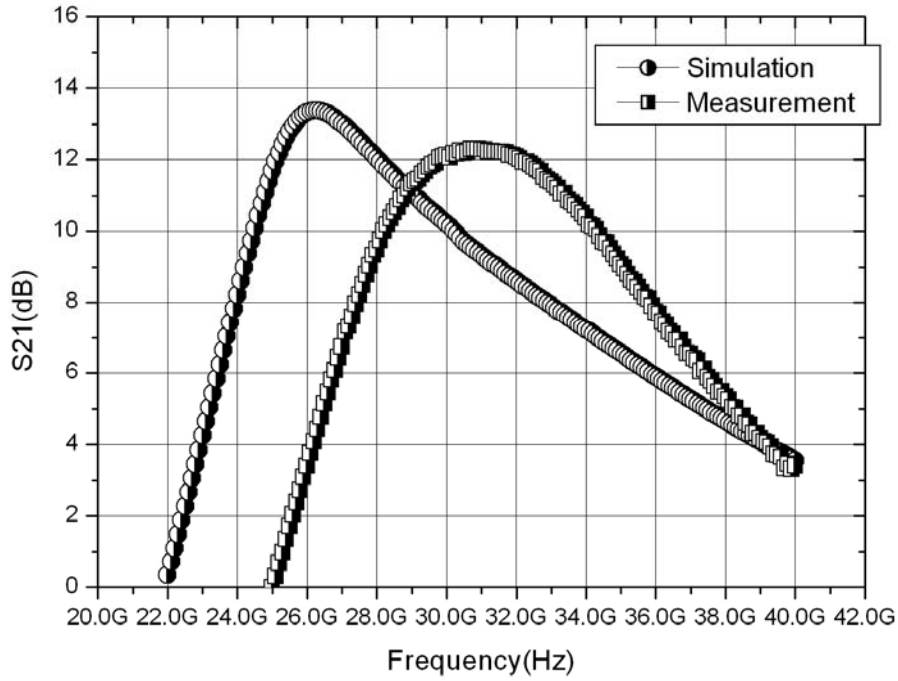


Fig. 3-40 Post-simulation and measurement of S21

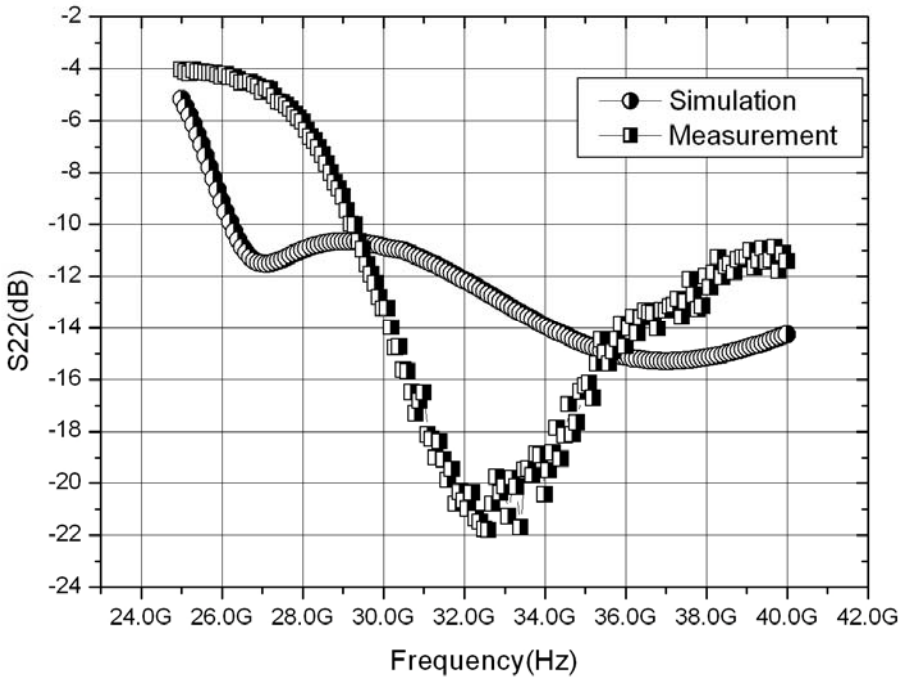


Fig. 3-41 Post-simulation and measurement of S22

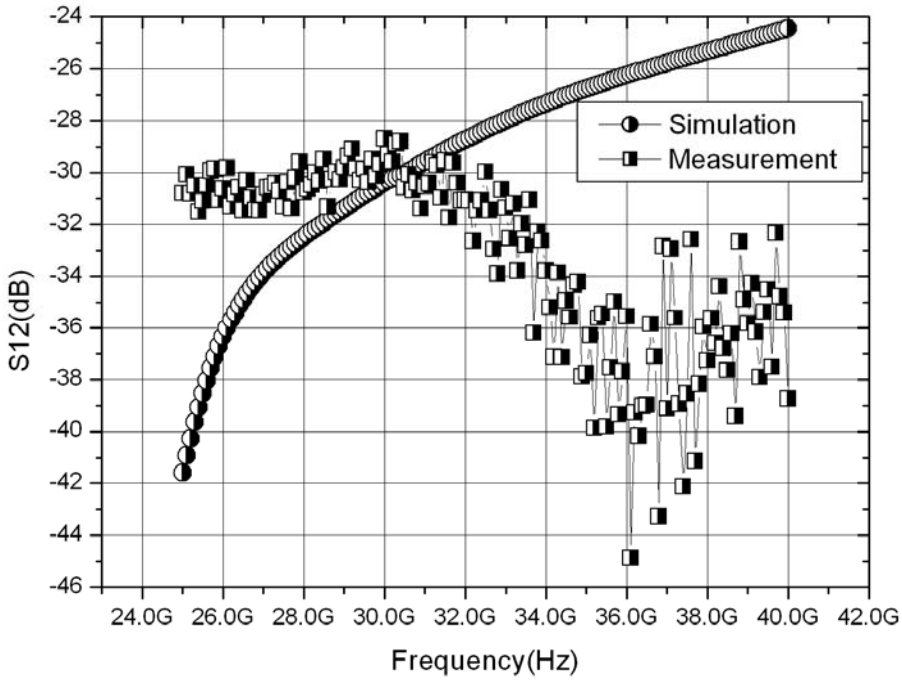


Fig. 3-42 Post-simulation and measurement of S12

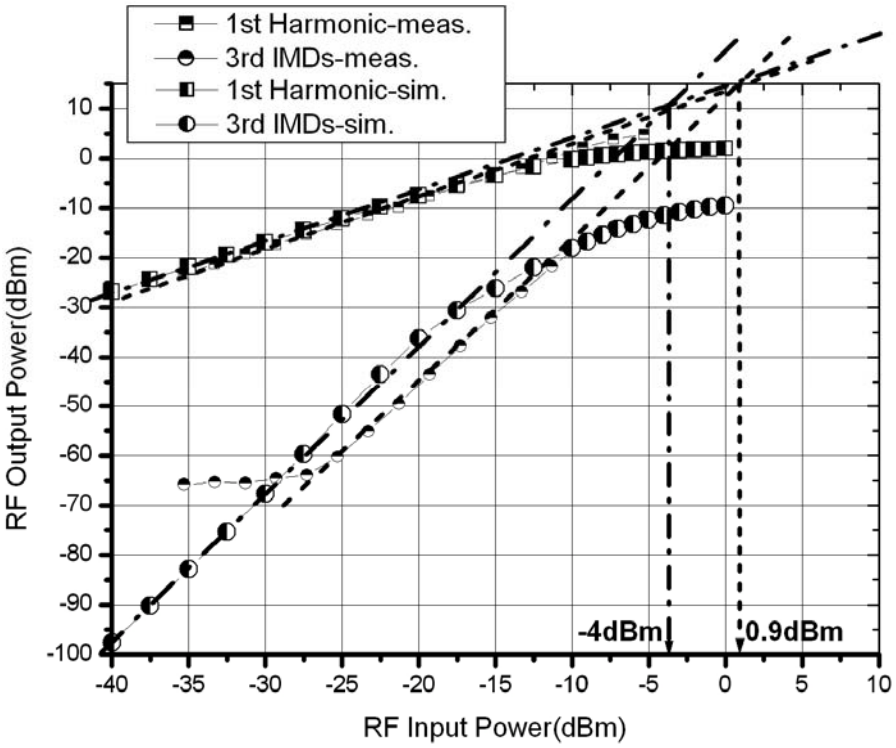


Fig. 3-43 Post-simulation and measurement of IIP3

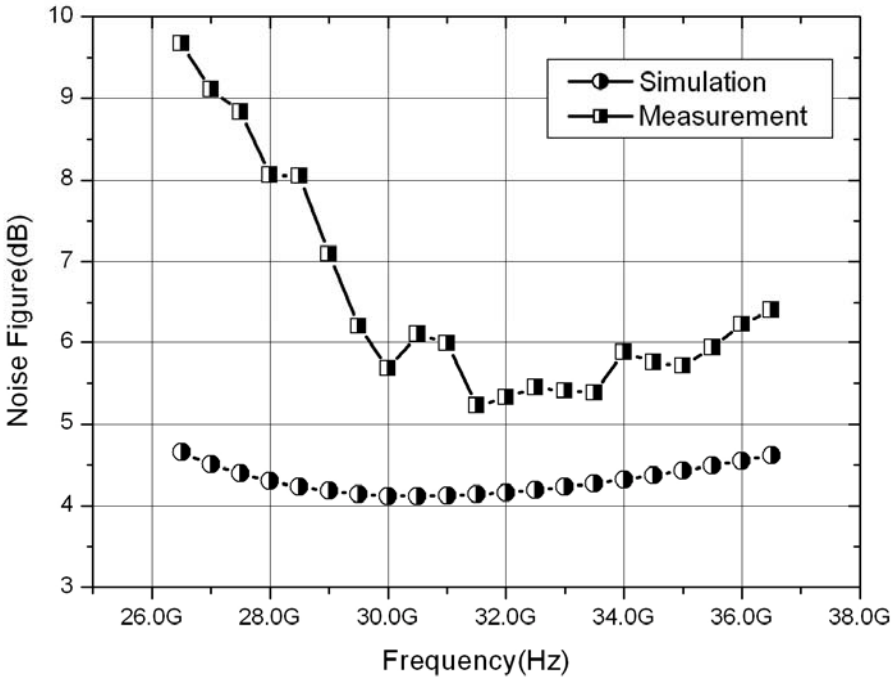


Fig. 3-44 Post-simulation and measurement of Noise Figure

	(Measurement)	(Post-simulation)
Technology	**0.18um CMOS**	**0.18um CMOS**
Center frequency	**32GHz**	**27GHz**
Vdd	**1V**	**1V**
S21	**12.08dB**	**13.005dB**
P1dB	**-11dBm**	**-12.8dBm**
IIP3	**0.9dBm**	**-4dBm**
S11/S22(dB)	**-6.3/-20.67**	**-10.38/-10.50**
power dispassion	**15.58mW**	**11.85mW**
NF	**5.325dB**	**4.5dB**

Table 13 Summary of the post-simulation and measurement

The post-simulation results are completed by simulating all transmission lines including

all T-junction. However, the coupling form line to line is difficult to take into account. The main reason is the restriction of EM simulator (sonnet9.52). Each port of the transmission line must be at the boundary of a rectangle, and this restriction confines the dimension of simulation. This coupling will cause parasitic capacitance and mutual inductance and hence the measured results are different from the post-simulation.

3.4.3 Comparison with Other Literatures

	This Work (Meas.)	[34] 2004 JSSCC	[35] 2004 MWCL	[36] 2005 MWCL	[37] 2004 RFIC
Technology	**CMOS 0.18um**	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um	CMOS 90nm
Center frequency	**32GHz**	21.8GHz	23.7GHz	24GHz	20GHz
Vdd	**1V**	1.5V	1.8V	1V	1.5V
S21	**12.08dB**	15dB	12.86dB	13.1dB	5.8dB
S11/S22(dB)	**-6.3/-20.67**	--/--	-11/-22	-15/-20	-20/-20
power dispassion	**15.58mW**	24mW	54mW	14mW	10mW
NF	**5.325dB**	6dB	5.6dB	3.9dB	6.4dB

Table 14 Measured results and comparison with other literatures

The comparison with recent published literatures is listed in Table 14. By CMOS 0.18um technology, this measured LNA with highest operating frequency ever reported performs 12.08 dB power gain and consumes 15.58mW from 1V power supply. Comparison shows this work consumes less power and has competition with other works. The well performed noise figure shows the noise matching is realized, however, there are still some improvements

required for this work. This work also demonstrates that 0.18um CMOS process has potential to implement above 30-GHz LNA. In our feature work, a better device size choice and source degeneration size selection is the main target for above 30-GHz. In addition, different EM simulators are requested to the feature works.

3.5 Conclusion

Recent works have shown CMOS as a promising means for building RF circuits in the low-gigahertz range. However, a high-performance CMOS front-end for applications above 20GHz has been reported and the performance of these CMOS circuits show CMOS process has potential for building RF systems above 20GHz.[34]~[36]. In this work, a 24-GHz low noise amplifier is designed, and the measured results shows the LNA achieves 12 dB gain at 30-GHz. By the CMOS 0.18um technology, this work presents the highest operating frequency compared with the reported literatures. The best matching point of the measured input return loss does not locate at 30-GHz, however it achieves -21 dB at 35-GHz. This deviation not only causes the gain lower than the desired one but also influences the noise figure performance. The frequency shift in this project is about 3-GHz form 27-GHz to 30-GHz. This phenomenon is observed in our simulation. The T-junction and the RF-pad are the issue in the EM simulation. The transmission lines as well as inductors in this project are simulated precisely. But the T-junction does not take into account. If the T-junctions are simulated, the frequency shift phenomenon appears. The RF pad and the input matching network are critical issues to the noise figure performance. The realistic RF pad and passive components contribute about 1.5 dB noise figure than the ideal passive components. These two problems are needed to overcome, and different EM simulators will be necessary to the high frequency simulation in the future for coupling affection.

Chapter 4
K BAND FREQUENCY SOURCE WITH X BAND LOW PHASE NOISE QUADRATURE CMOS VCO

4.1 Introduction

Using standard CMOS process to implement millimeter-wave frequency sources had garnered more and more attention and became a tendency by the reason of low cost and high integration ability with other analog and digital circuits. The on-chip inductors with low-Q are the main defect for Si substrate and influence the phase noise directly. However, many recently published literatures of Si-based VCOs had demonstrated their competition with the GaAs process [39]~[44].

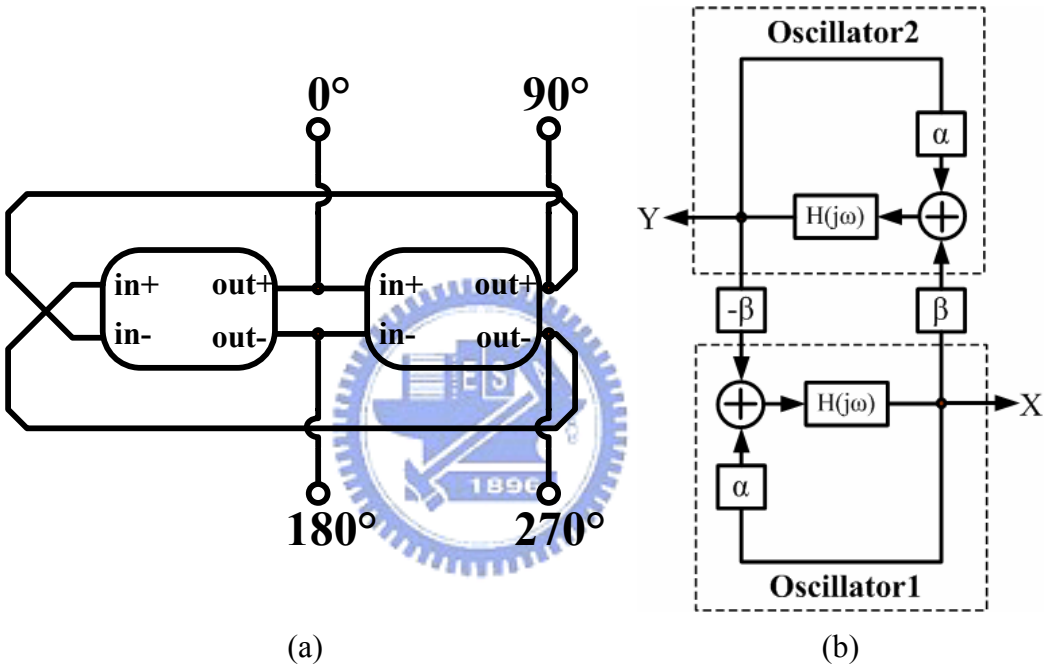
Above X band, a CMOS VCO with high performances is difficult to design. With a little increment of power consumption, frequency doubling scheme is the reasonable and effective approach to improving performance. There are several reasons to use a lower frequency oscillator with a frequency doubler instead of an oscillator operating at a higher frequency. Generally, the phase noise of the latter is higher than that of the former. Furthermore, the usage of a frequency doubler mitigates the design difficulty of a high-frequency phase-locked loop (PLL). In general, a VCO has an oscillation frequency up to $\sim f_{\max}$ and a frequency divider operates approximately up to 1/4~1/2 of f_T. It is very difficult to increase the operating frequency of a frequency divider up to the output of a high-frequency VCO.

A pair of differential signals of $2\times f_0$ can be realized by a balanced doubling method. To get a high-quality signal of a frequency doubler, accurate quadrature signals with low phase noises are required. A simple method to obtain accurate quadrature signals with low

phase noises is to couple two symmetric *LC*-tank VCOs [41]. Several quadrature VCOs had been implemented and demonstrated in the X-band [39]~[44]. Hence, a K band CMOS frequency source with X band low phase noise quadrature VCO will be presented.

4.2 Circuit Design

4.2.1 Quadrature Signal



(a) (b)

Fig. 4-1 Quadrature VCO architecture (a) connection of blocks (b) Transfer characteristic

Fig. 4-1 (a)(b) show the quadrature VCO architecture. The quadrature phase VCO comprises two mutually-coupled fixed frequency LC-oscillators. Frequency tuning is achieved by varying the coupling coefficient (β) between two oscillators. Oscillation frequency is adjusted along with loop gain compensation (α). This mechanism ensures that current injected into LC tank remains constant regardless of frequency tuning. Thus AM-to-PM phase noise conversion can be suppressed [41]

Consider two fixed-frequency LC oscillators whose outputs are coupled to their inputs with the coupling coefficients β and -β, as shown in Fig. 4-1. Each oscillator is modeled by a

positive feedback loop with open loop gain H(jω). In steady-state, and if the two oscillators synchronize to a single oscillation frequency, **ω,** the output of each oscillator must satisfy the following equations:

$$(\alpha X - \beta Y)H(j\omega) = X \tag{4.1}$$

$$(\alpha Y + \beta X)H(j\omega) = Y \tag{4.2}$$

It can be proven that

$$X = \pm jY \tag{4.3}$$

This proves that the oscillatory system of Fig. 4-1 indeed provides quadrature outputs X and Y. By substituting equation (4.3) into equation (4.2), equation (4.4) can be derived.

$$(\alpha \pm j\beta)H(j\omega) = 1 \tag{4.4}$$

Equation (4.4) governs the frequency transfer characteristic of the quadrature phase VCO. As the close loop phase response of these oscillators is varied by adjusting α/β, VCO's output frequency can be changed accordingly.

4.2.2 Frequency Doubler

4.2.2.1 *Harmonics of Quadrature Signals*

A VCO exhibits a strong nonlinear effect by the reason of the large output swing in the resonator. Since the nonlinear effect is related to many different physical phenomena, it cannot be modeled easily [39]. The output of a VCO now is modeled simply as a polynomial

$$V_{out} = A_0 + A_1 X + A_2 X^2 + ... \tag{4.5}$$

where the A_n's are the harmonic coefficients and X is the input signal. If X is substituted by $\cos(\omega t + \theta)$, then equation (4.5) can be derived as equation (4.6):

$$V_{out} = (A_0 + \frac{A_2}{2} + \frac{A_4}{2}) + (A_1 + \frac{3}{4}A_3)\cos(\omega t + \theta) + (\frac{A_2}{2} + \frac{A_4}{2})\cos(2\omega t + 2\theta) + (\frac{A_3}{4})\cos(3\omega t + 3\theta) + ... \tag{4.6}$$

If the four quadrature signals with the different phases of a quadrature VCO are inserted into

(4.6), and fundamental frequency components are canceled out by adding two output signals with an input phase difference of 180°. A frequency-doubled differential signals are obtained and it follows:

$$V_{out}(\cos(\omega t)) + V_{out}(\cos(\omega t + \pi)) \approx 2(A_0 + \frac{A_2}{2}) + A_2\cos(2\omega t) + ... \quad (4.7)$$

$$V_{out}(\cos(\omega t - \frac{\pi}{2})) + V_{out}(\cos(\omega t + \frac{\pi}{2})) \approx 2(A_0 + \frac{A_2}{2}) + A_2\cos(2\omega t + \pi) + ... \quad (4.8)$$

The results show that a set of quadrature signals can create a pair of differential output with doubled-frequency, $2 \times f_0$.

4.2.2.2 *Pinch-off Clipping*

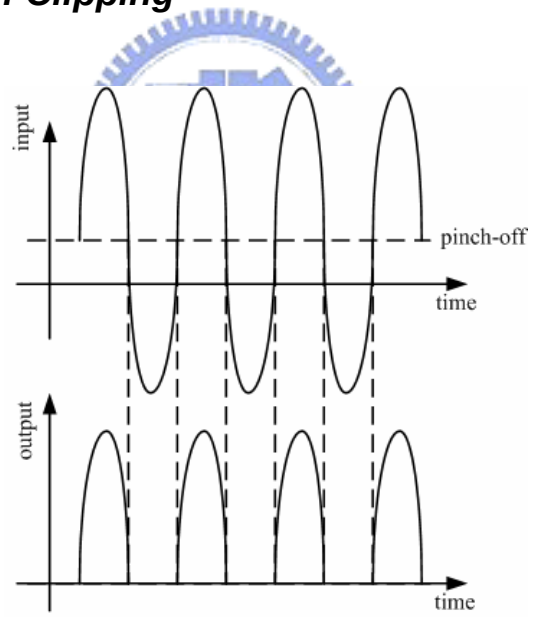


Fig. 4-2 Output signal of a pinchoff clipper derived by an input sinusoidal signal with low dc bias.

The device nonlinearity of a negative conductance cell mainly influences harmonics. Since a MOSFET has high linearity and low f_T, the harmonics of a MOS VCO are too small to use as a signal source, even though output power is increased by the push–push method. Thus, some nonlinearity operation must be introduced to increase the nonlinear terms.

Pinch-off clipping is a common method to increase harmonic power and the waveform of nonlinear operation is shown in Fig. 4-2. The output power can be thought of multiplying a square wave and a cosine wave. And this phenomenon can be represented as follows:

$$V_o = V_1 \cdot V_2 = [A_0 \cos(\omega t + \theta)]\left[B_0 + \sum_{n=1}^{\infty} B_n \cos\{(2n+1)\omega t + (2n+1)\theta\} \right]$$

$$= A_0 B_0 \cos(\omega t + \theta) + \sum_{n=1}^{\infty} \frac{A_0 B_n}{2} \left[\cos\{(2n)\omega t + (2n)\theta\} + \cos\{2(n+1)\omega t + 2(n+1)\theta\}\right] \quad (4.9)$$

If the driven signals have 180° phase difference and we combine these according two outputs, the output summation can be derived as follow:

$$V_{sum} = \sum_{n=1}^{\infty} A_0 B_n [\cos\{2n\omega t\} + \cos\{2(n+1)\omega t\}] \quad (4.10)$$

The results show that a pinch-off clipping can create a signal with doubled-frequency, $2 \times f_0$.

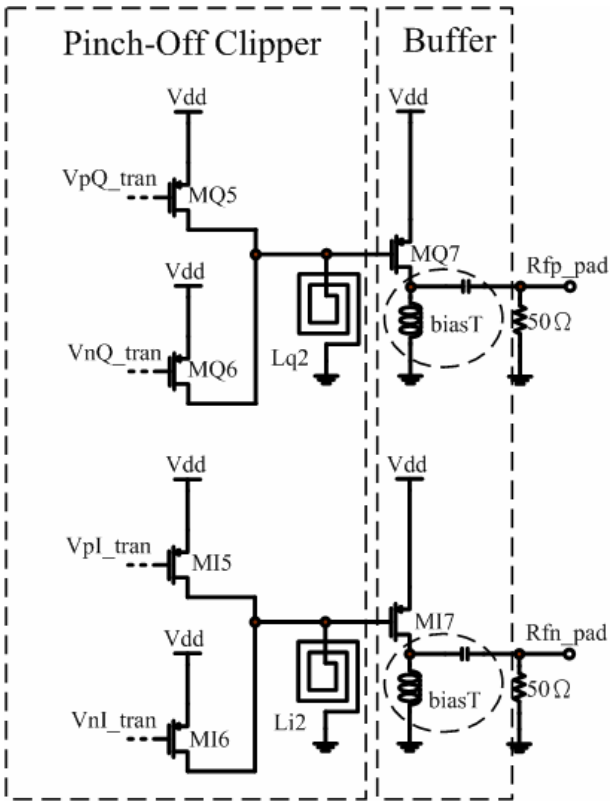


Fig. 4-3 The pinch-off clipping circuit used as a doubler in this project

The pinch-off clipping method is generally realized by driving a MOSFET with large signals. Fig. 4-3 shows the balanced pinch-off clipping circuits used in this project. Four PMOS transistors and two load inductors compose this clipper. And these PMOS transistors

are driven by a set of quadrature signal form QVCO illustrated in next section. Two inductors are served as loading of the summation signal. Buffers are required for the consideration of measurement. Two bias-T networks are also used at the output of MQ7 and MI7. By the simulation results, these two balanced clippers consume totally about 4.9mW.

4.2.3 Proposed K Band VCO Architecture

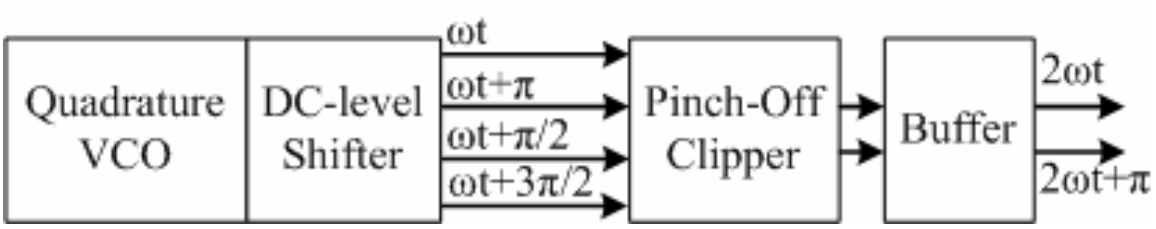


Fig. 4-4 Block diagram of the K band frequency source

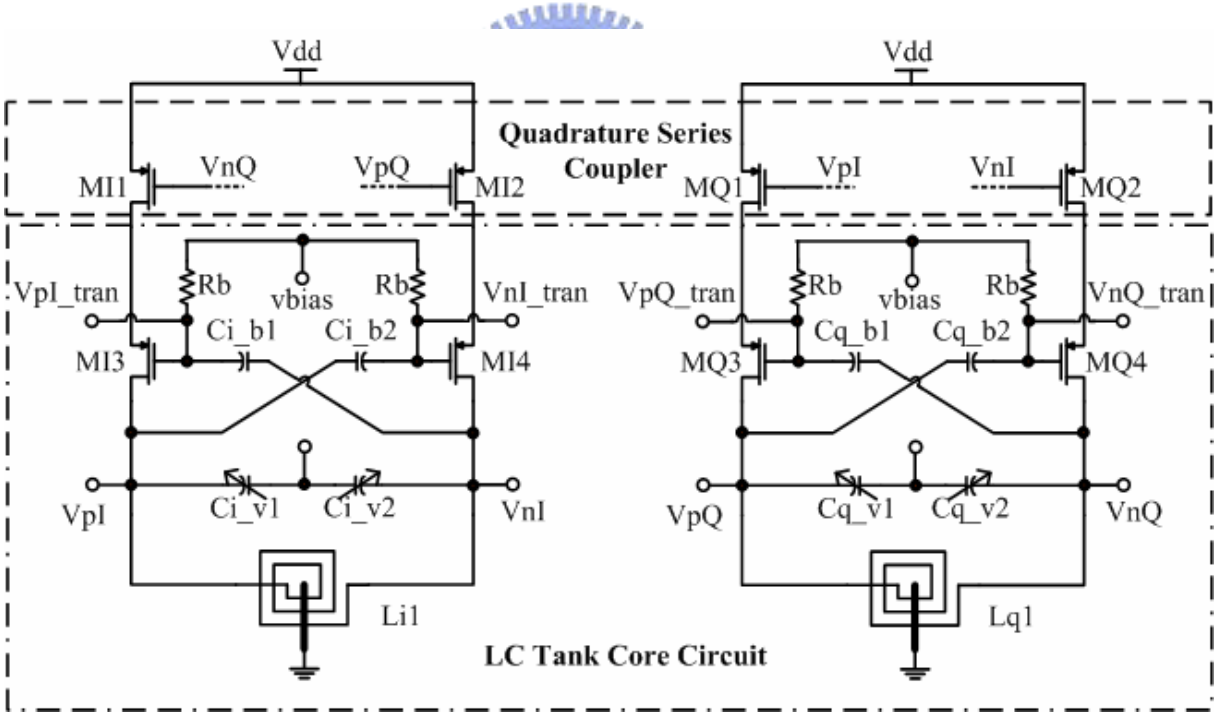


Fig. 4-5 The proposed quadrature voltage controlled oscillator.

Fig. 4-4 shows block diagrams of a balanced frequency doubler and quadrature VCO. The pinch off clipper is requested to increase the power of harmonics. The pinch off clipper in this project is constructed by PMOS transistors. Thus, the input of a pinch off clipper should

be biased at a higher dc level. However, the dc level of a VCO output is equal to the zero or half of that in a P-type or PN-type VCO. Dc level shifters are combined with the conventional P-type VCO to shift the output dc level of a QVCO at higher level. The quadrature VCO combining with dc shifter is shown Fig. 4-5.

The phase noise is a major consideration in a VCO design. The phase noise estimation has been widely discussed. For a single LC-oscillator, its phase noise can be expressed as below:

$$L\{\Delta\omega\} = 10 \cdot \log\left[\frac{8FkTR_{eff}}{V_o^2} \cdot \left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right] \tag{4.11}$$

$$F = 1 + \frac{4\gamma R_{eff} I_T}{\pi V_o} + \frac{4}{9}\gamma g_{m,tail} R_{eff} \tag{4.12}$$

Where I_T is the bias current, γ is the channel noise coefficient of the MOSFET, and $g_{m,tail}$ is the transconductance of the current source MOSFET, R_{eff} is the equal impedance of the LC tank, V_o is the amplitude of the oscillator [45].

The oscillation frequency can be roughly estimated by (4.13) [47].

$$f_{osc} = \frac{1}{\sqrt{L(C_{ind} + C_{load} + C_{MOS} + C_{\text{var}})}} \tag{4.13}$$

where C_{ind}, C_{load}, C_{MOS}, C_{var} are the parasitic capacitances of inductor, load, MOS transistor, and the varactor capacitance, respectively.

The proposed VCO has low noise due to three noise-reduction mechanisms. The negative resistance cells are all constructed by cross-coupled PMOS transistors first to lower the phase noise contributing from the flicker noise of MOSFETs.

The second is that only those cross-coupled transistors are biased in the saturation region. The transistor in the triode region exhibits low gain and low noise, while the transistor in the saturation region exhibits high gain and high noise [39]. In our proposed QVCO, MQ1 (MI1) and MQ2 (MI2) are quadratre coupling transistors and they do not need high gain. Therefore, the coupling transistors are all biased at deep triode region and their contributed noise is

negligible.

The last is the improvement of loaded Q. The biases of cross-coupled transistors in a VCO are all in a saturation region to provide negative resistance. However, these transistors are pushed into a triode region by the large output swing of a resonator for part of a period. The low output resistance of a transistor in a triode region decreases the loaded Q and hence depresses the phase noise performance. The coupling transistors are serves as current sources in this project. Even though they are not good current sources because they are biased in deep triode region. The improvement of the phase noise is similar or superior due to the absence of noise contributed from current source.

All the parameters are simulated by eldoRF and ADS2004, and the EM simulator (sonnet 9.52) is also used for post-simulation. The simulated results are shown and discussed in next section.

4.3 Simulation Results

All the simulations are based on the TSMC 0.18um CMOS technology. Fig. 4-6 shows that the proposed K band oscillator operating at 19.1-GHz, and the fundamental signal is suppressed about 45 dBc. In addition, the simulated tuning range of the VCO is 700-MHz and it is shown in Fig. 4-7. Fig. 4-8 shows the simulated phase noise, and the simulated result reveals that a phase noise of -112dBc/Hz is achieved in K band. Otherwise, the phase noise of the X band quadrature signal is also plotted, and it performs 6 dB lower than the K band. The core circuit of quadrature VCO and balanced doubler consume 10.92mW and 4.89mW, respectively. The power supply voltage is designed to be 1.5V for measurement consideration. The buffer consumes 31.679mW and the spectrum output power is about -3.5dBm. Finally, the transient waveform of K band signal source and X band quadrature signal in time domain are shown in Fig. 4-9 and Fig. 4-10, respectively. Table 15 summarizes the performance of our proposed K band VCO.

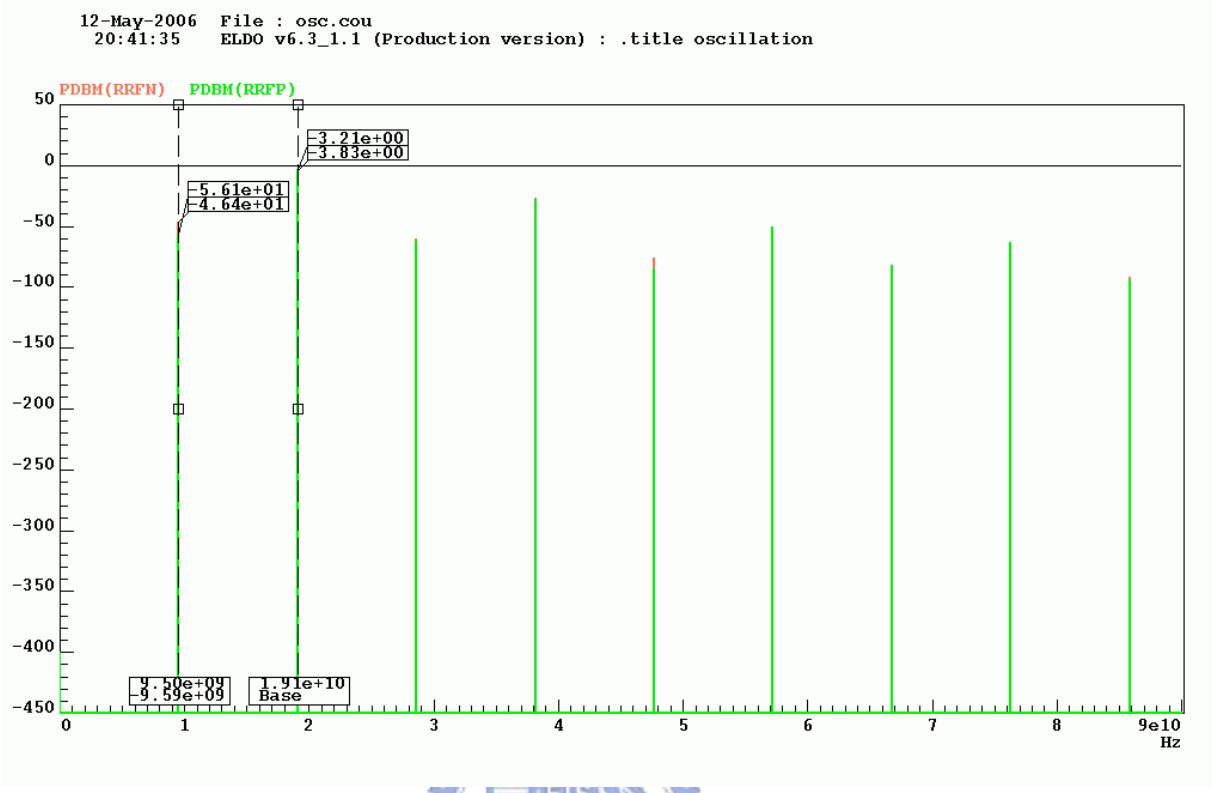


Fig. 4-6 The simulated result of output spectrum

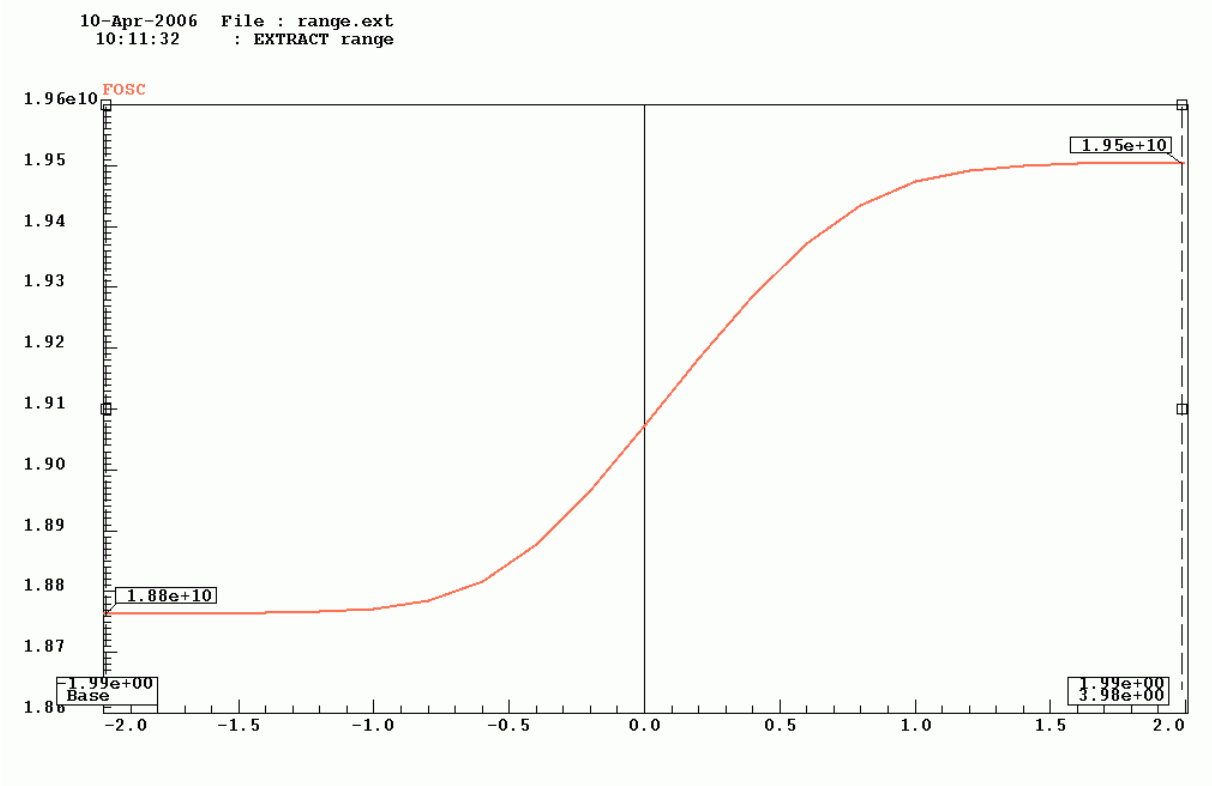


Fig. 4-7 The simulated result of tuning range

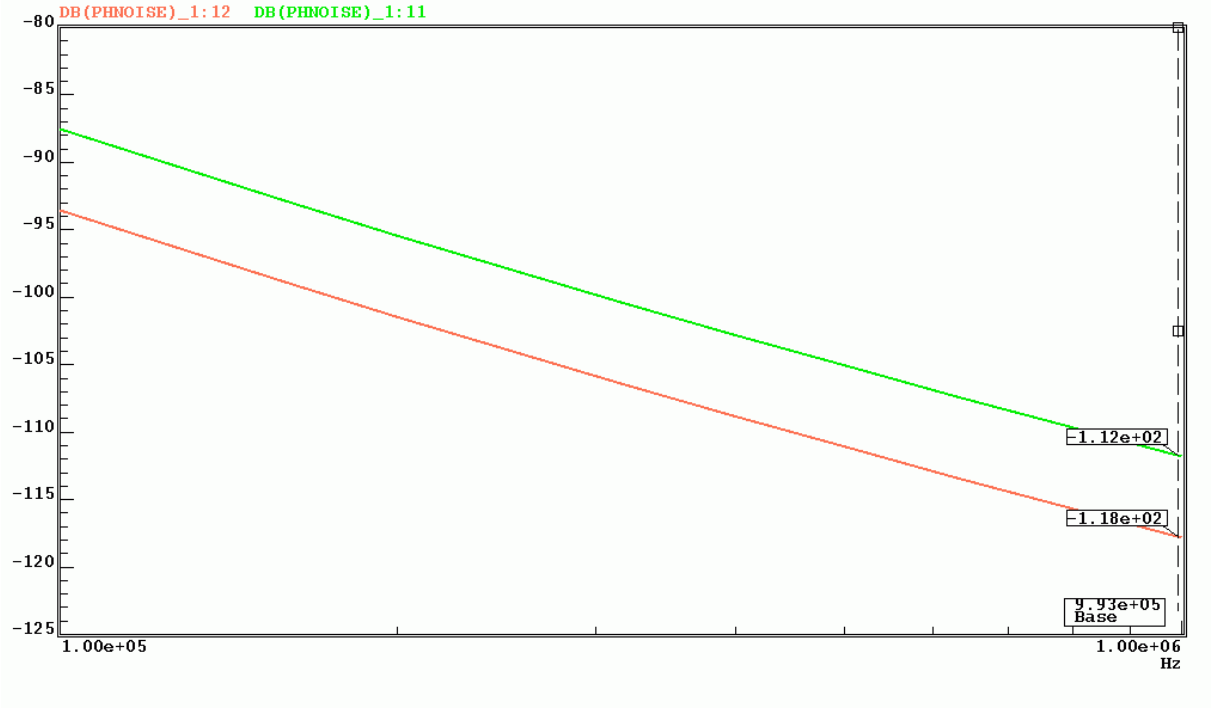


Fig. 4-8 The simulated phase noise of X band and K band signal

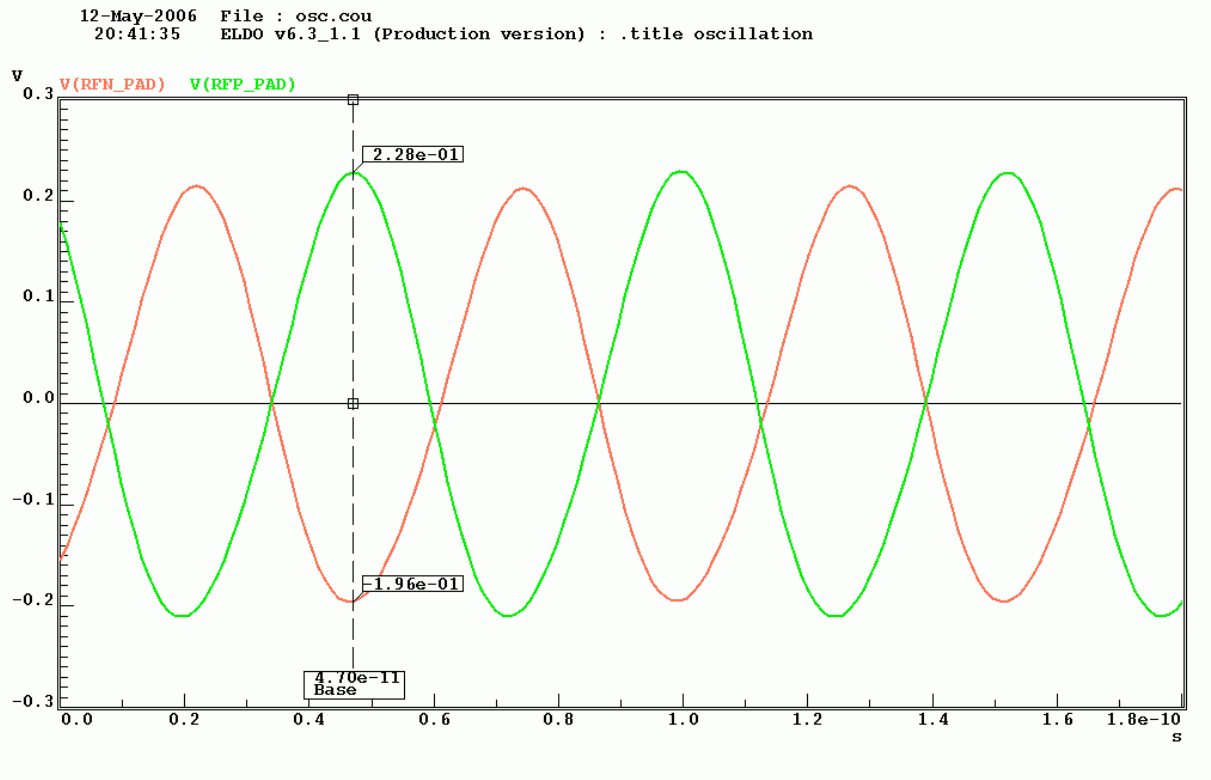


Fig. 4-9 The simulated transient result of K band signal source

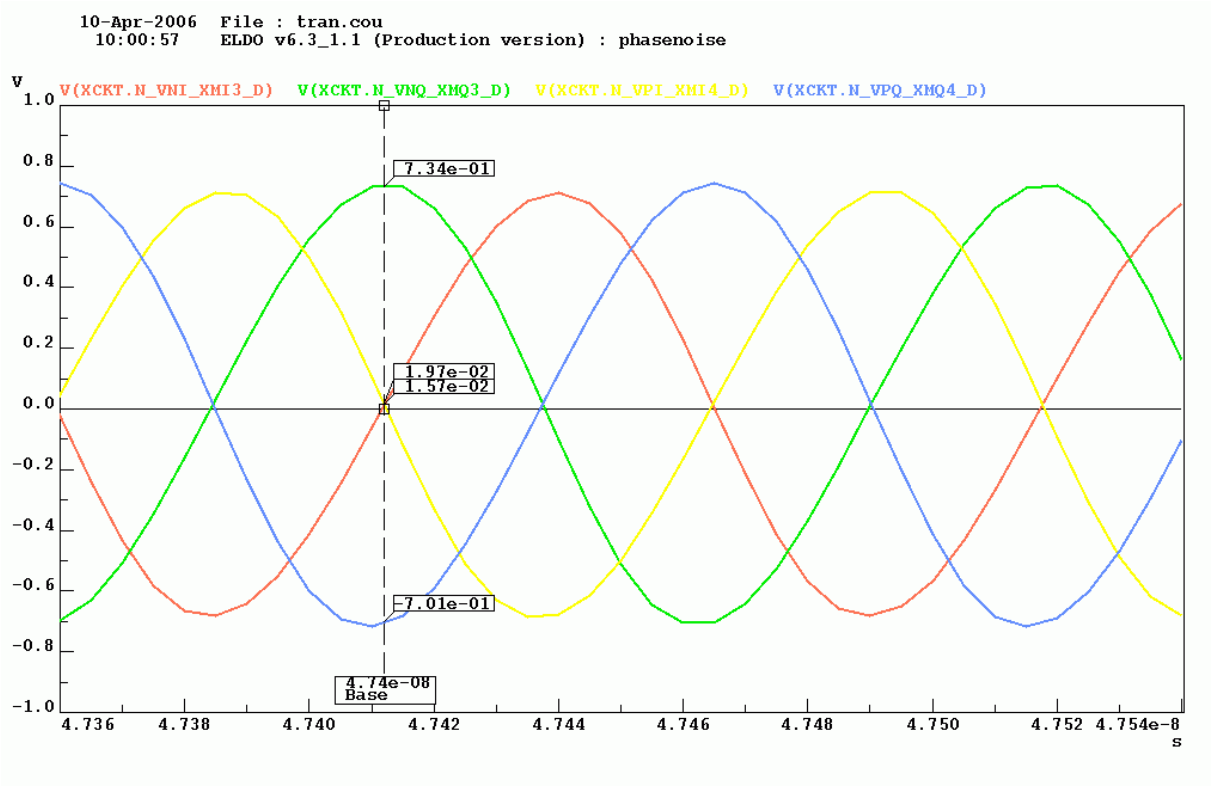


Fig. 4-10 The simulated transient result of X band quadrature signal

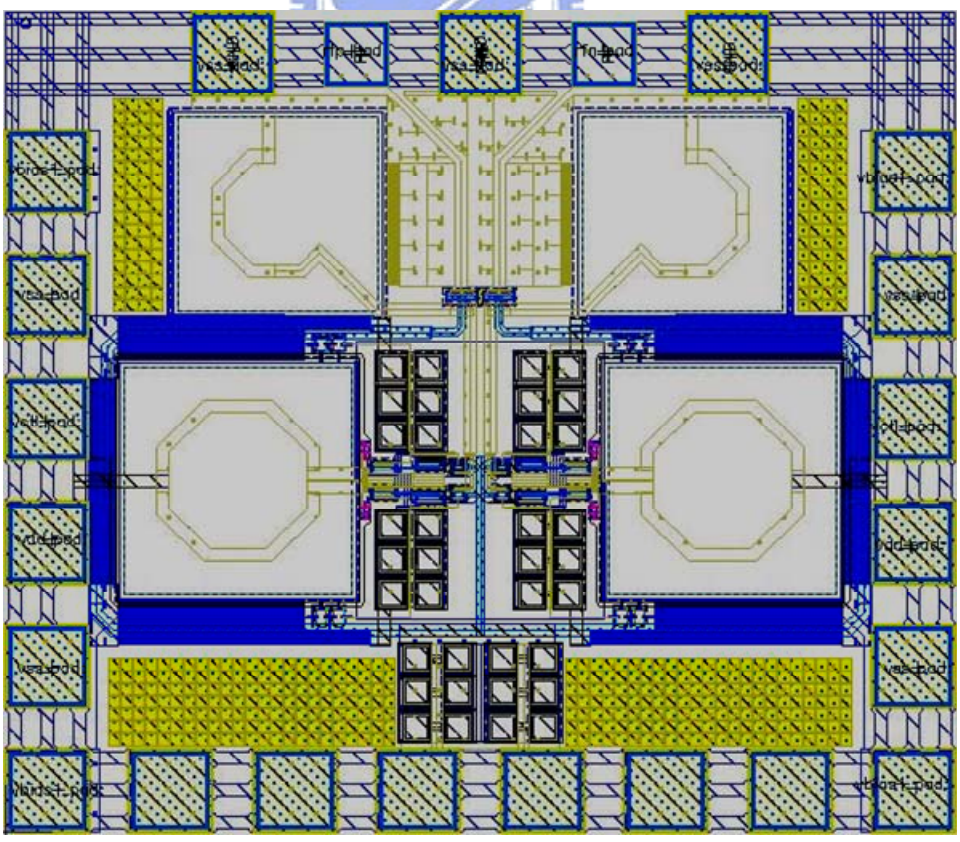


Fig. 4-11 Layout of the proposed K band VCO

Specification		Post Simulation
Process		CMOS 0.18um
Supply Voltage(Volt)		1.5
Frequency Range(GHz)		18.8~19.5
Output Power(dBm)		-3.21dBm
Tuning Range(MHz)		700 (3.655%)
Phase Noise(dBc/Hz)@1MHz		-112
Tuning Senstivity(MHz/V)		350
FOM(dB)		**185.63**
Power Consumption (mW)	Core(QVCO+doubler)	10.92+4.89=15.81
	Buffer	31.679
	Total	47.489

Table 15 Performance summary of the proposed K band VCO

4.4 Comparisons

Reference / Specification	[39] 2005 MTT Meas.	[40] 2004 MTT Meas.	This Work Sim.	
Process	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um	
Supply Voltage(V)	1.8	1.8	1.5	
Frequency Range(GHz)	19.84~22.01	9.3~10.4	18.8~19.5	9.4~9.75
Output Power(dBm)	-6.83	N/A	-3.21dBm	N/A
Tuning Range(MHz)	2170	1100	700	350
Phase Noise (dBc/Hz)	-111.67@1MHz	-91@100kHz	-112@1MHz -87.5@100kHz	-118@1MHz -93.5@100kHz
FOM(dB)	**182.03**	**165**	**185.63**	**187.24**
Core Circuit Power Consumption(mW)	40.32	14.4	15.81	

Table 16 Comparison with K band and X band VCO

Table 16 shows the comparison with K band and X band VCOs. In order to compare the performance with other recently proposed works in terms of center frequency, phase noise

and power consumption, the figure-of-merit (FoM) characteristic is expressed as [40]:

$$FoM = 10\log\left[\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{L(\lambda)P_D}\right] \tag{4.14}$$

Here, f_o is the oscillation frequency of the VCO, Δf is the offset frequency, P_D is the power consumption and $L(\lambda)$ is the phase noise at the oscillation frequency. The low phase noise and low power consumption result in high FOM in this work, and the calculated FoM of each work are listed in Table 16.

4.5 Conclusions

In this future work, we simulated a K band frequency with X band CMOS QVCO. Low phase noise and high FoM is the main design goal in this K band VCO. The power supply is designed as 1.5V for measurement consideration, and the buffers operating at K band consume large power. The simulation results reveal that low power consumption (15.81mW) and low phase noise (-112 dBc/Hz @ 1-MHz) is accomplished in K band. However, some prototypes such as transformers still benefit the performance of a VCO [40]. These prototypes will be the feature study for us.

Reference

[1] Guillermo Gonzalez, Microwave Transistors Amplifiers Analysis and Design (2nd edition), Prentice Hall Co., 1996

[2] Zhenbiao Li; Quintal, R.; O, K.K.; “A dual-band CMOS front-end with two gain modes for wireless LAN applications” Solid-State Circuits, IEEE Journal of Volume 39, Issue 11, Nov. 2004 Page(s):2069 – 2073

[3] Win-Ming Chang; Kuo-Hua Cheng; Jou, C.F.; “2.45GHz/5.2GHz switched dual-band CMOS LNA with 4 gain control modes” Microwave Conference Proceedings, 2005. APMC 2005. Asia-Pacific Conference Proceedings Volume 2, 4-7 Dec. 2005 Page(s):4 pp.

[4] Thomas H. Lee, The design of CMOS Radio-Frequency Integrated Circuits, Cambridge, U.K. : Cambridge University Press, 1998

[5] Bosco Leung, VLSI For Wireless Communication, Prentice Hall Co. , 2002.

[6] Behzad Razavi. RF Microelectronics, Prentice Hall, 1998

[7] Liang-Hung Lu; Hsieh-Hung Hsieh; Yu-Shun Wang; “A compact 2.4/5.2-GHz CMOS dual-band low-noise amplifier” Microwave and Wireless Components Letters, IEEE [see also IEEE Microwave and Guided Wave Letters] Volume 15, Issue 10, Oct. 2005 Page(s):685 - 687

[8] Tsang, T.K.K.; El-Gamal, M.N. “Dual-band sub-1 V CMOS LNA for 802.11a/b WLAN applications”; Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on Volume 1, 25-28 May 2003 Page(s):I-217 - I-220 vol.1

[9] Qiu-Huan Huan, Dar-Ron Huang, Huey-Ru Chuang, " A Fully-Integrated 2.4 / 5.7 GHz Concurrent Dual-Band 0.18 pm CMOS LNA For An 802.11 WLAN Direct Conversion Receiver”, Microwave Journal, Issue 4, Feb 2004, 16-20

[10] Jou, C.F.; Kuo-Hua Cheng; Pang-Ruci Huang; Mei-Chien Chen; “Design of a fully

integrated high linearity dual-band CMOS LNA" Electronics, Circuits and Systems, 2003. ICECS 2003. Proceedings of the 2003 10th IEEE International Conference on Volume 3, 14-17 Dec. 2003 Page(s):978 - 981 Vol.3

[11] Jou, C.F.; Kuo-Hua Cheng; Wei-Cheng Lien; Chun Hsien Wu; Chin Hsien Yen; "Design of a concurrent dual-band receiver front-end in 0.18 /spl mu/m CMOS for WLANs IEEE 802.11a/b/g applications" Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposium on Volume 1, 25-28 July 2004 Page(s):I - 177-80 vol.1

[12] Hashemi, H.; Hajimiri, A.; "Concurrent dual-band CMOS low noise amplifiers and receiver architectures" VLSI Circuits, 2001. Digest of Technical Papers. 2001 Symposium on 14-16 June 2001 Page(s)247 – 250

[13] Chen-Yang Huang; Yue-ming Hsin; "An integrated dual-band SiGe HBT low noise amplifier" Radio-Frequency Integration Technology: Integrated Circuits for Wideband Communication and Wireless Sensor Networks, 2005. Proceedings. 2005 IEEE International Workshop on 30 Nov.-2 Dec. 2005 Page(s):187 – 190

[14] Y.S.; Lu, L.-H.; "5.7 GHz low-power variable-gain LNA in 0.18 um CMOS" Wang, Electronics Letters Volume 41, Issue 2, 20 Jan. 2005 Page(s):66 - 68

[15] Tsang, T.K.K.; El-Gamal, M.N.; "Gain controllable very low voltage (⩽ 1 V) 8-9 GHz integrated CMOS LNAs" Radio Frequency Integrated Circuits (RFIC) Symposium, 2002 IEEE 2-4 June 2002 Page(s):205 – 208

[16] Sacchi, E.; Bietti, I.; Gatta, F.; Svelto, F.; Castello, R.; "A 2 dB NF, fully differential, variable gain, 900 MHz CMOS LNA" VLSI Circuits, 2000. Digest of Technical Papers. 2000 Symposium on 15-17 June 2000 Page(s):94 - 97

[17] Pennisi, S.; Scaccianoce, S.; Palmisano, G.; "A new design approach for variable-gain low noise amplifiers" Radio Frequency Integrated Circuits (RFIC) Symposium, 2000. Digest of Papers. 2000 IEEE11-13 June 2000 Page(s):139 - 142

[18] IEEE Std 802.11a, wireless LAN Medium Access Control (MAC) and Physical Layer

(PHY) Specifications: High-speed Physical Layer in The 5 GHz Band, September 1999

[19] IEEE Std 802.11b, Wireless LAN Medium Access Control (MAC) And Physical Layer (PHY) Specifications: Higher-speed Physical Layer Extension In The 2.4 GHz Band, September, 1999.

[20] IEEE Std 802.11g, wireless LAN medium access control (MAC) and physical layer (PHY) specifications, 2003

[21] Wang, Y.S.; Lu, L.-H.; "5.7 GHz low-power variable-gain LNA in 0.18 /spl mu/m CMOS" ; Electronics Letters Volume 41, Issue 2, 20 Jan. 2005 Page(s):66 – 68

[22] Che-Hong Liao; Huey-Ru Chuang; "A 5.7-GHz 0.18-/spl mu/m CMOS gain-controlled differential LNA with current reuse for WLAN receiver" Microwave and Wireless Components Letters, IEEE [see also IEEE Microwave and Guided Wave Letters] Volume 13, Issue 12, Dec. 2003 Page(s):526 - 528

[23] Raja, M.K.; Boon, T.T.C.; Kumar, K.N.; Wong Sheng Jau; "A fully integrated variable gain 5.75-GHz LNA with on chip active balun for WLAN" Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE 8-10 June 2003 Page(s):439 – 442

[24] Tuan-Anh Phan, Chang-Wan Kim, Min-Suk Kang, Sang-Gug Lee, Chun-Deok Su" Low noise and high gain CMOS down conversion mixer" Communications, Circuits and Systems, 2004. ICCCAS 2004. 2004 International Conference on Volume 2, 27-29 June 2004 Page(s):1191 - 1194 Vol.2

[25] Darabi, H.; Abidi, A.A.; "Noise in RF-CMOS mixers: a simple physical model" Solid-State Circuits, IEEE Journal of Volume 35, Issue 1, Jan. 2000 Page(s):15 – 25

[26] Klumperink, E.A.M.; Louwsma, S.M.; Wienk, G.J.M.; Nauta, B.; "A 1 Volt switched transconductor mixer in 0.18 /spl mu/m CMOS" VLSI Circuits, 2003. Digest of Technical Papers. 2003 Symposium on 12-14 June 2003 Page(s):227 - 230

[27] Klumperink, E.A.M., Louwsma, S.M., Wienk, G.J.M., Nauta, B. "A CMOS switched transconductor mixer" Solid-State Circuits, IEEE Journal of Volume 39, Issue 8, Aug.

2004 Page(s):1231 - 1240

[28] Won-Young Uhm; Woo-Suk Sul; Hyo-Jong Han; Sung-Chan Kim; Han-Sin Lee; Dan An; Sam-Dong Kim; Dong-Hoon Shin; Hyung-Moo Park; Jin-Koo Rhee; "A high performance V-band monolithic quadruple sub-harmonic mixer" Microwave Symposium Digest, 2003 IEEE MTT-S International Volume 2, 8-13 June 2003 Page(s):1319 - 1322 vol.2

[29] Perumana, B.G., Chang-Ho Lee, Laskar, J., Chakraborty, S. " A subharmonic CMOS mixer based on threshold voltage modulation" Microwave Symposium Digest, 2005 IEEE MTT-S International 12-17 June 2005 Page(s):4 pp.

[30] Feng, H., Wu, Q., Guan, X., Zhan, R., Wang, A., Yang, L.-W., " A 5 GHz sub-harmonic direct down-conversion mixer for dual-band system in 0.35 /spl mu/m SiGe BiCMOS" Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on 23-26 May 2005 Page(s):4807 - 4810 Vol. 5

[31] Chen, H.-C.; Wang, T.; Lu, S.-S.; Huang, G.-W.; "A Monolithic 5.9-GHz CMOS IQ Direct-Down Converter Utilizing a Quadrature Coupler and Transformer-Coupled Subharmonic Mixers" Microwave and Wireless Components Letters, IEEE [see also IEEE Microwave and Guided Wave Letters] Volume 16, Issue 4, April 2006 Page(s)197 - 199

[32] Upadhyaya, P., Rajashekharaiah, M., Deukhyoun Heo, " A 5.6-GHz CMOS doubly balanced sub-harmonic mixer for direct conversion -zero IF receiver" Microelectronics and Electron Devices, 2004 IEEE Workshop on 2004 Page(s):129 – 130

[33] Upadhyaya, P., Rajashekharaiah, M., Yang Zhang, Deukhyoun Heo, Yi-Jan Emery Chen, "A 5 GHz novel 0.18-/spl mu/m inductor-less CMOS sub-harmonic mixer" Information Processing in Sensor Networks, 2005. IPSN 2005. Fourth International Symposium on 15 April 2005 Page(s):71 - 74

[34] Xiang Guan; Hajimiri, A.; "A 24-GHz CMOS front-end" Solid-State Circuits, IEEE

Journal of Volume 39, Issue 2, Feb. 2004 Page(s):368 - 373

[35] Kyung-Wan Yu; Yin-Lung Lu; Da-Chiang Chang; Liang, V.; Chang, M.F.; "K-band low-noise amplifiers using 0.18 /spl mu/m CMOS technology" Microwave and Wireless Components Letters, IEEE [see also IEEE Microwave and Guided Wave Letters] Volume 14, Issue 3, March 2004 Page(s):106 - 108

[36]Shin, S.-C.; Ming-Da Tsai; Ren-Chieh Liu; Lin, K.-Y.; Huei Wang; "A 24-GHz 3.9-dB NF low-noise amplifier using 0.18 /spl mu/m CMOS technology" Microwave and Wireless Components Letters, IEEE [see also IEEE Microwave and Guided Wave Letters] Volume 15, Issue 7, July 2005 Page(s):448 - 450

[37] Masud, M.A.; Zirath, H.; Ferndahl, M.; Vickes, H.-O.; "90 nm CMOS MMIC amplifier" Radio Frequency Integrated Circuits (RFIC) Symposium, 2004. Digest of Papers. 2004 IEEE 6-8 June 2004 Page(s):201 - 204

[38] http://www.xilinx-china.com/esp/wireless/bfwa/lmds.htm

[39] Sangsoo Ko; Jeong-Geun Kim; Taeksang Song; Euisik Yoon; Songcheol Hong; "K- and Q-bands CMOS frequency sources with X-band quadrature VCO" Microwave Theory and Techniques, IEEE Transactions on Volume 53, Issue 9, Sept. 2005 Page(s):2789 – 2800

[40] Lin Jia; Jian-Guo Ma; Kiat Seng Yeo; Manh Anh Do; "9.3-10.4-GHz-band cross-coupled complementary oscillator with low phase-noise performance" Microwave Theory and Techniques, IEEE Transactions on Volume 52, Issue 4, April 2004 Page(s):1273 – 1278

[41] Wei-Zen Chen; Chien-Liang Kuo; Chia-Chun Liu; "10 GHz quadrature-phase voltage controlled oscillator and prescaler" Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European 16-18 Sept. 2003 Page(s):361 – 364

[42] Shenggao Li; Kipnis, I.; Ismail, M.; "A 10-GHz CMOS quadrature LC-VCO for multirate optical applications" Solid-State Circuits, IEEE Journal of Volume 38, Issue

10, Oct. 2003 Page(s):1626 – 1634

[43] Murji, R.; Deen, M.J.; “A low-power, 10 GHz back-gated tuned voltage controlled oscillator with automatic amplitude and temperature compensation” Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on Volume 4, 23-26 May 2004 Page(s):IV - 421-4 Vol.4

[44] Zheng Gu; Bartsch, B.; Thiede, A.; Rui Tao; Zhi-Gong Wang; “Fully integrated 10 GHz CMOS LC VCOs” Microwave Conference, 2003. 33rd European Volume 2, 7-9 Oct. 2003 Page(s):583 - 586 vol.2

[45] Fenglin Yang; Zhaofeng Zhang; Baoqi Li; Hao Min; “A 4.8GHz CMOS fully-integrated LC balanced oscillator with symmetry noise filtering technique” Solid-State and Integrated Circuits Technology, 2004. Proceedings. 7th International Conference on Volume 2, 18-21 Oct. 2004 Page(s):1315 - 1320 vol.2

[46] Sau-Mou Wu; Ron-Yi Liu; Wei-Liang Chen; “A 5.8-GHz high efficient, low power, low phase noise CMOS VCO for IEEE 802.11a” System-on-Chip for Real-Time Applications, 2003. Proceedings. The 3rd IEEE International Workshop on 30 June-2 July 2003 Page(s):94 – 97

[47] Byunghun Min; Hanggeun Jeong; “5-GHz CMOS LC VCOs with wide tuning ranges” Microwave and Wireless Components Letters, IEEE [see also IEEE Microwave and Guided Wave Letters] Volume 15, Issue 5, May 2005 Page(s):336 – 338