國 立 交 通 大 學

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碩 士 論 文

低功率三階連續時間三角積分調變器之設計與製作

The Design and Implementation of Low Power Third-Order Continuous-Time Sigma-Delta Modulator

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中 華 民 國 九十五 年 十 月

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摘要

隨著手持式電子產品的蓬勃發展(例如：筆記型電腦、手機、MP3 播放器…等)，系統單晶片(SOC)在減少這些電子裝置的耗電和重量上，是一個很重要的關鍵。在可攜式的產品中，電池的重量以及大小常是造成產品重量及大小的關鍵，因此減低功率的消耗可以有效的減少電池的個數以及電池的壽命。此外，因為電晶體的密度會隨著製程的進步而提昇，如此會使降低功率消耗的技術顯的更加重要。而在這類的電子產品上，軟體與硬體大多都是用數位的方法去實現，因此，一個高解析度、低功率耗電且面積小的類比數位轉換器是很重要的，因為如果橋接類比與數位兩種不同訊號的類比數位轉換器做得不夠好，會影響接下來許多數位電路效能。而三角積分類比數位轉換器就非常符合這個需求，因為它在有限頻寬的限制下可以達到非常高的解析度。除此之外，類比所佔的成份也相對比較少且對製程漂移的影響也比較小。因此，近幾年來三角積分類比數位轉換器都扮演著非常重要的角色。

三角積分類比數位轉換器在不同的應用範圍下通常會有兩種種類，一種是離散時間三角積分類比數位轉換器(Discrete-Time Sigma-Delta ADC)，因為它通常都是用交換電容的電路下實現，所以又稱為交換電容三角積分類比數位轉換器(Switched-Capacitor Sigma-Delta ADC)。一般而言，離散時間三角積分器為了在一個 clock 的時間可以快速的充放電到前級交換電容電路所儲存的電荷，所以它的積分器也就是 OPAMP 的規格，不管是頻寬、Slew Rate 和 Settling Time 都要訂得比較高才行，然而對於連續時間而言，它不需要在一個 clock 的時間下做處理，所以它的積分器的規格可以訂的比較寬鬆一點，因此它的功率消耗會減少很多。

因此，為了將連續時間三角積分類比數位轉換器的優點應用在基頻的範圍內，我的研究主題就是做出一個適用於基頻範圍的超低功率消耗的連續時間三角積分類比數位轉換器，所消耗的功率與面積將會比用離散時間方式做出來的還要更低，以符合可攜式電子產品需要低消耗功率的趨勢。晶片是以台積電 0.18 微米標準互補式金氧半導體製程所製造。

The Design and Implementation of Low Power Third-Order Continuous-Time Sigma-Delta Modulator

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Abstract

Along with rapid growth of battery-powered portable devices, such as laptop, cellular phones, and MP3 player, system on a chip (SOC) is an important issue to help devices become smaller and lighter. Moreover, batteries almost dominate portable devices' sizes and weight. Therefore, reducing the power dissipation in chip is desirable so as reduce the number of battery cells and extend the battery lifetime as much as possible. Furthermore, the raising complexity on a chip results in an increase of power density, which leads to even higher demand for power reduction techniques. In today's device application, digital circuits dominate the whole chip function. However, analog-to-digital converter (ADC) is also indispensable. Under these conditions, sigma-delta (ΣΔ) ADCs are very suitable for the application because they can achieve high accuracy for narrow band signals with few analog components and insensitivity to process and component variation.

Typically, there are two kinds of ΣΔ ADCs. The first one is discrete-time (DT) ΣΔ ADC and another is continuous-time (CT) ΣΔ ADC. The DT ΣΔ ADC also called the switched-capacitor (SC) ΣΔ ADC because of using switched capacitors. Generally, in order to charge and discharge the capacitors in one clock time, the specification of an OPAMP , such as gain-bandwidth, slew rate and settling time, will be increased. But for CT ΣΔ ADC, it doesn't need to process signals within a clock time, so the requirement of integrator will be reduced. This results in further power decreasing.

In order to combine the advantages of the CT ΣΔ ADC system with low-frequency low-power applications, this research focuses on ultra low power audio CT ΣΔ ADC. The power consumption and area will be reduced compared with DT ΣΔ ADC. The chip has been fabricated by TSMC 0.18-um CMOS process.

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林政翰

國立交通大學
中華民國九十五年十月

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Chapter 1

Introduction

1.1 Motivation

The demand for battery-powered electronic equipments in many applications, such as wireless communications or portable electronic systems, has increased the need for low-power circuit techniques. And the trend is forwards to move the VLSI circuits from the analog domain to the digital domain over the last several years due to some attractive advantages, such as high level resolution, power consumption reduction, noise robustness and less chip area. Thus, this is desirable to integrate more and more systems in digital domains, and of course digital circuits nearly dominate the whole chip functions. However, in real world, we human only can sense analog signals. Whether how advanced the digital circuit technique become, we still need some units to process and convert the analog signals to digital signals. Also, some units to convert digital signals to analog signals in real world are needed after the digital system processing (Figure 1.1).

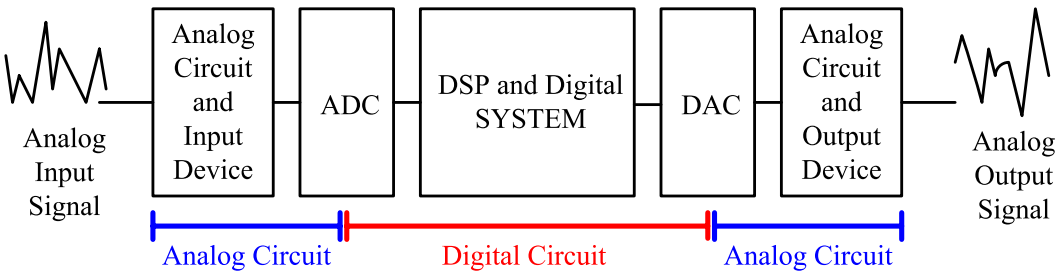


Figure 1.1 Battery-Powered System Block Diagram

The above means that a low power analog-to-digital interfaces are becoming more and more important between analog region and digital signal processing system. As the digital signal processing units (DSP) become much more powerful than before, high resolution and low power analog-to-digital converters which can be integrated in single system chip are needed for battery-powered devices.

Oversampling techniques with noise shaping strategy are widely used to implement the analog-to-digital interface between analog and digital domain in digital systems. This type of systems require high resolution or low power consumption. Sigma-delta data converters have meaningful advantages over traditional Nyquist-rate counterparts. In most cases, the linearity and accuracy of Nyquist-rate data converters are determined by the matching accuracy of the analog components used in the implementation. Thus, the Nyquist-rate data converters need to implement with calibration to guarantee an integral nonlinearity INL less than 0.5 LSB. However, the sigma-delta data converters are insensitive to circuit mismatch and provide higher resolution for digital system operation. In other words, they don't need precise matching for analog components. This advantage would reduce the systems and circuits complexity and save more power dissipation.

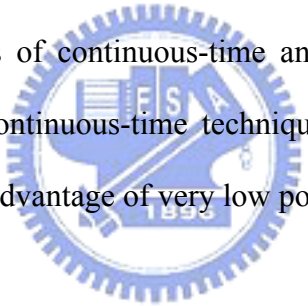
In this thesis, a 198μW, 10-bits, and 2.5MS/s continuous-time sigma-delta modulator (SDM) with the 1.8V supply voltage has been designed and implemented with the standard TSMC 0.18μm CMOS 1P6M process. By the way, no special process or multiplied voltage is needed in this research.

1.2 Thesis Organization

In Chapter 1, this thesis is briefly introduced.

Chapter 2 is the overview of sigma-delta data converters and other analog-to-digital data converters. It consists of classification and characteristics of performance and speed. Then, the oversampling technique and noise-shaping strategy are introduced and described mathematically. Finally, the various architectures of sigma-delta modulators will be introduced and compared.

Chapter 3 discusses the basic concept of continuous-time SDM which consisting the power consumption, clock jitter effect, and excess loop delay issues. Then, the advantages and disadvantages of continuous-time and discrete-time SDMs will be discussed. We will use the continuous-time technique to apply in audio-frequency domain in order to obtain the advantage of very low power consumption.



Chapter 4 presents the system level design consideration. After building the behavior model, we continue the circuit level design, including the operation amplifier, comparator, and feedback digital-to-analog converter (DAC). The circuits and simulation results will be shown in this chapter.

Chapter 5 presents the testing environment, including the instruments and external circuits on the printed circuit board (PCB). Measured results for the continuous-time SDM, which is fabricated in a standard TSMC 0.18μm CMOS mixed-signal process, will be plotted and summarized

Finally, the conclusions of this thesis are summarized in Chapter 6.

Chapter 2

An Overview of Sigma-Delta Data Converters

2.1 Introduction

This chapter reviews the basic concept of design the sigma-delta data converter. The discussion begins with a brief overview of data converter in the aspects of speed, resolution, and architecture. After this issue, the theories of how sigma-delta modulators work including sampling, quantization, oversampling, and noise shaping will be discussed. Following the introduction, tradeoffs of various sigma-delta modulator architectures will be discussed.

2.2 Overview of Analog-to-Digital Data Converters

The operations of analog-to-digital data converters can be roughly separated into two steps: sampling and quantization. The process of sampling transforms continuous time analog signals into discrete time step-like signals. The process of quantization converts the step-like signals to a set of discrete levels. Then, these discrete levels signals can be coded and be transmitted into DSP units or digital systems.

2.2.1 Categories of Analog-to-Digital Data Converters

According to operation, speed, and accuracy, there are three categories of analog-

to-digital converter shown in Table 2.1. Each category is applied in different field. But the demarcation for some structures nowadays is a little blurred.

TABLE 2.1 Various Kinds of Analog-to-Digital Data Converters

Speed	*Resolution*	*Structure*
Slow	High	Integrating Oversampling
Medium	Medium	Successive approximation Algorithmic
Fast	Low	Single-bit pipeline Flash Multiple-bit pipeline Folding Interpolating Time-Interleaved

2.2.2 Oversampling Ratio (OSR)

The oversampling ratio (OSR) of a data converter is defined as

$$OSR = \frac{f_s}{2 f_b} \tag{2.1}$$

where f_s is the sampling frequency and f_b is the signal bandwidth. When the OSR is equal to 1 ($f_s = 2 f_b$), it means the data converter is the Nyqist-rate data converter, however, when the OSR is great than 1, it means the data converter is the oversampling data converter. The OSR is the important parameter for oversampling data converters. The OSR increases the SNR by $(2n+1)\cdot 3\text{dB}$ or by $2n+1$ per octave, where n is the order of loop-filter.

The larger the OSR, the larger the sampling frequency when the signal bandwidth is fixed. Thus, it will need faster circuit and consume more power consumption. But the OSR need to keep as low as possible for high signal bandwidth consideration. In order to obtain the advantages of using noise-shaping strategy, the OSR should be at least 4 [01].

2.2.3 Signal to Noise Ratio (SNR)

The signal-to-noise ratio (SNR) of a data converter is the ratio of the signal power to the noise power, which measured at the output of the data converter. The maximum SNR that a converter can achieve is called the peak signal-to-noise ratio. Generally, the theoretical value of SNR for an N-bit Nyquist-rate ADC is given by

$$SNR = 6.02 \cdot N + 1.76 \quad dB \tag{2.2}$$

But for oversampling ADC, the theoretical value of SNR is

$$SNR = 6.02 \cdot N + 1.76 + 10\log(OSR) \ dB \tag{2.3}$$

2.2.4 Signal to Noise and Distortion Ratio (SNDR)

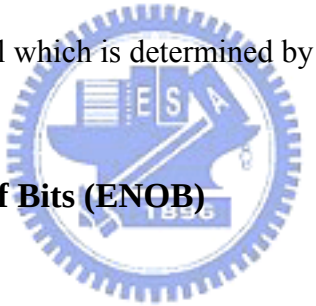
The signal to noise and distortion ratio (SNDR) of a data converter is the ratio of the signal power to the power of the noise plus the harmonic distortion components, which measured at the output of the data converter. The maximum SNDR that a converter can achieve is called the peak signal to noise and distortion ratio. Generally, SNDR is lower than SNR.

2.2.5 Spurious Free Dynamic Range (SFDR)

The spurious free dynamic range (SFDR) is defined as the ratio of rms value of amplitude of the fundamental signal to the rms value of the largest harmonic distortion component in a specified frequency range. SFDR may be much larger than SNDR of a data converter.

2.2.6 Dynamic Range at the input (DR)

The dynamic range is defined as the ratio between the power of the largest input signal which didn't significantly degrade the performance and the power of the smallest detectable input signal which is determined by the noise floor of converters.



2.2.7 Effective Number of Bits (ENOB)

For data converter, a specification often used in place of the SNR or SNDR is ENOB, which is a global indication of how many bits would be required to get the same performance as the converter. ENOB can be defined as follows:

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad bits\,. \tag{2.4}$$

2.2.8 Overload Level (OL)

OL is defined as the relative input amplitude where the SNR is decreased by 6dB compared to peak SNR value.

2.3 Sampling Theorem

Naturally, signals transmitted in the air are analog whether they originate from. The analog signals need to be sampled to become the digital signals for suitability in processing in the digital system. Thus, sampling is a very important procedure in the front end of the overall system. How much information can be preserve from the original signals depend on how fine to sample the signals and deal. It is crucial to choose the sampling frequency with a fixed signal bandwidth. And the relationship between the sampling frequency, f_s, and the signal bandwidth, f_b, is shown as follows :

$$f_s \geq 2 f_b \tag{2.5}$$

At least the sampling frequency must be greater than twice the input signal bandwidth to avoid aliasing. If f_s is smaller than twice the signal bandwidth, aliasing will occur at the output signal spectrum as shown in Figure 2.1.

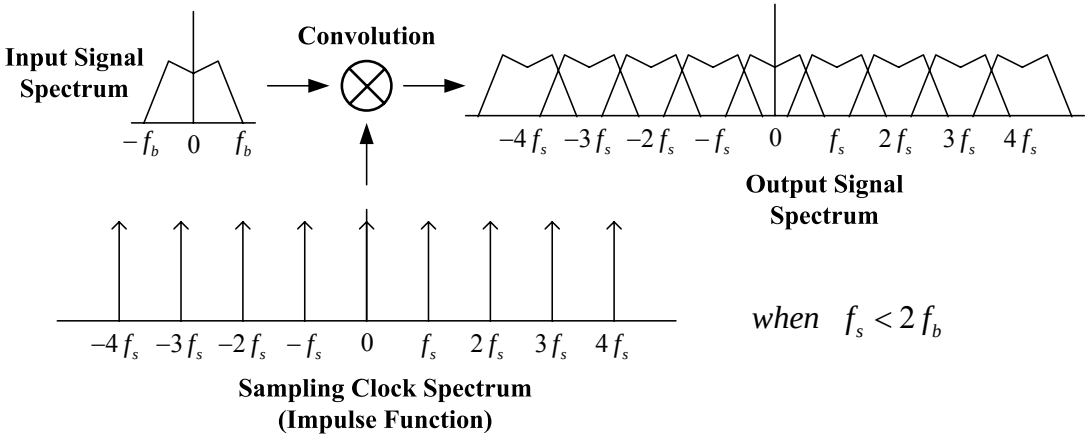


Figure 2.1 Illustration of the aliasing of the sampling process ($f_s < 2 f_b$)

There are two ways to deal with these problems. One is to cut the input signal bandwidth to f_{nb} to make f_s greater than twice the input signal bandwidth. But the disadvantage is that some high frequency information from the original signal will be loss (Figure 2.2). Another is to increase f_s to new sampling frequency f_{ns} in order to match the equation. This is more popular to deal with aliasing problems because there is no information of original input signal loss as shown in Figure 2.3. And just a low pass filter at the output is needed to recover the original signal.

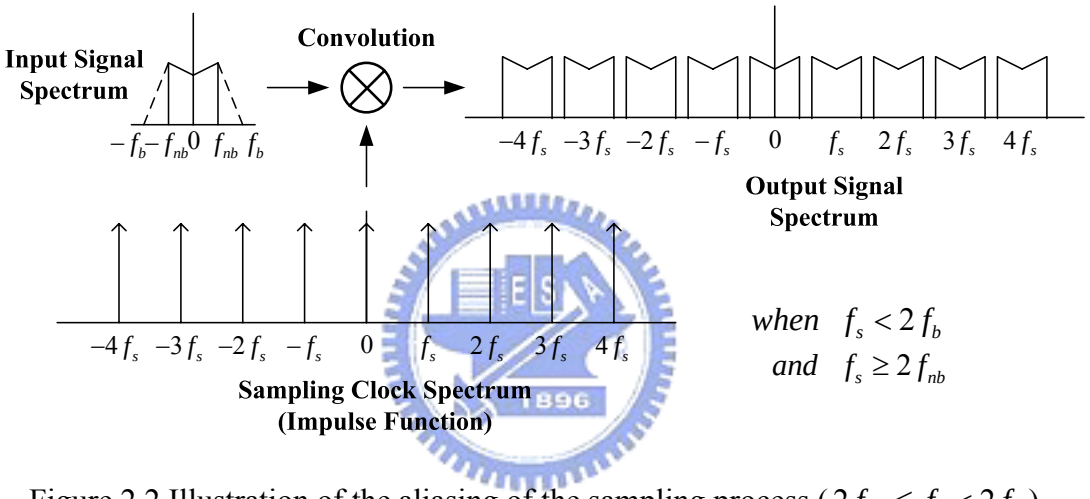


Figure 2.2 Illustration of the aliasing of the sampling process ($2f_{nb} \leq f_s < 2f_b$)

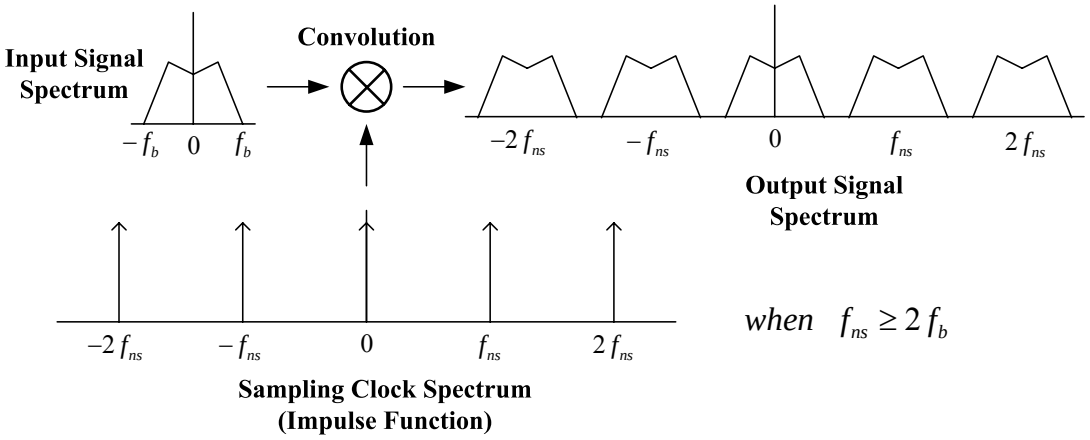


Figure 2.3 Illustration of the aliasing of the sampling process ($2f_b \leq f_{ns}$)

2.7 Quantization Noise

The quantizer is the interface between analog and digital domain. Once the analog signals pass through the quantizer, the signals will be digitized and separated into several different levels. The space between two adjacent levels is called a step size, Δ. There are two types of quantizer. One is uniform, and another is nonuniform. In a uniform quantizer, the distance between two adjacent levels is uniform; otherwise it is a nonuniform quantizer.

The process of quantization introduces an error, q(n). The error is defined as the difference between the input signal, x(n), and the output signal, y(n). And it is called the quantization error. Figure 2.4 and Figure 2.5 show the quantization process and assume the quantizer is uniform.

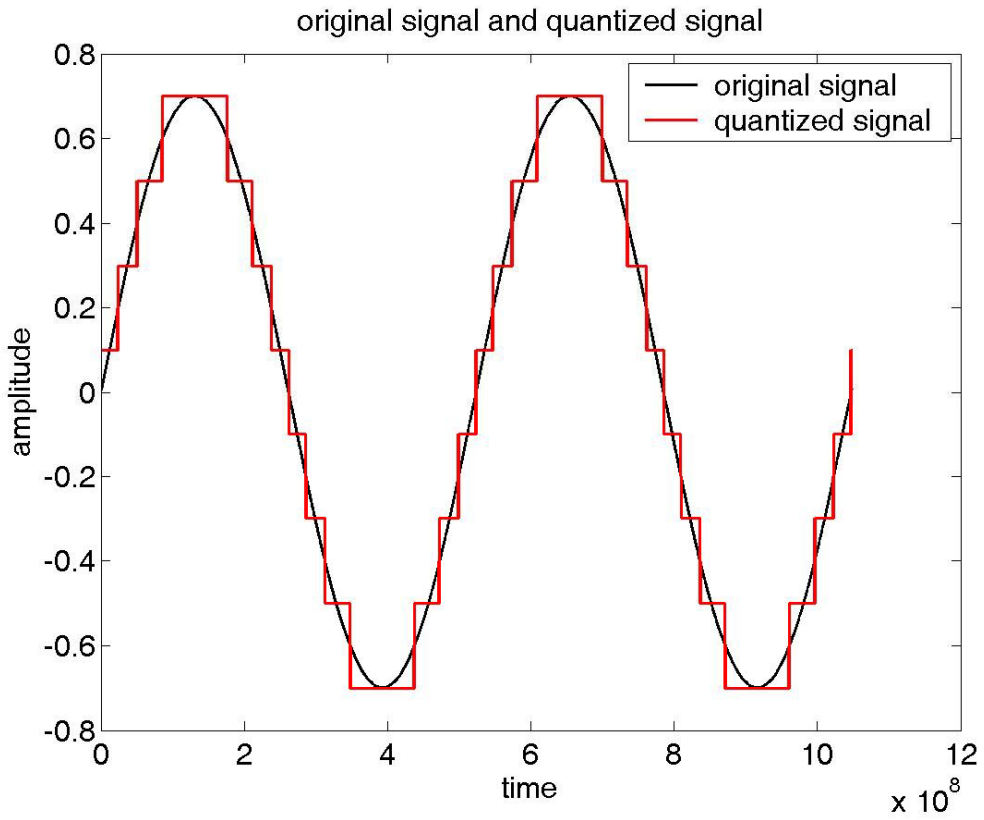


Figure 2.4 Quantized signal

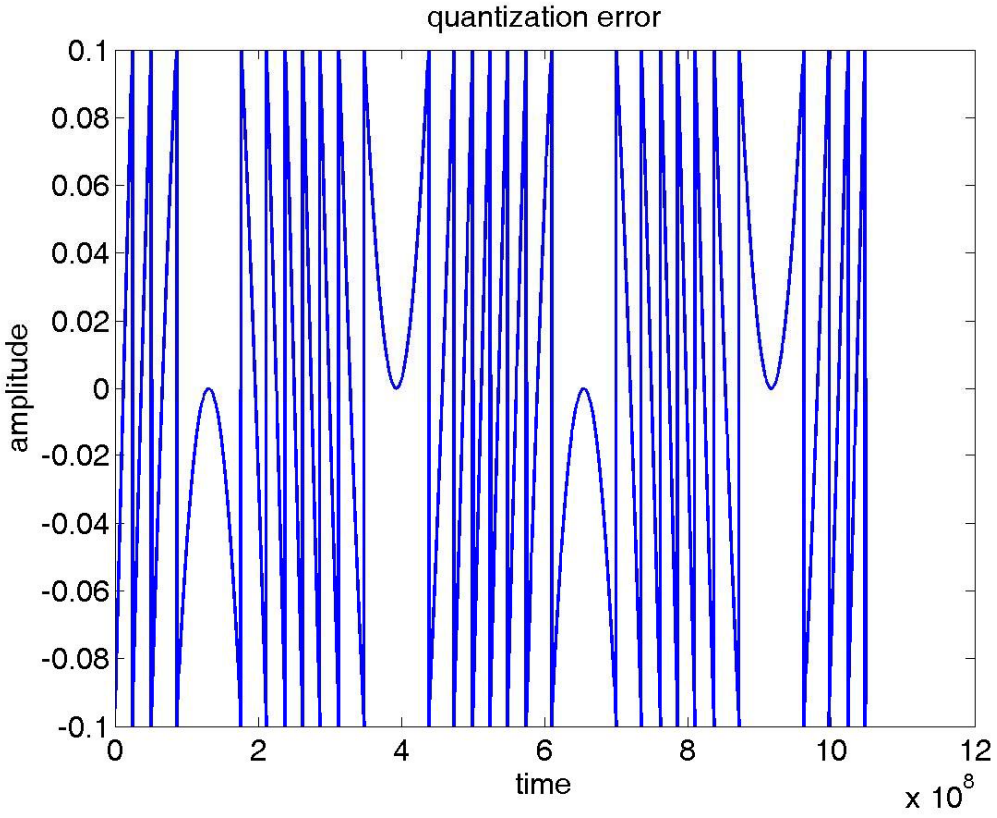


Figure 2.5 Quantization error

Many of the original results and insights into the behavior of quantization error are due to Bennett [02]. Bennett first developed conditions under which quantization noise could be reasonably modeled as additive white noise. A common statement of the approximation is that the quantization error has the following properties, which we call it the "input-independent additive white-noise approximation" [03]:

Property 1. q[n] is statistically independent of the input signal

Property 2. q[n] is uniformly distributed in [-Δ/2, Δ/2]

Property 3. q[n] is an independent identically distributed sequence or q[n] has a flat power spectral density (white).

Since the quantization noise, q(n), is equal to y(n)-x(n), a quantizer can be modeled as shown in Figure 2.6 [04] . For a uniform quantizer, if the input signal does not overload, the quantization error will be bounded by ±Δ/2. If the Δ is very small, it is convenient and reasonable to assume the quantization noise is zero mean and uniform distribution (Figure 2.7). The probability density function (pdf) of the quantization noise can be express as

$$f_Q(q) = \begin{cases} 1/\Delta, & -\Delta/2 \le q(n) \le \Delta/2 \\ 0, & \text{otherwise} \end{cases} \tag{2.6}$$

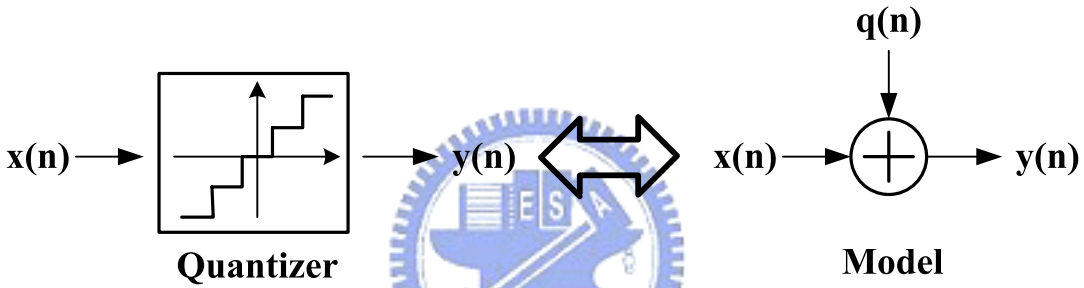


Figure 2.6 Quantizer and its linear model

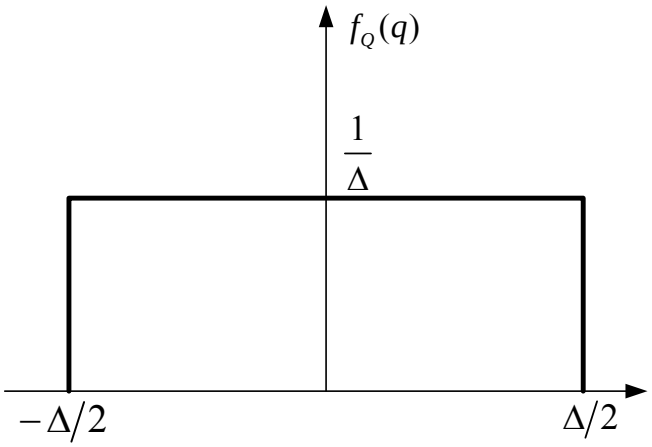


Figure 2.7 The pdf of quantization noise

From Figure 2.7, the power of quantization noise can be shown as follows:

$$P_{Q,noise} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q^2 dq = \frac{\Delta^2}{12} \tag{2.7}$$

The power spectrum density of q(n), $S_Q(f)$, within the range of $\pm f_s$ calculated using the equation (2.8) is

$$P_{Q,noise} = \frac{\Delta^2}{12} = \int_{-f_s/2}^{f_s/2} S_Q(f)df \tag{2.8}$$

And we obtain the final result of $S_Q(f)$ as

$$S_Q(f) = \frac{\Delta}{12 f_s} \tag{2.9}$$

From equation (2.9) we show that power spectrum density is inversely proportional to sampling frequency shown in Figure 2.8. The larger the sampling frequency is, the less the noise amplitude is.

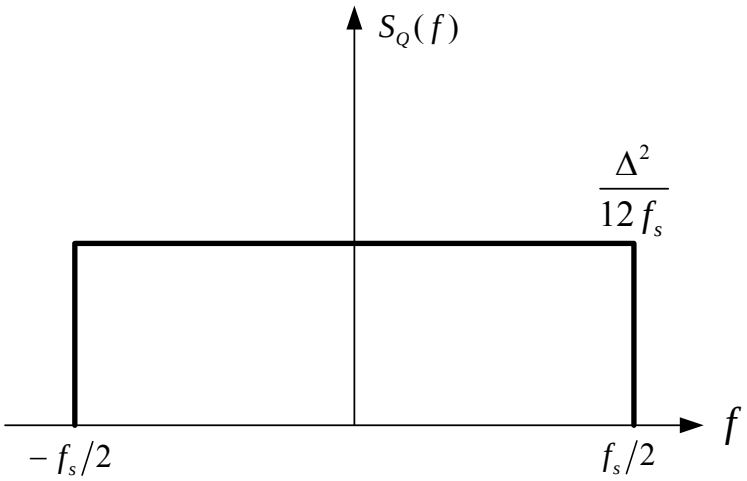


Figure 2.8 Power spectrum density of q(n)

Assume the quantization signal is uniformly distributed over the range $\pm V_A$, and N is the bits per sample. The step size can be write as

$$\Delta = \frac{2V_A}{2^N} \tag{2.10}$$

According to the equations above, the SNR can be shown as

$$SNR = 10\log\frac{P_{signal}}{P_{Q,noise}} = 10\log(\frac{V_A^2/2}{\Delta^2/12}) = 6.02N + 1.76 \tag{2.11}$$

Equation (2.11) shows that increasing the number of bits per sample in the qunatizer increases the accuracy of the converter by 6dB for each extra bit.

2.7 Oversampling Technique

Oversampling is an important technique for sigma-delta ADCs. It can release the requirement of anti-aliasing filter. And it also can improve the resolution of a sigma-delta ADC. This improvement is achieved by oversampling the signal. In other words, the sampling rate is much greater than Nyquist-rate. The definition of oversampling ratio (OSR) is

$$OSR = \frac{2f_s}{f_b} \tag{2.12}$$

where f_s is the sampling frequency and f_b is the input signal bandwidth. Assuming the quantization noise is white noise. It means that noise power is uniformly distributed between $-f_s/2$ and $f_s/2$. It had shown that total amount of noise power injected into the quantized signals are the same whether they are oversampling or Nyquist-rate conversions. But the distributions are different due to different sampling frequencies. Figure 2.9 shows the power spectrum density of

quantization noise $S_Q(f)$ for conversion of Nyquist-rate (dotted line) sampling with sampling frequency, $f_{s,NR}$, and oversampling (solid line) sampling with sampling frequency, $f_{s,OS}$, which is much greater than input signal bandwidth, f_b. The power spectrum density of input signal bandwidth for Nyquist rate is much greater than oversampling.

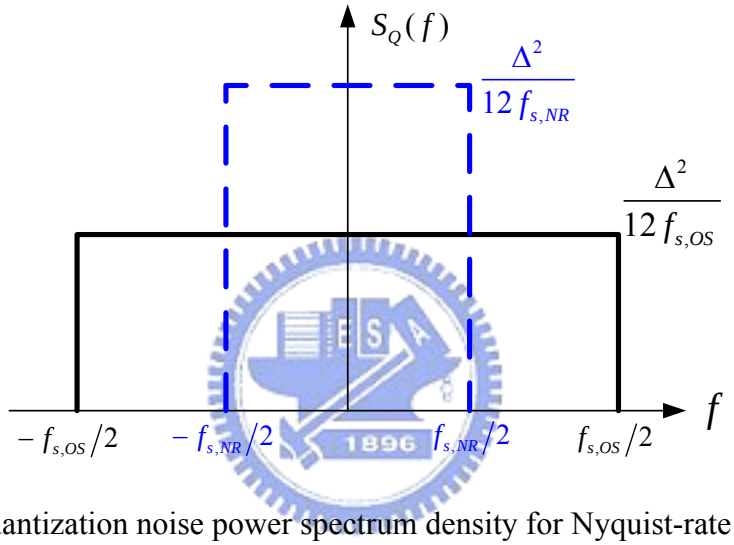
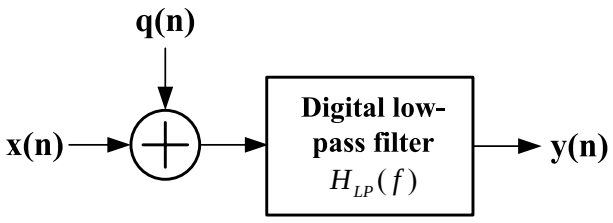
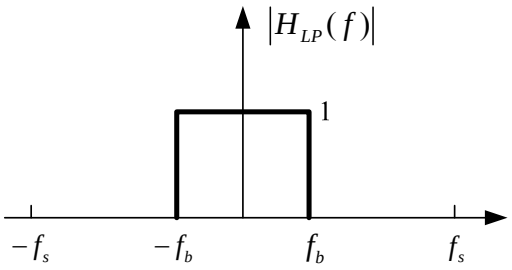


Figure 2.9 Quantization noise power spectrum density for Nyquist-rate (dotted line) and oversampling (solid line) conversion

The area of the both two rectangles meaning the total amount of noise power are the same and equal to $\Delta^2/12$. From Figure 2.9, it shows that the quantization noise power has spread to $f_{s,OS}/2$ and only a small fraction of quantization noise fall into the range of $-f_b$ and f_b. And the quantization noise outside the signal band will be attenuated by a digital low-pass filter as shown in Figure 2.10. Recollecting the quantization noise power spectrum density in equation (2.9) then we can show that the quantization noise is becoming



(a)



(b)

Figure 2.10 (a) Oversampling conversion with digital low-pass filter (b) magnitude of frequency response of digital low-pass filter

$$P_{Q,noise} = \int_{-f_s}^{f_b} S_Q(f)\cdot|H_{LP}(f)|^2 df = \int_{-f_b}^{f_b} S_Q(f)df = \frac{\Delta^2}{12 f_s}\cdot(2 f_b) = \frac{\Delta^2}{12}\cdot\frac{2 f_b}{f_s} \tag{2.13}$$

then we obtain

$$P_{Q,noise} = \frac{\Delta^2}{12}\cdot\frac{2 f_b}{f_s} = \frac{\Delta^2}{12}\cdot\frac{1}{OSR} \tag{2.14}$$

According equation (2.7), (2.10), (2.12) and (2.14), the SNR of oversampling conversion is

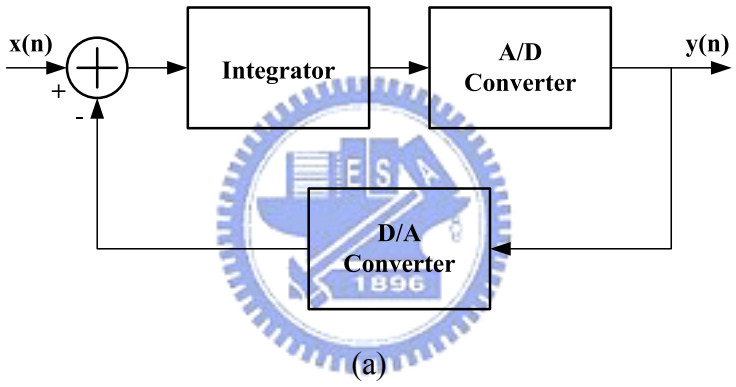
$$SNR = 10\log\left(\frac{P_{signal}}{P_{Q,noise}}\right) = 10\log\left(\frac{\frac{V_A^2}{2}}{\frac{\Delta^2}{12}\cdot\frac{1}{OSR}}\right) = 6.02N + 1.76 + 10\log(OSR) \tag{2.15}$$

The first term of equation (2.15) denotes the contribution of N-bit quantizer and the

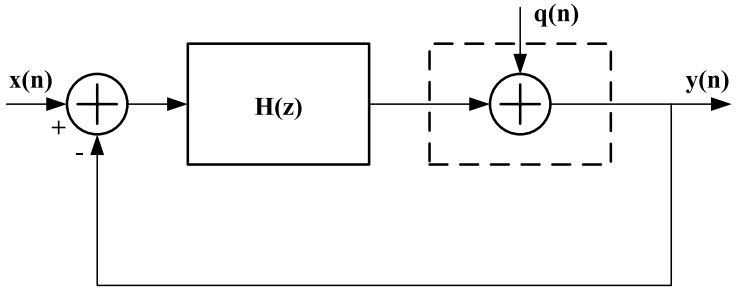
last term is the enhancement of oversampling technique. For every doubling the OSR, the SNR improve by 3dB corresponding to improve the resolution by 0.5 bit. Besides, since the resolution of N-bit quantizer is lower than overall resolution of system, it could reduce the complexity of analog circuit and power of overall system.

2.7 Noise Shaping Strategy

A general noise-shaped sigma-delta modulator and its linear model have been shown in Figure 2.11.



(a)



(b)

Figure 2.11 Block diagram of a noise-shaped SDM and its linear model

We can show that

$$y(n) = x(n-1) + q(n) - q(n-1) \tag{2.16}$$

After transforming equation (2.16) by *Z*-transform, we obtain

$$Y(z) = \frac{H(z)}{1+H(z)} X(z) + \frac{1}{1+H(z)} Q(z) \tag{2.17}$$

Then we can derive signal transfer function ($S_{TF}(z)$) by setting Q(z)=0

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \tag{2.18}$$

The same, we can derive noise transfer function ($N_{TF}(z)$) by setting X(z)=0

$$N_{TF}(z) = \frac{Y(z)}{Q(z)} = \frac{1}{1+H(z)} \tag{2.19}$$

The equation (2.17) will become

$$Y(z) = S_{TF}(z) \cdot X(z) + N_{TF}(z) \cdot Y(z) \tag{2.20}$$

The STF generally have all-pass or low-pass frequency response and the NTF have high-pass frequency response. In other words, the STF will be approximately unity over the signal band and the NTF will be approximately zero over the same frequency band. The quantization noise will be removed to high frequency band when using noise-shaping strategy [05]. The quantization noise over the frequency band of interest will be reduced and do not affect the input signal. This would improve the SNR significantly for overall system.

2.6.1 First-Order Sigma-Delta Modulator

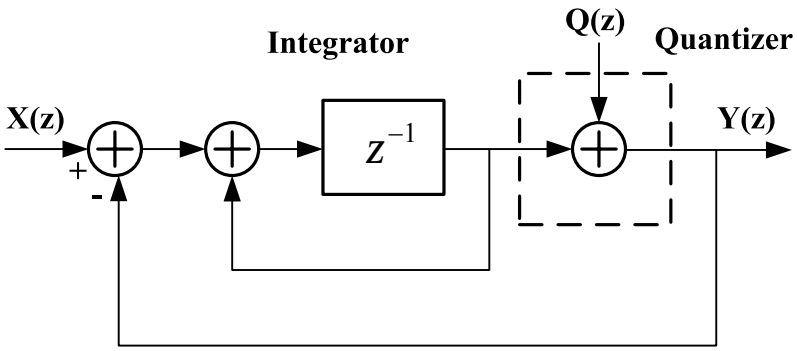


Figure 2.12 The First-Order SDM

In Figure 2.12, it is a simple block diagram of the first-order SDM [06]. It includes an integrator and 1-bit quantizer. The noise-transfer function, $N_{TF}(z)$, should have a zero at DC. And zeros of $N_{TF}(z)$ are equal to poles of the $H(z)$ (ie., has a pole at z=1). Therefore, the quantization noise will be high-pass filtered. In other words, the $H(z)$ will be small and the $N_{TF}(z)$ will large over the frequency band of interest. Thus, the discrete time integrator with a pole at DC can be expressed as

$$H(z) = \frac{1}{z-1} = \frac{z^{-1}}{1-z^{-1}} \tag{2.21}$$

According to equation (2.18) and (2.19) we obtain

$$S_{TF}(z) = \frac{H(z)}{1+H(z)} = \frac{z^{-1}/1-z^{-1}}{1+z^{-1}/1-z^{-1}} = z^{-1} \tag{2.22}$$

$$N_{TF}(z) = \frac{1}{1+H(z)} = \frac{1}{1+z^{-1}/1-z^{-1}} = 1-z^{-1} \tag{2.23}$$

The total transfer function of system is

$$Y(z) = X(z) \cdot z^{-1} + Q(z) \cdot (1 - z^{-1}) \tag{2.24}$$

From equation (2.24) we know the STF is just a delay and NTF is a high-pass filter. In another word, the output signal comprises the delayed input signal and high-pass filtered quantization noise. Now, we may consider the amplitude of the noise transfer function, $|N_{TF}(z)|$. Let $z = e^{j\omega T} = e^{j2\pi f/f_s}$, equation (2.23) will becomes

$$N_{TF}(z) = 1 - z^{-1} = 1 - e^{-j\omega T} = 1 - e^{-j2\pi f/f_s}$$

$$= \frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j} \cdot 2j \cdot e^{-j\pi f/f_s}$$

$$= \sin\left(\frac{\pi f}{f_s}\right) \cdot 2j \cdot e^{-j\pi f/f_s}$$

Then we obtain

$$|N_{TF}(f)| = 2\sin\left(\frac{\pi f}{f_s}\right) \tag{2.25}$$

The quantization noise power over the signal band is shown as follows:

$$P_{Q,noise} = \int_{-f_b}^{f_b} S_Q(f) \cdot |N_{TF}(z)|^2 \, df = \int_{-f_b}^{f_b} \frac{\Delta^2}{12} \frac{1}{f_s} \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \tag{2.26}$$

Because $OSR \gg 1$ for oversampling conversion, f_s would be much larger than f_b.

Thus, $\sin(\pi f / f_s)$ can be approximated to $\pi f / f_s$. Equation (2.26) will become

$$P_{Q,noise} = \frac{\Delta^2}{12 f_s}\int_{-f_b}^{f_b}\left[2\left(\frac{\pi f}{f_s}\right)\right]^2 = \frac{\Delta^2}{12}\cdot\frac{\pi^2}{3}\cdot\left(\frac{2 f_b}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \qquad (2.27)$$

Using the equation (2.10) and (2.27), we obtain the SNR of first-order SDM

$$SNR = 10\log\left(\frac{P_{signal}}{P_{Q,noise}}\right) = 10\log\left(\frac{\frac{V_A^2}{2}}{\frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3}\right) = 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3}\right)$$

$$= 6.02b + 1.76 - 5.17 + 30\log(OSR) \text{ dB} \qquad (2.28)$$

For every doubling the OSR, the SNR will improve by 9dB (ie., resolution will increase 1.5 bits). This result can be compared with equation (2.15), the SNR only can improve by 3dB when oversampling conversion do not use noise-shaping strategy. It will be much efficiency when using noise-shaping technique.

2.6.2 Second-Order Sigma-Delta Modulator

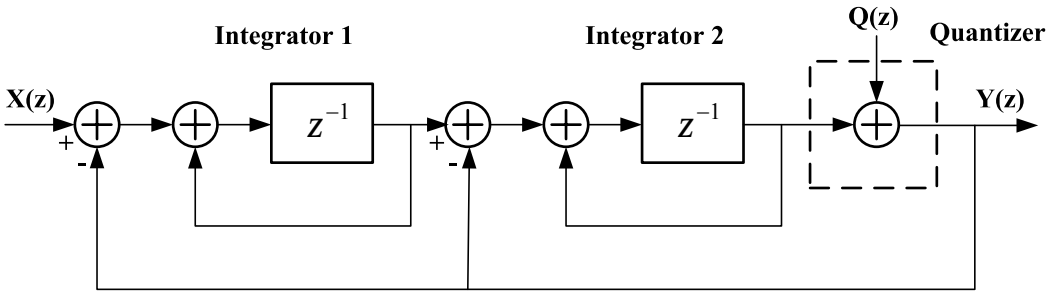


Figure 2.13 The Second-Order SDM

In Figure 2.13, it is a block diagram of a second-order SDM. It is popular and widely used in SDM designing. It includes two integrators and a 1-bit quantizer. Its fundamental theorem is the same as the first-order SDM. Thus, the transfer function can be expressed as

$$Y(z) = X(z) \cdot z^{-2} + Q(z) \cdot (1 - z^{-1})^2 \tag{2.29}$$

And we can show the $S_{TF}(z)$ and $N_{TF}(z)$

$$S_{TF}(z) = z^{-2} \tag{2.30}$$

$$N_{TF}(z) = (1 - z^{-1})^2 \tag{2.31}$$

Thus we obtain the magnitude of N_{TF}

$$\left|N_{TF}(f)\right| = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 \tag{2.32}$$

The quantization noise power over the signal band is shown as following

$$P_{Q,noise} = \int_{-f_b}^{f_b} S_Q(f) \cdot \left|N_{TF}(z)\right|^2 df = \int_{-f_b}^{f_b} \frac{\Delta^2}{12} \frac{1}{f_s} \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df$$

$$\approx \frac{\Delta^2}{12 f_s} \int_{-f_b}^{f_b} \left[2\left(\frac{\pi f}{f_s}\right)\right]^4 = \frac{\Delta^2}{12} \cdot \frac{\pi^4}{5} \cdot \left(\frac{2 f_b}{f_s}\right)^5 = \frac{\Delta^2 \pi^4}{60} \left(\frac{1}{OSR}\right)^5 \tag{2.33}$$

With the same method, we can obtain the SNR of the second-order SDM as

$$SNR = 10\log\left(\frac{P_{signal}}{P_{Q,noise}}\right) = 10\log\left(\frac{\frac{V_A^2}{2}}{\frac{\Delta^2\pi^4}{60}\left(\frac{1}{OSR}\right)^5}\right) = 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2\pi^4}{60}\left(\frac{1}{OSR}\right)^5}\right) \tag{2.34}$$

$$= 6.02b + 1.76 - 12.9 + 50\log(OSR) \text{ dB}$$

For every doubling the OSR, the SNR will improve by 15dB (ie., resolution will increase 2.5 bits). This result can be compared with equation (2.15) and (2.28), the second-order SDM can provide more suppression over the same band, and thus more noise power outside the signal band. Figure 2.14 shows the phenomenon of using noise-shaping technique or not. For a fixed signal band, the case of no noise-shaping has the largest quantization power over the signal band. The second and the third are

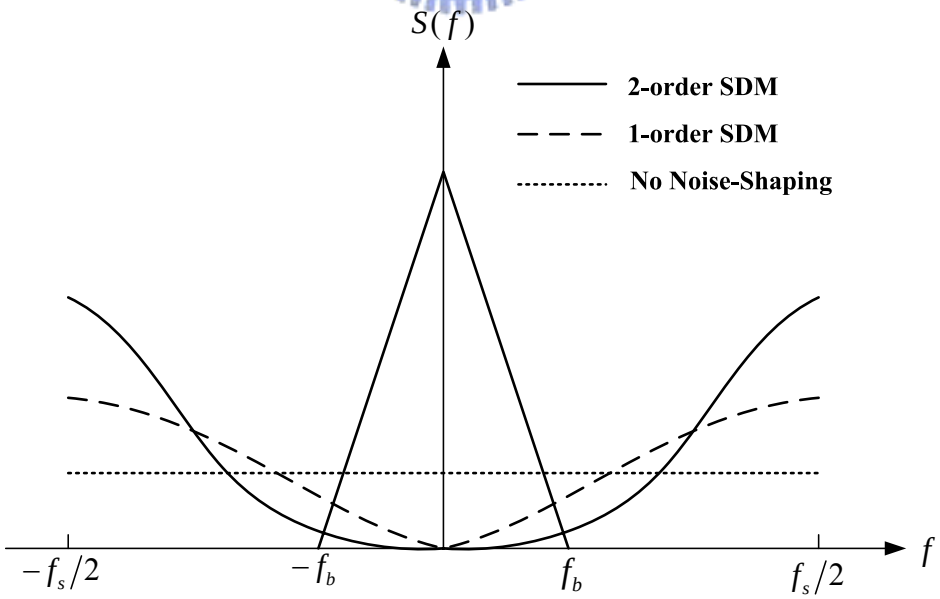


Figure 2.14 Power spectrum density of 1st order, 2nd order noise-shaping and non noise-shaping strategy

the first-order SDM and the second-order SDM respectively. As the number of order increasing, the quantization noise power will decrease over the same signal band. The simulation result can show as Figure 2.15.

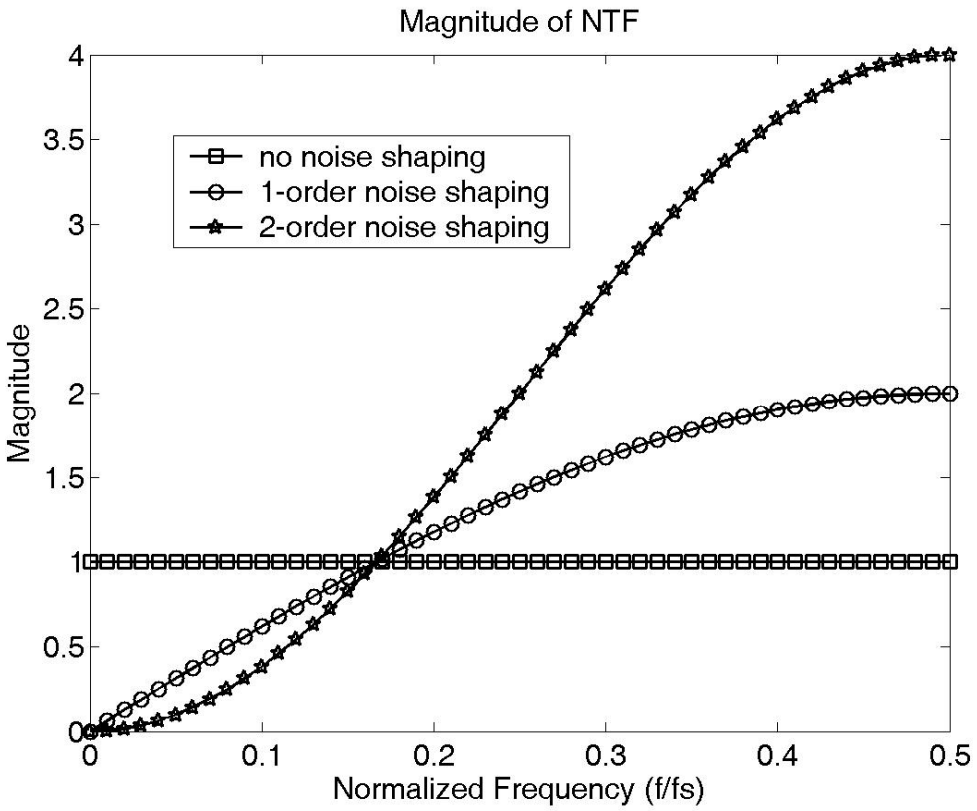


Figure 2.15 Magnitude of NTF

2.6.3 Higher-Order Sigma-Delta Modulator

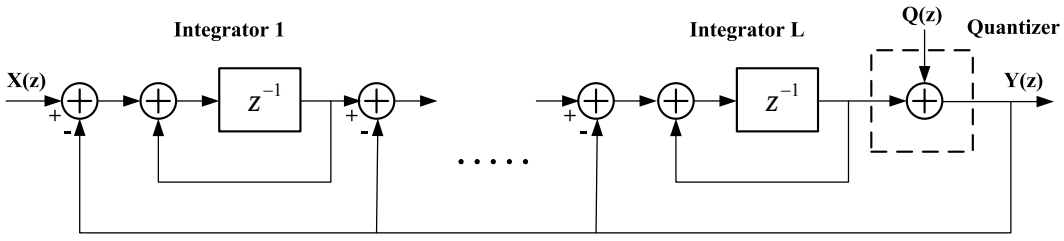


Figure 2.16 The Higher-Order SDM

Higher-order SDMs are divided into single-stage and multi-stage structures [07]. Figure 2.16 is the system block diagram of single-stage Lth-order SDM. Here, we will discuss the change of quantization noise and SNR when the number of order increases. With the same approach, we obtain the noise-transfer function, N_{TF} ,of the Lth-order SDM as follows:

$$N_{TF} = (1-z)^{L} \tag{2.35}$$

In a similar manner, the quantization-noise power over the signal band of the single-stage Lth-order SDM with N-bits quantizer is

$$\begin{aligned} P_{Q,noise} &= \int_{-f_b}^{f_b} S_Q(f)\cdot\left|N_{TF}(z)\right|^2 df = \int_{-f_b}^{f_b} \frac{\Delta^2}{12}\frac{1}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^{2L} df \\ &\approx \frac{\Delta^2}{12 f_s}\int_{-f_b}^{f_b}\left[2\left(\frac{\pi f}{f_s}\right)\right]^{2L} = \frac{\Delta^2}{12}\cdot\frac{\pi^L}{2L+1}\cdot\left(\frac{2f_b}{f_s}\right)^{2L+1} \\ &= \frac{\Delta^2\pi^{2L}}{12(2L+1)}\left(\frac{1}{OSR}\right)^{2L+1} \end{aligned} \tag{2.36}$$

Then the SNR of the single-stage Lth-order SDM is

$$SNR = 10\log\left(\frac{P_{signal}}{P_{Q,noise}}\right) = 10\log\left(\frac{\frac{V_A^2}{2}}{\frac{\Delta^2\pi^{2L}}{12(2L+1)}\left(\frac{1}{OSR}\right)^{2L+1}}\right)$$

$$= 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2\pi^{2L}}{12(2L+1)}\left(\frac{1}{OSR}\right)^{2L+1}}\right)$$

Finally, we get the result

$$SNR = 6.02b + 1.76 + 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \text{ dB} \qquad (2.37)$$

From equation (2.37), we know that for every doubling the OSR, the SNR will improve by (6L+3) dB (ie., resolution will increase L+0.5 bits). There are three ways to increase the SNR of a SDM. First, we can increase the bits of quantizer. The disadvantage is that multi-bit quantizer would induce harmonic distortion because of mismatch. Second, we can increase the number of order of a SDM. But it may have stability problem when the order is greater than 2. Third, increasing the OSR is the most popular way to improve the performance But for low power design, increasing

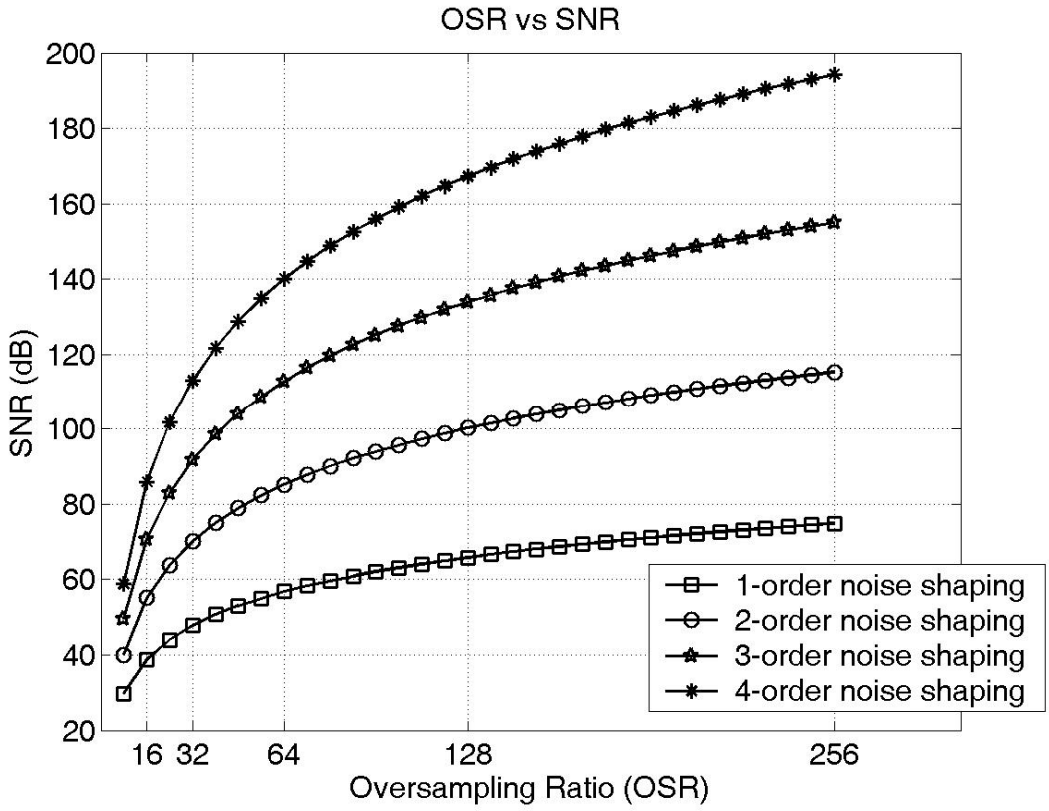


Figure 2.17 Plot of SNR versus SDM

the OSR is not suitable because the requirement of the integrators, such as settling time, bandwidth, and slew rate will be increased. Beside, the power of decimation filter will also be increased because of high sampling frequency. Figure 2.17 is the SNR of SDM. This plot provides a tradeoff between order, OSR and the power dissipation.

2.6.4 Multi-Stage Sigma-Delta Modulator (MASH) (Cascaded)

According the discussion above, we know that increasing the order of the SDM results in stability problems. There are many solutions to resolve the stability problem but may degrade the SNR of the system. This would significantly limit the benefits of increasing the order of the SDM. This problem can be overcome by employing cascaded-type structure. The cascaded SDM consists of several stages of first-order or second-order SDM and each stage converts the quantization error of the previous stage. Since the lower order SDMs are more stable, the system should remain stable [08] [09]. It is attenuated by the noise-shaping function of order equal to overall of cascaded [10]-[12].

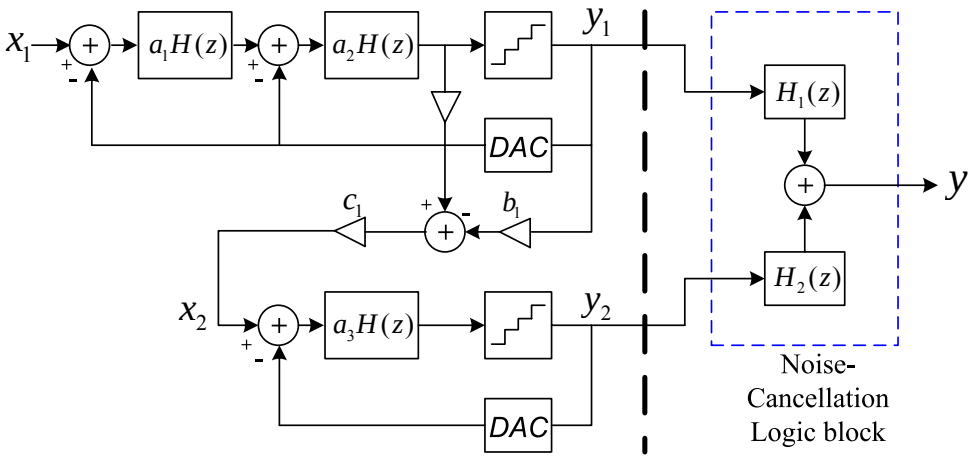


Figure 2.18 Block diagram of Multi-Stage SDM

Figure 2.18 is the block diagram of a third-order cascaded 2-1 SDM [01] [13]. The first stage is a second-order SDM and the second stage is a first-order SDM. The input of the second stage is the quantization noise from the first stage. The digital output of the second stage may contains both shaped and unshaped quantization noise of the first stage and also first-order shaped quantization noise form the second stage. The outputs of both the first stage and second stage will be combined and processed by the noise-cancellation logic which is shown in the right of Figure 2.18 (dashed line block) to cancel the shaped and unshaped quantization noise of the first stage. The operation will be discussed. For the first stage, the output of second-order SDM is

$$Y_1(z) = z^{-2} \cdot X(z) + \left(1 - z^{-1}\right)^2 \cdot E_1(z) \tag{2.38}$$

And for the second stage, the output of first-order SDM is

$$Y_2(z) = z^{-1} \cdot X(z) + \left(1 - z^{-1}\right) \cdot E_2(z) \tag{2.39}$$

Here, the $E_1(z)$ and $E_2(z)$ represent the quantization error of the first stage and second stage. And the output of the cascaded 2-1 structure can be written as

$$Y(z) = Y_1(z) \cdot H_1(z) + Y_2(z) \cdot H_2(z) \tag{2.40}$$

We can choose that

$$H_1(z) = z^{-1} \tag{2.41}$$

$$H_2(z) = \left(1 - z^{-1}\right)^2 \tag{2.42}$$

And the resulting output of the cascaded 2-1 topology is calculated by combining (2.38)-(2.42)

$$Y(z) = z^{-3} \cdot X(z) + \left(1 - z^{-1}\right)^3 \cdot E_2(z) \tag{2.43}$$

So the output of the overall system will only contain a delayed version of the input signal and the quantization noise of the second stage to achieve third-order noise-shaping. Unfortunately, the cascaded topology is not so perfect. If non-idealities appear in the SDM, the quantization error of the first stage will not be perfectly removed by the digital noise-cancellation logic and can become visible at the output of the converter. The degree of the cancellation depends on how well analog implementation of the $H(z)$ match the inverse of the digital implementation of $H^{-1}(z)$. If there are some mismatches between analog and digital circuit, noise-leakage will occur and degrade the performance of the system.

In a similar way, the cascaded topology can be used to generate fourth-order noise shaping converters. We can choose 2-2 cascaded topology consisting of two second-order stages or a 2-1-1 cascaded topology consisting of a second-order stage followed by two first-order stages. The output of two kinds of cascaded topology for fourth-order can be shown as

$$Y(z) = z^{-4} \cdot X(z) + \left(1 - z^{-1}\right)^4 \cdot E_2(z) \quad \text{for 2-2 cascaded} \tag{2.44}$$

$$Y(z) = z^{-4} \cdot X(z) + \left(1 - z^{-1}\right)^4 \cdot E_3(z) \quad \text{for 2-1-1 cascaded} \tag{2.45}$$

They have the similar properties for noise-shaping. And the principle of cascaded converters can also be applied to generate fifth and higher-order converters.

2.6.5 Multi-bit Sigma-Delta Modulator

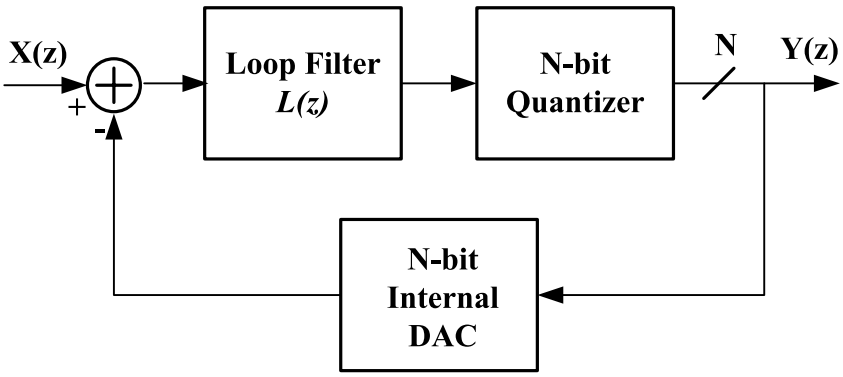


Figure 2.19 Block diagram of multi-bit SDM

The feedback of the SDM can be implemented in different ways. From previous chapters, we had introduced several N-order single-bit SDMs. Here, we will discuss the multi-bit SDM. Figure 2.19 is the block diagram of multi-bit SDM, and the single-bit quantizer and DAC were replaced with multi-bit quantizer and internal DAC. Single-bit SDM has good linearity but have problems such as easy to induce idle tone, sensitive to clock jitter, and poor to improve the performance. The primary advantage of multi-bit SDM is that the signal to total quantization noise power is effectively increased compared with that just employing single-bit quanitzer. Generally, increasing each bit improve the performance by 6dB. It means that we can improve the performance just employing multi-bit topology without increasing the order or OSR. In other words, the lower-order multi-bit, low-OSR multi-bit, and higher-OSR single-bit SDMs may have nearly the same performance. But the power dissipation will be the lowest due to relaxing the requirement of SDM such as digital decimation filter or integrator for only using multi-bit technique. The major disadvantage of multi-bit quantizer is its lack of linearity and resulting in increasing the total harmonic distortion due to the component mismatch of quantizer and internal

DAC. Therefore, it needs a high precise calibration circuit to achieve high linearity and low total harmonic distortion.

There are a lot of methods to compensate the non-ideal internal DAC to improve the overall performance. The most common approach to reduce the linearity requirements of the internal DAC is offered by dynamic element matching (DEM) technique. Originally, this technique was proposed to improve the accuracy of DACs. But it is very suitable to improve the accuracy of the internal DAC in multi-bit SDM. The operation principle is illustrated in Figure 2.20. The binary input-code of the DAC is transformed into a thermometer-code of $2^N - 1$ bit lines. Then the element selection logic will select different unit elements to represent a certain input code. For a traditional DAC without DEM, the errors due to some process variations are fixed for the same input codes. But for DAC with DEM, the unit elements selected by the element selection logic may have positive contribution or negative contribution in each clock period. Therefore, a time-vary error signal results. The errors introduced

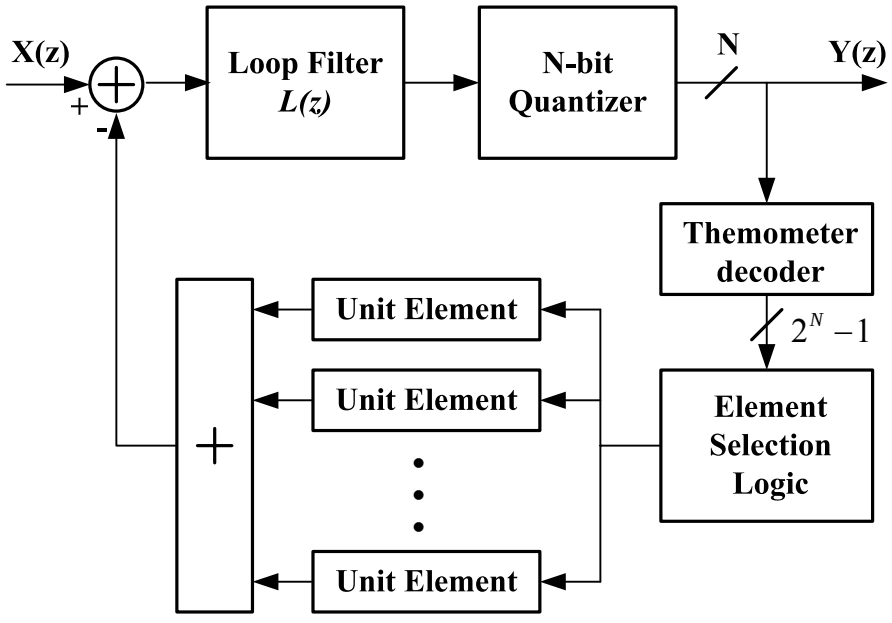


Figure 2.20 Block diagram of multi-bit SDM with DEM

by the internal DAC average to zero over multiple time instances. The errors due to component mismatch are moved to higher frequencies and can be removed by filtering.

2.6.6 System Analysis of Sigma-Delta Analog-to-Digital Converters

The system architecture for a typical oversampling ADC is shown in Figure 2.21. The anti-aliasing filter is used to filter the out-of-band noise of original input signal to avoid noise folding into signal band. Then, the signal is sampled and held and applied to a SDM and output a 1-bit digital signal. Usually, the sample-and-hold usually combines with the SDM. These three blocks are belonging to analog domain. A decimation filter which contains a digital low-pass filter and a down-sampling not only suppresses the out-of-band quantization noise but also down-sample the sampling frequency from f_s to Nyquist-rate [14]. Note that the digital low-pass filter here is like an anti-aliasing filter to limit signals to one-half the output sampling rate. The decimation filters generally are implemented using digital circuit technique in order to reduce the power dissipation and are easy to implement. Figure 2.22 shows the signal and spectra of each stage of oversampling ADC [15].

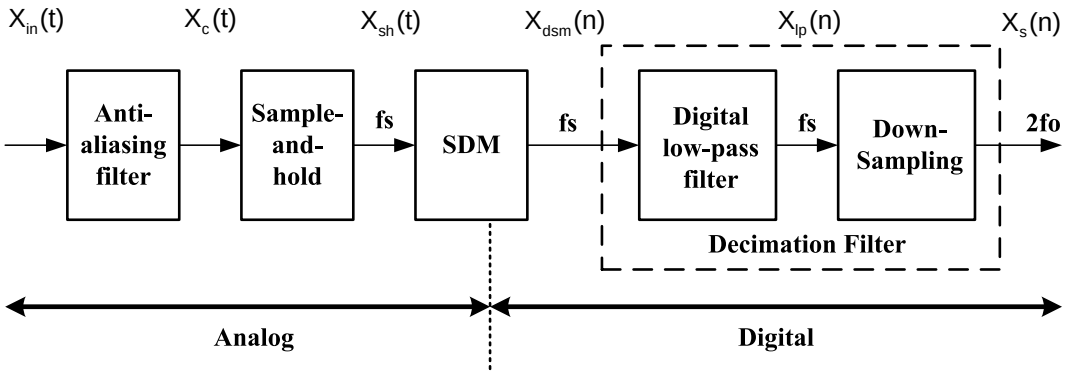


Figure 2.21 Block diagram of an oversampling A/D converter

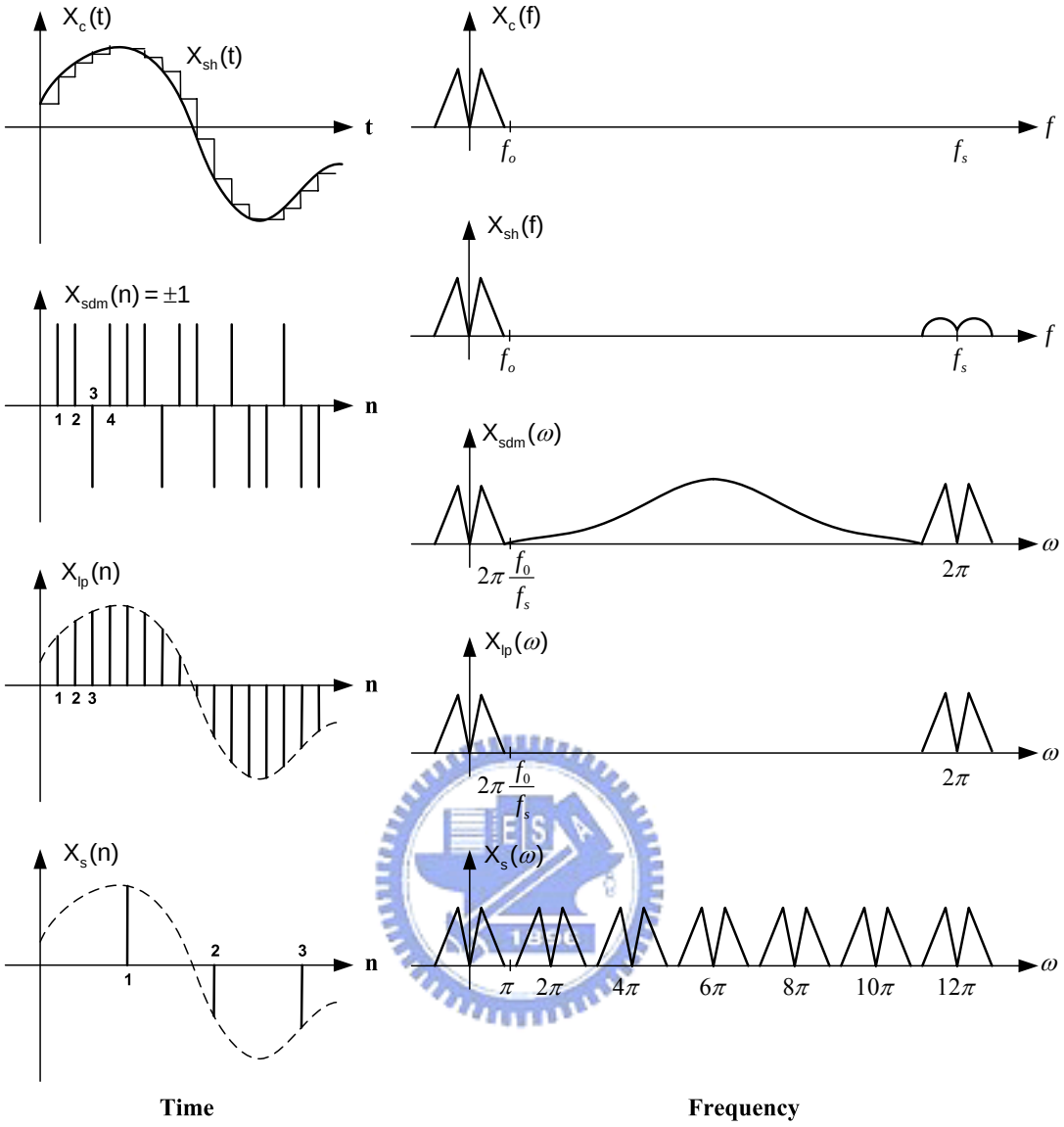


Figure 2.22 Signal and spectra in an oversampling ADC

2.6.7 System Analysis of Sigma-Delta Digital-to-Analog Converters

The system architecture for a typical oversampling DAC is shown in Figure 2.23. The input signal is a multi-bit signal and has an equivalent sample rate of Nyquist-rate and is sent into the interpolation filter. The interpolation filter is a digital brick-wall-type filter that passes 0 to $2\pi f_0 / f_s$ and rejects all other image signals. The interpolation filter also rise the sampling rate of input signal frequency from

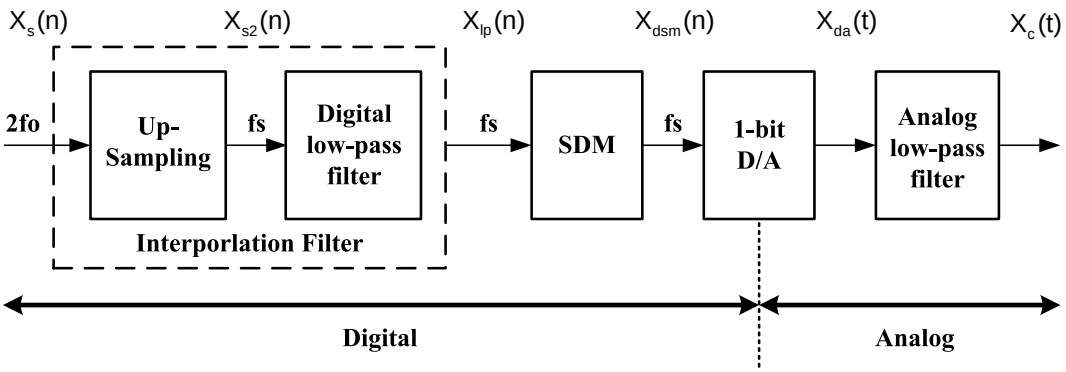


Figure 2.23 Block diagram of an oversampling D/A converter

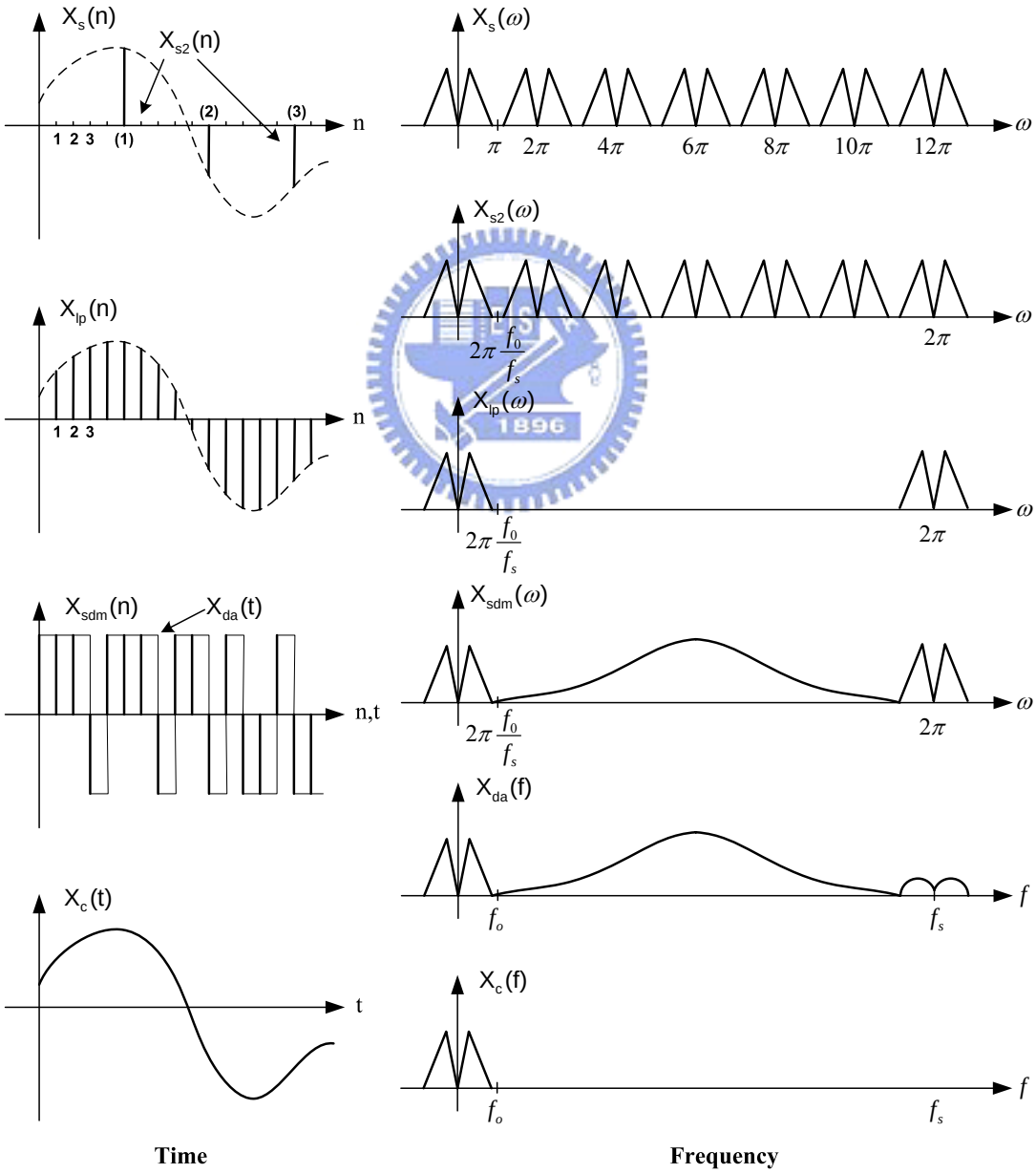


Figure 2.24 Signal and spectra in an oversampling DAC

Nyquist-rate to f_s. Then the output signal is applied to a fully digital SDM and a 1-bit output signal is generated by the digital SDM. The 1-bit output signal contains not only the original signal but also include a large amount of shaped quantization noise. After processing by the 1-bit DAC, the signal has good linearity but still has a large amount of out-of-band quantization noise. Finally, the desired output signal can be obtained by using an analog filter to filter out this out-of-band quantization noise to recover the original signal. The analog filter is also called the smooth-filter and its specification can be relaxed by the properties of using the oversampling. Figure 2.24 shows the signal and spectra of each stage of oversampling DAC

2.7 Summary

In this chapter, we have introduced the basic principles of sigma-delta modulator. Among these, the most important is the properties of shaped quantization error. Here, various architectures of SDM such as single-loop and cascaded was introduced and compared. And then, the advantages and disadvantages of multi-bit quantizer was described and analyzed. In the final part of this chapter, we discuss how the signal and spectra change in different section of the oversampling ADC and DAC. This would make us much clear about the operation of oversampling system.

Chapter 3

Basic Concept of Continuous-Time SDM Techniques

3.1 Introduction

Most of the SDMs are implemented with loop filters using discrete-time circuit techniques. The most popular techniques are switched-capacitor (SC) technique and switched-current (SI) technique. It is easy to map the mathematics of modulators onto the implementation. Beside, the discrete-time techniques are compatible with modern digital CMOS processing since high-quality capacitors are usually capable whereas high quality resistor are not. But the discrete-time techniques have some limitation for high-speed implementation due to settling-time constrains in typical discrete-time implementation and maximum clock rate is limited by the operation amplifiers used as integrators. For ideally consideration, resolution of SDM is determined only by the loop filter and the oversampling ratio. But if we overcome the clock rate restrictions, a high resolution converter with wider bandwidth for a given oversampling ratio and loop filter could be built. Continuous-time (CT) modulators have lower thermal noise levels than switched-capacitor modulators. Achieving the same in-band noise level as a low-valued resistor may require an unrealistically large value of a switched capacitor. Also, continuous-time modulators have inherent anti-aliasing filter and may have less power consumption and aliasing problems than switched capacitor design.

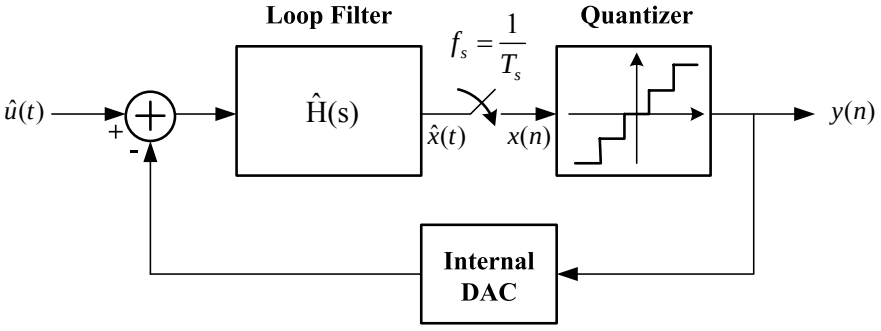
For continuous-time technique, another consideration is the property of low power

dissipation. Continuous-time modulators have received increasing attentions over the last several years due to meaningful and attractive advantages for power-saving over switched-capacitor discrete-time (DT) counterparts. First, the restrictions on the amplifier gain-bandwidth product (*GBW*) are relaxed for a fixed sampling frequency compared with the DT counterparts [16]. Second, CT loop filters have free anti-aliasing, and thus the use of a high order anti-alias filter at the front of the system is not necessary [17]. This results in further area decreasing and power-saving (Otherwise, a CT ΣΔ ADC can operate at higher frequencies). On the other hand, the CT ΣΔ ADCs are more sensitive to clock-jitter, extra loop delay, and nonlinearity of the integrators. These drawbacks will decrease the performance of the ΣΔ ADCs.

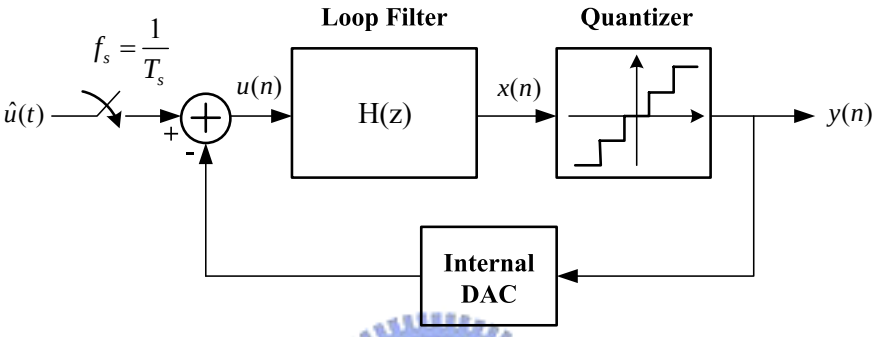
3.2 Discrete-Time versus Continuous-Time SDM

We have discussed some different properties between discrete-time and continuous-time SDMs. Now, we will discuss more about the differentia of using continuous-time and discrete-time SDMs.

The first important difference is the location of the sampling operation. For a discrete-time SDM, the input signals are sampled at the input of the SDM. Therefore, any non-linear effect introduced by the sampling operation directly infects the input signal especially when the supply voltage is reduced in deep sub-micron CMOS technologies. In a continuous-time SDM, the sampling operation is performed by the quantizer and the non-idealities of the sampling operation are subject to the same shaping as the quantization error. Therefore, the errors due to the sampling operation are less importance. The operation of sampling for both discrete-time and continuous-time are shown in Figure 3.1.



Continuous-Time SDM



Discrete-Time SDM

Figure 3.1 Different operation of sampling for continuous-time and discrete-time SDMs

The second difference is the implementation of the feedback DAC signal. For discrete-time SDMs, the feedback DAC is applied by sampling the reference voltage on a capacitance and integrating this charge. For continuous-time SDM, a continuous-time feedback DAC waveform is integrated and the SDM is sensitive to the exact waveform of the feedback DAC pulse. So the continuous-time SDMs are more sensitive to clock jitter since it affects the edges of the feedback pulses.

The third difference is the implementation of the integrators. The gain of the discrete-time integrators is determined by the ratio of the capacitors C_S and C_I which was shown in Figure 3.2. The relative matching of capacitors is accurately controlled and accuracies of 0.1% or better can be achieved in present technologies.

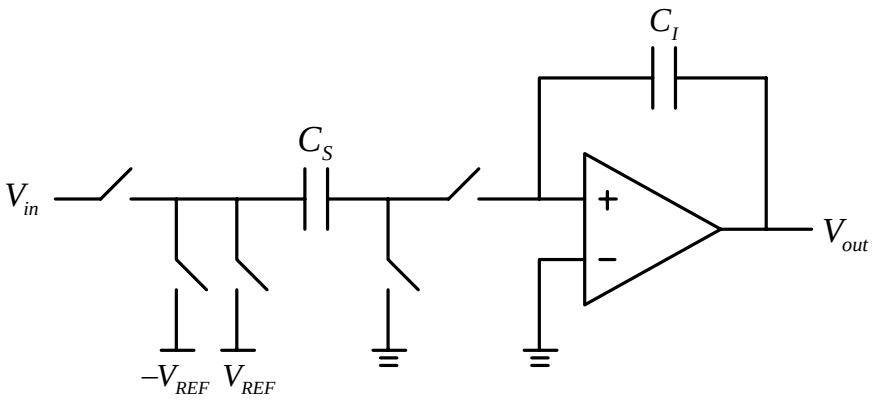
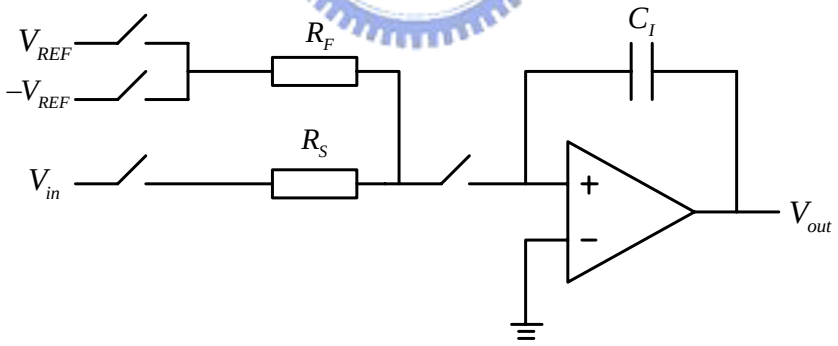
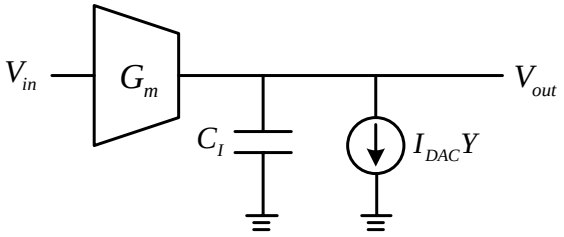


Figure 3.2 Discrete-time switched-capacitor integrator

In contrast to this, the gain of the two continuous-time integrators shown in Figure 3.3 is determined by the inverse of $R_S C_I$ for the active RC implementation and the ratio of G_m to C_I for the $G_m C$ implementation. The gain is now sensitive to the absolute variations of elements, errors up to 20% can occur due to process variations and temperature effects.



(a)



(b)

Figure 3.3 Continuous-time implementation of an integrator

3.3 Ideal Continuous-Time SDM Design

Up to now, there is a large amount of literatures to talk about the discrete-time SDM design. And it is easy to find a lot of software to help us choose the parameters for a given resolution and speed requirement. Although we have no tool to simulate the continuous-time SDM directly, there are still some ways to help us design the continuous-time loop filter with no extra work. Schreier presents a state-space method to design ideal CT SDMs [03]. Here, we will discuss the method of the *impulse-invariant transform* which is proposed by Cherry [17].

3.3.1 The Impulse-Invariant Transform

In a CT implementation, there is no sampling operation at the input of the converter. Instead, the sampling is performed by the quantizer. For this reason, the DT open loop filter *H(z)* can be replace by a CT equivalent *H(s)* with respect to the DAC feedback impulse response. Thus, design and simulation of the CT ΣΔ ADCs can be done by calculating the function of the DT ΣΔ ADCs with the method of impulse invariant transformation. The discrete-time modulator has a continuous-time equivalent which can be found through a transformation between the discrete-time and continuous-time domains. It will be shown that impulse responses of the continuous-time and discrete-time SDMs are the same. We can see the Figure 3.1 again, assume the inputs of two modulators are the same and both two modulators are operated in the time-domain. If the outputs of them are the same sequences, then we can guarantee that they are likely to be equivalent modulators. In others words, if we confirm the inputs of their quantizers are the same at a given sampling instant, each quantizer would then make the same decision and thus outputs will be produced the

same bits. And then the same bits would be operated with the same input voltage to produce the same input voltage of the quantizer at the next sampling instant.

$$x(n) = \hat{x}(t)\,|_{t=nT_s} \tag{3.1}$$

This would be satisfied if the impulse response of the continuous-time and discrete-time SDMs are equal at sampling times.

$$\mathcal{Z}^{-1}\{H(z)\} = \mathcal{L}^{-1}\left\{\hat{R}_D(s)\hat{H}(s)\right\}\,|_{t=nT_s} \tag{3.2}$$

or in the time domain

$$h(n) = \left[\hat{r}_D(t) * \hat{h}(t)\right]\,|_{t=nT_s} = \int_{-\infty}^{\infty} \hat{r}_D(\tau)\hat{h}(t-\tau)d\tau\,|_{t=nT_s} \tag{3.3}$$

Where $\hat{r}_D(t)$ is the impulse response of the feedback DAC. This transformation between continuous-time and discrete-time is called the impulse-invariant transformation. Thus, suppose we have a discrete-time modulator with a filter $H(z)$ with particular noise-shaping behavior, we can create a continuous-time modulator with identical noise-shaping behavior by first choosing a DAC pulse shape $\hat{r}_D(t)$. And then we can use equations (3.2) and (3.3) to find $\hat{H}(s)$.

To actually do the transform, we proceed as follows. First, we write $H(z)$ as a partial fraction expansion. Then we choose a DAC pulse shape. We can assume a perfectly rectangular DAC pulse of magnitude 1 that from α to β. It can be shown as equation (3.4) and Figure 3.4. This covers most types of practical DAC pulse. Finally,

$$\hat{r}(\alpha,\beta)=\begin{cases}1, & \alpha \le t < \beta,\ 0 \le \alpha < \beta \le 1\\ 0, & \text{otherwise.}\end{cases} \tag{3.4}$$

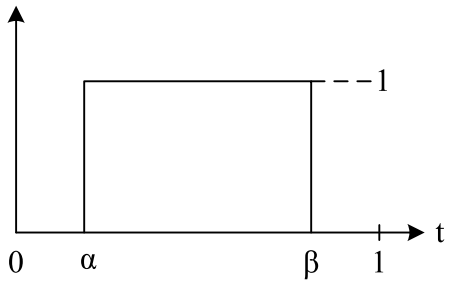


Figure 3.4 DAC pulse

we use Table 3.1 to convert each partial fraction pole from *z* to *s*. Then we will obtain the result of $\hat{H}(s)$. For example, if we use the DAC type, (α, β)=(0,1) in (3.4). And the transfer function is

$$H(z)=\frac{-3z+2}{(z-1)^2} \tag{3.5}$$

Table 3.1 s-domain equivalences for z-domain loop filter poles [17]

z-domain pole	Limit for $z_k=1$
$\frac{y_0}{z-z_k}$	$\frac{r_0}{s-s_k}$, $r_0=\frac{y_0}{\beta-\alpha}$
$\frac{y_0}{(z-z_k)^2}$	$\frac{r_1 s+r_0}{(s-s_k)^2}$, $r_0=\frac{y_0}{\beta-\alpha}$ $r_1=\frac{1}{2}\frac{(\alpha+\beta-2)y_0}{\beta-\alpha}$
$\frac{y_0}{(z-z_k)^3}$	$\frac{r_2 s^2+r_1 s+r_0}{(s-s_k)^3}$, $r_0=\frac{y_0}{\beta-\alpha}$ $r_1=\frac{1}{2}\frac{(\alpha+\beta-2)y_0}{\beta-\alpha}$ $r_2=\frac{1}{12}\frac{y_0}{\beta-\alpha}\left[\beta(\beta-9)+\alpha(\alpha-9)+4\alpha\beta+12\right]$

Then we write this in partial fractions yields

$$H(z) = \frac{-3}{z-1} + \frac{-1}{(z-1)^2} \tag{3.6}$$

Applying the first row of Table 3.1, we obtain

$$\hat{H}(s) = \frac{-3}{s} + \frac{-1+0.5s}{s^2} = -\frac{-1+2.5s}{s^2} \tag{3.7}$$

Then we had transformed the $H(z)$ to $\hat{H}(s)$ and obtain the new coefficients for continuous-time SDM.

3.3.2 Effect of Excess Loop Delay

Continuous-time SDMs suffer a problem not seen in discrete-time design. That is the excess loop delay [18]. Excess loop delay arises because of nonzero delay between the quantizer clock edge and the time when a change in output bit is seen at the feedback point in the modulator. It arises because the nonzero switching time of the transistors in the feedback path. Its effect is severe if the sampling clock speed is an appreciable fraction of the maximum transistor switching speed.

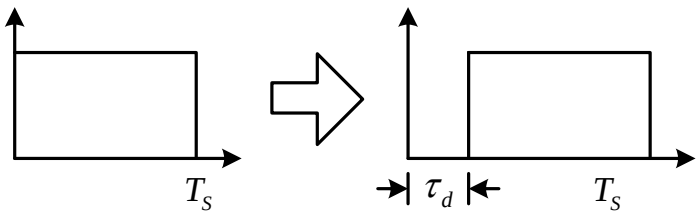


Figure 3.5 Illustrations of excess loop delay on NRZ DAC pulse

Chapter 4

Implementation of Low-Power Continuous-Time SDM

4.1 Introduction

In this chapter, we will introduce the implementation of a 3rd-order continuous-time sigma-delta modulator. In section 1, we will show the behavior simulation of the SDM. In section 2, we will discuss the circuit level design of the SDM. In section 3, we will show the performance and layout of the SDM.

4.2 Behavior Simulation

Figure 4.1 is the system architecture of third-order continuous-time SDM. Before the circuit level implementation, we need to simulate the behavior of the system. Here, we used Simulink to simulate and analysis the system performance. We need to simulate the third-order SDM in discrete-time domain as discuss above. Then we transform the coefficients from discrete-time domain to continuous-time domain.

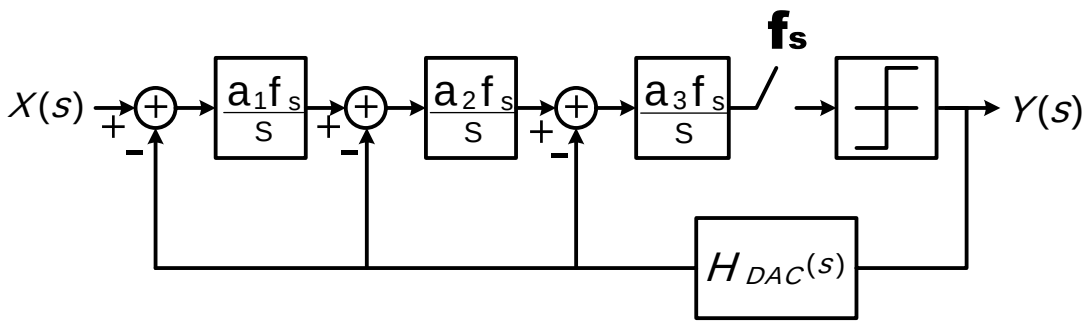


Figure 4.1 Third-order continuous-time SDM

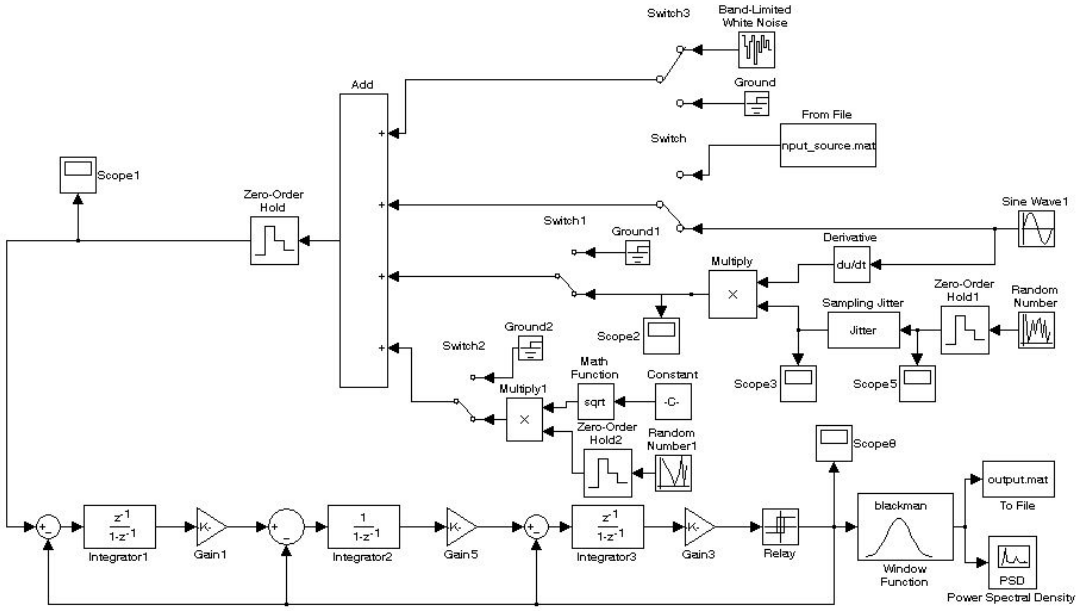


Figure 4.2 Behavior model of third-order SDM

Figure 4.2 is the behavior model of the third-order SDM [19]-[21]. The upper section is the noise source simulation and the lower section is the simulation of the SDM. The time-domain output datas is shown in Figure 4.3 and the plot of power spectrum density is shown in Figure 4.4.

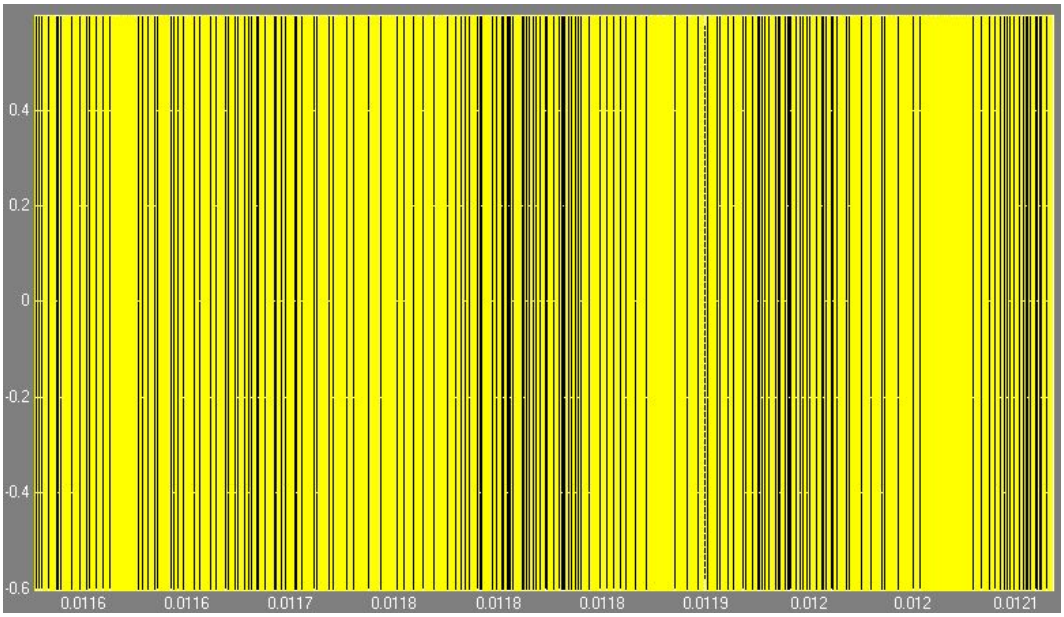


Figure 4.3 Simulation result in time-domain

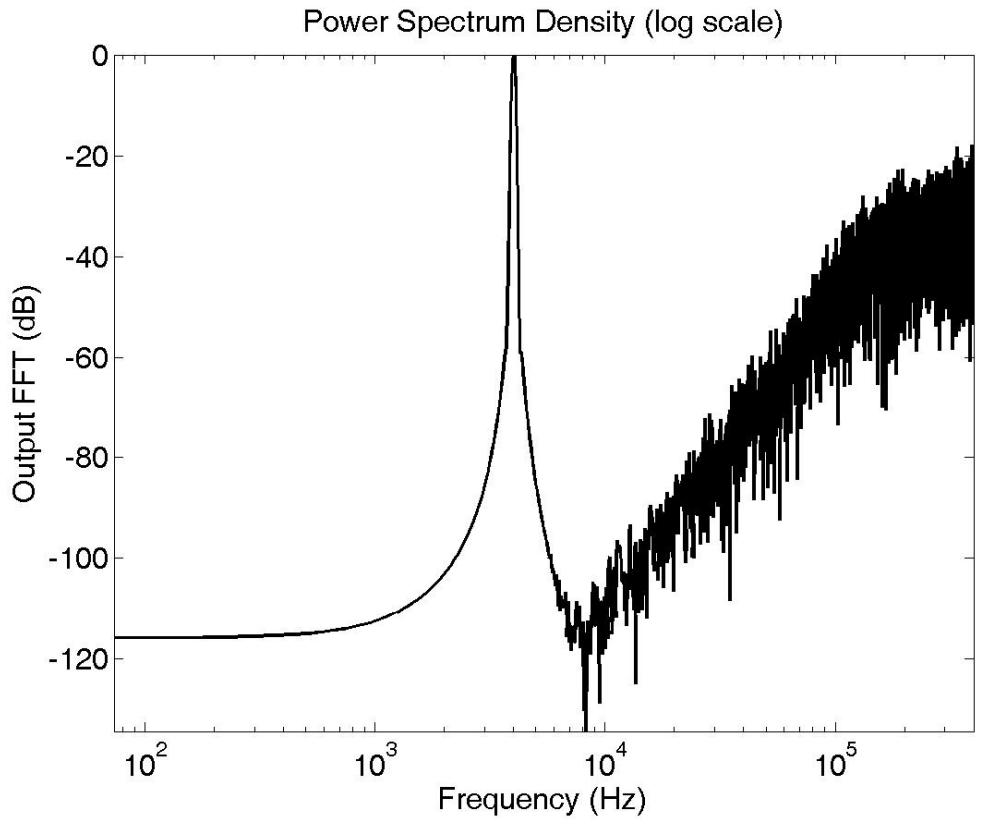


Figure 4.4 Output power spectrum density of behavior model

4.3 Circuit Level Implementation

From the system level simulation, we can predict and obtain the system performance roughly. There are many ideal components in the system level simulation. But for circuit level implementation, there are more detail considerations in the design. We will discuss the circuit level implementation of each component for the 3-order continuous-time SDM. For low-power application the single loop architecture as shown in Figure 4.1 is the preferred structure over cascaded architecture. The reason is that the single loop topologies do not have stringent specification for the integrator of the modulator except for the first stage. The advantage of using distributed feedback is insensitive to parameter variation. And Figure 4.5 is the implementation

of continuous-time SDM. The modulator consists of three building blocks : a CT loop filter, a clocked quantizer, and a feedback DAC. The modulator is fully differential circuit and the filter is implemented using three active *RC*-integrators. The detail circuit implementation for each component will be discussed in next several sub-chapters.

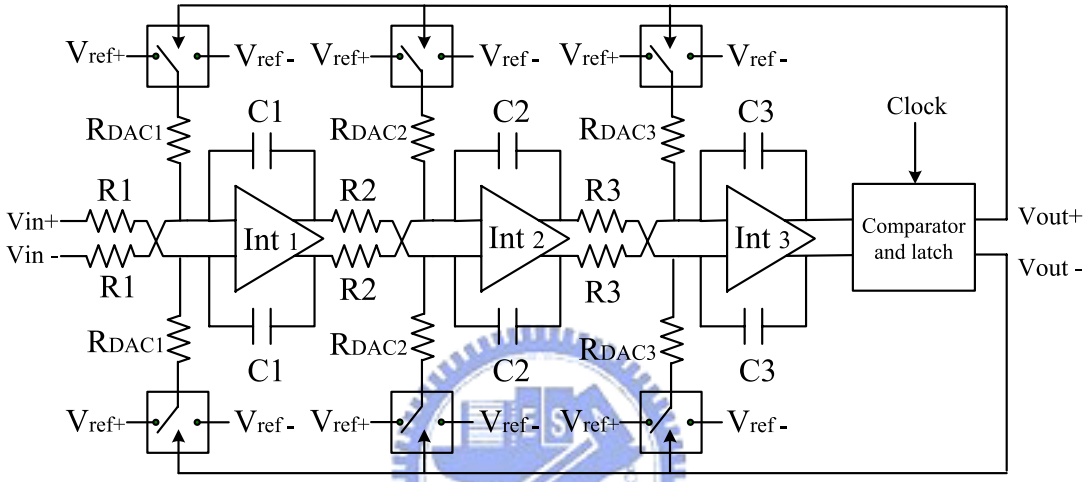


Figure 4.5 Implementation of third-order continuous-time SDM

4.3.1 Integrator

The major contributor of the ΣΔ modulator overall power dissipation is the first integrator when using single-loop architecture. Therefore, optimizing the performance of amplifier for what we need is very important. A proper circuit can save a substantial amount of power consumption. The specification of the first integrator influences the overall system performance very much. The finite DC-gain, distortion, and noise of the first integrator reduce performance of the entire ADCs since these errors add directly to the input signal. In order to achieve both the high gain and low-power requirement, a folded-cascode amplifier with simple common-mode

feedback (CMFB) has been chosen (Figure 4.6) [22]. The CMFB is operated with two transistors biased in linear region. The open-loop gain and gain-bandwidth (GBW) are shown as follows:

$$G_m \approx g_{m1,2} \tag{4.1}$$

$$\begin{aligned} |A_V| = G_m R_{out} = g_{m1,2}(g_{m6,7} + g_{mb6,7}) \cdot \\ r_{o6,7}(r_{o1,2} \| r_{o4,5}) \cdot (g_{m8,9} r_{o8,9} r_{o10,11}) \end{aligned} \tag{4.2}$$

and

$$GBW = \frac{G_m}{C_L} = \frac{g_{m1,2}}{C_L} \tag{4.3}$$

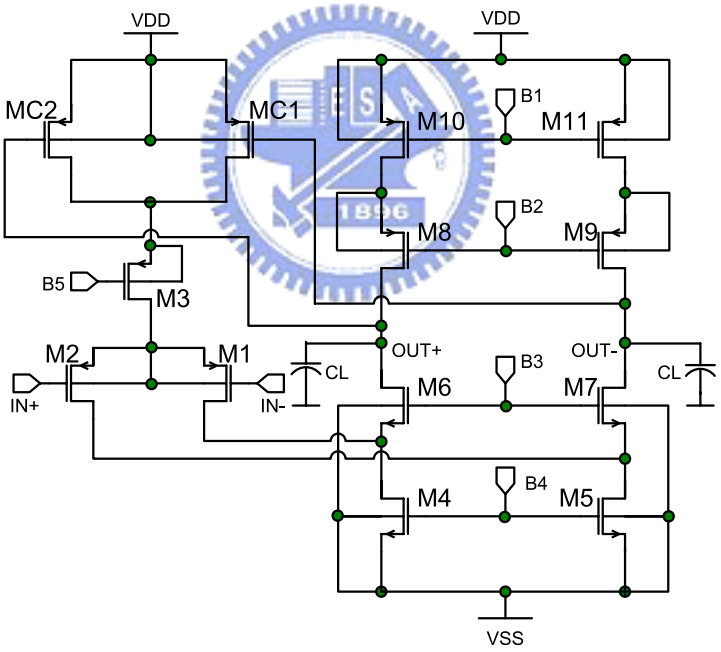


Figure 4.6 Schematic of implemented amplifier

The differential *RC*-integrator is shown in Figure 4.7. The transfer function of the *RC*-integrator is given by [23] :

$$H(s) = -\frac{1}{RCs} \cdot \frac{1}{1 + \frac{s}{GBW} + \frac{1}{GBW \cdot RC}} \tag{4.4}$$

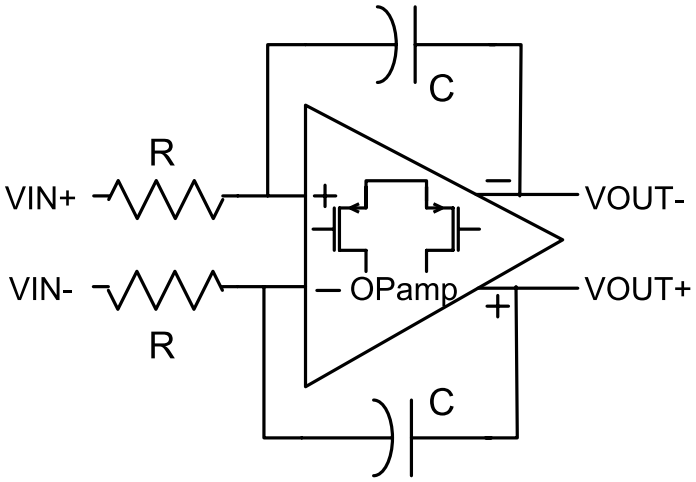


Figure 4.7 Differential *RC*-integrator

In order to achieve a good approximation of the ideal integrator, the term of gain error $1/(GBW \cdot RC)$ and phase error s/GBW must be minimized. Thus, a high amplifier GBW is required to reduce the integrator error as shown in Equation (4.4). The distortion of first integrator influences the overall performance much more than others. The dominant sources of distortion are the PMOS input pair which is operated in strong inversion. The third harmonic distortion and power consumption of the first integrator is [24] :

$$HD_3 \approx \frac{\hat{V}_{in}^2}{64\, g_{m1}\, R_{in}^3\, I_{ds1}^2}\left(1 + \frac{R_{in}}{R_{DAC}}\right) \tag{4.5}$$

$$P = \frac{V_{DD}\hat{V}_{in}^2}{4R_{in}}\sqrt{\frac{1}{g_{m1}HD_3}\left(\frac{1}{R_{in}} + \frac{1}{R_{dac}}\right)} \tag{4.6}$$

The relationships among the harmonic distortion, the power consumption, input transconductance g_{m1}, input resistance R_{in}, DAC feedback resistance R_{DAC}, and bias current I_{DS1} are shown in Equation (4.5) and (4.6). Power consumption can be reduced to optimum condition by increasing R_{in} and R_{DAC} up to the thermal noise limit. And the larger the input pair transconductance, the less the power dissipation.

The gain-bandwidth and phase-margin plot are shown in Figure 4.8 and the complete simulation of the amplifier of the amplifier results are shown in Table. 4.1.

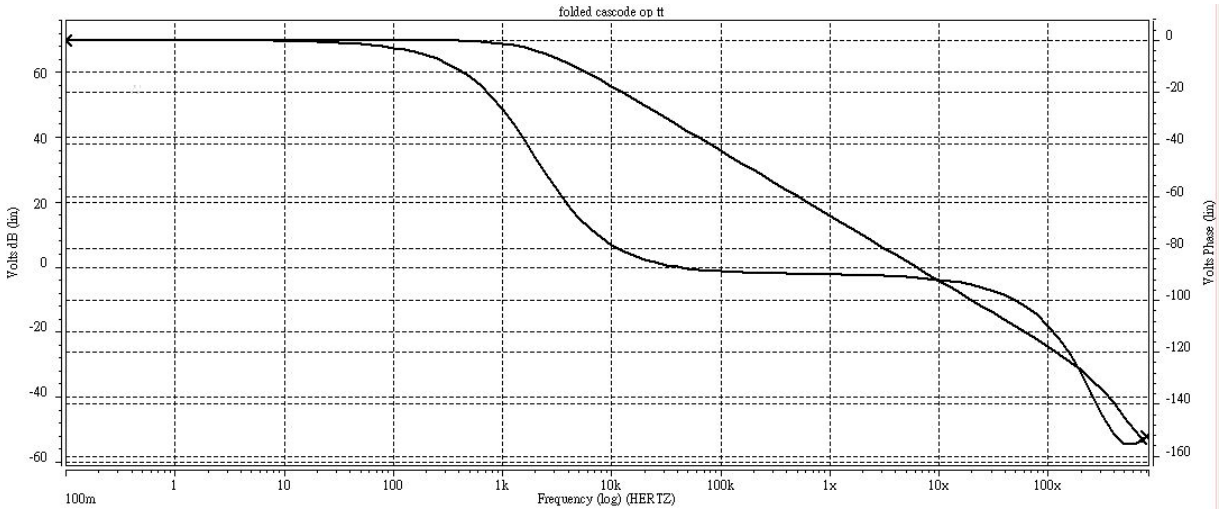


Figure 4.8 Gain-bandwidth and phase-margin of OPAMP

TABLE 4.1 Specification of the first amplifier

Parameters	***Simulation Result***
DC gain	**70 dB**
Phase Margin	**88.7 degree**
Unity Gain Frequency	**6.5 MHz**
Slew Rate	**5V/μs**
Settling Time	**20 ns**
Output Swing	**0.3V~1.5V**
Power Dissipation	**44μW**
Technology	**Standard TSMC 0.18μm 1P6M**

4.3.2 Comparator and Latch

For low-power consideration, a fully symmetrical regenerative comparator suitable for CT ΣΔ ADCs was used [25] [26]. The PMOS input devices are operated in the linear region. When the clock goes high, the comparator is reset. When the clock goes low and input voltage VIN+ is higher than VIN-, the current through M1 is higher than M2. The drain voltage of M5 or M7 is rise up to VDD through a latch and the drain voltages of M6 and M8 are pulling down to 0 in the same way. So VOUT+ is high and VOUT- is low through an inverter. In the same way the VOUT+ is low and the VOUT- is high when the input voltage VIN- is higher than VIN+. In order to increase the output range, we connect the body to the source. The comparator is shown in Figure 4.9.

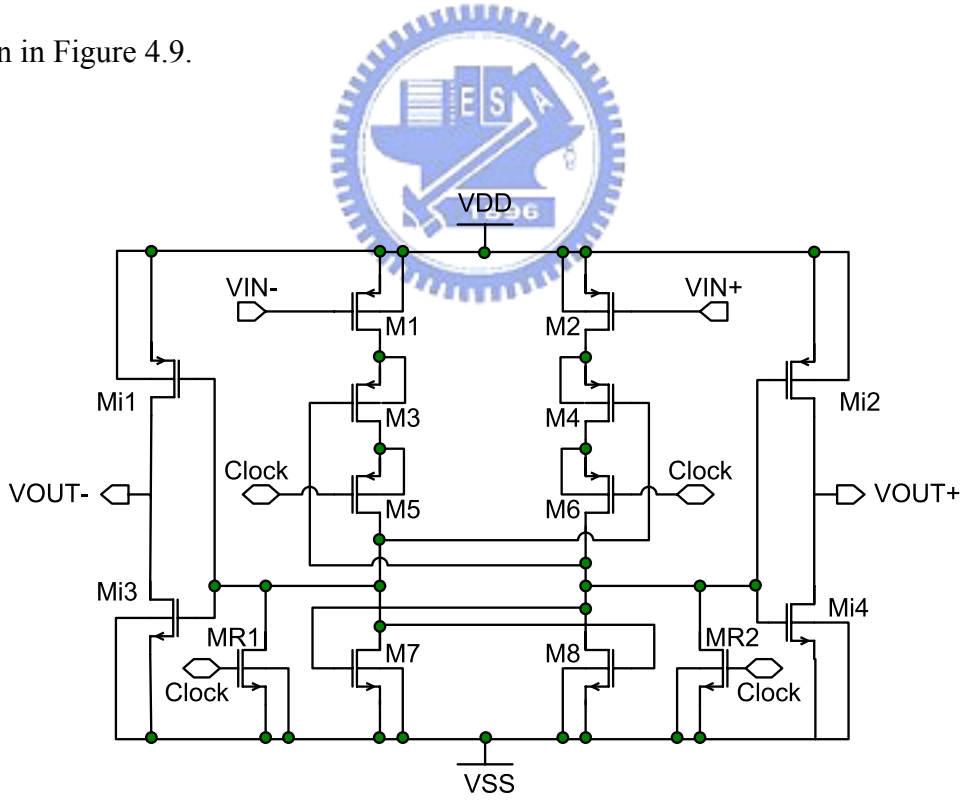


Figure 4.9 Schematic of implemented comparator

In order to lock the output state of the comparator, we need to add a SR-latch behind the comparator to lock the signal during one clock period. The circuit is shown in Figure 4.10. The simulation of comparator and SR-latch is shown in Figure 4.11. The upper plot is the input signal and the lower plot is the output signal of comparator followed by a SR-latch.

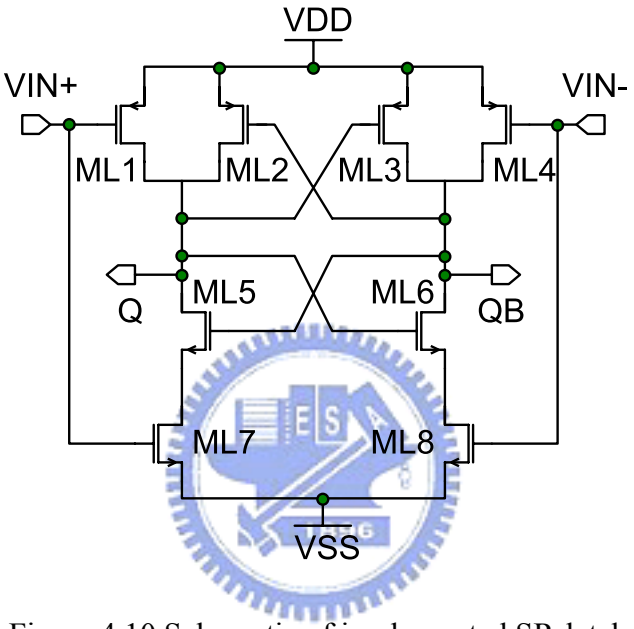


Figure 4.10 Schematic of implemented SR-latch

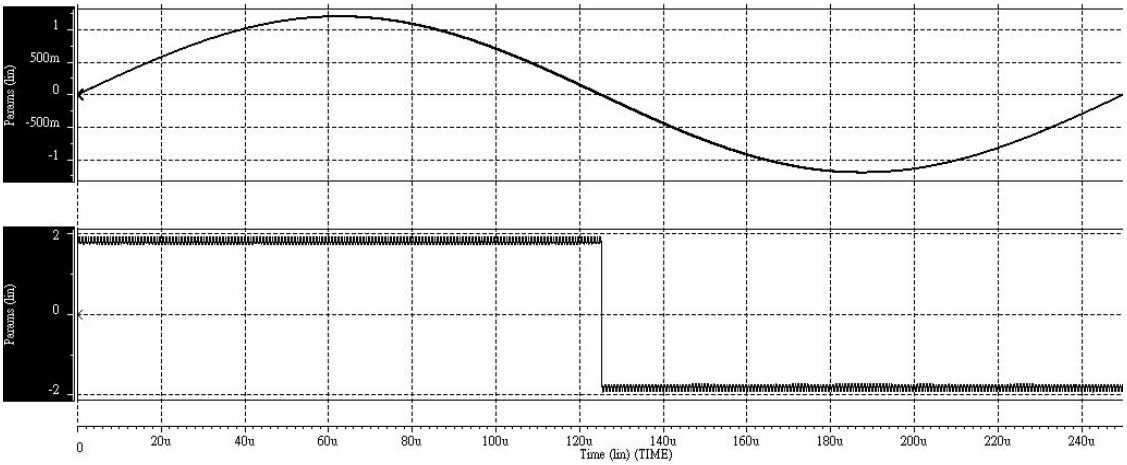


Figure 4.11 Simulation result of comparator

4.3.3 Feedback DAC

From view of system level design, the feedback DAC is used to generate signals to feedback into *RC*-integrators. The single-bit NRZ feedback DAC is shown in Figure 4.12 [27]. The feedback DAC has to output pairs of signal when fed complementary input. For tracking input signal, these output signals are generally reference voltages. It has four transmission-gate switches with near minimum size. The switches are controlled by the output state of the SR-latch. The positive reference voltage (Vref+) is 1.1V and negative reference voltage (Vref-) is 0.5V.

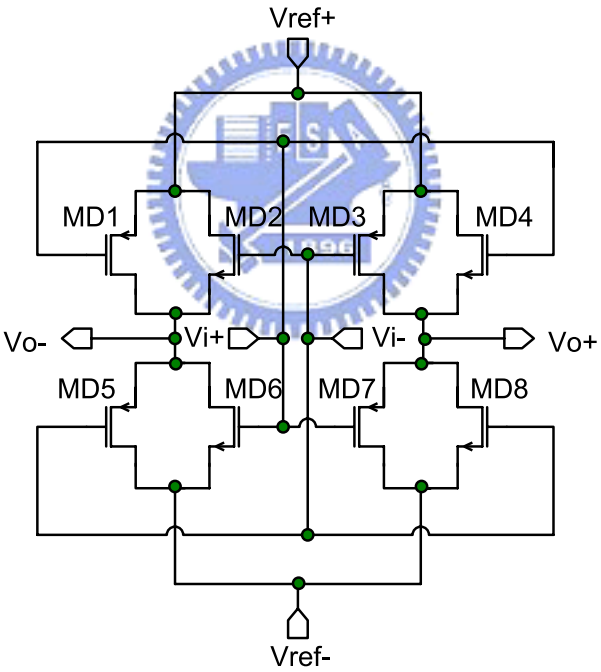


Figure 4.12 Schematic of feedback path DAC

Figure 4.13 is the simulation result of a feedback DAC. It can be shown that the feedback DAC will track the input signal (SR-latch output signal) and output the reference voltages what we need.

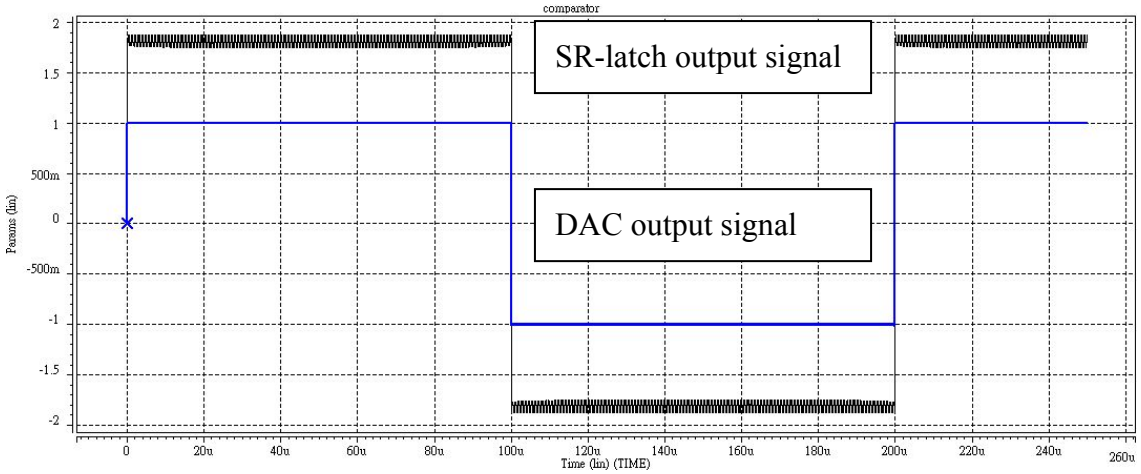


Figure 4.13 Simulation result of a feedback DAC

4.4 Simulation Result

Figure 4.14 is the plot of simulation in time-domain. And Figure 4.15 is the plot of power spectrum of the proposed continuous-time SDM. The sampling rate is 2.5 MS/s and input signal frequency is 4 kHz. The SFDR is 72 dB and SNDR is 62 dB.

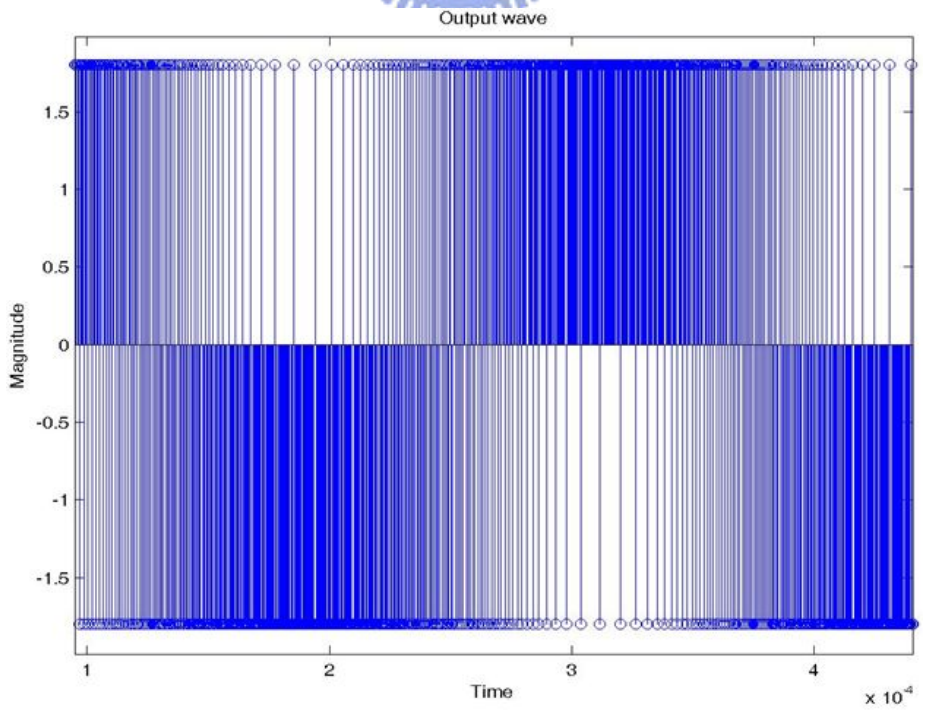


Figure 4.14 Transient analysis of SDM output

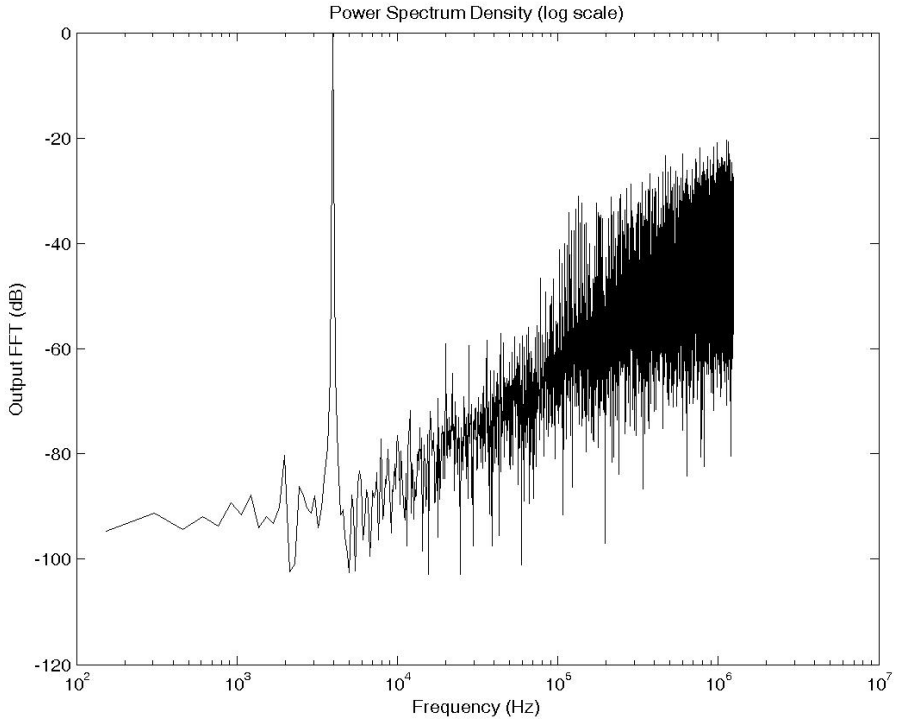


Figure 4.15 Power spectrum of SDM output

4.5 Layout level design

After the circuit level design, the real physical implementation is referred as the layout level. There are many detail problems to consider in layout level such as parasitic effect, component mismatch, noise consideration and ESD protection…etc. To avoid such problems, we use some technique for layout level design. (1) Use multi-finger transistors to avoid high gate parasitic resistance. (2) Use component symmetrization and dummy cell to improve components matching. (3) Use guard ring to prevent parasitic problems. The layout diagram is present in Figure 4.14 and the layout size is 0.56×0.56 mm^2.

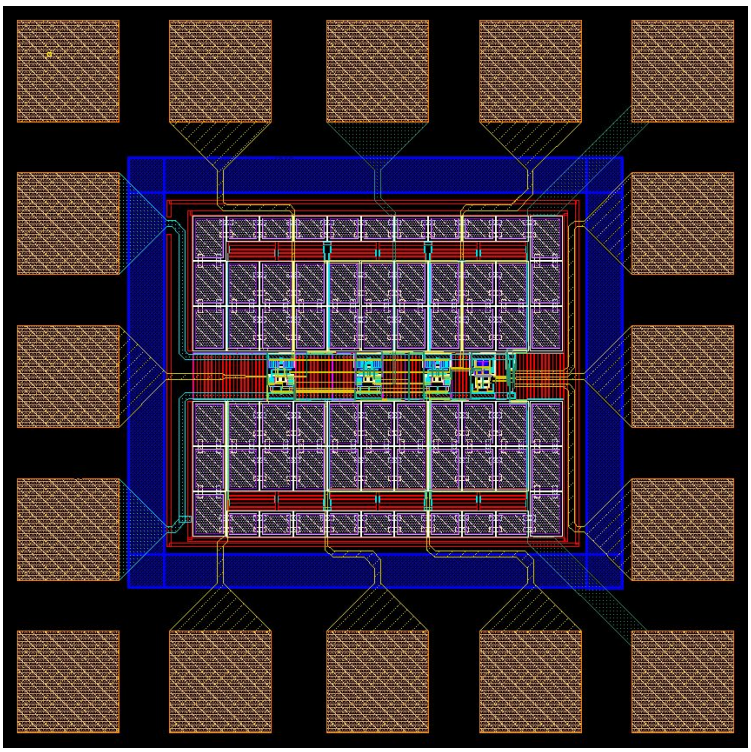


Figure 4.16 Diagram of SDM layout

Chapter 5

Test Setup and Experimental Results

5.1 Introduction

This 3-order continuous-time SDM has been fabricated by TSMC 0.18-μm CMOS Mixed-Signal process with one poly and six mental. In this chapter, we present the testing environment, including the component circuits on the DUT (device under test) board and the instruments. The measured results are presented in this chapter, too.

5.2 Measuring Environment

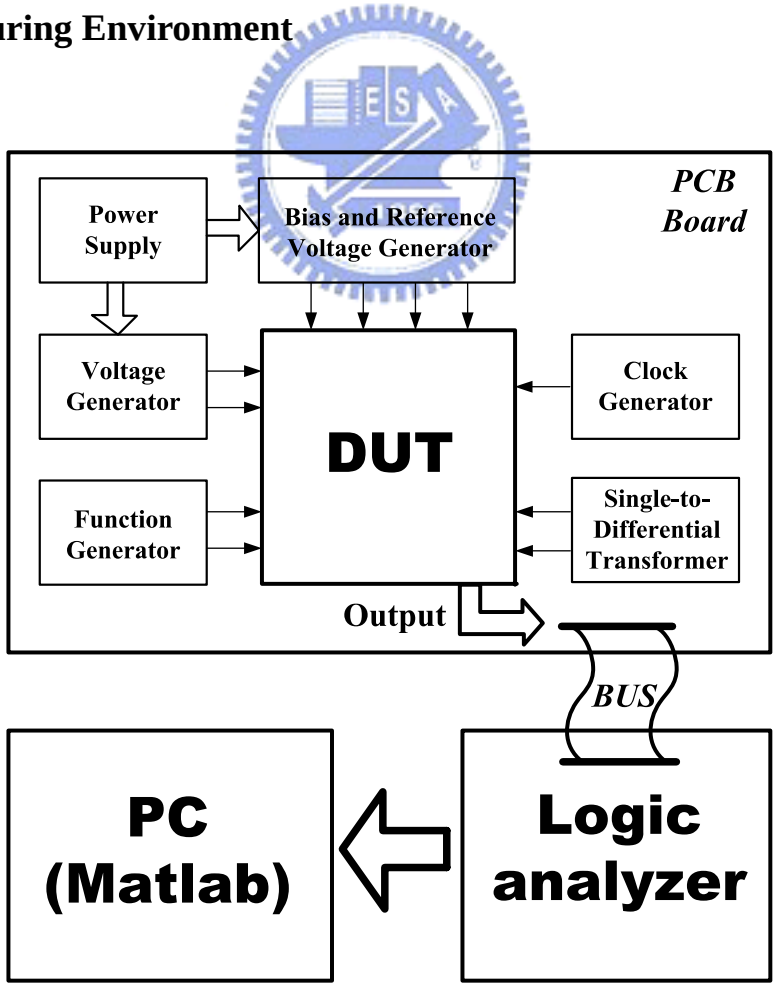


Figure 5.1 Experimental testing setup

Figure 5.2 The measurement environment

Figure 5.1 shows the whole measurement process and the testing setup used to measure the performance of the proposed SDM. Figure 5.2 show the measurement environment. We adopt a PC (for Matlab processing), an oscilloscope, two power supplies, a function generator and a pulse generator. The testing printed circuit board (PCB) contains voltage regulator, clock generator, single to differential transformer circuit, and the DUT. The supply voltages for regulators are supplied by the 9V batteries and the input signal and clock are provided by the function generators Agilent 33250A as shown in Figure 5.3. The digital output signals will be fed into the logic analyzer Agilent 16702B as shown in Figure 5.4. And we can show the output waveform by the oscilloscope Agilent S4832D as shown in Figure 5.5. Finally, the data will be loaded into the PC and be analyzed with Matlab to obtain the specification of the proposed SDM.

Figure 5.3 Function generator Agilent 33250A

Figure 5.4 Logic analyzer Agilent 16702B

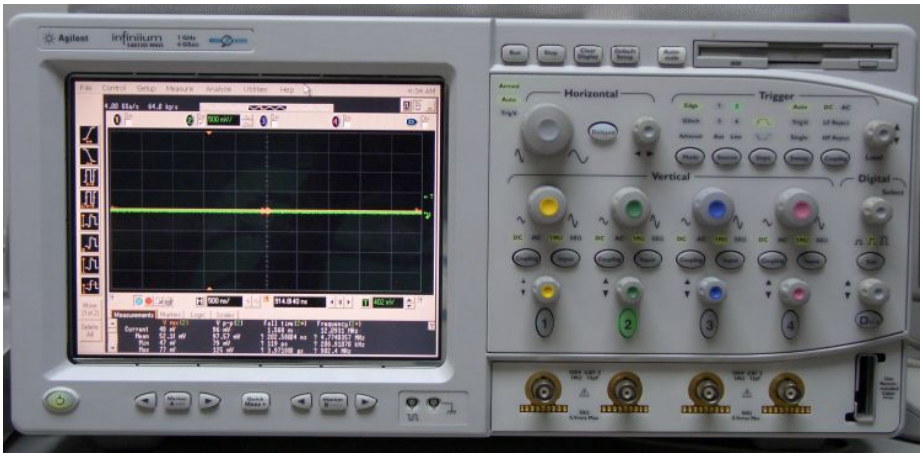


Figure 5.5 Oscilloscope Agilent S4832D

5.2.1 Power Supply Regulators

The supply voltages are generated by LM317 adjustable regulators as shown in Figure 5.6. The capacitor C1 is added to improve the transient response and capacitor C2 is the bypass capacitor. The output voltage of the Figure 5.5 can be expressed as

$$V_{out} = 1.25 \cdot \left(1 + \frac{R2}{R1}\right) \cdot I_{ADJ} \cdot R2 , \qquad (5.1)$$

where I_{ADJ} is the DC current that flows out of the adjustment terminal ADJ of the regulator [28].

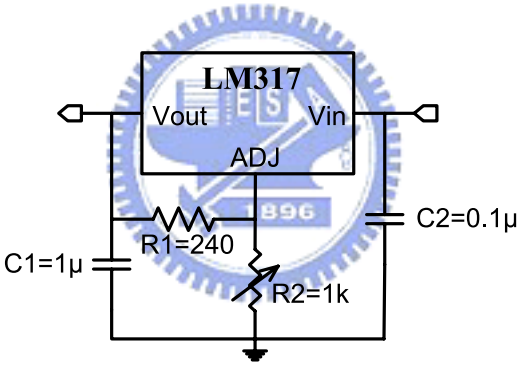


Figure 5.6 Power supply regulator

5.2.2 Input Terminal Circuit

A function generator can only provide AC component of input signal and the input signal is single-end. So we need the input terminal circuit which combined single-to-differential transformer circuit and AC couple circuit as shown in Figure 5.7. Because we can't ensure the common mode voltage is that we need, we need the adjustable resistances to tune the voltages. The operation amplifiers are OP-27 and supplied by ±9V for best operation condition [29].

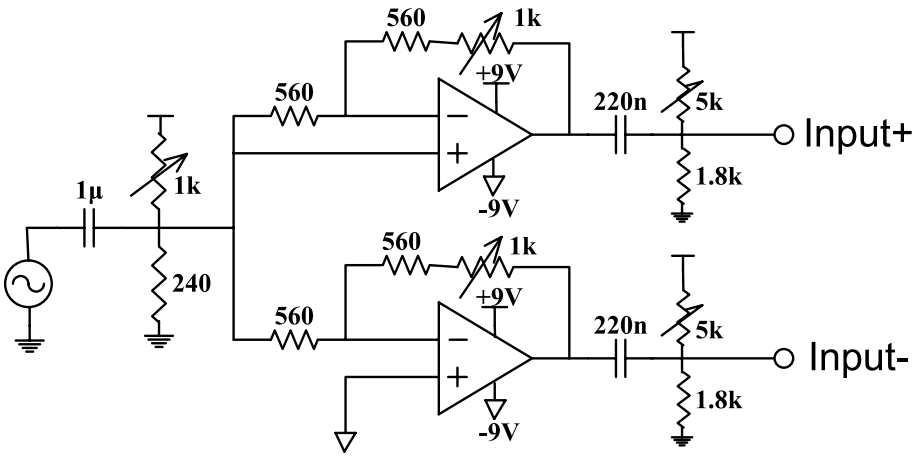


Figure 5.7 Input terminal circuit

5.3 The Die Photomicrograph, Testing Board, and Pin Configuration

Figure 5.8 shows the die photomicrograph of the experimental SDM and Figure 5.9 shows the photograph of the testing DUT board. Figure 5.10 presents the pin configuration and lists the pin assignments of the experimental SDM.

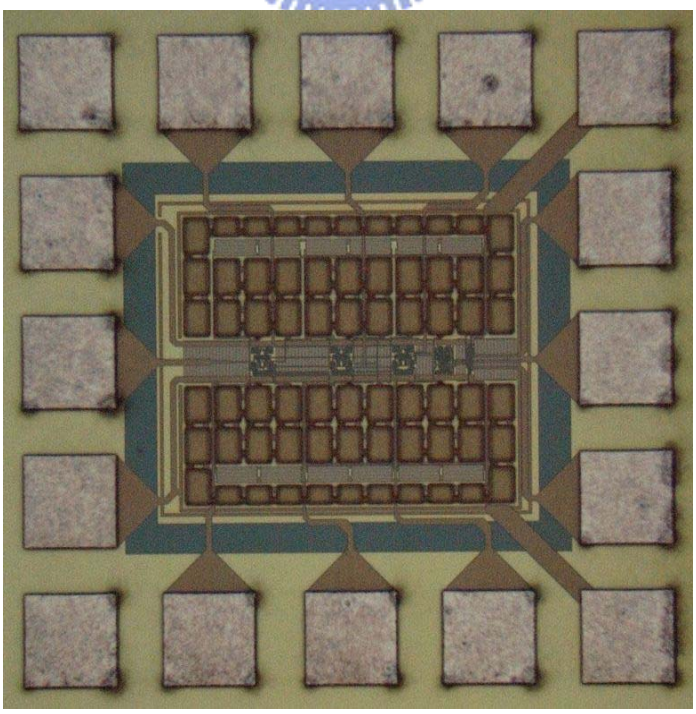


Figure 5.8 Die photomicrograph of the proposed SDM

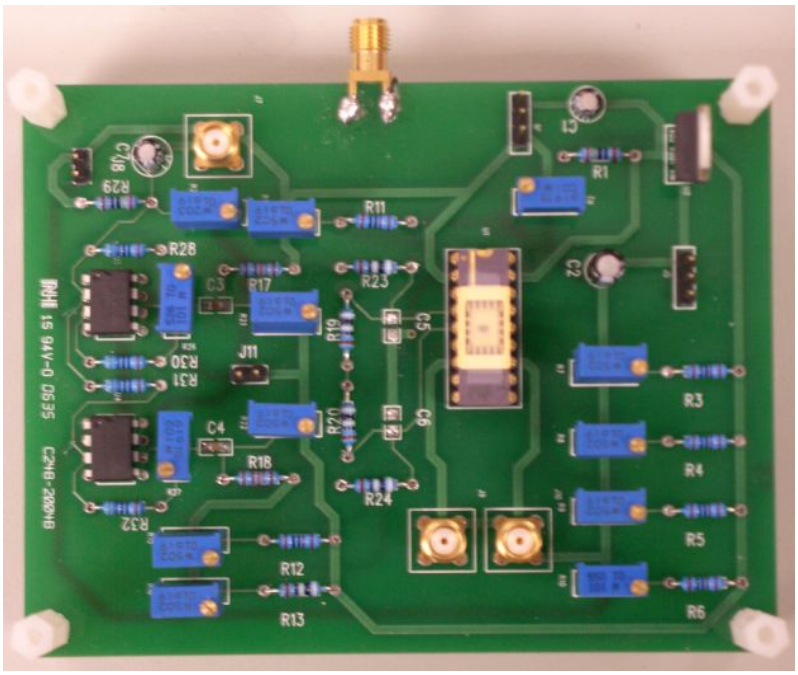
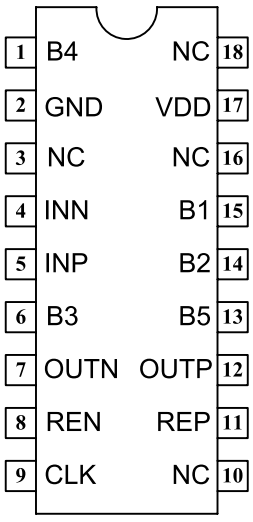


Figure 5.9 Photograph of the SDM DUT board



Pin	Name	I/O	Describe
1	NC	-	No connection
2	GND	-	DUT Ground
3	NC	-	No connection
4	INN	In	Input Signal (0°)
5	INP	In	Input Signal (180°)
6	B3	In	Bias Voltage
7	OUTN	Out	Output Signal (0°)
8	REN	In	DAC Feedback Voltage
9	CLK	In	System clock input
10	NC	-	No connection
11	REP	In	DAC Feedback Voltage
12	OUTN	Out	Output Signal (180°)
13	B5	In	Bias Voltage
14	B2	In	Bias Voltage
15	B1	In	Bias Voltage
16	NC	-	No connection
17	VDD	-	DUT Supply Voltage
18	NC	-	No connection

Figure 5.10 (a) Pin configuration diagram and (b) Pin assignment

5.4 Performance Evaluations of SDM

This proposed SDM chip has fabricated by TSMC 0.18 μm technology. It was powered by 1.8 V supply. A 4 kHz sine wave is applied and the clock rate is 2.5MHz while the corresponding bandwidth is 20 kHz. The time-domain analysis is measured by an oscilloscope (Figure 5.11).

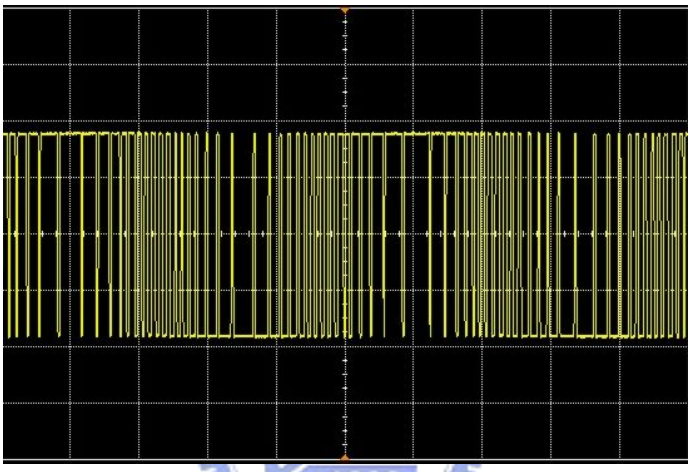


Figure 5.11 Measurement result of output waveform

Figure 5.12 shows the measured spectrum. The input signal frequency is 4kHz and the signal bandwidth is 20kHz. The output bit streams can be recorded with a logic analyzer, so that the data can be processed with MATLAB. The fast Fourier transformation with 8192 points was used and the Blackman window was applied [30]. Figure 5.13 shows the SNDR versus normalized input signal. The peak SNDR and DR are 43.2dB and 47dB of -9dB input, respectively. This corresponds to a resolution of 7 bits. The power consumption is only 0.198mW. The complete measured performance summary of the third-order SDM is given in Table 5.1.

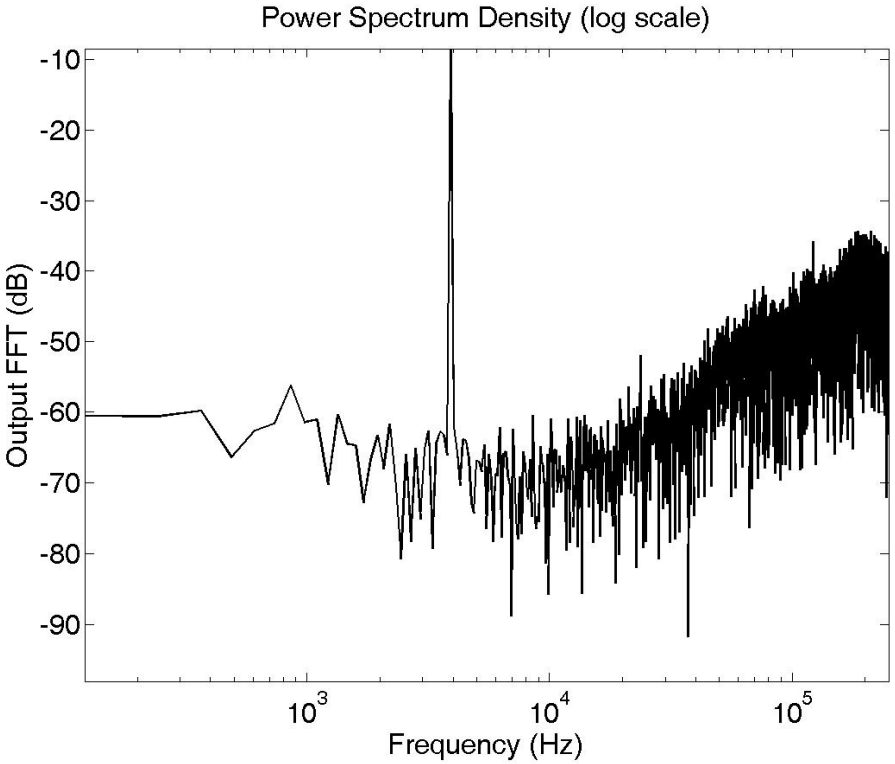


Figure 5.12 Measured output spectrum

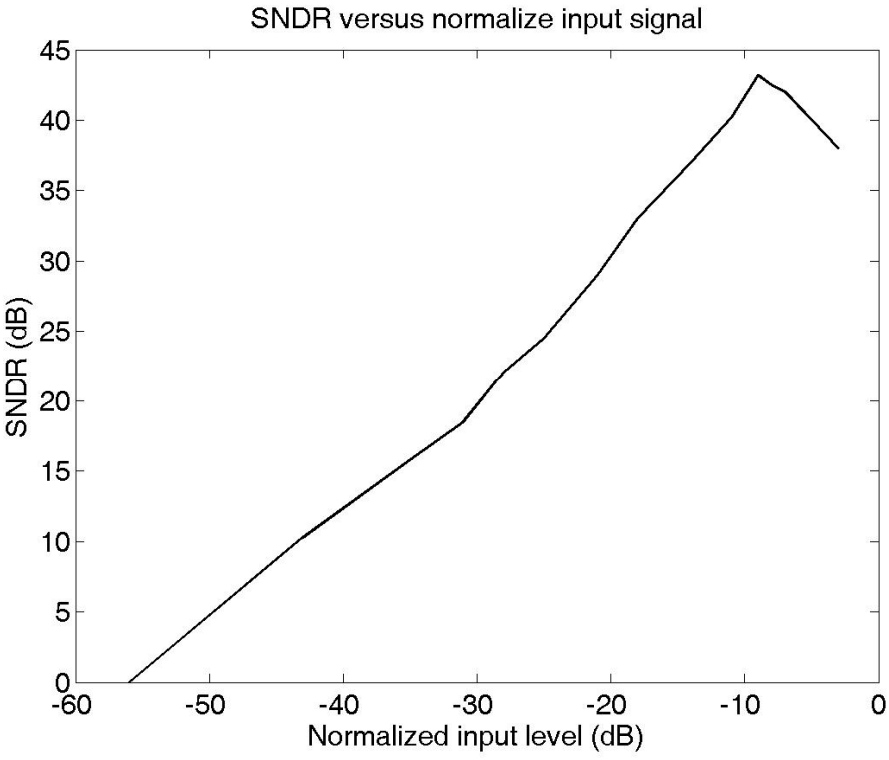


Figure 5.13 Plot of SNDR versus normalized input signal

Table 5.1 Summary of measured results of the SDM

Specification	***Measured Results***
Signal Bandwidth	**19.84 kHz**
Sampling Frequency	**2.5 MHz**
Dynamic Range	**47 dB**
Peak SNDR	**43.2 dB**
Peak SNR	**45.3 dB**
Resolution	**7 bits**
Area	**0.56×0.56=0.32 mm^2**
Power Dissipation @ 1.8V	**198 μW**
Technology	**Standard TSMC 0.18μm 1P6M**

5.5 Summary

The design of third-order continuous-time SDM was completed. It took the design considerations described in Chapter 3 and Chapter 4 into account. The original resolution was predicted to achieve 10bits. The measured result shows that the actual performance is 7bits. The possible reasons of performance decay are that the resistances variation, thermal noise, operation amplifier performance decay, and the noise of external circuits on the testing printed circuit board. The noise floor of the input signal is a little large due to the external circuits which are single-to-differential transformer circuit and AC couple circuit. And the mismatch of input differential signal is also the possible reason which causes the performance decay. If we could reduce the number of the external circuits, the performance would be much better.

Chapter 6

Conclusions

Generally, the continuous-time technique is applied in higher frequency domain. In order to achieve medium resolution and very low power in audio application domain, we use continuous-time technique to implement the SDM due to its important property of very low power consumption. This thesis presents the basic concepts for SDM including quantization noise, noise shaping strategy, and system overview of SDM are introduced. After system level simulation for building the behavior model to understand the characteristics of SDM and determine the specification, the circuit level and layout level design are presented.

In the thesis, a low power continuous-time SDM with active RC integrator is fabricated in TSMC CMOS 0.18 μm standard process. The resolution is 7 bits and the measured power consumption is only 0.198 mW for a 1.8-V supply. The influence of circuit design parameter and non-ideal effect like amplifier gain bandwidth and distortion on overall SDM has been studied. As a result, the low power consumption shows that the continuous-time technique is a good alternative to switched-capacitor realization.

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