國立交通大學

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碩士論文

使用 CMOS 0.18μm 技術設計一應用於多頻帶正交頻率多工超寬頻系統 band group 5 及一適用於 IEEE 802.11a 規格之整數型頻率合成器

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中文摘要

此篇論文主要探討了兩個電路設計，以及一個高整合性的多頻帶三角積分調變分數型頻率合成器。首先，設計一個使用 1.5V 供應電源應用於 10GHz，多頻帶正交頻率多工超寬頻系統 band group 5 處的整數型頻率合成器，提供了 9.29~10.9GHz 的頻率調變範圍及-5.9dBm 的輸出功率。壓控振盪器主要是由一組交互耦合的 NMOS 對與為了提高 Q 值而使用的中央抽頭式電感所構成。整個電路的相位雜訊為-97dBc/Hz@1MHz，頻率鎖定時間約為 25μs，功率消耗為 23.55mW。此外，電路中我們還額外設計一組暫存器，將控制訊號由七個轉換為兩個，有效地縮減電路所佔的面積。接著在第二部分我們探討 802.11a 整數型頻率合成器的設計。電路中的壓控振盪器使用堆疊的交互耦合 NMOS 與 PMOS 對，振盪頻率設計在 4.95 至 5.82GHz 之間，並藉由脈衝吞嚥技術器（pulse-swallow counter）來控制除數。只要調整外接的五個控制訊號即可有效地改變電路的總除數以達到所預定的振盪頻率。除此之外，設計一個外接的三階迴路慮波器除了考量在製程飄動的情況下尚能進行調整，低雜訊的要求也一併地考慮。鎖定時間大約是 20μs，相位雜訊為-126dBc/Hz@1MHz，總功率消耗則是 26.35mW。最後在附錄中我們介紹了一個利用 50% 除頻方法將 802.11a/b/g 無線網

路系統與 GSM/DCS1800 手機系統四個系統整合於單晶片中的頻率合成器。電路鎖定時間為 30μs，相位雜訊為-114dBc/Hz@1MHz，總功率消耗 105mW。

The Design of Integer-N Frequency Synthesizers Applied to MB-OFDM UWB 5th Band Group and IEEE 802.11a in 0.18μm CMOS

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Abstract

In this thesis, we will discuss two main circuit designs and present a highly integrated multi-band sigma-delta fractional-N frequency synthesizer. First, an integer-N frequency synthesizer operated at 10GHz around the MB-OFDM UWB system 5th band group with only 1.5V supply voltage which owns a varying frequency ranging from 9.29GHz to 10.9GHz and delivers -5.9dBm output power is shown. A single NMOS cross-coupled-pairs forms the core circuit of the voltage-controlled oscillator with a center-tapped inductor adopted to enhance the Q value at the same time, thus make the phase noise -97dBc/Hz at 1MHz. The frequency settling time is about 25μs and the whole circuit power consumption is 23.55mW. Besides, a register is designed to efficiently reduce the chip area by transferring the control signals from seven to two. In the second, we discuss about an 802.11a integer-N frequency synthesizer design. The oscillation frequency ranges between 4.95 and 5.82GHz while NMOS and PMOS cross-coupled pairs cascoded architecture is chosen in this design. The pulse-swallow counter is used to program the division number. As long as switching the five external control bits can we effectively adjust the total

division and obtain the oscillating frequency expected. Additionally, a third order loop filter is design to be implemented off the chip preparing for the adjustment against fabrication variations and low noise consideration. The settling time of the circuit is about 20μs or so and the phase noise is -126dBc/Hz at 1MHz. The total power consumption is about 26.35mW. At last in the appendix shows an 802.11a/b/g WLANs and GSM/DCS1800 mobile system frequency synthesizer integrated in a single chip by 50% frequency division techniques. The settling time is 30μs and the phase noise is -114dBc/Hz at 1MHz. Total power consumption is 105mW. The measuring preparations will also be discussed in the chapter.

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Chapter 1

Introduction

1.1 Background and motivation

With the great improvement in fabrication technology and extremely request for communication quality such as convenience and high speed transportation, wireless communication has consequently not only drawn a lot of attention among the whole world but also experienced several revolutions. From the very first 802.11a and Bluetooth systems to the recently developed ultra-wide band system, wireless communication indeed plays an important role in changing our daily life which also can be told from designers who devoted themselves to designing and planning. However, some important design goals like highly integration, smaller chip area, low cost, and less power consumption for a RF front-end circuit become more and more critical although we are about to step into the era of nano-scale. Therefore, a well planned architecture and deliberate map dominate whether the system and its application will be accepted and survive or not.

In a typical RF front-end circuit, there are many components which respond for different purposes such as low-noise amplifier (LNA) serves as the first stage in receiving signal and power amplifier which is demanded for the transmission. One of those varied circuits is so called a synthesizer, which acts as a local oscillator (LO) for up or down conversion in communication transceivers. The most important consideration while constructing a frequency synthesizer is noise restraint since ill designed circuit will make it unable to separate the desired signal from disturbance which always leads to distortion.

Besides, the design of phase-locked loops (PLLs) must generally deal with a tight tradeoff between the settling time and the amplitude of the ripple on the oscillator control line. This tradeoff limits the performance in terms of the channel switching speed and the magnitude of the reference sidebands that appear at the output. Therefore, the phase noise performance, settling time and the output power spectrum can be indexes determining whether a frequency synthesizer has well functionality or not. There are three synthesizers displayed in this thesis, two of them are 5GHz and 10GHz for different communication applications separately, and the other one makes it possible to integrate four communication systems into one single chip.

1.2 Thesis organization

We will discuss three frequency synthesizers in this thesis. The first is the one with 10GHz oscillating frequency applied to MB-OFDM UWB 5th band group while the second one is suited for 802.11a communication system and thus owns an oscillator operating at about 5GHz. The last one continues the unfinished designed work presented before which combined four systems and enabled it to receive different signals at the same time within the single chip. Down below lists details of each chapter:

Chapter 2 introduces an integer-N frequency synthesizer operates around the MB-OFDM UWB 5th band group. Occupying a 1GHz frequency tuning range and a -97dBc/Hz phase noise at 1MHz offset from the desired signal, the design verifies the possibility of a traditional architecture operates at high frequency band.

Chapter 3 is the design of an integer-N frequency synthesizer operates at 5.2GHz which suited for the application of 802.11a communication system. In this design the voltage controlled oscillator performs impressive phase noise at about -126dBc/Hz at 1MHz offset from the carrier and 20μs settling time.

Chapter 4 fulfills the unfinished design presented before. It is a quad-bands sigma-delta fractional-N frequency synthesizer that combines 802.11a/b/g and GSM/DCS1800 systems by using only a single oscillator under the fabrication of TSMC CMOS 0.18μm. The desired frequency of each application can be successfully produced through the closed loop. In the chapter we will briefly discuss the architecture of the circuit that already published before and then display the main effort of measurements and follow-up simulations in this thesis.

All these three circuits are fabricated in TSMC CMOS 0.18μm technology and have been put into practice, thus simulation results and measurement data will listed at the bottom of each chapter.

Finally in chapter 5 we will conclude the design work presented in the thesis and discuss the possible methods to improve the circuit performance and also some new ideas available for the future design.

Chapter 2

Integer-N Frequency Synthesizer Applied to MB-OFDM UWB 5th band group

Ultra wide band technology brings the convenience and mobility of wireless communications to high-speed interconnects in devices throughout the digital home and office. The Federal Communications Commission (FCC) in the US has mandated that UWB radio transmissions can legally operate in the range from 3.1GHz~10.6GHz [1], at a limit transmit power of -41dBm/MHz. Designed for short-range, wireless personal area networks (WPANs), UWB is the leading technology for freeing people from wires, enabling wireless connection of multiple devices for transmission of video, audio and other high bandwidth data. Fundamentally differs from other radio frequency communications, it is unique in that it achieves wireless communication without using a sine-wave RF carrier. Instead it uses modulated high frequency low energy pulses of less than one nanosecond in duration. Since the actual transmission is physically a wavelet, some authorities consider it to be true modulated-wavelet radio [2].

A traditional UWB transmitter as shown in Fig. 2-1 works by sending billions of pulses across a very wide spectrum of frequencies several GHz in bandwidth [3]. The pulses generated by the transmitter are completely defined by their center frequency and the bandwidth. This specific signal scheme is also defined as a “carrier-based” UWB due to the separate generation of the carrier and the envelope.

The corresponding receiver then translates the pulses into data by listening for a familiar pulse sequence sent by the transmitter. Specially, UWB is defined as any radio technology having a spectrum that occupies a bandwidth 20 percent greater than the central frequency, or a bandwidth of at least 500MHz.

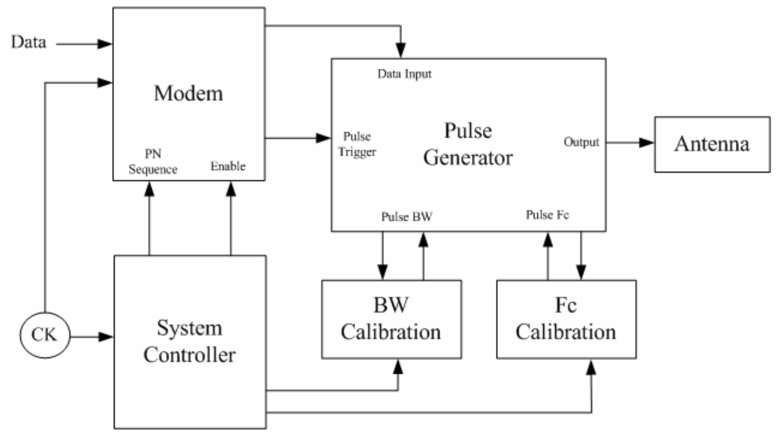


Fig. 2-1 Impulse-based ultra wideband transmitter architecture

However the modern UWB systems as shown in Fig. 2-2 use other modulation techniques, such as Orthogonal Frequency Division Multiplexing (OFDM), to occupy these extremely wide bandwidths [4]. In addition, the use of multiple bands in combination with OFDM modulation can provide significant advantages to traditional UWB systems, including high spectral efficiency, inherent resilience to RF interference, robustness to multi-path, and the ability to efficiently capture multi-path energy. The multi-band OFDM approach also allows for good coexistence with narrow band systems such as 802.11a, who owns a frequency band less than 500MHz, adaptation to different regulatory environments, future scalability and backward compatibility [5].

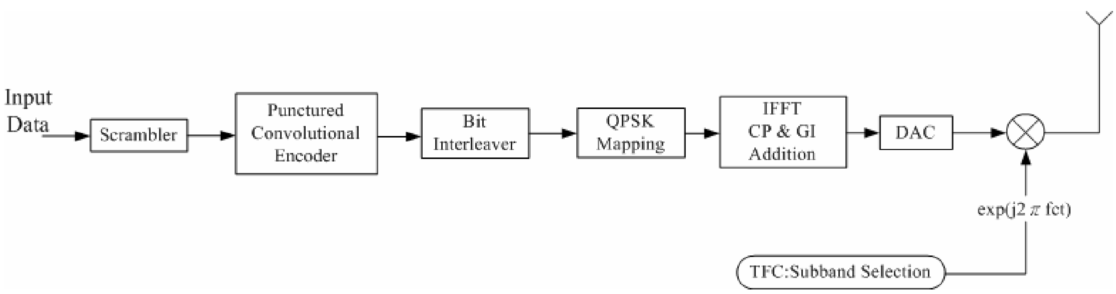


Fig. 2-2 Transmitter Architecture of the multi-band OFDM system

The transmitter of the OFDM-UWB system architecture that operates in 3.1 to 4.6 GHz section since the other bands are preserved for later use is shown in Fig. 2-3 while the band scheme for the MB-OFDM in Fig. 2-4 shows that five logic channels are mapped out while multiple groups of bands enable multiple modes of operation for MB-OFDM devices. Channel 1, which contains the very first three bands, is mandatory for all UWB devices and radios, used in longer range applications while channel 3 and 4 are for shorter range applications [6].

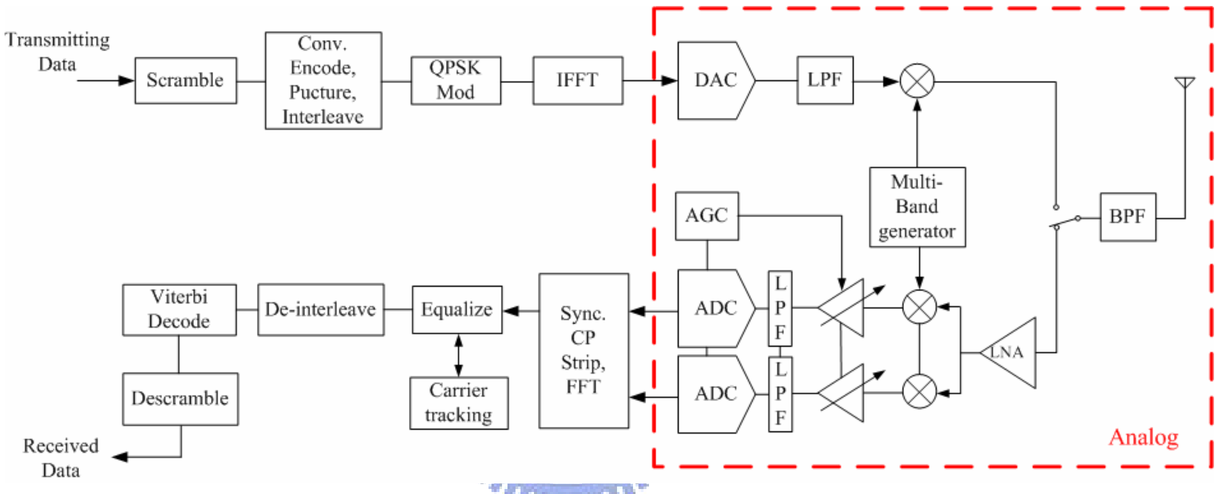


Fig. 2-3 A basic OFDM UWB System Architecture

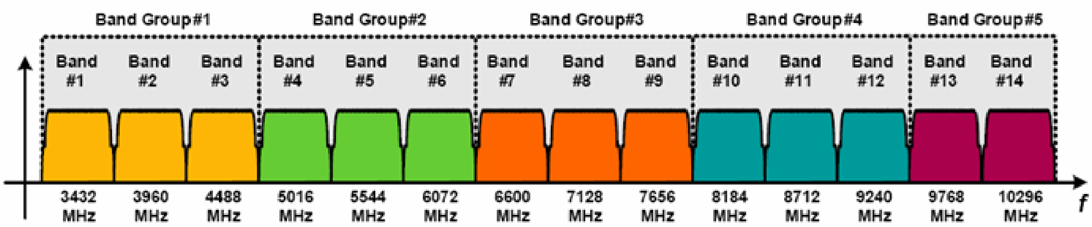


Fig. 2-4 A multi-band OFDM band plan

2.1 Architecture [7]

In a MB-OFDM UWB system, the very wide frequency band is divided into five band groups while the 5th group divided into two frequency bands. Since frequency synthesizers designed at 10GHz such a high frequency are not popular yet, and a synthesizer that can operates from 3.1GHz~10.6GHz needs not only more control signals than usual but also raising the circuit implementation complexity. Besides, a designing work of a frequency synthesizer that covers the first four band groups is undergoing, we will try to prove that the highest band is possibly realizable by using the conventional PLL architecture.

In this chapter, a synthesizer shown in Fig. 2-5 with a varying frequency ranging from 9.5GHz~10.6GHz is designed, and a fully programmable multi-modulus frequency divider (FPMMFD) [8] scales down the oscillating frequency to meet the target we set.

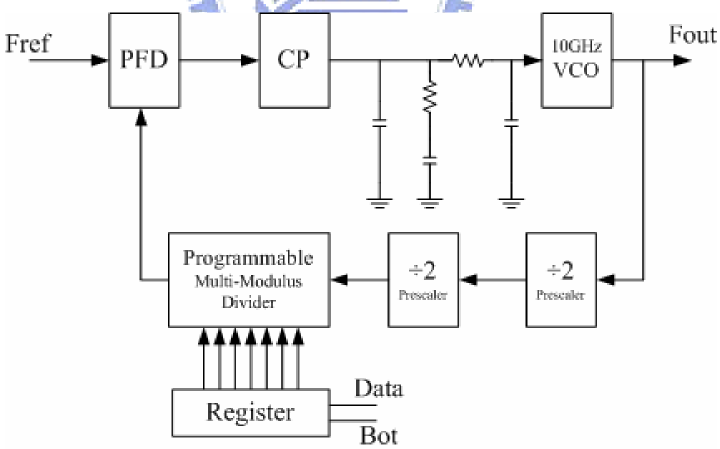


Fig. 2-5 10 GHz frequency synthesizer with multi-modulus divider

2.2 10GHz VCO

Instead of using complementary cross-coupled pairs as usual, we adopt a single NMOS couple pair fort the voltage controlled oscillator in this work and outputs two differential signals. As shown in Fig. 2-6, differential outputs can effectively alleviate the common-mode noise coupled from the substrate.

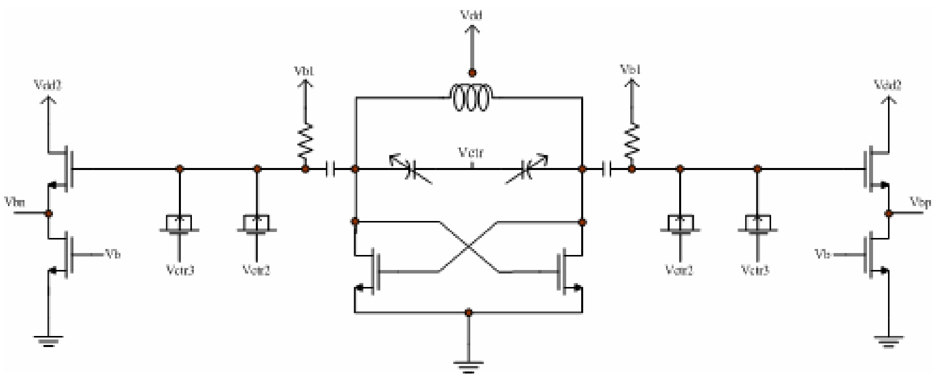
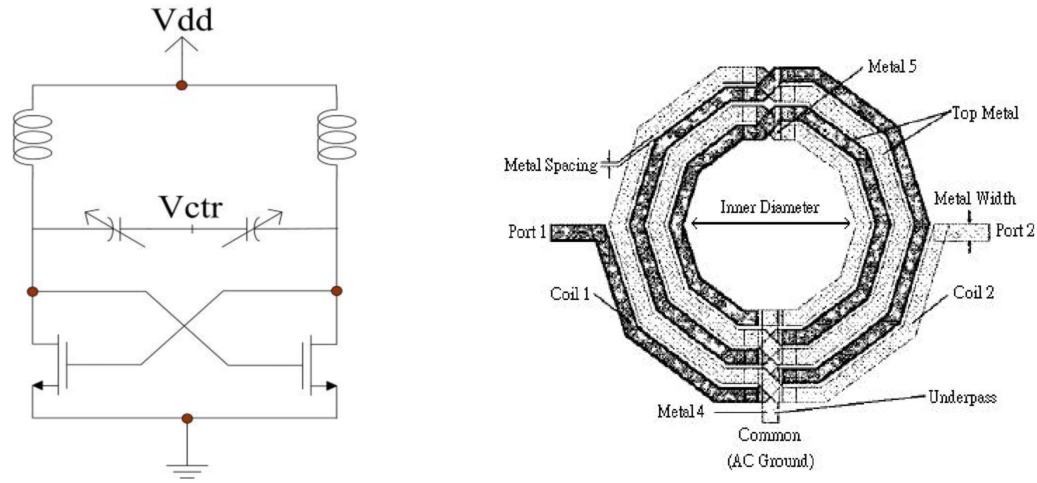


Fig. 2-6 NMOS cross-coupled VCO

Although we used to widen the output power by increasing conductance through the complementary PMOS coupled pairs, it can still be replaced by a simple architecture at high frequency, a NMOS coupled circuit, which is free from the upper operating region limits that bothers a lot under the cascoding condition. As long as well adjusting the size of NMOS can we obtain a greater output waveform.

In this design, we get rid of the traditional single-in single-out inductor often used in NMOS-only voltage controlled oscillator, and choose a center-tapped structure as shown separately in Fig. 2-7(a) [9] and Fig. 2-7(b) [10] in behalf of high Q value and improvement in economizing the circuit area. Fig. 2-8 also shows the equivalent circuit model of a traditional spiral inductor.



(a) (b)

Fig. 2-7 (a) A Traditional NMOS-only VCO

(b) A differential-in center-tapped inductor

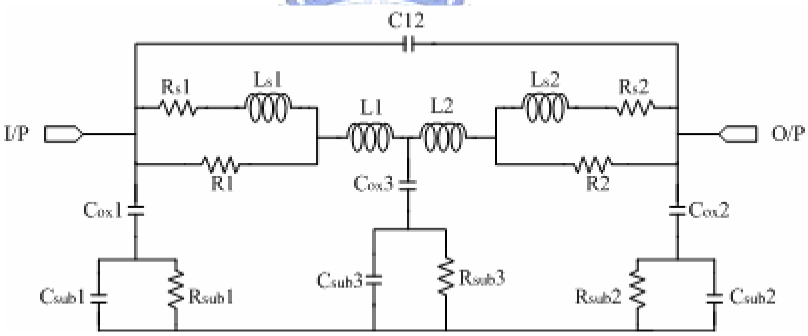
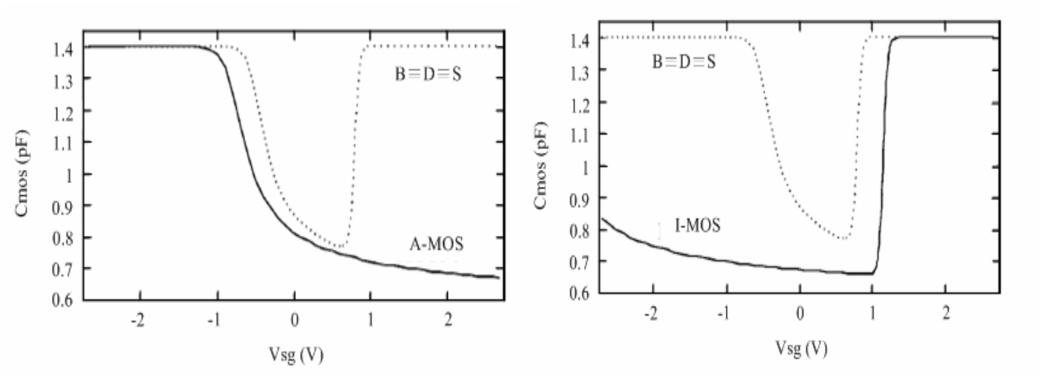


Fig. 2-8 Equivalent circuit model of a spiral inductor

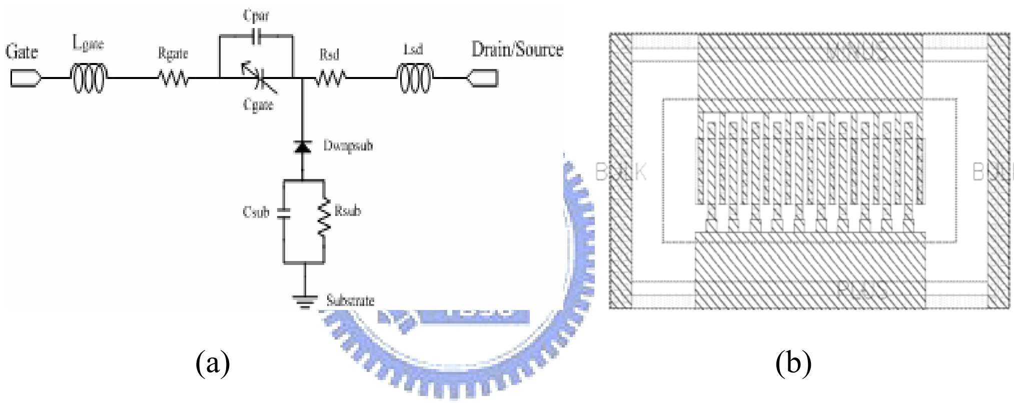
Some additional elements, varactors, are added to the circuit to modulate the oscillating frequency by their identity of voltage-controllable capacitance. There are two kinds of varactors, accumulation-mode and inversion-mode. For the latter one, when a control bit of capacitor bank is at low level, the MOS varactor has small capacitance. Otherwise, if a control bit is set at high level, the MOS varactor will turn into large capacitance. The relationship between control voltage and capacitance is shown in Fig. 2-9(a), (b), and Fig. 2-10 is an equivalent circuit model and a practical layout of MOS varactor [11].



(a) (b)

Fig. 2-9 (a) Tuning characteristics for the accumulation-mode MOS capacitor

(b) Tuning characteristics for the inversion-mode MOS capacitor



(a) (b)

Fig. 2-10 (a) Equivalent circuit model of a varactor

(b) Practical layout of a varactor

Because a frequency synthesizer needs many control signals, it can not be measured on wafer. Consequently considering the load effect and parasitic effect while designing is very important. As shown in Fig. 2-11, since the output signals from the core circuit of VCO are connected to pads through the buffer first and then measured by a spectrum analyzer, the pad parasitic capacitance, bond-wire induced inductance, blocking capacitance and input resistance of the instrument are considered while simulating.

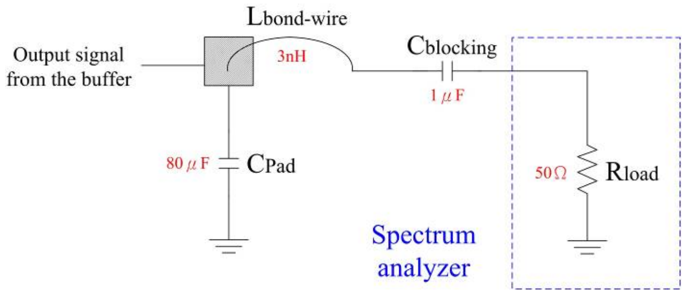


Fig. 2-11 Output stage simulation consideration of a VCO

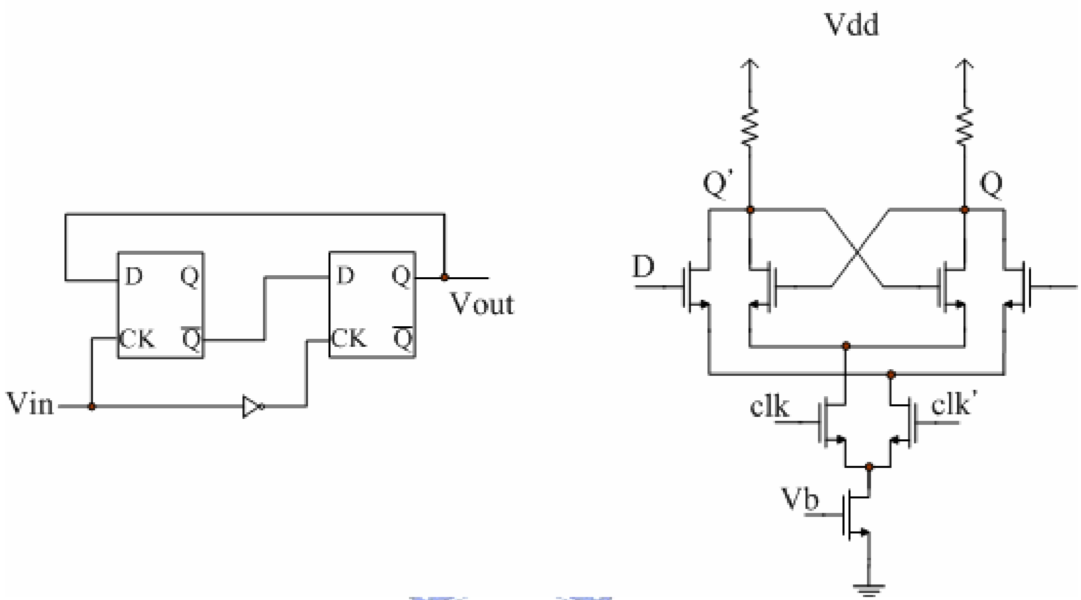
2.3 High Speed Frequency Divider

A digital frequency divider [12] is in principle a counter. The main advantage of digital dividers over their analog counterparts is that they can be readily designed for variable division ratios and are easily cascaded to generate very large division ratios. The general characteristics of these dividers are that they are wideband and the power consumption increases with the operating frequency. However digital logic DFF (shown in Fig. 2-12(a)) will not work accurately at high frequency. We will sketch an analog-based divider in this project [13].

Dividers which fit for high frequency application are generally injection-lock frequency divider (ILFD) and current-mode logic (CML) these two types. Since that the voltage-controlled oscillator has wide frequency tuning range and ILFD not only locked within a narrow ambit but also occupies considerable area due to usage of inductors, the CML architecture will be our first priority while meditating.

So in this design, an analog DFF frequency divider based on the topology of source coupled logic (SCL) rather than injection lock is adopted owing to the circuit size consideration as shown in Fig. 2-12(b), besides, remove the tail current source can effectively improve the input frequency range about 10% and reduce the layout complexity.

Fig. 2-13 is the simulation result of a 10GHz signal pass through two cascaded dividers, as it can tell from the graph, the minimum acceptable input signal is about 500mV peak to peak.



(a) (b)

Fig. 2-12 (a) Block diagram of a divider-by-2 circuit

(b) Structure of an analog DFF

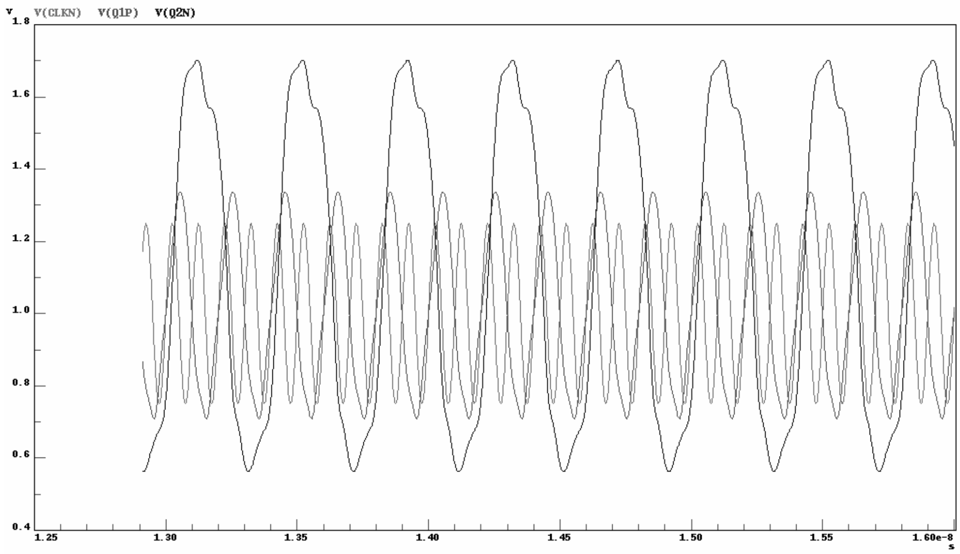


Fig. 2-13 A 10GHz signal downscaled by two cascaded divide by 2 circuit

2.4 Fully programmable multi-modulus frequency divider

The most common choice of frequency dividers in frequency synthesizer are phase-switching circuit and programmable pulse-swallow counter, however these two architectures have lower flexibility. So in this design we adopt the fully programmable multi-modulus frequency divider (FPMMFD) [8] which is not only easy to be implemented, but can also effectively reduces the possibility of dividing error since that the delay time of every stage only related to next stage compared with other divider architecture.

Fully programmable multi-modulus divider is put to use in order to achieve both high-speed frequency division and moderate power consumption. It consists of 7 asynchronously cascaded dual modulus divide-by-2/3 dividers as shown in Fig. 2-14, with the first two stages assumed to operate at high frequency. Therefore, both two circuits are realized in a differential source coupled logic (SCL) and the others are accomplished as digital devices.

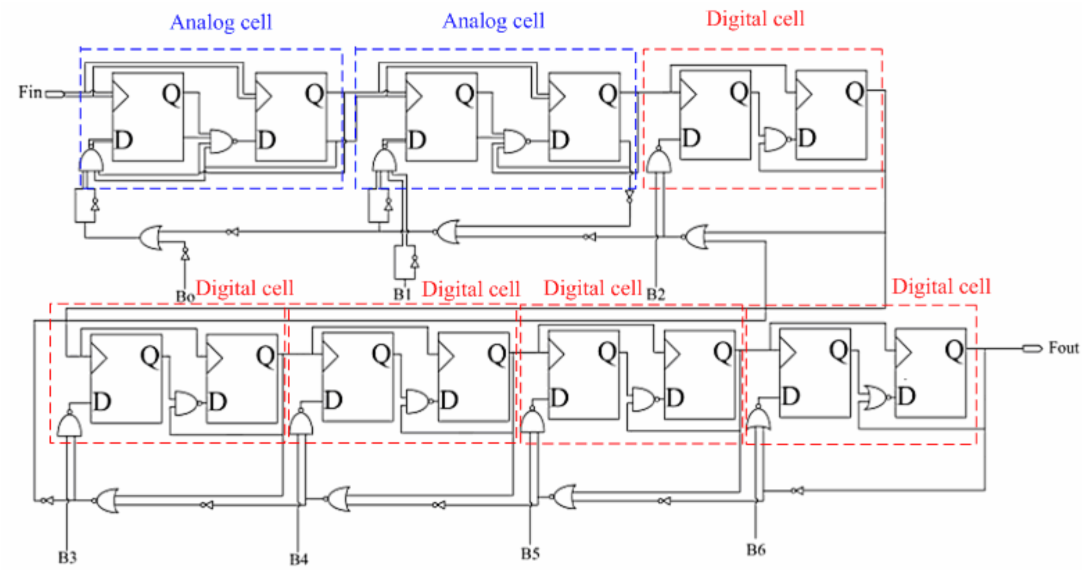


Fig. 2-14 Fully programmable multi-modulus frequency divider

We can vary the total division N by changing the input level of each block's control bit (B_0, B_1, B_2…). In this work, the VCO is designed to oscillate at 10GHz and the output signals are downscaled by two cascaded dividers, that is to say, the signal sent into the multi-modulus divider is at about 2.5GHz. Under this frequency order, the divider can be programmed to all integer values in between 128 and 255, depending on the input control bits $B_{0…6}$, which are brought out from the register which will be introduced in next section, and the programmable dividing ratio is:

$$N = 2^7 + \sum_{n=0}^{6} b_n \cdot 2^n = 128 + \sum_{n=0}^{6} b_n \cdot 2^n$$

This divider structure provides high flexibility and the simple logic of the AND/OR gates assures that the modulus signals of the last stages are produced first and given to the next stage. Thus the delay time in the critical path, the feedback of the first stage, is minimized.

As it shows in the figure above, the 2^{nd} 2/3-divider outputs a pair of differential signals but only the positive edge is connected to the next stage. So we insert an additional differential amplifier with single output (Fig. 2-15) to connect these two stages and enlarge the signal at the same time in case of unexpected weak waveform lacks the ability to drive the following dividers.

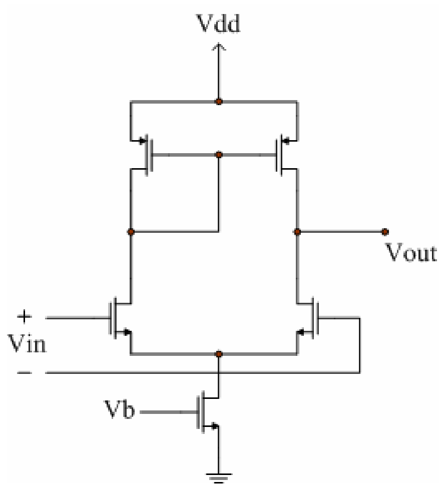


Fig. 2-15 Differential amplifier with single ended output

As we mentioned before, in order to perform the high frequency operating at the first two dividing stages, the architecture of differential source coupled logic must be used and logic gates will embedded in it. A simple structure of a two-modulus divider is shown in Fig. 2-16 [14], and since that the parasitic capacitance has great influence upon maximum operating speed, the first stage requests for a symmetrical and accurate layout.

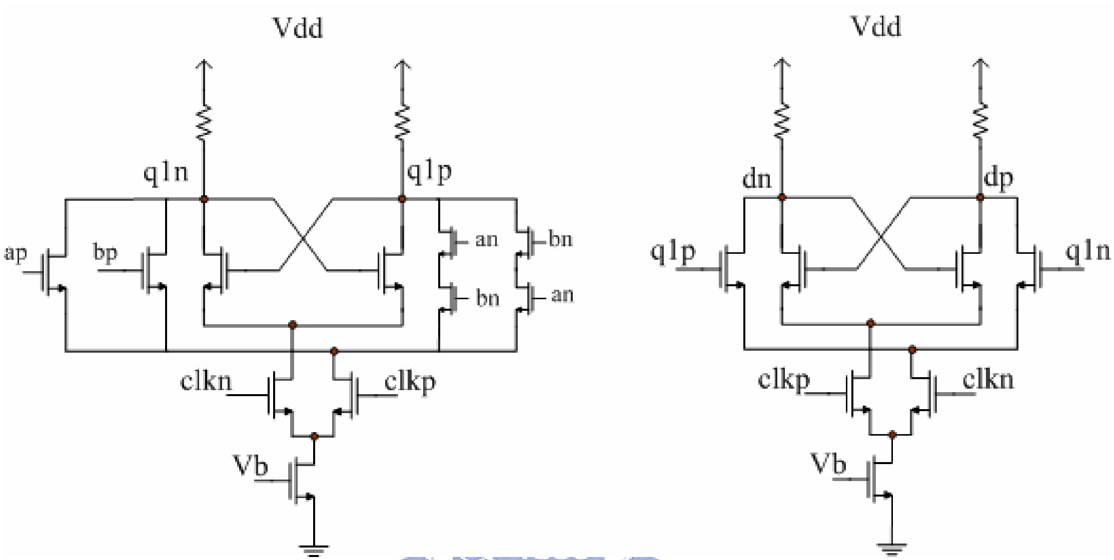


Fig. 2-16 Basic two-modulus divider in differential source-coupled form

2.5 Register

Owing to the great number of input signals a frequency synthesizer has, if we design a pad for every single input control signal and output signal, the chip size will be enlarged. Furthermore, we implement a fully programmable multi-modulus frequency divider in the circuit, which needs seven control bits to adjust the division, and will again make the chip even bigger. In order to improve the drawback, a register is designed to fix the problem.

As shown in Fig. 2-17, a register is composed of seven cascaded D–type flip flops due to seven control signals a single FPMMFD needs. The control signals are input from the node named Data, and by the clock ticking, the frequency divider can be accurately loaded. The register not only prevents long metal lines in layout which will lead to serious parasitic effects, it also scales the chip size down by reducing the pad numbers from seven to two.

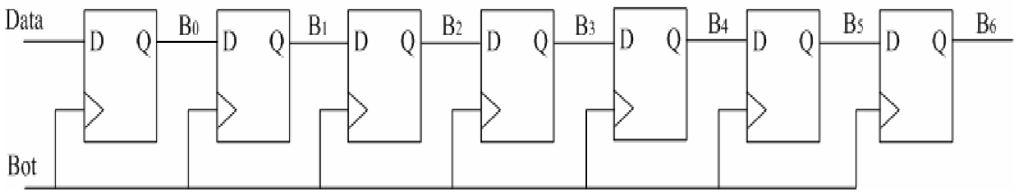
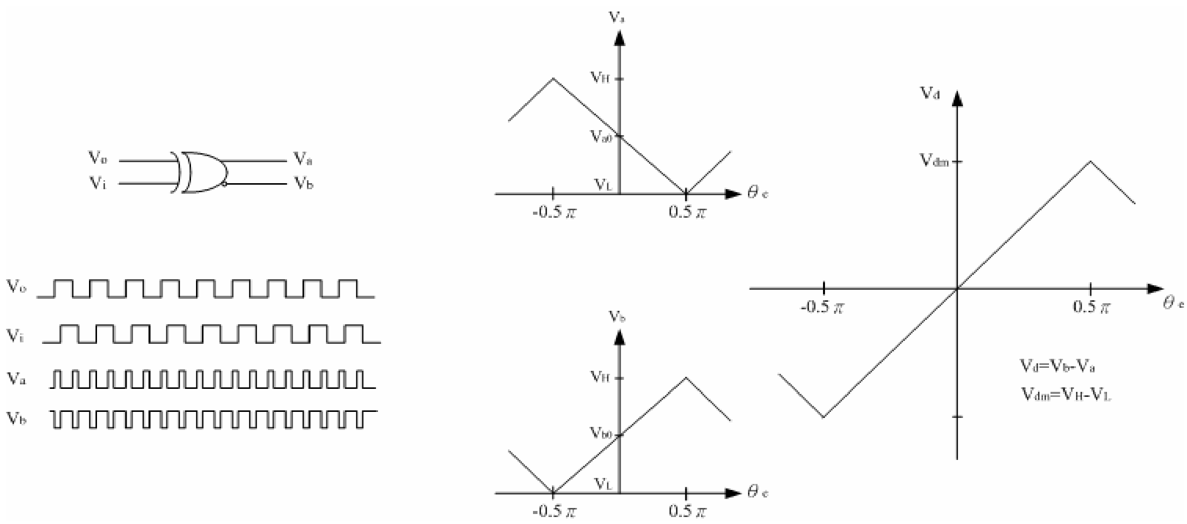


Fig. 2-17 A seven stages cascaded register

2.6 Phase/Frequency Detector

The phase detector is an architecture that generates the error signal required in the feedback loop of the synthesizer. The PFD compares the reference frequency F_{ref} with that of the divided down VCO signals (F_{vco}/N) and activates the charge pumps based on the difference in phase between these two signals. It can be classified into two types: analog and digital structures, the former one includes double balanced multiplier and Gilbert cell while the latter one can be realized in exclusive-OR logic gates, two-state detector and three-state detector these three kinds. The analog type PFD is widely adopted at about hundreds MHz order, however the signal inputs to the PFD in this frequency synthesizer is down scaled by a sequence of dividers to tens MHz, for this reason, we will put digital architectures to use.

Exclusive-OR gate is the simplest circuit to realize a phase/frequency detector as shown in Fig. 2-18(a), but it has a serious drawback that can only resolve phase differences between $\pm \pi/2$. Fig. 2-18(b) shows the tendency of V_d while phase error varies.

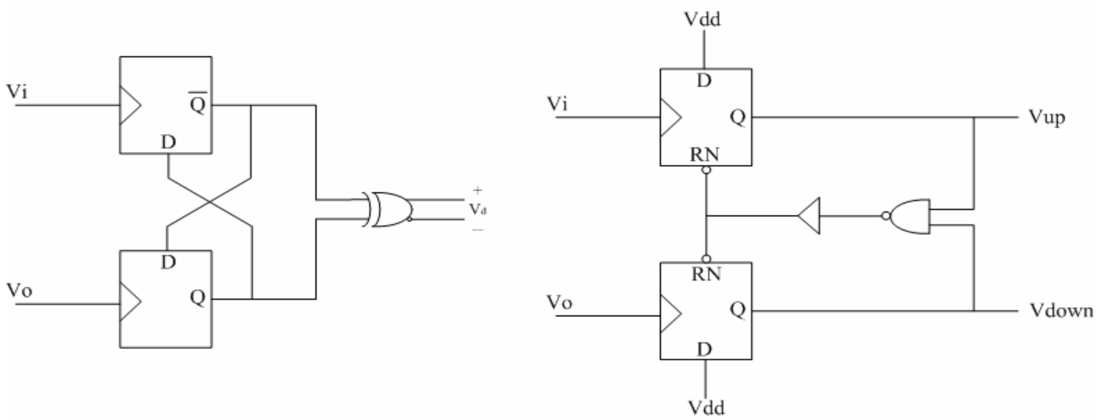


(a) (b)

Fig. 2-18 (a) XOR PFD and the timing diagram

(b) Output voltage vs. phase difference

Therefore, another two different types of PFD are developed to fix the problems. As shown in Fig. 2-19(a) and Fig. 2-19(b), a two-state PFD is composed of two D-type flip flops and a single exclusive-OR, while a three-state PFD involves two D-type flip flops with asynchronous active–low reset, RN. But still, the former one only can resolve phase differences in the $\pm\pi$ range which can not satisfy our basic requirement, and thus make three-state PFD that has a $\pm 2\pi$ range the first priority in this project.



(a) (b)

Fig. 2-19 (a) Two-state PFD (b) Three-state PFD

Why we are so eagerly demanding for a PFD to have a $\pm 2\pi$ resolution range? The operational characteristics of a phase/frequency detector can be separated particularly into three segments: frequency detection, phase detection, and locking mode. When two signals sent in, as long as the phase difference is greater than $\pm 2\pi$, the charge pump connected afterwards will output a constant current and thus make the loop filter integrate a continuously changing control voltage applied to VCO. This is so called the frequency detection and the PFD will keep on recurring until the phase difference is less than 2π.

Once the condition discussed above happened, the PFD will then turn to the mode of phase detection. In this mode, the charge pump switches between up and down depends on the two input frequencies. If the reference signal is faster than the divided one, the PFD will generates high and low level signals and force the charge pump generate a charge current to the loop filter so as to raise the oscillating frequency to catch up with the reference source, vice versa. As long as the phase difference reaches zero, the whole circuit is in the state called phase and frequency locked.

Dead zone consideration is also a significant topic when designing a PFD. The dead zone takes place while the two compared signals have only slight difference in phase, and such tiny discrepancy make the charge pump connected afterwards fail to catch up with the variation and correctly react before the D-type flip flops being reset. So a buffer stage is added between the NAND gate and the reset end as realized in Fig. 2-19(b) to hold off the reset signal until the charge pump is properly functioned. The dead zone improvement result of this circuit is shown in Fig.2-20. Besides, while operating in the phase lock state, the PFD will still output narrow spikes, occur at the frequency equal to the reference signal, due to the finite logic responding speed and will be filtered out for fear of moderating the VCO and lead to unwanted spurious noise.

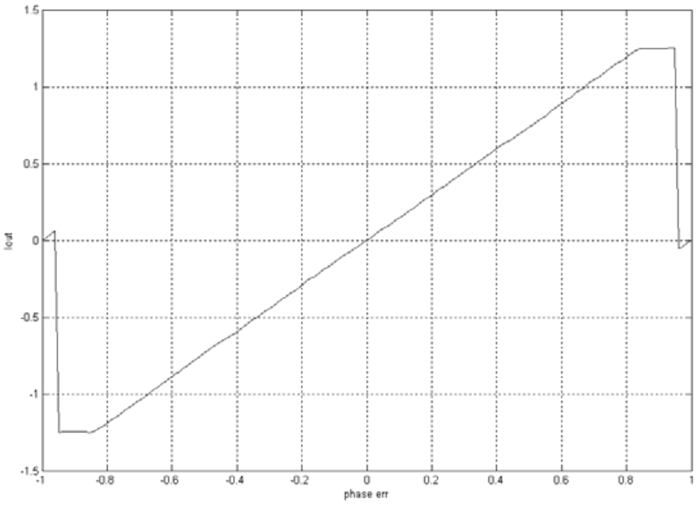


Fig. 2-20 dead zone elimination simulated by MATLAB

2.7 Loop filter design

There are two types of loop filters, active and passive. Active loop filters include OP-amplifiers and are usually differential, allowing the frequency synthesizer to generate tuning voltage levels higher than the PLL IC can generate on chip. Passive loop filters are mainly R, C those passive components and often connected directly between the charge pump and the VCO to generate a control voltage that can adjust the oscillating frequency.

Loop bandwidth plays an important role in designing, not only because a high loop bandwidth will lead to the circuit fast locked, a lower one enables it to suppress spurious noise leaked from PFD and charge pump efficiently. We adopt a 3rd order loop filter as shown in Fig. 2-21 in this design, and set the phase margin to about 60 degrees for the stable consideration.

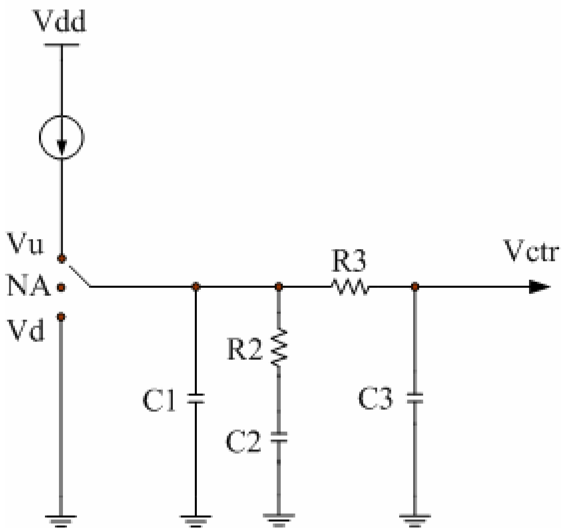


Fig. 2-21 A 3^{rd} order loop filter

The loop filter transfer function is:

$$H(s) = K_h \cdot \frac{(s+\omega_z)}{s \cdot (s+\omega_{p1})(s+\omega_{p2})}$$

where $K_h = \frac{1}{R_3 C_1 C_3}$, $\omega_{p1} = \frac{C_1 + C_2}{R_2 C_1 C_2}$, $\omega_{p2} = \frac{1}{R_3 C_3}$, $\omega_z = \frac{1}{R_2 C_2}$

Locations of poles, zeros, and loop bandwidth determine the synthesizer settling time, spurious noise, and phase margin. Generally we will make the frequency difference between ω_{p1} and K_h equals to the difference between ω_z and K_h for the consideration of maximum phase margin. There is a useful criterion shown in Fig. 2-22 to determine the value of K_h, ω_{p1}, ω_{p2}, and ω_z, so as to derive the preliminary value of the passive component use in the loop filter. The formulas are described in detail and down below shows a simple example.

$$R_2 = K_h \cdot (1+\frac{1}{\chi}) = \frac{K \cdot N}{K_0 \cdot K_d} \cdot (1+\frac{1}{\chi}) \quad \text{where} \quad \chi = \frac{C_2}{C_1} = \frac{\omega_{p1}}{\omega_z} - 1$$

$$C_2 = \frac{1}{\omega_2 R_2}, \quad C_1 = \frac{C_2}{\chi},$$

$$C_3 = \frac{1}{\omega_{p2} R_3} \quad \text{and needs to be enlarge to bypass spurious noise}$$

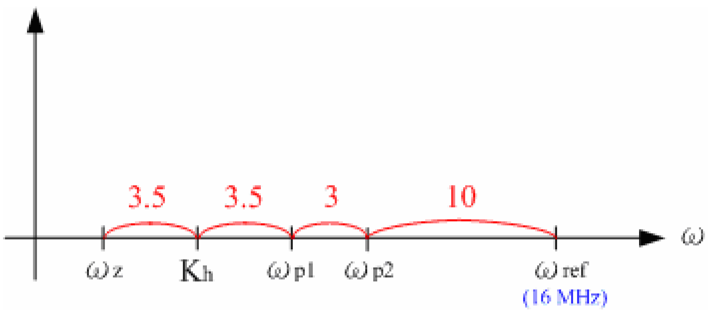


Fig. 2-22 Allocation diagram of poles, zero, reference frequency and loop bandwidth

Here we assume the current outputted from the charge pump is 50μA, and K_{vco} is 200 MHz/V, that is to say the value of R_2 is:

$$R_2 = K_h \cdot (1+\frac{1}{\chi}) = \frac{K \cdot N}{K_0 \cdot K_d} \cdot (1+\frac{1}{\chi}) = \frac{\frac{2\pi \cdot 16 \cdot 10^6}{105} \cdot 625}{2\pi \cdot 200 \cdot 10^6 \cdot \frac{50 \cdot 10^{-6}}{2\pi}} \cdot (1+\frac{1}{13}) = 64.44(K\Omega)$$

$$C_2 = \frac{1}{\omega_2 R_2} = \frac{367.5}{2\pi \cdot 16 \cdot 64.44} = 56.73(pF)$$

$$C_1 = \frac{C_2}{\chi} = \frac{56.73}{13} = 4.36(pF) \qquad C_3 = 39(pF)$$

$$R_3 = \frac{1}{\omega_{p2} C_3} = \frac{10}{2\pi \cdot 16 \cdot 39} = 2.55(K\Omega)$$

We use MATLAB to simulate whether those calculated values make the closed loop frequency synthesizer stable or not. However it shows that the filter designed provides low damping factor and will easily make the loop unstable, for this reason, we will change the multiple betweenω_{p1}, ω_z, and K_h to four, that is to say, the value of χ will be 15. The modified settling voltage and time simulation results are shown in Fig. 2-23 and Fig. 2-24 separately telling that with greater damping factor comes more stability of the closed loop. In the figures we find out that the settling falls at 1V at about 25us and the oscillating frequency will maintain at 10GHz.

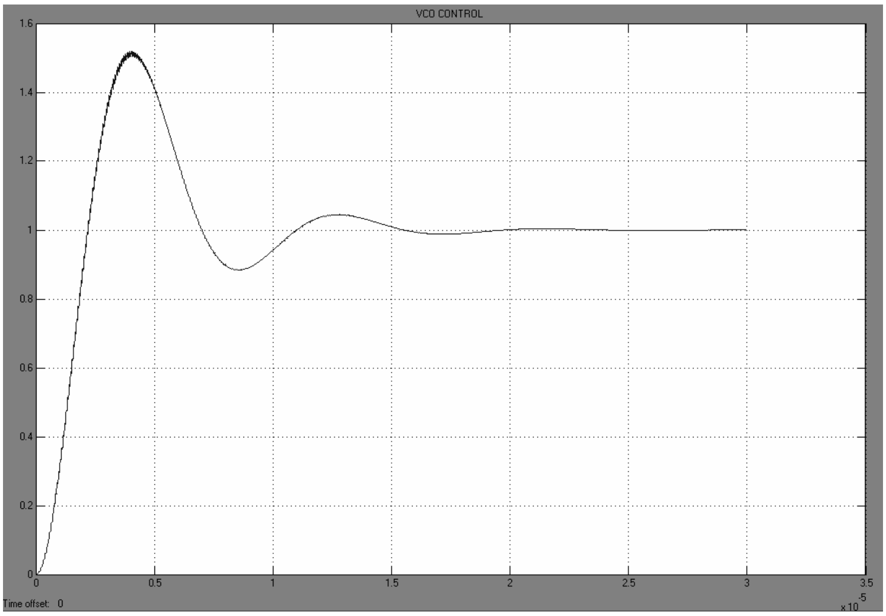


Fig. 2-23 Settling voltage at about 1V

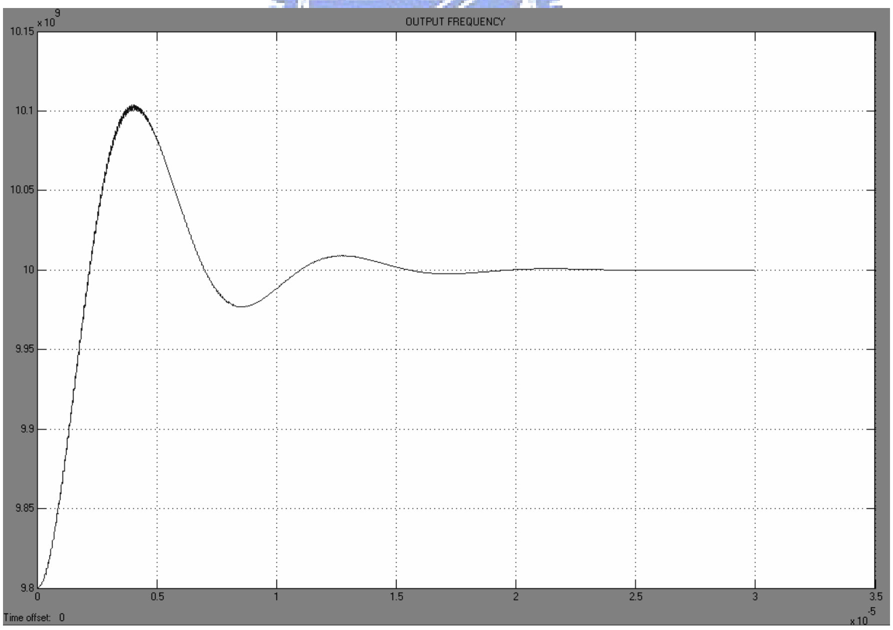


Fig. 2-24 Locking frequency vs. settling time

2.8 Simulation results

In order to make sure the frequency synthesizer with a VCO that operates at 10GHz can accurately lock, we adopted the traditional architecture to accomplish the whole circuit and realize the circuit blocks from VCO to the register at first to testify whether the practical measurements will meet what we expected and predicted or not. Fig. 2-25 is the tuning range of the VCO which owns the varying range between 9.29GHz and 10.9GHz.

Down below in Fig. 2-26 is the output signal through the buffer of a 10GHz VCO and can be clearly distinguished that the output peak-to-peak voltage is about 1000mV, Fig. 2-27 also shows the output power spectrum, and the simulated result is -5.79dBm at 10GHz, and Fig. 2-28 is the phase noise performance which is -97dBc/Hz at 1MHz.

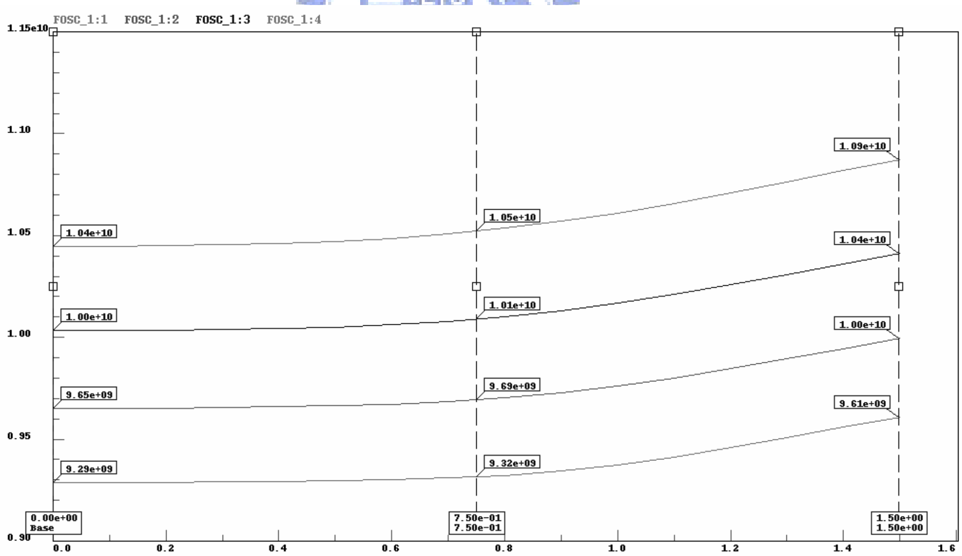


Fig. 2-25 VCO tuning range varies from 9.29GHz to 10.9GHz

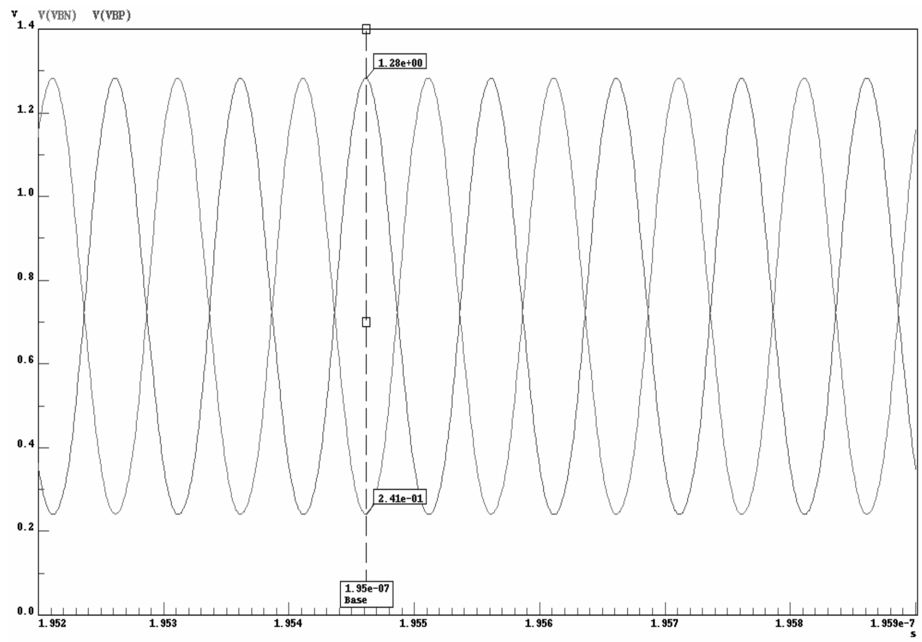


Fig. 2-26 Output voltage of a 10GHz VCO

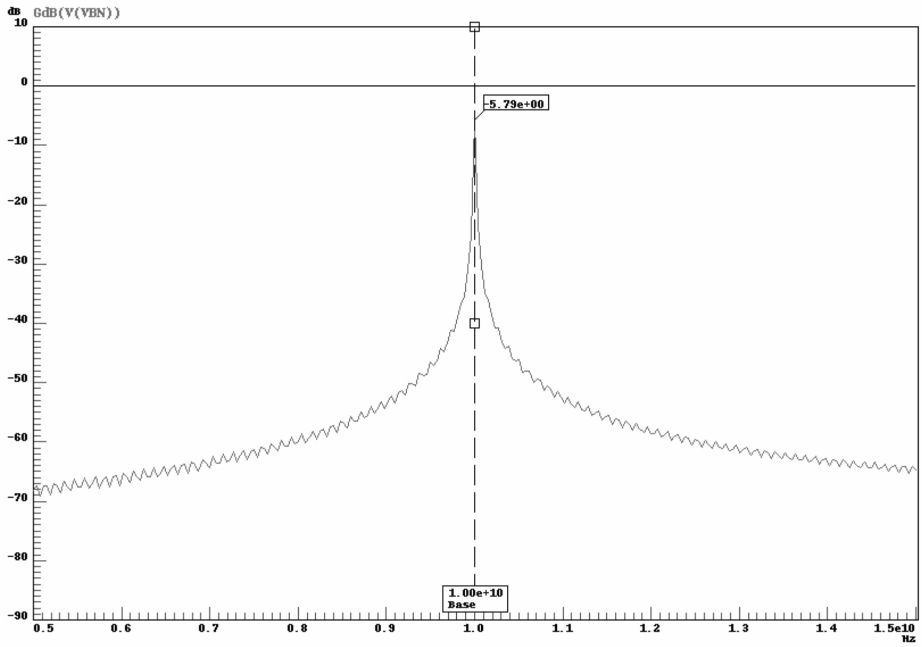


Fig. 2-27 Output power is -5.79dBm at 10GHz

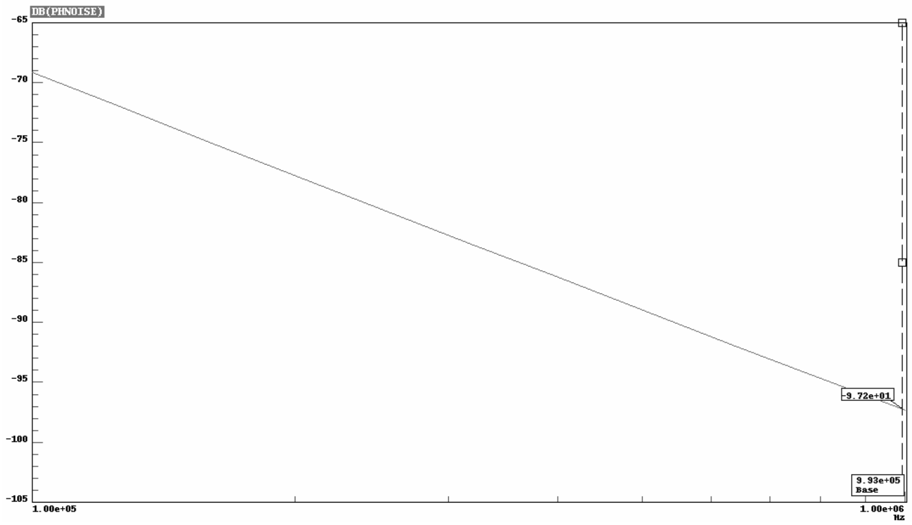


Fig. 2-28 Phase noise is about -97dBc/Hz at 1MHz

Fig. 2-29 is the simulated results of different register input codes. We input 0000000 and 0011111 codes separately to verify whether the output oscillating signal can be properly scaled down by the sequence of dividers and controlled by the register or not. At last in Fig. 2-30 is the chip layout and the dimension of it is 0.998mm X 0.7mm.

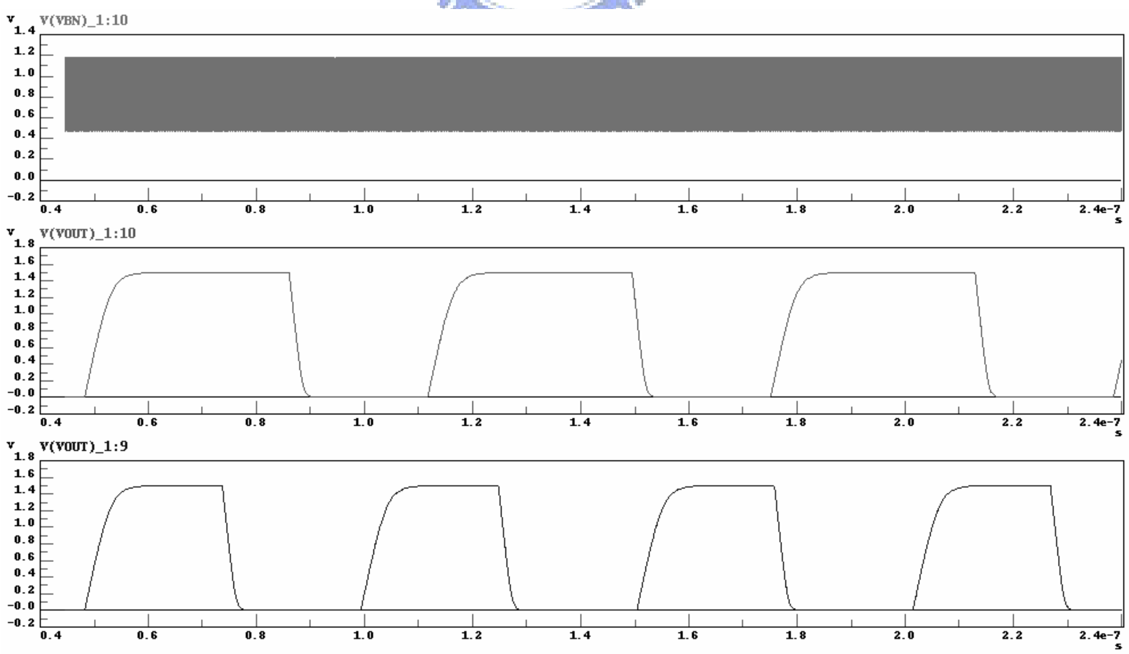


Fig. 2-29 Output signal with a register controlling different division

Tab. 2-1 Summary of the simulation results

Specification	[15] 2006	Simulation Result
Fabrication	0.13μm CMOS	0.18μm CMOS
Supply Voltage	1.5V	1.5V
Center Frequency	7.92GHz	10GHz
Tuning Range	7.84~9.41GHz	9.29~10.9GHz
Tuning Varactors	3	3
Settling Time	1.5ns	25us
Phase Noise	-115dBc/Hz @ 1MHz	-97.8dBc/Hz @ 1MHz
Reference Frequency	33MHz	16MHz
Die Area	1.3mm X 0.7mm	0.998mm X 0.7mm
Power Dissipation	62mW	23.55mW

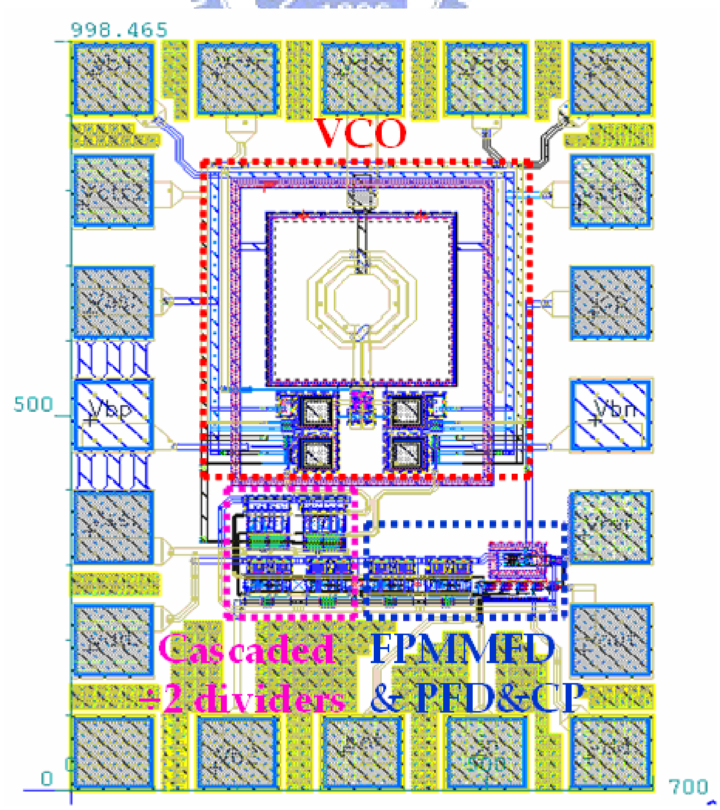


Fig. 2-30 Full chip layout of the 10GHz Synthesizer

2.9 Conclusion

Due to its high channel capacity, an ultra-wide band system is an attractive solution for the implementation of very high data rate (>100Mb/s) short range wireless networks. Nevertheless frequency synthesizers that applied to such high operating frequency are not yet so popular recently not only due to their realistic applications not being extensively but also the serious high frequency parasitic effects that make it more complicate for the designers to meditate the circuit.

However there are still some issues published lately discussing applications to UWB system. According to those references, phase noise suppression and power management will become the first priority while designing. A high oscillating frequency VCO may not only face the problem of circuit stability, parasitic effects will also lead to the frequency deviation, at the meanwhile draw extra power and increase the cost. A frequency divider that operates at high frequency also determines whether a circuit works or not because of the easily varying division. Besides, passive components such as inductors must be redesign since a simple metal path is inductor alike and will lead to unexpected results.

Carefully dealing with those problems may possibly complicate the designing process, but in order to make the circuit owns great performance and high stability, these considerations are important and necessary.

Chapter 3

802.11a Pulse-Swallow Integer-N Frequency Synthesizer

The two most popular structures of RF frequency synthesizers are the fractional-N frequency synthesizer and the integer-N frequency synthesizer. As it tells from the name, the fractional-N structure synthesizes fractional frequency of the reference frequency while the latter one produces integral times of the input signal. In the very beginning of this chapter, we will briefly explain the differences of architectures and applications between these two architectures.

As we just mentioned above that the minimum step size of an integer-N synthesizer equals the reference frequency, however fractional-N breaks this coupling, the step can be designed very small indeed, and designers are free to increase comparison frequency and wide loop bandwidth, locking time is thus reduced, reference spurs and microphonics are eliminated. In Fig. 3-1 it indicates that by periodically changing the division ration from N to N+1 and back, in such that the average is N+A/M where $0 \leqq A < M$ (N, A, M are all integers), the total average ratio will be fractional:

$$N_{avg} = \frac{A \cdot (N+1) + (M-A) \cdot N}{M} = N + \frac{A}{M}$$

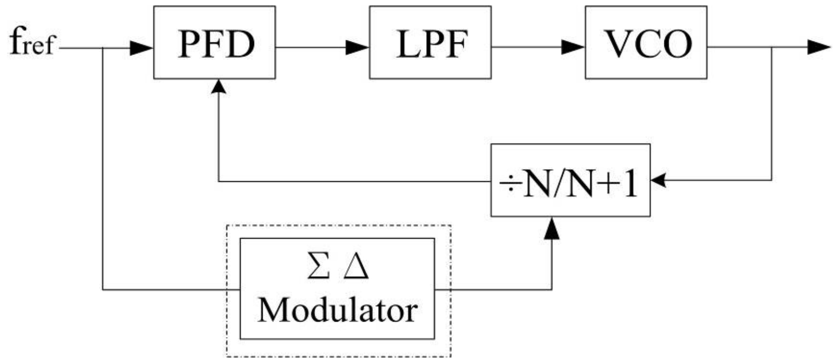


Fig. 3-1 Basic view of Fractional-N Synthesizer

Although fractional-N synthesizer owns great performance in frequency resolution and settling time, its division number depends on accumulator carrier which may lead to spur noise closing to the wanted signal due to the periodically produced characteristic. Figure 2 is a basic topology of integer-N synthesizer, because of the integer multiple of the input signal and constant division number in every reference period, spur noise of integer-N structures is less than Fractional-N synthesizer. Consequently, compared with the integer-N frequency synthesizer, a more complicated modulator is needed to alleviate the influence of noise for fractional-N synthesizer.[16]

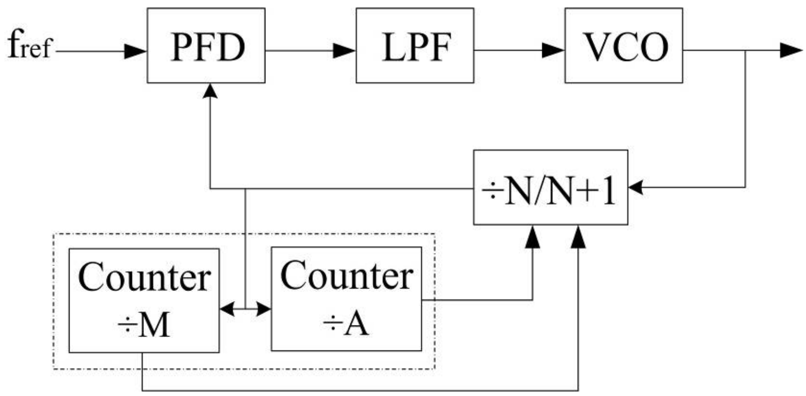


Fig. 3-2 Basic view of Integer-N Synthesizer

If frequency resolution is not the main factor among designing progress (ex: 20MHz for 802.11a/b/g WLANs system), integer-N structure will be the better choice due to its spectrum purity. The comparisons of these two architectures are summarized in Tab. 3-1

Tab. 3-1 Comparison between integer-N and fractional-N Synthesizers

	Integer-N	Fractional-N
Complexity	Low	High
Spurious noise	Well	Poor
Settling time	Slow	Fast
Frequency resolution	Slender	Adequate
Power consumption	Low	Medium

3.1 Architecture

In this chapter we will explain thoroughly a 802.11a pulse-swallow integer-N frequency synthesizer design flow [17]. In Fig. 3-3 shows basic blocks of the circuit. The whole circuit is designed on chip except the loop filter. It is not only because of larger resistances and capacitances required by the loop filter compared with on-chip components, but also for the intention of adjusting the performance which may be influenced by the fabrication variations. The reference frequency is set to 10MHz and a pulse-swallow counter is designed for the purpose of controlling the dual-modulus divider (÷8/9).

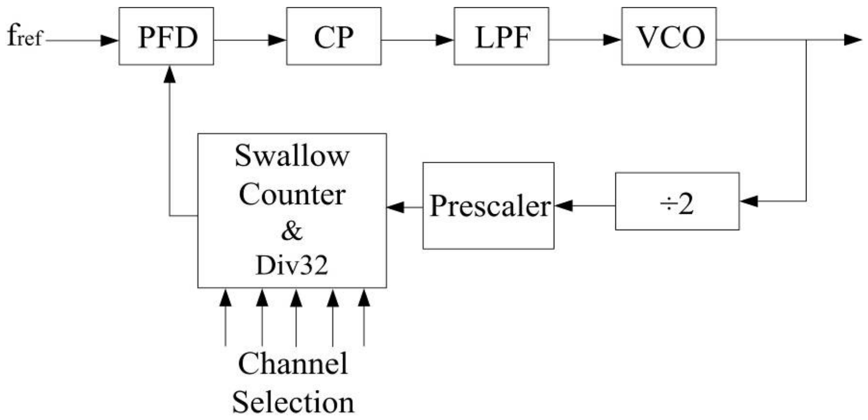


Fig. 3-3 Basic architecture of an integer-N frequency synthesizer

3.2 VCO Design

In order to fit the specifications of 802.11a WLANs system, we adopted a differentially and complementary cross-coupled pairs to generate 5GHz differential symmetric signal outputs [19]. The circuit is shown in Fig. 3-4, as we can see; using both PMOS and NMOS cross-coupled pairs at the same time provides higher negative resistance and symmetries the output waveform. With differential outputs, the common-mode noise coupled from substrate can be alleviated certainly and will lead to impressive low phase noise, meanwhile, since PMOS owns great ability against flicker noise, it can suppress noise up-converted from 1/f noise and other low frequency noise sources efficiently. The design concepts of varacters and buffer used in this circuit are the same as mentioned in Chapter 2.

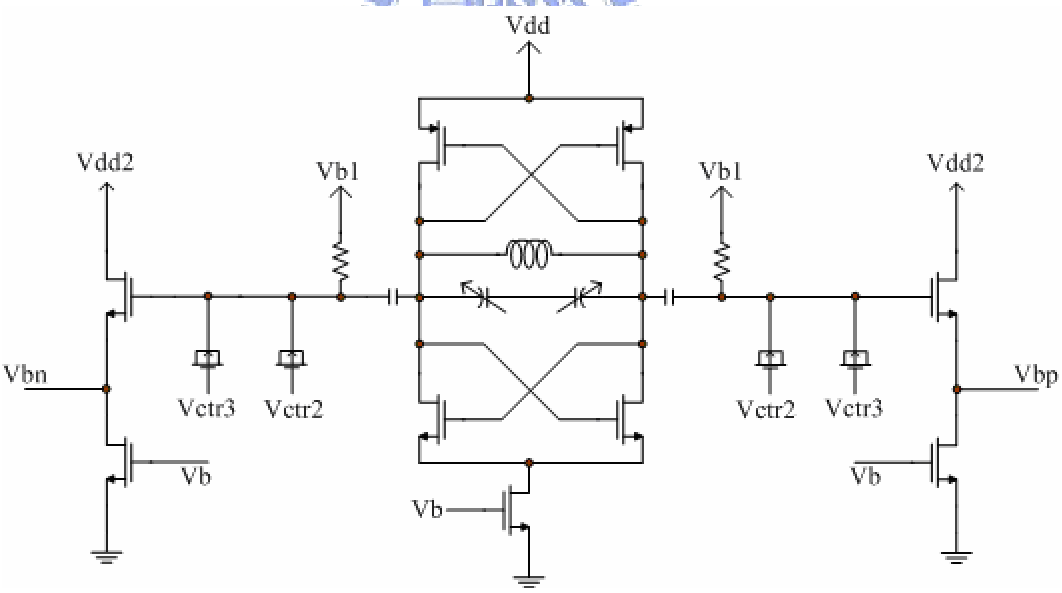


Fig. 3-4 5.2GHz Voltage controlled oscillator architecture

3.3 High Speed Frequency Divider

In this work, we apply D-type flip flop operation principles to achieve an analog DFF divide- by-2 circuit shown in Fig. 3-5 since all digital units will not function properly at high operating frequency. We can find out in the figure that a divide-by-2 circuit needs to be well planned while performing layout because of its high sensitivity to those parasitic capacitances and resistances resulted from cross signal lines. So take these parasitic effects into consideration during circuit simulation make it the key to precisely division. Fig. 3-6 is the transient simulation result of a 5.2GHz sine wave inputted divider that operates from 4~6GHz with 70 mV minimum acceptable input signal.[12][13]

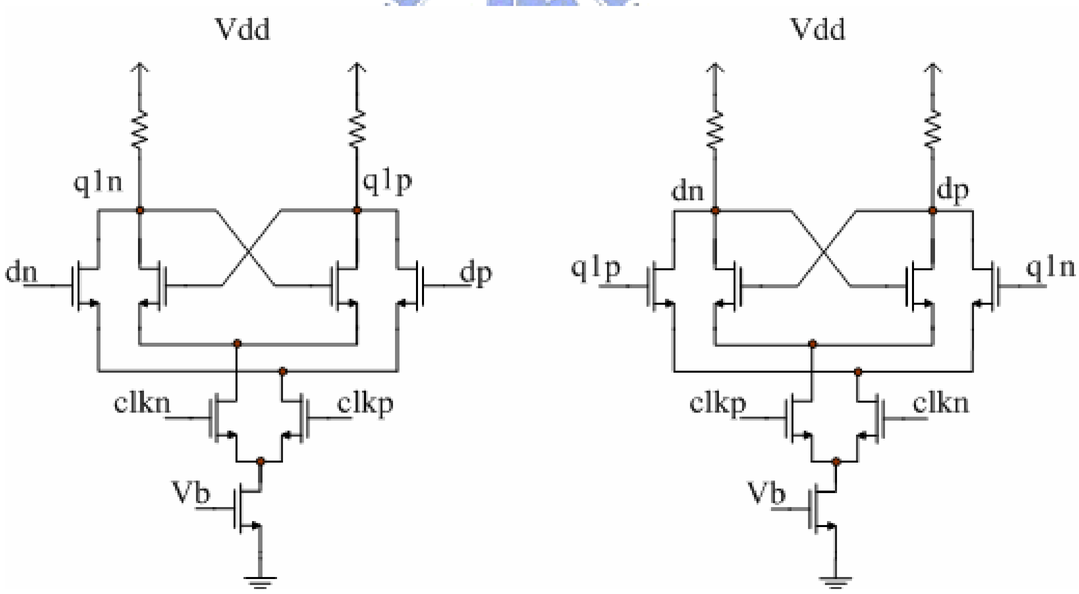


Fig. 3-5 Analog structure of a divide-by-2 circuit

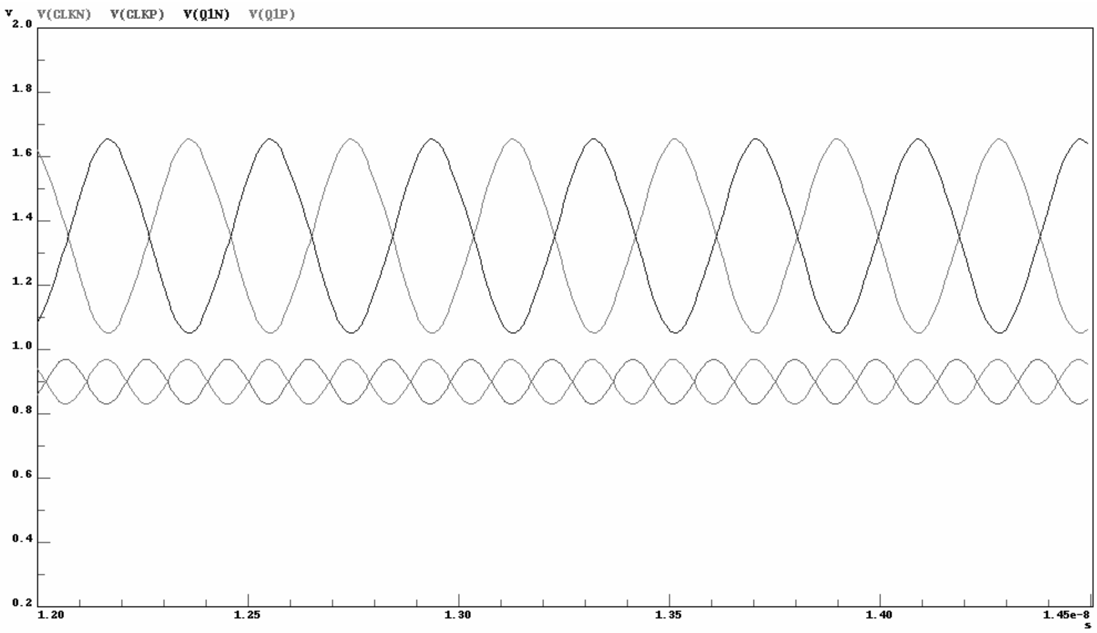
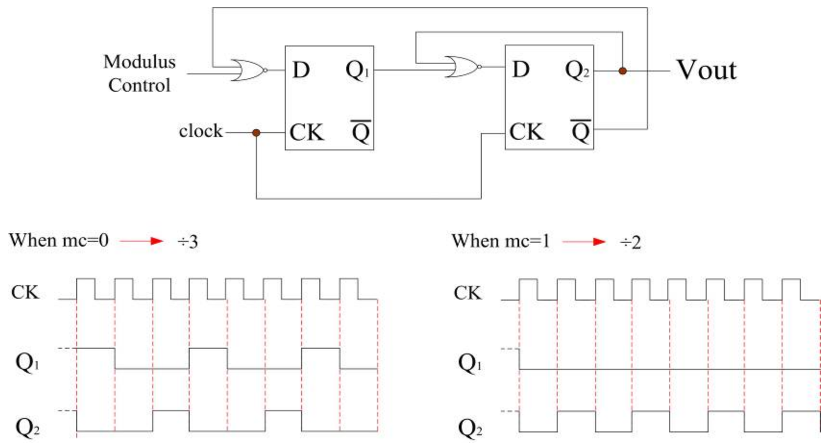


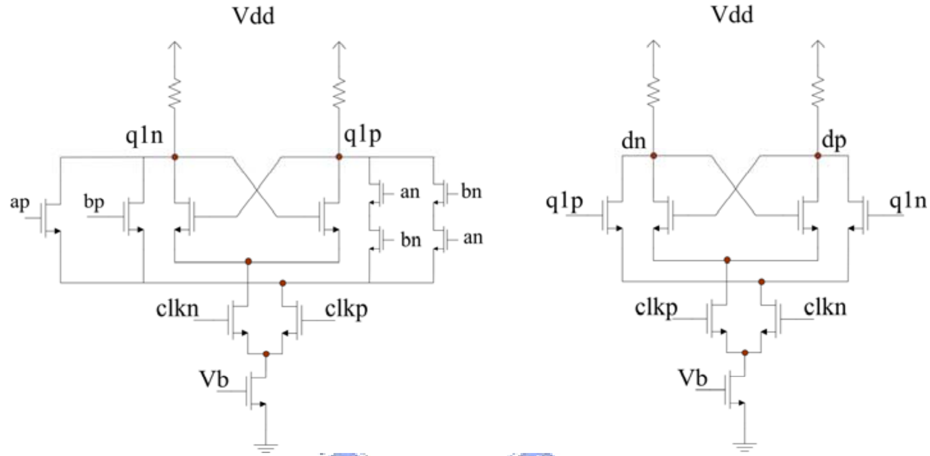
Fig. 3-6 Simulation result of a divider with 5.2GHz, 80mV sine wave input

3.4 Dual-Modulus Frequency Divider (DMFD)

Since we modulate the oscillating frequency by setting control signals to change the total divisor, a circuit which can carry out more than one division is needed. In this design work we realize a dual-modulus frequency divider that can switch division between 2 and 3 by combining NOR gates to D-type flip-flops. The circuit prototype is shown in Fig. 3-7(a) with clock time diagram analyzed, and the single analog D-type flip-flop is also presented in Fig. 3-7(b). Besides, a DMFD can also accomplished by substituting the NOR gates for NAND gates which graphed in Fig. 3-8.



(a)



(b)

Fig. 3-7 (a) The Prototype of DMFD and its clock timing diagram

(b) Architecture combining both DFF and NOR gate

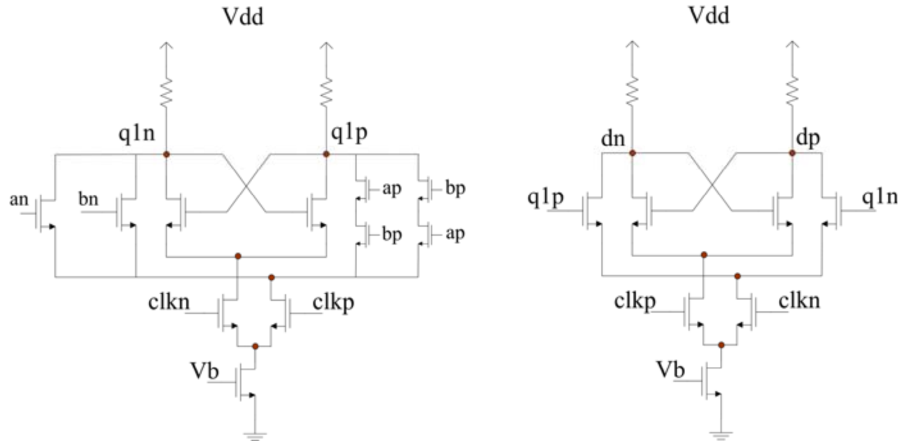


Fig. 3-8 Architecture combining both DFF and NAND gate

As the same situation mentioned in last section, a DMFD must be well constructed and be carefully dealt with its parasitic effects which are due to the complicated cross-coupled signal lines. So the layout is laid in a compact way and the estimated parasitic capacitances about 25fF are connected to the output nodes. Because of the additional D-type flip-flops, a DMFD costs more power than a divide-by-2 divider does.

3.5 Prescaler Design

The prescaler in this design work is actually a combination of two divide-by-2 dividers and a DMFD, thus makes the total division varies between 8 and 9. It is connected right after the outputs of a divider that the main function is to lower down the oscillating frequency. The circuit blocks are shown in Fig. 3-9, the modulus control signal (mc) is provided by the pulse-swallow counter which will be explained in next section. In this figure exist some digital components, since a clear and definite signal must be generated to control the division,delay time and output signal magnitude between each circuit have to be well-planned. The frequency synthesizer generally fails because of signal mistakes in prescaler.

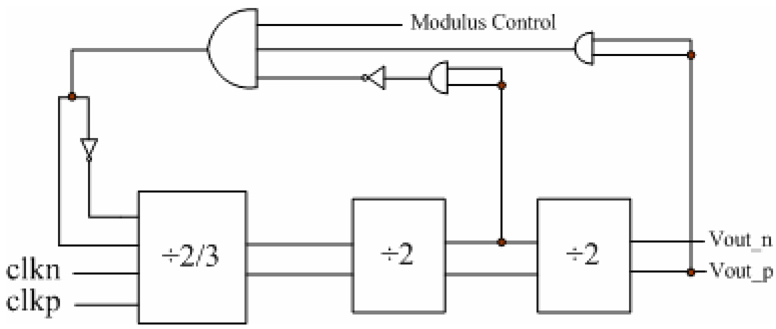


Fig. 3-9 Components of a prescaler

3.6 Pulse-Swallow Counter

Pulse-swallow counter is the key circuit in the close loop design since it controls dual modulus division (÷8/9) we just discussed. It consists of a channel detecting circuit and a loading / resetting counter. The basic way it operates is that the counter counts up from zero to the setting input codes (e.g. 00111), then be reset to counts down from 28 to the input codes thus makes a period of 32. Each block will discuss thoroughly below.[20]

3.6.1 Loading and Resetting Counter

Fig. 3-10 shows a loading and resetting counter consists of 5 JKFFs with which J and K are shorted together. The control signal UD determines the counting mechanism of the circuit, when the signal is low, the counter will count up, and comparatively it will count down if the control signal UD is set to high. In the very first beginning, we set the loading number to 28 instead of 32, this is because that switching between count-up and count-down consumes two clocks and the input codes appear twice cost one extra clock.

The counter counts up from 0 and UD=RL=high at first, when A1~A5 equal to the external channel input codes, RL will be set to low only for one single clock and switched back to high, at the meanwhile, the counter resets and UD changes to low forcing the counting mechanism reversed downwards from 28. As A1~A5 equal to the channel input codes again, RL changes to low still for one clock, and UD turns to high making the counter to re-count upwards from 0. The clock timing diagram is shown in Fig. 3-11.

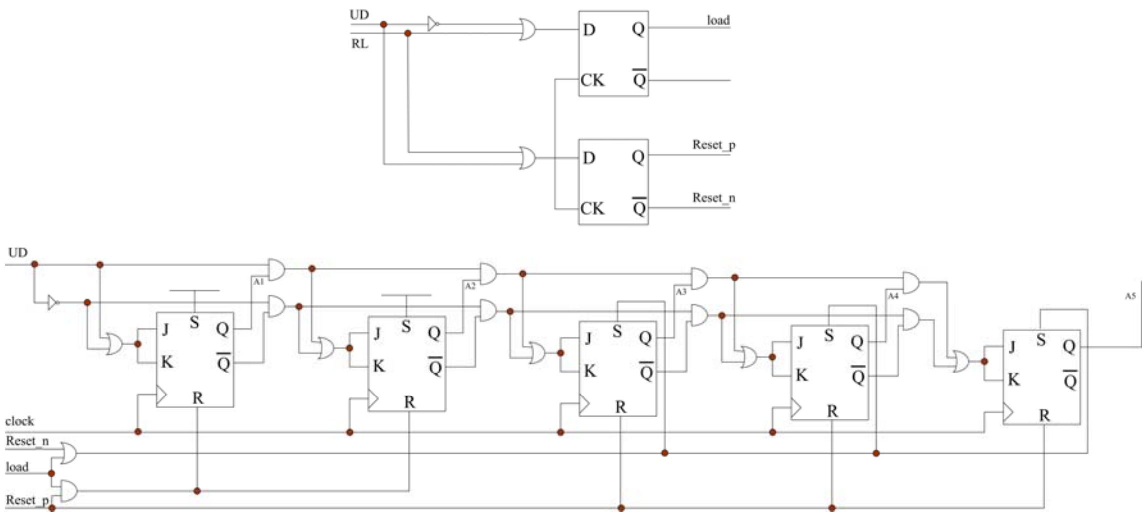


Fig. 3-10 Loading and resetting counter

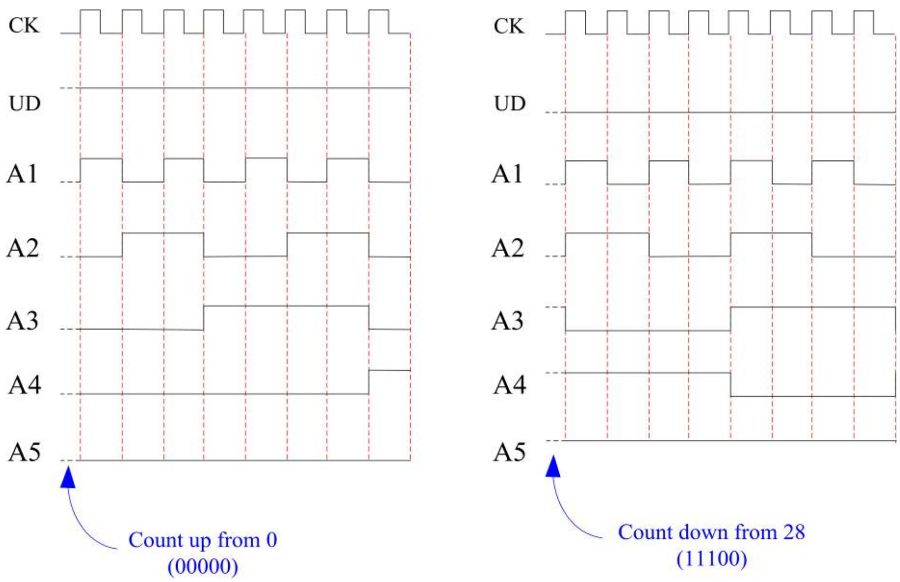


Fig. 3-11Timing diagram of loading and resetting counter

3.6.2 Pulse-Swallow Counter [21][22]

The fully-integrated pulse-swallow counter is shown in Fig. 3-12, we can see that the 5 output signals of the loading / resetting counter are connected to XORs to compare with the external channel input signals. As long as A1~A5 equal Ch1~Ch5, the RL signal will turn into low and consequently make the JKFF, which J, K shorted together, output a low level signal sent back to UD. Remember that the RL signal will swap between high and low only on the instance A1~A5 equal Ch1~Ch5.

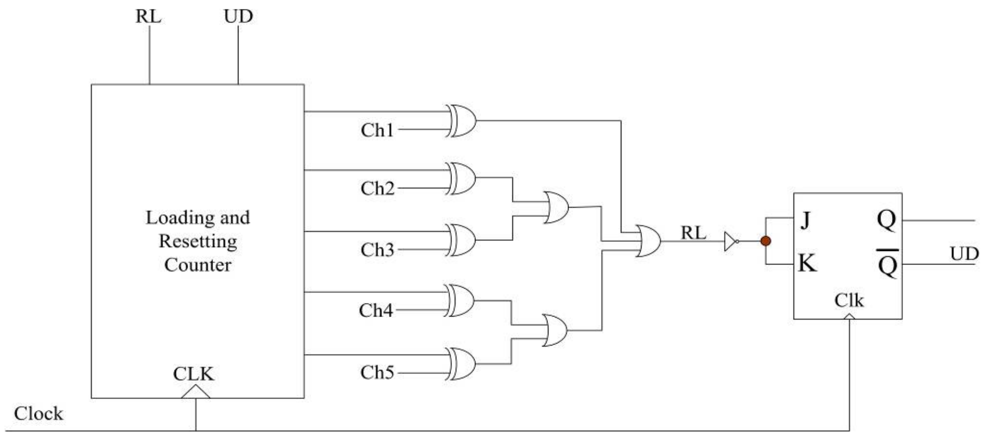


Fig. 3-12 Architecture of fully-integrated pulse-swallow counter

We mentioned in last section that the load number of the counter should be set to 28 instead of 32, it can be explained by the timing diagram shown in Fig. 3-13. Assume the external channel input codes are 00110 (i.e. 6), no matter the counter counts up from 0 or counts down from 28, the digit 6 is calculated twice, and the same circumstance occurs during loading the codes and reset the counter.

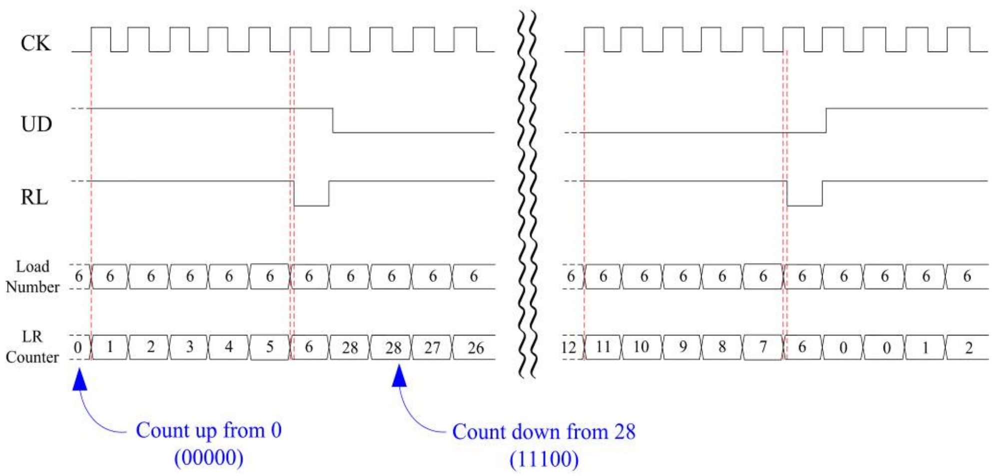
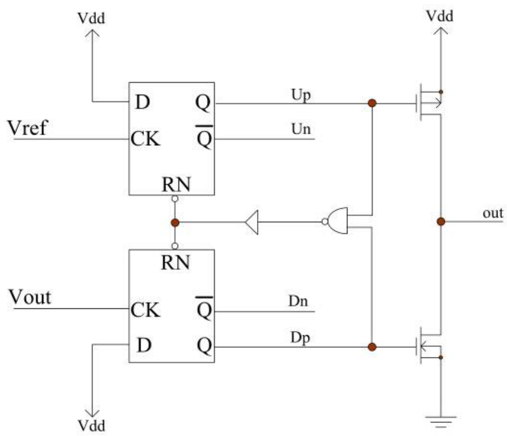


Fig. 3-13 Analysis of a pulse-swallow counter

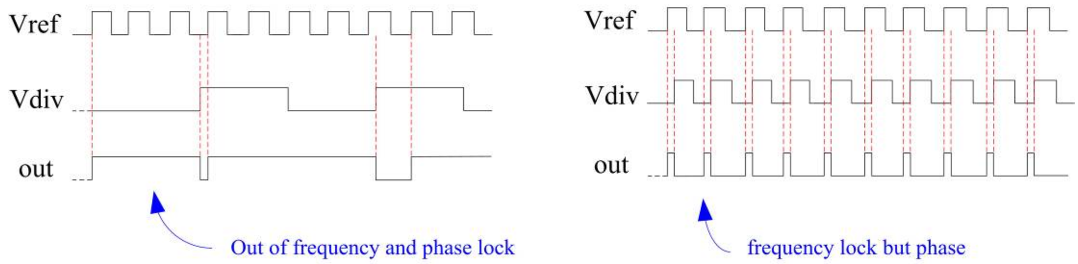
3.7 Phase / Frequency Detector

The heart of a synthesizer is the phase / frequency detector. This is where the reference frequency signal is compared with the signal fed back from the voltage controlled oscillator output, and the resulting error signal is transformed into current by charge pump in order to drive the loop filter and the VCO control bit. Generally in a RF frequency synthesizer design, the VCO output signal will be scaled down gradually by several analog and digital dividers so that the frequency inputting to a phase / frequency detector will be only a few tens MHz, and for this reason, a digital PFD is the most adopted in designing RF frequency synthesizers.[25]

Down below in Fig. 3-14(a) shows a basic implementation of PFD and a simple charge pump which in next section will be described, basically consisting of two D-type flip flops and digital delay cells. As we can see in the Fig. 3-14(b), if the reference signal (V_{ref}) is faster than the signal scaling down from VCO (V_{div}), the upper flip flop will send the output high and this is maintained until the first rising edge occurs on V_{div}, till then the NAND gate will generate a signal low back to reset both flip flops. In a practical system this means that the output which input to the VCO is driven higher forcing the oscillating frequency to catch up with the reference signal, vice versa.



(a)



(b)

Fig. 3-14 (a) Phase / frequency detector

(b) Time diagram comparison between Vref and Vdiv

3.8 Charge Pump

Fig. 3-15 shows the architecture of a charge pump which functions as a transforming mechanism turning phase mismatch detected by PFD into a charging current. In this project the charge pump works with a fixed reference current, and in order to obtain high voltage output range, the transistor size of the current mirror transistors (M_1~M_{11}) must be designed carefully.

Besides, since mismatched current produced at the time the two input signals out of phase will cause interference with adjacent channel and spurious tones in RF receiver, we will implement two extra transistors (M_{12}, M_{14}) in the circuit to solve the problem. Those two NMOS guarantee that M_{13} and M_{15} sources are already pre-charged when switching takes place. Also an accurate layout of the circuit can improve the matching among the positive and negative currents to reduce undesired spectral emission in RF transmitter.

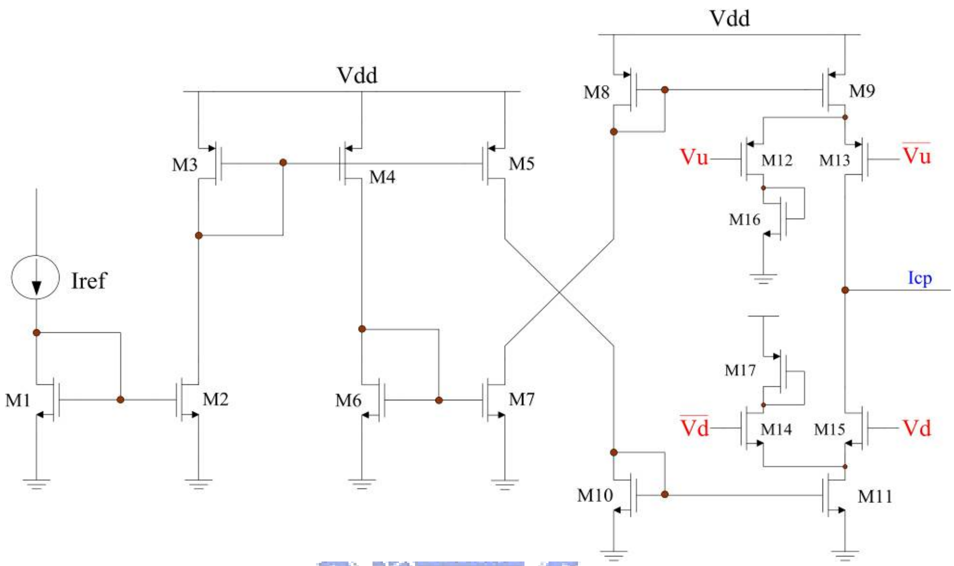


Fig. 3-15 Schematic of charge pump

3.9 Loop Filter

We choose a 3rd order RC loop filter in this work as shown in Fig. 3-16 since it is an extremely critical key point in designing a frequency synthesizer. Output of a loop filter is a dc voltage and directly connected to VCO, so a well considered circuit not only can degrade high frequency noise but also prevent the disturbance produced while PFD and charge pump switching states from influencing VCO, and at the meanwhile can the synthesizer come to stable. Loop bandwidth of the filter owns great affections to the synthesizer settling time, so we make the filter the only one circuit exclude from the chip so as to modulate the response of the circuit. Based on simulation results, we can obtain a set of element values and are shown in Tab. 3-2.

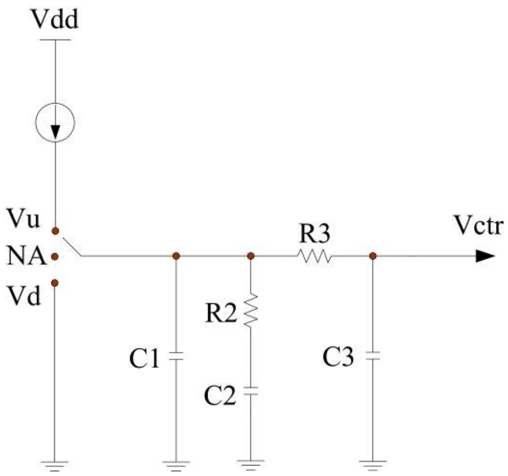


Fig. 3-16 A 3rd order loop filter

Tab. 3-2 Optimized loop filter elements

Component	Value
C1	19.92 pF
R2	19.57 kΩ
C2	300 pF
R3	4 kΩ
C3	39.79 pF

3.10 Synthesizer Simulation Results

All of the building blocks mentioned before will be combined into a single frequency synthesizer to simulate together and display in this section. Fig. 3-17 is the whole circuit schematic, and Fig. 3-18 shows the frequency synthesizer pre-analyzed by MATLAB since the whole circuit simulation takes a lot of time.[23]

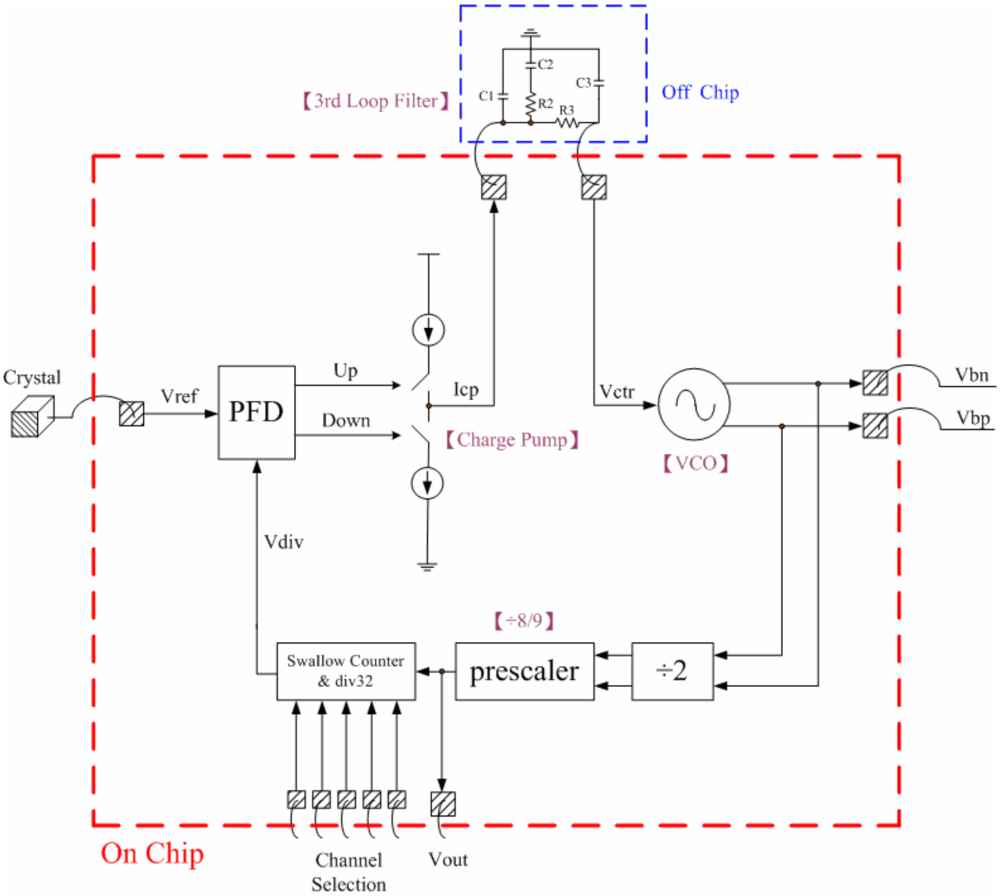


Fig. 3-17 Schematic of an integer-N frequency synthesizer

We can find out in the figure that the phase margin is more than 55 degree. After that, we adopt Eldo RF to examine whether the close loop performance meet our expectation or not and the results in Fig. 3-19 shows that the settling time is less than 30μs (the circuit enters the stable region at about 20μs), also in Fig. 3-20 shows the output power spectrum with the peak magnitude -9.9dBm, and Fig. 3-21 is the channel-switching result between 00000 and 00010 (at the meanwhile, oscillating frequency changes from 5.14GHz to 5.20GHz). In Tab. 3-3 are the results of the full circuit closed-loop simulation, The layout of an integer-N frequency synthesizer that occupies a dimension 1.219mm^2 is shown in Fig. 3-22 which.

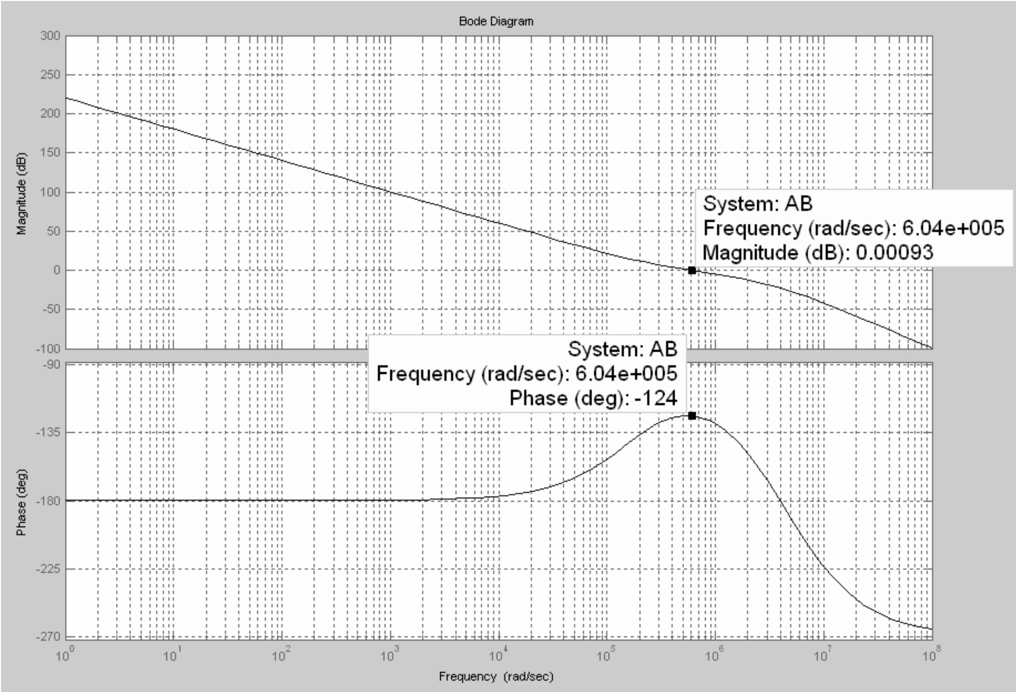


Fig. 3-18 MATLAB simulation results

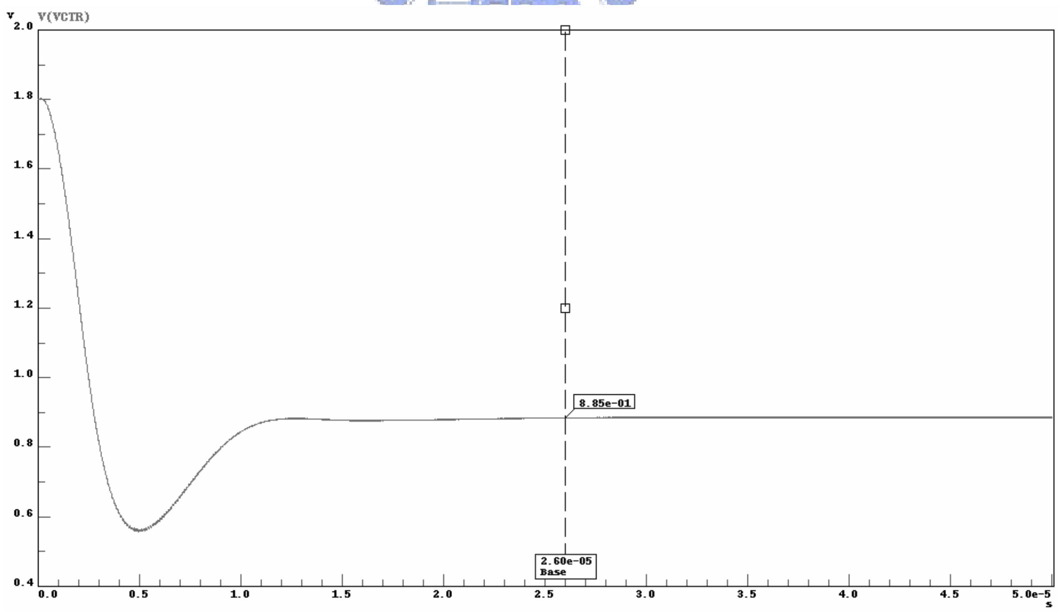


Fig. 3-19 Settling time of the close loop is less than 30μs

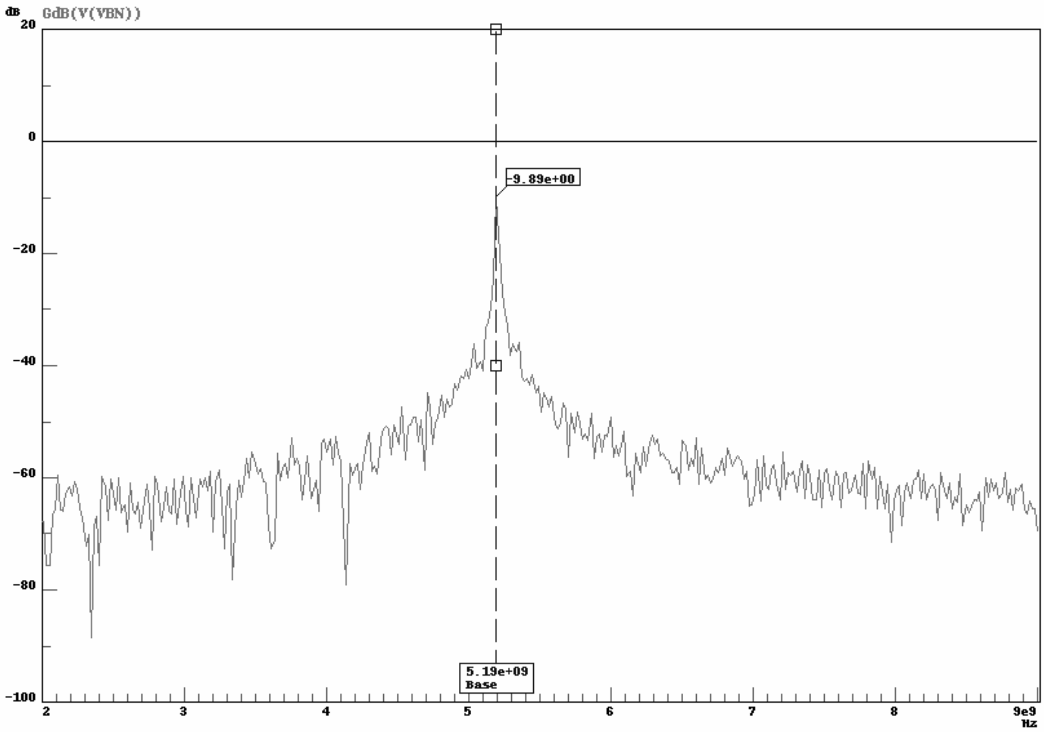


Fig. 3-20 Output power spectrum (about -9.9dBm)

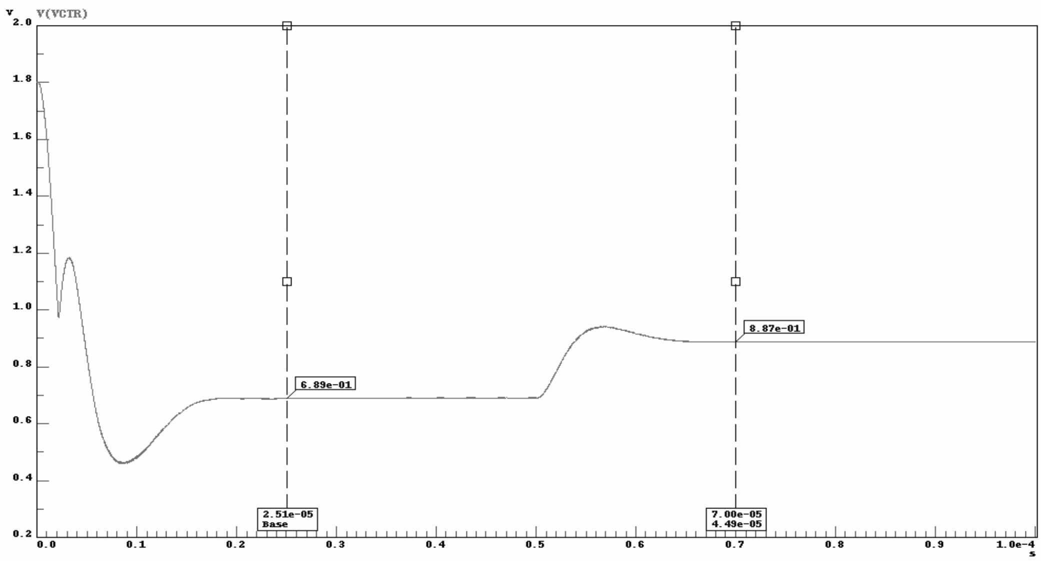


Fig. 3-21 Channels switch from 00000 to 00010 (5.14GHz to 5.20GHz)

Tab. 3-3 Simulation results of a integer-N frequency synthesizer

	Simulation Results
Application	802.11a
Manufacturing process	TSMC 0.18um CMOS
Supply voltage	1.8V
Synthesizer type	Integer-N pulse-swallow
Oscillating frequency	5.2GHz
Reference frequency	10MHz
Tuning range	4.95GHz~5.82GHz
Phase noise	-114dBc/Hz @ 1MHz
Settling time	20us
Output power	-9.9dBm
Die area	1.15mm X 1.06mm
Power dissipation	18.844mW

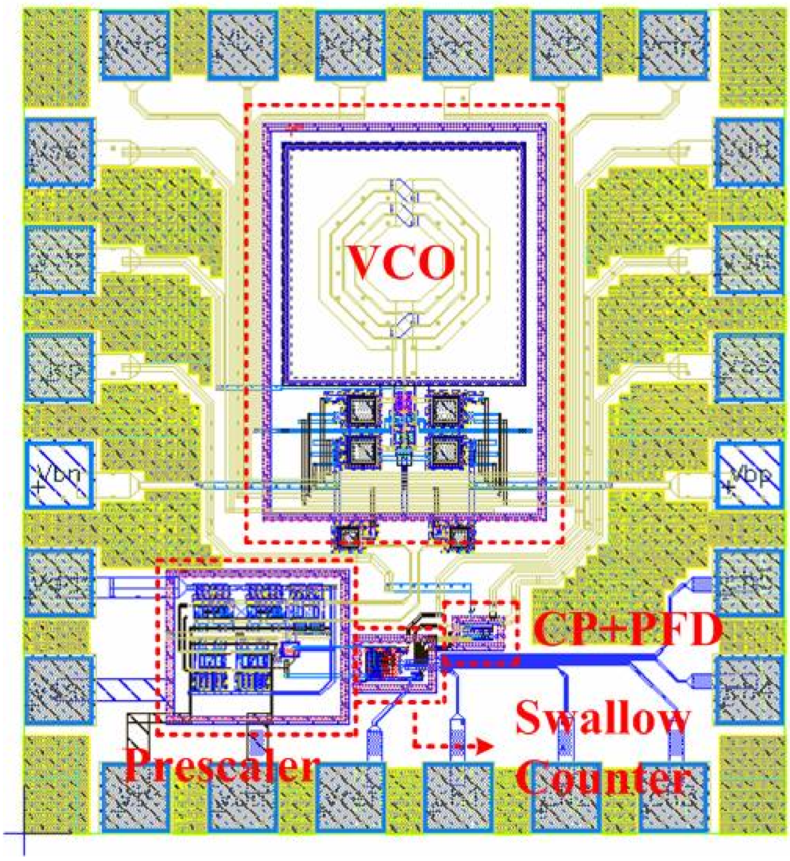


Fig. 3-22 Layout of the integer-N frequency synthesizer

3.11 Measurement Results

3.11.1 Measurement Preparation

Since a frequency synthesizer owns a lot of output pads including supply voltage, bias voltage, input channel control signals, reference signal, and output signals, it is quite unlikely to measure the whole circuit on wafer. We design a PCB (printed circuit board) layout which graphed in Fig. 3-23 and use SMA connectors to make it possible connect the circuit to the measuring equipments. The measuring equipments for VCO and frequency synthesizer contains Agilent E5052A signal source analyzer (Fig. 3-24a at CIC), Agilent E4407B spectrum analyzer (Fig. 3-24b at CIC), HP 8563E spectrum analyzer (Fig. 3-24c at lab), HP54610B oscilloscope (Fig. 3-24d at lab), HP E3611A power supply (Fig. 3-24e at lab), and HP33120A function generator (Fig. 3-24f at lab).

While designing a PCB layout, we can tell from Fig. 3-23 that the line widths of the output signal from VCO need to be matched to 50Ω which is the interior resistance of the instruments. We also reserve extra space for bypass and DC blocking capacitors, and the chip is stuck to the board with all I/O pads bounded onto it via bond-wires. Fig. 3-25 is the practical FR4 PCB measurement circuit and the die photo is shown in Fig. 3-26.

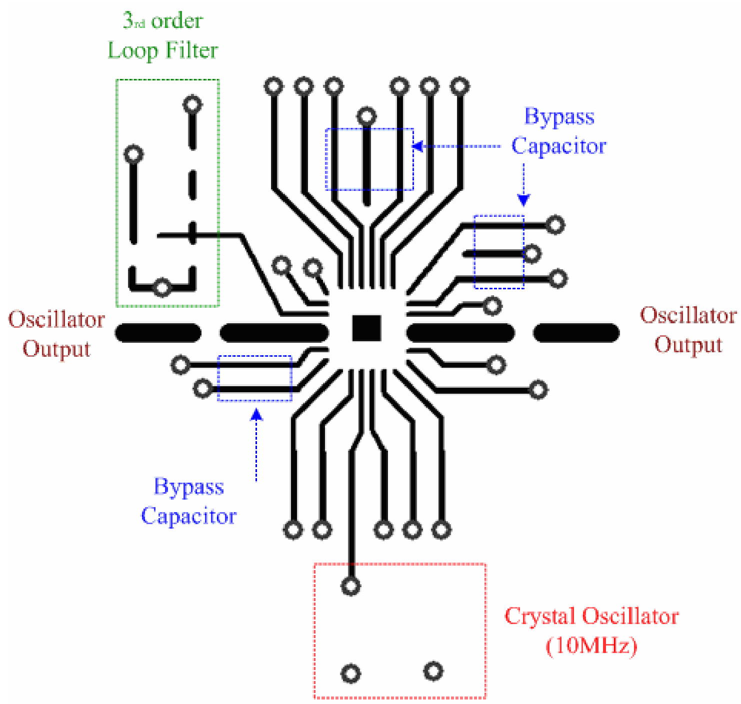
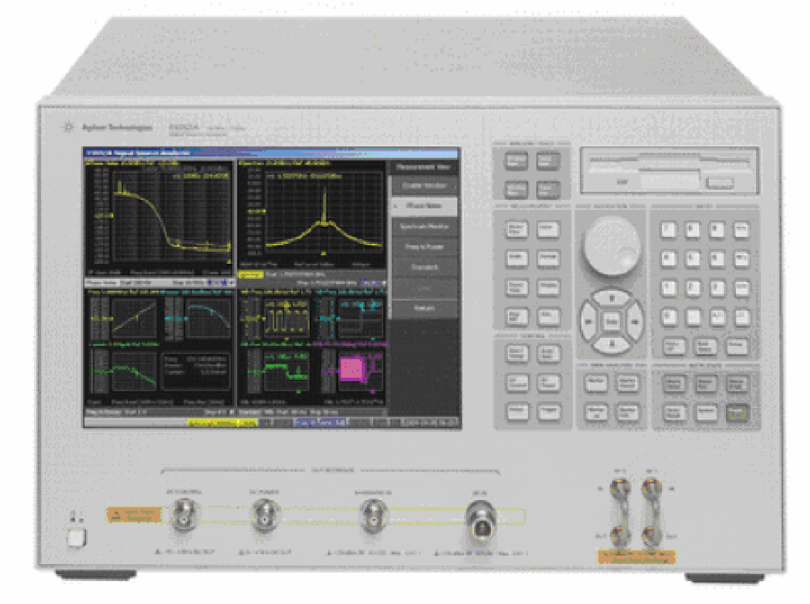
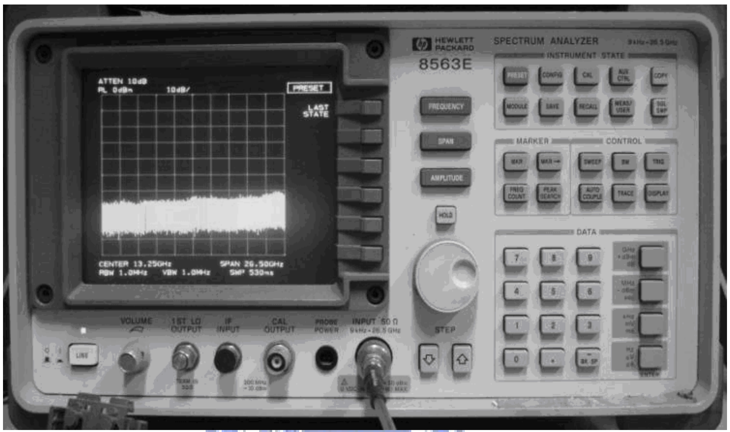


Fig. 3-23 PCB layout of the frequency synthesizer



(a)

(b)


HEWLETT PACKARD
SPECTRUM ANALYZER
8563E
INSTRUMENT STATE
FREQUENCY
SPAN
AMPLITUDE
MARKER
CONTROL
DATA
ATTEN 10dB
RL 0dBm 10dB/
PRESET
LAST STATE
CENTER 13.25GHz SPAN 26.50GHz
RBW 1.0MHz VBW 1.0MHz SWP 530ms
VOLUME
1ST LO OUTPUT
IF INPUT
CAL OUTPUT
PROBE POWER
INPUT 50 Ω
STEP

(c)


HEWLETT PACKARD
54610B OSCILLOSCOPE
500 MHz
STORAGE
HORIZONTAL
TRIGGER
VERTICAL
Volts/Div
Position
Time/Div

(d)

(e)

(f)

Fig. 3-24 (a) Agilent E5052A signal source analyzer

(b) Agilent E4407B spectrum analyzer (c) HP 8563E spectrum analyzer

(d) HP54610B oscilloscope (e) HP E3611A power supply

(f) HP33120A function generator

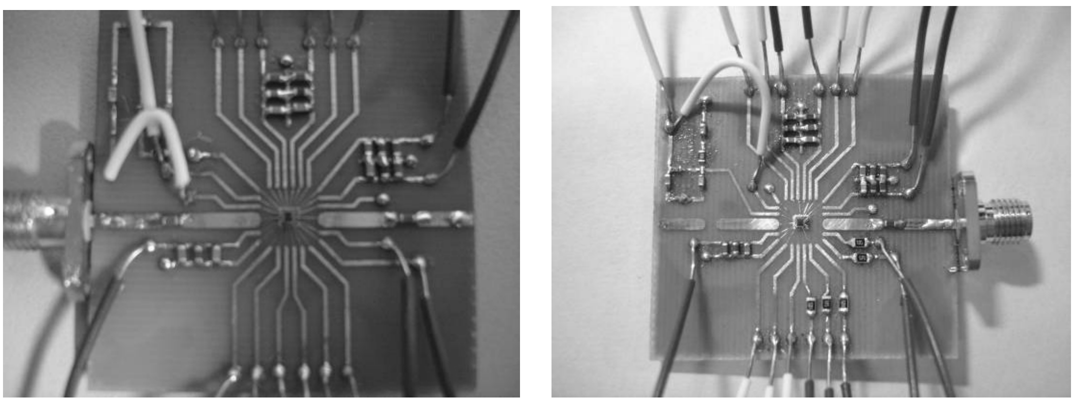


Fig. 3-25 A practical FR4 PCB measurement circuit

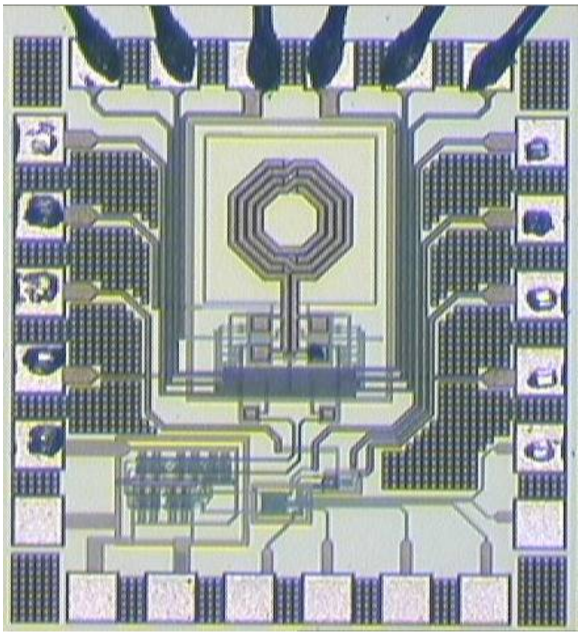


Fig. 3-26 A 5.2GHz integer-N frequency synthesizer

3.11.2 Measurement Results

First we will discuss about the tuning curve and output power of the voltage controlled oscillator. We can see from Fig. 3-27 that all the banks (from 00 to 11) include the frequency range needed, namely, as long as picking up the right control bits corresponds to each bank can we make the frequency synthesizer lock successfully. In Fig. 3-28 is the comparison of tuning range between simulation and measurement at bank 10.

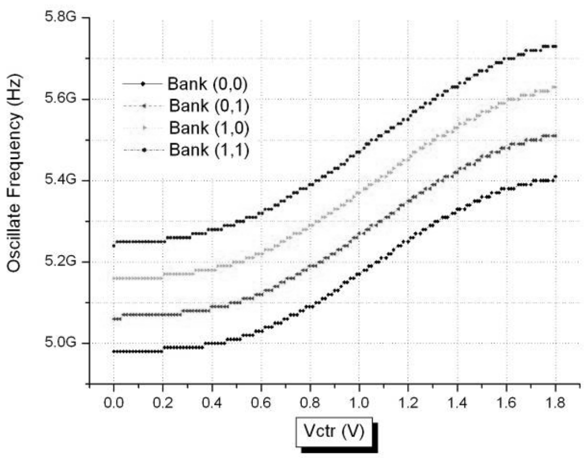


Fig. 3-27 Measured tuning range under different banks

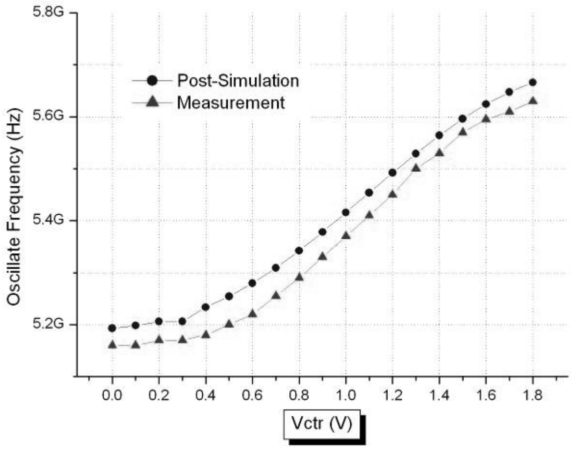


Fig. 3-28 Comparison between post-simulation and measurement at bank 10

According to the graph, a successful prediction of parasitic capacitor was performed since that the central part of tuning curves are almost the same linear for both post-simulation and measurement even though there is a little difference when control voltage is nearly 0V and 1.8V.

Next we will find out the critical parameter of a voltage-controlled oscillator, phase noise. First we set the buffer’s bias voltage to 0.9V just as what has been done during the simulation to examine the phase noise at 1MHz offset from the carrier and obtain the result shown in Fig. 3-29. However the output power is smaller compared to the simulation result, we raise the bias voltage up to meet the DC analytic anticipation and come to the end which is almost the same as expected.

Fig. 3-30(a) shows the post-simulation result, Fig. 3-30(b) shows the measurement, and Fig. 3-31 is the output power spectrum showing the magnitude of -13.5dBm. Besides we can improve the phase noise by adjusting the bias voltage, consequently a value -126dBc/Hz is obtained and shown in Fig. 3-32.

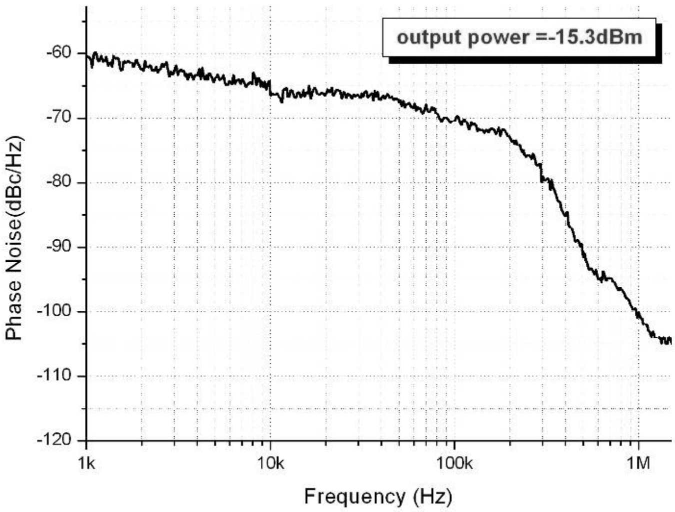
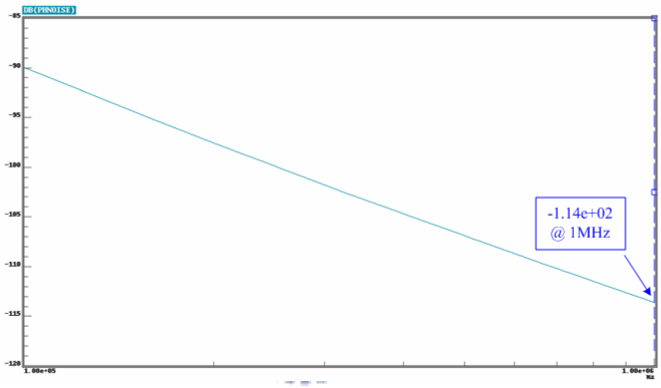
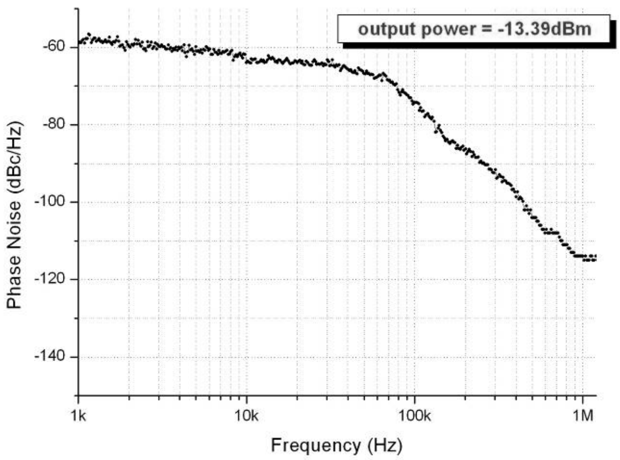


Fig. 3-29 Phase noise is about -100dBc/Hz @ 1MHz with V_b=0.9V



(a)



(b)

Fig. 3-30 (a) Post-simulation phase noise is -114dBc/Hz @ 1MHz

(b) Measured phase noise is -114dBc/Hz @ 1MHz

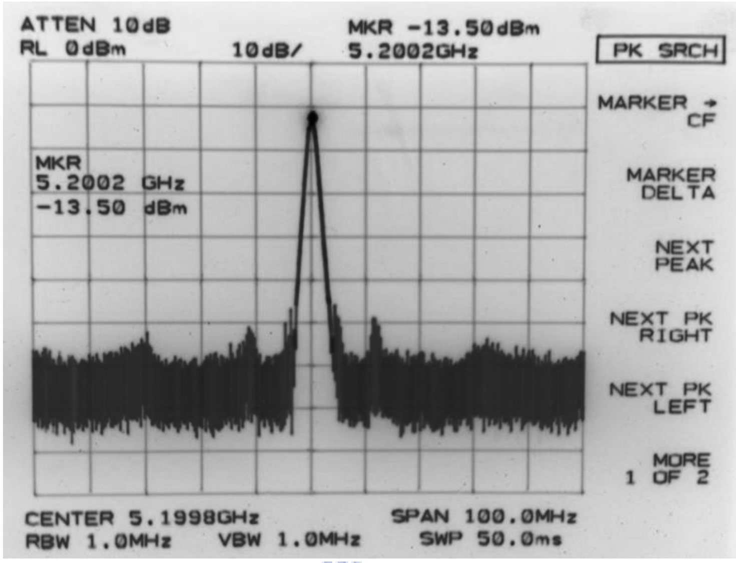


Fig. 3-31 VCO output power is -13.50dBm at 5.2GHz

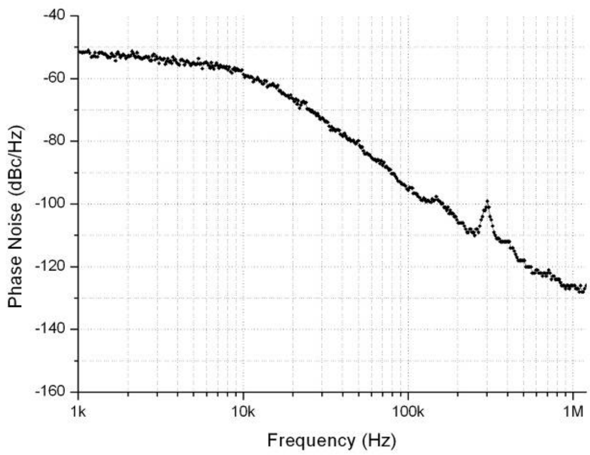


Fig. 3-32 Phase noise is -126dBc/Hz @ 1MHz after adjusted

Down below in Fig. 3-33 is the measurement result of the settling time while applying a periodical clock signal to the division control bit. Since it is impossible to read the settling time from an oscilloscope directly due to the locking time ranges at micro-seconds, we have to observe the transient by switching the total division through a function generator.

As which can be distinguished that the settling time is just a little bit longer than 20μs which derived from the simulation. The control voltage is stably locked at about 40μs. Tab. 3-4 shows the comparison between the simulation and the measurement results while Tab. 3-5 is the comparison with the references.

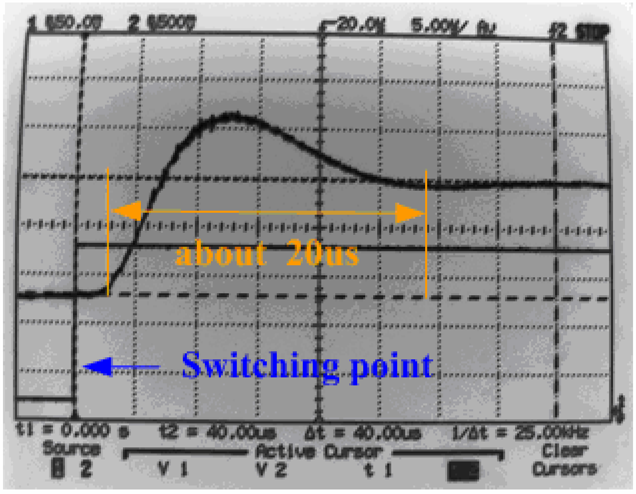


Fig. 3-33 Settling time of the close loop

Tab. 3-4 Comparison between simulation and measurement

Spec.	**Simulation**	**Measurement**
Tuning Range	4.95GHz~5.82GHz	4.98GHz~5.73GHz
Phase noise	-114dBc/Hz @ 1MHz	-126dBc/Hz @ 1MHz
Settling time	20us	~20us
VCO output power	-9.9dBm	-13.5dBm
Power dissipation	18.844mW	26.35mW

Tab. 3-5 Comparison between reference papers and this work

Reference	[16] 2005	[19] 2005	[17] 2003	[8] 2003	This work
Frequency band (GHz)	N/A	4.11~4.35	5.15~5.70	5.15~5.82	4.98~5.73
Tuning range	N/A	5.64%	27.2%	N/A	14.42%
Phase noise	-125dBc/Hz (@3MHz)	-139dBc/Hz (@20MHz)	-116dBc/Hz (@1MHz)	-106dBc/Hz (@1MHz)	-126dBc/Hz (@1MHz)
Divider architecture	Fractional-N	Integer-N	Integer-N	Fractional-N	Integer-N
Reference frequency	N/A	16MHz	10MHz	19MHz	10MHz
Settling time	25us	N/A	100us	520us	20us
Power consumption	54mW	9.68mW	13.5mW	N/A	26.35mW
Supply voltage	1.8V	1.0V	2.5V	1.8V	1.8V
Manufacturing process	0.18um	0.18um	0.25um	0.18um	0.18um

Chapter 4

Conclusions and Future Works

4.1 Conclusions

We have presented a frequency synthesizer that applied to MB-OFDM UWB 5th band group. Throughout the design, each component is accomplished in the traditional architecture in order to testify the possibility for an ordinary circuit to operate at high frequency. A differential-in center-tapped inductor is adopted while designing a 10GHz VCO not only for the chip area consideration but also anxiety for high Q value and impressive performance in phase noise. Only NMOS cross-coupled pairs are used instead of NP cascaded structure as mostly seen prevents the upper voltage limitation occurs a lot in the latter one and make it easier to design.

Fully programmable multi-modulus frequency divider is consists of 7-stage cascaded divide by 2/3 circuits with varying division from 128 to 159 and is used to scaled down the operating frequency for the phase/frequency detector to compared with the reference signal. A register is designed to load all the divider control signals since that preparing each control path a pad will lead to extremely large chip size. The VCO is simulated to have a 1000mV peak-to-peak voltage swing at 10GHz and -5.79dBm output power. The tolerant frequency range varies from 9.29GHz to 10.9GHz due to adjustment of two-pairs of varactors, besides it owns a -97dBc/Hz phase noise at 1MHz and a settling time at about 25us.

After that we introduce an integer-N frequency synthesizer applied to IEEE 802.11a. In the design a cascode NMOS and PMOS cross-coupled pairs forms the core circuit of the voltage controlled oscillator, only a single dual modulus frequency is adopted in order to lower power consumption. A pulse-swallow counter is designed to control the switching mechanism of the dual modulus frequency divider by comparing the internal proceeding signal with the external setting control bits. The loading number is set to be 28 instead of 32 due to extra clocks needed during the comparison takes place.

The tuning range measurement results are very alike to the simulations although shift down slightly. This may results from the neglect of parasitic inductors which come from the overlong metal line connected to the output pad while simulating. It can be solved henceforward by using other simulation software such as SONNET. The measuring phase noise comes to the best at about -126dBc/Hz after adjusting the power supply and the bias voltage with resulting output power -13.5dBm at 5GHz. And the settling time is closely 20us with one of the division control bit connected to the function generator.

4.2 Future works

In spite of a frequency synthesizer applied to 802.11a has already been successfully fabricated, there are still some space left for improvement. Scaling the chip size down and efficiently suppress the power dissipation are good aspects since which can be clearly told from the layout shown before that some space is wasted by some overlong control signal paths and dummy. Furthermore, we can try to lower down the supply voltage to 1V and modified the circuit architecture to reduce power consumption. So a more compact chip with lower power dissipation can be expected.

Besides that, the pulse-swallow counter we adopted in this design actually existing some problems while putting into practice. Time delay consideration and clock control which easily vary as seen while during simulation determine whether the counter derives the right compared signal or not. Consequently finding new substitute architectures or taking every possible problem into consideration will enhance the possibility for a circuit to functions well.

Ultra wide-band systems have recently received a great deal of interest due to their potential for high-speed wireless communication. Not only offers a promising solution to the RF spectrum drought by allowing new services to coexist with current radio systems with minimal or no interference, but also brings the advantage of avoiding the expensive spectrum licensing fees that providers of all other radio services must pay. In IEEE 802.15.3a, multi-band orthogonal frequency division multiplexing (MB-OFDM) with fast frequency hopping is proposed as a means of high bit-rate wireless communication in the UWB spectrum.

As the result, a proper transceiver design that applied to UWB system will be one of the main streams in the future. Although some articles mentioned that they are almost getting this job done, make it more complete and even better are still moving forward and needs great devotion. How to map out a well-performance frequency synthesizer that can carry out stable oscillating frequency varying from the lowest band group 3.1GHz to the highest one 10.6GHz and come to the specifications required by the system is our next objective.

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Chapter 5 Appendix

Highly Integrated Quad-Bands ΣΔ Fractional-N Frequency Synthesizer

As modern GSM cell phones become more and more popular, the critical factors in their manufacture become cost, size, and time to the market [24]. Another important integration is the wireless local area network (WLAN) used most in data communications. Although system integration is a trend nowadays, and the high integration of radio ICs also reduces board area and complexity while cutting component cost and system design time, there are still a lot of discrepancies between these two different communication systems such as channel bandwidth, data rates, and central frequency, etc. thus make it difficult for the applications come to the market. In this chapter we will discuss and design a quad-bands frequency synthesizer that can fit to the system specification of 802.11a/b/g, DCS 1800, and GSM 900 by frequency division switching and fractional-N ΣΔ modulation methods. Down below in Tab. 5-1 shows the specifications for WLAN, DCS 1800, and GSM 900 standards.

Tab. 5-1 System Specifications

	IEEE 80211a	**IEEE 802.11 b/g**	**DCS 1800**	**GSM 900**
RF Frequency	5.15~5.35 GHz	2.4~2.483 GHz	1710~1880 MHz	890~960 MHz
Channel Bandwidth	20MHz	20MHz	200KHz	200KHz
Phase Noise	-110 @1MHz	-110 @1MHz	-116 @600KHz	-121 @600KHz
Locking Time	< 200μs	< 200μs	N/A	N/A

5.1 Traditional Architecture

Integration between different systems has already draw lots of intension recently. There are two ways to realize a multi-bands circuit: frequency doubling/dividing and dual VCOs. We will discuss separately in the next sections.

5.1.1 Dual VCOs frequency synthesizer

There are many ways to reach the goal of multi-bands frequency synthesizer, and one of them is by adopting dual voltage controlled oscillators as shown in Fig. 5-1 [25]. In this design, since two oscillators operate at different oscillating frequency are placed in the circuit to make it multi-bands, the whole chip size will consequently enlarged due to inductors' great dimension. Therefore, under the consideration of economic cost, this topology will be the last choice among our design forethought in spite of their great power due to directly output from oscillators. In Tab. 5-2 are the performance of the circuit.

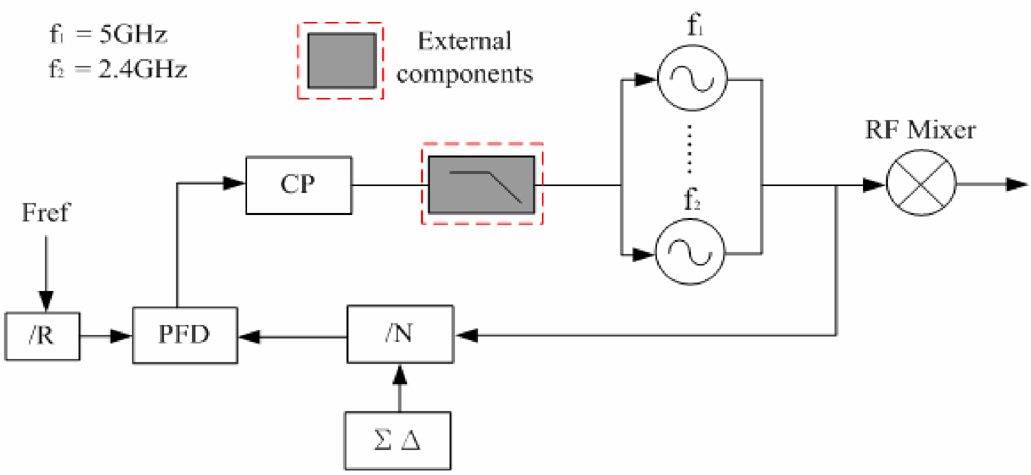


Fig. 5-1 Architecture of a multi-bands frequency synthesizer

Tab. 5-2 Summary of synthesizer performance

Specification	Performance
High VCO tuning range	4.93GHz~5.35GHz
Med VCO tuning range	4.47GHz~4.91GHz
Low VCO tuning range	3.52GHz~3.87GHz
VCO phase noise	-120dBc/Hz @ 1MHz
In band phase noise	-93dBc/Hz
Loop corner frequency	150KHz
Reference frequency	40MHz
Channel resolution	1MHz
Reference spurs	-56dBc
Power supply	2.75V
Current consumption	84mA

5.1.2 Multi-bands frequency synthesizer by doubling/dividing

As shown in Fig. 5-2 are the circuit blocks of a frequency synthesizer that reach the goal of multi-bands switching by adopting a divide-by-3 divider and a multiply-by-2 multiplier. The voltage controlled oscillator is designed to oscillate during the frequency range 1245MHz to 1650MHz. After passing through a buffer, the oscillating signal will divide by three, thus produce a frequency f_1 between 451MHz to 550MHz. Finally a multiplier makes it possible to realize a triple-bands frequency synthesizer by double the output signal from the divider. The circuit performances are summarized in Tab. 5-3.

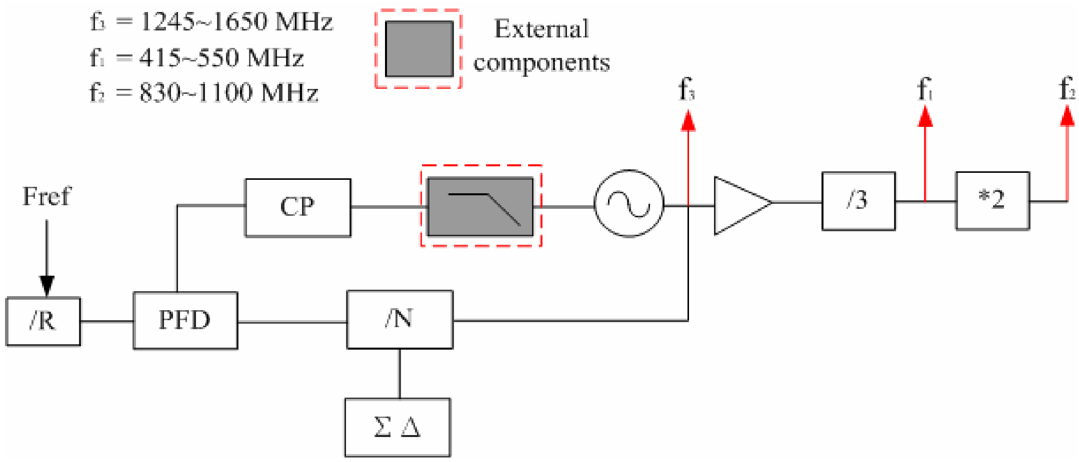


Fig. 5-2 Triple-bands frequency synthesizer

Tab. 5-3 Synthesizer summary

Specification	**Performance**
Tuning range	1250MHz~1650MHz
Resolution	3Hz
Settling time	175μs
Phase noise @ 100KHz	-106dBc/Hz
Phase noise @ 400KHz	-124dBc/Hz
Phase noise @ 3MHz	-141dBc/Hz
Bias current	28mA

5.2 System Adjustment

We will discuss adjustments needed while integrating those discrepancies between each system, by this way, it will be more distinct to make the design complete.

5.2.1 Frequency bands consideration

The most difficult in combing different systems is to adjust frequency bands, phase noise, and channel bandwidths between each other. As we can tell from Tab. 5-1, those dissimilar frequency bands vary from 890 MHz to 5.35GHz, in order to output those frequencies by a structure that is as simple as possible, dividers will be adopted to modulate the oscillating frequency. We will take the highest frequency as the reference target and outputted directly from the oscillator, then the signal will pass through a 50%-duty-cycle divide-by-2 circuit to obtain the 802.11b/g signal. Similarly, the DCS 1800 signal will come from a 50%-duty-cycle divide-by-3 circuit while the GSM 900 signal is from a divide-by-6 divider. The specification of each system after integration is shown in Tab. 5-4.

Tab. 5-4 System specifications after integrated to 5GHz

	IEEE 80211a	IEEE 802.11 b/g	DCS 1800	GSM 900
RF Frequency	5.15~5.35 GHz	4.8~4.96 GHz	5.13~5.64 GHz	5.34~5.76 GHz
Channel Bandwidth	20MHz	40MHz	600KHz	1200KHz
Phase Noise	-110 @1MHz	-110 @2MHz	-116 @1.8MHz	-121 @3.6MHz
Locking Time	< 200μs	< 200μs	N/A	N/A

5.2.2 Frequency switching consideration

Although we know how to obtain different signals by only a single oscillating frequency, switch back to each desired system is the prior concern. As we can tell from the data shown in last section, the operating frequency varies from the lowest 4.8GHz to the highest 5.76GHz, and if we make the voltage controlled oscillator to accomplish that without aids, it will end up a 20% frequency tuning range and thus make the system easily unstable. Consequently, we design three pairs of varactors in order to cover the required carrier frequency range even under the worst–case PVT conditions and divide the 1GHz variation into eight sections and Fig. 5-3 shows the simulation results [26]. We will reserve the lowest and the highest tuning ranges in case of frequency deviation and allot each bank code to the corresponding system applications as detailed in Tab. 5-5.

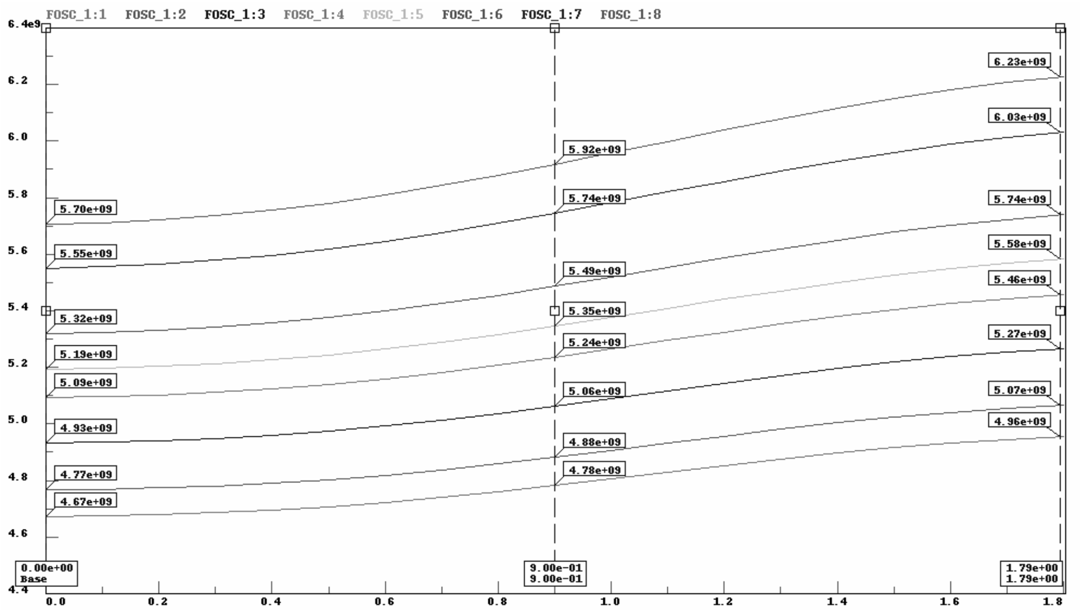


Fig. 5-3 Simulation results of a VCO tuning range

Tab. 5-5 Corresponding bank code of different systems

	Integrated frequency	Corresponding bank code
802.11a	5.15~5.35GHz	4
802.11b/g	4.80~4.96GHz	2
DCS 1800	Tx: 5.130~5.355GHz Rx: 5.415~5.640GHz	4,6
GSM 900	Tx: 5.340~5.490GHz Rx: 5.610~5.760GHz	6,7

5.2.3 Phase noise consideration

Not only frequency shifting should we concern while combining different systems, the ability against noise also needs to be well considered. According to the frequency division theory we know that a signal skirt will shrink as long as it passes through an ideal divider. It can be explained down below in Fig. 5-4. As we can see that the 1MHz frequency difference between the desired signal and the measuring point is put off relatively, and the magnitude will also be scaled down about 6dB because of the divide-by-two circuit functioning.

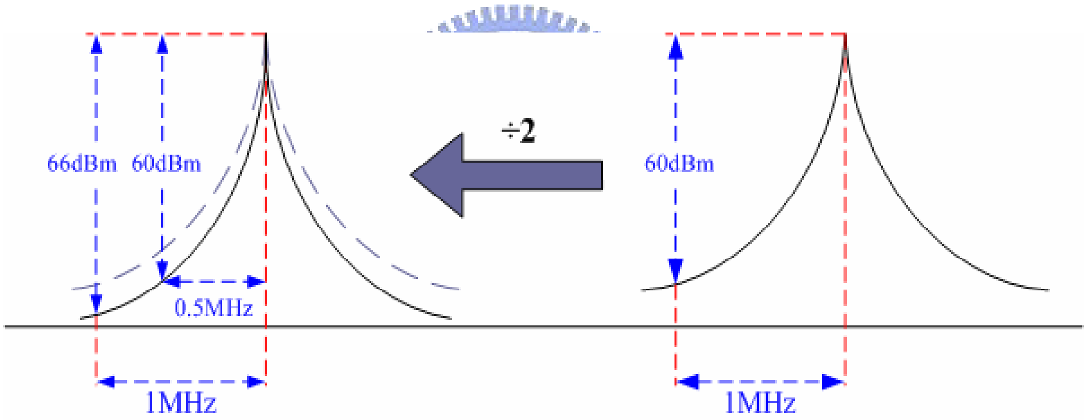


Fig. 5-4 Phase deviation through a divide-by-2 divider

A divide-by-two circuit can effectively improve the performance of phase noise to about 6dB, and respectively, the one divide-by-three can make it 9~10dB. Due to such characteristic of a divider, we can design a voltage controlled oscillator that meets a particular system specification and scaled the output frequency down to fit the next level application with appropriate improvement in phase noise. Fig. 5-5 is the simulation results of the VCO and labeled the value at 1MHz, 1.8MHz, 2MHz, and 3.6MHz separately. The system specifications are also compared with the results as shown in Tab. 5-6.

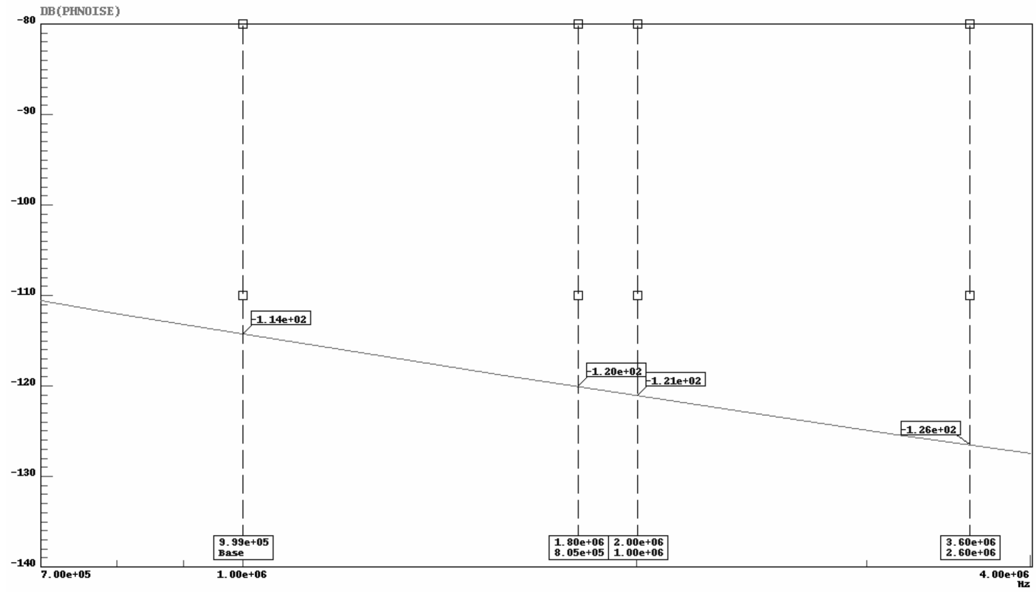


Fig. 5-5 Phase noise at different frequencies

Tab. 5-6 Comparison between system spec. and simulation

	System specification after adjustment	Simulated results
802.11a	-110 @1MHz	-114 @1MHz
802.11b/g	-110 @2MHz	-121 @2MHz
DCS 1800	-116 @1.8MHz	-120 @1.8MHz
GSM 900	-121 @3.6MHz	-126 @3.6MHz

5.3 Topology of a quad-bands frequency synthesizer

As just discussed in several past sections, we know that to build a frequency synthesizer integrating four different communication systems needs only a VCO and some dividers for the purpose of frequency scaling. The architecture shown in Fig. 5-6 is the first conception came to the mind, but soon be found out that some problems exist.

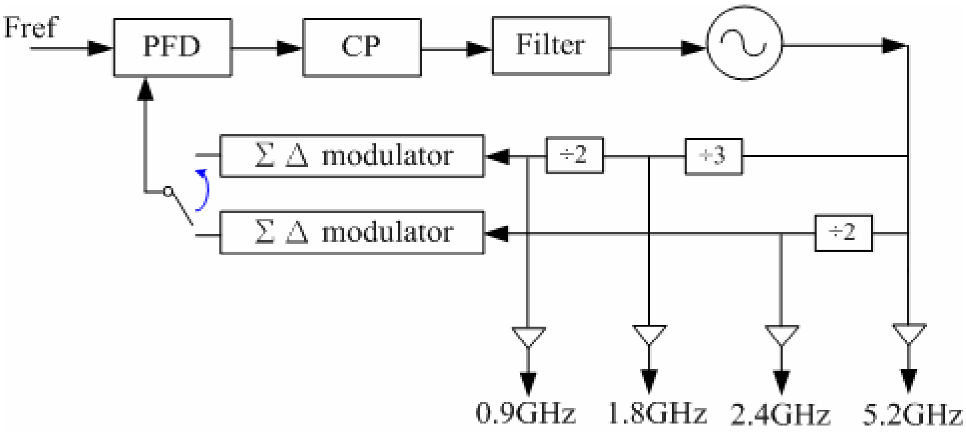


Fig. 5-6 First architecture of a quad-bands frequency synthesizer

We separate 802.11a/b/g and DCS1800/GSM900 into two groups and design ΣΔ modulators for individual path controlled by a switch because of the channel bandwidth discrepancy between these two system groups. But in this structure there exists a loading effect problem: as can be seen above that the divide-by-three circuit not only outputs the 1.8GHz signal through a buffer but also manages to drive the next divider and will thus easily failed. In order to prevent the 50% divide-by-three circuit from breakdown, we have to adjust the signal propagation path and fix the loading problem. The new architecture is as shown in Fig. 5-7 with the reference frequency set to 16MHz for the consideration of spur noise suppression and fast settling time compromise.

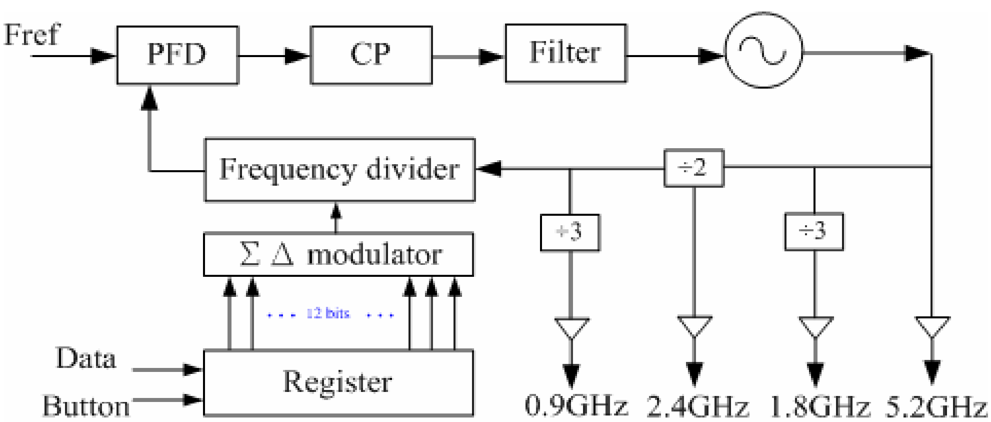


Fig. 5-7 Modified architecture of a quad-bands frequency synthesizer

It is obviously told in this new structure that both divide-by-three circuits are connected merely to the output buffers and can thus effectively release the associated loading effects. Although we know that channel bandwidth between 802.11a/b/g (20MHz) and DCS1800/GSM900 (200 KHz) differs a lot, use a high resolution $\Sigma\Delta$modulator composed of twelve-bit accumulator can fix the divergence.

5.4 Divide-by-three circuit

There are some problems arise from the implementation of a divide-by-three circuit. The foremost among these is the fact that the output signals are typically rich in even-order harmonics in a traditional odd-order frequency divider, since these harmonic contents result from outputs taking the form of rectilinear waveforms with non 50%duty cycles [27]. Since the output waveforms of a general frequency divider are derived only from the rising or falling edges of its input, odd order divider outputs are typically restricted to pulse widths that are integer multiples of the period of their inputs. In order to overcome problems mentioned above, a true 50% duty cycle frequency divide-by-three using three phase-switchable level-sensitive latch connected in a loop is indeed has to be implemented.

The basic phase switchable ECL D flip flop with three input signals D, CLK, and Θ which is able to set the polarity of the CLK signal that triggers the circuit is shown explicitly in Fig. 5-8. By dynamically driving the Θ inputs of the flip flops, the outputs can be made to transition on either a rising or falling edge, depending on the state of other flip flops in the circuit. Each flip flop's output drives the next one's input, with the inversion in the feedback. The truth table of a polarity switchable flip flop is list in Tab. 5-7, and the block of a cascaded 3-stage divide-by-three circuit is also shown in Fig. 5-9 .

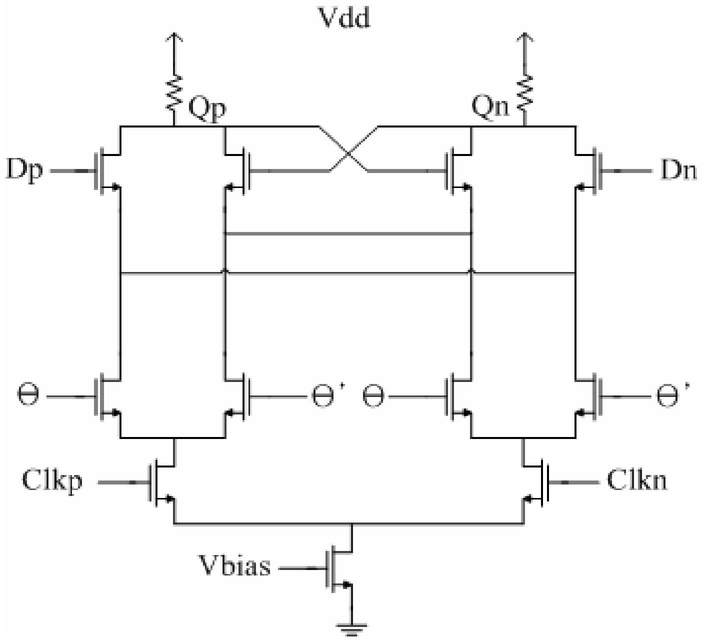


Fig. 5-8 Externally triggering controlled ECL D flip flop

Tab. 5-7 Truth table of the externally controllable DFF

Dp	0	0	0	0	1	1	1	1
Θ	0	0	1	1	0	0	1	1
Clkp	0	1	0	1	0	1	0	1
Qn	0	Hold	Hold	0	1	Hold	Hold	1

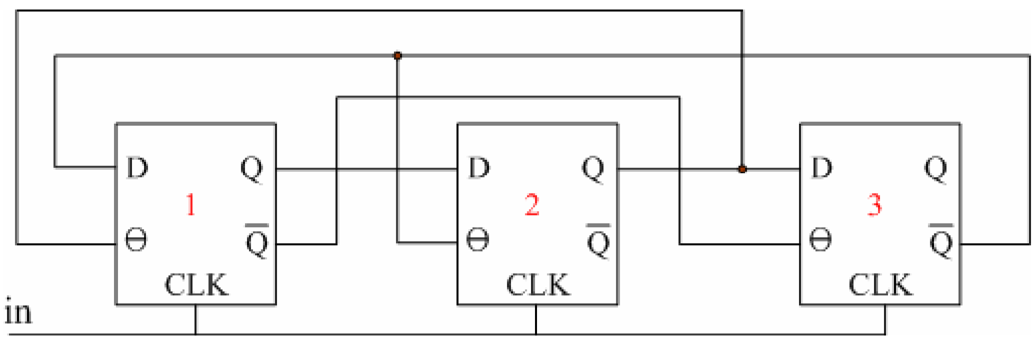


Fig. 5-9 Architecture of a divide-by-three circuit with 50% duty cycle

Fig. 5-10 shows the simulation results of a 50% duty cycle divide-by-three circuit with which input signals directly supplied by a 5.2GHz VCO. By the kind of circuit, the system expectation of DCS-1800 and GSM-900 can thus be attained and effectively suppress the even-order harmonic at the meanwhile.

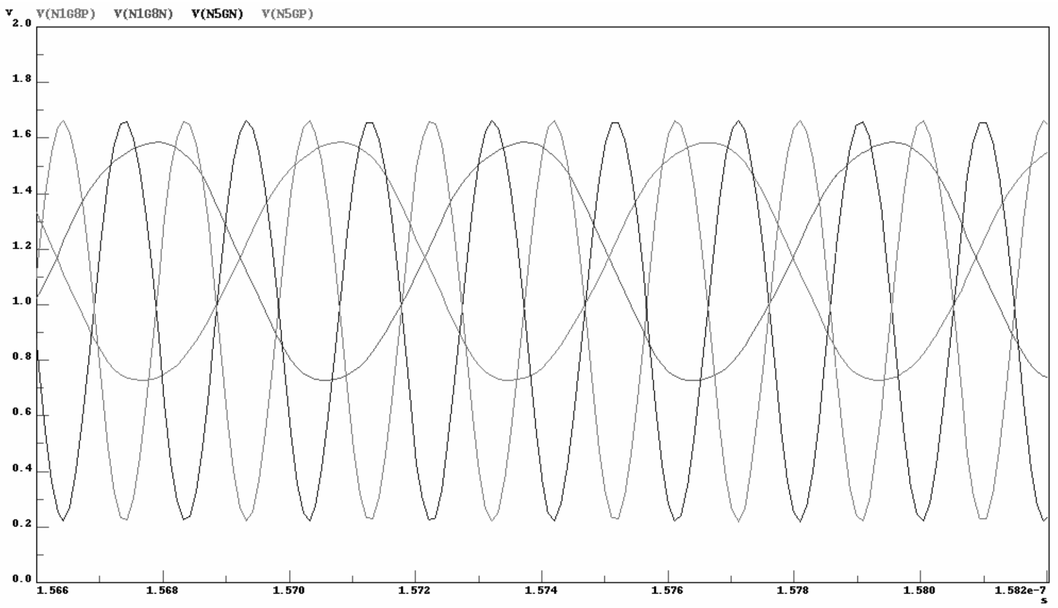


Fig. 5-10 Simulation results of a divide 3 circuit

5.5 Sigma-delta modulator

In order to speed up the settling time of a frequency synthesizer, different methods have been adopted including change the dividing architecture. In the past two chapters, we made the total divide number integral and thus cause the settling time more than 50μs while a divide by fractional ratios structure will supersede and improve the problem [28].

The basic concept of a fractional division is to make the counting clock switch between dividing N and N+1, as can be explained in Fig. 5-11. A digital input $K = n \cdot 2^K$ is applied to the accumulator with $n \in R[0,1]$ and the carry output is produced every K cycles of the reference frequency f_{ref}, which is also the sampling frequency of the digital accumulator. As the result, the dual-modulus frequency divider divides N+1 for K times and N for $2^K - K$ times thus make the total divisor N+n which derived in Eq. (5-1).

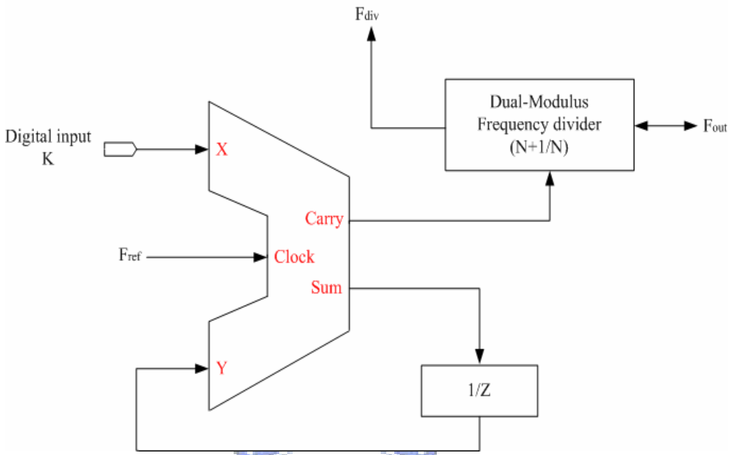


Fig. 5-11 Basic blocks of a fractional divisor structure

$$N_{total} = \frac{K \cdot (N+1) + (2^K - K) \cdot N}{2^K} = N + \frac{K}{2^K} = N + n \quad (5\text{-}1)$$

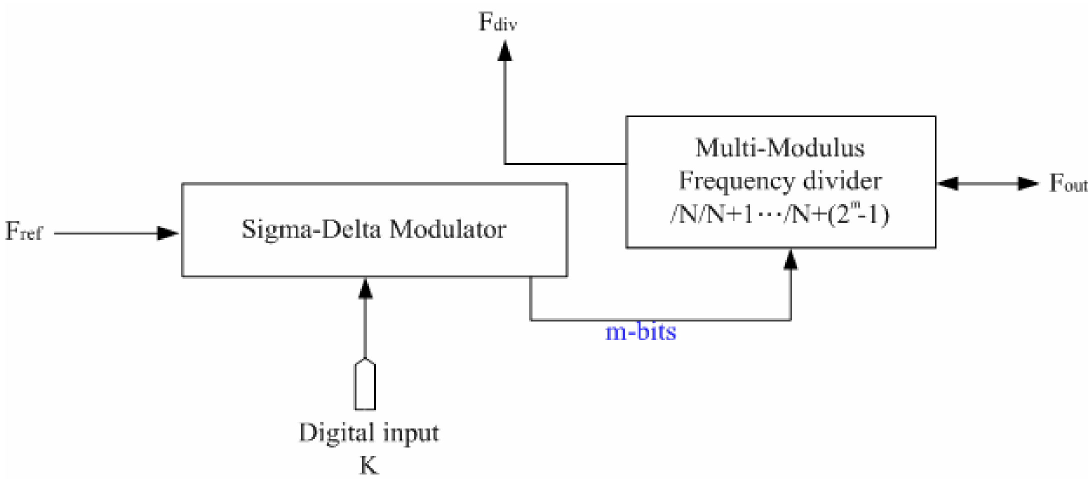


Fig. 5-12 Fractional divisor structure using sigma-delta modulator

However, a periodical characteristic of the overflow signal under this architecture will lead to more serious spurious noise in the frequency synthesizer. To fix the problem a sigma-delta modulator as shown in Fig. 5-12 above must be put to use. The basic concept of a sigma-delta modulator is shifting the quantization noise power to higher frequency first by an integrator and a differentiator at last as explained in Fig. 5-13. Thus the spurious problem due to periodical overflow-signal will be greatly reduced.

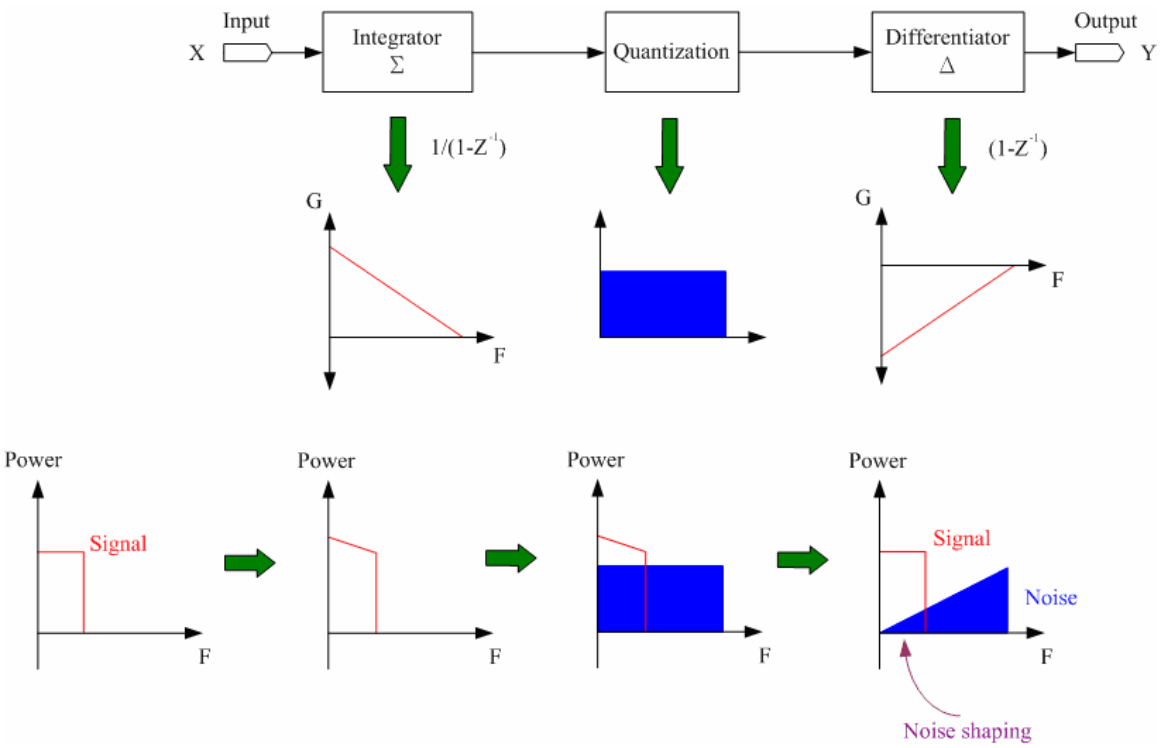


Fig. 5-13 Noise shaping of a sigma-delta modulator

The equation between X and Y can be derived by simple feedback loop analysis and end in $Y = X + q_a \cdot (1 - Z^{-1})$. By this architecture we can suppress the noise level at lower frequency and still maintain the signal power density. In the next section we will introduce the first-order and the third-order, two types of sigma-delta modulator, and compares with each other at last.

5.5.1 First-order Σ-Δ Modulator

The basic blocks of the first-order Σ-Δ modulator is shown in Fig. 5-14 and it works just as an accumulator with the transfer function $N[z] = .f[z] + (1 - z^{-1}) \cdot q_a[z] = .f[z] + q_e[z]$. It can be easily told that the quantization noise $q_a[z]$ is filtered by a high pass filter and turns into $q_e[z]$.

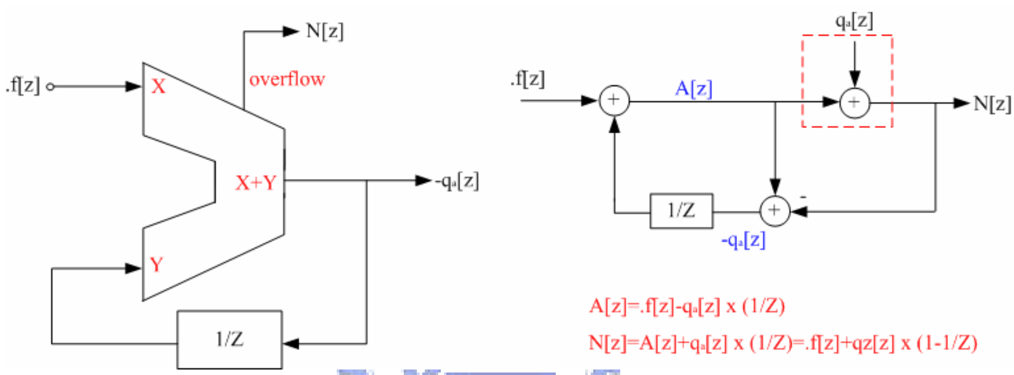


Fig. 5-14 First order sigma-delta modulator

The transfer function of noise is:

$$H_{noise}(f) = 1 - z^{-1}$$

$$H_{noise}(f) = \left| 1 - \exp(-\frac{j2\pi f}{f_{ref}}) \right|$$

$$H_{noise}(f) = \left| 1 - \cos(\frac{j2\pi f}{f_{ref}}) - j \cdot \sin(\frac{j2\pi f}{f_{ref}}) \right|$$

$$H_{noise}(f) = \left| 2 \cdot \sin(\frac{\pi f}{f_{ref}}) \right| \tag{5-2}$$

Now we will define the normalized frequency error: as we know that the ideal output of a divider is:

$$f_{div} = f_{out} = \frac{f_{out}}{N + .f} = \frac{f_{out}}{N + \frac{K}{2^M}} \tag{5-3}$$

However, if the quantization error is taken into consideration, the real output will turns into:

$$f_e(t) = \frac{f_{out}}{N + \frac{K}{2^M} + q_e(t)} = \frac{f_{out}}{N' + q_e(t)} \quad \text{while} \quad N' = N + \frac{K}{2^M} \tag{5-4}$$

Thus the normalized frequency error is:

$$f_{diff} = \frac{f_{div} - f_e(t)}{f_{div}} = 1 - \frac{1}{1 + \frac{q_e(t)}{N'}} \cong \frac{q_e(t)}{N'} \tag{5-5}$$

The phase error is defined:

$$\theta_e(t) \equiv 2\pi \cdot \int \left(f_{div} - f_e(t) \right) dt = 2\pi \cdot f_{div} \cdot \int f_{diff}(t) dt = 2\pi \cdot \frac{f_{ref}}{N'} \cdot \int q_e(t) dt \tag{5-6}$$

$$\theta_e'(t) = 2\pi \cdot \frac{f_{ref} \cdot q_e(t)}{N'} \tag{5-7}$$

Therefore the relation of power spectrum density (PSD) between phase error and quantization error is:

$$\begin{aligned} S_{\theta_e}(f) &= \frac{1}{(2\pi f)^2} \cdot S_{\theta_e'}(f) \\ &= \left(\frac{2\pi f_{ref}}{2\pi f \cdot N'} \right)^2 \cdot S_{q_e}(f) \\ &= \left(\frac{f_{ref}}{f \cdot N'} \right)^2 \cdot S_{q_e}(f) \end{aligned} \tag{5-8}$$

As the result, the phase noise power spectrum density can be obtained by combining the Eq.(5-2) and Eq.(5-8):

$$S_{q_e}(f)=S_{q_{ae}}(f)\cdot H_{noise}{}^{2}(f)$$
$$=\frac{1}{12\cdot f_{ref}}\cdot 4\sin^{2}(\frac{\pi f}{f_{ref}})$$
$$=\frac{1}{3\cdot f_{ref}}\cdot \sin^{2}(\frac{\pi f}{f_{ref}})$$
$$S_{\theta_e}=\left(\frac{f_{ref}}{f\cdot N'}\right)^{2}\cdot\frac{1}{3\cdot f_{ref}}\cdot\sin^{2}(\frac{\pi f}{f_{ref}}) \qquad (5\text{-}9)$$

The PSD of $S_{\theta e}$ is flat and thus cannot suppress the spurious noise effectively as can be easily figured out in Fig. 5-15 and

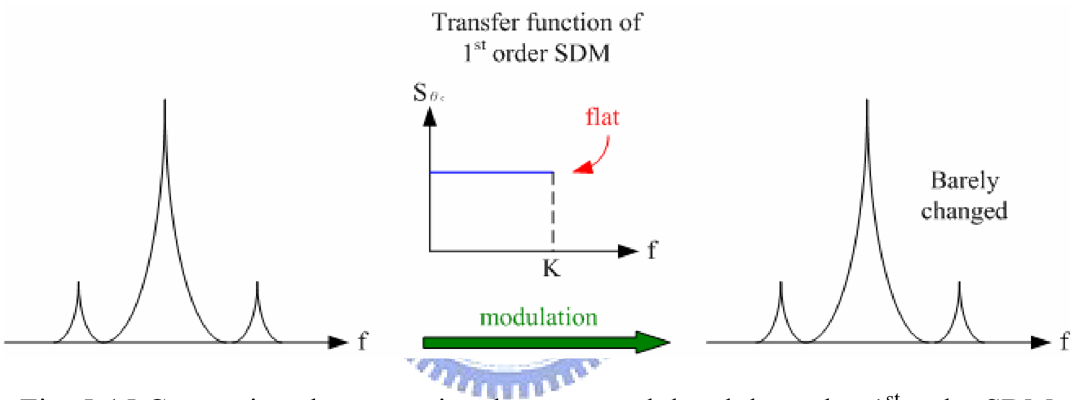


Fig. 5-15 Comparison between signal power modulated through a 1st order SDM

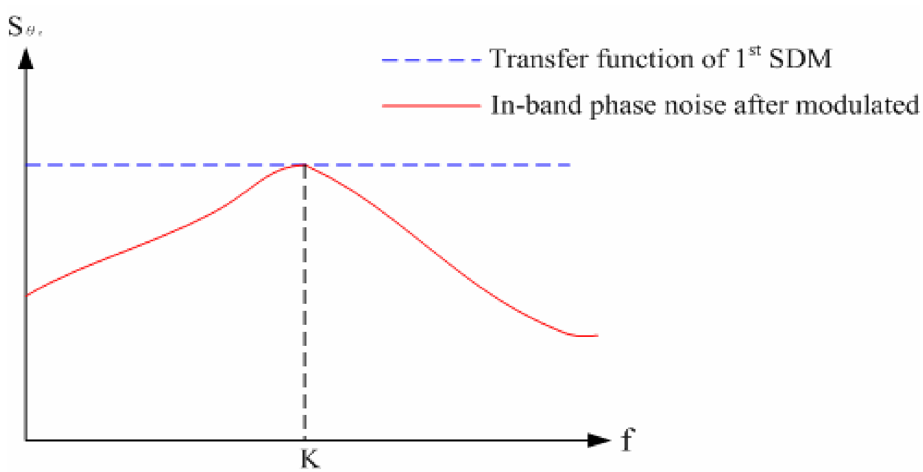


Fig. 5-16 In-band phase noise after modulated

Since a first-order sigma-delta modulator dose not make it to transfer phase noise to high frequency effectively, a higher order one must be adopted for improving the in band noise shaping. Next we will introduce a 3rd order SDM.

5.5.2 Third-order Σ-Δ Modulator

The architecture of a third-order sigma-delta modulator is as shown in Fig. 5-17 which is composed of a three-stage cascaded accumulator with a transfer function (5-10) alike to the first-order SDM but only differs in order. Fig. 5-18 also shows blocks of the transfer function.

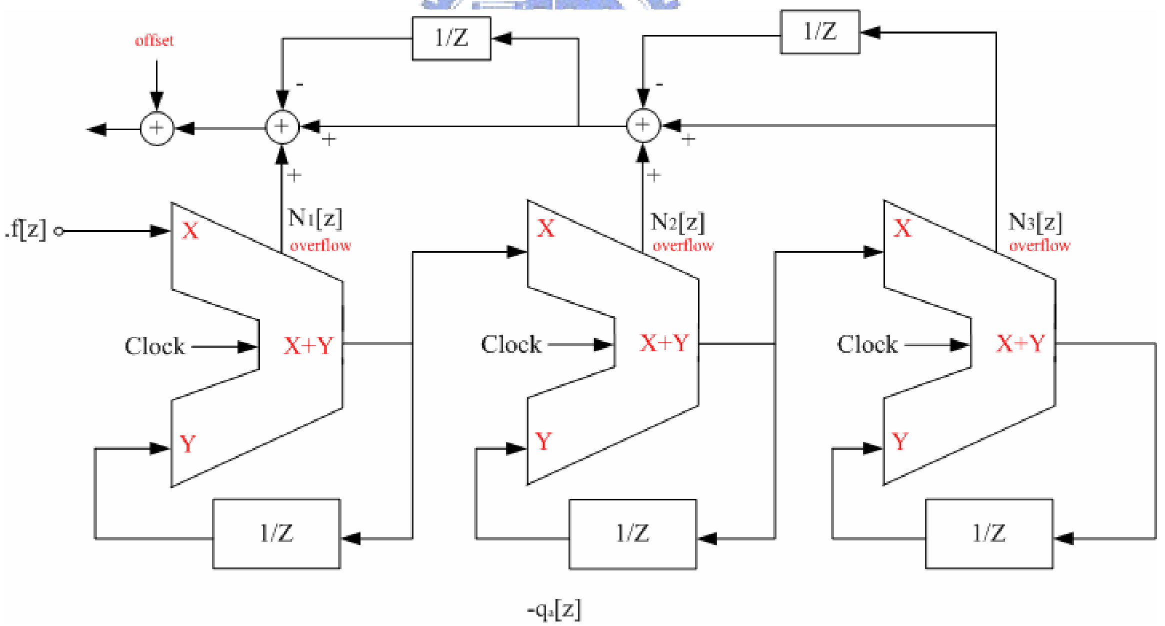


Fig. 5-17 Third order sigma-delta modulator

$$N[z] = .f[z] + (1 - z^{-1})^3 \cdot q_a[z] \tag{5-10}$$

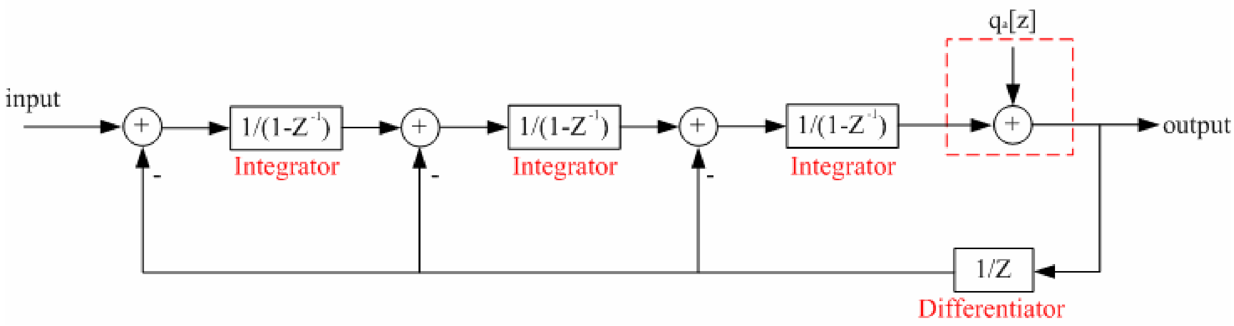


Fig. 5-18 Basic transfer function blocks of a 3rd order sigma-delta modulator

The quantization noise turns into $q_e[z] = (1 - z^{-1})^3 \cdot q_a[z]$ and thus the noise transfer function is:

$$H_{noise}(f) = (1 - z^{-1})^3$$

$$H_{noise}(f) = \left|1 - \exp(-\frac{j2\pi f}{f_{ref}})\right|^3$$

$$H_{noise}(f) = \left|1 - \cos(\frac{j2\pi f}{f_{ref}}) - j \cdot \sin(\frac{j2\pi f}{f_{ref}})\right|^3$$

$$H_{noise}(f) = \left|2 \cdot \sin(\frac{\pi f}{f_{ref}})\right|^3 \qquad (5\text{-}11)$$

Assume the ideal power spectral density of quantization error $S_{e_q}(f) = \frac{1}{12 \cdot f_{ref}}$ with step δ=1, thus the PSD of phase error can be derive as shown in Eq.(5-12):

$$S_{q_e}(f) = S_{q_{ae}}(f) \cdot H_{noise}{}^2(f)$$
$$= \frac{1}{12 \cdot f_{ref}} \cdot 64 \sin^6(\frac{\pi f}{f_{ref}})$$
$$= \frac{16}{3 \cdot f_{ref}} \cdot \sin^6(\frac{\pi f}{f_{ref}})$$

$$S_{\theta_e} = \left(\frac{f_{ref}}{f \cdot N'}\right)^2 \cdot \frac{16}{3 \cdot f_{ref}} \cdot \sin^6(\frac{\pi f}{f_{ref}}) = \frac{16 \cdot f_{ref}}{3 \cdot (f \cdot N')^2} \cdot \sin^6(\frac{\pi f}{f_{ref}}) \qquad (5\text{-}12)$$

As we can see from the derivation above, the in band transfer function $S_{\theta e}$ is proportional to 4^{th} order of frequency f and therefore can hold back the spurious noise. It is graphed thoroughly in both Fig. 5-19 and Fig. 5-20.

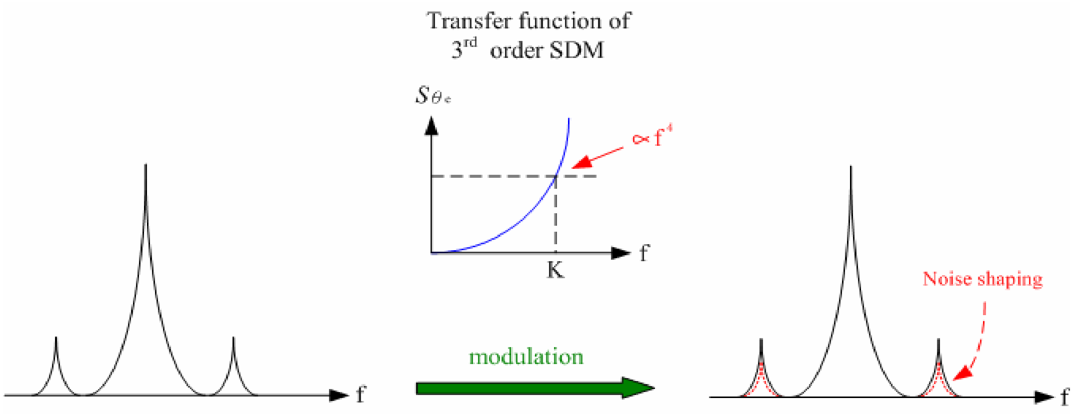


Fig. 5-19 Comparison between signal power modulated through a 3rd order SDM

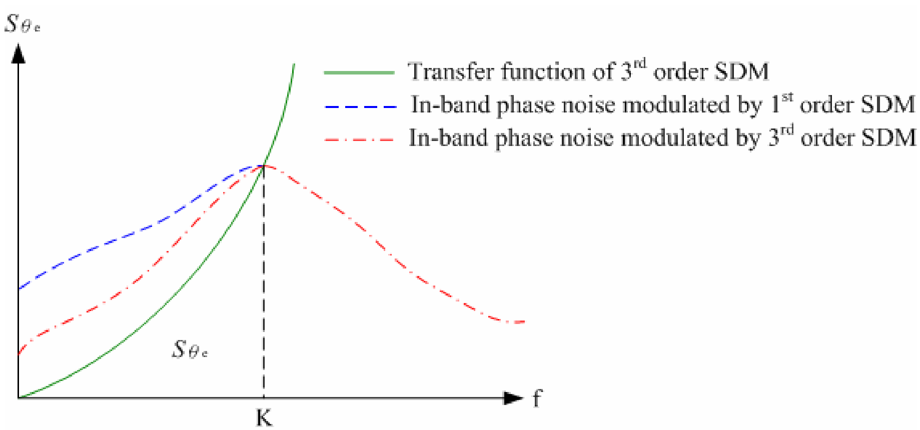


Fig. 5-20 In-band phase noise after modulated

Due to great ability at suppressing the noise, the 3rd order sigma-delta modulator will be adopted in this design and the bit of accumulator will decided depending on each system's specifications.

5.6 Simulation results

5.6.1 5.18GHz Simulation results

The output voltage swing of a 5.18GHz VCO is shown in Fig. 5-21 while the peak-to-peak amplitude is about 500mV. The output power spectrum is also shown in Fig. 5-22 as can be told that the maximum delivering power is -12.4dBm. In Fig. 5-23 is the settling time which is 30μs although the circuit nearly enters the steady state at 15μs.

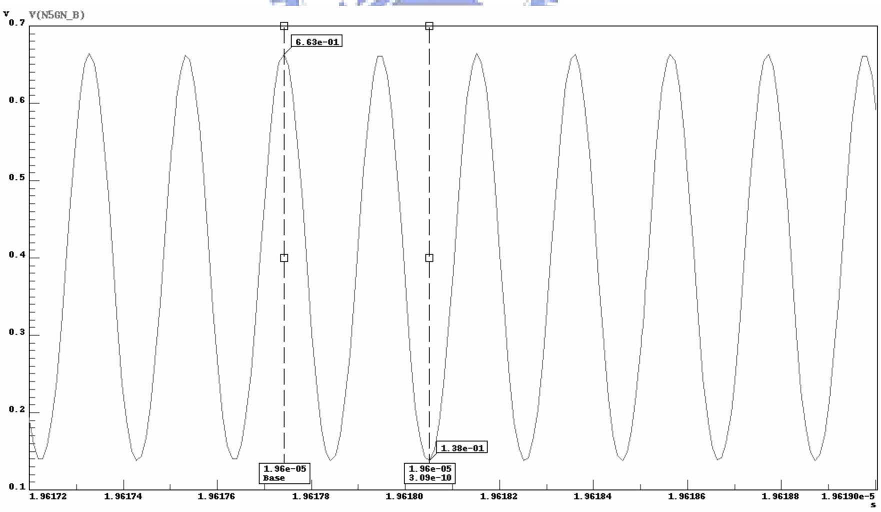


Fig. 5-21 Output voltage swing of the VCO

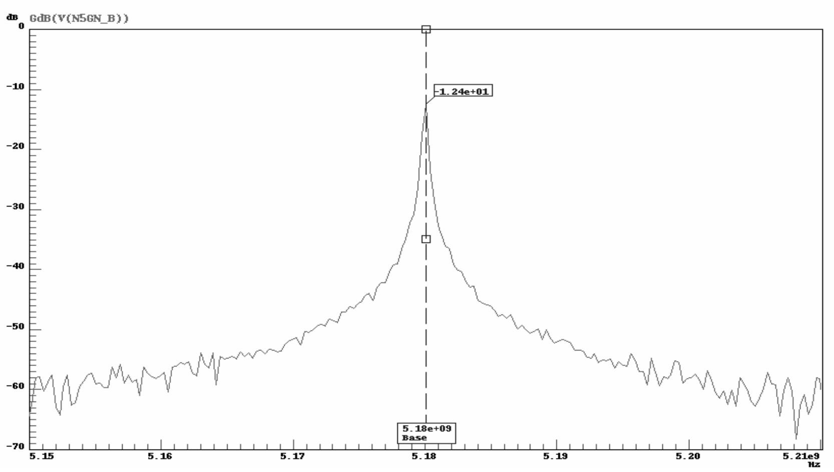


Fig. 5-22 Output Power spectrum of a 5.18GHz signal

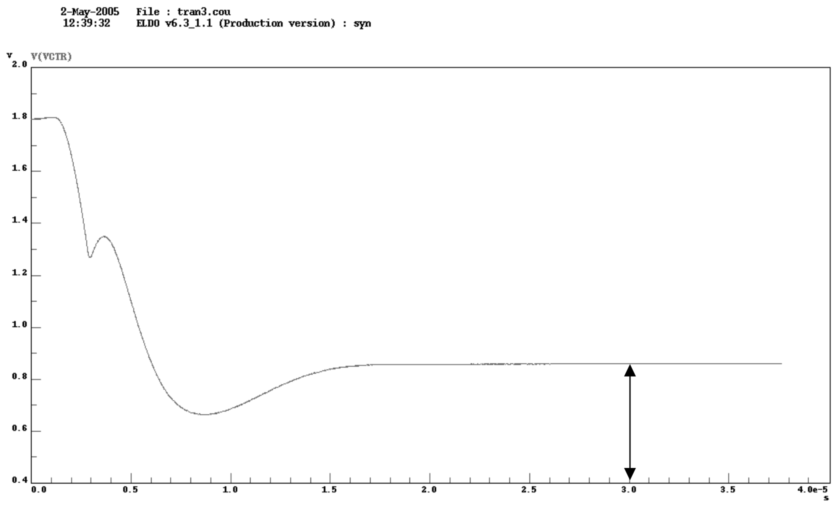


Fig. 5-23 Settling time of a 5.18GHz output

5.6.2 2.40GHz Simulation results

The output voltage swing of a 2.4GHz VCO is shown in Fig. 5-24 while the peak-to -peak amplitude is about 230mV. The output power spectrum is also shown in Fig. 5-25 as can be told that the maximum delivering power is -18.9dBm. In Fig. 5-26 is the settling time which is 30μs although the circuit nearly enters the steady state at 15μs.

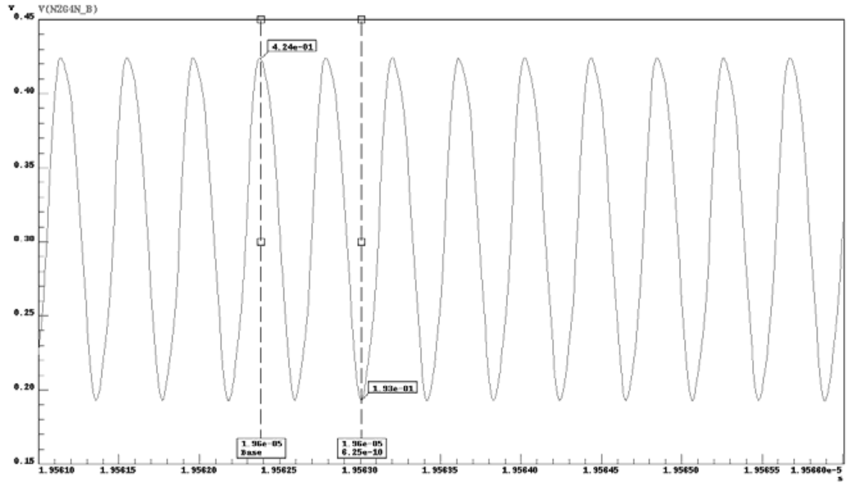


Fig. 5-24 Output voltage swing of a 2.40GHz signal

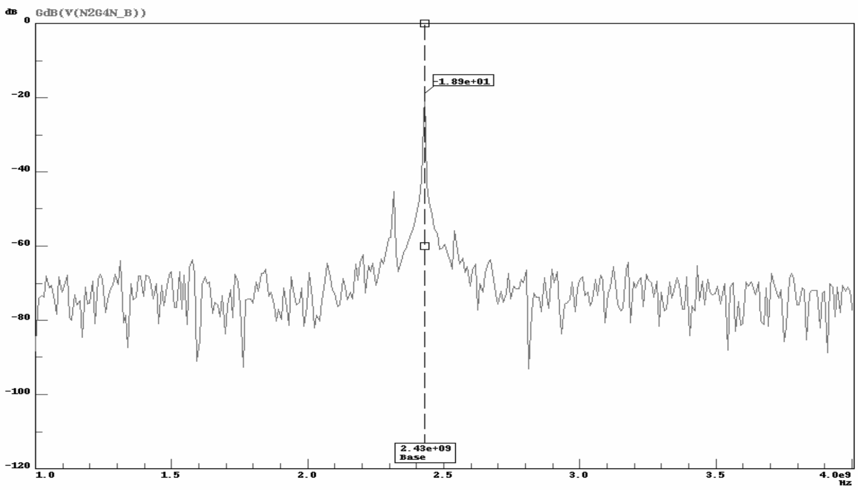


Fig. 5-25 Output Power spectrum of a 2.40GHz signal

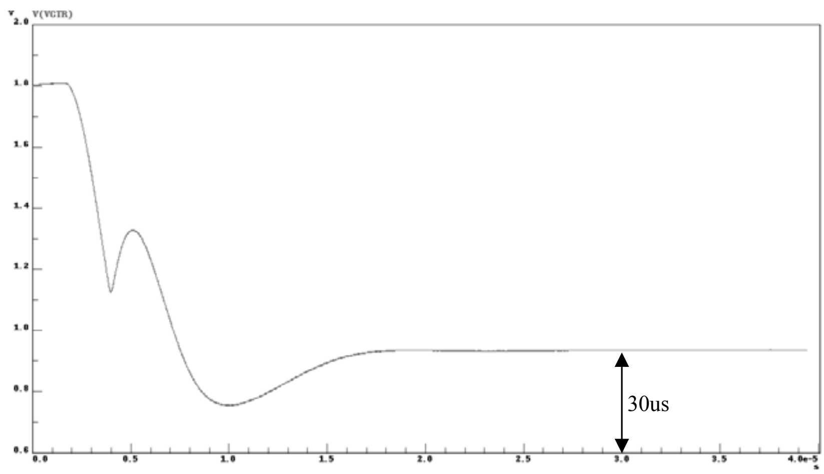


Fig. 5-26 Settling time of a 2.40GHz output

5.6.3 1.726GHz Simulation results

The output voltage swing of a 1.726GHz VCO is shown in Fig. 5-27 while the peak-to -peak amplitude is about 260mV. The output power spectrum is also shown in Fig. 5-28 as can be told that the maximum delivering power is -17.25dBm. In Fig. 5-29 is the settling time which is 30μs although the circuit nearly enters the steady state at 15μs.

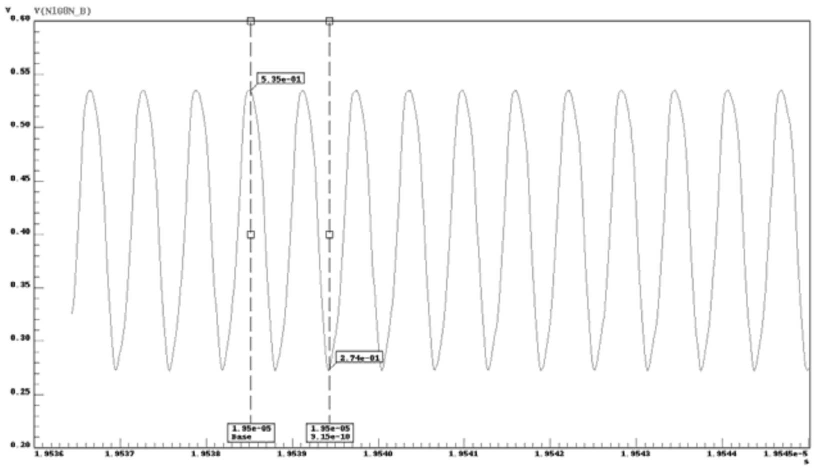


Fig. 5-27 Output voltage swing of a 1.726GHz signal

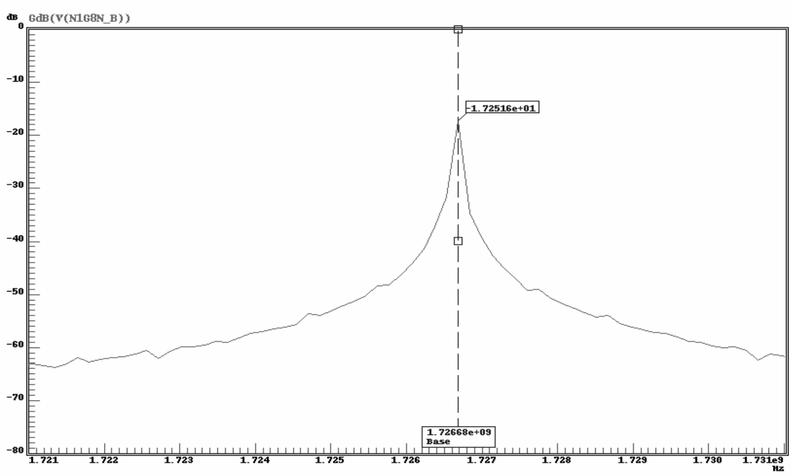


Fig. 5-28 Output Power spectrum of a 1.726GHz signal

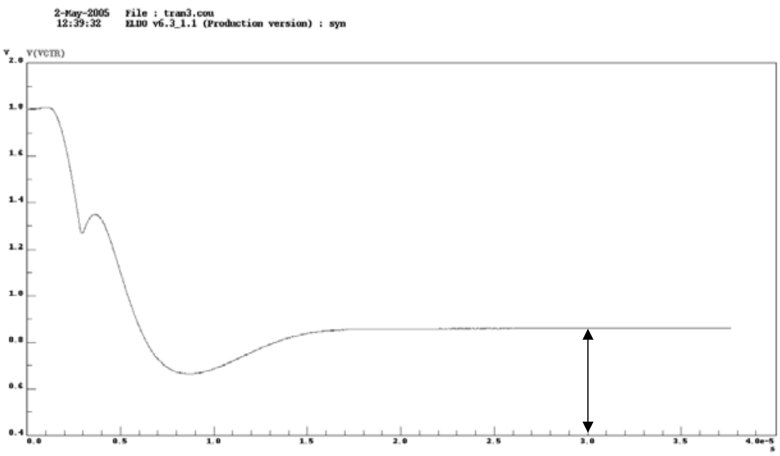


Fig. 5-29 Settling time of a 1.726GHz output

5.6.4 900MHz Simulation results

The output voltage swing of a 900MHz VCO is shown in Fig. 5-30 while the peak-to -peak amplitude is about 160mV. The output power spectrum is also shown in Fig. 5-31as can be told that the maximum delivering power is -22.3dBm. In Fig. 5-32 is the settling time which is 30μs although the circuit nearly enters the steady state at 15μs.

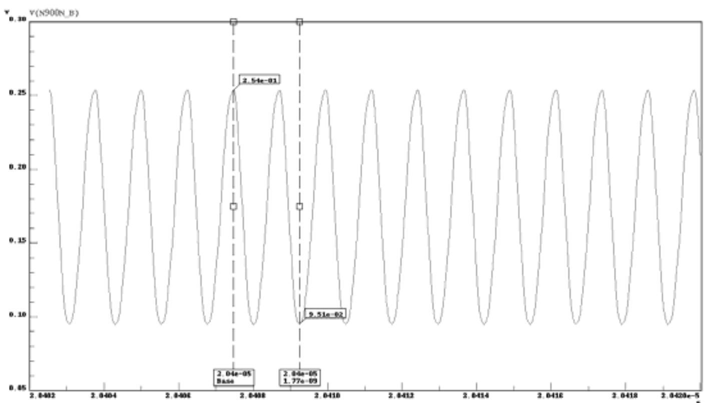


Fig. 5-30 Output voltage swing of a 900MHz signal

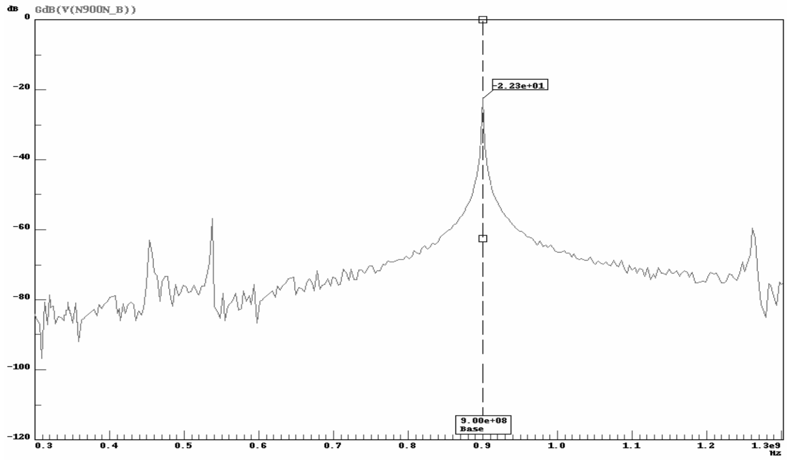


Fig. 5-31 Output Power spectrum of a 900MHz signal

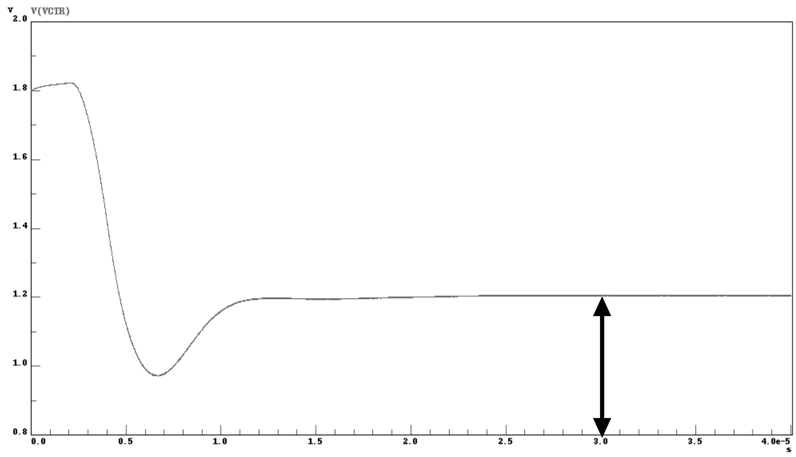


Fig. 5-32 Settling time of a 900MHz output

5.6.5 Simulation results and layout

Down below in Tab. 5-8 displayed the total simulation results and the chip layout in Fig. 5-33 which owns the dimension 1.45x1.114 mm^2 is also shown. Tab. 5-9 is the comparison between simulations and references.

Tab. 5-8 Simulation results summary

	Simulation Results
Fabrication process	TSMC 0.18um CMOS
Supply voltage	1.8V
Synthesizer type	Fractional-N Σ-Δ
Oscillating frequency	5.2GHz
Reference frequency	16MHz
Tuning range	4.67GHz~6.23GHz with 8 different banks
Bits no. of accumulator	12 bits
Phase noise	-114dBc/Hz @ 1MHz for 802.11a -121dBc/Hz @ 2MHz for 802.11/b/g -120dBc/Hz @ 1.8MHz for DCS 1800 -126dBc/Hz @ 3.6MHz for GSM 900
Settling time	30us
Output power	-12.4dBm for 802.11a -18.9dBm for 802.11b/g -17.25dBm for DCS 1800 -22.3dBm for GSM 900

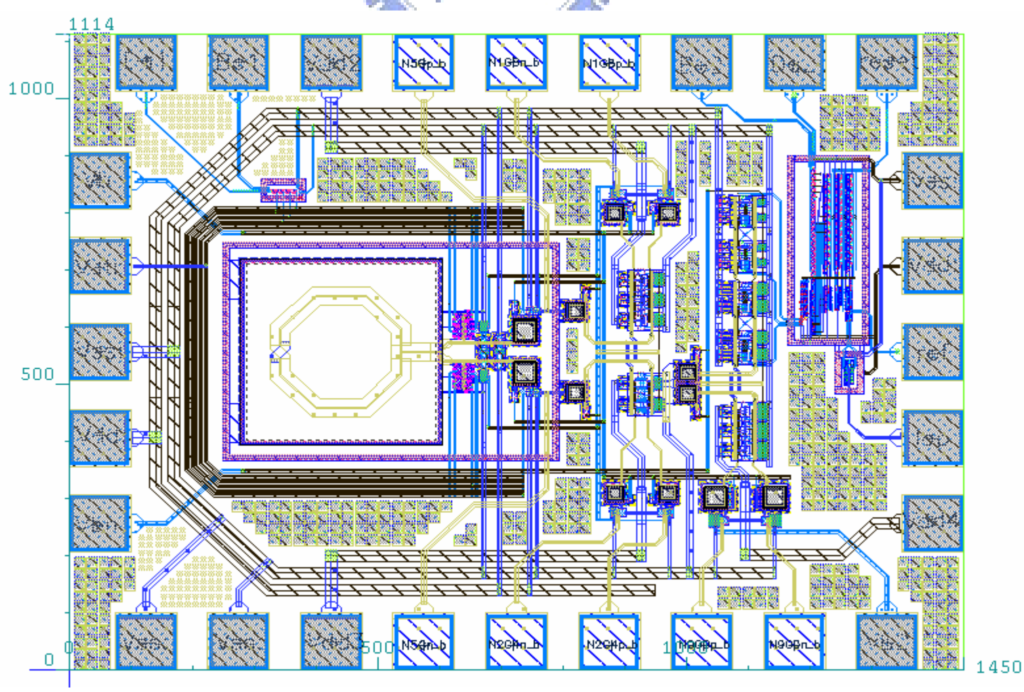


Fig. 5-33 Chip layout of a highly integrated quad-bands synthesizer

Tab. 5-9 Comparison between references and this work

Specification	[This work]	[25] 2003	[29] 2005	[30] 2004
Fabrication	0.18um CMOS	0.5um SiGe	0.5um SiGe	0.35um CMOS
Oscillation frequency	802.11a/b/g DCS/GSM 1800	3.52~3.87GHz 4.47~5.35GHz	2.4GHz 4.9~5.8GHz	1.87~2.3GHz 3.74~4.6GHz
Reference frequency	16MHz	40MHz	40MHz	N/A
Bit no. of accumulator	12	N/A	6	16
Phase noise	-114dBc/Hz @1MHz	-120dBc/Hz @1MHz	-120dBc/Hz @1MHz	-114dBc/Hz @5MHz
Power dissipation	104.4mW	231mW	99mW	80mW
Supply voltage	1.8V	2.75V	2.75V	2V
Chip size	1.615 mm^2	12.4 mm^2	3.22 mm^2	3.52 mm^2

5.7 Measurements

5.7.1 Measurement consideration

Since a frequency synthesizer needs more control signals than any other kind of RF frequency circuits, a well concerned measurement method is necessary. While designing a PCB layout as shown in Fig. 5-34, we must first preserve the bypass paths connected to the power supply lines through capacitors prevent the wanted signal influenced by extra noise. The die photo is also shown in

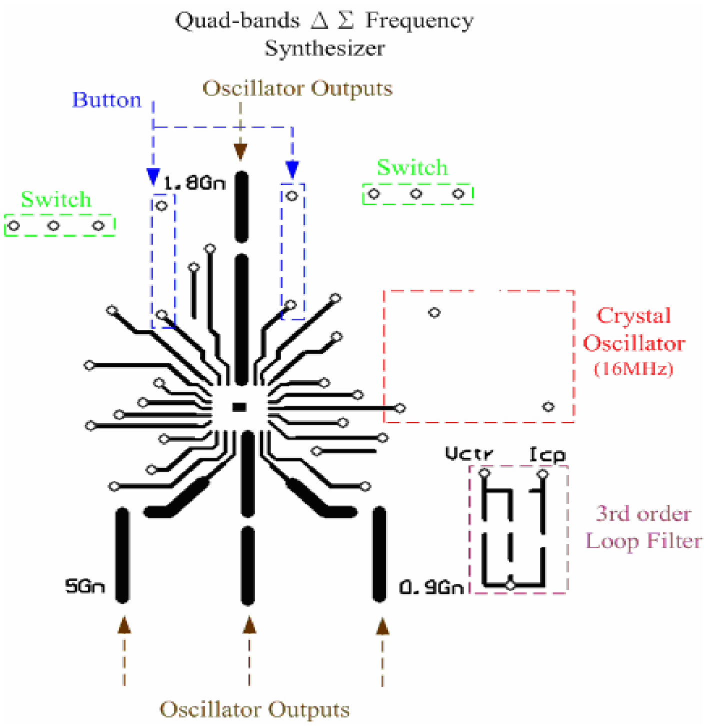


Fig. 5-34 PCB layout of the quad-bands ΔΣ fractional-N frequency synthesizer

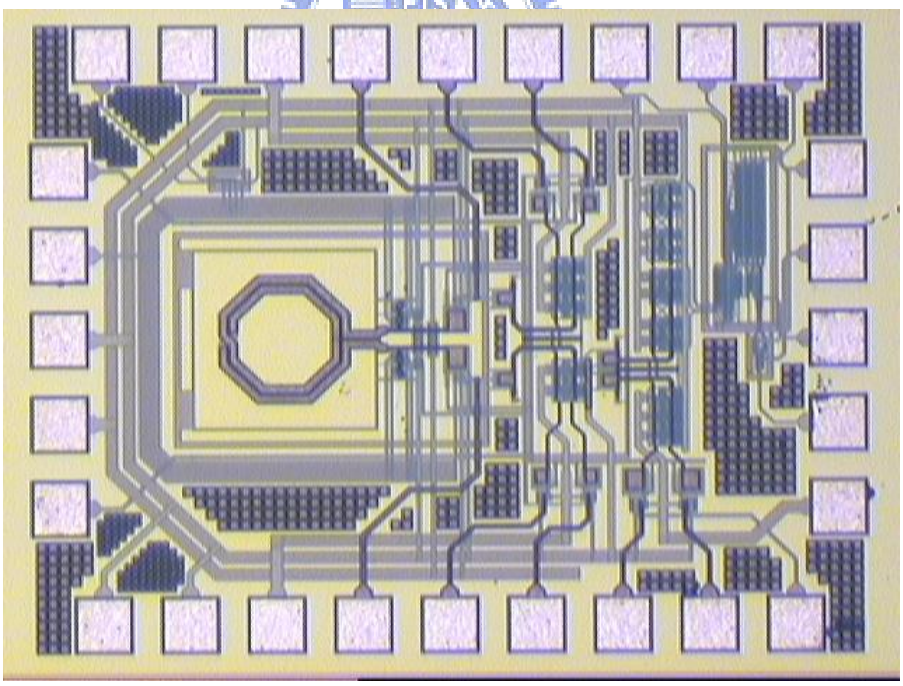
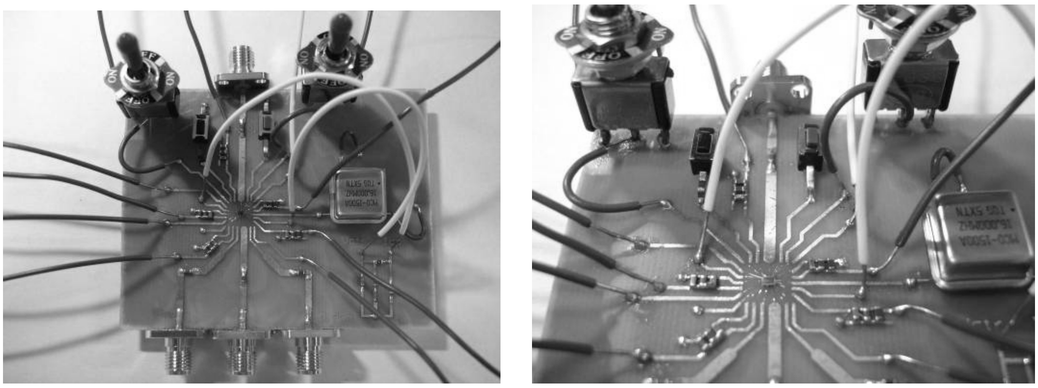


Fig. 5-35 Chip photo of the frequency synthesizer

Besides, the metal lines that connected the output signals to the measuring instruments must be wide enough to meet the purpose of internal resistance 50Ω because of the matching cogitation. The measuring equipments are mentioned in the last chapter and shown in Fig. 3-24(a) ~ (f) and in Fig. 5-36(a) and (b) are practical PCB layout seen aside and above separately.



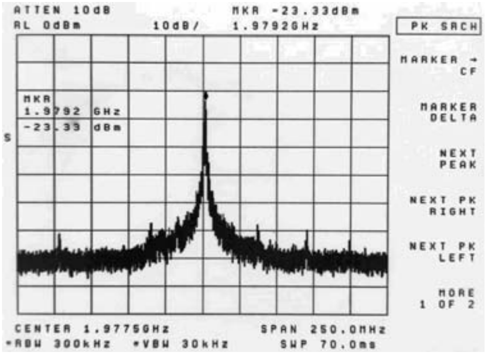
(a) (b)

Fig. 5-36 (a) Practical PCB measurement circuit seen above

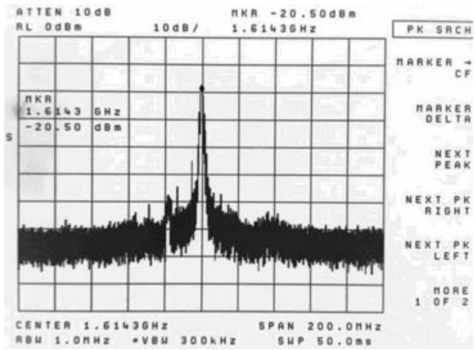
(b) Practical PCB measurement circuit seen aside

5.7.2 Measurement results

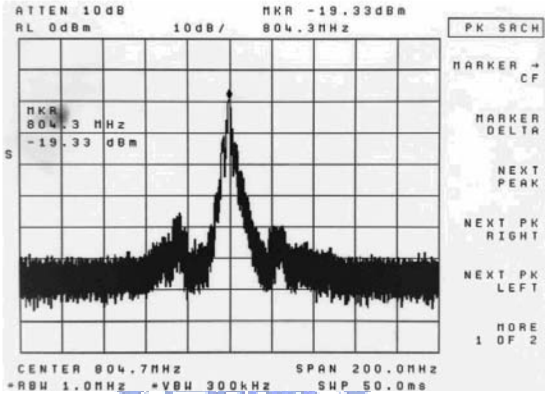
Down below in Fig. 5-37 shows the output power spectrum of each system. We find out that the circuit outputs -23.33dBm at 1.9792GHz, -20.5dBm at 1.6143GHz, and -19.33dBm at 804.3MHz corresponding to 2.4GHz, 1.8GHz, and 900MHz separately. Not only missing the 5.2GHz signal, frequency deviation is also severe upon the design work. This may due to improper designing considerations and over-small output power of each signal path.



(a)



(b)



(c)

Fig. 5-37 (a) Output power spectrum of signal 2.4GHz

(b) Output power spectrum of signal 1.8GHz

(c) Output power spectrum of signal 900MHz

The first thing needs to be done to fix the problem is to increase the output power to make sure the signal is large enough to drive the following stages. Besides that, the implementation of registers need to be carefully premeditation since overuse will lead to complicated measuring procedure and often cause error to happen.