國立交通大學

電信工程學系

碩 士 論 文

12 位元 500 百萬赫芝電流式互補式金氧化
半導體數位類比轉換器

A 12-bit 500-MSamples/s Current–Steering
CMOS D/A Converter

研 究 生：蔡宗諺

指導教授：洪崇智　教授

中 華 民 國 九 十 五 年 十 月

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研 究 生：蔡宗諺　　Student：Tsung-Yen Tsai

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國立交通大學電信工程學系（研究所）碩士班

摘　　要

高速類比數位轉換器和數位類比轉換器是目前高效能系統中不可獲缺的主要電路。高速數位類比轉換器在設計上，需要考慮如何將電路不匹配所造成的靜態和動態的誤差如 DNL、INL 和 SFDR 等誤差降低，以增加電路的解析度。

本論文設計實現一個 12 位元 500MHz 的數位類比轉換器，主要著重在 SFDR 的設計，在數位類比轉換器電路的實現，切換電流源式是一個很好的實現方法。在編碼方面，由於考量到電路的線性度表現，還有晶片面積的大小，所以採用低位元及高位元不同的編碼；低位元採用二進位權重，高位元採用溫度計編碼。除此之外，為了增進數位類比轉換器的動態效能及提高解析度與元件間的匹配，分別使用了抑制突波的拴鎖器和特殊的佈局，來增加數位類比轉換器的效能。整個電路利用電流源的切換，已達到較高的速度，電流源利用 PMOS 來達成，以降低本身電路的 flick noise 及 substrate 的干擾。同時也考量了在佈局繞線時產生的寄生電容，所造成速度還有信號不同步的效應。這個數位類比轉換器採用 TSMC 0.18 μm 1P6M mixed-signal CMOS 製程來實現，整體晶片的核心面積為 1.615 mm^2，加入 PADs 之後為 2.896 mm^2。

A 12-bit 500-MSamples/s Current–Steering CMOS D/A Converter

Student：Tsung-Yen Tsai　　Advisor：Dr. Chung-Chih Hung

Department of Communication Engineering
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ABSTRACT

Digital-To-Analog converters are essential components of modern applications, such as digital signal synthesis, video signal processing, and both wired and wireless transmitters. For data converters used in communications applications, the integral nonlinearity (INL) and differential nonlinearity (DNL) are not sufficient to characterize the performance. It is more convenient to characterize the performance in the frequency domain using measures as the spurious-free dynamic range (SFDR).

The major target specification for SFDR of this paper, a 12-bit 500-MSample/s D/A converter, is 60 dB for signal frequencies up to 170 MHz. An additional design goal was to derive maximum benefit from this relatively advanced technology. This architecture is divided into a coarse sub-DAC and a binary-weighted fine sub-DAC. The differential switches of current sources are controlled by de-glitch latch. The routing complexity and parasitic capacitance have to be considered for speed and signal synchronization. A 12-bit 500-MSample/s current-steering D/A converter integrated in a TSMC 0.18μm CMOS technology is presented. It is based on a current steering doubly segmented 8 + 4 architecture

and requires no trimming, no calibration, or dynamic averaging. The increased switching noise associated with a high degree of segmentation has been reduced by a new latch. The measure resultant shows that with the signal frequency of 34.33 MHz at the update rate of 100 MHz, the SFDR is 32 dB. The differential nonlinearity and integral nonlinearity are below 3.3 and 5.4 least significant bits (LSB's), respectively. The converter consumers a total power of 128 mW and it's active area is 1.615 mm^2.

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國立交通大學

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Chapter 1

Introduction

In the communication system, high-speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are key components [1]. For data converters used in communications applications, the integral nonlinearity (INL) and differential nonlinearity (DNL) are not sufficient to characterize the performance. It is more convenient to characterize the performance in the frequency domain using measures as the spurious-free dynamic range (SFDR) [2].

1.1 Motivation

Although Process variations and other parasites will influence the matching between current sources and introduced noise and distortion, CMOS current-steering DAC architectures are particularly suitable for these applications for the following reasons: (1) they can be designed in a standard digital CMOS technology, with evident cost and power consumption advantages in the integration with the digital circuits, and (2) they are intrinsically faster and more linear than competing architectures such as resistor-string DACs .

Current-steering DACs, with performance limited by fabrication process due to the mismatch in current cells, have been traditionally favored for high speed and high resolution applications because of their inherent monotonicity and their ability to drive a resistive load directly without the need of a voltage buffer. Recently, several examples of CMOS DACs with the current-steering architecture have been demonstrated in [3]-[17]. In terms of attaining static linearity, techniques such as trimming [17], and calibration [15] have been used, as reliable as the combination of the intrinsic device matching performance and special layout

techniques to combat gradient effects [4][6].

A 12-bit 500MHz (no trimming, no calibration, or dynamic averaging) current-steering segmented architecture DAC fabricated in TSMC 0.18μm CMOS is designed by using segmented current-steering architecture that consists of 8 MSB's of unary cells and 4 LSB's of binary cells. In addition, a high speed and low crossing point switch driver is designed to minimize glitch error during dynamic switching transition. In order to reduce the mismatch, the new layout will help overcome the variation across a range of process.

1.2 Organization

This thesis is organized as six chapters. Brief content of each chapter is described as follows. In chapter2, the fundamental concepts and architectures of DAC are described first. In addition, the static and dynamic specifications that will impact a DAC's performance are discussed. Chapter 3 presents the nonidealities of current-steering DAC, including finite output impedance, mismatch in current source, timing nonidealities, and nonidealities due to switching in a current-steering DAC. In Chapter 4, based on the consideration discussed in chapter 2 and chapter 3, the design and implementation of a 12-bit 500MHz current-steering segmented architecture DAC is described in chapter 4.

Chapter 5 presents the simulation and measurement results. Conclusion and future work are in chapter 6.

Chapter 2

Digital-to-Analog Converter Architecture

Digital-to-analog conversion is an essential function in data processing systems. D/A converters (DACs) interface the digital output of signal processors with the analog word. The digital-to-analog (D/A) converts a discrete amplitude, discrete time signal to a continuous amplitude, continuous time output.

If the DAC generate large glitches during switching from one code to another, then a deglitching circuit is used to mask the glitches. Finally a low-pass filter is required to suppress the sharp edges introduced by the DAC [22].

In this chapter, the fundamental of DAC and different techniques for converting a digital signal into an analog signal representation is presented. The approaches differ in speed, chip area, power efficiency, achievable accuracy, etc.

2.1 Ideal D/A converter

A digital-to-analog converter produces an analog output V_{out} that is proportional to the digital input B_{in}. For a N-bit D/A converter shown in Fig. 2.1, the output V_{out} can be expressed as :

$$V_{\text{out}}=V_{\text{ref}} \times B_{\text{in}} \qquad (2.1)$$

$$V_{\text{LSB}}=V_{\text{ref}} / 2^{N} \qquad (2.2)$$

$$B_{in} = \sum_{i=0}^{N-1} b_i \cdot 2^i \qquad (2.3)$$

where b_i equals 1 or 0. We also define b_0 as the least significant bit (LSB) and b_{N-1} as the most

significant bit (MSB).

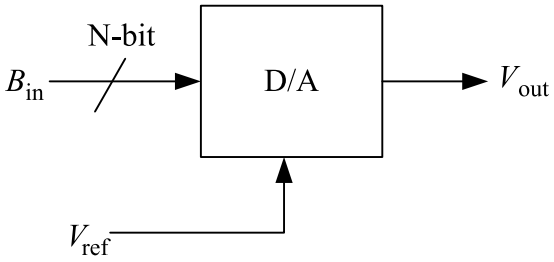


Fig. 2.1 Block Diagram of a N-bit D/A converter

2.2 Static Performance of DACs

Due to non-ideal circuit elements in the actual implementation of a data converter the code transition points in the transfer function will be moved as illustrated in Fig. 2.2.

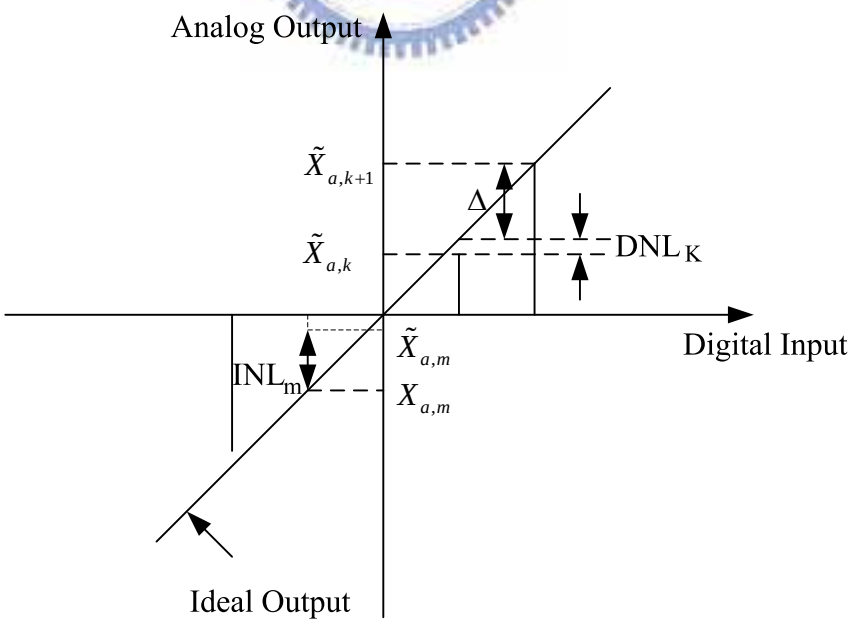


Fig. 2.2 Non-ideal transfer function with INL and DNL errors of DAC

To distinguish between the actual and ideal values in the data converters, all actual values are indicated with a ~. This means that $X_{a,k}$ corresponds to the ideal analog value for digital code $X_{d,k}$ while $\tilde{X}_{a,k}$ corresponds to the actual value.

The step size in the non-ideal data converter deviates from the ideal size △ and this error is called the differential nonlinearity (DNL) error. For a DAC the DNL can be defined as the difference between two adjacent analog outputs minus the ideal step size, i.e.

$$DNL_k = \tilde{X}_{a,k+1} - \tilde{X}_{a,k} - \Delta \qquad (2.4)$$

The DNL is often normalized with respect to the step size to get the relative error, i.e.

$$DNL_k = \frac{\tilde{X}_{a,k+1} - \tilde{X}_{a,k} - \Delta}{\Delta} \qquad (2.5)$$

The above definitions are often most practical for DACs since the analog values can be directly measured at the output.

The total deviation of an analog value from the ideal value is called integral nonlinearity (INL). The normalized INL can be expressed as

$$INL_k = \frac{\tilde{X}_{a,k} - X_{a,k}}{\Delta} \qquad (2.6)$$

The relation between INL and DNL is given by

$$INL_k = \sum_{\iota=1}^{k} DNL_\iota \qquad (2.7)$$

The nonlinearity errors are usually measured using a low frequency input signal to exclude dynamic errors appearing at high signal frequencies. The DNL and INL are therefore usually used to characterize the static performance.

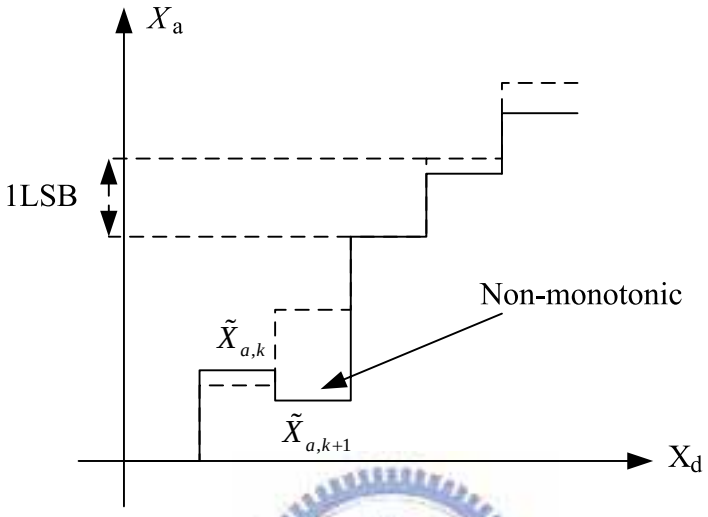


Figure 2.3 A non-monotonic DAC

If the analog amplitude level of the converter increases with increasing digital code, the converter is monotonic. An example of a non-monotonic DAC is shown in Fig 2.3. Monotonicity is guaranteed if the deviation from the best-fit straight line is less than half a LSB, i.e.

$$\left|INL_k\right| \le \frac{1}{2} LSB \quad \text{for all k} \tag{2.8}$$

This implies that the DNL errors are less than one LSB , i.e.

$$\left|DNL_k\right| \le 1LSB \quad \text{for all k} \tag{2.9}$$

It should be noted that the above relations are sufficient to guarantee monotonicity, but it is possible to have a monotonic converter that does not meet the relations in (2.8) and (2.9). There are some data converter architectures that are monotonic by design, e.g. a thermometer coded DAC.

2.3 Dynamic Performance of DACs

In addition to the static errors that are caused by mismatch in the components in the data converter, several other error sources will appear when the input signal change rapidly. These dynamic errors are often dependent on signal frequency and increases with signal amplitude and frequency. They appear in data converter but are usually more critical in DACs since the shape of the analog wave form determines the performance [2].

A number of dynamic effects arise when the output signal is changed between two samples. These dynamic error sources will have a large impact on the DAC performance, especially at high clock and signal frequencies. When the input of the DAC is changed, the analog output should ideally change from the ideal start value, $X_{a,k}$ to the ideal final value, $X_{a,m}$ see Fig. 2.4. Due to circuit imperfections the actual start and final values are $\tilde{X}_{a,k}$ and $\tilde{X}_{a,m}$ respectively. The output signal of an actual DAC can not change its value instantly. The time it takes for the output to settle within a certain accuracy of the final value, for instance 0.1%, is called the settling time T_s, and determines the highest possible speed of the circuit.

The settling can be divided in two phases, a non-linear slewing phase and a linear settling phase. The slewing phase should be as small as possible since it both increases the settling time and introduces distortion in the analog waveform. The slewing is normally

caused by a too small bias current in the circuit driving the output and is therefore increased for large steps when more current is needed.

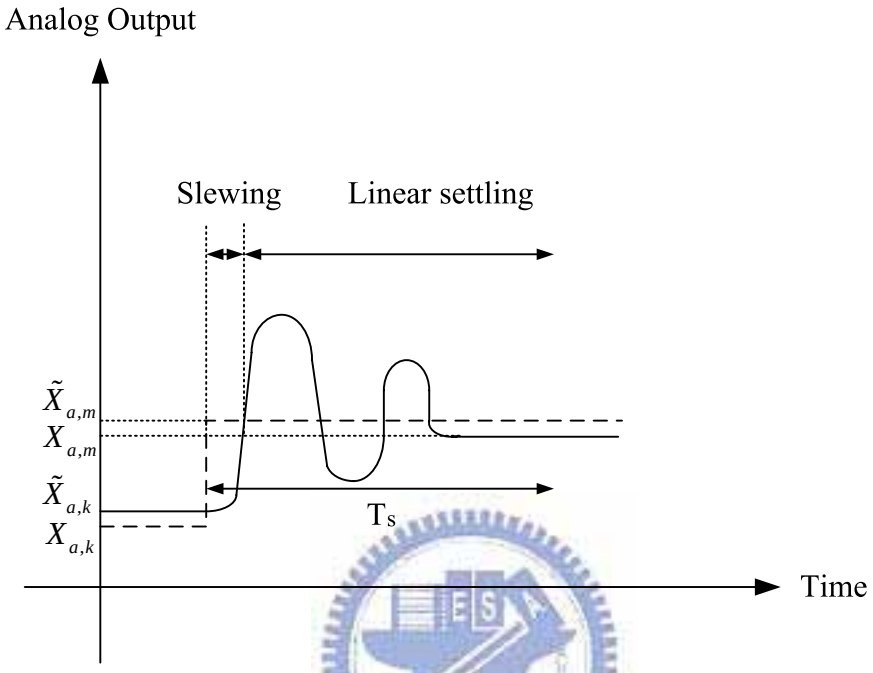


Fig. 2.4 Actual output signal and ideal output signal (dashed) of a DAC

Glitches occur when the switching time of different bits in a DAC is unmatched. For a short period of time a false code could appear at the output. For example if the code transition is

0111……111 → 1000……000

and the MSB switches faster than the LSBs, the code 1111……111 may be present for a short time This code represents the maximum value and hence a large glitch appears at the output. The glitch adds a signal dependent error to the output signal that degrades the performance. The effect on the output signal is determined by the energy of the glitch.

The clock feedthrough (CFT) can introduce both harmonic distortion and distortion

tones at multiples of the clock signal. It is caused by the finite overlap capacitance between the gate and drain terminals. In Fig. 2.5, when the gate control voltage CLK changes to high voltage, the PMOS turns off and C_{ov} conducts the transition and changes the voltage stored on C_L by an amount equal to

$$\Delta V = \frac{C_{ov}}{C_{ov} + C_L} V_{CLK} \tag{2.10}$$

The CFT is reduced when reducing the capacitive coupling and therefore the switch transistor sizes should be small to decrease the size of the parasitic capacitances. However, with a smaller transistor, the on-resistance increases which may degrade the performance due to an increased settling time.

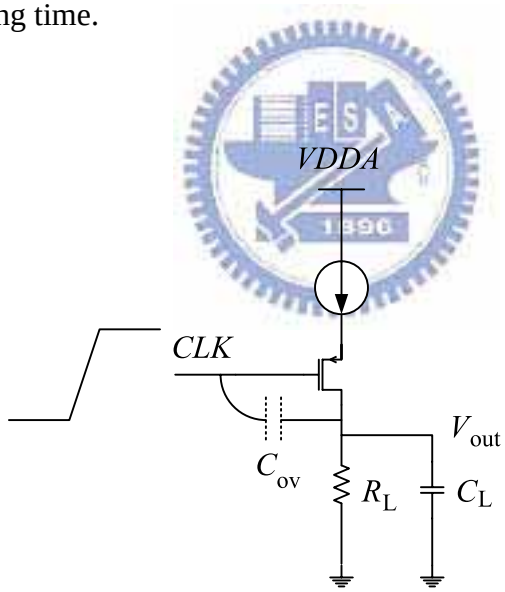


Figure 2.5 Clock Feedthrough for MOS switch

2.4 Charge Redistribution DAC

The charge redistribution DAC is a switch capacitor (SC) circuit, where the charge stored on a number of binary weighted capacitors is used to perform the conversion. Fig. 2.6

is an example of a N-bit converter. Typically, the weighted capacitors are created using a number of unit capacitors.

At time nT (on phase ψ_1), the bit b_i determine which of the binary weighted capacitors that should be charged from the reference voltage, V_{ref} . During this phase, the plates of capacitor C_N are connected to ground and virtual ground at the input of the op amp, i.e., there is no charge on C_N, and $q_N(nT) = 0$. Capacitor C_C is used for offset compensation.

The total charge on the binary weighted capacitors at time nT is given by

$$q_T(nT) = V_{ref} \sum_{l=0}^{N-1} C_l \cdot b_l = V_{ref} \sum_{l=0}^{N-1} 2^l \cdot C \cdot b_l = V_{ref} \cdot C \cdot k(nT) \qquad (2.11)$$

At time $nT + T/2$, on phase ψ_2, the weighted capacitors are discharged since their plates are connected to DC and virtual grounds. The charge is redistributed to ground and C_N . The charge on C_N at the end of the settling is

$$q_N(nT + \frac{1}{2}T) = C_N \cdot V_{out}(nt + T/2) \qquad (2.12)$$

Charge conservation gives

$$q_N(nT + \frac{1}{2}T) = -q_T(nT) \qquad (2.13)$$

Using (2.11) and (2.12) in (2.13) we have

$$V_{out}(nt + T/2) = \frac{C}{C_N} \cdot k(nT) \cdot V_{ref} \qquad (2.14)$$

The architecture in Fig. 2.6 is insensitive to offset voltage and finite gain of the amplifier. The limitations of the converter are the matching of the capacitors, the switch-on resistance, and finite bandwidth of the amplifier.

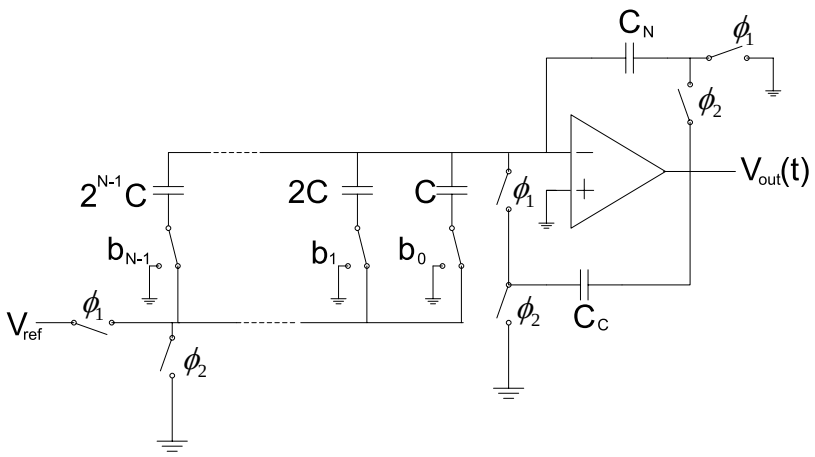


Fig. 2.6 The architecture of a N-bit charge-redistribution DAC

2.5 R-2R Ladder DAC

It is easy to construct a resistor-based binary-weighted DAC. But the resistance spread is very large for a large number of bits *N*. To reduce the large resistor ratios in a binary-weighted DAC, the R-2R ladder architecture is a good choice. An *N*-bit R-2R ladder architecture is shown in Fig. 2.7. The current sources are all equally large, and the switches are controlled by the bits b_i. At every node, the impedance is always *R*. The output current is given by

$$I_{out} = \frac{I}{2^{N-1}} \cdot \sum_{i=0}^{N-1} b_i \cdot 2^i = \frac{I}{2^{N-1}} \cdot K \qquad (2.15)$$

This DAC architecture is power inefficient, since there is a current loss through the resistive network. Due to the fact that all current sources are equally large, the matching can

be improved. In a poor process, the resistors can be non-linear and contain signal-dependent capacitive parts yielding distortion. Time-skew between switching instants generates glitches in this architecture. In this R-2R ladder architecture there is the same amount of current through all switches, which makes the design of the switches simpler. However, the internal voltage nodes are still AC varying and therefore the current sources will have varying terminal voltages.

As a conclusion, one of the major advantages is that we only have a few number of different component sizes to implement, i.e., two resistor sizes, *R* and *2R*, one current source size, and one type of current switch. This allows a more regular layout and since the current sources all have the same size. R-2R ladder DACs are more widely used in bipolar processes where high-quality resistors are available.

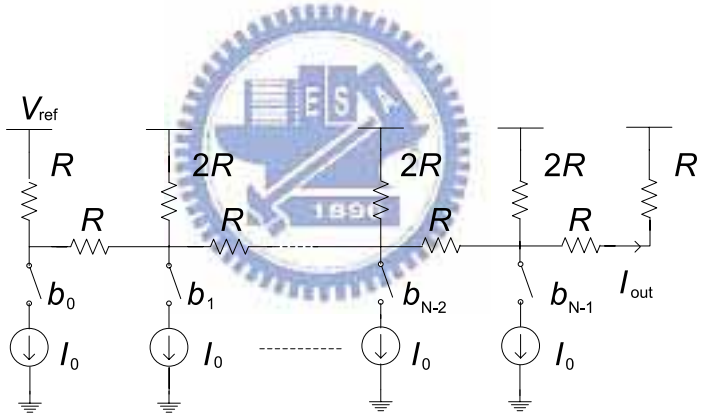


Fig. 2.7 An *N*-bit R-2R ladder DAC

2.6 Binary Weighted Current-Steering DAC

The switched-current (SI) technique is a common choice in a CMOS process, since the reference and sum elements as well as switches are relatively easy to be implemented. The general architecture of a binary weighted current-steering DAC is shown in Fig. 2.8.

The switches are controlled by the input bits, b_i , where i = 0, 1, … , N-1 and N is the

number of bits. b_0 is the LSB and the corresponding current source has the DC value I_{LSB} . The source controlled by bit b_i , i.e., the i -th LSB current source, is formed by connecting 2^i LSB current sources (unit current sources) in parallel, hence the MSB current source has the DC value $I_{MSB}=2^{N-1}I_{LSB}$. The use of unit element sources increases the matching of the sources. The output current, I_{out} , of the DAC shown in Fig.2.8 is given by

$$I_{out}(k) = I_{LSB} \cdot b_0 + 2I_{LSB} \cdot b_1 + \cdots + 2^{N-1} I_{LSB} \cdot b_{N-1} = I_{LSB} \cdot k \qquad (2.16)$$

Where k is the digital input given by

$$k = b_0 + 2 \cdot b_1 + \cdots + 2^{N-1} \cdot b_{N-1} = \sum_{l=0}^{N-1} 2^l \cdot b_l \qquad (2.17)$$

The current-steering DAC has the advantage of being quite small for resolution below 10 bits and it is very fast. The major disadvantage is the sensitivity to device mismatch, glitches, and current source output impedance for higher number of bits. Another good property of the current-steering DAC is that its high power-efficiency since all power is directed to the output. The current-steering DAC is suitable for high-speed high-resolution applications, especially when special care is taken to improve the matching of the converter.

To achieve monotonicity, reduce the influence of glitches and reduce the sensitivity to matching errors, the DAC should be segmented into a coarse and fine part. The coarse part is realized by thermometer coded and fine part is kept binary weighted. This is referred to as a segmented converter and is discussed further.

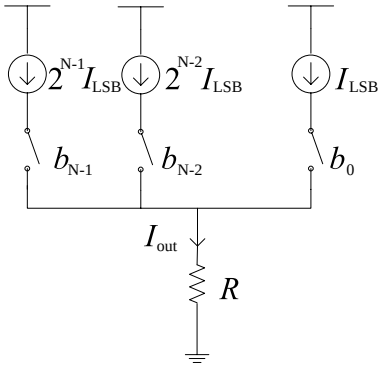


Figure 2.8 An *N*-bit current-steering binary weighted DAC

2.7 Thermometer Coded DAC Architecture

The thermometer coded DAC differs from a binary one is that a thermometer-code has 2^{N-1} digital inputs to represent 2^N different values. Each digital inputs control the current sources with equally large value, I. Fig.2.9 shows a N-bits example of thermometer coded current steering DAC converter. The binary input coded is encoded into a thermometer coded as illustrated in Table 2-1 for a 3-bit input example.

Monotonicity is guaranteed here since, when the binary input changes to the next higher value, one more digital value in the thermometer code goes high, causing additional current to be drawn out and forces the resistor output to go some amount high. The DNL and INL are improved compared to the binary version. The requirements on element matching are also relaxed. In fact, if the matching is within a 50% margin, the converter is still monotonic.

More importantly, a D/A converter based on a thermometer code greatly minimizes glitches, as compared to binary version, since banks of current sources are never exchanged at slightly different times when the output should be change by on 1LSB. The major drawback of thermometer-coded DAC is area, since for every LSB this architecture needs a current source, a switch, and a decoding circuit, as well as the binary to thermometer decoder.

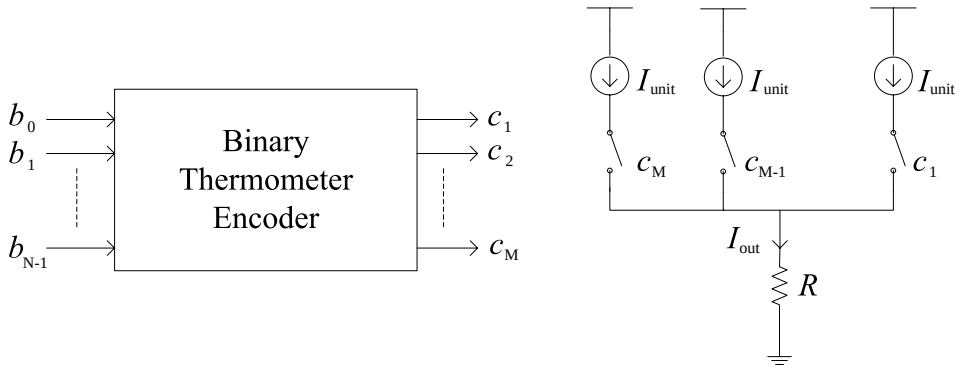


Figure 2.9 A thermometer coded current-steering DAC with encoding circuit

Decimal	**Binary**			**Thermometer Code**						
	b_2	b_1	b_0	c_7	c_6	c_5	c_4	c_3	c_2	c_1
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

Table 2-1 Thermometer Code Representations for 3-Bit Binary Values

2.8 Hybrid DAC Architecture

As mentioned in the previous section, architectures based on different DACs suffer form several important drawbacks. First, they require tight device matching to achieve

monotonicity (DNL<1LSB). Second, they require exhibit large glitch impulse. Third, the decoding circuits may be complexity, and consume large area. Hybrid architecture is commonly used to alleviate these problems. The M-bit Hybrid architecture is illustrated in Fig. 2.10 where each N-bit DAC can be of completely different types.

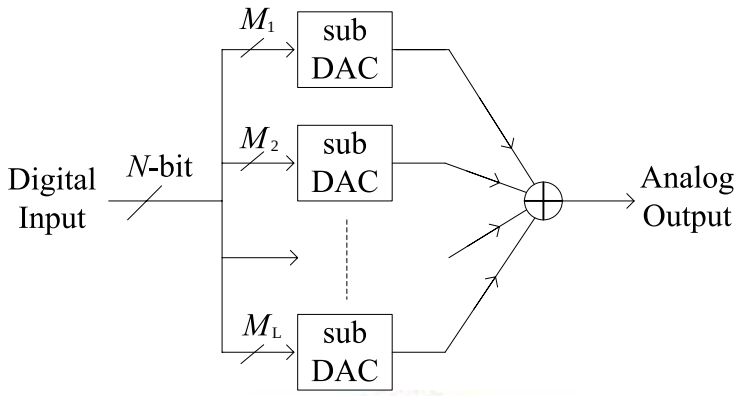


Fig. 2.10 Hybrid DACs use a combination of a number of different types of DACs

For instance, a popular hybrid converter architecture is the so called segmented architecture as show in Fig.2.11. This architecture is divided into a coarse sub-DAC and a binary-weighted fine sub-DAC. In other words, for a resolution of K = M+N, the M most significant bits are converted to thermometer code and drive a 2^{M-1} unit segmented array, while the remaining N bits are directly applied to an N-bit binary array.

The choice of *M* and *N* in general depends on the matching of the current source, the tolerable glitch, and area. When increasing *M*, the size of the encoder grows exponentially and a larger amount of switches and interconnection are needed. However, the advantages are the improved device matching and linearity over binary weighted DACs. One of the key issues is to find the optimum number of MSBs to encode into a thermometer code. Reasonable size for *M* is in the range from 4-8.

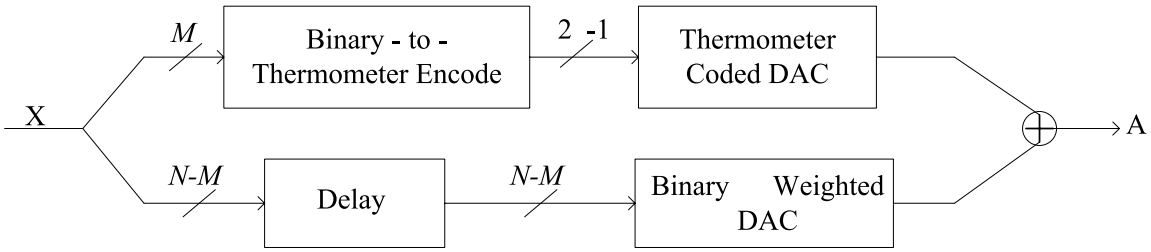


Fig. 2.11 An *N*-bit segmented DAC where *M* MSBs are thermometer coded

2.9 Summary

In this chapter, the fundamental of the digital-to-analog Converters (DACs) is presented first. The performance parameters used to characterize the specifications of DAC is also described. Also, different types of Nyquist-Rate DACs are introduced.

According to the discussions of the advantages and disadvantages for different type DACs, we can choose the suitable architecture for our applications among several trade-offs, like power consumption, speed, and die area.

Chapter 3

Nonidealities in Current-Steering DAC

Current-steering DAC is a popular topology when high speed and high resolution is needed since it can drive resistive loads directly, and do not require high speed amplifiers at the output. A differential output type current steering DAC is preferred because it can lower the common mode noise and second harmonic distortion. But it still has some nonidealities that will degrade the performance of the DAC. The errors sources that cause the nonidealities include finite output impedance effect, current source mismatch, timing nonidealities and nonidealities due to switching the current cells.

The effects of nonidealities mentioned above on the performance of a current-steering DAC can be categorized into two groups:

Increased Random Noise : An increase in the noise floor in the signal band reduces the dynamic range of the converter. Sources of random noise include the thermal noise of transistors and resistors and the coupling of noise from digital circuitry into the analog circuits through the common substrate, package, and supply lines.

Harmonic Distortion : Signal-dependent nonidealities result in harmonic distortion in the DAC output. Ideally, even harmonics are completely cancelled through the use of a differential topology, but mismatch between the differential paths results in some residual even-harmonic distortion. In the following section, we discuss the nonidealities of current-steering DAC and the effects they will cause on both static performance and spectrum specification.

3.1 Finite output impedance of current source

The output impedance of a current-steering DAC consists of the parallel combination of load resistance and total impedance of current sources that are turned on. The output voltage is determined by the current flow through the output resistance. Because the output impedance is variable due to finite output impedance of the current sources that are turned, the performance of the DAC will degrade [2].

Fig. 3.1 shows a current-steering array including output impedance of each current source. It is a thermometer coded structure, where r_o represents the output impedance of each current source. For the thermometer code of height j, the actual output voltage is

$$V_{out,j} = j \cdot I \cdot \left(R_L \,||\, \frac{r_o}{j} \right) \qquad (3.1)$$

The dependence of the term in parentheses introduces integral nonlinearity (INL). To obtain the INL profile, we pass a straight line through the end points of (3-1) (given by j = 0 and j = *N*) and find the difference between (3-1) and the line. It is described as follow :

For j = *N*

$$V_{out,N} = NI \left(R_L \,||\, \frac{r_o}{N} \right) \qquad (3.2)$$

therefore the ideal output voltage for height j is

$$V_{out,j} = j \cdot I \cdot \left(R_L \,||\, \frac{r_o}{N} \right) \qquad (3.3)$$

The difference between the ideal and actual voltage can result in INL error

$$INL_j = j \cdot I \left(R_L \| \frac{r_o}{j} - R_L \| \frac{r_o}{N} \right) \tag{3.4}$$

After an approximation the INL error can be expressed as

$$INL_j = \frac{IR_L^2}{r_o} j(N-j) \tag{3.5}$$

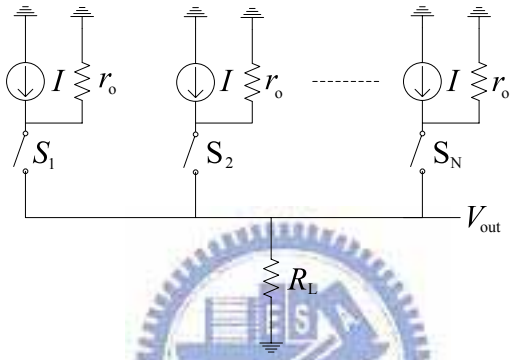


Fig. 3.1 Current Steering Array Including Output Impedance of Each Current Source

Any non-ideal current source has a finite output resistance and can be modeled as shown in Fig. 3.2 [2]. In the figure the current source is terminated over a resistive load at the output. When the different current sources are switched to the output, the total output resistance is changed and when only static values are considered, the AC current through the load, I_L, is

$$I_L = \frac{I_{out} R_{out}}{R_{out} + R_L} \tag{3.6}$$

Where I_{out} is the nominal output current from the DAC, R_{out} is the output resistance, and R_L is the load resistance. From (3.6) it is seen, that if the output resistance of the DAC is

constant, there is only a gain error, which does not degrade linearity. If the output conductance depends on the input, it will give rise to distortion. Using (3.6) and assuming a signal-dependent output resistance of the DAC, $R_{\text{out}}(k)$, the current delivered to the load is

$$I_L(k) = I_{out}(k) \cdot \frac{R_{out}(k)}{R_{out}(k) + R_L} = (I_{unit} \cdot k) \frac{\frac{R_{out}}{k}}{R_L + \frac{R_{out}}{k}} \qquad (3.7)$$
$$= I_{unit} \cdot \frac{k}{1 + k \cdot \rho} = \frac{I_{unit}}{\rho} \left(1 - \frac{1}{1 + k \cdot \rho} \right)$$

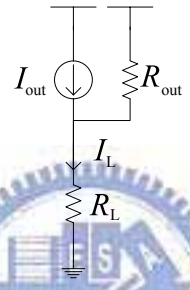


Fig. 3.2 Generalized view of a current source with a non-zero output conductance

Where k is the DAC's digital input and $\rho = R_{\text{L}} / R_{\text{unit}}$.

Assume that the input signal is a sinusoidal signal

$$k = K_{dc} + K_{ac} \cdot \sin\theta + v \qquad (3.8)$$

Where K_{dc} is the DC level of the signal, is the amplitude of the sinusoid, K_{ac} is the normalized signal frequency times the sequence index, and v corresponds to the quantization error, which is AWGN for converters with a larger number of bits.

Then the output current as given by (3.7) and (3.8) becomes

$$I_L(k) = \frac{I_{unit}}{\rho} \cdot \left(1 - \frac{1}{1 + \rho \cdot (K_{dc} + K_{ac} \cdot \sin\theta)} \right) \tag{3.9}$$

where the noise term *v* has been neglected. The equation is rewritten as

$$\begin{aligned} I_L(k) &= \frac{I_{unit}}{\rho} \cdot \left(1 - \frac{1}{1 + \rho \cdot (K_{dc} + K_{ac} \cdot \sin\theta)} \right) \\ &= \frac{I_{unit}}{\rho} \cdot \left(1 - \frac{1}{1 + \rho \cdot K_{dc}} \cdot \frac{1}{1 + \frac{\rho \cdot K_{ac}}{1 + \rho \cdot K_{dc}} \cdot \sin\theta} \right) \end{aligned} \tag{3.10}$$

Examining (3.10) we find that only the second term within parenthesis contains AC frequency information, and we have

$$I_L(k) = \frac{I_{unit}}{\rho} \cdot \left(1 - \frac{1}{1 + \rho \cdot K_{dc}} \cdot I_{ac}(k) \right) \tag{3.11}$$

The gain factors inside and outside the parentheses can be neglected since we are considering only power *ratios* when determining the *SFDR*, and the AC signal is

$$I_{ac}(k) = \frac{1}{1 + A\sin\theta} \tag{3.12}$$

Where

$$A = \frac{\rho \cdot K_{ac}}{1 + \rho \cdot K_{dc}} \tag{3.13}$$

Comparing (3.10) with (3.11) it is clear that and will have the same distortion, since they only differ in offset and constant gain. To avoid signal clipping we have that $K_{ac} < K_{dc}$ for a binary offset code, and we have

$$0 \le A < 1 \tag{3.14}$$

and obviously that

$$\left| A \cdot \sin\theta \right| < 1 \tag{3.15}$$

This implies that we may find a converging Taylor series expansion of from (3.12).

$$\begin{aligned} I_{ac}(k) &= \sum_{n=0}^{\infty} (-A \cdot \sin\theta)^n \\ &= 1 - A\sin\theta + \sum_{n=1}^{\infty} (-A \cdot \sin\theta)^{2n} - \sum_{n=1}^{\infty} (-A \cdot \sin\theta)^{2n+1} \end{aligned} \tag{3.16}$$

The DC level and the gain can once again be neglected. By using trigonometric formulas [19] , we find that (3.16) may be written as

$$\begin{aligned} I_{ac}(k) = f(k) - \sin\theta \cdot A \cdot \left[1 + \sum_{n=1}^{\infty} \left(\frac{A}{2} \right)^{2n} \binom{2n+1}{n} \right] - \cdots \\ \cdots - \cos 2\theta \cdot 2 \cdot \sum_{n=1}^{\infty} \left(\frac{A}{2} \right)^{2n} \binom{2n}{n-1} \end{aligned} \tag{3.17}$$

where $f(k)$ contains the DC component and higher order harmonics that do not influence the *SFDR.* The *SFDR* is now found in (3.17) as the power ratio between the fundamental and

the 2nd harmonic as

$$SFDR = \frac{A^2}{4} \cdot \left[\frac{1 + \sum_{n=1}^{\infty} \left(\frac{A}{2}\right)^{2n} \binom{2n+1}{n}}{\sum_{n=1}^{\infty} \left(\frac{A}{2}\right)^{2n} \binom{2n}{n-1}} \right]^2 = \left(\frac{1+\sqrt{1-A^2}}{A} \right)^2 \qquad (3.18)$$

By substituting back A from (3.13) in (3.18) this becomes

$$SFDR = \left[\frac{1+\rho \cdot K_{dc}}{\rho \cdot K_{ac}} + \sqrt{\left(\frac{1+\rho \cdot K_{dc}}{\rho \cdot K_{ac}} \right)^2 - 1} \right]^2 \qquad (3.19)$$

which may also be written as

$$SFDR = \left[\frac{R_{ratio} + K_{dc}}{K_{ac}} + \sqrt{\left(\frac{R_{ratio} + K_{dc}}{K_{ac}} \right)^2 - 1} \right]^2 \qquad (3.20)$$

Where $R_{\text{ratio}} = 1/\rho$. In the special case with a full-scale sinusoid ($K_{ac} = K_{dc} = \frac{2^N - 1}{2} \approx 2^{N-1}$) and R_{ratio} is very large, we have that (12-34) can be approximated

$$SFDR \approx \left[2 \cdot \frac{R_{ratio} + K_{dc}}{K_{ac}} \right]^2 = 20 \log R_{ratio} - 6(N-2) \quad \text{dBc} \qquad (3.21)$$

3.2 Current Source Mismatch

Current steering DACs are based on an array of matched current cells that are steered to the DAC output depending on the digital input. The current sources in an array may exhibit mismatches due to random or gradients variation, which are referred as random error and systematic error, individually.

3.2.1 Random Error

The random error of the current sources is determined by matching properties of the MOS transistors. Consider two normally identical current sources as shown in Fig. 3.3. The output currents I_1 and I_2 exhibit mismatch components due to mismatch between transistors M_1 and M_2. The nominally identical devices suffer from a finite mismatch due to uncertainties in each step of the manufacturing process. For example, as illustrated in Fig. 3.4 the gate dimensions of MOSFETs suffer from random, microscopic variations and hence mismatches between the equivalent lengths and widths are laid out [18].

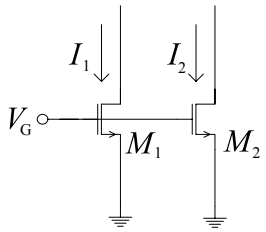


Fig. 3.3 Nominally Identical MOS Current Sources

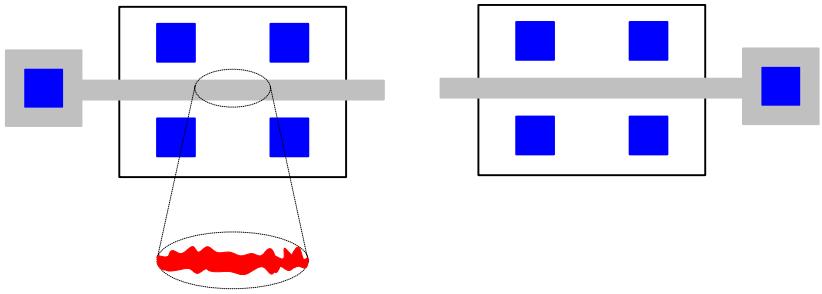


Fig. 3.4 Random Mismatch Between Two Identical Devices

For Fig. 3.3, assume M_1 and M_2 are nominally identical and have square-law I-V characteristics：

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_T\right)^2 \qquad (3.22)$$

Usually we increase W, L, and V_{GS} to lower the mismatch in the drain current. However, larger W leads to higher drain-substrate and gate-drain capacitance and large area, larger L requires higher V_{GS}-V_T to attain a given I_D, and increasing V_{GS}-V_T limits the voltage swing at the drain of M_1 and M_2. As a consequence, some compromise is usually necessary to obtain a reasonable combination of accuracy, speed, and output voltage swing.

The current mismatch will degrade static and dynamic performance that will be discussed in section 3.2.3. In order to reduce to effect of current mismatch, proper dimensions of current sources should be chosen. An estimation of the minimum channel area of transistor versus mismatch parameters are described as follow [13]：

$$I_D = \frac{1}{2}\beta\left(V_{GS} - V_T\right)^2 \qquad (3.23)$$

Where $\beta=\mu C_{ox}(W/L)$, the relative current mismatch is

$$\sigma^2\left(\frac{\Delta I}{I}\right)=\sigma^2\left(\frac{\Delta\beta}{\beta}\right)+4\frac{\sigma^2(\Delta V_T)}{\left(V_{GS}-V_T\right)^2} \tag{3.24}$$

According to [6], the minimum size of current source is equal to

$$\left(WL\right)_{\min}=\frac{\frac{1}{2}\left[A_\beta^2+\frac{4A_{VT}^2}{\left(V_{GS}-V_T\right)^2}\right]}{\left(\frac{\sigma_I}{I}\right)^2} \tag{3.25}$$

Where

$$\sigma^2(\frac{\Delta\beta}{\beta})=\frac{A_\beta}{WL} \tag{3.26}$$

$$\sigma^2(\Delta V_T)=\frac{A_{VT}}{WL} \tag{3.27}$$

The parameter A_{VT} and A_β are technology parameter, depended on the given process. From (3-25), we can see that the minimum area of the current source, $(WL)_{\min}$, is function of overdrive voltage, $(V_{GS}\text{-}V_T)$, and the current mismatch standard deviation (σ_I/I). By increasing the overdrive voltage, and minimum area required for current source can be decreased.

3.2.2 Systematic Error

If the resolution of the DAC increases by a single bit, the number of current-source

array doubles. The area occupied by a single unity current source also doubles because of random matching constraint. This leads to a four times area increase for the current source array for each additional bit. For DAC with a resolution of 10-bit and higher, the dimension of the current source array become so large that process, temperature, and electrical gradients have to be considered. The nonlinearity errors introduced by these gradients can be partially compensated by the introduction of a special switching scheme. We only focus on the error source here.

The error sources of systematic error consist of edge effects, voltage drops in the supply lines, thermal gradients, and doping gradients. The edge effect means the current sources in the edge of the current cell matrix have different surrounding environments than the other current sources. This effect can be avoided by adding dummy cells in the edge of the current cell matrix, as shown in Fig. 3.5.

The current error caused by the voltage drop in the ground lines is given by [8]

$$i_{voltage\ drop}(x) = \sqrt{g_m R_{gnd}}\,\frac{\cosh(\sqrt{g_m R_{gnd}}\,x)}{\sinh(\sqrt{g_m R_{gnd}})} \approx a_0 + a_1 x^2 + \ldots \qquad (3.28)$$

where x is the coordinate of the current source along the ground line. Eliminating the voltage drop in the ground line to achieve high linearity by properly sizing the ground line would incur an unacceptable increase in the area of the current source array. Therefore, this error is preferred to be compensated by the switching scheme.

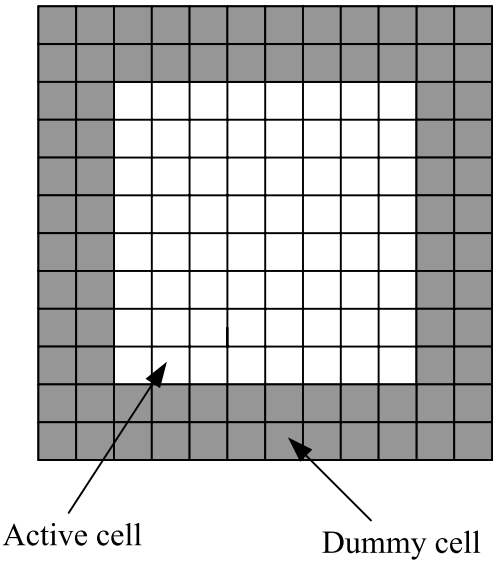
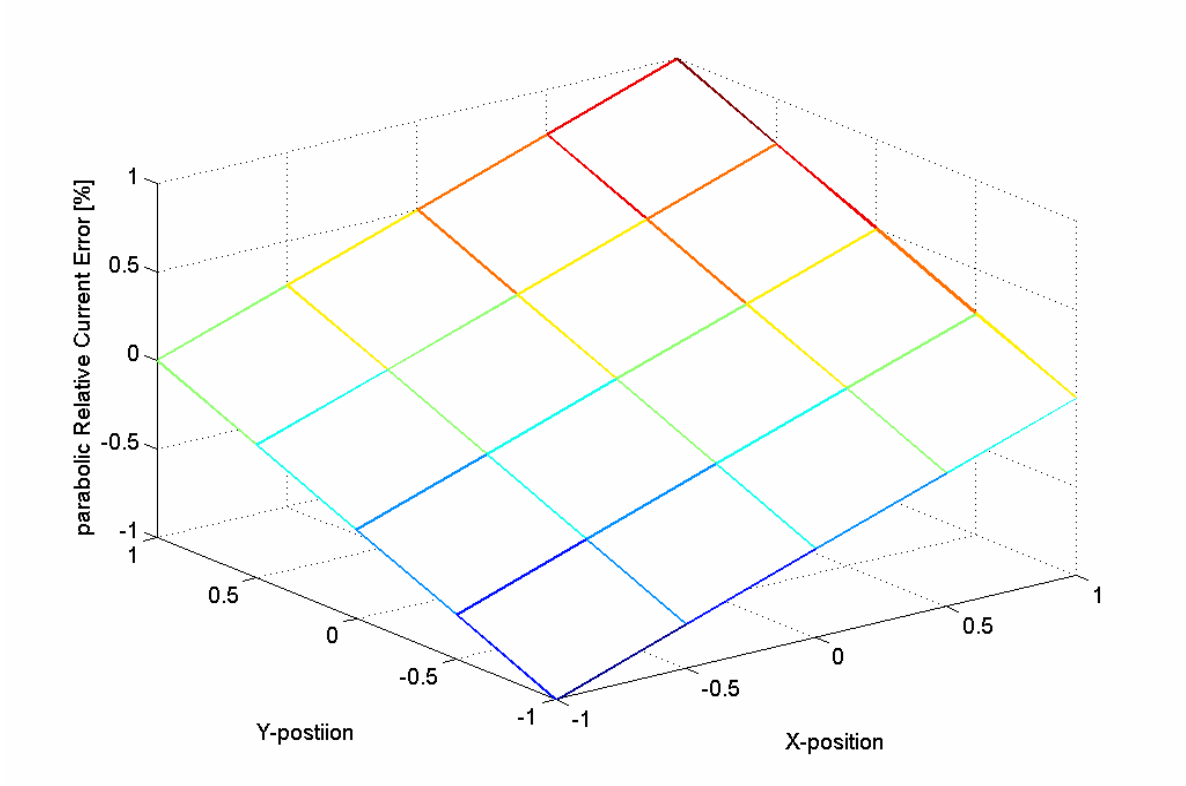


Figure 3.5 Current Cell Matrix With Dummy Cell

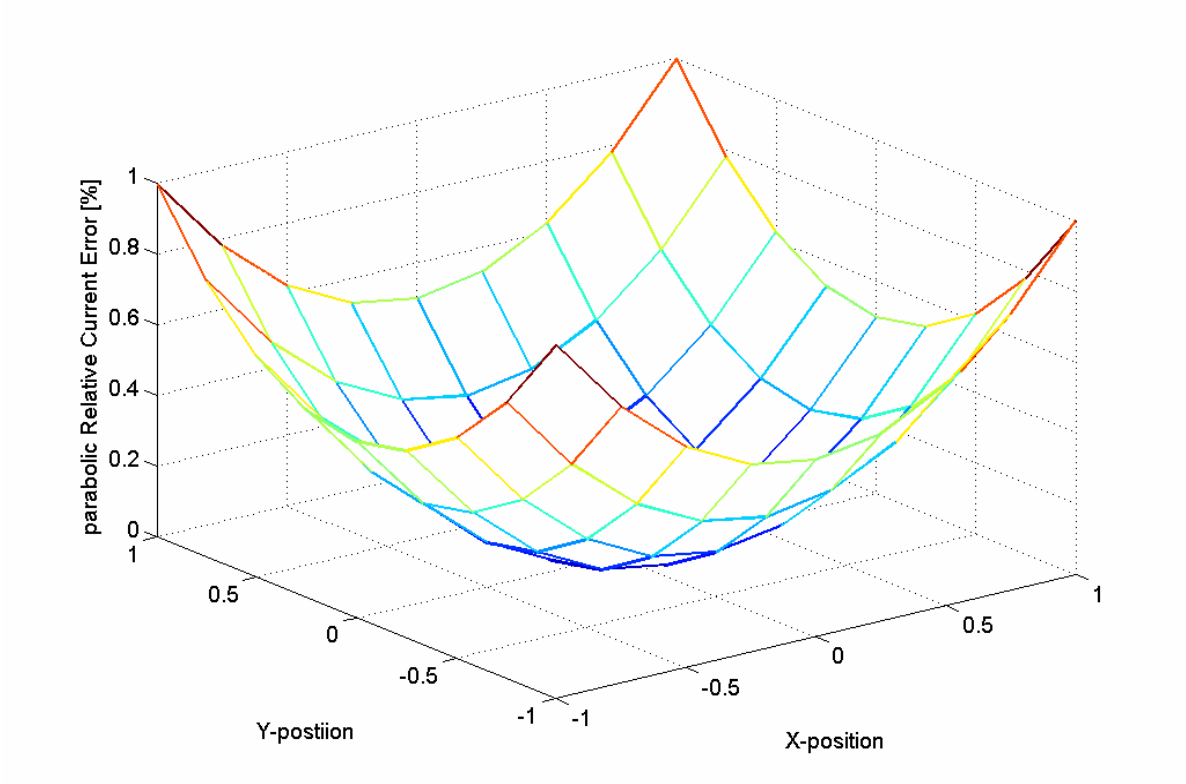
The thermal gradients and technology-related errors are approximated by a Taylor series expansion around the center of the current source array [8].

$$i_{thermal,technology,\cdots}(x,y) = b_0 + b_1 x + b_2 y + b_3 xy + b_4 x^2 + b_5 y^2 + \cdots \quad (3.29)$$

where (x,y) is the coordinate of the unit in the current source array. The current source array that contains errors mentioned above can be linear (first order) and quadratic (second order) in spatial distribution, as shown in Fig. 3.6 [6][8].



(a)



(b)

Fig. 3.6 (a) Two-dimensional linear error and (b) 2-D parabolic error

3.3 Nonidealities Due to Switching in the Current Cells

Glitch is a limitation during high-speed operation for converters that have digital logic directly related to switching different signals. For example, when the digital input code changes from 0111…1 to 1000…0, all of LSB turn off and MSB turn on. So it has two kinds of situation happen. One is possible that the switches of LSB will turn off before MSB turn on, causing the current fall to zero. Other is the switch of LSB will turn off after MSB turn, causing the current rise to high. Finally, the most popular way to reduce glitches is to modify some or all of the digital code from a binary code to a thermometer code.

Ideally, the voltage at the output nodes of the current sources should be constant. Examples of the sources of error are the parasitic capacitances shown in the current steering cell in Fig. 3.7. However, the voltage on the drain of the current source undergoes significant fluctuations when the current cell is switched. Due to the parasitic capacitance at the drain node , C_1, and due to the finite output impedance of the current source, the voltage on this node settles to its final value sometime after the inputs to the cell finish their transitions. This voltage variation induces variation in the cell current not only due to the channel-length modulation of the PMOS current source, but also due to the current needed to charge and discharge C_1. Moreover, the perturbation of the cell current is a function of the output voltage level because of channel-length modulation in the differential pair transistors, which in turn introduces harmonic distortion into the signal. In order to reduce the impact of the error on the D/A output, C_1 should be made as small as possible.

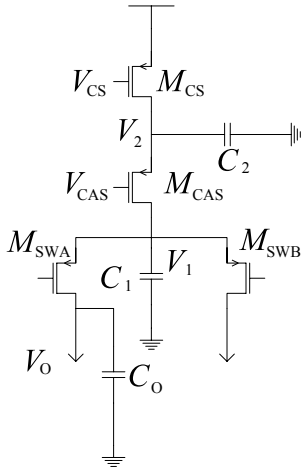
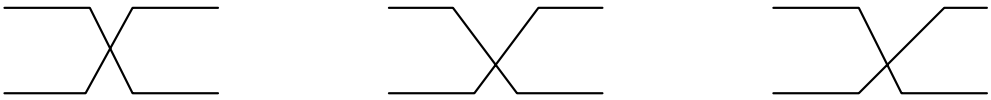


Fig. 3.7 The Parasitic Capacitances in the Current Steering Cell

These circuits have been proposed that limit the voltage fluctuation, by ensuring that the two switching transistors are never simultaneously switched off. This design criterion turns out to have an important positive impact on the dynamic characteristics of the DAC because any asymmetry in the output lines of each current cell give rise to a glitch at the DAC output during a code transition. The correct timing of the switching control signals is thus of crucial importance because it reduces simultaneously the voltage swing at the internal nodes and the amplitude of the glitch.

This circuit put one switching transistor at the threshold of conducting by lowering the crossing point of the switching control signals, so that as soon as one of the switching transistors begins to switch off, the complementary switching transistor begins to switch on. Two different alternatives have been proposed: (1) circuits the use different rise/fall times [21] and (2) circuits that introduce a delay in one of the transitions [6] [8]. Both classes of circuits have a high switching speed. Fig. 3.8 shows the waveform of crossing point of the switching driver. Fig. 3.8 (a) shows the middle crossing point that both the switching transistors may be off at the same time. Fig. 3.8 (b), (c) show the low crossing points that both the switching transistors turn on at the time of transition for using different types of switching drivers, as

mentioned above.



(a) (b) (c)

Fig. 3.8 The Output Waveforms of Switch Drivers the Current Cell

(a) Middle Crossing Points (b) Low Crossing Points Due to Use the Driver of Intrinsic Delay (c) Low Crossing Points Due to Use the Driver of Rise / Fall Time

3.4 Clock Jitter

Jitter in the clock that strobes the synchronization of the switching driver used for driving the current cell can significantly degrade the performance of the current steering DAC. The digital data to the switch signal is aligned globally with a latch to reduce the time skew. Therefore, a good clock distribution is needed. Fig. 3.9 shows a tree structure with clock-distribution approaches, which is suitable for high speed and high accuracy. The clock trees improve the skew to a single- line clock distribution.

Since the jitter assed to a clock signal inside the chip increases linearity with the buffer stages used to generate the clock, it is important to minimize the number of buffers used to generate the clock signal that drives the sensitive synchronization flip-flops. Besides, an on-chip PLL can be designed for a DAC since a clock source with low jitter needed for the DAC can be exported more easily by PLL circuits than an external clock source.

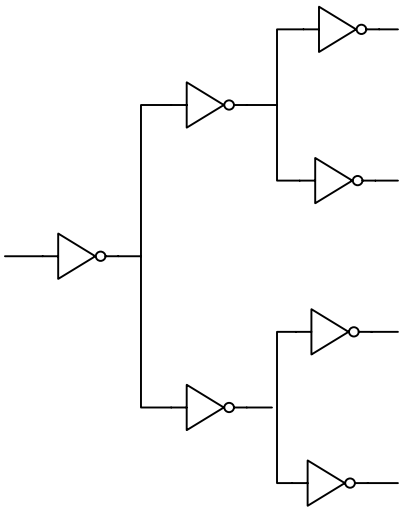


Figure 3.9 Clock Tree Structure

3.5 Summary

The nonidealities of current steering DAC is discussed in this chapter, including finite output impedance of current source, current source mismatch, nonidealities due to switching in current cells, and clock jitter. In order to design a high-speed and high-resolution current steering DAC, we should pay more attention to these nonidealities. The approaches to improve the nonidealities are also mentioned in this chapter.

Chapter 4

DAC Circuit Design

In this chapter, the designed architecture of a 12-bit 500-MSamples/s current–steering CMOS D/A converter is introduced at first. Then each block of the DAC is presented and the circuit design is discussed. To design a high speed and high resolution DAC, we should pay more attentions to choose the proper architecture that can achieve a balance between good static and dynamic specifications versus a reasonable circuit power, area, and complexity. Besides, special layout technique is also presented to compensate the systematic and gradient errors, as mentioned in chapter 3.

4.1 The Architecture of DAC

Base on the discussions of different architectures of DACs, we choose the segmented architecture because this architecture can get a compromise between static and dynamic performance. Fig. 4.1 shows the overview of the specifications of thermometer coded, binary weighted, and segmented implementations of current steering DAC. The binary weighted architecture has advantages of small area, low power consumption and less complexity. However, this architecture has large DNL error, glitch energy and not guaranteed monotonicity, which will degrade the performance of the DAC. The thermometer coded architecture has a contrary advantages and disadvantages to the binary weighted architecture. To keep the advantages of both binary weighted and thermometer coded architectures, segmented architecture is a good candidate and is used in this thesis.

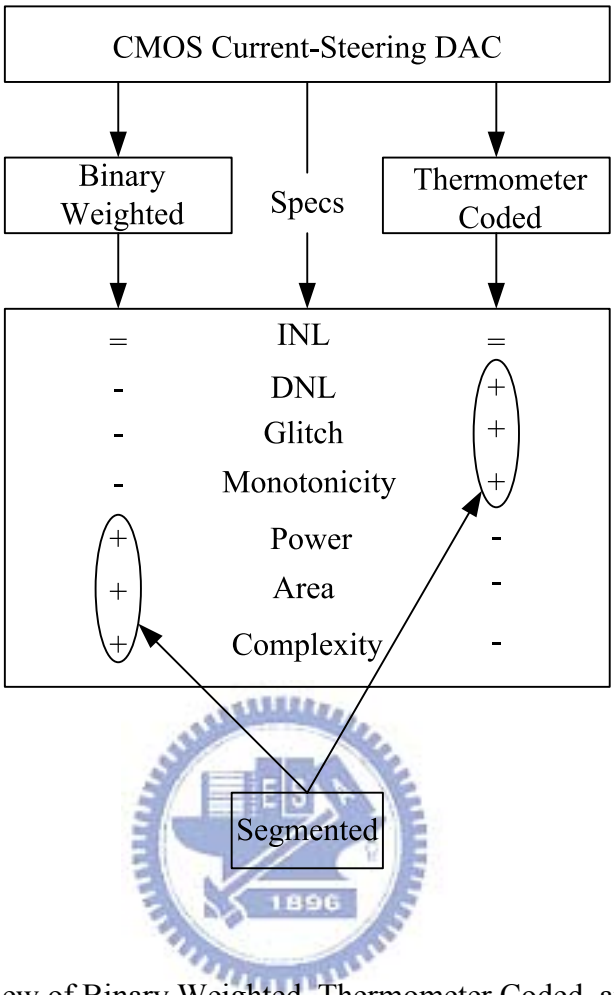


Figure 4.1 Overview of Binary Weighted, Thermometer Coded, and Segmented Implementations

The architecture of a 12-bit 500-MSamples/s current–steering CMOS D/A converter presented in this thesis is shown in Fig. 4.2. There are several blocks in this DAC, including digital circuits, latches, current cells, and bias circuit. The input binary codes are either processed through digital circuits, then changed to thermometer codes (A11 – A4) or simply equally delayed (A3 – A0). The processed signals then pass through the latches to keep synchronization used for driving switches of the current cells. In addition to synchronization, the latches can also reduce the glitch effect due to the drain voltage fluctuations of current sources. Finally, the current cell matrix can provide differential output currents controlled by

the switches whose input signals have been synchronized. In the following, all the sub-circuitry of this DAC will be further discussed.

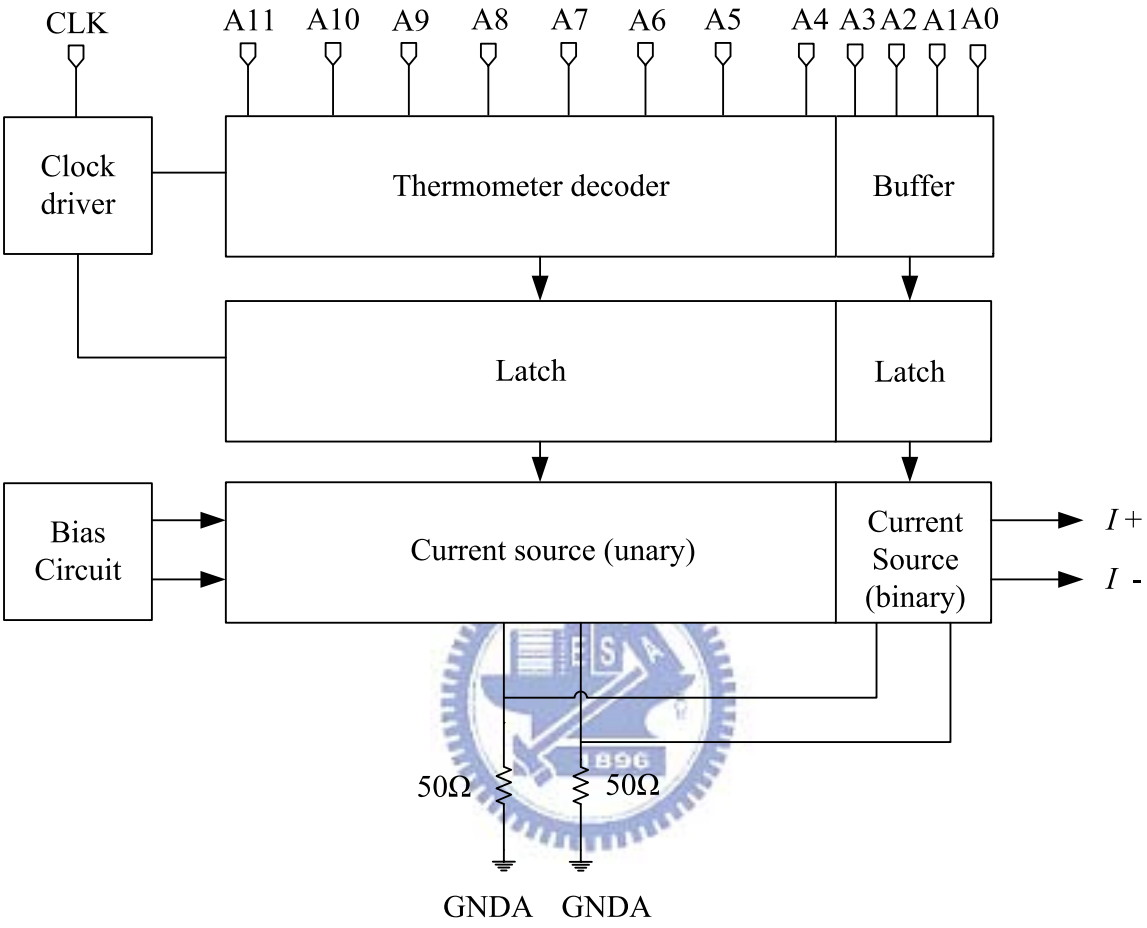


Fig. 4.2 Block Diagram and Floorplan of the Segmented 12-bit DAC

4.2 Digital Circuits

In a segmented current-steering DAC, the function of the digital circuits it to convert the binary code to either thermometer code or only delayed the binary code. To design the digital circuits, several issues should be taken into account:

- High speed operation
- Circuit complexity
- Power consumption

From the issues, several compromises between decoder architecture, coding scheme and circuit implementation of digital circuits should be considered carefully.

In order to use the segmented architecture, we should determine the number of bits for MSB's and LSB's that are thermometer decoded and delay equalized, individually. To achieve a good DNL specification and glitch energy, the number of bits implemented in the binary weighted part of the DAC has to be small. However the number of output lines of the thermometer encoder increases with 2^N where N is the number of bits, resulting in complex logic and large input capacitance. A direct consequence is often a reduction in the maximum operating speed. Equally important is the fact that the area used by the decoding and interconnections inside the matrix increases, and consequently the process and electric systematic errors become more difficult to compensate [6]. So the DAC has a 8 + 4 segmented architecture: first, the eight most significant bits (MSB's) are linearly decoded; second, the four least significant bits (LSB's) are binary weighted.

4.2.1 Thermometer decoder

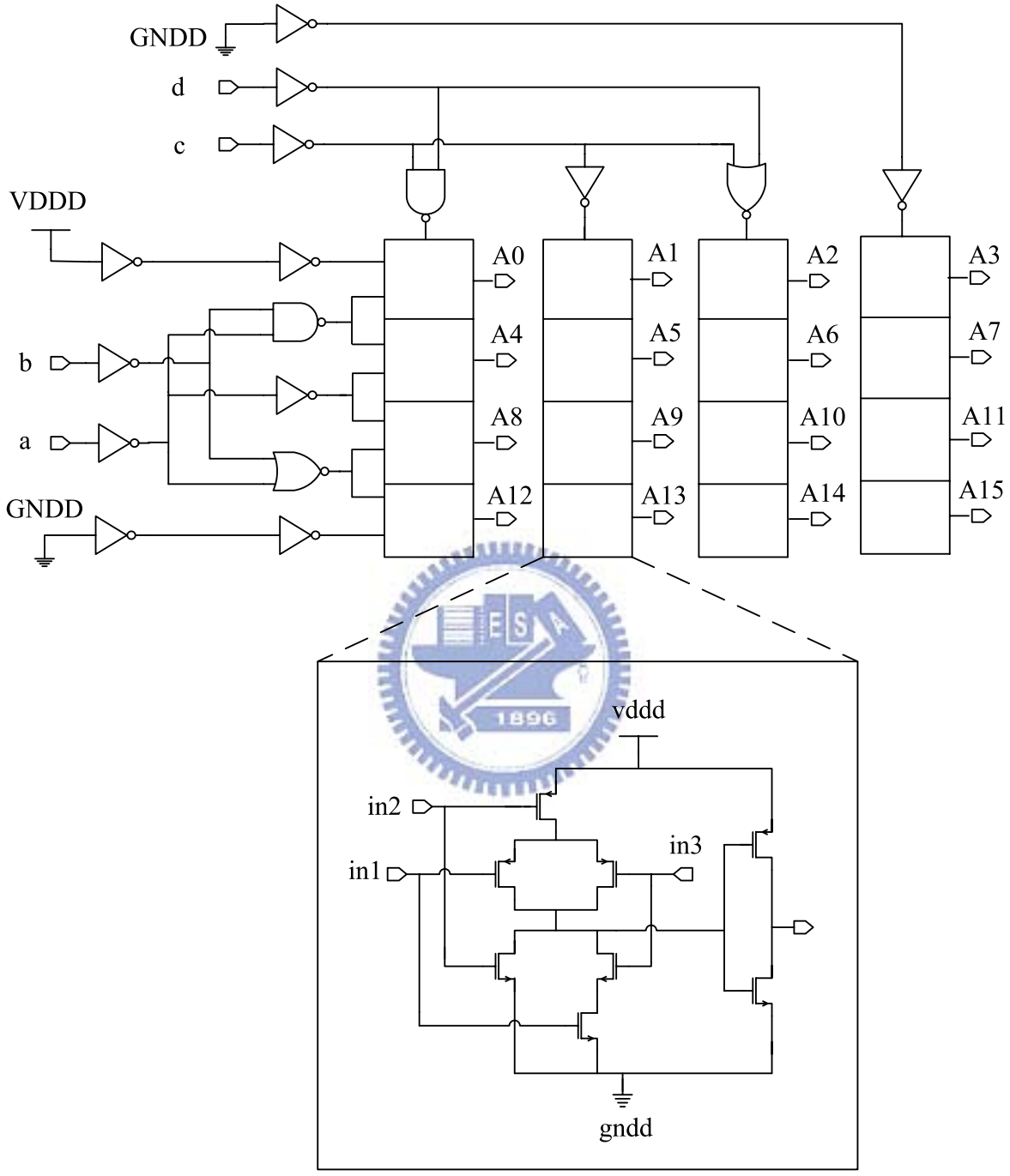


Fig. 4.3 The 4-bit thermometer decoder logic

From the Fig. 4.2, the system block diagram reveals that one kind of 8-bit thermometer decoder is essential. The 8-bit thermometer decoder is divided into tow 4-bit thermometer

decoder. Row-column selection decoding is a simple method to supply high speed transformation [6]. In high speed realization, the adopted decoder can limit the clock rate of the D/A converter. Fig. 4.3 shows the row-column selection decoding methodology. Two 4-bit thermometer decoder forms the major part of the 8-bit thermometer decoder in Fig. 4.4.

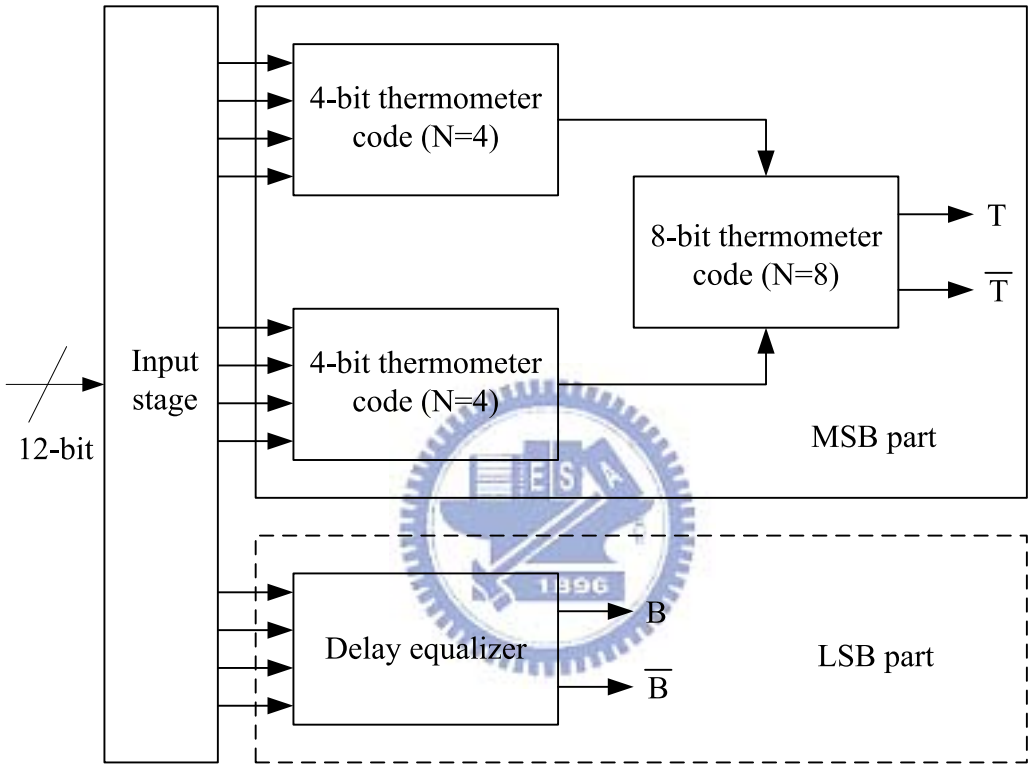


Fig. 4.4 The Digital Circuit used in the DAC

4.2.2 High speed latch

The dynamic performance degradation of a current-steering DAC can be caused by several reasons associated with current source switching. Some important issues that have been identified to cause dynamic limitations are :

- Imperfect synchronization of the control signals at the switches.

- Drain-voltage variations of the current-source transistors caused by the fact that both switch transistors are simultaneously in the off state.
- Coupling of the control signals through the C_{gd} of the switches to the output.

To minimize the three effects, a well-designed synchronized driver is used. The high speed, low glitch latch is illustrated in Fig. 4.5(a). It provides two complementary signals needed at the input of the current switches.

In the conventional latch, both switches will be off for a short period. As a result, the capacitance at the drain of the current source transistor will be charged and then the current source will turn off. To recover the normal operation, the current source must progress through the linear region and back into saturation. Hence, turning off the current source not only slows down the speed but also increases glitch at the output. To solve the problem, the function of this latch is designed to shift down the crossing point of the differential signals used for driving the switches of the current cell.

The latch used here is a rise/fall time based driver. In order to obtain instantaneous change for output node with falling input, extra PMOS transistors (M1 and M2) are placed in parallel with each other cross-coupled at the top of the circuit. When the transitions of input signals (high → low or low → high) occur, the transistors M3-M10 will immediately change their states. However, the crossed-coupled PMOS transistors M1 and M2 will hold their states for a short period. After these transistors change their states, the charging speed will be increased. Thus, the combination of the (μ_n / μ_p) scaled PMOS transistors and the PMOS positive feedback loop results in the rise time that is much faster than the fall time of the driver circuit. Due to the use of two additional inverters at the output of the driver and properly sizing the transistors of the whole latch, a lower crossing point can be realized. Fig. 2 (b) shows the voltage waveforms of the differential outputs, Q and $\overline{Q}$. This latch not only performs the final synchronization of the signals used for switching different current cells but

also reduces the delay between the different digital decoders.

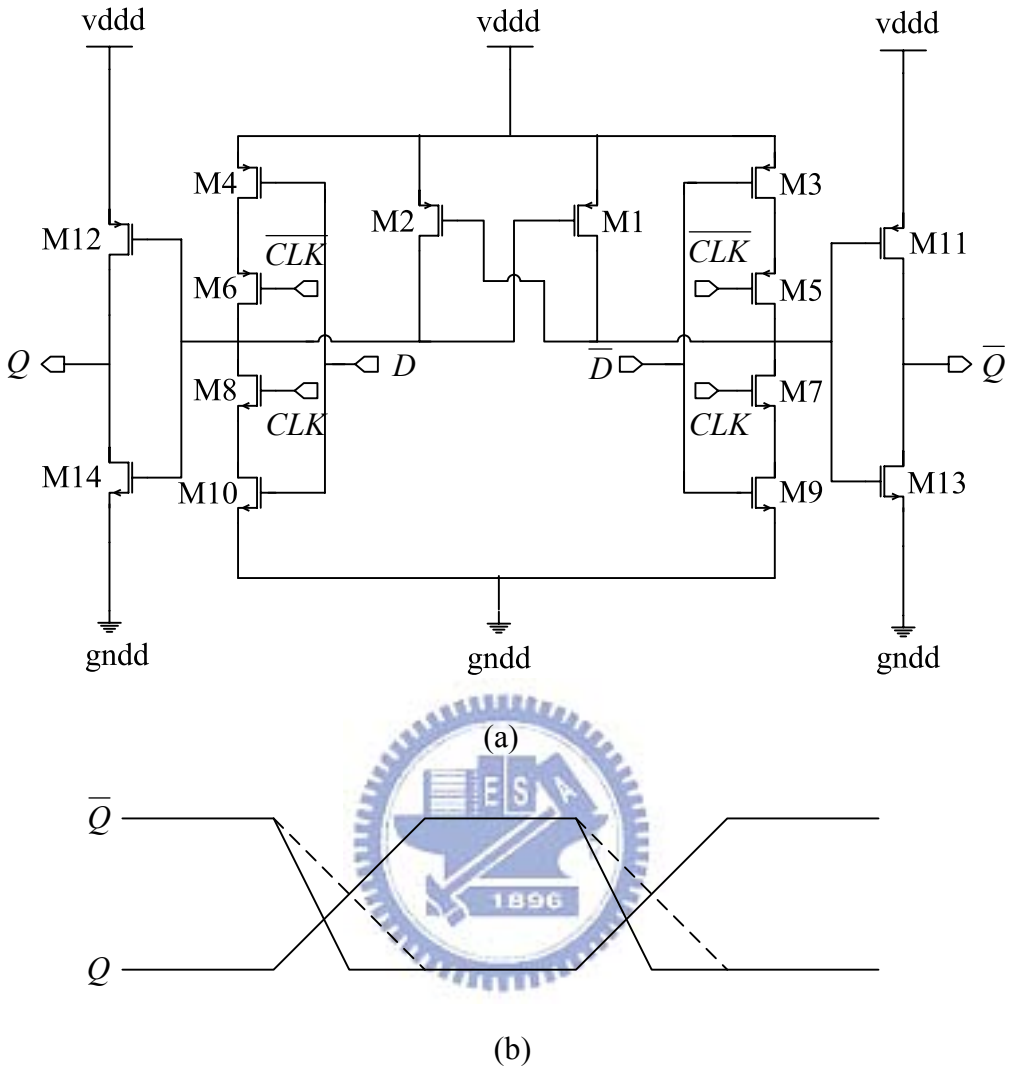


Fig. 4.5 (a) Dynamic Latch Schematic Diagram (b) Output Signals

4.3 Analog Circuits

To generate the accurate current, several concerns should be taken into account. First, the size of the current sources should be properly designed to reduce the mismatch error between different current sources due to the fabrication. Second, the finite output impedance of each current source is designed large enough to get a good static performance. Finally, a bias circuit used to generate the bias current of current source is also required. The design

considerations and circuit implementation of each circuit is described in next subsections.

4.3.1 Implementation of Switch Unit Current Cell

The PMOS current source has two advantages. PMOS devices built in n-well are thus shielded from the substrate. PMOS has less flicker noise than NMOS. The circuit schematic of the cascode switch current cell is shown in Fig. 4.6. The output impedance of the current source which is $r_{o1} + r_{o2} \cdot (1 + g_{m1} \cdot r_{o1})$ is very large.

In the following content, we will continue to find out what size of current source transistor should be used. Design flow of the current cell's size is shown in Fig. 4.7. If we want to decide the size of the current cell, we need INL_yield , process parameter (A_β and A_{VT}), and gate overdrive voltage (V_{GS}-V_T) . We also need to consider DAC specification, including INL and SFDR.

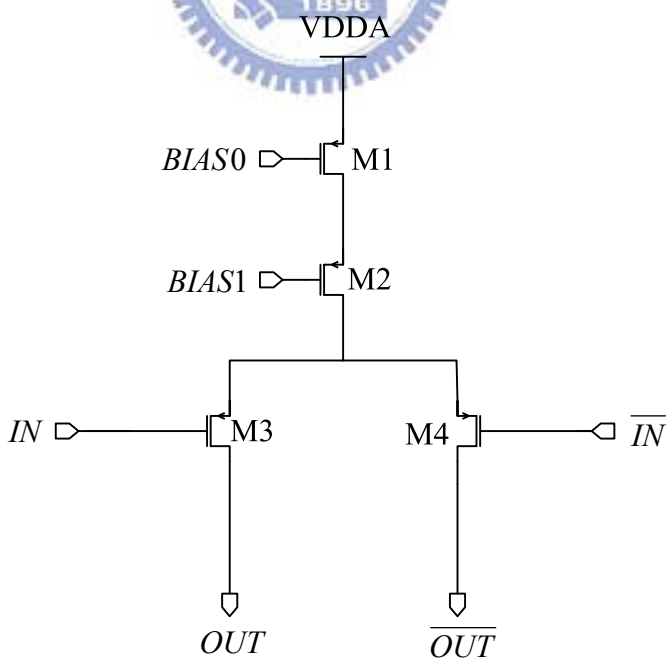


Fig. 4.6 The circuit schematic of cascode switch current cell

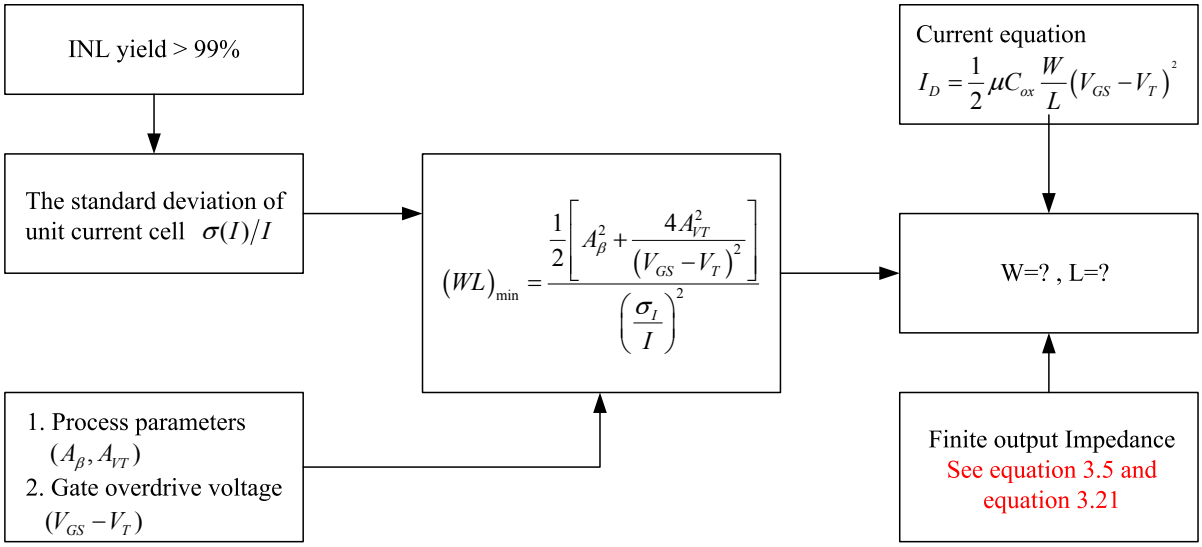


Fig. 4.7 Design flow of the current cell's size

There was discussion of spatial errors in current source array in the former section. Actually it is convenient to distinguish these errors by two parts: one is systematical error and the other is random error. These errors can disturb the static accuracy and dynamic performance of D/A converter. Generally speaking, systematical error can be subdivided into four kinds:

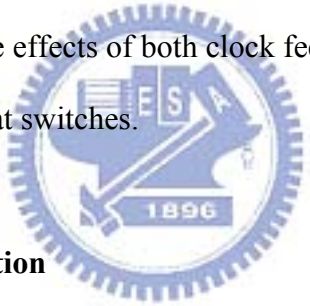
- Process gradients
- Voltage drops in the supply line
- Thermal gradients
- Output impedance of the current source

The switching scheme was to average the spatial errors in the current source array caused by process gradients. It also suppressed the nonlinearity contributed by thermal gradients. The residues are left for the following sections. So turn back our attention on our topic of this section: How random errors degrade the accuracy of our designs? According to

[14], the identical device with the same size and similar geometry was suffered random mismatch due to the fabrication in real world.

For a current-steering DAC, the INL is mainly determined by the matching behavior of the current sources. A parameter that is well suited for expressing this technology versus DAC specification relation is the INL_yield. This yield figure is defined as the percentage of functional D/A converters with an INL specification smaller than half an LSB (least significant bit).

Finite output impedance is also an error source that will cause performance degradation of the current-steering DAC. Base on the analysis in section 3.1, we can design the proper current source output impedance to get both good static and dynamic performance. From Fig. 4.7, we can find that in order to meet the specification .Also, the size of the switches should be as small as possible to avoid the effects of both clock feedthrough and charge injection during the transition of the signal at switches.



4.3.2 Reference Current Generation

Fig. 4.8 shows the biasing scheme for the cascode current sources. An external resistor, R , is used to generate the reference current. The NMOS sections of the biasing circuits are labeled as “global biasing” while the PMOS sections are labeled as “local biasing.” The cascode current mirror in the current cell can be used to reduce short-channel effects and increase the output impedance, but it will limit the signal swing. In order to reduce this limitation, a wide-swing cascode current mirror bias scheme is shown in “local biasing” of Fig. 4.8.

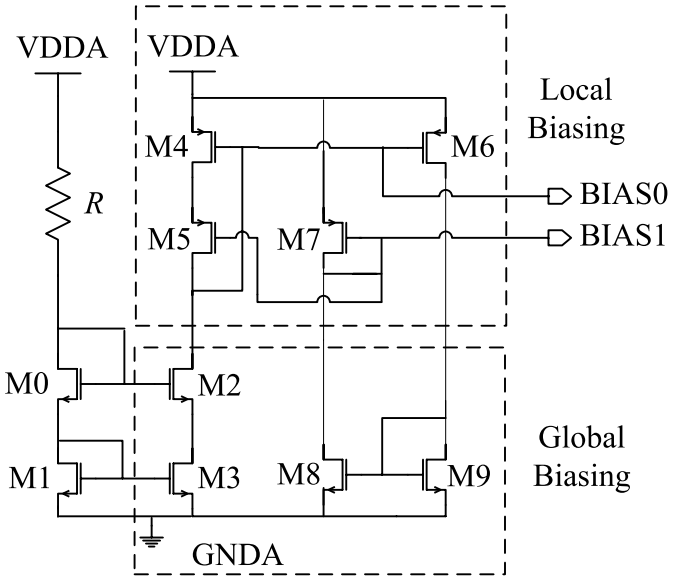


Fig 4.8 The Circuit Schematic of the Bias Circuit

4.4 Layout

d	d	d	d	d	d	d	d				d	d	d	d	d	d	d	d
d	d	d	d	d	d				4				d	d	d	d	d	d
d	d	d					36	76		100	32					d	d	d
d	d	d		16	112	96	57				53	85	104	20		d	d	d
d	d		40	64					22					45	12		d	d
d	d		88			14	94	110	42	78	103	31			108		d	d
d			72		46	62	74	106	2	99	67	54	39		68			d
d		24	116		118	83	26				58	19	87		29	48		d
		93			70	50			0			90	115			80		
	9			6	34	10		60		61		11	35	7			8	
		81			114	91			1			51	71			92		
d		49	28		86	18	59				27	82	119		117	25		d
d			69		38	55	66	98	3	107	75	63	47		73			d
d	d		109			30	102	79	43	111	95	15			89		d	d
d	d		13	44					23					65	41		d	d
d	d	d		21	105	84	52				56	97	113	17		d	d	d
d	d	d					33	101		77	37					d	d	d
d	d	d	d	d	d				5			d	d	d	d	d	d	
d	d	d	d	d	d	d	d				d	d	d	d	d	d	d	d

Fig. 4.9 Improved “ balanced ring ” technique of this work for reduction of quadratic errors (a) rings (1 and 6) versus rings (3 and 4)

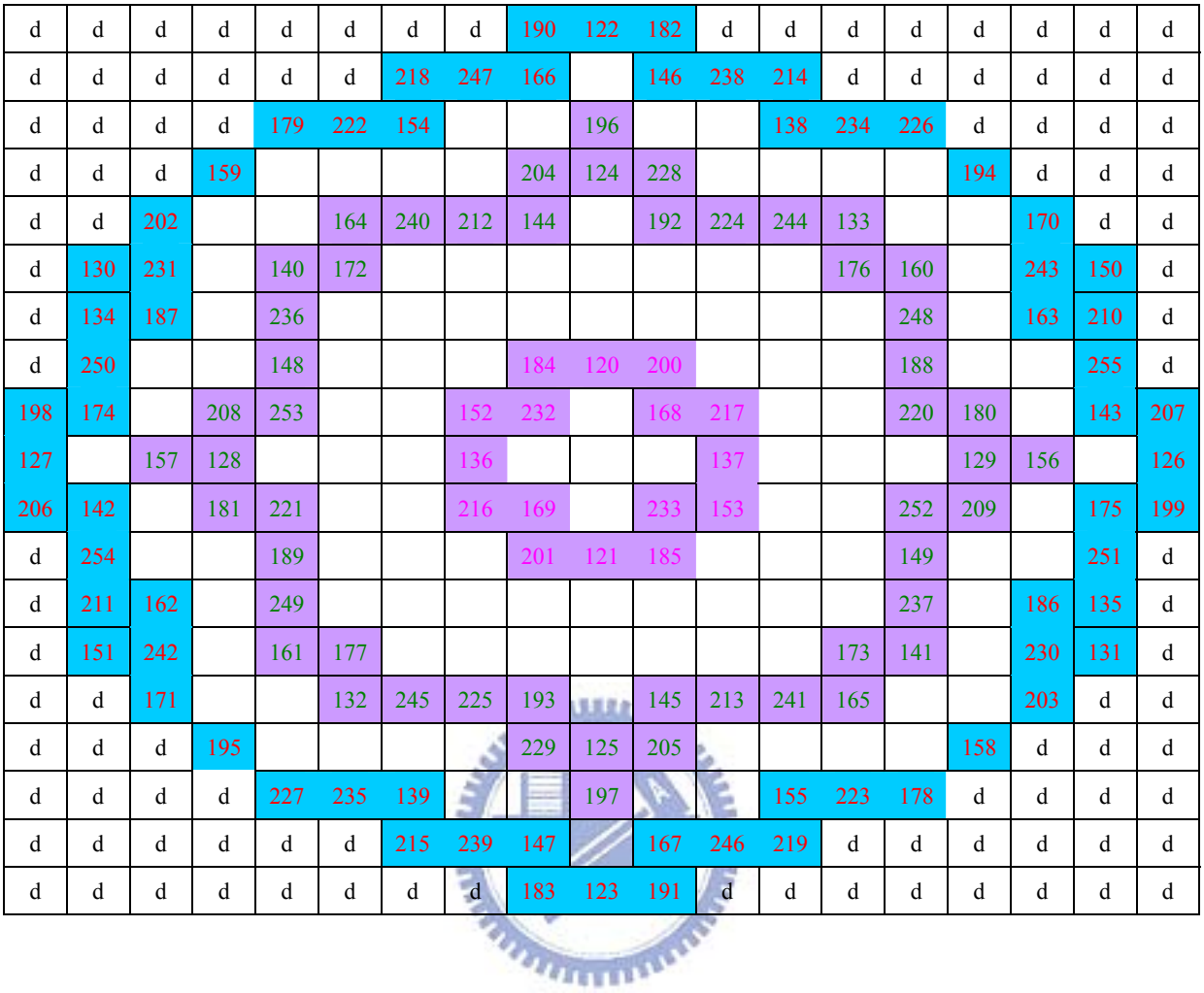


Fig. 4.9 Improved “ balanced ring ” technique of this work for reduction of quadratic errors (b) rings (2 and 5) versus rings (7)

d	d	d	d	d	d	d	d	190	122	182	d	d	d	d	d	d	d	d
d	d	d	d	d	d	218	247	166	4	146	238	214	d	d	d	d	d	d
d	d	d	d	179	222	154	36	76	196	100	32	138	234	226	d	d	d	d
d	d	d	159	16	112	96	57	204	124	228	53	85	104	20	194	d	d	d
d	d	202	40	64	164	240	212	144	22	192	224	244	133	45	12	170	d	d
d	130	231	88	140	172	14	94	110	42	78	103	31	176	160	108	243	150	d
d	134	187	72	236	46	62	74	106	2	99	67	54	39	248	68	163	210	d
d	250	24	116	148	118	83	26	184	120	200	58	19	87	188	29	48	255	d
198	174	93	208	253	70	50	152	232	0	168	217	90	115	220	180	80	143	207
127	9	157	128	6	34	10	136	60		61	137	11	35	7	129	156	8	126
206	142	81	181	221	114	91	216	169	1	233	153	51	71	252	209	92	175	199
d	254	49	28	189	86	18	59	201	121	185	27	82	119	149	117	25	251	d
d	211	162	69	249	38	55	66	98	3	107	75	63	47	237	73	186	135	d
d	151	242	109	161	177	30	102	79	43	111	95	15	173	141	89	230	151	d
d	d	171	13	44	132	245	225	193	23	145	213	241	165	65	41	203	d	d
d	d	d	195	21	105	84	52	229	125	205	56	97	113	17	158	d	d	d
d	d	d	d	227	235	139	33	101	197	77	37	155	223	178	d	d	d	d
d	d	d	d	d	d	215	239	147	5	167	246	219	d	d	d	d	d	d
d	d	d	d	d	d	d	d	183	123	191	d	d	d	d	d	d	d	d

Fig. 4.10 Selection sequence for MSB part of input code for improved “balanced-ring” technique in Fig. 4.9

The layout of the DAC plays an important role since the random mismatch of current source due to process variation will degrade the accuracy of the DAC significantly. Thus we should pay mode attention to the floor plan of the DAC and special layout technique should be used, like [6] , [8] and [10] . To compensate for symmetrical and graded errors caused by temperature, process, and electrical gradients, special switching schemes should be implemented.

In this design a floor plan of current cell matrix called improved “Balanced-ring” is used, as shown in Fig. 4.10. In the improved “balanced-ring” technique, the array is

subdivided into rings as shown by rings 1 to 7. First, we add up the quadratic errors of the cells within each ring. Then, starting from the ring 1 and 6, we determine how many of the ring 3 and 4 are required to cancel the error in ring 1 and ring 6. It turns out that four inner rings will do the job as shown in Fig. 4.9(a). Proceeding the same way for the remaining rings results in the selection of rings 2 and 5 for ring 7, is seen in Fig. 4.9(b). Now in each step we select the cells from counterpart rings (e.g., ring 1 and 6 versus rings 3 and 4) in a way that avoids accumulation of quadratic errors, as described above. Of course all these selections also obey the procedure.

Dummy cells and bias circuits can be placed in the "d" cell matrix. But additional rows or columns of dummy current source will not cause significant area increase of the current cell matrix.

The digital part of the DAC is placed on the left and the current cell matrix is placed on the right. To minimize the systematic error introduced by the voltage drop in the ground lines of the current-source transistors, wide sheets of metal have been used. Special care has been taken to realize a symmetrical interconnection array in order not to degree the matching performance. The power domains were separated into three parts: analog, digital and guard ring to avoid the analog section disturbed by the transient current of logic switching. The pins for ground and output were assigned more than one because of reducing the *IR* drop effect and parasitic inductance. In the current source array, dummy cells were adopted to lower the edge effect and can be treated as decoupling capacitor on the sensitive bias nodes. They are created by dummy transistor with body, source and drain all connected.

The chip will be fabricated with TSMC 0.18 μm mixed signal technology. The final layout was shown in the Fig. 4.11. These numbers in the graph means the pin orientation in the package. The active die size only has 1.615 μm^2.

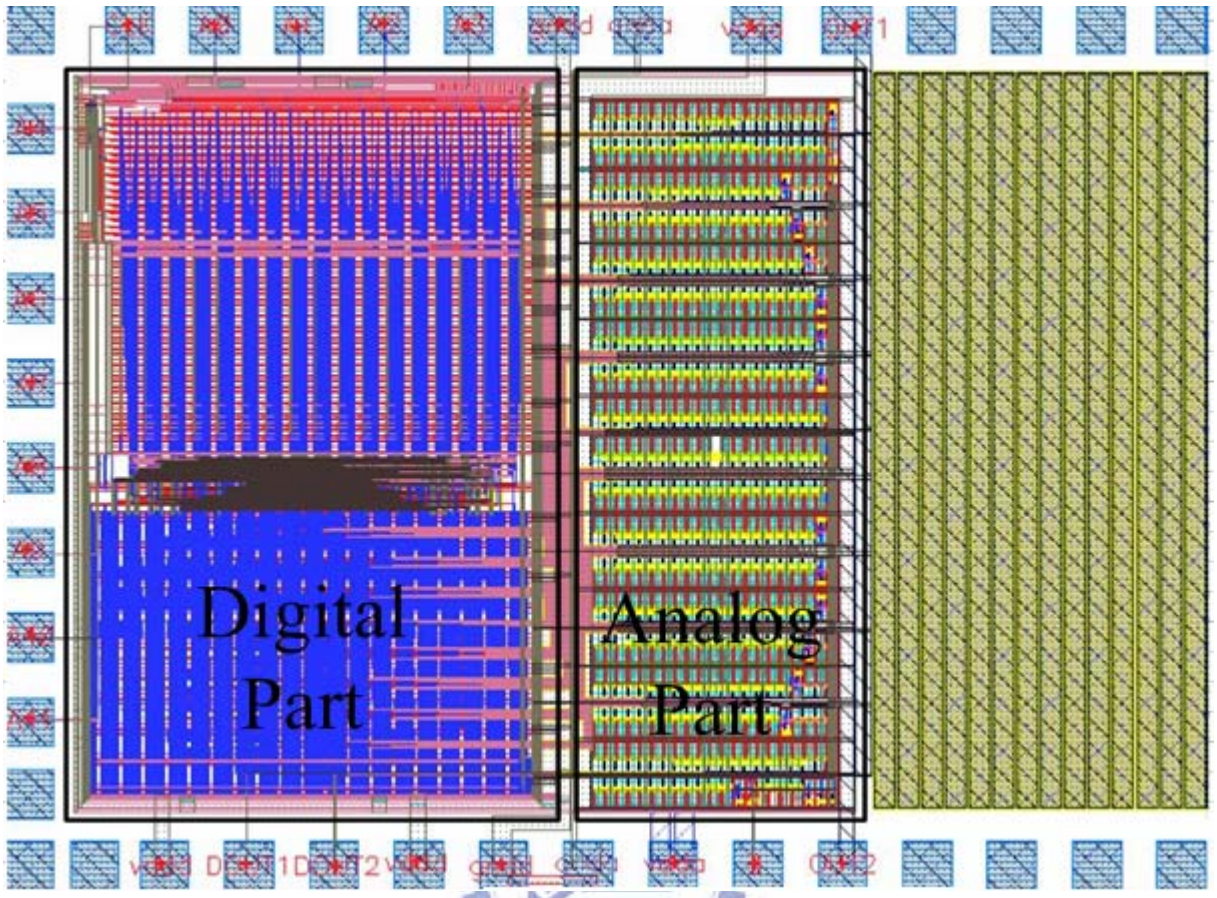


Fig. 4.11 The Final Layout

4.5 Summary

A 12-bit 500-MSamples/s current–steering CMOS D/A converter is designed in this chapter. The architecture is shown first. Then, the design consideration and circuit diagram of each sub-block is described in each section. Finally, the layout concern and the switching scheme of current cell matrix have also been discussed. Since the DAC has been designed, the simulation and result of this DAC should also be presented to test the performance. This will be done in the next chapter.

Chapter 5

Simulation and Measurement Results

This current DAC has been designed and laid out by using the TSMC 0.18 μm CMOS Mixed-Signal process with one poly and six mentals. In this chapter, we present simulation resultant and the testing environment. The measured results are presented in this chapter, too.

5.1 Simulation results

The major target specification for SFDR of this paper, a 12-bit 500-MSample/s D/A converter, is 60 dB for signal frequencies up to 170 MHz. An additional design goal was to derive maximum benefit from this relatively advanced technology.

The sample rate is set to 500MHz at input frequency 1.46 MHz, 10.25 MHz, 38.57 MHz, 49.32 MHz, 72.75 MHz, 96.19 MHz, 110.84 MHz and 171.39 MHz, respectively. A simulate sine wave spectrum for F_s = 500 MHz and F_{sig} = 110.84 MHz is shown in Fig. 5.1. A simulate sine wave spectrum for F_s = 500 MHz and F_{sig} = 171.39 MHz is shown in Fig. 5.2. Fig. 5.3 shows the SFDR of input frequency between 1.46 MHz and 171.39 MHz at the sample rate 500 MHz. The differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in the Fig 5.4. The total simulation result of this DAC is summarized in Table 5-1.

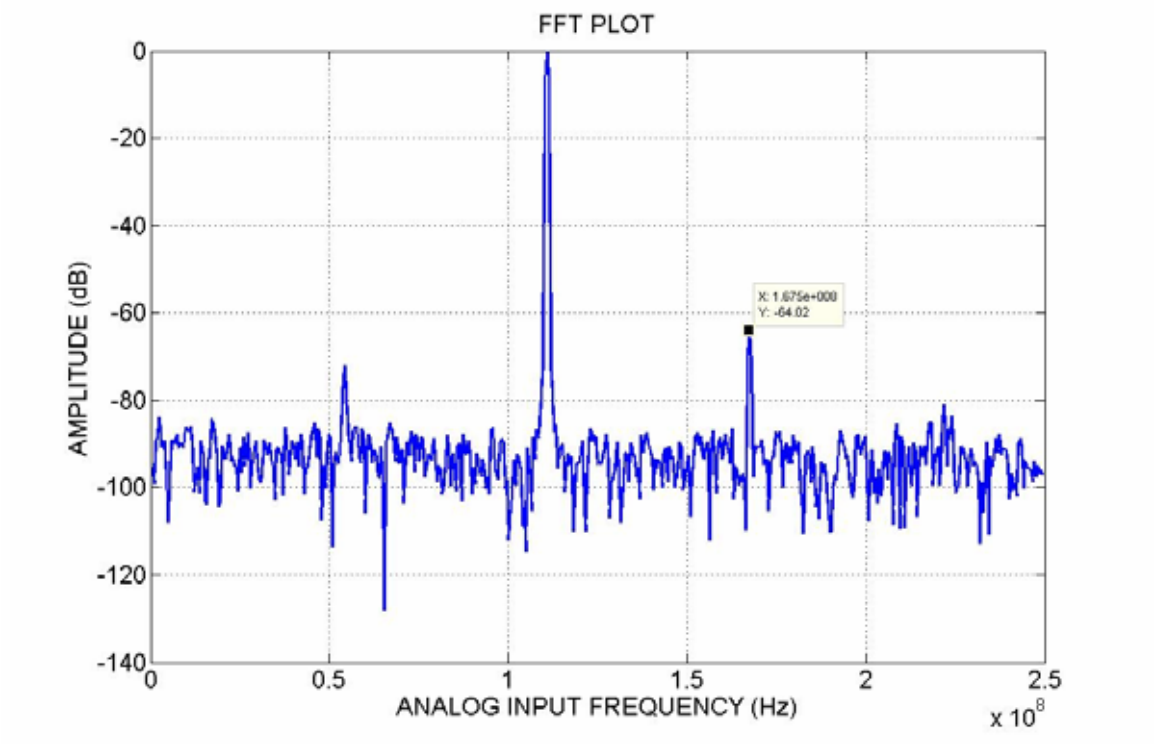


Fig. 5.1 Sine wave spectrum for F_s = 500 MHz and F_{sig} = 110.84 MHz

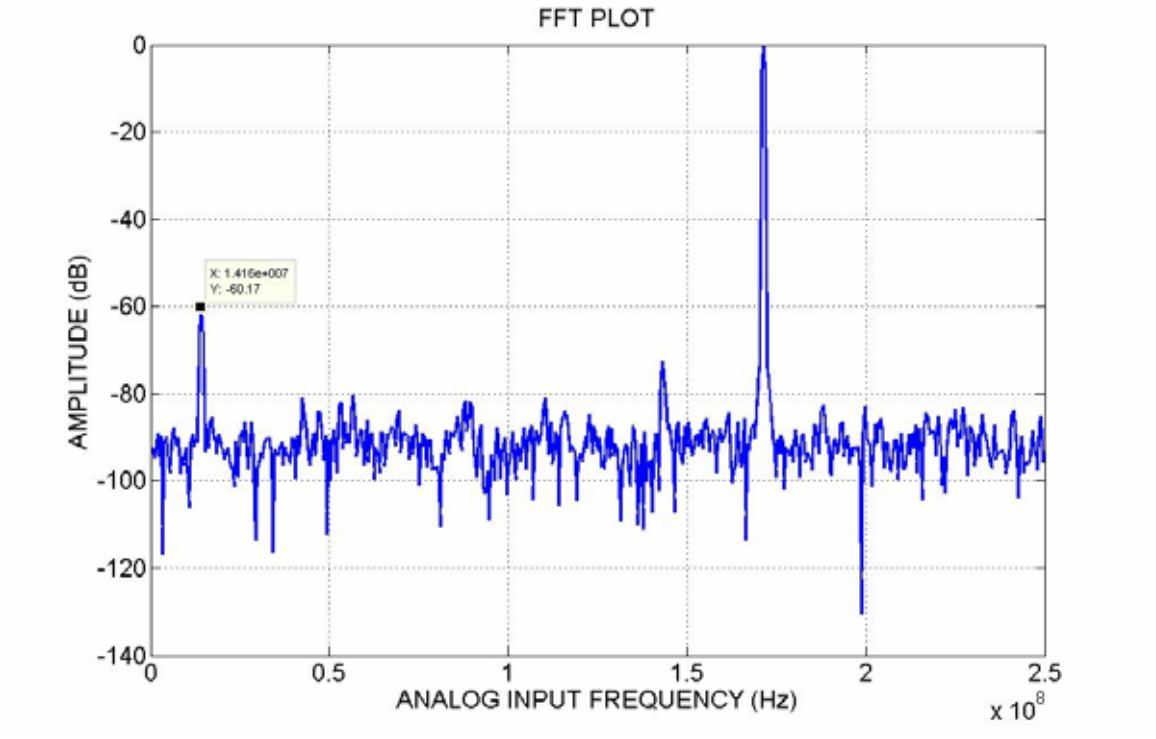


Fig. 5.2 Sine wave spectrum for F_s = 500 MHz and F_{sig} = 171.39 MHz

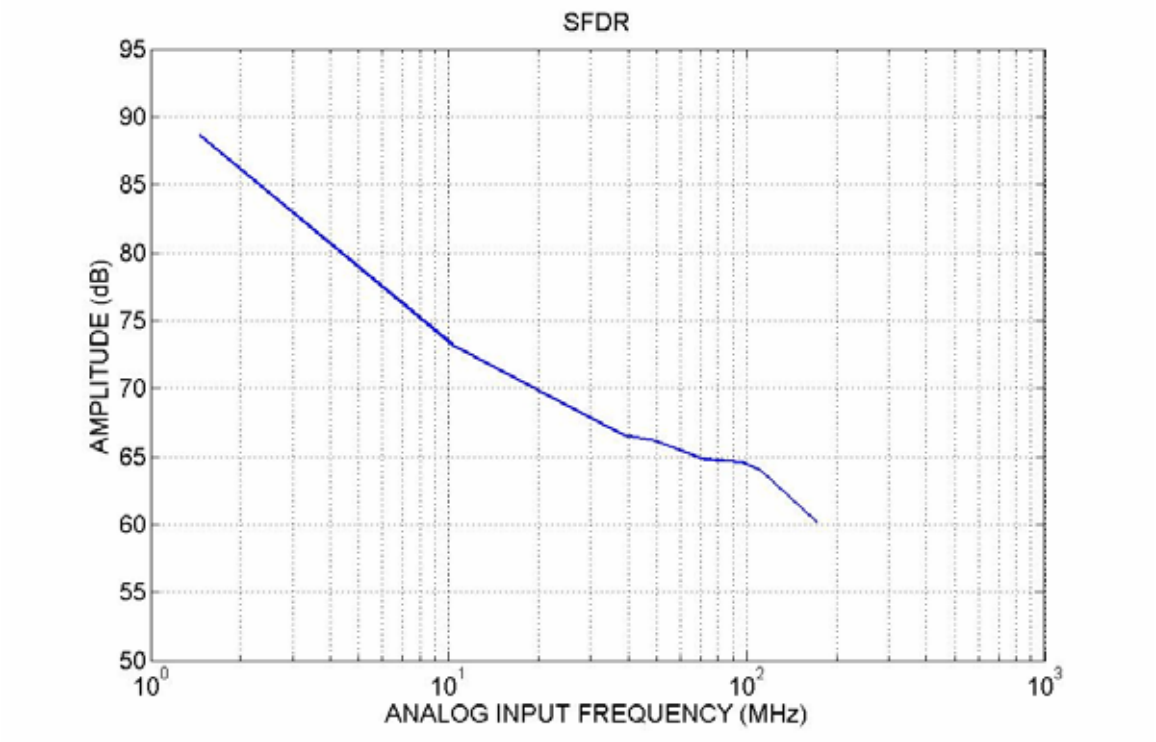


Fig 5.3 The SFDR of input frequency between 1.46 MHz and 171.39 MHz at the sample rate 500 MHz

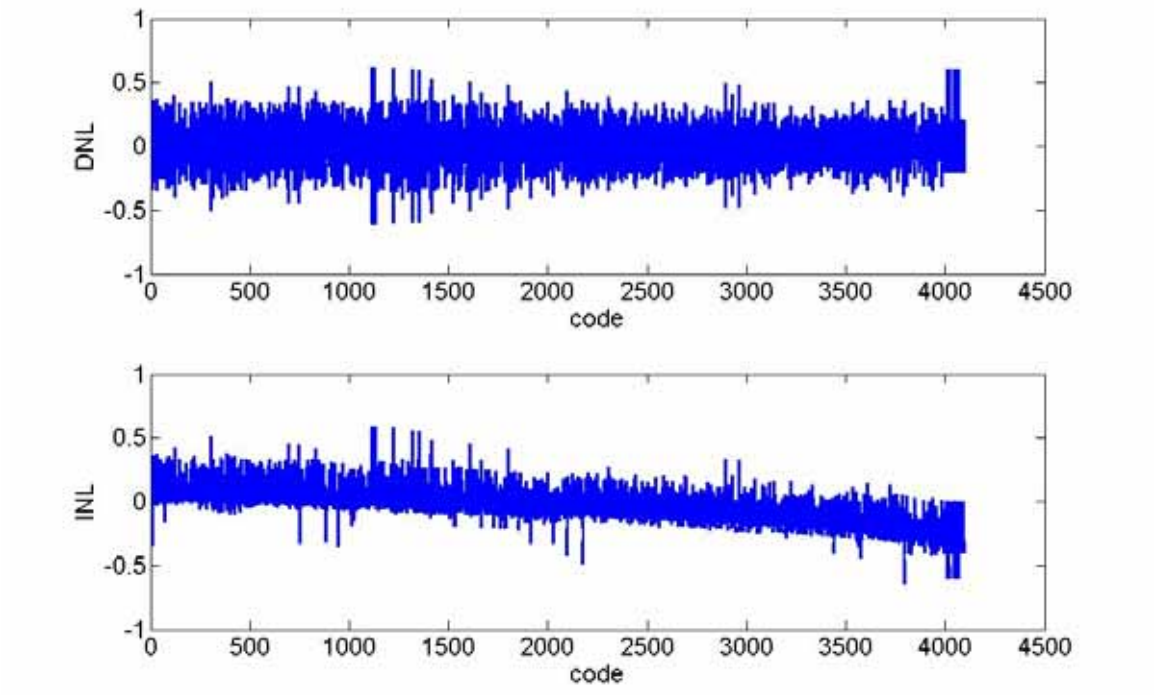


Fig 5.4 The differential nonlinearity (DNL) and integral nonlinearity (INL)

Table 5-1 The total simulation results of this DAC

Process	TSMC 0.18 μm CMOS Mixed-Signal
Supply Voltage	Digital supply 1.8 V Analog supply 3.3 V
Sampling Frequency	500 MHz
DNL	< 0.7 LSB
INL	< 0.7 LSB
SFDR (Fin = 170.39 MHz)	60.1747 dB @ CLK = 500 MHz
Power Dissipation	126 mW
Active Area	1.615 mm^2

5.2 Test Circuits

Fig. 5.5 shows the measurement setup of the overall DAC testing. In the setup, the input digital code is generated by Agilent 16902B Logic analysis System. The differential output of the DAC is converted to a signal-ended output by using an active probe to provide rejection of common mode noise and even order distortion. This signal-ended output is measured by Agilent E4440A 3 Hz-26 GHz PSA Series Spectrum Analyzer to get spectrum performance. The Voltage transient output signals are measured by Agilent 34401 Digital Multimeter. Two precise power supplies are used to generate both analog and digital supply.

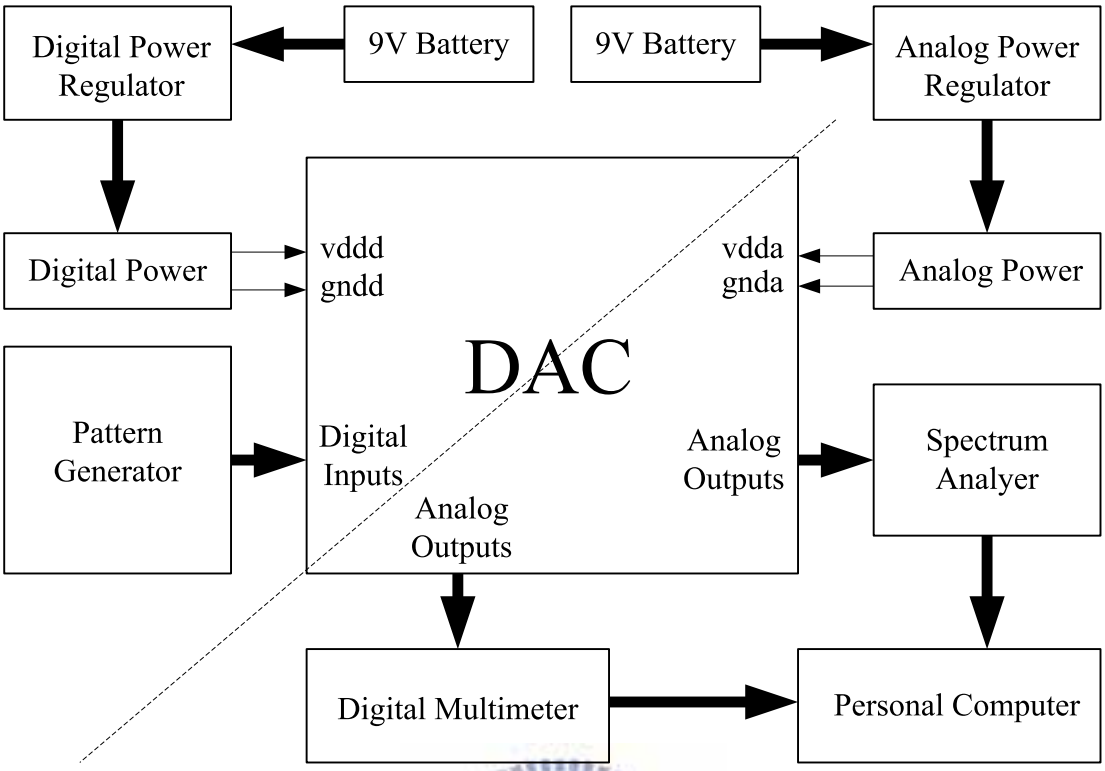


Fig. 5.5 Testing Setup

The analog and digital power supplies are generated by the application of the LM317 adjustable regulators shown in Fig. 5.6. The capacitor C1 is used to improve the ripple rejection and capacitor C2 is the input bypass capacitor. The resistor R1 is the fixed resistor and resistor R2 is the precise variable resistor. The output voltage of the Fig. 5.6 can be expressed as

$$V_{out} = 1.25V \cdot (1 + \frac{R_2}{R_1}) \cdot I_{ADJ} \cdot R_2 \qquad (5.1)$$

Where I_{ADJ} is the DC current that flows out of the adjustment terminal ADJ of the regulator. By the way, the resistor R1 can use the low temperature coefficient of the metal film resistor to get the stable output voltage.

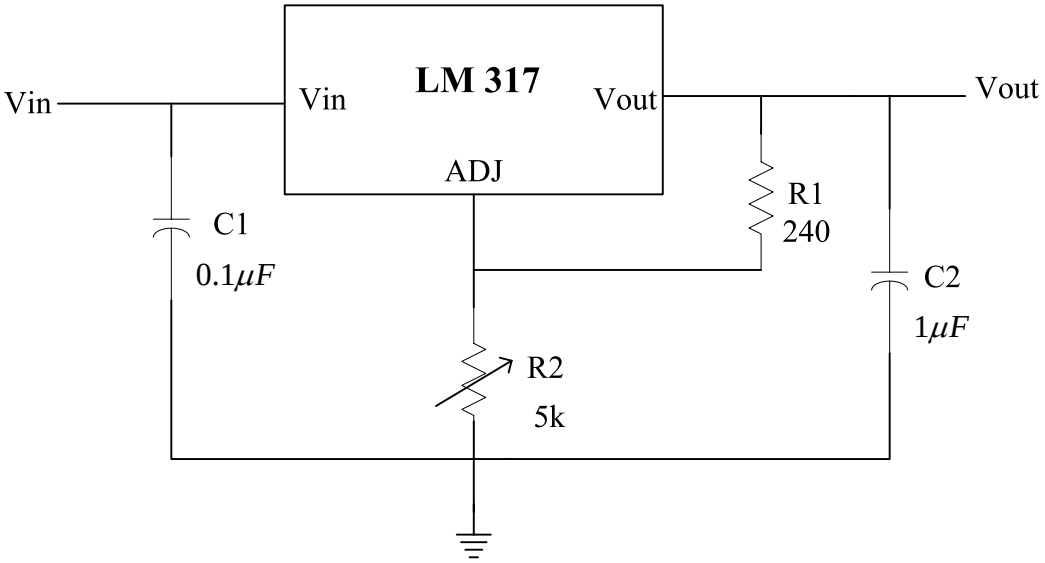


Fig. 5.6 Power Supply Regulator

5.2 Measurement Results

The sample rate is set to 100 MHz at input frequency 3 MHz, 5.17 MHz, 12.83 MHz, 20.67 MHz and 34.33 MHz, respectively. A measured sine wave spectrum for F_s = 100 MHz and F_{sig} = 3 MHz is shown in Fig. 5.7. A measured sine wave spectrum for F_s = 100 MHz and F_{sig} = 5.17 MHz is shown in Fig. 5.8. Fig. 5.9 shows the SFDR of input frequency between 3 MHz and 34.33 MHz at the sample rate 100 MHz. The differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in the Fig 5.10. The total measured result of this DAC is summarized in Table 5-2 and the die microphotograph is shown in Fig. 5.11.

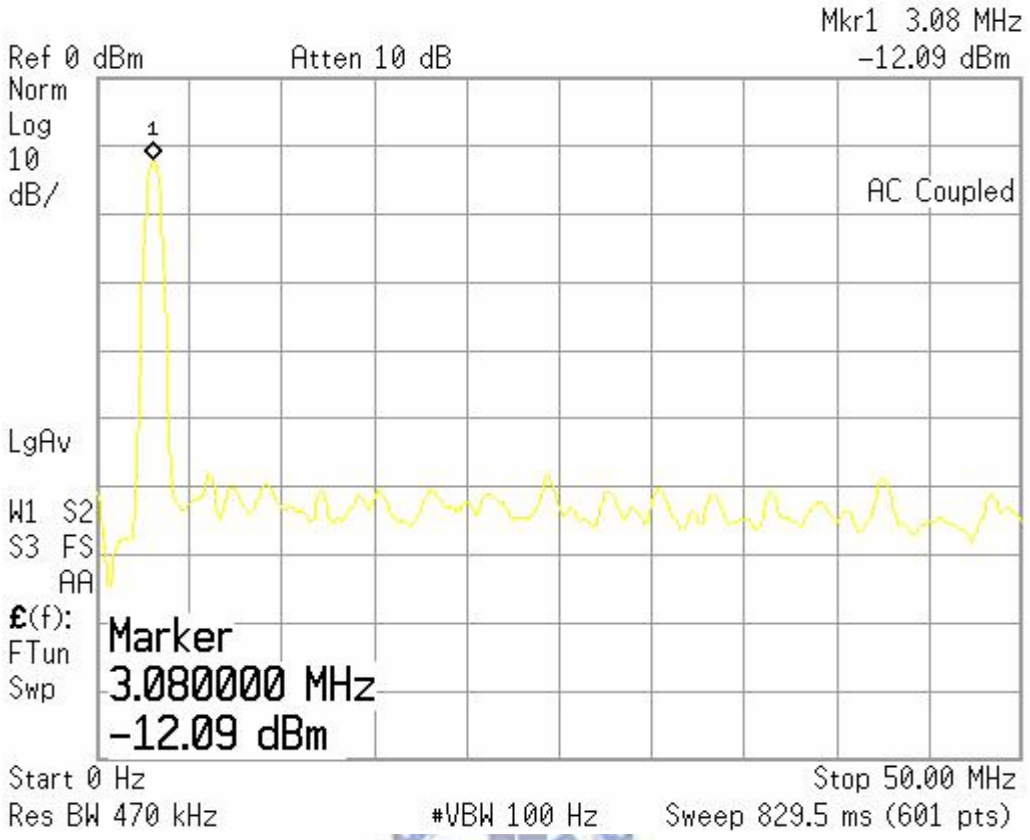


Fig. 5.7 Sine wave spectrum for F_s = 100 MHz and F_{sig} = 3 MHz

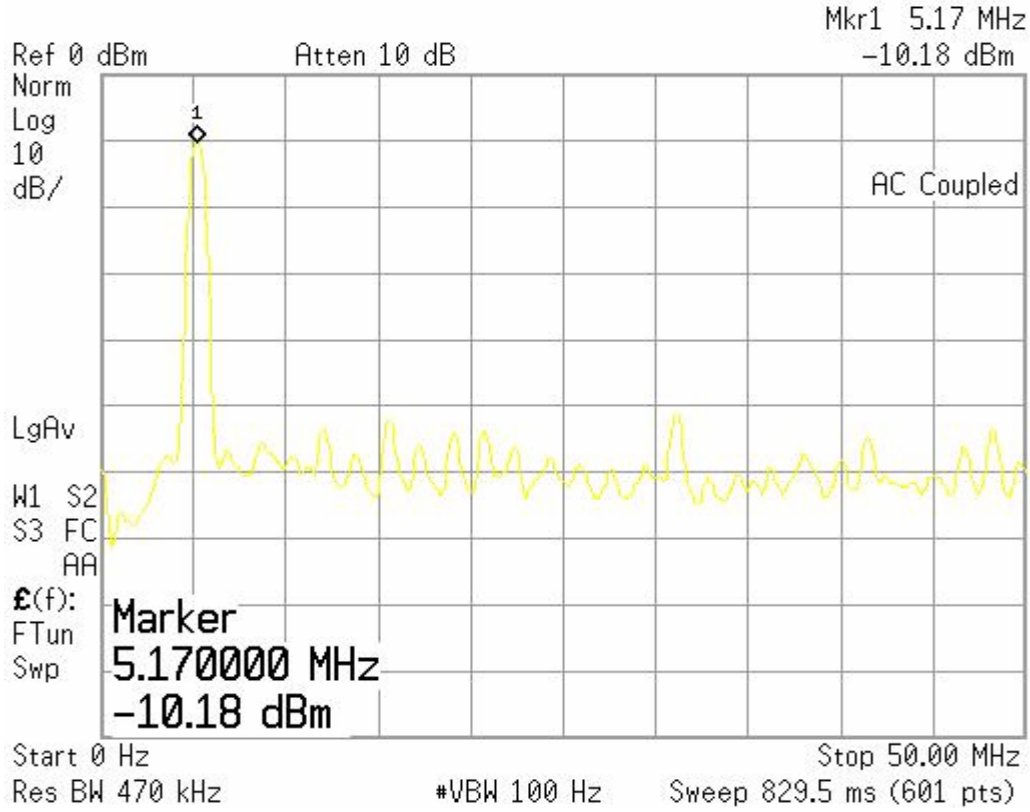


Fig. 5.8 Sine wave spectrum for F_s = 100 MHz and F_{sig} = 5.17 MHz

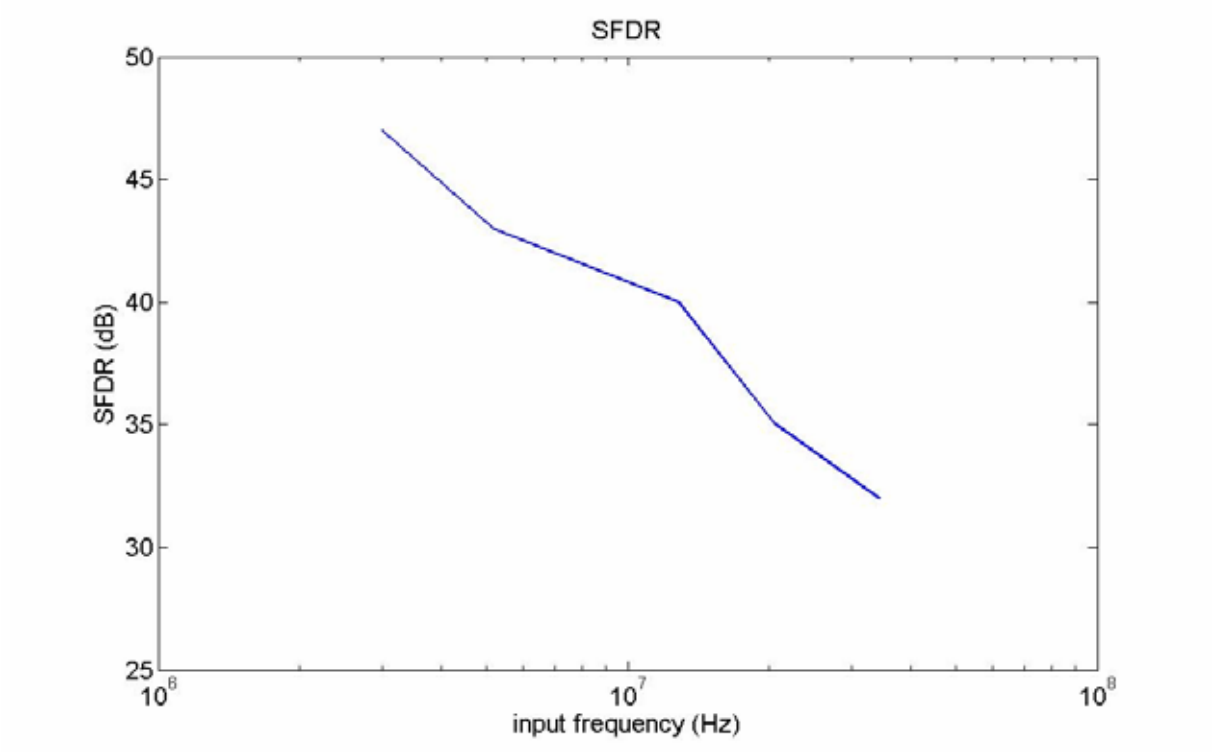


Fig 5.9 The SFDR of input frequency between 3 MHz and 34.33 MHz at the sample rate 100 MHz

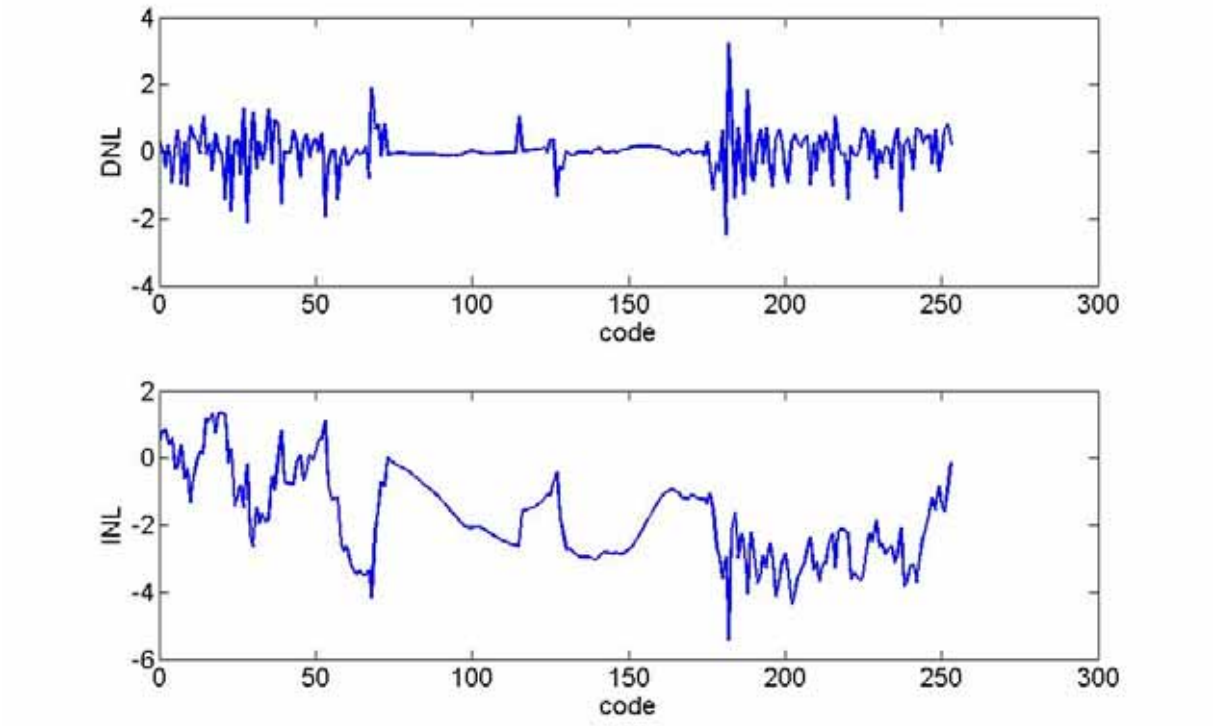


Fig 5.10 The differential nonlinearity (DNL) and integral nonlinearity (INL)

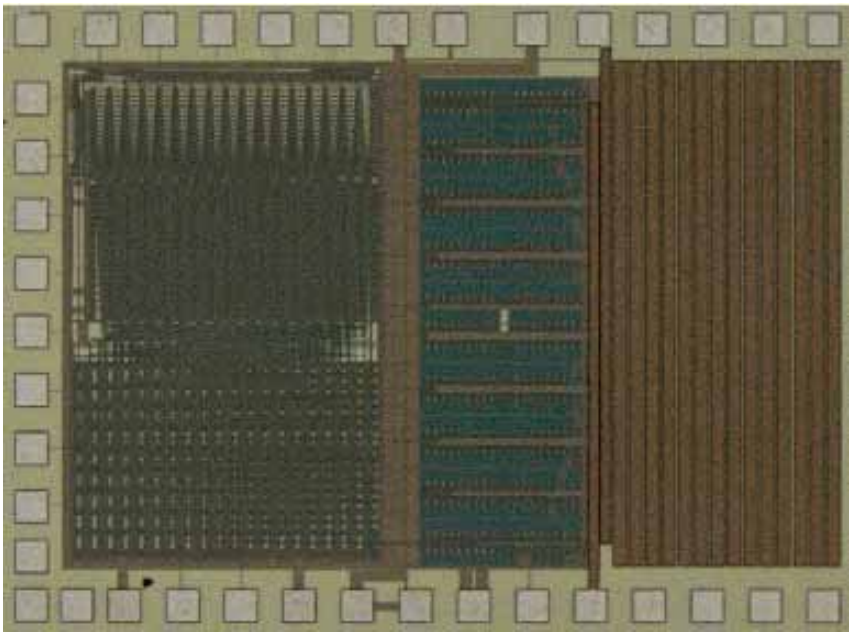


Fig 5.11 The die microphotograph

Table 5-2 The total measurement results of this DAC

Process	TSMC 0.18 μm CMOS Mixed-Signal
Supply Voltage	Digital supply 1.8V Analog supply 3.3V
Sampling Frequency	100 MHz
DNL	< 3.3 LSB
INL	< 5.4 LSB
SFDR(Fin = 3 MHz)	47 dB @ CLK = 100 MHz
Power Dissipation	128 mW
Active Area	1.615 mm^2

Chapter 6

Conclusions and Future Work

In this thesis, the implementation of 12-bit DAC is presented to operate at high update rate. To design a high speed DAC, the current steering architecture is a suitable candidate. But the nonidealities effects of the DAC will affect the overall system performance. The current source is properly designed to reduce the nonlinearity caused by finite output impedance of current source. To overcome the random error and systematic error, the proper area of current source is selected and special layout technique is used. It can improve quadratic error and cancel gradient error. A high speed, low crossing point latch is implemented to compensate the error at the DAC output due to switching in the current cells. The DAC is fabricated by 0.18 μm 1P6M CMOS Mixed-Signal. The active area of the DAC is about 1.615 mm^2 and the total area is about 2.896 mm^2. Besides, the power dissipation is 128 mW. The measure result shows that with the signal frequency of 34.33 MHz at the update rate of 100MHz, the SFDR is 32 dB. The differential nonlinearity and integral nonlinearity are below 3.3 and 5.4 least significant bits (LSB's).

The DAC can be improved from several points of view in the future. First, Several recommendations were proposed for digital signal integrity. Adding buffer is the best way to overcome the heavy load. The drive ability of digital logics should be enhanced to defend the largest parasitic capacitance. We may choose redesign of the latch cell and thermometer coded to achieve the above discussion. Second, due to lack of considering the parasitic loading effect caused by the layout, the post-layout dynamic performance simulation results will be degraded than the pre-layout simulation at high input frequency. Therefore, the DAC should be designed to keep enough margins to endure the loading effect and the floor plan should be modified to decrease the parasitic loading. Finally, the clock should be designed carefully because the current DAC operated at high speed. And pay more attention to routing between circuit blocks. The DAC can be taped out several times and compared the performance by using differential layout methods.

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